Theme B: Energy Harvesting-Aware Computation Circuits

Newcastle University and University of Southampton

Prof Alex Yakovlev (alex.yakovlev@ncl.ac.uk), Prof Bashir Al-Hashimi, Dr Alex Bystrov, Dr Delong Shang, Dr Fei Xia

Harvested energy could be regarded as having an unlimited supply of energy in the long run, but limited power at any time. This theme explores ways of designing circuits which take advantage of these properties.

On-chip reference-free sensing

To properly take advantage of harvested energy the computation circuits must be able to operate efficiently over a large range of Vdd variation. In order to properly control the computation to best track the available energy or power over time, knowledge of these physical parameters is necessary. We developed sensors capable of operating under non-deterministic power supply (e.g. harvested energy), without needing stable references.

Self-timed (asynchronous) SRAM

Memory that can work under radically variable Vdd down to subthreshold levels is difficult to realize. We developed the world's first truly self-timed SRAM in several versions which demonstrates a number of advantages including functionality across large range run time Vdd variations and data retention capability down to very low Vdd.

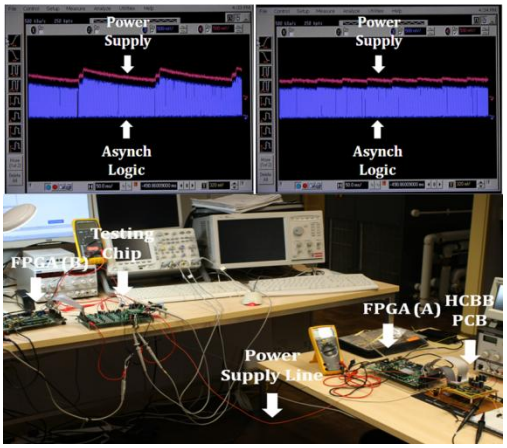

Fig. 1: SRAM and power delivery testing

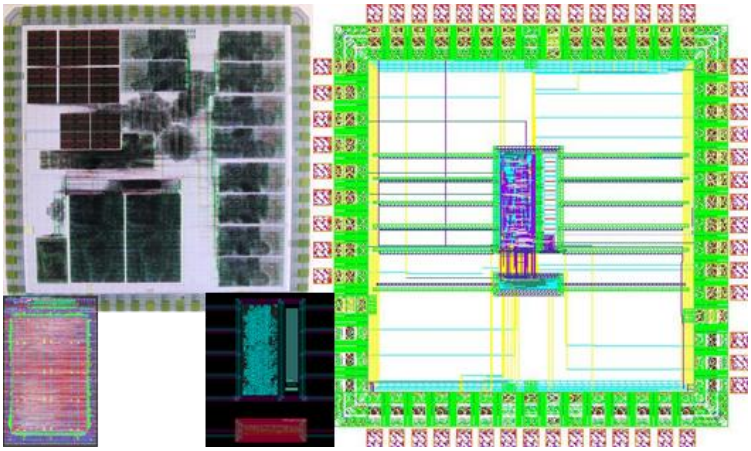

Fig. 2: Sub-clock power gating and async. SRAM chips.

On-chip power delivery

Power flow can be smoothened through storage elements but the usual off-chip solutions with their large capacity and slow operation may not always be necessary. We developed novel on-chip solutions which have been demonstrated to work well under energy harvesting and asynchronous computation assumptions.

Sub-clock power gating

Traditional low power techniques such as voltage and frequency scaling do not target leakage power loss whose relative significance is increasing. Power gating targets this with detaching circuits from Vdd during idle modes, but leakage is not exclusive to idle modes and our novel techniques of sub-clock power gating extends this to active modes. A chip with an ARM Cortex-M0 core was fabricated and tested to demonstrate this method

Publications

see http://www.holistic.ecs.soton.ac.uk/publications.php

R. Ramezani, A. Yakovlev, F. Xia, J. Murphy D. Shang, "Voltage Sensing Using an Asynchronous Charge-to-Digital Converter for Energy-Autonomous Environments", IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 3(1), March 2013, pp.35-44.

X. Zhang, D. Shang, F. Xia, A. Yakovlev, "A Novel Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems", ACM JETC 7(4): 16 (2011).

F. Xia, A. Mokhov, Y. Zhou, Y. Chen, I. Mitrani, D. Shang, D. Sokolov, A. Yakovlev, "Towards Power Elastic Systems through Concurrency Management", IET Computers & Digital Techniques 6(1), January 2012, pp.33-42.

A. Baz, D. Shang, F. Xia, and A. Yakovlev, "Self-Timed SRAM for Energy Harvesting Systems", Proceedings of the 20th international conference on Integrated circuit and system design: power and timing modeling, optimization and simulation (PATMOS'2010), pp.105-115,LNCS 6448, Grenoble, France, September 7-10, 2010.

A. Baz, D. Shang, F. Xia, and A. Yakovlev, "Self-Timed SRAM for Energy Harvesting Systems", Journal of Low Power Electronics, Vol 7, No. 2, pp 274-284, 2011.

R. Ramezani, D. Sokolov, F. Xia, A. Yakovlev, "Energy-modulated quality of service: New scheduling approach," Faible Tension Faible Consommation (FTFC), 2012 IEEE Conference of, pp.1-4, 6-8 June 2012.

X. Zhang, D. Shang, F. Xia, H. S. Low, A. Yakovlev, "A Hybrid Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems", New Circuits and Systems Conference (NEWCAS), 2012 IEEE 10th International, Montreal, Canada, 17-20 June 2012.

R. Ramezani and A. Yakovlev, "Reference Free Voltage Sensing Using an Asynchronous Charge-to-Digital Converter", IDTechEx Energy Harvesting Europe, 15-16 May 2012, Berlin, Germany.

J. Mistry, J. Myers, "An ARM Cortex-M0 for Energy Harvesting Systems: A Novel Application of UPF with Synopsys' Galaxy Platform", SNUG 2012, Silicon Valley, March 2012.

A. Baz, D. Shang, F. Xia, A. Yakovlev, A. Bystrov, "Improving the robustness of self-timed SRAM to Variable Vdds", Proceedings of 21st International Workshop, PATMOS 2011, Madrid, Spain, Sept. 2011, LNCS 6951, Springer, pp. 32-42.

X. Zhang, D. Shang, F. Xia, and A. Yakovlev, "A Novel Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems", Proceedings of 17th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2011), pp. 89-98.

H. S. Low, D. Shang, F. Xia, and A. Yakovlev, "Variation Tolerant AFPGA Architecture", Proceedings of 17th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2011), pp. 77-86 (Best Paper Candidate).

A. Yakovlev, "Energy-Modulated Computing", Design, Automation and Test in Europe 2011 (DATE 2011), Grenoble, France, 14-18 March 2011, pp. 1340-1345.

J. N. Mistry, B. M. Al-Hashimi, D. Flynn, and S. Hill, "Sub-Clock Power-Gating Technique for Minimising Leakage Power During Active Mode", DATE 2011, Grenoble, France, 14-18 March, 2011, pp. 106-111.

Other Resources

see www.holistic.ecs.soton.ac.uk/resources.php)

Energy-modulated computing lecture and SRAM demo videos

Prof Yakovlev's DATE'11 lecture on energy-modulated computing and async SRAM videos are on the Holistic website.