Final report on EPSRC grant "Reliable cell design methods for variable processes" (EP/G066361/1)

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Investigators: Dr Gordon Russell

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Project value: £248,293

The project has made the following contributions to the project's objectives:

1) Evaluation, adaptation and development of simulation tools for the characterisation of variability and optimisation of circuits.
    a. Variability modelling and analysis methods and tools based on DoE and RSM, including studying the effects of process variation on the device, circuit and system architecture levels, M-PRES, VARMA [Shedabale-3, Burns – 12, Ni – 8, 22, 23]
    b. Statistical analysis of the impact of cross-talk on onchip communications in NoCs [Halak - 6]
2) Design of a set of cells suitable for use in a network on chip
    a. Multi-resource arbiter with concurrent service [Golubcovs - 1]
    b. Robust synchronisers (to Vdd variations) and finding tradeoffs between latches and synchronise [Zhou - 4, Alshaikh - 19]
    c. Latches and C-elements robust to SEUs [Juli - 10, AlTarawneh – 17,25]
    d. Logic parameterization in self-timed control circuits robust to variable operating conditions [Mokhov - 14]
    e. Dynamical systems approach to analyse CMOS circuit stability [Syranidis – 22]
3) Development and implementation of an on chip communication link.
    a. Wagging synchronizers and reconfiguration structures robust to variability [Alshaikh - 18,Guido - 20]
    b. Speculative synchronization for low latency [Tarawneh- 7]
4) Measurement of the actual characteristics of the cells produced on chip and derivation of the principles of design that should be used in development of a nanometre cell library.
    a. Sensors for on-chip condition monitoring and Vdd drop detection [Tarawneh - 9, Syranidis - 11]
    b. Improved time amplifier [Alahmadi - 13]
    c. Fault-tolerant NoC based on thresholding [Dai - 5]
    d. 3D structure characterisation and testing [Perry - 21]
5) Speed-independent SRAM
    a. New design and demonstrator chip testing [Baz - 15,16]

PhD Theses (completed):

Basel Halak, The analysis and optimisation of performance and reliability metrics of capacitive links in deep submicron semiconductor technologies, December 2009.

Zyiad Al Tarawneh, The effects of process variations on performance and robustness of bulk CMOS and SOI implementations of C-elements, September 2011.

Pagnaiotis Asimakopoulos, Optimizing the integration and energy efficiency of through silicon via based 3D interconnects, November 2011.

Stanislavs Golubcovs, Multi-resource approach to asynchronous SoC: design and tool support, December 2011.

PhD Theses (passed viva):

Chenxi Ni, Architectural level delay and leakage power modelling of manufacturing process variation, October 2012.

References

1. S. Golubcovs, D. Shang, F. Xia, A. Mokhov and A. Yakovlev. Concurrent Multi-Resource Arbiter: Design and Applications, IEEE Trans. Computers, vol.PP, no.99, pp.1, doi: 10.1109/TC.2011.218, to appear in January 2013.
2. A.N.M. Alahmadi, G. Russell, A. Yakovlev, Time difference amplifier design with improved performance parameters, Electronics Letters, 2012, 48(10), 562-563.
3. S. Shedabale, G. Russell and A. Yakovlev. M-PRES: a statistical tool for modelling the impact of manufacturing process variations on circuit-level performance parameters, IET Circuits Devices Systems, Vol. 5, No.5, pp. 403-410, September 2011. DOI: 10.1049/iet-cds.2010.0110
4. J. Zhou, M. Ashouei, D. Kinniment, J. Huisken, G. Russell and A. Yakovlev. Sub-threshold Synchronizer, Microelectronics Journal, vol. 42, no. 6, June 2011, pp. 840-850.
5. L. Dai, D. Shang, F. Xia and A. Yakovlev, Monitoring circuit based on threshold for fault-tolerant NoC, Electronics Letters, Vol. 46, Issue 14, pp. 984-985, 8 July 2010.
6. B. Halak and A. Yakovlev, Statistical analysis of crosstalk-induced errors for on-chip interconnects, IET Computers & Digital Techniques, Vol. 5, No. 2, pp. 104-112 (March 2011).
7. G. Tarawneh and A. Yakovlev, Adaptive Synchronization for DVFS Applications, PATMOS 2012, Newcastle upon Tyne, Sept 2012, to be published in LNCS, v. 7606, Springer, 2013.
8. Chenxi Ni, Ziyad Al Tarawneh, Gordon Russell and Alex Bystrov. Modelling and Analysis of Manufacturing Variability Effects from Process to System Level, PATMOS 2012, Newcastle upon Tyne, Sept 2012, to be published in LNCS, v. 7606, Springer, 2013.
9. G. Tarawneh, T. Mak and A. Yakovlev, Intra-chip Physical Parameter Sensor for FPGAs using Flip-Flop Metastability, Proc. 22nd Int. Conf. on Field Programmable Logic and Applications (FPL2012), Oslo, Norway, Aug. 2012.
10. N. Julai, A. Yakovlev and A. Bystrov. Error detection and correction of single event upset tolerant latch, IOLTS, 2012, Sitges, Spain, June 2012.
11. I. Syranidis, F. Xia, A. Yakovlev. A reference-free voltage sensing method based on transient mode switching, Proceedings of the 2012 8th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), pp.143-146, Aachen, Germany, 12-15 June 2012.
12. G. Russell, F. Burns, A. Yakovlev, VARMA – Variability Modelling and Analysis Tool, Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2012 IEEE 15th

International Symposium on, Tallinn, pp.378-383, 18-20 April 2012, doi: 10.1109/DDECS.2012.6219091
13. A.N.M. Alahmadi, G. Russell, A. Yakovlev, Reconfigurable time interval measurement circuit incorporating a programmable gain time difference amplifier, Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2012 IEEE 15th International Symposium on, Tallinn, pp.366-371, 18-20 April 2012, doi: 10.1109/DDECS.2012.6219089
14. A. Mokhov, D. Sokolov and A. Yakovlev. Adapting asynchronous circuits to operating conditions by logic parameterisation, Proc. 2012 IEEE 18th Int. Symp. on Asynchronous Circuits and Systems, Copenhagen, Denmark, IEEE Comp. Soc, pp. 17-24, May 2012 (best paper finalist award).
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