Final Report on EPSRC grant "Self-Timed Event Processor" (EP/E044662/1)

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Main areas of achievement:

(1) Foundations and basic modelling techniques for event base processing, analysis, synthesis and tools:

The development of Conditional Partial Order Graphs (CPOGs) [1, 8] is a significant advancement in the formal modelling of microcontrol circuits for specification and synthesis purposes. It is especially beneficial for a class of systems with many behavioural scenarios defined on the same set of primitive events or actions, which includes event processors. As a result of this work several synthesis, verification, optimisation and mapping tools have been developed to facilitate specification and synthesis of microcontrollers using the proposed methodology. The tools have been successfully incorporated into the Workcraft framework for visualisation and simulation support.

Another work in this area is the investigations into policies exemplified by the synthesis of nets with step firing policies [4].

(2) Low Power Event Processor Modelling, Analysis and Design, including accumulate and fire, power-latency tradeoffs

A central topic of this project is low power event processors. In this area, extensive investigations were carried out at all levels of abstraction. These include architectural explorations and analyses using Petri net and Matlab discrete models, detailed studies on the central accumulate and fire method, detailed designs of accumulate and fire components and further explorations on extending the use of the accumulate and fire concept Network on Chip fault monitoring. One important work covers the modelling and analysis of power and latency in systems where tasks are managed through accumulate and fire, exposing power and latency tradeoffs [3, 7]. Accumulate and fire as an event response technique was demonstrated to be an effective and efficient method to manage power, latency, and other important properties such as faults [2].

(3) Multi-client Multi-resource Arbitration and Design of C

Another aspect of event processing is how to deal with multiple nondeterministic incoming events; a simple and elegant solution to this front-line problem is through multi-input arbitration. A substantial body of work on multi-input, multi-resource arbitration was carried out within this project with a number of arbiter solutions obtained [17, 10]. More importantly, methods of designing multi-input arbiters were established to enable maximum concurrency between handshake pairs of clients and resources (previous known asynchronous solutions lacked concurrency between such handshakes), and using fully scalable techniques such as the assembly of matrices of standard tiles [13, 15]. This also led to the concept of virtual delay insensitive design and opened up a potential research direction into asynchronous future generation FPGAs [12].

(4) NoCs and applications to neural processing

With the accumulate and fire method in (2) above providing an effective way of monitoring faults in NoCs, further explorations into fault processing and deadlock detection and control were carried out. Asynchronous communications in NoCs were investigated [5]. Architectures for NoC fault processing and deadlock management were proposed and further research is being actively pursued in this direction [28, 30].

Our work on NoCs was further extended by the development of a connection-centric network architecture for mapping spiking neural networks to NoC's. This is a significant step in the attempt to solving the connectivity problem in the realistic representation of biological neural networks with potential interest to neuroscientists [9, 18]. A chip was successfully designed in this work and fabricated through Europractice resources.

Research output:

Publications generated by this project include journal and conference papers, PhD theses, and a book chapter (full list below).

There are also a fabricated chip [Nerual-NOC in http://async.org.uk/chip-gallery.html] and modelling and synthesis tools incorporated into Workcraft [http://workcraft.org/wiki/doku.php].

Other useful contributions:

The project's supported PhD student, Stanislavs Golubcovs, had a work placement with NEC in the US. During this work, he obtained valuable training as a systems designer and helped foster a close collaborative relationship between NU and NEC. Some knowledge produced in this project was used in consultancy for Elastic Clocks (Spanish/US start-up on commercialising the methods and CAD for desynchronising RTL designs), advising for the start-up iGXL and in a KTA project "ECG Healthcare System on Chip (ECHO)", whose aim is to develop an ultra-low power platform for health-service applications.

Follow-on:

Much of the work in this project is extremely relevant to and helped form the group's work in the Holistic project on energy harvesting, which is a collaboration among four institutions including NU supported by EPSRC funding [EP/G066728/01]. Other directions of work opened up by the work in this project include the power-elastic system design methodology, soft-arbiters, and asynchronous FPGA's based on the concept of virtual delay insensitive blocks.

List of STEP Project Publications

Journal papers:

1. A. Mokhov and A. Yakovlev, Conditional Partial Order Graphs: Models, Synthesis and Application, IEEE Transactions on Computers, to appear in October 2010 (available through "early access" on ieeexplore).
2. L. Dai, D. Shang, F. Xia and A. Yakovlev, Monitoring circuit based on threshold for fault-tolerant NoC, Electronics Letters, Vol. 46, Issue 14, pp. 984-985, 8 July 2010.
3. Y. Chen, F. Xia, D. Shang, and A. Yakovlev, Fine-grain stochastic modelling of dynamic power management policies and analysis of their power–latency tradeoffs, IET Software, Vol.3, Iss.6, pp. 458-469, Dec.2009
4. P. Darondeau, M. Koutny, M. Pietkiewicz-Koutny, and A. Yakovlev. Synthesis of Nets with Step Firing Policies, Fundamenta Informaticae, Vol. 94, No.3-4, pp. 275-303, IOS Press, 2009.

Chapters in books:

5. S. Golubcovs and A. Yakovlev. Asynchronous Communications for NoCs, Chapter 4 in C. Silvano, M. Lajollo, and G. Palermo "Low Power Networks-on-Chip", Springer Verlag, October 2010, ISBN 978-1-4419-6910-1

PhD theses:

6. S. Dasgupta, Formal Design and Synthesis of GALS Architectures, PhD Thesis, Newcastle University, March 2008.
7. Y. Chen, High Level Modelling and Design of a Low Power Event Processor, PhD Thesis, Newcastle University, January 2009.
8. A. Mokhov, Conditional Partial Order Graphs, PhD Thesis, Newcastle University, September 2009.
9. R. Emery, PhD thesis on NoC structures for spiking neural networks, Newcastle University, near completion.
10. S. Golubcovs, PhD thesis on arbitration, Newcastle University, being written up.

Refereed conference papers:

11. Andrey Mokhov, Arseniy Alekseyev, and Alex Yakovlev, Automated Synthesis of Instruction Codes in the Context of Micro-architecture Design, Proc. Tenth Int. Conference on Application of Concurrency to System Design (ACSD'10), 21-25 June 2010, Braga, Portugal, Ed. Luis Gomes, V. Khomenko and J.M. Fernandes, IEEE CS Press, June 2010, pp. 3-12 (**Best paper award**).
12. Delong Shang, Fei Xia, Alex Yakovlev, Asynchronous FPGA Architecture with Distributed Control, Proc. 2010 IEEE International Symposium on Circuits and Systems (ISCAS'10), pp.1436-1439, May 30th - June 2nd 2010, Paris, France.
13. Delong Shang, Fei Xia, Alex Yakovlev, Highly Parallel Multi-Resource Arbiters, Proc. 2010 IEEE International Symposium on Circuits and Systems (ISCAS'10), pp.4117-4120, May 30th - June 2nd 2010, Paris, France.
14. Yuan Chen, Isi Mitrani, Delong Shang, Fei Xia, Alex Yakovlev, Stochastic Analysis of Power, Latency and the Degree of Concurrency, Proc. 2010 IEEE International Symposium on Circuits and Systems (ISCAS'10), pp.4129-4132, May 30th - June 2nd 2010, Paris, France.
15. D. Shang, F. Xia, S. Golubcovs, and A. Yakovlev, The magic rule of tiles: virtual delay insensitivity, In Proc. of PATMOS 2009, Delft, The Netherlands, September 2009.

16. Mokhov, V. Khomenko and A. Yakovlev. Flat Arbiters, Proc. Ninth Int. Conference on Application of Concurrency to System Design, 1-3 July 2009, Augsburg, Germany, Ed. S. Edwards, R. Lorenz and W. Vogler, IEEE CS Press, July 2009, pp. 99-108
17. S. Golubcovs, D. Shang, F. Xia, A. Mokhov and A. Yakovlev, Modular Approach to Multi-Resource Arbiter Design, Proceedings of the 15th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC'09), Chapel Hill, NC, USA, May 2009, IEEE CS Press, pp. 107-116.
18. R. Emery, A. Yakovlev and G. Chester, Connection-Centric Network for Spiking Neural Networks, Proceedings of the 3rd ACM/IEEE International Symposium on Networks-on-Chip (NoCs 2009), San Diego, CA, USA, May 2009, IEEE, pp. 144-152.
19. S. Dasgupta and A. Yakovlev, Desynchronization techniques using Petri nets, Proceedings of the Fourth Workshop on Globally Asynchronous, Locally Synchronous Design (FMGALS 2009), Ed. S. Shukla and J.-P. Talpin, DATE'09 Friday workshop, Nice, France, April 2009, pp. 73-89 (to appear in Electronic Notes in Computer Science).
20. Y. Chen, F. Xia, D. Shang, and A. Yakovlev. Fine Grain Stochastic Modelling and Analysis of Low Power Portable Devices with Dynamic Power Management. In: A. Argent-Katwala, N.J. Dingle and U. Harder (Eds.): UKPEW 2008, Imperial College London, DTR08-9, pp. 226-236, http://ukpew.org.
21. P. Darondeau, M. Koutny, M. Pietkiewicz-Koutny, and A. Yakovlev. Synthesis of Nets with Step Firing Policies, in: K.M. van Hee and R. Valk (Eds.), Applications and Theory of Petri nets, Proc. 29th In. Conference Petri nets 2008, Xi'an, China, June 2008, LNCS 5062, Springer, pp. 112-131 **(Best Paper Award)**.
22. J. Carmona, J.Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. A Symbolic Algorithm for the Synthesis of Bounded Petri Nets, in: K.M. van Hee and R. Valk (Eds.), Applications and Theory of Petri nets, Proc. 29th In. Conference Petri nets 2008, Xi'an, China, June 2008, LNCS 5062, Springer, pp. 92-111.
23. K. Gorgônio and F. Xia, Modeling and Verifying Asynchronous Communication Mechanisms using Colored Petri Nets, in: J. Billington, Z. Duan, and M. Koutny (Eds), ACSD 2008, Proc. 2008 8th Int. Conf. on Applicatioon of Concurrency to System Design, June 2008, Xi'an, China, IEEE Press, pp. 138-147.
24. Mokhov and A. Yakovlev, Verification of Conditional Partial Order Graphs, in: J. Billington, Z. Duan, and M. Koutny (Eds), ACSD 2008, Proc. 2008 8th Int. Conf. on Applicatioon of Concurrency to System Design, June 2008, Xi'an, China, IEEE Press, pp. 128-137.
25. Yakovlev, D. Sokolov and I. Poliakov, Self-timed Circuit Design: Stepping from Control to Data Path, Proceedings of Workshop Concurrency Methods, Issues and Applications (CHINA 2008), Xi'an, China, June 2008, pp. 35-40 (also registered as Tech Report CS-TR-1102 of School of Computing Science, Newcastle University) **(invited talk)**.
26. Mokhov and A. Yakovlev. Conditional Partial Order Graphs and Dynamically Reconfigurable Control Synthesis, Proceedings of DATE'08, Munich, March 2008, pp. 1142-1147.
27. D. Shang, C.H. Shin, P. Wang, F. Xia, A. Koelmans, M.H. Oh, S. Kim, and A. Yakovlev, Asynchronous Functional Coupling for Low Power Sensor Network Processors, Nadine Azémard, Lars J. Svensson (Eds.): Integrated Circuit and System Design. Power and Timing Modeling, Optimization and Simulation, 17th International Workshop, PATMOS 2007, Gothenburg, Sweden, September 2007, Proceedings. LNCS 4644, ISBN 978-3-540-74441-2, pp. 53-63.

Non-refereed conference papers:

28. R. Al-Dujaily, T. Mak, F. Xia, and A. Yakovlev, A Methodology for Deadlock Detector Minimization in Interconnection Network, UK Electronics Forum (UKEF 2010), Newcastle, June-July 2010.

29. M. Rykunov, A. Mokhov, A. Yakovlev, A. Koelmans, Automated Generation of Control Logic for Processor Architectures, UK Electronics Forum (UKEF 2010), Newcastle, June-July 2010.
30. Raaed Al-Dujaily, Li Dai, Fei Xia, Delong Shang and Alex Yakovlev, NoC Monitoring Infrastructure: A Supervisory and Control Service, 21st UK Asynchronous Forum, Bristol, Sept. 2009.
31. Li Dai, Raaed Al-Dujaily, Fei Xia, Delong Shang and Alex Yakovlev, Network-on-Chip Monitoring and Diagnostic System, 21st UK Asynchronous Forum, Bristol, Sept. 2009.
32. Yu Zhou and Alex Yakovlev, Dynamic Concurrency Reduction for Power Management, 21st UK Asynchronous Forum, Bristol, Sept. 2009.
33. Andrey Mokhov, Ulan Degenbaev and Alex Yakovlev, Synthesis of Instruction Codes in the Context of Asynchronous Microcontrol Design, 21st UK Asynchronous Forum, Bristol, Sept. 2009.
34. Mokhov, A. Yakovlev, Introduction to Conditional Partial Order Graphs, 5thh UK Embedded Forum, Leicester, Sept 2009.
35. Y. Chen, F. Xia, D. Shang, A. Yakovlev, Stochastic Modeling of Dynamic Power Management Policies and Analysis of Their Power-Latency Tradeoffs, 4th UK Embedded Forum, Southampton, 9-10 Sept 2008.
36. Stanislavs Golubcovs, Andrey Mokhov and Alex Yakovlev. Multi-resource Arbiter Design, 0th UK Asynchronous Forum, Manchester, September 2008.
37. Andrey Mokhov and Alex Yakovlev. Synthesis of multiple rail phase encoding circuits, 20th UK Asynchronous Forum, Manchester, September 2008.
38. Robin Emery, Alex Yakovlev and Graeme Chester. Dense-Near/Sparse-Far Hybrid Reconfigurable Neural Network Chip, 20th UK Asynchronous Forum, Manchester, September 2008.
39. Andrey Mokhov and Alex Yakovlev, Conditional Partial Order Graphs and Dynamically Recongurable Control Synthesis, 19th UK Asynchronous Forum, London, September 2007.