Device Modelling for Bendable Piezoelectric FET-Based Touch Sensing System

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***Abstract*— Flexible electronics is rapidly evolving towards devices and circuits to enable numerous new applications. The high-performance, in terms of response speed, uniformity and reliability, remains a sticking point. The potential solutions for high-performance related challenges bring us back to the time-tested silicon based electronics. However, the changes in the response of silicon based devices due to bending related stresses is a concern, especially because there are no suitable models to predict this behavior. This also makes the circuit design a difficult task. This paper reports advances in this direction, through our research on bendable Piezoelectric Oxide Semiconductor Field Effect Transistor (POSFET) based touch sensors. The analytical model of POSFET, complimented with Verilog-A model, is presented to describe the device behavior under normal force in planar and stressed conditions. Further, dynamic readout circuit compensation of POSFET devices have been analyzed and compared with similar arrangement to reduce the piezoresistive effect under tensile and compressive stresses. This approach introduces a first step towards the systematic modeling of stress induced changes in device response. This systematic study will help realize high-performance bendable microsystems with integrated sensors and readout circuitry on ultra-thin chips (UTCs) needed in various applications, in particular, the electronic skin (e-skin).**

***Index Terms*— Flexible Electronics, POSFET, Interfacing Circuit, e-Skin, Tactile Sensing, Device Modeling**

I. Introduction

The field of flexible and printed electronics has received considerable interest in recent years and is seen as the future of electronics, as also indicated by electronics industry roadmap [1]. So far, the progress in this field has mainly come through organic semiconductors and various printing and stamping techniques [2-5]. The devices from organic semiconductors gain from the inherent mechanical flexibility, but due to poor charge carrier mobility of these materials (~1 $cm^2/V.s$ (maximum reported ~43 [6]) cf. ~1000 $cm^2/V.s$ for single crystal Si) the devices are slow. Factors such as large channel lengths (>20μm cf. <100nm in deep submicron technology [5]) of printed devices is another reason why these devices are slow. The high-performance in terms of device response, speed, uniformity, reliability, and stability are critical for flexible electronics to address the fast computation and communication needs of many emerging applications such as e-skin in robotics, smart cities, and internet of things. For example, in robotics the feedback from tactile skin over the body should be fast enough (<milli sec) for quick action [7-10]. For these reasons, recently the field of flexible electronics has seen renewed interest in silicon, with devices and circuits made from transfer printed silicon nanowires (NWs) and ultra-thin chips (UTCs) [11, 12]. A hybrid mix of circuits from inherently flexible materials like organic polymers and inorganic semiconductors in new forms such as NWs and UTCs will be an interesting development [12]. This will also benefit from advances such as 3D integrated circuits (ICs) and heterogeneous integration.

Irrespective of the material and circuits are made from, they exhibit stress-induced variations in response when they are bent. For example, in tactile skin, or e-skin, the electronics are required to conform to 3D surfaces, and this means electronics should bend [13, 14]. The bending of electronics in this case (and in many other applications) induces stress on the devices, which results in deviation or alteration of the performance from the designed values [15, 16]. A few attempts made to include stress-induced effects in device models are mainly related to strained silicon devices [17-19]. This paper reports advances in this direction through our research on bendable piezoelectric oxide semiconductor field effect transistors (POSFET) and the associated interface circuitry. This paper extends our work reported in [20], where we presented the analytical model of POSFET devices using the piezoelectric capacitor model and the underlying physics related to metal-oxide-semiconductor Field Effect Transistors (MOSFETs). This extended paper compliments the analytical model of POSFETs with Verilog-A model to describe their behavior under normal force and stressed conditions. The focus is on the characteristics of stressed POSFET devices and their electro-mechanical response. The cancellation of the stress induced changes in the response of the readout circuit, due to tensile and compressive stress, has been studied along with the

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use of mobility enhancement to alter the sensitivity of the sensor under bent conditions. The results presented in this paper include the first approach towards a systematic analysis of the response of planar and stressed on-chip conventional configuration of POSFET devices with arrangements, such as source follower, differential op-amp and chopper amplifier.

This paper is organized as follows: A brief description of the state-of-the-art related to various flexible electronics device modelling schemes is given in section II. The structure and working of POSFET devices is presented in section III. A detailed discussion of the analytical model of POSFET is given in section IV. This section also includes the Verilog-A model, which defines the behavior of planar and stressed POSFET. Section V presents various on-chip circuit implementation for POSFET device in planar, compressive and tensile stress and their simulation results. Finally, the major outcomes are summarized in Section VI.

II. State of the Art of Bendable Device Modelling

Devices and circuits on flexible substrates get stressed when they, or their substrate, are bent and this results in major changes in the parameters, such as charge-carrier mobility, threshold voltage etc. It is important to understand how these parameters change so as to ensure the reliable functioning of circuits on flexible substrates when they are bent. A circuit designer should be aware of potential shifts in behavior of devices due to mechanical stress or strain – which may be because of bending during their use, or other factors such as fabrication related stress. The bending induced stress is known to affect the performance of CMOS solid-state sensors in terms of offset voltage and sensitivity [15, 21].

The external stress also changes the energies between the conduction and valence band, by shifting the energy spectrum, which is reflected as a change of the charge carrier mobility [22]. The is also termed as the piezoresistive effect, which should be considered while designing circuits on UTCs [23]. The advanced MOS compact models available today can be used to account for layout-induced stress effects, but they are insufficient to handle bending related large stress [24].

To model this effect, two approaches have been explored in literature. The first approach defines charge carrier mobility of a device as a function of strain and then uses the modified mobility with standard equations in simulation tools like Verilog-A [25]. In this case, total mobility is expressed as:

$$\mu_n^{tot} = \sum_{i=1}^{3} p^{(i)} . \mu_{n,str}^{(i)} \quad (1)$$

where $p^{(i)}$ is the relative population of each conduction valley and $\mu_{n,str}^{(i)}$ strain dependent mobility for the i^{th} valley. The term $\mu_{n,str}^{(i)}$ is expressed as:

$$\mu_{n,str}^{(i)} = \frac{\beta . \mu^L}{1+(\beta-1).h^{(i)}+\beta.\left(\frac{\mu^L}{\mu^{LI}}-1\right)} . m_{(i)}^{-1} \quad (2)$$

where, $m_{(i)}^{-1}$ is the scaled effective mass tensor for the i^{th} valley, μ^L is the lattice mobility, μ^{LI} is the lattice mobility which takes into account the scattering due to doping, β is a function of strain in silicon, and $h^{(i)}$ is a physical parameter, details of which are given in [26]. This approach is mostly used to study the effect of bending on standalone devices. The second approach involves using the changes in energy levels, and could also be used to study circuit performance on flexible or bendable substrates. Modern compact models such as BSIM4 usually provides a set of parameters related to material, like band gap, bulk mobility, work function, electron affinity etc., which affect the electrical characteristics [27]. However, the requirement of a priori knowledge of stress values and dependence on material parameters makes the above mentioned approaches inconvenient for circuit designers. Therefore, in the presented work, we have used the analytical equations along with Verilog-A, to investigate the effect of bending on the performance of single POSFET devices and associated readout circuits.

The impact of piezo-resistive effect can be minimized by: (a) surface structural arrangement, such as fabricating the devices and circuits in the neutral plane of overall structure, (b) suitable layouts which are stress independent, and (c) dynamic circuit compensation methods. For example, if a priori information is available about the orientation of stress, then the circuits could be designed along the crystal axis experiencing minimum effects of bending. However, if stress appears arbitrarily then the fabrication process corner needs to be wider to ensure proper functioning of circuit [28]. A full compact, and Cadence environment friendly model has been reported recently to compensate the effect of piezoresistive effect in CMOS based bendable hall sensor [16]. A few works using basic compensation circuits such as inverters and ring-oscillators etc. have been reported, as well as to mitigate the bending related deviations in device performance [29]. The structural arrangement to mitigate the stress related effects include depositing an encapsulation layer on top of the device in such a way that the device appears on a neutral plane where there is no strain. However, there are practical difficulties for realizing electronics in the neutral plane, especially when then top surface is required to be open to receive external stimuli. A combination of the above approaches could perhaps offer better solution.

III. Bendable POSFET Touch Sensor Device

A. POSFET Device Structure

POSFET devices make a key building block of our e-skin related research [30]. The detailed design and various implementations of planar POSFET devices have been reported in our previous works [13, 14, 31]. However, a short description is given here for quick reference. The structure of POSFETsis similar to Ferroelectric Random Access Memory (FeRAM) device, where a stack of ferroelectric material and gate oxide is used as the gate dielectric. The read and write operations of FeRAMs are governed by the voltage applied over the ferroelectric material [32]. In POSFETs, a piezoelectric material lies between the gate electrode of underlying MOS device and the top metal as shown in Fig.1. In other words, the device structure can be defined as a piezoelectric capacitor coupled to gate electrode of MOSFET [14].

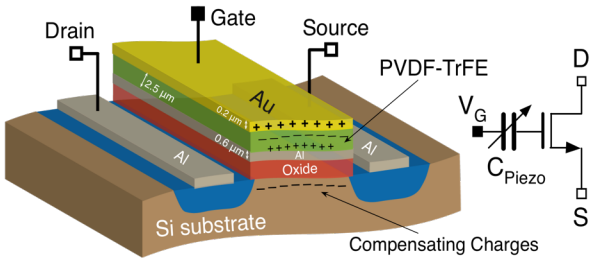


Figure.1. Illustration of bendable POSFET.

The piezoelectric material by its virtue produces charge when pressed and this is given by the constituting equation as [33]:

$$D_{33} = d_{33}\, T_3 + \varepsilon_{33}^{T} E_3 \qquad (3)$$

where D is the electric displacement, T is the mechanical stress, E is the electric field, ε_{33} is the dielectric constant under constant stress, and d_{33} is the piezoelectric constant in thickness mode. The charges produced by piezoelectric effect modulate the channel current, which is then used to quantify the applied force. Various piezoelectric materials such as PZT, AlN, and PVDF etc. could be used to make the piezoelectric layer of POSFETs. PZT shows a high piezoelectric coefficient but the presence of lead makes it less attractive for many applications, especially those related to biomedical field. AlN is a good alternative, but it exhibits low piezoelectric coefficient and needs high temperature for sintering, which makes it difficult to use when materials such as aluminum are used for interconnections. Also, challenges in ensuring the crystal orientation (002) during deposition makes AlN less attractive. Therefore, in POSFETs we have used piezoelectric polymer, P(VDF-TrFE), which has moderate piezoelectric coefficient, easy and low temperature processing and inherent mechanical flexibility.

POSFET devices provide high-performance, thanks to the silicon based CMOS technology. Like silicon based solid-state sensors, POSFETs have high speed, better sensitivity and excellent integration with readout and signal conditioning electronics [14]. Moreover, it can be miniaturized to obtain high spatial resolution and can be advanced towards system on chip. However, the intrinsic rigid and brittle nature of silicon substrate limits their placement to planar surfaces only.

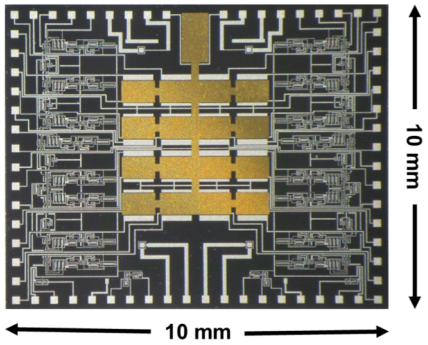


Figure. 2. Optical image of fabricated tactile sensing chip using CMOS technology.

B. Design and Tactile Sensing Chip Layout

The new design of POSFET based touch sensing system is influenced by human tactile spatial resolution. For example, in fingertips we need high density of sensors (to achieve 1 mm tactile acuity [10]) and therefore we have designed a 4 × 4 array of sensors. Each sensor has channel length of 12 µm and channel width of 3276 µm to achieve high aspect ratio of 273. The total active area is 0.36 cm^2 and overall chip size is1cm × 1cm, as shown in Fig. 2.

The tactile sensing chip fabrication is based on NMOS technology, using *p*-well in *n*-type wafer, single metal and single poly. Serpentine shape of gate is chosen to accommodate this high channel width in a compact active area of 750 µm x 1000 µm per device. After transistor fabrication, the piezoelectric layer is spin coated from a solution prepared by dissolving P(VDF-TrFE) pellets in RER500 solvent. This is followed by annealing of piezoelectric layer in nitrogen ambient at 150^{o}C. After the top metal (i.e. gold) is evaporated. The P(VDF-TrFE) is then selectively dry etched using oxygen plasma from areas not covered by gold. Finally, the processed wafers are thinned down using anisotropic wet etching to obtain bendable POSFET chips.

IV. Analytical and Verilog-A Model

A simple analytical model is presented here to define the output and transfer characteristic equations of POSFET. A Verilog-A model is also developed to investigate the response of tactile sensing device for a wide range of applied forces (0-2N) under planar, and stressed condition.

A. Analytical model

One of the most important process during fabrication of POSFET is poling - the process of aligning the dipoles along a preferred direction. This is done by applying high electric field

across the piezoelectric layer. Before poling, the dipoles are randomly oriented in the polymer and no piezoelectricity is observed. In presence of high electric field, carbon-fluorine and carbon-hydrogen covalent bonding rotate around the main chain of the polymer molecule, leading to the effect of piezoelectricity in molecule [34, 35]. With suitable steps, such as grounding all metal layers underneath the piezoelectric layer, the impact of poling on devices could be avoided [13, 36]. The effect of poling on electrical characteristics of POSFET is investigated here through new mathematical model. This model combines the hysteresis property of piezoelectric polymer with standard MOSFET equations. To calculate the amount of polarization charges due to applied electric filed, Miller et al [37], have proposed simple equation which relates the polarization charges to the electric field.

These equations are:

$$P^{+}(E) = P_s tanh\left(\frac{E-Ec}{2\delta}\right) + \varepsilon_F \varepsilon_o E \tag{4}$$

where,
$$\delta = E_c \left(ln\left(\frac{1+\frac{P_r}{P_s}}{1-\frac{P_r}{P_s}}\right)\right)^{-1} \tag{5}$$

$$P^{-}(E) = -P^{+}(-E) \tag{6}$$

Here, P_s is saturation polarization, which is the maximum polarization charge achieved during the process of poling. This can be extracted from the level at which hysteresis loop saturates. P_r is remnant polarization, the polarization charge left when electric field is removed after poling. E_c is the coercive field at which the polarization changes their polarity. $P^{+}(E)$ and $P^{-}(E)$ denotes positive going (lower) branch and negative-going (upper) branch of hysteresis curve, respectively.

During poling, the switching polarization, P_{sw}, is developed in the polymer. P_{sw} is the amount of polarization switched from one remnant polarization state to the maximum polarization state of the opposite polarity. With transistor underneath the piezoelectric layer, the P_{sw} results in creation of an extra layer of charge in the semiconductor channel to maintain charge neutrality. These extra charges can be termed as compensation charge, P_{comp}, and can be written as:

$$P_{comp} = P_{sw} = P_r + P_s \tag{7}$$

Thus, after poling there is a fixed amount of charge present at oxide-semiconductor interface which results in changes of the flat band voltage. The flat band voltage of transistor is defined as the difference between the gate metal work function, $\emptyset_M$, and the semiconductor workfunction $\emptyset_s$, and is expressed as:

$$V_{FB} = \emptyset_M - \emptyset_s \tag{8}$$

This change leads to either increase, or decrease in the flat band voltage depending on the poling direction. In case of POSFET devices, poling is done by applying positive voltage on the top metal and keeping the gate metal at ground. This condition creates a layer of negative charges at the oxide-semiconductor interface and so the flat band voltage for n-MOSFET decreases, and can be expressed as:

$$V_{FB\_eff} = V_{FB} - \left(\frac{P_s + P_r}{C_{ox}}\right) \tag{9}$$

The threshold voltage of transistor is directly related to the flat band voltage according to the following equation:

$$V_{th} = V_{FB} + 2\emptyset_F + \frac{\sqrt{2\epsilon_s N_a (2\emptyset_F + V_{SB})}}{C_{ox}} \tag{10}$$

where, $\emptyset_F$ is the fermi potential, and N_a is the doping concentration of bulk silicon. A change in the flat band voltage results in a change in the threshold voltage, which can be written as:

$$V_{th\_eff} = V_{th} - \left(\frac{P_s + P_r}{C_{ox}}\right) \tag{11}$$

After quantifying the change in threshold voltage due to poling, and taking into account the overall device capacitance, which is the in series combination of the polymer capacitance and oxide capacitance, the characteristic current equation of POSFET in linear and saturation region can be written as:

$$I_{ds} = \begin{cases} \mu_n C_{stack}\left(\frac{W}{L}\right)\left\{\left(V_{gs} - V_{th_{eff}}\right)V_{ds} - \left(\frac{1}{2}\right){V_{ds}}^2\right\} \\ \mu_n C_{stack}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th_{eff}}\right)^2 \end{cases} \tag{12}$$

Where $\frac{1}{C_{stack}} = \frac{1}{C_{ox}} + \frac{1}{C_{PVDF}}$

Both parts of Eq. (12) are simulated in MATLAB, using the parameters given in Table I, and plotted against the experimental measurements performed over the device with channel width 3276 µm and length 12 µm, as shown in Fig.3.

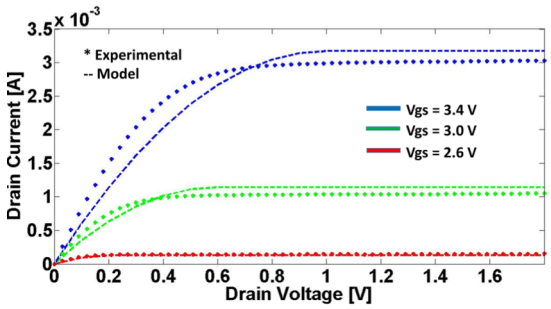
The reasonable match with the experimental values observed in output characteristics, validates the proposed analytical model. The minor deviation observed in transfer characteristics between the simulated and experimental results could be attributed to the change in charge distribution in the polymer upon biasing the top metal. The polarization charge distribution in piezoelectric polymer depends upon the voltage applied across it (Eq. (4)) and at higher gate voltages this charge affects the channel region minority carriers. Since this dynamic behavior is not included in the model, we observe the deviation.

TABLE I
VALUES USED IN THE PROPSED MODEL

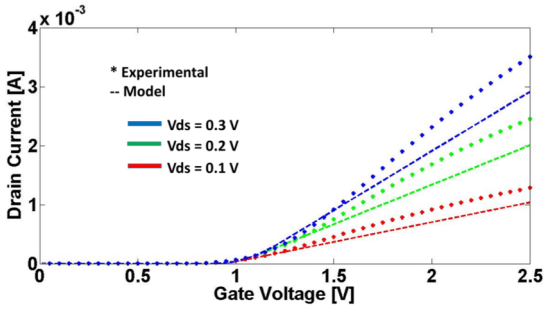
Symbol	Parameter	Value
W	Channel Width (μm)	3276
L	Channel Length (μm)	12
μ	Carrier mobility ($cm^2/V.s$)	850
t_{ox}	Oxide thickness (nm)	45
t_{pvdf}	PVDF thickness (μm)	2.5
ε_{pvdf}	Permittivity of PVDF	12
ε_{ox}	Permittivity of oxide	3.9
P_r	Remnant polarization (nc/cm^2)	33
P_s	Saturation polarization (nc/cm^2)	13
E_c	Coercive field (kV/cm)	160
V_{th}	Threshold voltage (V)	1.5

B. Verilog-A model

The physico-mechanical model described in the previous



(a)



(b)

Figure. 3. (a) Characteristic curves of POSFET at different gate voltages, and (b) transfer curves of POSFET at different drain voltages.

subsection could be adapted to fully characterize the POSFET devices [20]. Starting from these physical models we have implemented a general macro-model in Verilog-A. We have considered the standard 0.18-µm CMOS technology in our model implementations. To this end, POSFET was considered to comprise of two fully uncoupled stages: an electro-mechanical stage (i.e. P(VDF-TrFE) capacitor) where it is assumed that in bent condition the area of contact between the stimuli and the sensor remains the same, and so the charge produced due to piezoelectric layer remains unchanged. The second stage is the electronic stage which is underlying MOSFET experiencing bending stress. However, this assumption does not follow the condition of charge neutrality of the POSFET structure, given by:

$$\sigma_I + \sigma_P + \sigma_s = 0 \tag{13}$$

where σ_I, σ_P, and σ_S are the charge densities at the interface of gate electrode - piezoelectric polymer, in the bulk of the piezoelectric polymer, and in the semiconductor, respectively. Usually σ_s is much smaller than σ_I and σ_{P_S}, and constant with respect to the applied force, and therefore Eq. (13) reduces to:

$$\sigma_I + \sigma_P = 0 \tag{14}$$

With this the electronic stage can be considered as fully uncoupled from the electro-mechanical stage.

The formulated approach discussed in previous sections leads to the POSFET equivalent macro-model shown in Fig. 4(a). The capacitors C_{PVDF} and C_{ox} can be written as the equivalent capacitor C_{stack}, defined as:

$$C_{Stack} = \frac{C_{PVDF}C_{OX}}{C_{PVDF}+C_{OX}} \tag{15}$$

On the application of force, the piezoelectric layer accumulates charge according to Eq. (3), which can be approximately written as:

$$Q = d_{33}F \tag{16}$$

The new dipoles will align according to the bias voltage polarity, resulting the creation of a potential (φ_{Force}) which changes the effective gate voltage of the transistor, i.e.

$$\varphi_{Force} = \frac{d_{33}F}{C_{PVDF}} \tag{17}$$

From Eq. (17) it is clear that the potential φ_{Force} can be modelled as a linear voltage-controlled voltage source, with its value depending both on the applied force and the capacitance C_{PVDF}.

The macro-model has been defined as two sub-circuit blocks presented in Fig. 4(b), showing the outer connections, where V_{bias}, G', G, D, B, S stand for the bias voltage applied to the top electrode, the connection towards the gate of the MOSFET, the gate, the drain, the bulk, and the source of the strained MOSFET, respectively.

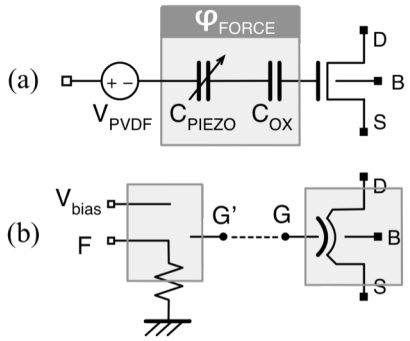


Figure. 4. (a) POSFET macro-model structure, and (b) Strained POSFET Verilog-A sub-circuit blocks and external connections.

The terminal F stands for the independent applied force source, modelled by a voltage source connected to a dummy resistor. This voltage is used to control the potential φ_{Force} of the macro-model. The voltage difference created during this event is given by Eq. (17) and affects the gate voltage of transistor which can be written as:

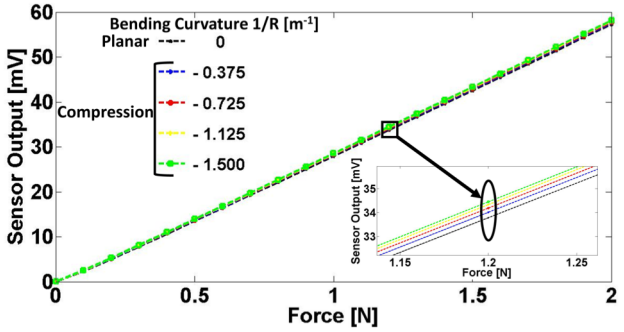
$$V_{gs_{eff}} = V_{gs} + \frac{d_{33}F}{C_{pvdf}} \tag{18}$$

Assuming the device working in saturation region and when force is applied, the change in current can be written as:

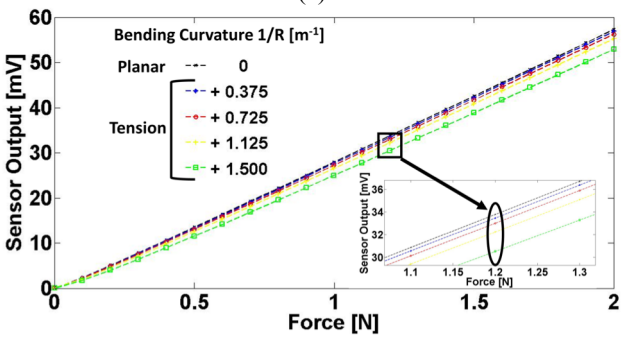
$$\Delta I_{ds} = \mu_n C_{stack}\left(\frac{W}{2L}\right)\left(V_{gs_{eff}} - V_{th_{eff}}\right)^2 - \mu_n C_{stack}\left(\frac{W}{2L}\right)\left(V_{gs} - V_{th_{eff}}\right)^2 \tag{19}$$

Due to change in the current, the output voltage of the device changes proportionally with the applied force, as is shown in Fig. 5.

As explained in Sec. II, the bending–induced stress in silicon chip changes the electronic transport properties, and the channel resistivity changes as well [38]. This is eventually reflected as a change in drain current. The threshold voltage changes proportionally with the applied stress and a gain of more than 50% in electron mobility can be expected in the case of uniaxial stress applied to Si-crystal. In this work, compressive as well as tensile stress has been applied, which leads to an increase and decrease in the drain current of the transistor, respectively. This eventually shows up as an increase, or decrease, in the output voltage of the source follower configuration, as is shown in Fig. 5.



(a)



(b)

Figure. 5. Response of planar and strained POSFET to dynamic force using different (a) compressive and (b) tensile bending stresses.

The change of the sensitivity of the stressed POSFET device varies between 1% and 7% with respect to its planar counterpart. This shows that bendability of sensors not only allow them to conform to the curved surfaces, but also improves their performance under appropriate conditions.

V. Towards Stress-Independent Sensing Circuitry

Nullifying, or minimizing the mechanical stress effects on the active sensing devices and circuits requires an accurate and systematic simulation study. Stress affects the transistor's performance and consequently varies the output signals of the analog and digital circuit building blocks. Furthermore, in CMOS-compatible sensors, such as piezoelectric pressure, temperature, chemical/biological, or other sensors, stress introduces offsets that affect the sensitivity and detection of static and low frequency environment signals. In order to fabricate ICs that function within specifications, both planar as well as during mechanical deformation, the effects of stress must be considered in the design process. This section presents some techniques such as correlated double sampling (CDS) and chopper amplifier circuits to dynamically cancel the piezo-resistive effects due to mechanical stress. These techniques help us obtain a stress-independent operation of sensor interface in bendable electronic systems.

Various applications have different set of requirements which lead to varied specifications. In some cases, the range of force experienced by the sensor is not defined and hence we need the sensor to maintain reliable functionality in a wide range of applied contact force. For this reason, in past we biased the POSFET device in common drain mode, popularly known as source follower configuration [14, 39]. The major advantages of this configuration are simplicity, stability and predictability with very high input impedance and low output impedance. In case of POSFETs, the gate is floating and the sensor is biased using constant current source. The force is applied using shaker which presses the sensor with sinusoidal varying signals [36]. Since the current is constant, the voltage at the source follows the input. Because of less than unity gain, the POSFET sensor could be used for wide force range.

However, when the sensor output voltage is restricted by the available voltage line, the range of applied force is limited. In other words, for limited voltage the sensitivity can be adjusted as per the desired force range. For example, in e-skin for robots the preferred range is set by the human daily sensing range (0.1-1 N) [10]. The output voltage produced for this range of force should be within the maximum voltage available from the supply over robot.

Considering these conditions, we have proposed a new operational amplifier circuit configuration where one of the differential pair transistors has been replaced with POSFET model in the positive input[40]. This nullifies the noise, common to both input transistors, and rescues the signal difference by directly measuring the input terminals. Using a differential pair configuration, we can also reduce the environmental noise entering at the output. Furthermore, the differential type amplifiers allow dynamic cancellation to reduce any change in response, due to the piezoresistive effect and circuit noises etc. using techniques, such as chopper stabilization and correlated double sampling[41].

Fig. 6(a) shows the simplified block diagram of the proposed microsystem. This scheme employs the bendable MOS transistors implemented by Verilog-A description using the parameters extracted from a standard 0.18-µm CMOS technology. The transistor model predicts the performance of device under stress, and makes it easy to obtain bendable large-scale integrated circuit.

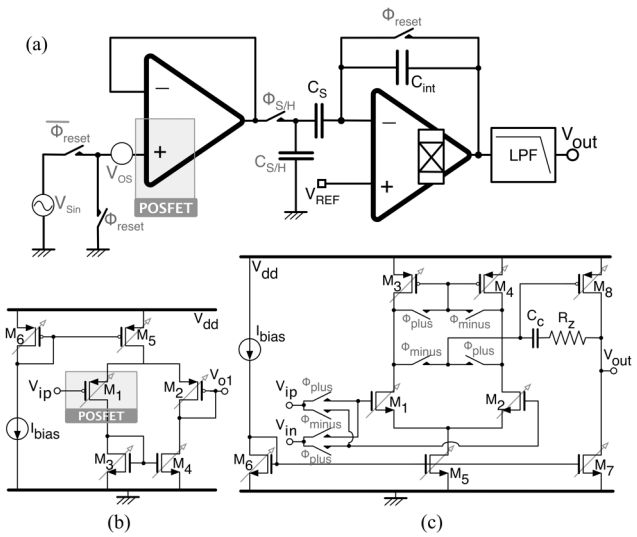


Figure. 6. (a) Block diagram of the proposed readout circuit for POSFET microsystem. (b) Schematic diagram of the POSFET biasing as voltage follower, and (c) Schematic circuit diagram of two stage single-ended amplifier.

Based on the theoretical concepts and experimental results from literature related to the piezoresistive effect, and the observed behavior of the tested transistors, the drain current is modified due to mobility variation and threshold-voltage parameters in the BSIM4 model [19]. Two parameters are defined in the MOS models in order to perform simulations: the radius of curvature (R) from -1.5 to 1.5 m and the stress orientation (θ) between 0° and 90° versus wafer crystal direction. The thickness of wafer, h = 500 µm, and the Young's modulus for silicon, E ≅ 169 GPa has been considered in model [42].

The proposed scheme utilizes the POSFET in a differential pair as a positive input transistor to configure a voltage follower, as shown in Fig. 6(b). In order to sense the applied force, the output voltage (V_{o1}), which is equal to the surface potential of the bottom electrode, is acquired. The circuit functions as follows: When the POSFET op-amp is configured as voltage follower, any difference in input stage gets amplified at the output. So whenever the sensor experiences some contact force stimulus (while the other transistor remains at fixed bias voltage) the amplified difference appears at the output. The entire readout employs the CDS technique to reduce the amplifier's offset and noises due to piezoresistive effects of uniaxial bending stress, as well as to lower the effect of the finite amplifier gain.

A chopper amplifier is considered as a modulation approach to further cancel the input-referred noises including 1/f and offset [43]. Fig. 6(c) shows the two stage chopper amplifier with chopping frequency of 40 kHz, which has been employed in the integrator. In order to avoid output buffers, a switched-capacitor, used as low pass filter (LPF), has been used to drive the output pins [44].

The readout circuit has been designed in a standard 0.18-µm CMOS technology. In this design, POSFET bias circuit is biased with external current source of value 1µA, and chopper amplifier bias current is 10 µA with 1.8 V. A sinusoid input signal with amplitude of 2mV corresponding to the applied force has been used on the top electrode of piezoelectric layer. On application of force, input at the POSFET terminal changes, which is then amplified by the circuit. This amplification can be tuned so that the output remains below the maximum voltage value.

Fig. 7 shows the timing diagram and waveforms of the input and output of the POSFET readout circuit. Resetting frequency and chopping clock frequency have been set to 1.25 kHz and 40 kHz, respectively.

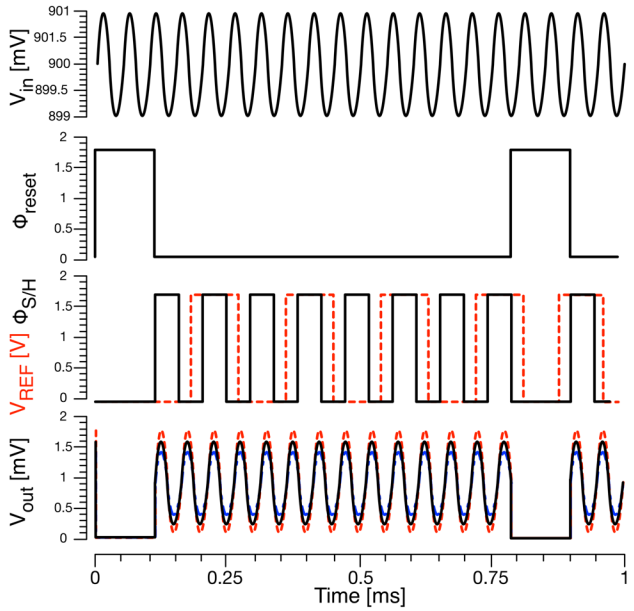


Figure. 7. Simplified timing diagram of a complete readout operation with transient response of output voltage. Black line shows the output voltage in planar state, where the red and blue dotted lines show the transient response under compression and tension, respectively.

The proposed circuit is also simulated under compression and tension by using the Verilog-A model for POSFET and MOS transistors. In this case study, we considered small bending curvature to introduce stress in the circuit. Simulation of the POSFET with readout circuit shows a maximum 12.5% increase in peak-to-peak voltage for compression (bending curvature = -1.5 m^{-1}) and a maximum 9% reduce in peak-to-peak voltage for tension (bending curvature = +1.5 m^{-1}).

VI. Conclusion

With flexible electronics gaining interest, the need for high-performance has also gained prominence. In this regard, silicon based flexible electronics is being explored and the work presented here is one example. For designing of electronics on flexible silicon it is also important to advance the circuit design tools by developing new models. The investigations in this paper about response of POSFET devices in presence of stress is a step in that direction. The presented analytical and Verilog-A model have been used to fully characterize the device for electrical and mechanical responses for a wide range of applied forces, showing a variation in the sensitivity of the stressed POSFET device between 1% and

7% with respect to its planar counterpart. Further, the effects of stress on the readout circuit have been analyzed and techniques to dynamically minimize the piezo-resistive effect due to mechanical stress have been presented. In the simulations, different radii of curvature and stress orientations have been used, showing a maximum increase of 12.5% in peak-to-peak voltage for compressive stress, and a maximum decrease of 9% in peak-to-peak voltage for tensile stress. Future work will be focused on the investigation of the response of the readout circuit using different stresses at different MOS models of the circuit, introducing also the effects of bending in the electro-mechanical stage of the Verilog-A POSFET macro-model.

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