High Efficiency Bias Stabilisation for Resonant Tunneling Diode Oscillators

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***Abstract*— We report on high efficiency, high power and low phase noise resonant tunneling diode (RTD) oscillators operating at around 30 GHz. By employing a bias stabilization network which does not draw any direct current (DC), the oscillators exhibit over a 10-fold improvement in the DC-to-RF conversion efficiency (of up to 14.7%) compared to conventional designs (~0.9%). The oscillators provide a high maximum output power of around 2 dBm, and low phase noise of -100 dBc/Hz and -113 dBc/Hz at 100 kHz and 1 MHz offset frequencies, respectively. The proposed approach will be invaluable for realizing very high efficiency, low phase noise and high-power millimeter-wave (mm-wave) and terahertz (THz) RTD-based sources.**

***Index Terms*— Bias stabilisation, high frequency oscillators, negative differential resistance (NDR), resonant tunneling diode (RTD)**

I. Introduction

HIGH FREQUENCY sources are a key building component of many modern electronic systems and therefore their design is of paramount importance. For millimetre wave (mm-wave) and terahertz (THz) oscillators, those based on the resonant tunnelling diode (RTD) are being actively researched for a variety of applications including short range multi-gigabit wireless links and imaging [1]-[4]. They are also being deployed in mm-wave radar sensors for a variety of applications [5]. Advantages of RTDs include the facts that they are extremely broadband with fundamental oscillations up to 1.98 THz recently reported [6], operate at room temperature, are compact, consume low power and the output power is easily modulated though the bias network.

In our recent work, we have reported RTD oscillators with record output powers in the 0.5-1mW range up to 300 GHz [7]-[10]. We have used this technology to demonstrate 15 Gbps wireless links using W-band RTD oscillators [4], and now developing such links for future wireless data centres [11]. The technology has the potential to underpin emerging new applications requiring short range high capacity wireless links such as virtual gaming, wireless memory sticks, etc. Part of the appeal for RTDs is in their simplicity, e.g. a 1 mW J-band source requires only a single RTD device realised using just photolithography [10], whilst transistor technologies such as CMOS require an array of 8 or more (active) devices, sub-100 nm high resolution lithography and advanced circuit design techniques [12]. Also, RTDs can provide highly efficient electronic sources beyond about 300 GHz, frequencies that cannot generally be easily covered by any transistor technologies today [13].

The basis of the RTD oscillator is the negative differential resistance (NDR) region of its current-voltage (*I-V*) characteristic. Since the NDR exists right from DC, RTDs are affected by instability when biased in this region resulting in unwanted parasitic bias oscillations. If present, these reduce oscillator output power [14], [15]. The conventional approach to eliminate the bias oscillations in planar RTD oscillators uses a shunt resistor across the RTD so that the combined *I-V* characteristic remains positive in the NDR region of the device [16]. Using this method in RTD oscillators however greatly reduces the DC-to-RF conversion efficiency to under 1% by providing a dc path to ground through the usually low value resistance, typically ~10 Ω) [7], [17]. Many earlier RTD oscillators were implemented in rectangular waveguide technology and used a lossy section of transmission line to minimise bias oscillations, and so had limited efficiency [19]. Therefore, approaches to improve efficiency could have a major impact with regards to the adoption of the technology, especially for portable devices where battery capacity is at a premium.

To improve the DC-RF conversion efficiency of NDR (tunnel-diode) oscillators, a non-linear resistor (Schottky diode) was used instead of a linear resistor to reduce the dc power consumption of the stabilizing resistor [18]. The dc power consumption was reduced by a factor of 3-6 using this approach. In [15], an integrated Schottky diode was used but this approach is limited to only RTD epitaxial designs for which the forward voltage drop of the Schottky diode lies within the NDR of the device, which is often not the case and so the

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approach has limited applicability. Another approach to provide dc stabilization of an RTD is the use of large shunt capacitance [19]. Even though this would not impact the dc current consumption, its implementation in an oscillator circuit is not always possible due to the large capacitor value required (typically in the pF-μF range) as this would take up a large chip area in an integrated circuit realisation. Nonetheless, this approach has been employed in an RTD wavelet generator circuit in which a gated RTD oscillator works in pulsed mode [20], with the technology forming the basis of commercially available mm-wave radar sensors [5].

In this paper, we report a new RTD oscillator implementation that enables over a 10-fold increase in DC-RF conversion efficiency. Specifically, conventional RTD oscillator designs exhibiting less than 1% efficiency are re-designed to achieve over 10 % efficiency, with this being only limited by the employed RTD epitaxial design. The new approach replaces the shunt bias stabilisation resistor in the conventional designs with a shunt series resistor-capacitor (RC) network, thereby sharply reducing the dc power requirements but without compromising the oscillator performance. Therefore, the proposed approach could lead to very high efficiency high frequency oscillators.

The paper is organised as follows: Section II describes the RTD epitaxial design, the device characteristics and discusses the new bias stabilisation approach. Section III describes the oscillator design and fabrication, while Section IV the oscillator characterisation and a discussion of the achieved results. Conclusions are given in Section V.

II. RTD DEVICE

A. RTD device structure and characteristics

The RTD epitaxial layer structure in this work consisted of a very low energy bandgap (E_g) material, InAs (indium arsenide, E_g = 0.36 eV), sandwiched between a low bandgap material, $In_{0.53}Ga_{0.47}As$ (indium gallium arsenide, E_g = 0.71 eV), which was in turn sandwiched between two high bandgap barriers AlAs (aluminium arsenide, E_g = 2.15 eV), making up a double barrier quantum well (DBQW) structure. The structure is completed by an un-doped and/or lightly doped $In_{0.53}Ga_{0.47}As$ spacer layer, an n-type emitter/collector layer and a highly doped contact layer. The complete epitaxial layer structure is shown in Table I and was adapted from [21]. It provides a large peak to valley current ratio (PVCR) and low peak voltage, which are essential device characteristics for high performance oscillator design.

The epitaxial wafer was grown by a commercial supplier using molecular beam epitaxy (MBE) on a semi-insulating InP substrate. The RTD device sizes were chosen as large as possible for high RF output power and to meet bias stability requirements as described in [22]. Micron-sized 4×4 μm^2 RTD devices were fabricated by optical lithography techniques. The mesa size was defined by H_3PO_4:H_2O_2:H_2O wet etching, while the passivation was done using polyimide PI-2545, a low dielectric constant material. The measured IV characteristic is shown in Fig. 1. From this, the peak current density and the peak-valley current ratio of the RTD are 2.18 mA/μm^2 and 5.83 respectively, and the voltage span of the NDR region, ΔV, is approximately 0.65 V, while the peak to valley current difference, ΔI, is 27 mA. The maximum RF power of an oscillator using this device can be estimated using the equation ($(3/16)\,\Delta V\,\Delta I$)) [23] and is approximately 3.3 mW. The device self-capacitance, C_n, comprises the geometrical capacitance and the quantum well capacitance and was estimated using the approach in [4] to be 125 fF.

TABLE I
RTD EPI-LAYER DESIGN

Layer number	Thickness (Å)	Composition	Doping (cm^{-3})	Description
1	450	$In_{0.53}Ga_{0.47}As$	3E19 : Si	Collector
2	800	$In_{0.53}Ga_{0.47}As$	3E18 : Si	Sub-Collector
3	500	$In_{0.53}Ga_{0.47}As$	5E16 : Si	Space II
4	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
5	11	AlAs	Un-doped	Barrier
6	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
7	14	InAs	Un-doped	Sub-Well
8	11	$In_{0.53}Ga_{0.47}As$	Un-doped	Well
9	11	AlAs	Un-doped	Barrier
10	20	$In_{0.53}Ga_{0.47}As$	Un-doped	Spacer
11	500	$In_{0.53}Ga_{0.47}As$	5E16 : Si	Spacer II
12	800	$In_{0.53}Ga_{0.47}As$	3E18 : Si	Sub-Emitter
13	200	InP	1E19 : Si	Etch Stop
14	4000	$In_{0.53}Ga_{0.47}As$	3E19 : Si	Emitter
15	2000	InP	Un-doped	Buffer
		SI : InP		Substrate

The measured *I-V* characteristic in the NDR region is distorted into the typical plateau-like feature due to the presence of parasitic oscillations during measurement. An analytical model of the *I-V* was derived by fitting the measured data in the PDR (positive differential resistance) regions using a large signal-based model [24], with the NDR region approximated with a smooth trace as shown in Fig. 1. From the modelled *I-V*, the device's differential conductance was computed and is also shown in Fig. 1 (blue trace). The device has a maximum negative differential conductance G_n value of -70 mS. The series resistance of the RTD can be estimated from standard TLM (transmission line method) measurements. The measured Ohmic contact resistance was 128 Ω-μm^2 for the collector (top) contact layer. So, for the 4×4 μm^2 RTD, the device resistance is approx. 9 Ω. The cut-off frequency of the device was estimated from the device equivalent circuit parameters (C_n, G_n, and contact resistance) [19] and/or from the electron dwell time within the quantum well and the electron transit time through the spacer layer [25] and which for this structure is around 480 GHz.

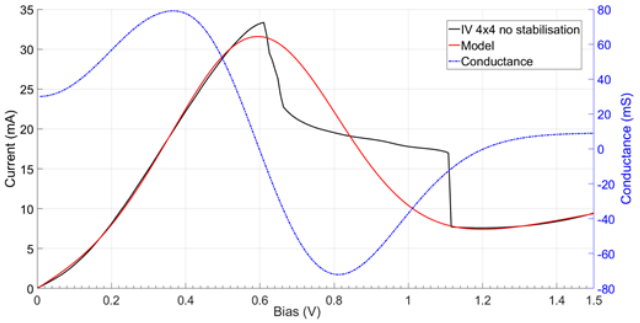


Fig. 1. Measured and modelled *I-V* characteristic of the 4 μm × 4 μm RTD device from the epi-structure in Table I. The peak voltage is at (0.62 V, 33 mA), the valley voltage at (1.27 V, 6 mA). The device conductance derived from the modelled *I-V* is also shown (blue trace).

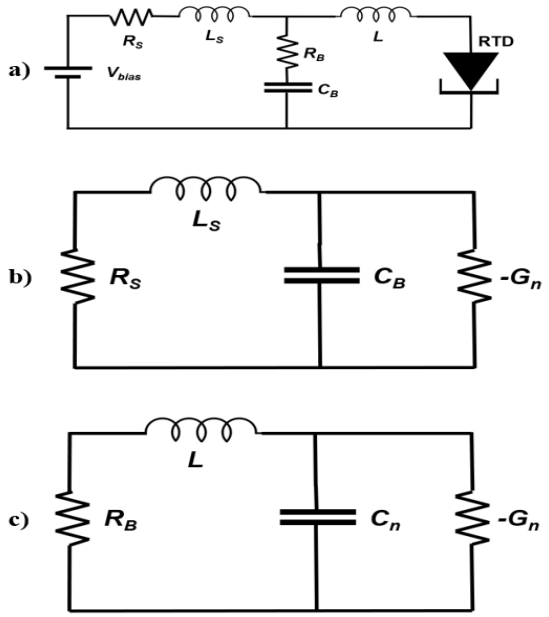


Fig. 2. a) Proposed stabilisation circuit for RTD device, where V_{bias} is the bias voltage, R_S and L_s are the parasitic introduced by the biasing network, R_B and C_B are the shunt stabilising resistor and capacitor and L is the inductance of the CPW line. b) Low frequency equivalent circuit, L is considered a short and the impedance of R_B is ignored c) High frequency equivalent circuit, L_S is considered an open circuit and the capacitance C_B is a short circuit.

B. Stabilising circuit and its characterisation

The RTD bias stabilisation network approach presented in this paper employs the addition of a shunt capacitor C_B connected in series with the stabilising resistance, to eliminate the dc path to ground. The circuit is shown in Fig. 2 (a), where V_{bias} is the bias voltage to set the device in the NDR region, R_S and L_S are the resistance and inductance introduced by the biasing cable, R_B and C_B are the shunt resistor and capacitor, respectively, and L is the series inductance of the contact pads of the device. This stabilisation network was used earlier by the authors for the direct characterisation of the NDR region of tunnel diodes under stable non-oscillatory conditions [26]. It is being employed in high efficiency RTD oscillator realisation for the first time in this paper.

For low frequencies (MHz range), the circuit in Fig. 2 (a) can be simplified to the equivalent circuit in Fig. 2 (b), where the RTD is represented by its negative differential conductance ($-G_n$) and self-capacitance (C_n). In this case, the inductance L is considered a short circuit, R_B is ignored since the impedance of capacitor C_B becomes dominant and the device capacitance C_n (typically tens of femtofarads) is considered negligible when compared with C_B (typically tens of picofarads). On the other hand, at high frequencies (GHz range), the circuit in Fig. 2 (a) can be simplified to the equivalent circuit in Fig. 2 (c), where the inductance L_B is considered an open circuit and the capacitance C_B is a short circuit. Note that the circuits in Fig. 2 (b) and 2 (c) are identical, only with different element values. We analyse the circuit in Fig. 2 (b) using nodal analysis by applying Kirchoff's current law to give:

$$\frac{V}{R_S+sL_S} + sC_BV - G_nV = 0 \tag{1}$$

where V is the voltage across the parallel circuit and s the complex frequency. From (1), we obtain the following characteristic equation:

$$C_BL_Ss^2 + (C_BR_S - L_sG_n)s + 1 - G_nR_s = 0 \tag{2}$$

The solutions to (2) are given by:

$$s = \frac{(L_sG_n - C_BR_S) \pm \sqrt{(C_BR_S - L_sG_n)^2 - 4C_BL_S(1-G_nR_S)}}{2C_BL_S} \tag{3}$$

The roots of (3) can be classified in 2 possible cases.
Case 1: the solutions are complex and therefore:

$$(C_BR_S - G_nL_s)^2 - 4C_BL_s(1 - G_nR_s) < 0 \tag{4}$$

For the circuit to be stable, the solutions of (3) must fall on the left half of the complex frequency plane. As a result, the circuit is stable if:

$$R_S > \frac{L_SG_n}{C_B} \quad \text{or} \quad C_B > \frac{L_SG_n}{R_S} \tag{5}$$

Case 2: the solutions are real and so:

$$(C_BR_S - G_nL_s)^2 - 4C_BL_s(1 - G_nR_s) > 0 \tag{6}$$

For these solutions to fall in the left half of the complex frequency plane the magnitude of the term under the square root sign of (3) must be smaller than the magnitude of the first term, so:

$$R_s < \frac{1}{G_n} \tag{7}$$

Combining the conditions derived from case 1 and 2, the condition to achieve low frequency circuit stability is:

$$\frac{L_SG_n}{C_B} < R_s < \frac{1}{G_n} \tag{8}$$

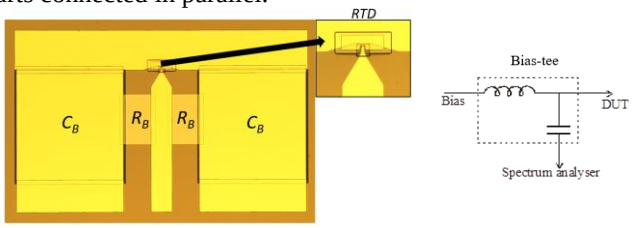
Since the circuits of Fig. 2 (b) and Fig. 2 (c) are identical, equation (8) can be re-written with the corresponding elements to provide the condition for stability at high frequencies as:

$$\frac{LG_n}{C_n} < R_B < \frac{1}{G_n} \tag{9}$$

From (5), (8) and (9), the chosen values of the R_B and C_B were 10 Ω and 144 pF, respectively. Here, R_S and L_S were approximated to be 2 Ω and 900 pH, respectively. L_S was assumed to be dominated by the bias-T inductance. C_n was 125 fF and G_n was -70 mS as earlier noted.

To determine the efficacy of the proposed bias stabilisation approach, devices with and without bias stabilisation were fabricated. The resistor R_B was realised with thin film nichrome (NiCr) deposition. The integrated capacitor (C_B = 140 pF) was realized as a metal-insulator metal (MIM) capacitor with a thin 75nm Si_3N_4 dielectric layer deposited by inductively coupled plasma (ICP) chemical vapour deposition (CVD), while the RTD was realised as earlier described. A micrograph of the fabricated device having the RC stabilising network is shown in Fig. 3. Due to the used CPW (coplanar waveguide) pad

configuration, both R_B and C_B were realised from 2 identical parts connected in parallel.



a) b)

Fig. 3 a) Micrograph of a fabricated 4 μm x 4 μm RTD device with an integrated stabilising network. Inset shows actual RTD. The capacitor C_B and resistance R_B are each realized from two parts and are placed in parallel with the RTD. b) Setup for measuring bias oscillations using a bias tee. The DUT (device under test) is either an un-stabilised or stabilised RTD device.

Bias oscillations for an individual un-stabilised RTD device were first characterised using a spectrum analyser, see Fig. 3 (b). The device was biased in the NDR region through the dc port of the bias tee with the spectrum analyser connected to the RF port and the DUT (device under test) to the DC+RF port. Fig. 4 shows the measured bias oscillations whose frequency is determined largely by the connecting coaxial cable, bias tee inductance and the device capacitance, and lie in the 2-3 MHz range for fundamental oscillations (black trace). This experiment was then repeated for RTD devices with the conventional shunt resistor bias stabilisation (red trace) and the other with the shunt series RC bias stabilisation (blue trace). No bias oscillations are observed for the stabilised devices.

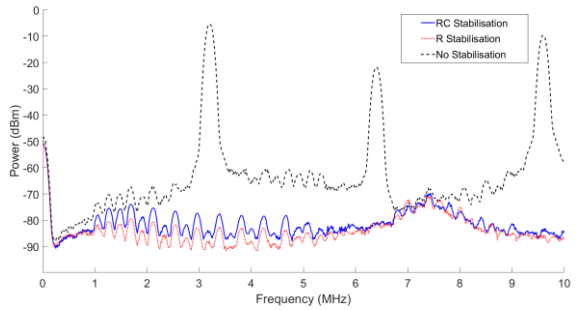
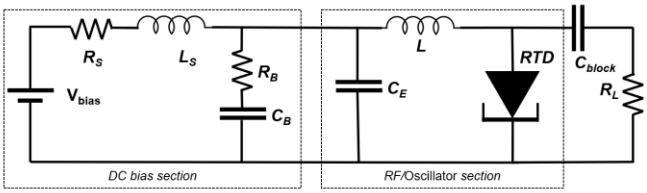


Fig. 4 Measured spectrum on bias lines at V_{bias} = 0.8 V, i.e. in the NDR region for 4×4 μm^2 RTD devices with and without stabilisation (dashed black line). No bias oscillations detected for both shunt resistor (red trace) and shunt series resistor-capacitor stabilisation (blue trace)

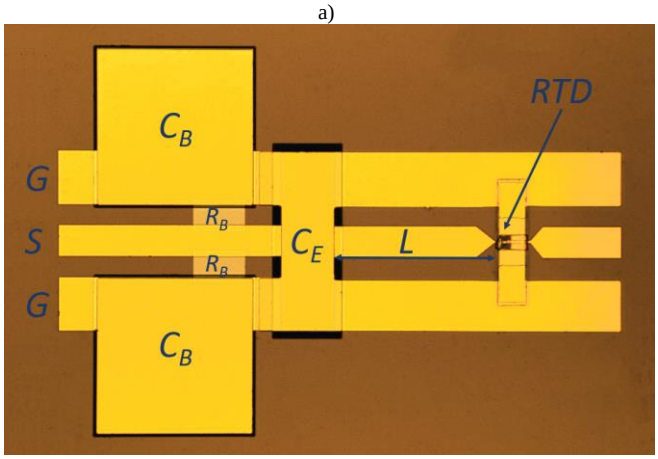
III. RTD Oscillator Design & Fabrication

The schematic diagram of the oscillator circuit employing the high efficiency bias stabilisation network is shown in Fig. 5 (a). It also employs a decoupling capacitor C_E (30pF) which was added to create a short circuit path for the RF oscillator signal, and so avoid the loss of RF power in the stabilising network. At low frequencies C_E and C_B are in parallel (R_B is ignored) and can be combined, and so the analysis described in section II is applicable. The inductance L is realised as a short-circuited coplanar waveguide (CPW) and along with the device capacitance determines the oscillation frequency. The value for L was 140 pH in our design for the ~30 GHz oscillators. This was realised with a CPW transmission line that was terminated with capacitor C_E (which acts as an RF short circuit at the oscillation frequency). The choice of the oscillation frequency of around 30 GHz was to facilitate easier circuit realisation and characterisation to demonstrate the proposed bias stabilisation concept.

The RTD and passive components were fabricated as earlier described. The complete MMIC (monolithic microwave integrated circuit) fabrication process is described in [8]. R_L is the load resistance introduced by the spectrum analyser which is 50 Ω with a coaxial dc block in between. A micrograph of the fabricated oscillator circuit is shown in Fig. 5 (b). The overall size of the oscillator circuit was around 1000×700 μm^2.



a)



b)

Fig. 5 a) The schematic circuit of an oscillator employing a resistor and capacitor stabilisation network (R_B, C_B). The section in the dashed rectangle as realized as MMIC (monolithic microwave integrated circuit). b) Micrograph of the fabricated RTD oscillator with an integrated stabilising network. For measurement, a GSG probe is used. The capacitor C_B and resistance R_B are split in two and placed in parallel with the RTD. The capacitor C_E acts as a short to ground for the RF signal.

The same measurements that are described by Fig. 4 were carried out on the oscillator circuit and no low frequency parasitic oscillations were observed.

IV. Measurement Results

The MMIC RTD oscillator frequency was measured on-wafer using an Agilent E4448A spectrum analyser (3 Hz – 50 GHz). The measured spectrum is shown in Fig. 6 (a). When the bias voltage is 0.94 V the RTD oscillates at 34 GHz with an output power of 3.95 dBm. The dc current was 18 mA and so the DC-to-RF conversion efficiency was 14.7%. This compares well to the estimated maximum oscillator power from the device's NDR region of 3.3mW (5.18 dBm), i.e. theoretical DC-to-RF efficiency of around 19.5%. For this measurement setup, the insertion loss of the probe, dc block and cable between the oscillator and the spectrum analyser was measured to be 3.4 dB, 5.4 dB and 5.46 dB at 25 GHz, 30 GHz and 35 GHz, respectively, and was corrected from the reported results. For an RTD oscillator employing only a 10 Ω shunt resistance for

stabilisation, the dc current was 100 mA and the DC-to-RF conversion efficiency was 0.93 %. This low efficiency is clearly due to the dc power that is dissipated through the low value shunt resistance.

The phase noise of the RTD oscillators was also measured and a typical result is plotted in Fig. 6 (b). At 100 kHz and 1 MHz offset frequency, the phase noise values were −100.2 dBc/Hz and −112.9 dBc/Hz, respectively. The values are comparable with an RTD oscillator stabilised with a shunt resistor realized on the same wafer. The measured low phase noise is consistent with our earlier results [7] and is key to applications such as wireless communications or radar. Fig. 7 shows the oscillator spectrum and output power measurements at different bias levels for the high efficiency oscillator. It has a tuning range of about 7 GHz and high output power of around 1-2 dBm across most of this range, corresponding to efficiencies of around 6-10%.

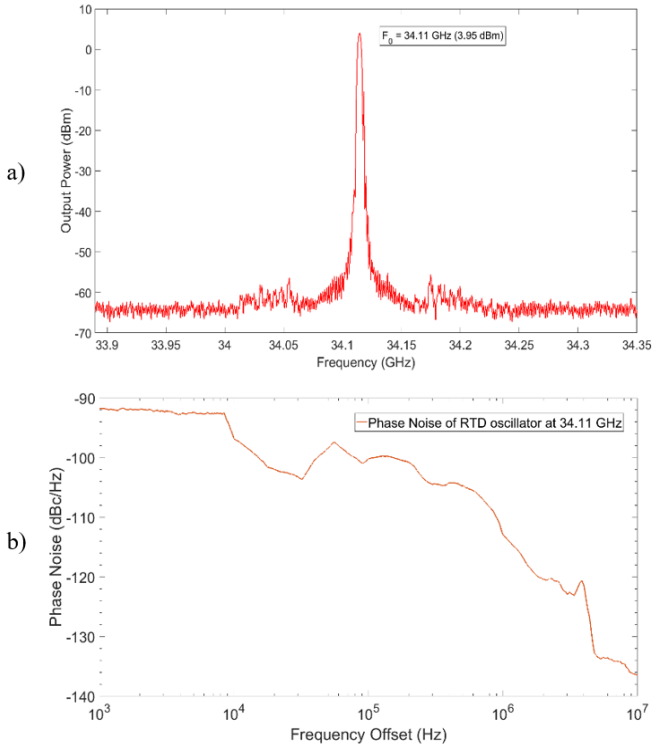


Fig. 6 a) Measured output spectrum of RTD oscillator with capacitor and resistor stabilising network at V_{BIAS} = 0.94 V, I_{BIAS} = 18 mA. b) Measured SSB phase-noise performance at 34.1 GHz carrier frequency.

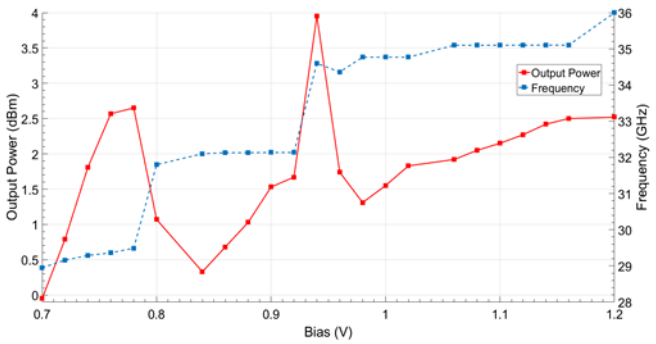


Fig. 7 Measured oscillator output power and frequency as a function of bias voltage.

V. Discussion and Conclusion

Highly efficient mm-wave RTD oscillators with tuneable frequency between 29 and 36 GHz were presented in this paper. They employ a bias stabilisation network that does not consume dc power resulting in over a 10-fold improvement in DC-RF conversion efficiency. The oscillators also exhibit low phase noise. For further higher DC-RF oscillator efficiencies, a reduction of the peak voltage and of the valley current is necessary. Compared to other semiconductor electronic technologies, RTD oscillators provide a simple, low cost solution for future short-range high capacity wireless communication systems and other applications, and as such improvements need to be made to increase their output power (~10 mW @ >100 GHz) and efficiency (>20%). For high RF output power, increasing the span of the NDR region is required. Therefore, future work will thus focus on designing advanced RTD epitaxial layer structures and optimally loaded mm-wave and THz oscillators using this high efficiency bias stabilisation approach.

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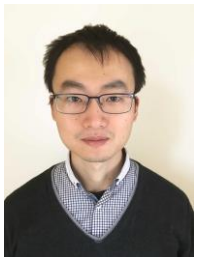

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