# Polysilicon photonic resonators for large-scale 3D integration of optical networks

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**Abstract:** We demonstrate optical microresonators in polycrystalline silicon with quality factors of 20,000. We also demonstrate polycrystalline resonators vertically coupled to crystalline silicon waveguides. Electrically active photonic structures fabricated in deposited polysilicon layers would enable the large-scale integration of photonics with current CMOS microelectronics.

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**OCIS codes:** (130.3130) Integrated optical materials; (230.5750) Resonators; (130.3120) Integrated optical devices.

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## 1. Introduction

On-chip silicon photonic networks are a promising solution for the interconnect bottleneck in high performance microelectronics [1-2], but the additional silicon real estate required to integrate hundreds or thousands of microphotonic devices is one of the main barriers to their immediate implementation. Many planar silicon photonic building blocks have been recently demonstrated [3-10]. Most of the major progress in silicon photonics has been based on single-crystalline silicon on insulator (SOI), which is widely available and has well-understood material properties. By itself, however, the SOI platform restricts active electronic and photonic devices to a single layer. This limits the number of devices that can fit on a chip.

Vertical integration of multiple silicon layers would resolve the issue of limited real estate on a chip by separating the photonic waveguides and devices from the microelectronics. Several schemes for fabricating multiple single-crystalline silicon layers have been demonstrated, including wafer bonding [11], epitaxy [12], and separation by implantation of oxygen (SIMOX) [13] techniques. While in the future one or more of these methods may become feasible from a manufacturing standpoint, none of them is currently a standard CMOS fabrication technique.

Using only standard CMOS techniques, vertical integration could be achieved by depositing thin films of silicon. These films are not crystalline but rather are polycrystalline or amorphous, and therefore it is not immediately clear whether they have suitable optical and

electrical properties. While waveguides made from hydrogenated amorphous silicon (a-Si:H) deposited by plasma-enhanced chemical vapor deposition (PECVD) have been demonstrated with propagation losses of a few dB/cm [14-15], the electrical carrier mobility in such films is on the order of 1 cm²/V·s [16]. This value is around three orders of magnitude lower than the mobility in crystalline silicon. As a result, a-Si:H films are not appropriate for active devices such as electro-optic modulators, which are critical components for on-chip optical networks.

Polycrystalline silicon, or polysilicon, can have an electronic carrier mobility on the order of 100 cm²/V·s [17] and therefore may enable the integration of electrically active photonic devices with CMOS microelectronics. Polysilicon has largely been ignored by the photonics community due to the challenges introduced by its optical losses. A few exceptions include a three-dimensional photonic crystal with an infrared band gap [18], a MOS based electro-optic modulator which included a polysilicon gate built into a centimeter-length crystalline silicon waveguide [19], and passive polysilicon waveguides and ring resonators [20-22]. Optical material loss mechanisms in polysilicon are dominated by scattering and absorption at the polysilicon grain boundaries, whose size and nature are greatly influenced by deposition and annealing conditions [20]. By using high temperature (1100°C) anneals and special hydrogen plasma passivation steps, channel waveguides with losses as low as 9 dB/cm [21] and resonators with loaded quality factors of 7,000 [22] were demonstrated by Kimerling et al.

In this paper we experimentally demonstrate high performance polysilicon photonic ring resonators with loaded quality factors of 20,000 for wavelength filtering applications [23] and show for the first time the ability to vertically integrate polysilicon structures with low loss single-crystalline materials. Additionally we examine the use of polysilicon for electro-optic modulators, which are important photonic devices for on-chip optical networks.

## 2. Polysilicon ring resonators and waveguides

We fabricate high quality factor resonators as shown in Fig. 1. A 2 μm silicon dioxide layer is thermally grown on a four-inch silicon substrate and a thin film of amorphous silicon is subsequently deposited using low-pressure chemical vapor deposition (LPCVD) at 550°C. Using atomic force microscopy (AFM), we measure the root mean square (RMS) surface roughness of this film to be 0.3 nm. In order to stabilize the smooth top surface during crystallization and limit the migration of silicon atoms, we allow a native oxide to grow [17]. We then anneal the samples in $N_2$ at 600°C, which crystallizes the amorphous silicon into polycrystalline silicon, and anneal further at 1100°C, which maximizes the crystallized fraction and removes defects from the crystalline regions [20-21]. The final thickness of the film is 220 nm, and the final RMS surface roughness is measured by AFM to be 0.7 nm. E-beam resist is spun on and patterned by e-beam lithography, and the pattern is transferred by reactive ion etching (RIE) using a chlorine-based silicon etch recipe. Finally, an $SiO_2$ cladding layer is deposited by PECVD.
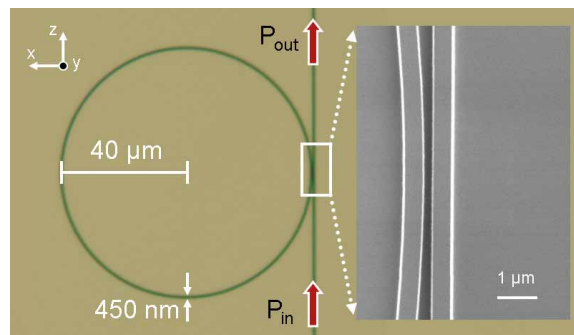


Fig. 1. Optical microscope image and scanning electron microscope (SEM) inset of a polysilicon waveguide side coupled to a polysilicon ring resonator.

We measure the transmission spectrum of the quasi-TM (y-polarized electric field) mode in order to determine the resonant properties of the device. Light from a tunable infrared laser is sent through a polarization controller, out of a tapered lens fiber, and coupled on- and off-chip using adiabatic nanotapers at the ends of the patterned waveguides [24]. The output from the chip is collected by an objective lens, passed through a polarization filter, and measured with an infrared detector. The figures of merit for the ring as a wavelength filter are the loaded quality factor $Q_{loaded} \approx \lambda_0 / \Delta\lambda_{FWHM}$ and the extinction ratio $ER = 10 \log (P_{min}/P_{max})$, with $\Delta\lambda_{FWHM}$ the full width at half-maximum, $P_{min}$ the transmission on resonance, and $P_{max}$ the maximum transmission off resonance. The $Q_{loaded}$ of a resonator coupled to a single waveguide is described as:

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_0} + \frac{1}{Q_{coupling}} \quad , \tag{1}$$

where $Q_0$ is the intrinsic quality factor of the device and $Q_{coupling}$ arises from coupling to the bus waveguide. For a maximum extinction ratio, the critical-coupling condition $Q_0 = Q_{coupling}$ should be met. This lowers the loaded $Q$ to half of the intrinsic value.

The mode profile of a polysilicon waveguide with oxide cladding is shown in Fig. 2(a), as simulated by a finite element mode solver. The effective index of the TM-polarized mode is calculated to be $n_{eff} = 1.76$ at $\lambda = 1550$ nm using $n_{Si} = 3.48$ and $n_{oxide} = 1.46$. Figure 2(b) shows a transmission spectrum for a 40 μm radius ring with $\Delta\lambda_{FWHM} = 0.079$ nm, $Q_{loaded} = 20,000$ and a maximum extinction ratio of 24 dB, indicating that the resonator is nearly critically coupled.
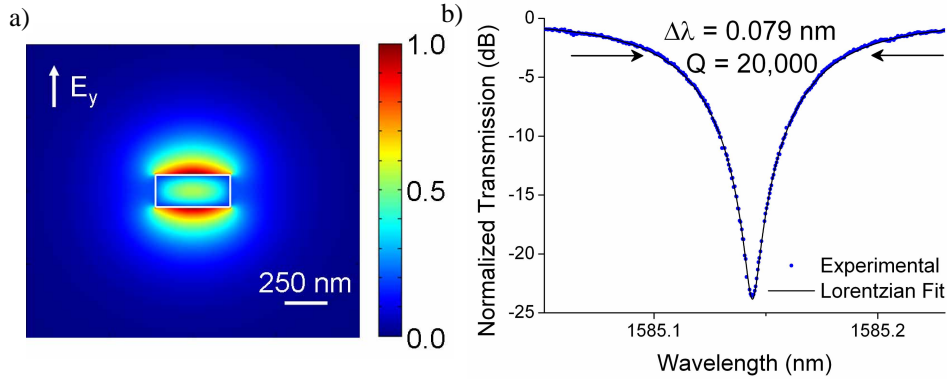


Fig. 2. (a): Quasi-TM polarized optical mode calculated with a finite element mode solver. (b): Transmission spectrum for a 40 μm radius polysilicon ring resonator annealed at a maximum temperature of 1100°C.

The group index $n_g$ can be calculated from the measured free spectral range and the path length $L$ as $n_g \approx \lambda_0^2 / (FSR)(L)$ [25]. From the measured free spectral range of 2.345 nm, we calculate $n_g = 4.26$ near $\lambda_0 = 1585$ nm. Under the critical coupling condition, $Q_{loaded}$ can be written as [25]:

$$Q_{loaded} = \frac{1}{2}Q_0 = \frac{\pi \cdot n_g}{\lambda_0 \cdot \alpha_{ring}} \quad , \tag{2}$$

where $\alpha_{ring}$ is the total propagation loss per unit length in the ring. Using Eq. (2) we estimate a propagation loss in the ring $\alpha_{ring} = 18$ dB/cm and an intrinsic quality factor $Q_0 = 40,000$.

The refractive index of the film is approximately equal to its value in crystalline silicon because the volume of the polycrystalline film is mostly single crystalline, but interspersed with nanometer-thin amorphous grain boundaries. To compare the relative size of the crystalline grains to the size of our waveguides, we use a defect etching scheme. First we

thermally oxidize an unclad sample which has polysilicon waveguides. During this process, oxygen diffuses quickly into the amorphous silicon grain boundaries and oxidizes the boundaries more rapidly than the crystalline grains [17]. After wet etching the grown oxide with HF, we are then able to observe the grain size of the polycrystalline silicon using a standard top-down SEM. Figure 3 shows an SEM image of the coupling region between a ring and a waveguide in a defect etched polysilicon sample. We estimate an average grain size of 300 nm using the line-intercept method [26]. This measured average grain size is comparable to reported values for similarly prepared polysilicon films [20]. Using a first-order approximation of each grain as a 300 nm crystalline silicon cube with 1 nm thick amorphous silicon boundary on each surface, we can estimate that the volume of our polysilicon film is more than 97% crystalline.
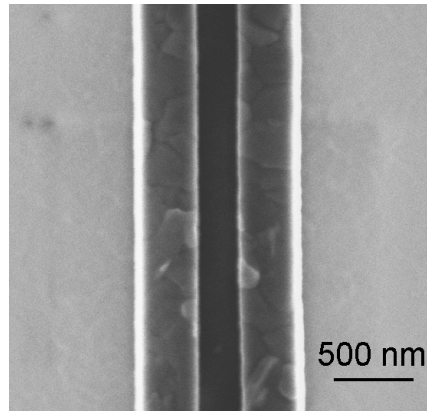


Fig. 3. Coupling region between two defect etched polysilicon waveguides showing an average grain size of approximately 300 nm.

For on-chip optical networks where the flow of light is dynamically controlled, we expect both the electrical and optical properties of polysilicon to support ring resonator-based active devices such as switches and modulators. Plasma dispersion is the dominant electro-optic effect in silicon [27] and is the mechanism for high speed signal modulation. From the relation between the index of refraction and the carrier concentration [27] we find that a carrier concentration of $\Delta N = \Delta P = 3.4 \times 10^{16}$ cm$^{-3}$ shifts the refractive index of the polysilicon by $\Delta n = -1.7 \times 10^{-4}$. Using a finite element mode solver program, we estimate a corresponding shift in the mode's effective index of $\Delta n_{eff} = -8.6 \times 10^{-5}$ and a shift of the resonant wavelength in Fig. 2(b) of $\Delta \lambda = -0.079$ nm. This gives rise to a modulation depth as high as 22 dB. The required carrier concentration is comparable to that used in state of the art ring resonator-based GHz electro-optic modulators in crystalline silicon [28]. The electrons and holes can be introduced either optically using a pump beam, or electrically using a PIN diode. Polysilicon electrical devices such as diodes and transistors are commonly used in thin-film displays [17]. This is possible because adequately doped polysilicon films (on the order of $10^{17}$ cm$^{-3}$) can have electrical carrier mobility and resistivity within about an order of magnitude of their values in crystalline silicon [17].

## 3. 3D integration of polycrystalline resonators with low-loss waveguides

To demonstrate the suitability of the polysilicon platform for vertical integration, we fabricate resonators which are offset-vertically coupled to low-loss waveguides of a different material (in this case, crystalline silicon). The integration of deposited active devices with low-loss bus waveguides would enable massive integration of photonic networks on chip. While our demonstration uses crystalline silicon to efficiently guide light to and from polysilicon resonators, any low-loss optical material could be used in a final system. For example, amorphous silicon [14-15] or silicon nitride [29-30] films could be deposited and patterned

into low-loss waveguides above or below the polysilicon rings. By depositing layers of two different materials, one can take advantage of the benefits of each; for instance, an optical network could use the electrical characteristics of polysilicon for active switching devices, while still benefiting from the optical properties of amorphous silicon to guide light over centimeter-long distances on chip.

The processing steps to fabricate polysilicon resonators over SOI waveguides are shown in Fig. 4, as generated in the ATHENA process simulator from SILVACO [31]. For the crystalline substrate we use an SOI wafer containing a 3 μm buried oxide layer and a 250 nm thick silicon layer. Waveguides are patterned in the crystalline silicon layer by e-beam lithography and RIE, shown in Fig. 4(a), and a 350 nm film of oxide is deposited from a tetraethoxysilane (TEOS) precursor by PECVD, shown in Fig. 4(b). We then deposit a 250 nm thin film of amorphous silicon in an LPCVD furnace tube and carry out crystallization anneals at 600ºC and 1100ºC, shown in Fig. 4(c), as in Section 2. Racetrack resonators with different radii and coupling lengths are then patterned in the polysilicon layer by e-beam lithography and RIE, shown in Fig. 4(d). Finally, we deposit a PECVD oxide cladding, shown in Fig. 4(e). Note that the process does not include the use of chemical mechanical polishing (CMP). In order to ensure that the racetrack is not located on the hill created by the non-planar surface, a center-to-center horizontal offset larger than 800 nm is needed between the resonator and the adjacent waveguide. We use racetrack resonators to increase the coupling between the waveguides and the resonator in this arrangement. We also use waveguides and resonators with a 350 nm wide cross section to decrease the optical confinement and therefore increase the coupling as compared to 450 nm wide structures.
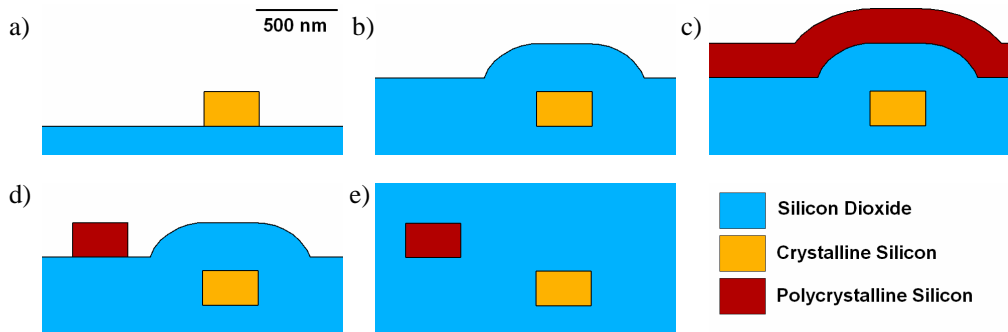


Fig. 4. Process flow for vertical coupling sample. (a): Definition of crystalline silicon waveguides by e-beam lithography and etching. (b): Deposition of TEOS oxide by PECVD. (c): Deposition of amorphous silicon layer, and anneal steps to crystallize amorphous silicon to polycrystalline silicon. (d): Definition of polysilicon resonators by e-beam lithography and etching. (e): Deposition of oxide cladding by PECVD.

The fabricated structure is shown in Fig. 5a before oxide cladding, as in Fig. 4(d). In Fig. 5(b) we show the quasi-TM spectrum of a structure with a racetrack of radius $r = 40$ μm and a coupling region length $L_0 = 3$ μm. Note that for these dimensions the resonator is undercoupled at shorter wavelengths but comes closer to critically coupled at longer wavelengths. At wavelengths near $\lambda_0 = 1600$ nm, the FSR is measured to be 2.3 nm and the group index is calculated to be $n_g = 4.33$. We measure $Q_{loaded}$ values over 4,000 and extinction ratios near 10 dB. Figure 5c shows a smaller racetrack with $r = 10$ μm and $L_0 = 5$ μm. Here we measure once again $Q_{loaded}$ values approaching 4,000 and extinction ratios greater than 10 dB, but with a larger free spectral range of 8.08 nm near $\lambda_0 = 1600$ nm. We calculate the group index to be $n_g = 4.35$.
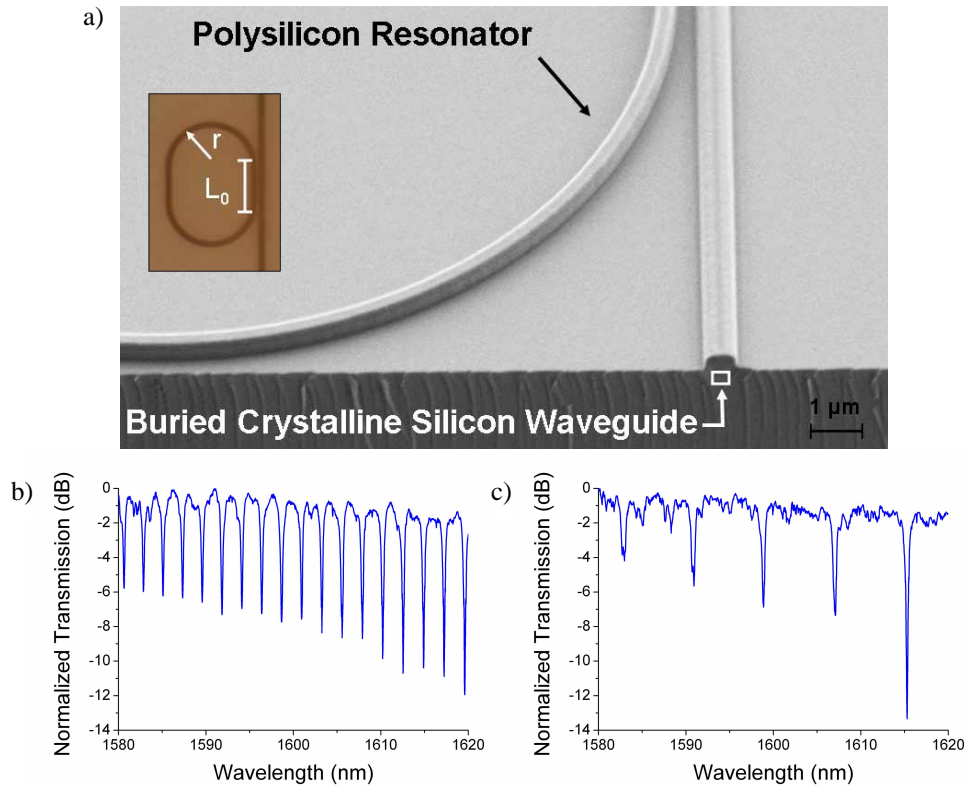
Fig. 5. Polysilicon racetrack resonators coupled to crystalline silicon waveguides. (a): Cross-section SEM of the structure before oxide cladding. Inset: Definition of $r$ and coupling length $L_0$. (b) and (c): Quasi-TM polarized transmission as a function of wavelength for (b) $r = 40$ μm, $L_0 = 3$ μm and (c) $r = 10$ μm, $L_0 = 5$ μm.

## 4. Discussion

We have demonstrated CMOS-compatible polysilicon resonators with intrinsic $Q_0$ values of 40,000. The primary limitations on $Q$ are scattering from sidewall roughness, scattering due to a refractive index difference between the crystalline grains and amorphous silicon grain boundaries, and absorption due to dangling bonds at the amorphous grain boundaries. Lower losses and higher $Q$'s could be achieved by implementing hydrogen passivation of the dangling bonds at the polysilicon grain boundaries [21].

We have also demonstrated for first time to our knowledge a mixed-silicon optical system, in this case crystalline silicon waveguides coupled vertically to polysilicon resonators with $Q_{loaded}$ values of 4,000. A previous demonstration of vertical coupling used polysilicon for both the waveguide and the resonator and $Q_{loaded}$ values of 1,000 were shown [32]. We could increase both the $Q$ values and the amount of coupling by using a planarization step such as CMP. The rings or racetracks could then be placed directly above the waveguides, increasing the quasi-TM mode overlap and coupling even for larger vertical separations. Also, the polishing step could produce a smoother oxide surface to deposit silicon onto, potentially making lower loss polysilicon films with higher $Q$ values.

The maximum processing temperature is an important consideration for the integration of photonics with CMOS microelectronics. Polysilicon processed at 1100°C is compatible with front end of the line fabrication, above the crystalline silicon transistor layer but below the metal interconnect layers and before ion implantation. The polysilicon layer could also be

introduced on top of the metal interconnect layers after all of the electrical processing is completed. In order to achieve this, the annealing temperature could be reduced below 450°C using excimer laser annealing. This technique has been demonstrated to crystallize low temperature amorphous silicon into large-grain polycrystalline silicon for thin film transistors [33-34]. With grain sizes in these films on the order of micrometers, an entire photonic device could fit within a single grain and exhibit near-single crystalline behavior.

## Acknowledgements