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New Semiconductor Devices

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A review of recently emerging semiconductor devices for nanoelectronic applications is given. For the end of the international technology roadmap for semiconductors, very innovative materials, technologies and nanodevice architectures will be needed. Silicon on insulator-based devices seem to be the best candidates for the ultimate integration of integrated circuits on silicon. The flexibility of the silicon on insulator-based structure and the possibility to realize new device architectures allow to obtain optimum electrical properties for low power and high performance circuits. These transistors are also very interesting for high frequency and memory applications. The performance and physical mechanisms are addressed in single- and multi-gate thin film Si, SiGe and Ge metal-oxide-semiconductor field-effect-transistors. The impact of tensile or compressive uniaxial and biaxial strains in the channel, of high k materials and metal gates as well as metallic Schottky source-drain architectures are discussed. Finally, the interest of advanced beyond-CMOS (complementary MOS) nanodevices for long term applications, based on nanowires, carbon electronics or small slope switch structures are presented.

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1. Introduction

Since the 60's the shrinking of electronic components has been driven by the fabrication of integrated circuits, which will continue for at least the next two decades. The critical feature size of the elementary devices (physical gate length of the transistors) will drop from 25 nm in 2007 (65 nm technology node) to 5 nm in 2020 (14 nm technology node). In the sub-10 nm range, beyond--CMOS (complementary MOS) devices will certainly play an important role and could be integrated on CMOS platforms in order to pursue integration down to nm structures. Si will remain the main semiconductor material in a foreseeable future, but the needed performance improvements for the end of the ITRS (international technology roadmap for semiconductors) [1] will lead to a substantial enlargement of the number of materials, technologies and device architectures.

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Therefore, new generations of nanoelectronic integrated circuits (ICs) present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc. [1, 2]) resulting in an urgent need of long term research based on a scientific approach, in order firstly to understand the underlying physical mechanisms and hence remove the present technological limitations. The industry is indeed increasingly relying on new ideas in order to continue technological innovation.

This paper addresses the more Moore domain, with some very advanced ideas for keeping CMOS on the road (new channel materials, very low Schottky barrier contacts, novel gate stacks, multi-gate devices) and the beyond-CMOS field (nanowires, carbon structures, small slope nanoelectronic switches, realization of nanodevices by templated self-assembly). This work is partly based on some important advances for nanoelectronic devices and materials recently obtained in the framework of the FP7-Nanosil and FP6-Sinano European Networks of Excellence [3].

2. More Moore

2.1. New channel materials for ultimate CMOS

As simple scaling of silicon CMOS becomes increasingly complex and expensive there is considerable interest in increasing performance by altering the material of the conducting channel. In the first instance the silicon can be strained, which reduces the valley degeneracy and lowers the carrier effective mass, thus improving carrier mobility and drive current in a device. Although a certain degree of strain can be process-induced with tensile liners, higher strains have been obtained by growing Si on a relaxed $Si_{1-x}Ge_x$ virtual substrate (VS).

Since the quality of buffer layers significantly influences transport properties of carriers in the strained quantum well (QW), appropriate $Si_{1-x}Ge_x$ buffers with a high degree of relaxation, smooth surface morphology and low threading dislocations density (TDD) on the surface are in a great demand. Useful Ge composition in the SiGe buffer layer for subsequent growth of a tensile strained Si QW with high electron mobility varies from 10% up to 40%. In contrast, formation of a compressive strained Ge QW with high hole mobility is more difficult because it requires much higher Ge content SiGe buffers from 60% up to 90%.

Virtual substrate development allows strained Ge layers to be created for *p*-channel operation, where the hole mobility can exceed the electron mobility in silicon. Relaxed buffers have been produced using a terrace grading approach with terminating layers having $x = 80\%$, yet still retaining a good TDD significantly below 10^6 cm^{-2} and no pile up of dislocations (Fig. 1).

Reduction of the SiGe buffer layer thickness is also of great importance in order to reduce self-heating effects due in particular to the poor thermal conductivity of the SiGe layer compared with Si [4]. Therefore, further developments enabled thin VSs (< 300 nm thick) to be produced by RP-CVD (Reduced-Pressure Chemical Vapor Deposition) with p-channel devices fabricated having a 150 nm gate

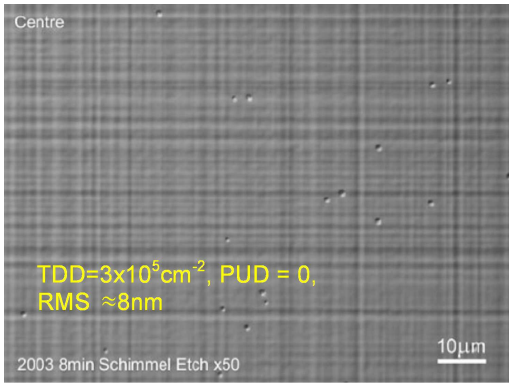

Fig. 1. Relaxed buffer layer of $Si_{0.2}Ge_{0.8}$ on Si(001), after etching to reveal threading defects (seen as pits) with density below 10^6 cm^{-2}.

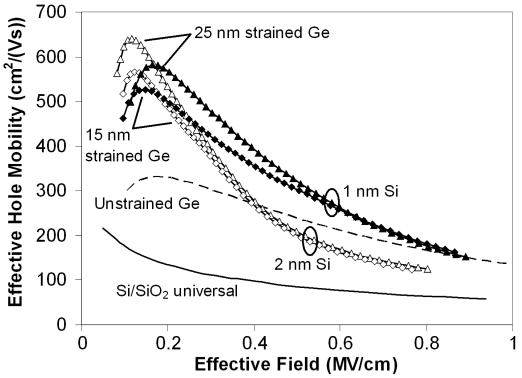

Fig. 2. Hole mobility of strained Ge channel devices, indicating large improvements over the previous state-of-the-art (dashed line for unstrained Ge and solid for bulk silicon).

length and a drive current exceeding 1 mA/μm [5]. The hole mobility (Fig. 2) in these high-k gated devices shows a massive enhancement over unstrained Ge and the universal Si values at low effective field. This is somewhat compromised at higher effective fields, especially for devices with a thicker Si interlayer, where the holes penetrate this cap. It appears that the device performance is currently limited by the high-k dielectric to channel interface rather than the Ge channel, which may promise yet more.

Strained silicon on insulator (sSOI) has been fabricated based on thin SiGe buffer layers relaxed by the so-called "Juelich-process". In the process, a 200 nm thick pseudomorphic SiGe layer, with 23 at% Ge content grown on a Si(100) wafer and capped with a few nanometers pure Si layer is implanted with He^+ ions at $\approx$ 200 nm depth below the SiGe/Si substrate interface. During post-implantation annealing at 850°C, diffusive implanted He^+ ions form overpressurized He bubbles

which punch out dislocations loops. Under the influence of the strain field, these dislocation loops move up to the interface forming misfit dislocations that lead to strain relaxation of the SiGe layer. If the Si cap layer thickness lies below a critical thickness (< 8 nm), an induced strain is transferred immediately during the relaxation of the SiGe layer. Finally, the thickness of the strained Si cap can be increased by a further epitaxial growth step. A high resolution Z-contrast transmission electron micrograph (HRTEM) shows the perfect alignment of the crystalline lattice of the strained Si cap and of the relaxed SiGe layer. In the next fabrication step, the wafer is cleaved with hydrogen implantation according to the Smart-Cut® process and the stack layer is bonded to an oxidized handle wafer. After a final etch back step, the strained Si layer remains directly on the SiO_2 (Fig. 3a). Strain values of $\approx 0.65\%$ were achieved in 58 nm thick sSOI layers with TDDs as low as 5×10^5 cm^{-2}, as shown in Fig. 3b. Split-CV (capacitance-voltage) mobility measurements shown in Fig. 3c demonstrate the enhanced performance of the fabricated sSOI, with electron mobility values as high as 1200 cm^2/(V s) [6].

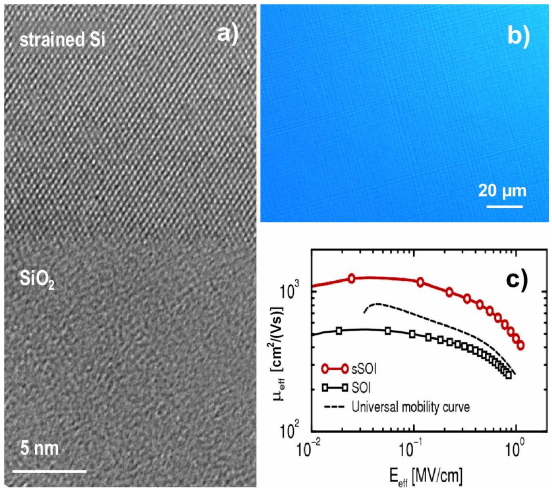

Fig. 3. HRTEM cross-section image of a fabricated sSOI (a). The high quality sSOI surface with low TD densities ($< 5 \times 10^5$ cm^{-2}) as well as low roughness is shown (b); and the enhanced mobility curves of sSOI in respect of SOI are compared (c).

Another example of sSOI materials is exemplified in Fig. 4 showing a plot of the dependence of electron and hole mobilities as a function of the charge density [7]. The strained Si layer is fabricated with sacrificial thin relaxed SiGe and smart cut. In the sSOI devices, substantial enhancements of both electron (about 100%) and hole (about 50%) mobilities are obtained compared with the control SOI device at intermediate charge densities for long channel transistors.

The impact of strained layers has also been demonstrated for short channel devices. An enhancement of the electron mobility of about 15–20% has been

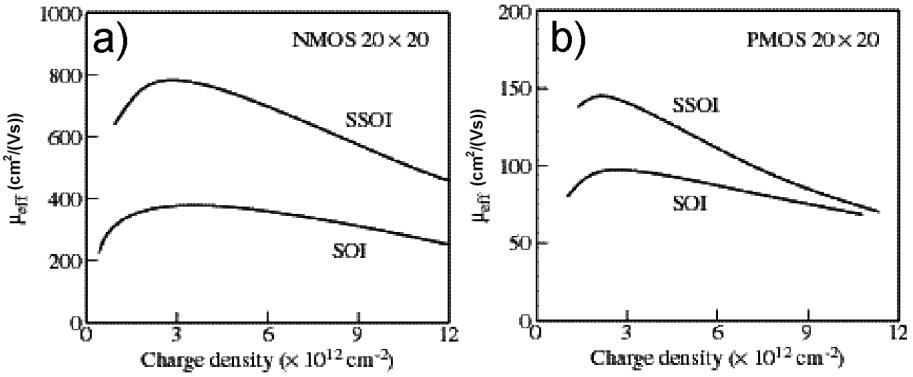

Fig. 4. Effective mobility comparison between sSOI and SOI MOSFETs.

obtained for 70 nm technology SGOI MOSFETs (strained Si on SiGe on insulator) together with superior short channel control. A significant increase in the driving current has been shown for these advanced devices (Fig. 5) [8, 9].

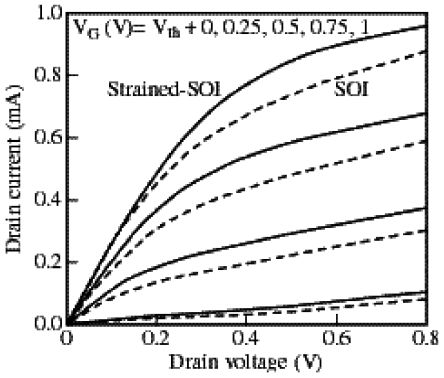

Fig. 5. $I_{\mathrm{d}}-V_{\mathrm{d}}$ of 70 nm MOSFETs ($W = 1$ μm).

The impact of the percentage of Ge is shown in Fig. 6. The electron mobilities are represented for various Ge content of the SiGe layer and different Si film thicknesses. The electron mobility enhancement is maximum for 30% of Ge due to the increase in alloy scattering and/or surface roughness, and the hole mobility continuously increases with Ge up to 50% [9]. It is also worth noting that the enhancement of carrier mobility is reduced in thinner strained Si films due to interface states and fixed charges induced by the diffusion of Ge atoms to the interfaces.

Figure 7a,b shows I_{dsat} and G_{msat} as a function of channel length for SGOI and SOI MOSFETs. An enhancement of I_{d} is outlined down to sub-50 nm transistors for SGOI, but the difference diminishes at smaller channel length due in

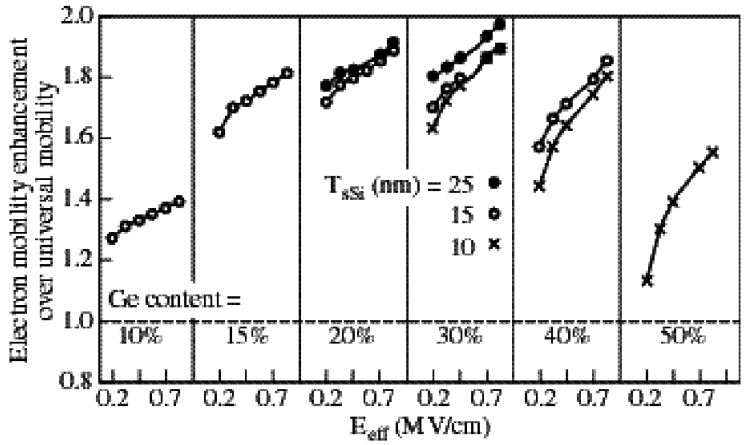

Fig. 6. E_{eff} dependence of electron mobility enhancement as a function of Ge content ar

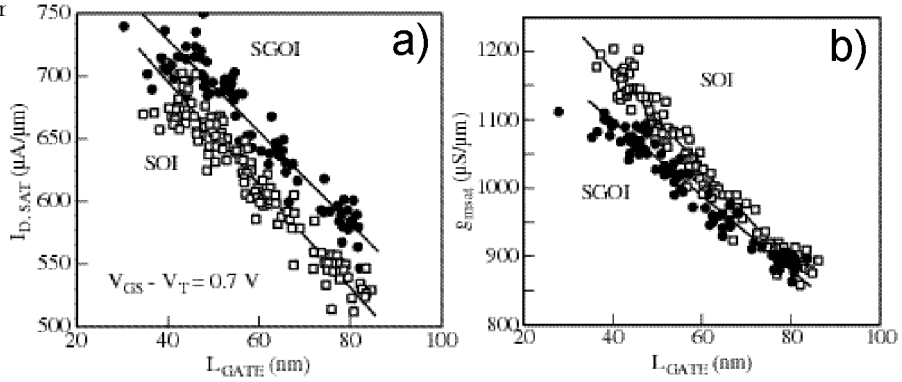

Fig. 7. Comparison of I_{dsat} and G_{msat} at a constant gate overdrive.

particular to larger self-heating (SH) in SiGe than in Si. This SH effect in SGOI degrades G_{msat}, which is more sensitive to SH than I_{d}. Therefore the transconductance appears degraded in SGOI as compared to SOI but after correction of the self-heating a similar increase is obtained for I_{d} and G_{m} in the SGOI structure [10].

The HOI structure (strained Si/strained SiGe/ strained Si heterostructure on insulator) presents also substantial electron and hole mobility enhancements [11]. In particular, hole mobilities are very high for thin Si cap layer (enhancement of about 100%) compared with the universal SOI mobility and are also significantly larger that the best SSDOI mobility (strained Si directly on insulator) due to the compressively strained buried SiGe channel (Fig. 8).

Uniaxial strain engineering is also useful for mobility enhancement for Si film thickness in the sub-10 nm range [12], which will be needed for the ultimate integration of nanoMOSFETs. A similar enhancement of electron mobility in 3.5 nm SOI devices under biaxial and uniaxial tensile strain has been obtained.

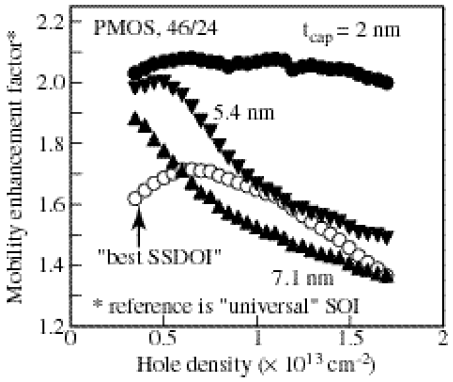

Fig. 8. Mobility enhancement in HOI compared with the best SSDOI curve relative to the "universal" SOI mobility.

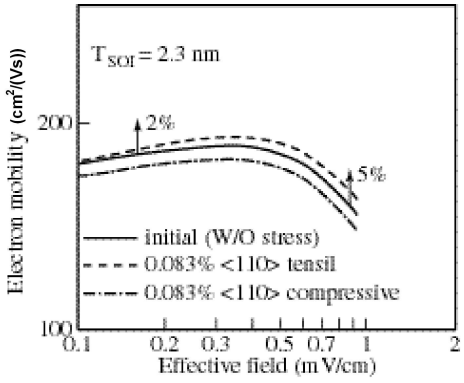

Fig. 9. Electron mobility in 2.3 nm ultra-thin-body MOSFET under ⟨110⟩ uniaxial strain.

The electron mobility is also enhanced in 2.3 nm Si layer under uniaxial tensile strain (Fig. 9), and the hole mobility increases in 2.5 nm film under uniaxial compressive strain.

The influence of surface roughness (SR) in ultra-thin films is very important. Figure 10 shows the SR limited hole mobility as a function of body thickness for Si (SOI) and Ge (GOI) channels. The variation of hole mobility is outlined for various surface orientations [13], which is also a major parameter for the optimization of the MOSFET electrical properties.

Figure 11 represents electron mobilities in FinFETs with various fin orientations. An improvement of electron mobility is observed for ⟨100⟩ and an enhancement of hole mobility has also been shown for ⟨110⟩ orientation [14].

Process-induced strain is also interesting to boost semiconductor device performance. It has recently been shown that the use of a metal gate (TiN) can induce significant compressive stress along the channel direction. This stress is

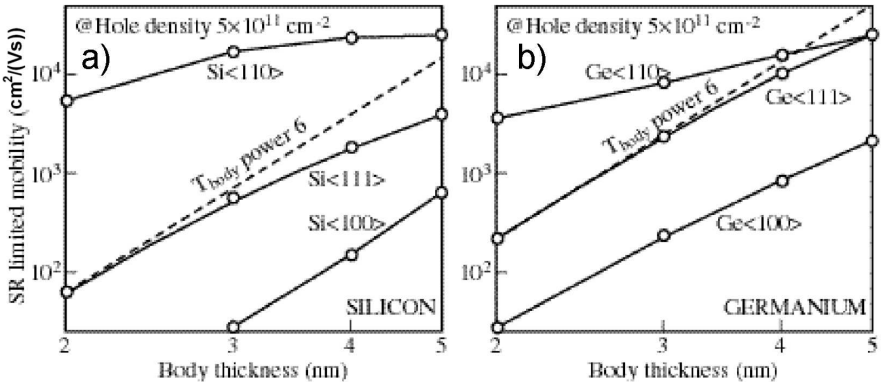

Fig. 10. Simulated surface roughness limited hole mobility for Si and Ge with various orientations.

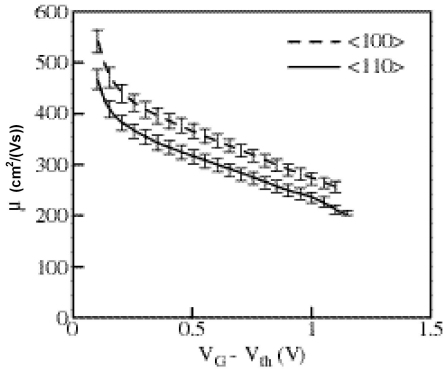

Fig. 11. Electron mobility of FinFETs (Fin Field-Effect Transistors) with $\langle 100 \rangle$ and $\langle 110 \rangle$ fin orientation. $T_{ox} = 2$ nm, 4.5×10^{13} cm^{-2} channel implantation.

increased as the gate length decreases. This phenomenon progressively degrades electron mobility while hole transport is improved. Similar behaviors are obtained in single and double gate SOI devices, and the use of $\langle 110 \rangle$ channel orientation is the most favorable in terms of electrical performance [15].

2.2. Metallic Schottky source/drain MOSFETs

As CMOS technology is entering the decananometer era, the contact resistance associated with the silicide/silicon interface is identified as one of the biggest challenges to solve in order to preserve current drive capabilities. In that context, source/drain (S/D) engineering takes an increasing importance in the development of leading edge CMOS generations because of the increasing impact of S/D series resistances on transistor performance. In order to further pursue down-scaling of MOSFETs in the sub-32 nm range of gate lengths, novel devices that hierarchically combine alternative materials as well new architecture concepts such as multi-gated channel have been proposed. Considering that the aforementioned

innovations are expected to contribute to a higher current drive at shallower junction depth and reduced silicide thickness, extremely severe constraints are placed on the junction and contact technologies.

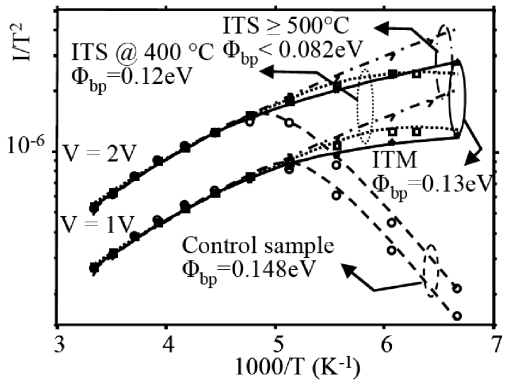

Fig. 12. Extraction of the Schottky barrier height from the Arrhenius diagram. The extraction procedure is based on a transport model that considers thermionic and tunnel injection as well as barrier lowering by charge induction. Results obtained under the ITM (implant-to-metal) and ITS (implant-to-silicide) flavors under a reduced thermal budget of 500°C.

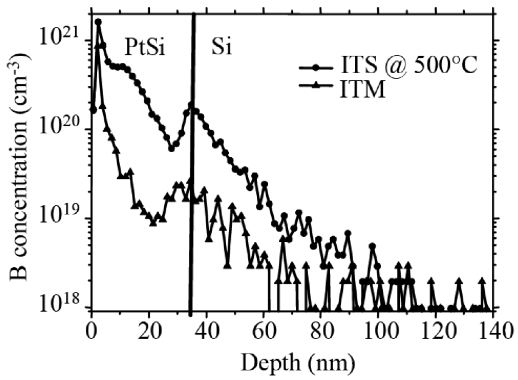

Fig. 13. SIMS characterization of the boron pile effect at the silicide/silicon interface. Results obtained under the ITM and ITS flavors under a reduced thermal budget of 500°C.

In order to address this challenge, one alternative is to implement metallic S/D combined to a dopant segregation (DS) strategy at reduced thermal budget. The expected benefit is to considerably reduce the specific contact resistance of the metal/semiconductor junction while keeping activated dopants sharply localized at the interface. In the framework of the European projects, the efficiency of dopant

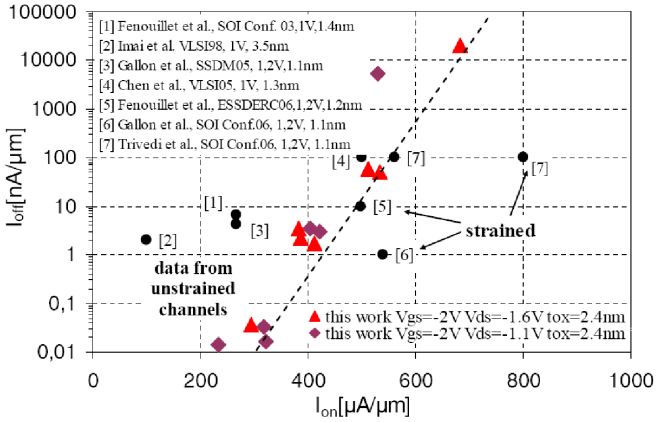

Fig. 14. $I_{on}-I_{off}$ state-of-the-art of S/D p-MOSFET on SOI substrate indicating that boron DS p-MOSFETs is leading the SOA of both SB and conventional unstrained thin-film SOI technologies.

segregated Schottky contacts has been demonstrated [16–18]. The implementation of dopant segregated contact is illustrated by considering the following three distinctive features: (i) implant-to-silicide (ITS), (ii) band-edge low Schottky barrier (SB) to holes (PtSi) and (iii) thermal budget limited to 500°C. It has been shown that the ITS scheme coupled to BF_2^+ provides a sub-100 meV barrier (Fig. 12) consistently with the boron pile-up observed at the PtSi/Si interface (Fig. 13). A new state-of-the-art current drive performance has been established for SB-MOSFETs at 25 nm of gate length: I_{on} of 530 μA/μm at $V_g = V_d = -1.1$ V. Figure 14 also demonstrates that metallic S/D competes with best unstrained channel SOI p-FET technologies. A record RF performance for a 30 nm p-type unstrained thin-film fully depleted SOI SB MOSFET has been demonstrated with a f_T of 180 GHz [16]. The effect of strained semiconductor is also thoroughly studied: carrier injection from a metallic junction should benefit from band splitting and from the corresponding Schottky barrier height reduction.

2.3. High-k materials

In the search for new insulator materials for the 22 nm CMOS node and beyond, the dielectric constant itself is not sufficient as a physical quantity to fulfill for technical device specification. The ultimate device property in this context is the gate leakage current for a given "equivalent oxide thickness" (EOT) needed to achieve a high enough capacitive coupling between transistor gate and channel. For a perfectly amorphous or monocrystalline insulator material, this quantity is limited by tunneling. Thus, the combination of dielectric constant, k, and the energy barrier height governed by the offset, E, between the energy bands of the insulator and silicon is crucial from this viewpoint. For electron leakage, the relation between these two quantities can roughly be described as hyperbolic such that $E \times k = C_E$, where C_E is a constant, determined by the leakage and

gate coupling properties required for a certain technology node [19]. For the "low standby power" (LSTP) 22 nm bulk CMOS node, $C_E \approx 70$ eV, while the corresponding requirement for SOI technology (fully depleted double gate) can be set to $C_E \approx 30$ eV. These relations are summarized in Fig. 15.

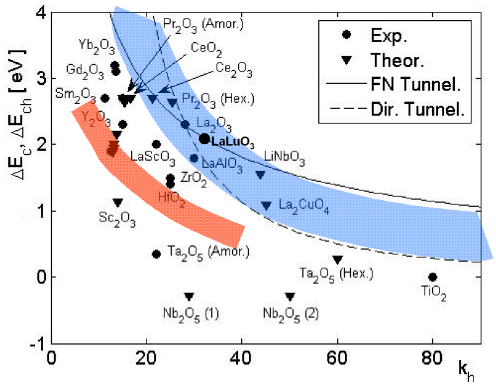

Fig. 15. Energy offset values between the conduction bands of various dielectrics and silicon versus dielectric constant. The upper shadowed area is a border for the 22 nm LSTP bulk CMOS node. The lower shadowed area represents the corresponding border for FD DG SOI technology.

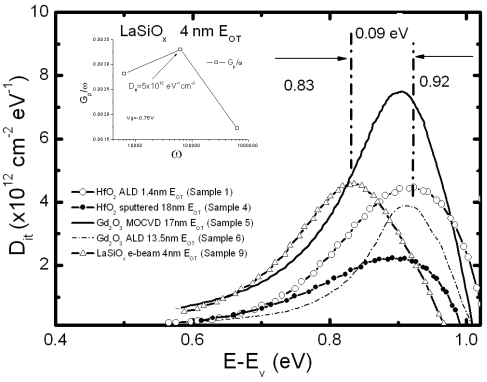

Fig. 16. Density of interface states as a function of free energy gap position related to the silicon valence band. The peaks for all three materials, HfO_2, Gd_2O_3 and $LaSiO_x$ are in the range 0.2–0.3 eV, common for the P_b peak.

For Gd_2O_3, prepared by two different methods, atomic layer deposition (ALD) and MBE, respectively, for $LaSiO_x$ prepared by evaporation and for HfO_2 prepared by sputtering, studies have been performed in order to understand the behavior of interface states at the high-k/silicon interface. We have found that for all these materials, the interface states behave similar to P_b centers existing

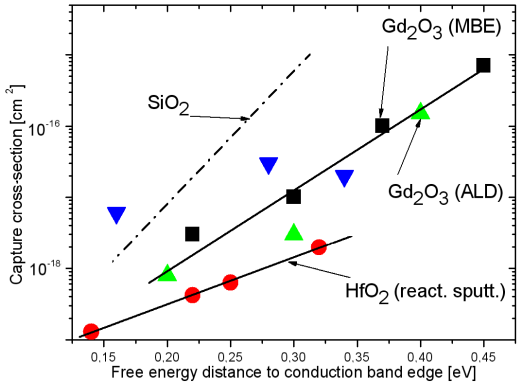

Fig. 17. Capture cross-section as a function of free energy distance between the silicon conduction band edge and interface states for Gd_2O_3 and HfO_2 compared with corresponding data for SiO_2.

at SiO_2/Si interfaces. The typical peaks at 0.2–0.3 eV from the band edges exist also in the case of the high-k materials (Fig. 16) and the mechanism for electron capture is of multiphonon type as earlier found for P_b centers at SiO_2/Si interfaces treated by gamma irradiation [20, 21]. This phenomenon was demonstrated to have the same physical background as that leading to an exponential energy dependence of capture cross-sections as shown in Fig. 17.

As future 22 nm and 16 nm node transistors probably will be produced in SOI technology, the lower C_E value mentioned above offers a large number of possibilities for gate dielectrics as seen in Fig. 15. This means that tunneling probably will not be the limiting factor. Instead the material choice will be governed by other properties like thermal stability and charge carrier traps. This has led us to activities on ternary compounds like GdSiO and LaLuO, which are examples of materials with high chemical stability.

2.4. Multi-gate devices

Multi-gate MOSFETs realized on thin films are the most promising devices for the ultimate integration of MOS structures due to the volume inversion in the conductive layer, leading to an increase in the number and the mobility of electrons and holes [22].

The on-current I_{on} of the MOSFET is limited to a maximum value I_{BL} that is reached in the ballistic transport regime. Figure 18 reports the self-consistent Monte Carlo (MC) simulation of the ballistic ratio BR = I_{on}/I_{BL} versus drain-induced-barrier-lowering (DIBL), which is one of the main short channel effects, showing that one can increase the BR by scaling the gate length, thus increasing the longitudinal field at the source, but this comes at the cost of a larger DIBL. For a given DIBL, an increased ballisticity is obtained for low doping double gate SOI devices [23].

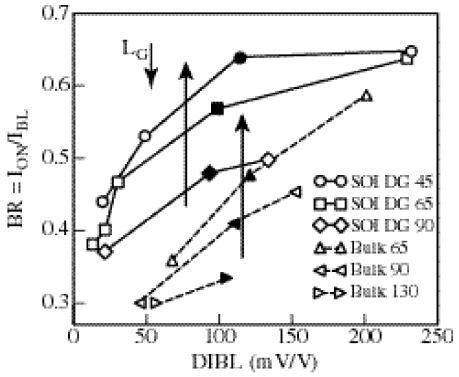

Fig. 18. Ballisticity ratio at $V_g = V_d = V_{dd}$ vs. DIBL. Filled symbols represent transistors with the nominal gate length for the high-performance MOSFET of each technology node.

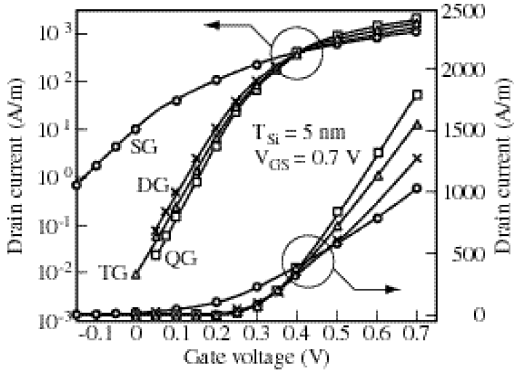

Fig. 19. $I_d(V_{gs})$ at $V_{ds} = 0.7$ V in thin layers for different multi-gate architectures.

The transfer characteristics of several multiple-gate (1, 2, 3 and 4 gates) MOSFETs, calculated using the 3D Schrödinger–Poisson equation and the non-equilibrium Green function (NGEF) formalism for the ballistic transport or MC simulations, have shown similar trends. The best performance (drain current, subthreshold swing) is outlined for the 4-gates (QG — quadruple gate or GAA — gate all around) structure [24, 25] (Fig. 19).

However, Fig. 20 demonstrates that the propagation delay in triple gate (TG) and quadruple gate MOSFETs are degraded due to a strong rise of the gate capacitance. A properly designed double-gate (DG) structure appears to be the best compromise at given off-sate current I_{off} [25].

Figure 21 compares the calculated ballistic drive current for Si and Ge double-gate MOSFETs at the operation point of each generation as predicted by ITRS [26]. Si barely satisfies the ITRS requirement, whereas Ge offers much higher current drive. However, the simulated value of the real drain current of

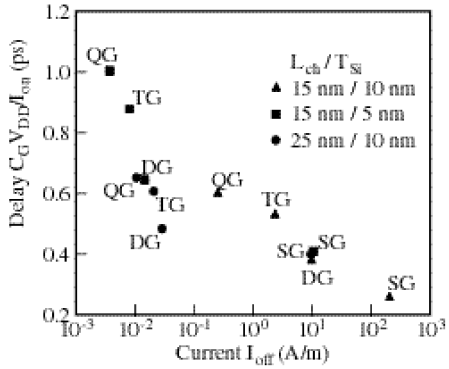

Fig. 20. Propagation delay versus I_{off} for single-gate and multi-gate SOI devices.

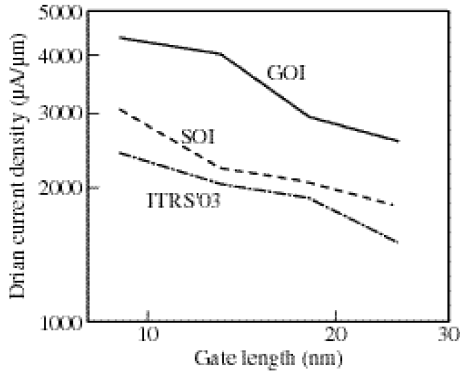

Fig. 21. Ballistic drive current for different technology nodes for SOI and GOI devices.

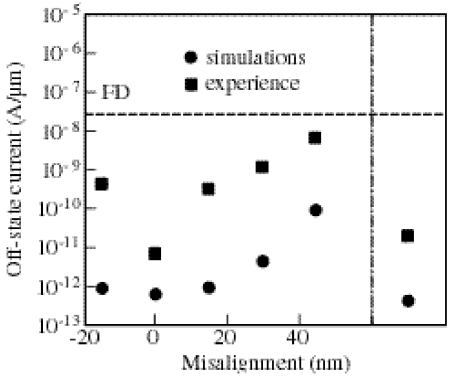

Fig. 22. Evolution of I_{off} with misalignment (experimental and simulations results, $V_{\text{d}} = 1.2$ V). Single gate FD results are represented in dashed line.

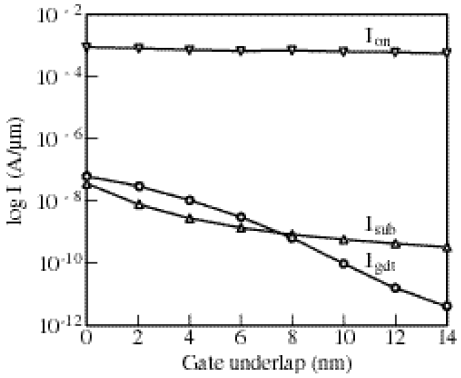

Fig. 23. I_{on}, subthreshold (I_{sub}) and gate direct tunneling (I_{gdt}) currents as a function of gate underlap.

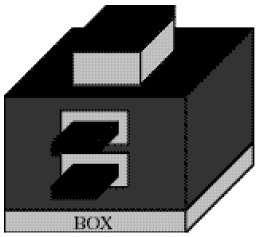

Fig. 24. Schematic diagram of MBCFET on SOI.

2G SOI transistors is not able to satisfy the ITRS objectives, even for intrinsic devices without parasitic S/D resistances. 2G GOI MOSFETs are able to provide the needed current drive, but parasitic resistances drastically affect the drain current (not shown here).

For a double gate device, the impact of a gate misalignment on the drain current is important. The impact of a gate misalignment is significant for I_{on} in 2G MOSFETs [27]. A large back gate (BG) shift reduces the saturation current compared to the aligned case, whereas a slight BG shift towards the source increases I_{on}. This is due to a lower source access resistance. In terms of short channel effects, aligned transistors exhibit the best control while highly misaligned MOSFETs operate like single gate ones. I_{off} is much more influenced by the misalignment than I_{on} due to a degradation of the electrostatic control (Fig. 22). The oversized transistor shows attractive static performance (right hand side of Fig. 22) and a larger tolerance to misalignment but the dynamic performance is rapidly degraded as the overlap length increases.

In decananometer MOSFETs, gate underlap is also a promising solution in order to reduce the DIBL effect. Figure 23 presents the variations of the driving current I_{on}, the subthreshold current I_{sub} and the gate direct tunneling current I_{gdt} versus gate underlap [28]. The on-current is almost not affected by the gate

underlap whereas the leakage currents are substantially reduced due to a decrease in DIBL and drain to gate tunneling current. A reduction of the effective gate capacitance C_g for larger underlap values at I_{on} has also been shown. This reduction of C_g leads to a decrease in the propagation delay and power.

In order to reach very high performance devices at the end of the roadmap, multi-bridge-channel MOSFETs (MBCFET) present very high driving currents larger than those of GAA devices and exceeding the ITRS requirements (Fig. 24) [29].

3. Beyond-CMOS

The background of the activities investigated in this field is concentrated on future emerging nanodevices because the CMOS roadmap predicts downscaling limits and the end of classical and non-classical CMOS in the first 2 decades of the current century. New devices and architectures are thus required, but a lot of physical phenomena and alternative fabrication approaches which could be useful for new devices are not completely understood. Investigations are pursued to overcome the limitations and to ensure reliable achievement in future nanoelectronics.

The objectives are to explore the horizon beyond CMOS, or beyond Moore, by following closely the emerging nano-sciences and -technologies for alternative silicon-based memory/logic devices.

3.1. Nanowires and carbon electronics

It has been shown previously that multi-gate architectures based on the concept of volume inversion are very promising in order to overcome the number of challenges for CMOS integration (short channel effects, driving current, etc.) down to decananometer gate length devices [22]. Gate-all-around semiconductors nanowires (NW) can be seen as the ultimate integration of these innovative nanodevices and present very interesting properties.

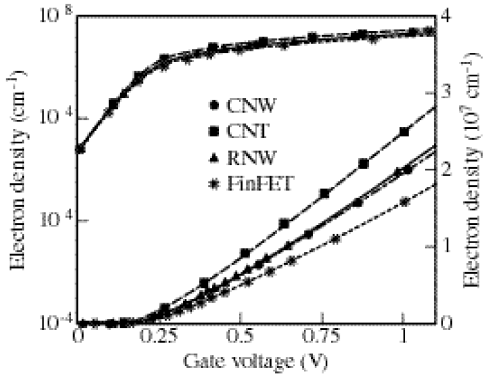

Fig. 25. Electron density per unit length for various devices (FinFET, nanowires and carbon-nanotube FETs). 65 nm technology node data (EOT = 0.9 nm, t_{si} = 5 nm).

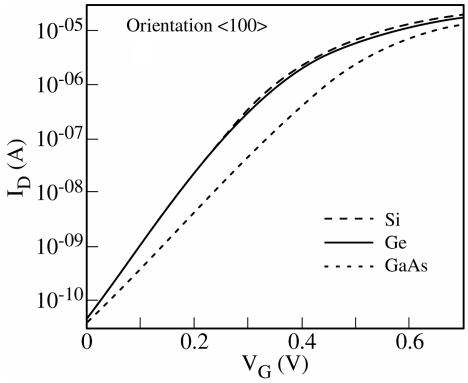

Fig. 26. $I_{\rm d}(V_{\rm g})$ characteristics calculated for Si, Ge and GaAs gate-all-around nanowires oriented along the [100] direction, with 4 nm wire diameter and 9 nm gate length; 1 nm gate oxide; $V_{\rm ds} = 0.4$ V.

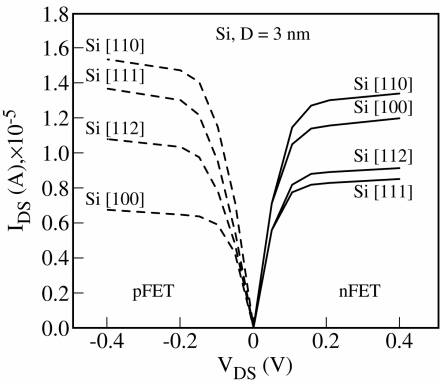

Fig. 27. $I_{\rm d}(V_{\rm d})$ characteristics calculated for n- and p-types Si nanowire FETs with four different channel orientations; 3 nm wire diameter, 8 nm gate length; 1 nm gate oxide; $V_{\rm ds} = 0.4$ V.

Therefore, it is interesting to compare the electrical properties of multi-gate devices with cylindrical and rectangular nanowires and with gate-all-around carbon nanotubes — CNT-FET. It is shown that the CNT-FET exhibits superior performance (Fig. 25) due to electron charge confinement at the surface of the nanotube, whereas in the Si-based nanowires the charge confinement at the center of the wire is responsible for an additional depletion capacitance in series with the oxide capacitance, which reduces the overall effectiveness of the gate [30]. However, the integration of these CNT-FETs on CMOS platform present many challenges that will be discussed below. On the other hand, it is worth noting that the performances of GAA nanowires, which could be realized using top-down technological processes, are larger than those obtained in FinFETs.

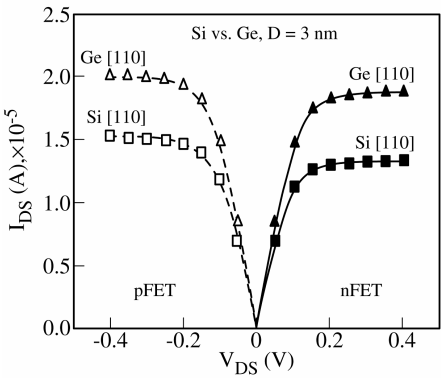

Fig. 28. $I_{\rm d}(V_{\rm d})$ characteristics calculated for Si and Ge nanowires FETs with [110] channel orientation; 3 nm wire diameter, 8 nm gate length; 1 nm gate oxide; $V_{\rm ds} = 0.4$ V.

Very small nanowires, with diameters in the sub-10 nm range, are compared for various channel materials and orientations using 3D quantum-mechanical simulations in pure ballistic regime [31]. Figure 26 shows the transfer current–voltage characteristics for a 9 nm long nanowire with a 4 nm diameter, the gate workfunctions being adjusted to provide identical off-current. The Si and Ge nanowires provide similar on-current, whereas the GaAs nanowire suffers from a high source-to-drain tunneling in the subthreshold region leading to a smaller $I_{\rm on}/I_{\rm off}$ ratio.

In Fig. 27, the output $I_{\rm d}-V_{\rm d}$ characteristics are calculated using full-band simulations with a ballistic FET model for Si n- and p-type nanowire FETs with four different channel orientations, 8 nm gate length and 3 nm wire diameter [32]. Due to the behavior of the transport effective-mass and valley degeneracy, it is demonstrated that [110] is the best orientation for n- and p-channels that offers the highest $I_{\rm on}$ for the same off-current for this 3 nm wire diameter. For this optimum channel orientation, Ge nanowires lead to an increase in $I_{\rm d}$ between 30 and 40% for p- and n-type devices, respectively, compared to Si nanowires (Fig. 28).

The variation of the intrinsic device delay with the wire diameter is shown in Fig. 29 for Si and Ge n- and p-type nanowires and various channel orientations [32]. p-channel nanowires display a monotonically increasing speed with decreasing the wire diameter, while the performance of n-channel nanowires highly depends on wire orientation and material.

The combination of strain effects with these 1D structures can lead to very high performance ICs for the end of the roadmap. Top-down bended gate-all-around nanowires have been fabricated in order to improve carrier mobility and driving current [33]. A bending induced by thermal oxidation in suspended nanowires is shown in Fig. 30. A maximum tensile strain is obtained in the middle of the wire.

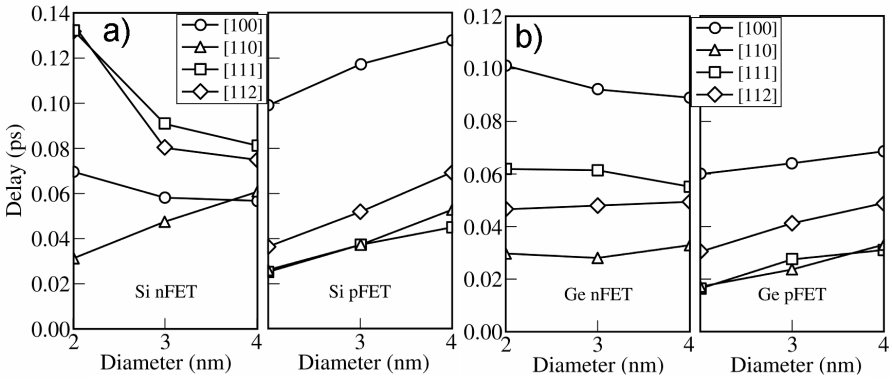

Fig. 29. Intrinsic device delay as a function of wire diameter for n and p Si and Ge nanowires FETs with various channel orientations; 8 nm gate length; 1 nm gate oxide; $V_{\rm ds} = 0.4$ V.

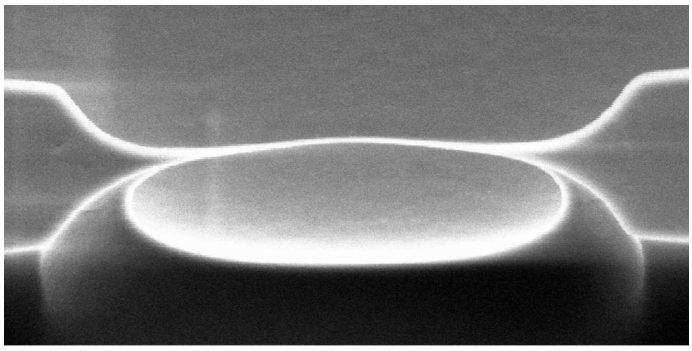

Fig. 30. Illustration of bending induced by thermal oxidation in suspended wires providing maximum tensile strain in the middle of the nanowire.

Tensile stresses from 200 MPa to 2 GPa can build-up in these suspended nanowires. The substantial enhancement of electron mobility in these structures is shown in Fig. 31.

One of the most promising future options to enhance Si-based ICs is the introduction of carbon electronics. These last years, many works have been devoted to carbon nanotubes, due to their remarkable electrical properties, as shown theoretically in Fig. 25. One major challenge for the implementation of CNT-based electronic circuits is a controllable assembly of CNTs onto electrodes. Recently, through surface functionalization using sodium dodecyl sulfate (SDS), we have succeeded in depositing individual semiconducting single-walled CNTs onto electrode pairs by means of ac dielectrophoresis [34]. The impact of Pd all-around contacts for SWNTs (Fig. 32a,b) is shown in Fig. 32c. The driving current has increased after the formation of all-around contacts with a high $I_{\rm on}/I_{\rm off}$ ratio.

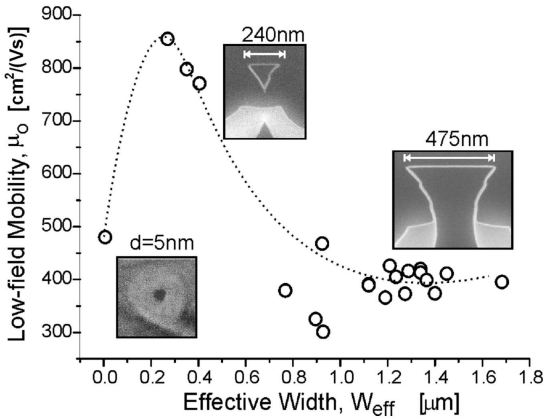

Fig. 31. Low field mobility versus nanowire cross-section highlighting the effect of tensile strain induced mobility enhancement in bended structures for $W_{\rm eff} < 1$ μm.

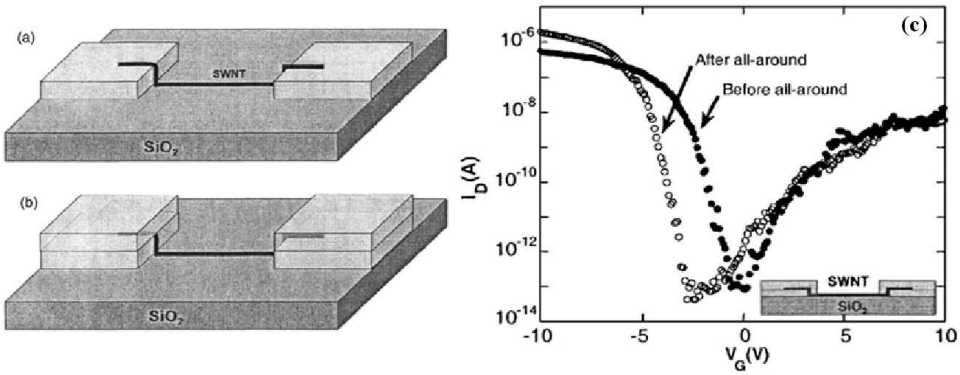

Fig. 32. Schematic of the process used for the formation of all-around contacts (a),(b); transfer $I_{\rm d}-V_{\rm g}$ characteristics for semiconducting single-walled CNTs before and after the formation of all-around contacts (c).

Another very recent solution for carbon electronics deals with the development of two-dimensional carbon sheets, which have been demonstrated to be thermodynamically stable. Graphene monolayers lead to excellent electronic properties with extremely high carrier mobility and to the possibility of using top-down CMOS compatible process flows. A back- and top-gated graphene flake has recently been studied, with a total length from source to drain of about 7 μm, a width of 265 nm and a gate length of 500 nm (Fig. 33). An ambipolar conduction controlled by the front and back gates has been observed, confirming that the field effect can be applied to graphene devices. Preliminary results show the impressive potential of graphene, with electron and hole mobilities around 4800 cm^2/(V s) in pseudo-MOS structures at 300 K, and mobilities in the range 500–700 cm^2/(V s) obtained in top-gated devices [35]. Band gap tuning by using for instance nanorib-

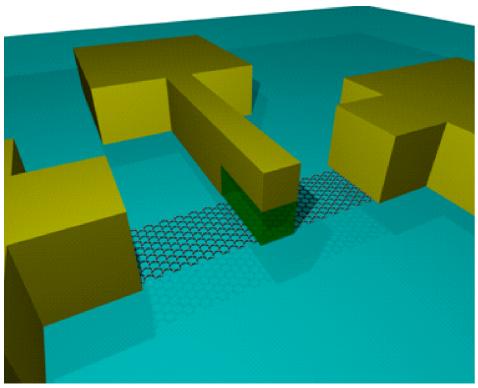

Fig. 33. Schematic of graphene field-effect devices.

bons or bilayer graphene could be used to improve gate modulation and device characteristics.

3.2. Templated self-organization

The main objectives of this work are the defined positioning of self-organized nanostructures, their functionalization, and the demonstration of routes toward their implementation on fabrication schemes for integrated devices.

The crucial step in exact positioning is given by the nucleation on patterned templates where the pattern is larger than the self-organized nanostructures. The material systems for starting are dots from silicon (Si)/oxide and SiGe/Si and catalyst/Si wires. The extension to other material systems is planned for coupled self-organization sequences (e.g. self-organized contact to self-organized dot, phase change structure on top of a transistor array). Functionalization is directed toward enhanced transport, carrier injection and storage, tunneling for novel write erase strategies, optoelectronic emission/absorption for optical interconnect. Device fabrication routes are demonstrated for nanodevices using templated self--organization. The economic prospects of the implementation of templated self--organization in the manufacturing process are assessed. A breakthrough for utilization of templated self-organization is envisioned which should pave a way to technical and economic benefits connected with a simpler manufacturing scheme.

We describe here recent progress of templated self-organization on nanostructure formation by different techniques and demonstration of functionalization.

Quantum dots (QDs) implementation in devices allows the improvement of device performances and the design of new device structures, however, it requires the control of QD locations. In order to define dot positions, molecular beam epitaxy growth of Ge in oxide window is employed. Besides its compatibility with Si technology, this positioning process is able to produce dislocation-free single Ge dots in selected areas. Figure 34 gives an example of a single Ge dot positioned in oxide window.

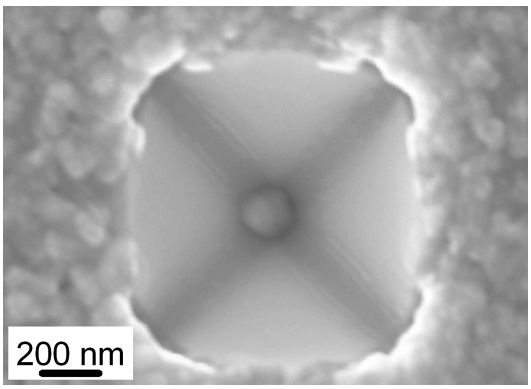

Fig. 34. Scanning electron microscopy image of Ge dot grown by molecular beam epitaxy in oxide window.

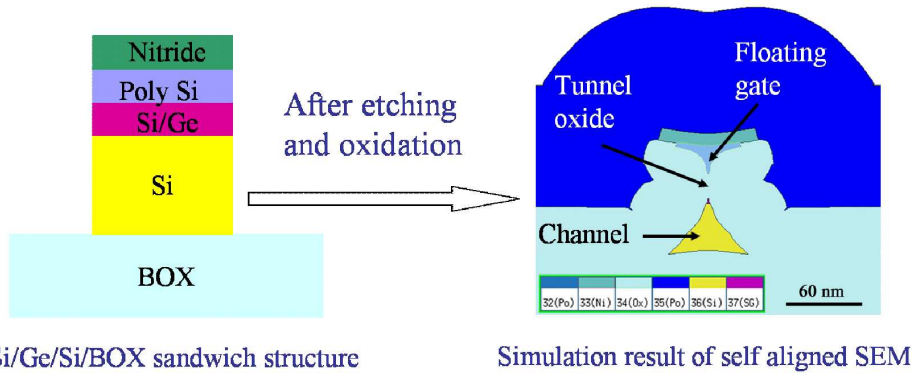

Fig. 35. Simulation of single-electron memory structure obtained by etching and oxidation of Si/Ge heterostructure.

Not only growth, also etching can be used for the fabrication of nanostructure. For instance, self-aligned single-dot memory based on arsenic-assisted etching and oxidation effects has been fabricated using the fastest etching rate of Si where As is at its peak concentration [36].

Another self-aligned process based on the etching and oxidation of SiGe heterostructure is investigated in order to form single electron memory (SEM). The etching and oxidation of Ge are faster than those of Si. By adjusting Ge/Si layer thickness the floating gate and the tunnel oxide of the SEM could be formed self aligned to the channel with well defined gate size and oxide thickness. Figure 35 shows the starting structure and the result of the process simulation where the channel, the tunneling oxide, and the floating gate of the SEM can be distinguished.

Bottom-up approaches for nanowires let us expect exciting properties. Vapor-liquid-solid (VLS) [37, 38] and vapor-solid (VS) [39] processes are chosen as

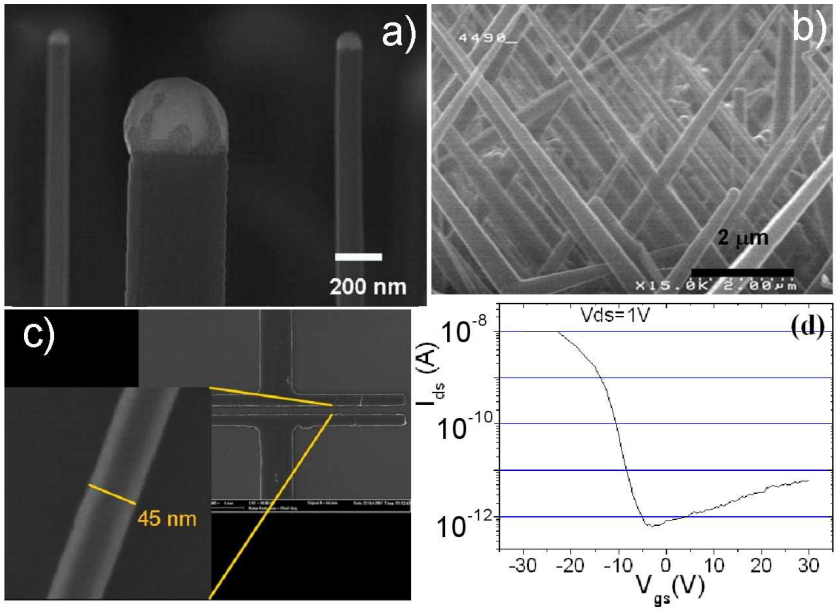

Fig. 36. Scanning electron microscopy of: (a) Si NWs grown with Au as catalyst, (b) Si NWs grown with PtSi as catalyst, and (c) 45 nm diameter connected NW. (d) $I(V)$ characteristic of a NW FET.

vehicles to generate Si quantum wires. The VLS method uses liquid Au-Si droplet as a catalyst to initiate the growth by chemical vapor deposition (CVD). A two-step process has been recently proposed to obtain very small diameter nanowires (< 10 nm). Firstly, the growth of large diameter NWs is realized. Depending on the growth conditions, gold nanoparticles could remain at the sidewalls of the wire directly after the growth. Then, experimental parameters are changed in order to grow the nanometric diameter NWs at the sidewalls, i.e. a nanotree with nanometric branches is formed [37, 38]. Nevertheless, gold particles introduce deep levels in silicon which is detrimental to device functionality.

Unlike Au-Si liquid droplet, the solid Pt-Si used as catalyst for VS process is fully CMOS-compatible, the nanowire growth direction being random (Fig. 36a,b) [39].

Nanostructure functionalization is important as it is the first step toward their implementation in device structures. Functionalization of Si nanowire is achieved through its implementation in FET device (Fig. 36c). The influence of the gate on the NWs conduction and a drain current modulation of about 4 orders of magnitude have been observed (Fig. 36d).

Other bottom-up processes have been developed for the CVD growth of Si nanowires and carbon nanotubes with CMOS-compatible catalysts (Al for Si NWs and Ge for CNTs [40]).

These results show a rapid progress in self-organized formation of nanostructures and a successful demonstration of Si nanowire functionalization.

3.3. Small slope switches

Even though the aggressive scaling will continue to play an important role in the future nanoelectronics, new technology drivers, such as *ultra-low power* and *new functionality* will open alternative ways for future high performance systems.

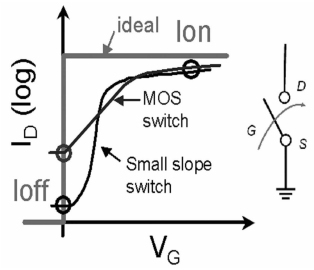

Fig. 37. Comparison of $I_{\rm off}/I_{\rm on}$ transition in ideal, small slope and MOS switches.

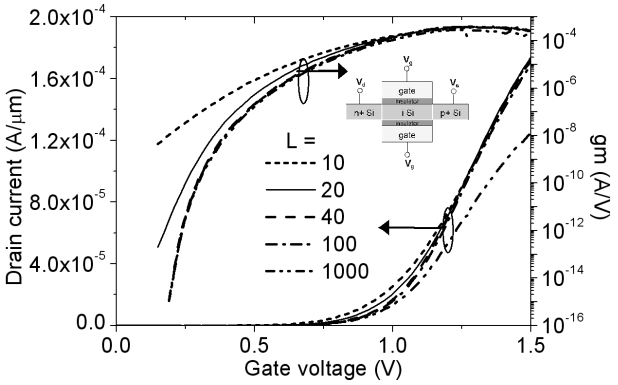

Fig. 38. Effect of gate length scaling from 1 μm down to 10 nm on $I_{\rm D}-V_{\rm G}$ and $g_{\rm m}-V_{\rm G}$ characteristics of high-k double-gate tunnel FET.

One interesting class of beyond CMOS devices are the small slope switches. A small slope electronic switch (Fig. 37) is defined here as a solid-state semiconductor device showing a value of the subthreshold slope smaller than the 60 mV/decade limit for a conventional MOSFET, set by the Boltzmann distribution at room temperature. The smaller the value of S, the more abrupt the transition from the off- to the on-state and closer the switch to the ideal case. Benefits of small slope switches are the ultra-low standby power due to a very low $I_{\rm off}$ but also the high-speed potential and dynamic power savings, since less

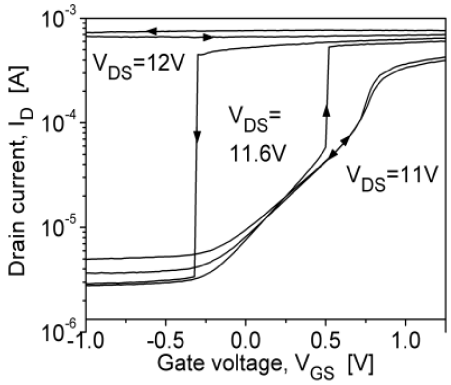

Fig. 39. Abrupt switching in PIMOS due to impact ionization and bipolar onset.

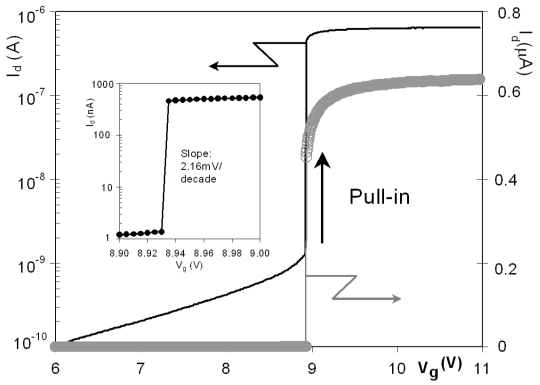

Fig. 40. Abrupt switching in SG-MOSFET due to electro-mechanical non-equilibrium (pull-in effect).

power is drawn per transition when the subthreshold slope is more abrupt. Development of small slope switches requires exploration of new physical principles for very abrupt off-on transition, such as: (i) impact ionization, (ii) band-to-band tunneling and (iii) electro-mechanical instability, solutions that are the candidates analyzed in this work. It is worth noting that all these small slope device architectures can be implemented as extensions of advanced silicon CMOS or by hybridization of silicon CMOS with other compatible technologies (SiGe, CNT, nano-electro-mechanical).

The tunnel FET [41–43] is a gated $p{-}i{-}n$ diode with a gate over the intrinsic region; it exploits the gate controlled electron tunneling from the valence band of the p-region to the conduction band of the i-region for reversed biases, resulting in very abrupt off-on transition. They have been reported on Si, III–V and CNT alternatives. High-k tunnel FETs can be scaled to shorter lengths before important characteristics such as transconductance, $I_{\rm on}/I_{\rm off}$, and subthreshold swing are degraded (Fig. 38). Optimized silicon body of 7–8 nm (for $L_{\rm g} = 50$ nm) in double-

-gate tunnel FET with high-k dielectrics leads to improved characteristics with higher I_{on} ($I_{on}/I_{off}\#10^{11}$) and smaller subthreshold swing (average: 57 mV/dec — minimum point swing: 11 mV/dec) [43].

The IMOS (impact ionization MOS) device, a partially-gated pin device, where it is possible to modulate the breakdown voltage by a gate voltage to abruptly switch from the off-state to the on-state with less than 10 mV/decade, was proposed in [44]. Recently, a new punch-through impact ionization MOS (PI-MOS) transistor, more scalable than IMOS and free of hot carrier degradation, has been demonstrated on low doped body, Ω-gate MOSFET architecture, Fig. 39 [45].

The suspended-gate FET (SG-FET) is a hybrid solid-state micro-electro-mechanical device, for which both abrupt and 1 T memory functions [46, 47] can be obtained using the electro-mechanical instability (at pull-in and pull-out voltages, see Fig. 40) of a mobile gate over the channel region of a MOSFET. SG-FET is scalable (using silicon nanowires or taking advantage of CNT technology) and behaves as dynamic threshold voltage transistor, with a high threshold voltage V_T at low bias voltage V_G and low-V_T at high V_G, which makes it very attractive as power management switch.

4. Advanced modeling and characterization

The main objective of the development of advanced modeling and characterization methods in nanoscale devices is to tackle the main device physical challenges foreseen for the 22-16 technology nodes and beyond, namely mobility enhancements, off currents, interface effects, low dimensional transport.

For instance, the physical understanding of mobility in new CMOS technologies is a formidable challenge both from the viewpoint of the experimental characterization and of the modeling. One of the major effort is aimed to develop and validate various measurement techniques ($I-V$, split $C-V$, MR, etc.) for the experimental determination of the mobility and to address the relative importance of the different scattering mechanisms (phonons, charges, roughness and strain impact) by using magneto-transport measurements versus gate voltage and temperature, as well as external strain effects [48].

The determination of mobility relies on very rigorous approaches starting from the calculation of the sub-band structure for the 2D carrier gas and of the corresponding scattering rates. For the pMOS transistors the problem arises of an efficient method to be used to describe the hole dispersion energy in the inversion layer. In this frame a new semi-analytical model for the energy dispersion of hole in inversion layers (Fig. 41a) [49] has been used to develop a multi subband Monte Carlo (MSMC) simulator for pMOSFETs. The transport model has been successfully calibrated on experimental mobility data (Fig. 41b). This approach can be extended to the study of strained layers and Ge pMOSFETs and to the simulation of nanoscale transistors.

Figure 42 shows an example of a comparison of different models developed for nanowires. The carrier distribution function is calculated as a function of

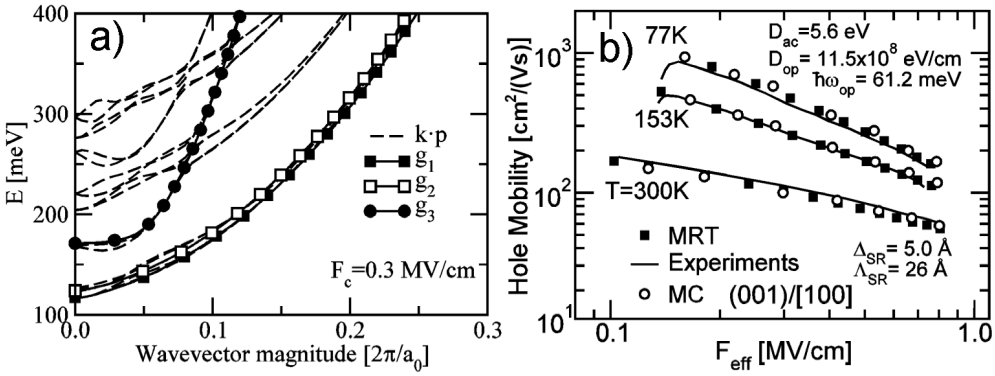

Fig. 41. A new semi-analytical model for the energy dispersion of hole in inversion layers has been used to develop a MSMC simulator for pMOSFETs (a). The transport model has been successfully calibrated on experimental mobility data (b).

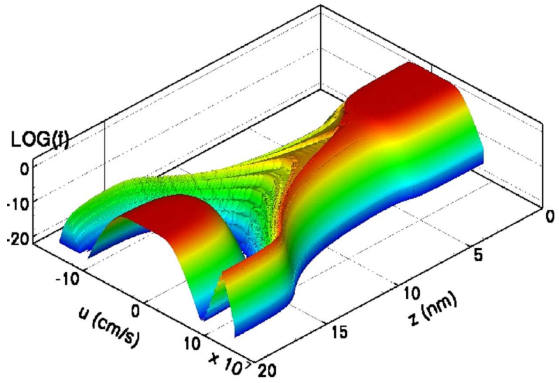

Fig. 42. Electron distribution function in a silicon nanowire as a function of energy, velocity and position.

energy, velocity, and position, in a silicon nanowire using a deterministic solution of the Boltzmann transport equation [50]. The calculated currents are shown in Fig. 43. A significant drop of the driving current is obtained when the scattering mechanisms are turned on compared to the ballistic case.

Figure 44 shows the study of the scattering from random dopants, which is a one of the biggest sources of variability, in n-channel nanowires using full self-consistent 3D Poisson-NEGF simulations [51]. Three cases are considered, two of them have a discrete donor in the channel (DM: located at the middle of the cross-section, DA: donor located close to the SiO_2 interface), the third one has a discrete acceptor. The device without impurity is shown for comparison. The off-current is substantially increased in the cases of DM and DA due to two effects: the decrease in the gate barrier because of the presence of the attractive impurity and secondly the resonant tunneling structure induced by the impurity potential.

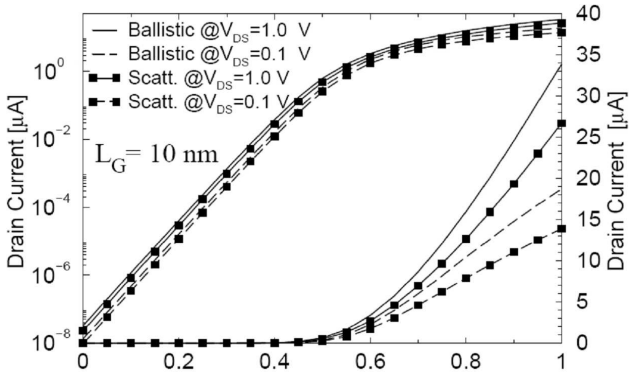

Fig. 43. Turn-on characteristics of the cylindrical NWs with $L_g = 10$ nm.

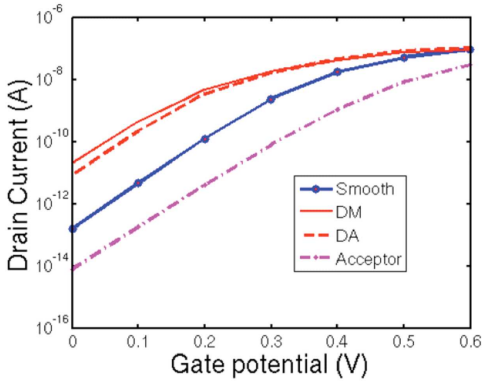

Fig. 44. Transfer $I_d - V_g$ characteristics of n-channel nanowires for smooth and different discrete dopants: donor (DM, DA) and acceptor cases.

The acceptor impurity device has the lowest current due to the repulsive barrier of the acceptor [52]. This theoretical analysis demonstrates the major importance of the variability studies for the optimization of future semiconductor devices.

5. Conclusion

A number of recent advances obtained in the more Moore and beyond-CMOS activities have been presented. These researches, mainly devoted to N+4 technology node and beyond for studying and validating new concepts, novel materials and technologies, innovative device architectures, will enable us to overcome the number of research challenges of ultimate CMOS and post-CMOS nanodevices in order to speed up technological innovation for the nanoelectronics of the next 2–3 decades.

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