A CMOS Neural Interface for a Multichannel Vestibular Prosthesis

Kristin N. Hageman, Zaven K. Kalayjian, *Member, IEEE*, Francisco Tejada, *Member, IEEE*, Bryce Chiang, Mehdi A. Rahman, Gene Y. Fridman, Chenkai Dai, Philippe O. Pouliquen, *Member, IEEE*, Julio Georgiou, *Senior Member, IEEE*, Charles C. Della Santina, and Andreas G. Andreou, *Fellow, IEEE*

***Abstract*—We present a high-voltage CMOS neural-interface chip for a multichannel vestibular prosthesis (MVP) that measures head motion and modulates vestibular nerve activity to restore vision- and posture-stabilizing reflexes. This application specific integrated circuit neural interface (ASIC-NI) chip was designed to work with a commercially available microcontroller, which controls the ASIC-NI via a fast parallel interface to deliver biphasic stimulation pulses with 9-bit programmable current amplitude via 16 stimulation channels. The chip was fabricated in the ONSemi C5 0.5 micron, high-voltage CMOS process and can accommodate compliance voltages up to 12 V, stimulating vestibular nerve branches using biphasic current pulses up to 1.45 ± 0.06 mA with durations as short as 10 μs/phase. The ASIC-NI includes a dedicated digital-to-analog converter for each channel, enabling it to perform complex multipolar stimulation. The ASIC-NI replaces discrete components that cover nearly half of the 2nd generation MVP (MVP2) printed circuit board, reducing the MVP system size by 48% and power consumption by 17%. Physiological tests of the ASIC-based MVP system (MVP2A) in a rhesus monkey produced reflexive eye movement responses to prosthetic stimulation similar to those observed when using the MVP2. Sinusoidal modulation of stimulus pulse rate from 68–130 pulses per second at frequencies from 0.1 to 5 Hz elicited appropriately-directed slow phase eye velocities ranging in amplitude from 1.9–16.7°/s for the MVP2 and 2.0–14.2°/s for the MVP2A. The eye velocities evoked by MVP2 and MVP2A showed no significant difference (t-test, $p = 0.34$), suggesting that the MVP2A achieves performance at least as good as the larger MVP2.**

***Index Terms*—Application specific integrated circuit (ASIC), electrical stimulation, neural engineering, prosthesis, vestibular implant, vestibulo-ocular reflex (VOR).**

I. Introduction

THE vestibular labyrinth of the inner ear senses head rotation and head orientation, driving reflexes that maintain stable vision and posture during head motion. The labyrinths' angular velocity sensors are toroidal semicircular canals (SCCs). The three SCCs in one ear are coplanar to those in the contralateral ear, forming three mutually orthogonal pairs, the horizontal pair (HZ) comprising the left horizontal (LH) and right horizontal (RH) SCCs, the LARP pair comprising the left anterior (LA) and right posterior (RP) SCCs, and the RALP pair comprising the right anterior (RA) and left posterior (LP) SCCs. The mutually orthogonal orientation of the pairs allows for any 3-dimensional head movement to be decomposed and projected onto the planes of each SCC pair.

Sensory hair cells located in each SCC ampulla transduce head movements, modulating the spike frequency of neuronal activity in the corresponding ampullary nerves. Afferent neurons from the six SCCs spontaneously fire at nonzero rates when the head is motionless, and they encode head angular velocity by either upward (excitatory) or downward (inhibitory) rate modulation of neuronal firing around this baseline rate. Head rotation in the plane of a given pair of SCCs elicits complementary changes in firing rates of afferents innervating the SCCs on either side of the head. For example, turning the head to the left will excite neurons innervating the LH SCC while inhibiting neurons innervating the RH SCC. These changes in firing rate are processed in the brainstem to generate control signals for extraocular muscles. These muscles are arranged in pairs that are approximately coplanar with the three pairs of SCCs, driving the 3-dimensional vestibulo-ocular reflex (VOR) and postural reflexes [1].

Damage to an individual's vestibular labyrinths disables the VOR, causing blurry vision during head movements and consequent loss of visual acuity. It also causes postural instability, chronic disequilibrium, and reduced quality of life [2]–[4]. Currently, there is no adequate treatment option for individuals with severe bilateral vestibular deficiency (BVD) who fail to compensate despite vestibular rehabilitation exercises. However, the past decade has witnessed increasing interest in developing a vestibular prosthesis that can sense head motion and drive vestibular nerve fibers [5]–[17]. The Johns Hopkins Vestibular NeuroEngineering Lab's multichannel vestibular prosthesis (MVP) architecture comprises motion sensing circuitry, a microcontroller, and a neural interface (schematized in Fig. 1 and further detailed in [5], [16]). Motion sensor signals are converted to current pulses where magnitude, direction, duration, and timing are controlled by a microcontroller to generate variations in vestibular nerve afferent activity to emulate normal physiological encoding of head movement. (For review see [18]).

Fig. 2 represents the design progression of the MVP system. The 1st and 2nd generation MVP system (MVP1 Fig. 2(a)

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K. N. Hageman, B. Chiang, M. A. Rahman, G. Y. Fridman, C. Dai, and C. C. Della Santina are with the Vestibular NeuroEngineering Lab (affiliated with the Departments of Biomedical Engineering and Otolaryngology Head and Neck Surgery), Johns Hopkins School of Medicine, Baltimore, MD 21205 USA (e-mail: kristin.hageman@jhmi.edu).

Z. K. Kalayjian, F. Tejada, P. O. Pouliquen, and A. G. Andreou are with the Department of Electrical and Computer Engineering, Johns Hopkins University, Baltimore, MD 21218 USA.

J. Georgiou is with the Department of Electrical and Computer Engineering, University of Cyprus, 1678 Nicosa, Cyprus.

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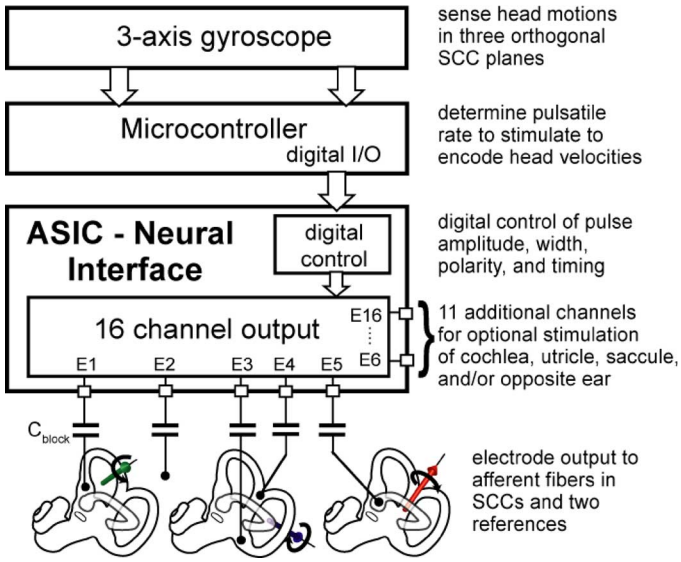

Fig. 1. Architecture for the Multichannel Vestibular Prosthesis (MVP) system. A mixed-signal application-specific integrated circuit neural interface (ASIC-NI) provides an interface to the afferent fibers located in each semi-circular canal (SCC) of the vestibular labyrinth. The chip incorporates 16 stimulation channels, each with its own 9-bit digital-to-analog converter (DAC) current source or sink. E1, E3, and E5 provide stimulation to the three SCCs, while E2 and E4 are the body and common crus reference electrodes respectively. 11 electrodes remain for expanding stimulation to the cochlea, utricle and saccule, and/or the opposite ear semicircular canals.

and MVP2 Fig. 2(b)) were designed with a semi-implantable approach, using a percutaneous connection between implanted electrodes and external motion sensors, processing circuitry, and the power source. The MVP2 requires this connection to deliver stimulation to the ampullary nerves. To avoid the issue of decoupling, which would cause loss of stimulation from the prosthesis and sudden onset of vertigo due to loss of baseline stimulation, the design goal for the next generation MVP (MVP3) is intended to be a fully implantable system. For fully implantable vestibular devices, size and power consumption are key considerations, driving need for custom, low-power integrated circuit (IC) design.

Multiple groups have recently reported on efforts to develop ASIC-based stimulators for incorporation into vestibular implants, including a system based on a field-programmable analog array [19], a custom ASIC-based system including telemetry, power and stimulation management [20]–[22] and an ASIC-based system incorporating motion sensors [23]. Here we report on a complementary metal-oxide semiconductor (CMOS) application specific integrated circuit neural interface [ASIC-NI, Fig. 2(c)] that was designed according to the MVP architecture [24]. This design provides the ability for pulsatile stimulation with pulses as short as 10 μs/phase, amplitudes as high as 1.45 mA, and rates up to 12 kHz. The use of independent DACs in each of the 16 electrode channels allows for multipolar stimulation. The ASIC-NI is integrated with the MVP system by replacing the highlighted area of the MVP2 in Fig. 2(b) to create the MVP2A. With the ASIC-NI, the MVP system provides equivalent stimulation to previous MVPs, but with a notable size and power consumption reduction. This size reduction is a first step toward reaching our system size goal to use the existing hermetic can of an implantable cochlear implant [25]–[27]. Outlines of existing cochlear implants are shown in Fig. 2(d) for size comparison.

II. ASIC-NI Design Overview

The ASIC-NI was designed to adhere to the existing control scheme of the MVP system. This custom design organizes the signals from the microcontroller, i.e., pulse amplitude, polarity, and timing, to efficiently produce the desired stimulation.

A. High Compliance-Voltage Programmable Current Stimulation

Delivering a given amount of charge per phase using short duration pulses achieves more selective stimulation of the vestibular nerve [28] and reduces the likelihood of timing clashes that occur with longer-duration pulses. However, achieving the desired charge per phase with short duration pulses requires higher current levels. This in turn demands the use of a relatively high compliance voltage and circuit elements that can withstand higher voltage levels. The MVP requirements for electrode impedance and stimulation current output range dictate that the neural interface chip operate at compliance voltages that exceed typical maximum voltages for standard CMOS processes. Therefore, the high-voltage OnSemi C5F/N CMOS process was used for design and fabrication of the ASIC-NI for the MVP. Compliance voltages of up to 12 V are achieved using this process by virtue of high-voltage (HV) transistors featuring lightly doped drains (LDD) and thick gate oxides.

Each stimulation channel is individually addressed and programmed by the external, commercially available microcontroller through a digital multiplexer. Inside each channel, a 10-bit buffer stores the 9-bit current amplitude and 1-bit current direction. A global STIM signal is used to activate all channels simultaneously and provide stimulation.

Each ASIC-NI stimulation channel consists of a 9-bit DAC, a *partial current steering* circuit to obtain bipolar pulses, and control registers. The 9-bit DAC is a unary type current source array laid out in a common centroid arrangement to minimize mismatch. Current source transistor sizes were computed using a statistical yield model based on fabrication process parameters in order to achieve maximal inter-channel matching within die area constraints [29]. Each DAC is programmed and activated independently for maximal stimulation flexibility.

To maximize battery life for a prosthetic stimulating device, the power consumption of the neuroelectronic interface must be limited. We implemented each stimulation sub-circuit using a *partial current steering* design similar to that described in [30] but realized using a high voltage, augmented differential pair amplifier with a wide range output stage (circuit and transistor sizes shown in Fig. 3). This stimulation sub-circuit maximizes charge delivery while keeping stimulus pulses brief enough to allow high pulse rates up to 12 kHz (using minimum pulse duration of 10 μs/phase and minimum interphase gap (IPG) of 25 μs). Low-voltage transistors were used in the current source array for their superior matching properties. High voltage cascode transistors were employed to shield these low-voltage transistors from large voltage swings. The differential pair

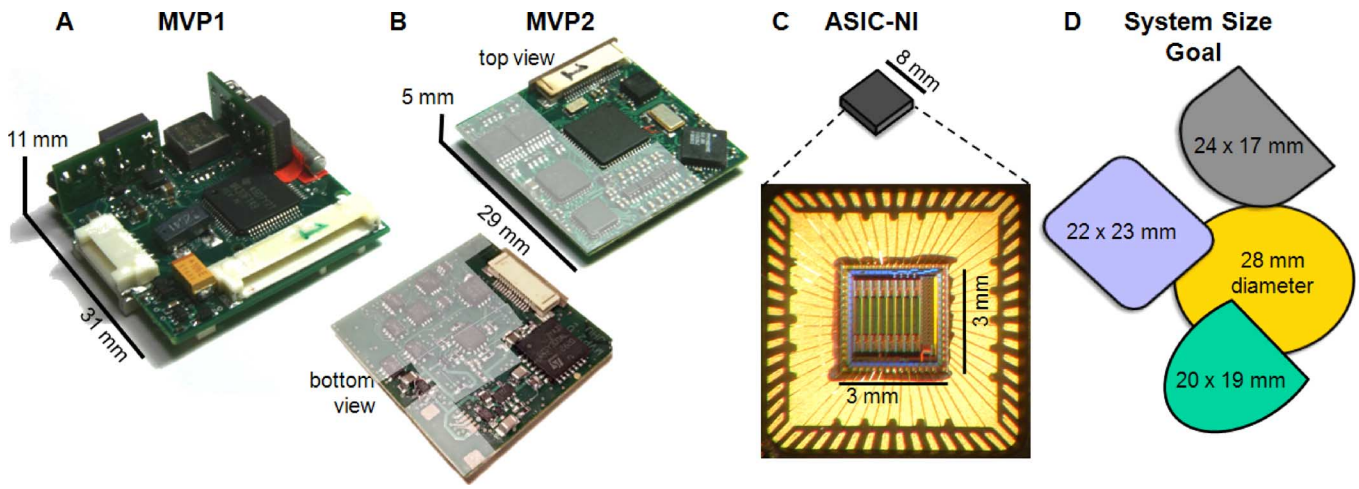

Fig. 2. (a) The first generation Multichannel Vestibular Prosthesis, MVP1, occupied 31 mm × 31 mm × 11 mm and consumed 100 mW [5]. (b) Top and bottom views of the 2nd generation MVP2, which decreased in area, thickness and power consumption to 29 mm × 29 mm × 5 mm and 70 mW [16]. The highlighted area on the MVP2 ($\sim$ 866 mm^2) indicates discrete analog elements replaced by the (c) 64 mm^2 QFN56A package for our Application Specific Integrated Circuit neural interface (ASIC-NI) and a photomicrograph of the fabricated chip in this package. The ASIC-NI allows for 48% size reduction in the MVP system size – which provides a significant first step to meet our system size design goals, shown in (d). The outlines in (d), drawn to scale with the MVP1 and MVP2, show the sizes of the hermetic cans of commercially available cochlear implants [25]–[27].

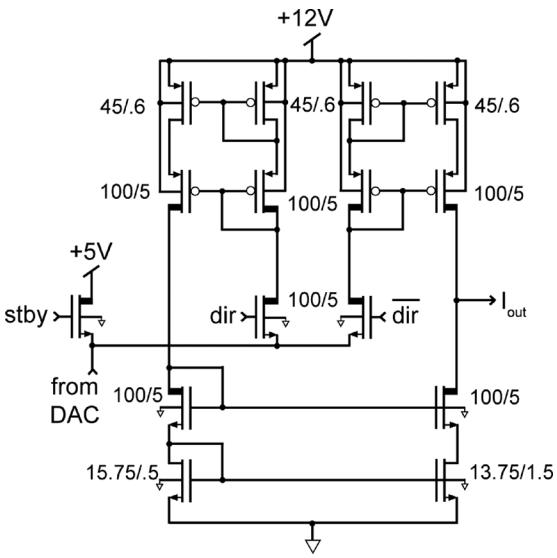

Fig. 3. A high voltage steering circuit based on an augmented differential pair and cascode transistors with lightly doped drains (thick lines). Transistor sizes are indicated next to each transistor. The compliance voltage, Vcomp, can be 5–12 V. The signal *dir*, supplied by the microcontroller, controls the direction of stimulus current (amplitude set by each channel's DAC). An additional signal *stby*, also provided by the microcontroller, is employed to minimize power consumption by putting the interface circuit into a standby state between pulses.

and standby path transistor are composed of HV transistors with gate signals constrained to a maximum of 5 V; thus, the maximum voltage the DAC can see during normal operation is 5 V.

The *partial current steering* circuit shown in Fig. 3, provides three paths for current flow; one dummy path, one for cathodic pulses, and one for anodic pulses. When control registers for a channel are assigned for current stimulation but stimulation is not yet initiated, the DAC is activated and the current steering circuit is put on standby (*stby*). In this state, the programmed current is steered toward a low-voltage (5 V) dummy load. This allows a lower voltage on the dummy path transistor, yielding lower power consumption in standby mode and simultaneously allowing the DAC current output to relax from charge-up transients. When the signal to enable stimulation is received from the microcontroller, indicating the start of the biphasic pulse, the standby circuit path is disabled and one of the differential pair transistors is activated based on the current direction (*dir*) signal, which chooses either anodic or cathodic current stimulation output. A non-overlapping switching network is used to switch between the dummy output path and the actual electrode output. This method of *partial current steering* has been effectively used to minimize power in a similar neural simulator [30]. A differential pair is then used to steer the circuit into HV current mirrors, which either source or sink the programmed current into the electrode output, depending on the channel setting.

The impedance of the output stage measured from the results of the output simulation is approximately 1.8 GOhm. This was determined at a bias current of 300 μA and an output voltage of $\mathrm{Vdd}/2$.

III. Bench Test Methods and Results

A. ASIC-NI Bench Test Methods

Each ASIC-NI's stimulating channel's DAC was initially tested using a 5 V compliance voltage. All registers were cleared by a power cycle reset, and then output current levels were measured for each of the 16 channels for every possible 9-bit DAC command input. The DAC output current was measured using a Source Measurement Unit (SMU) with the output stage clamped at 2.5 V. Once DAC functionality was verified, tests were repeated with the compliance voltage increased to 12 V.

After integration of the ASIC-NI into a MVP2A system board (which includes off-the-shelf MSP430F149 microcontroller (Texas Instruments, Dallas, TX), supply voltage regulation,

TABLE I
RESULTS MEASURED FROM THE ASIC-NI.

Characteristic	Measured Value
Stimulator Characteristics	
Max Current output	1.45±0.06 mA
Output Current Resolution	9 Bits
Relative Accuracy (max)	±5 LSB
Differential non-linearity	±0.8 LSB
Offset error	±0.2 % of Full Scale
Gain error	±6 LSB
Output Current Settling Time	360±50 ns
Charge Balance	3.6±2.5 %
Current Out Channel Isolation	-39±10 dB (at 1kHz)
Power Requirements	
AV_{dd} – core	5 V
AV_{dd} – output stage	12 V
DV_{dd} – core	5 V
Quiescent Power Consumption	7.4±0.2 mW
Active Power Consumption*	7.7 mW

*Calculated as described in Section III.B.3 using typical MVP stimulation parameters of 94 pps baseline on 3 channels, with biphasic pulses of 150 μs/phase and 120 μA.

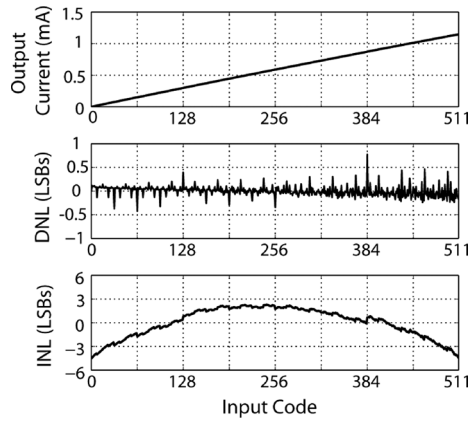

Fig. 4. Representative DAC output from one channel of one ASIC-NI channel. This was recorded with Vcomp set to 12 V and maximal current output at 1.2 mA. Current output was measured using a Source Measurement Unit with the ASIC-NI output clamped at 2.5 V. Over the full range of DAC operation, the output is highly linear (top), differential non-linearity error (DNL, middle) is $\leq$ 0.8 LSB, and integral non-linearity (INL, bottom) remains within 5 LSB of ideal. The linearity in the DAC is more than adequate for the intended application of the DAC as a programmable interface for a prosthesis.

DC-blocking capacitors, and other components), stimulus current measurements were repeated with the device set to deliver 150 μs/phase, biphasic, symmetric current pulses with amplitude ranging from 0–1.45 mA between pairs of electrodes immersed in isotonic saline (0.9% NaCl). Bare 90% Pt/10% Ir electrodes of contact area 51,000 μm^2 (area equivalent to that of our *in vivo* electrodes, and therefore similar impedances) each were constructed by stripping Teflon™ insulation from the distal 200 μm of 75 μm diameter wires, each of which was connected to an ASIC current source or sink via a series combination of a 1 μF DC-blocking capacitor and a 10 Ohm sense resistor used for current measurement.

Power consumption of the ASIC-NI was measured using 10 Ohm sense resistors for each of the three power supply lines for the ASIC-NI (DVDD, AVDD, and V_{comp}). Quiescent power consumption was measured with output current set to 0 μA across all ASIC-NI output channels. The instantaneous power consumption during a pulse output was measured at varying output currents, allowing for calculation of total operating power consumption based on current amplitude and duty cycle of pulse output.

B. ASIC-NI Bench Test Results

1) ASIC-NI Performance: Table I summarizes bench performance results for the ASIC-NI. The DAC current output was measured and differential non-linearity (DNL), and integral non-linearity (INL, also termed relative accuracy) were calculated for all channels (n = 16) on one ASIC-NI chip with a 12 V compliance voltage. Representative data from one output channel is shown in Fig. 4. Using a best-fit method, the DNL magnitude is $<$ 0.8 least significant bit (LSB), and the maximum INL deviation from ideal was 5 LSB.

The output current settling time was measured using the maximum current output for the chip to calculate a worst case settling time. Both rise and fall times averaged 360 $\pm$ 50 ns. (n = 12, four channels on each of three separate chips). This fast current settling time allows for short duration pulses with a maintained square pulse shape. The shortest pulse duration possible with the ASIC is 10 μs.

The ASIC was designed to be used with DC-blocking capacitors to maintain charge balance between biphasic pulses. The charge balance between the cathodic and anodic phases without the DC-blocking capacitors was measured across five source-sink pairs on two separate ASICs. Data was collected from the ASIC output for 10 seconds, with each pair programmed at 100 pps, 150 μs/phase, 120 μs IPG, at four different current amplitudes. The average difference in charge delivered between the cathodic and anodic phases without the DC-blocking capacitors is 3.6% $\pm$ 2.5%.

Current output channel isolation was measured by delivering a 1 kHz square pulse from one channel while all other channels were off. The frequency content seen at the output of neighboring channels was measured to quantify channel isolation. The average channel isolation was -39 dB $\pm$ 9 dB, measured over all channels on two ASICs.

Fig. 5 shows the DAC current output amplitude from three channels on each of three ASIC-NIs for 15 individual DAC input codes (between 0–511) as the compliance voltage is increased from 5 V up to the maximum 12 V. At low compliance voltages, the current output begins to saturate. With the high compliance voltage, the DAC is nearly linear over a wider range and achieves higher current output. The difference in maximum current magnitude between Figs. 4 and 5 is due to differences in measurement procedure. For Fig. 4, the output node of the ASIC-NI was clamped at 2.5 V with an SMU. For Fig. 5, a more realistic experimental set-up using electrode wires in saline, was used to measure the current output.

2) MVP System Size: Replacing multiple discrete and off-the-shelf components of the MVP2 with the ASIC-NI significantly decreased the size of the MVP system (Fig. 2). Whereas the MVP2 represents only a 12% reduction in circuit board area from the first generation MVP1 [Fig. 2(a)], the MVP2A replaced all of the MVP2's stimulation circuitry [highlighted

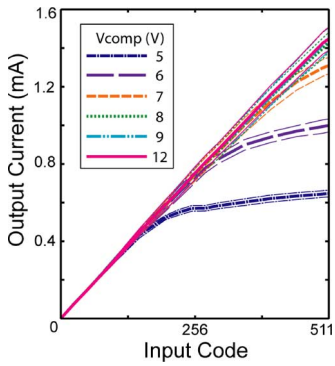

Fig. 5. Average current output (thick lines) from three ASIC-NIs, three channels from each ASIC-NI (n = 9) using different voltages applied to the compliance voltage pin of the ASIC-NI (V_{comp}). Current values were measured at 15 input codes with a 120 Ω sense resistor for measuring current, in series with a 1 μF coupling capacitor connected to a 75 μm Pt-Ir wire electrodes with Teflon-insulation stripped 0.2 mm and placed in normal saline (0.9% NaCl). DAC performance is linear for (V_{comp}) $\geq$ 8 V, reaching maximum current levels of around 1.45 $\pm$ 0.06 mA. The current output saturates as current is increased when using a V_{comp} below 8 V. Standard deviations (thin line) ranged from $\pm$2.2% to $\pm$4.5% of the current magnitude. All values were collected using the same pulse rate and pulse duration.

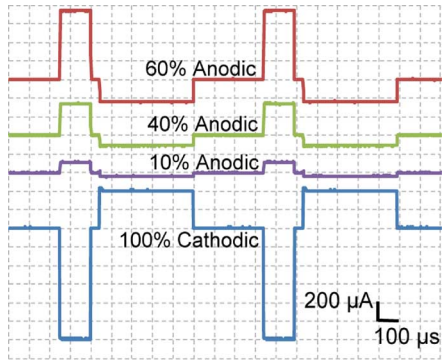

Fig. 6. Two delayed pseudo-monophasic multipolar pulses for current steering [46] using four of the 16 stimulus output channels from the ASIC-NI, delivering pulses at 1 kHz. Although, the MVP uses a mono-polar configuration with charge-balanced, symmetric, biphasic pulses for stimulation this demonstrates the versatility in using the ASIC-NI. First phase: 150 μs with the main stimulating source supplying a 1.2 mA cathodic pulse (bottom trace), while return electrodes steer current at 60%, 30%, and 10% returns of the total source. Interphase gap (IPG): 50 μs; Second phase: 450 μs pulse width, main current source at 400 μA to maintain charge balance and return electrodes. Each channel's load was a 120 Ω sense resistor in series with a 1 μF coupling capacitor connected to a 75 μm Pt-Ir wire electrodes with Teflon-insulation stripped 0.2 mm and placed in normal saline (0.9% NaCl).

area of 866 mm^2 in Fig. 2(b)] with the 8 mm $\times$ 8 mm packaged ASIC-NI, yielding a 48% further reduction in the system board area. With the integration of the ASIC-NI [photomicrograph shown in Fig. 2(c)] and use of hybrid technology for mounting an unpackaged ASIC and other system components, we aim to have future designs toward a finalized system fit in the hermetic enclosure of an existing cochlear implant [Fig. 2(d)].

3) ASIC-NI Power Consumption: The ASIC-NI consumes 7.4 $\pm$ 0.2 mW (P_0) during quiescent conditions when all channels are set to 0 μA amplitude. A linear regression ($R^2 = 0.99$) of measured instantaneous power consumption during current output against current amplitude, showed an overall increase from P_0 of 1.2 mW due to ASIC-NI operation, and an additional 0.02 mW per μA of pulse output. With the typical parameters used for MVP stimulation, 94 pps on 3 channels with biphasic pulses of 150 μs/phase (giving a duty cycle of 8.5%), and 120 μA amplitude, the ASIC-NI power consumption is calculated to be 7.7 mW.

The ASIC-NI replaces circuitry in the MVP2 that consumed $\sim$ 20 mW (based on specifications of the off-the-shelf components used). For the entire MVP system, the inertial sensors remain the highest source of power consumption; however, improvements in MEMS technologies continue to achieve decreased power consumption for motion sensors. The optimized design of the ASIC-NI decreases the overall power consumption of the MVP2 system from 70 mW in the MVP2 [16] to 58 mW in the MVP2A. Despite the high power consumption of the inertial sensors used with the MVP2A, incorporation of the ASIC-NI enables production of a MVP with lower power consumption and, equivalently, longer device run time on a given battery's full charge.

4) Multipolar Stimulation: The ASIC-NI's multiple current sources enable it to perform stimulation paradigms more complex (and potentially more physiologically effective) than the symmetric biphasic pulses most neuroelectronic prostheses employ. For example, the ASIC-NI can deliver delayed-pseudomonophasic multipolar current pulses at 1 kHz (Fig. 6), in which excitatory current passed by a single cathodic electrode near the target neural tissue is returned in different proportions to each of three anodic electrodes, redirecting the current field away from nontarget neurons. In Fig. 6, each trace displays the output of one of four electrodes; the bottom trace provides the main, cathodic first, stimulation while the top three act as the return electrodes to steer current of different magnitudes to the respective electrodes sites.

IV. Physiological Test Methods and Results

A. Physiological Test Methods

After bench testing confirmed that the ASIC-NI met design specifications, performance of the MVP2A system was quantified during physiological studies of prosthetic stimulation in a vestibular-deficient rhesus monkey (F060738RhG; *Macaca mulatta*; 6–12 kg). The purpose of this experiment was to directly compare physiological responses achieved using the MVP2A system with those elicited by an existing and already well-characterized multi-channel vestibular prosthesis based on commercial off-the-shelf components, the MVP2 [16]. All animal experiments were performed in accordance with a protocol approved by the Johns Hopkins Animal Care and Use Committee, which is accredited by the Association for the Assessment and Accreditation of Laboratory Animal Care, and consistent with European Community Directive 86/609/EEC.

1) Surgical Overview: Surgical methods have been previously described in detail [16]. In brief, under general anesthesia (isoflurane, 1.5%–5%), the monkey was fit with a cylindrical plastic chamber secured to the cranium and aligned with the mean horizontal SCC axis. Two mutually orthogonal Teflon™ coated stainless steel wire coils were surgically affixed to the sclera of the right eye to permit precise measurement of 3-dimensional rotational position using the search coil technique

[31], [32]. The distal aspects of a MVP2 electrode array were implanted into the three ampullae of the left labyrinth via a transmastoid approach and run to a percutaneous connector embedded in dental acrylic within the protective plastic chamber [16]. The electrode array comprised 11 electrodes: three electrodes per ampulla (which were positioned as close as possible to the ampulla's neurosensory epithelium), a distal reference (placed in musculature outside the temporal bone) and a "near" reference inserted into the common crus of the labyrinth. Details on the electrode array can be found in [16]. Electrode impedance measured around the time of the experiment of the three stimulating electrodes was 5 kOhms – 6 kOhms (measured with a 20 kHz square wave delivered across electrode leads). After recovery from the surgery, natural vestibular sensory function in the implanted ear was ablated via unilateral intratympanic injection of gentamicin (26.7 mg/mL, buffered with bicarbonate to neutral pH, dwell time 30 minutes under general inhalational anesthesia). This regimen has been proven effective at reducing the function of vestibular hair cells to cause a near-total failure of vestibulo-ocular reflexes [33]–[35].

2) Stimulation Protocol: The monkey was placed in a primate chair enclosure, using the head chamber as a means for atraumatic head restraint during the experiment. The monkey was kept in complete darkness during the experiment to avoid visual cues that would otherwise suppress or enhance VOR responses. The monkey was free to move its body and limbs within the enclosure, but its head remained stationary throughout the experiment to ensure that VOR responses observed were solely due to prosthetic electrical stimuli, which were delivered by the prosthesis with timing and amplitude appropriate to engender vestibular nerve activity that would typically occur in a normal animal during head rotation. Because the head was kept stationary, the microcontroller was programmed to replace signals from the MVP's gyroscopes with sinusoidal pulse-frequency-modulating waveforms that occurred independent of actual head movement, encoding virtual sinusoidal head rotations of 50 degrees per second (dps) at 0.1, 0.2, 0.5, 1, 2, and 5 Hz rather than actual movements of the head.

Current amplitude for each SCC electrode was optimized to maximize eye movement response slow-phase velocity while minimizing misalignment of the 3-dimensional VOR (which would indicate current spread to non-target branches of the vestibular nerve) and ensuring the absence of facial twitching (which would signify spurious activation of motor neurons in the nearby facial nerve). These optimized amplitudes ranged from 100–200 μA, depending on the electrodes used. Both the MVP2A and the "gold standard" MVP2 delivered charge-balanced, cathodic-phase-first, 150 μs/phase biphasic pulses with a 120 μs interphase gap. Pulse rates were modulated over a range of 68-130 pulses/s (pps) using a sinusoidal modulating waveform passed through a sigmoidal operating curve designed to emulate the normal encoding of head velocity into afferent neuron firing rate that is characteristic of normal rhesus monkey vestibular afferent neurons [5], [16], [36]. Parameters describing the operating curve parameters using the scheme in [5] were: $\mathrm{C} = 2$, baseline pulse rate 94 pps, and maximum pulse rate 350 pps. The range of stimulus pulse rates used was approximately equivalent to those that the MVP2 would typically generate during a sinusoidal head rotation with $50^\circ/\mathrm{s}$ peak velocity.

At the outset of the experiment, baseline stimulation at 94 pps was applied asynchronously to each of the three SCCs while the monkey remained still in a well-lit room with a visually rich scene. At the onset of baseline, nystagmus was apparent with slow phase eye movements away from the prosthetically stimulated ear (and rapid nystagmus "quick phases" resetting the eyes back near the center of their range of travel). This is typical immediately after the sudden onset of a large asymmetry in aggregate afferent firing rates on vestibular nerves from the two ears. However, the animal being tested had experienced such transitions enough times during prior experiments to develop the ability to rapidly adapt (such context-specific adaptation is also seen in humans exposed repeatedly to rapid changes in vestibular or visual input [37], [38]), so within 20 min of exposure to the baseline prosthetic stimulus in room light, her slow phase nystagmus faded to less than $\sim 5^\circ/\mathrm{s}$, consistent with central vestibular nervous system neurons adapting to correct for the asymmetry (a process known as vestibular compensation [1]).

At this point, trials of stimulus pulse rate modulation began. Prior to modulating the pulse frequency for a given stimulus trial, eye position was confirmed to be within 10° of center via direct observation using an infrared camera. The camera was turned off when modulation began to ensure no visible light from the camera's LEDs interfered with VOR responses. At least ten cycles were completed for each stimulation parameter set, for each of the three SCC's. Pulse frequency was modulated for one electrode channel (and SCC) at a time; the other two were kept at baseline stimulus rates.

3) Eye Movement Recording and Analysis: Physiological responses to prosthetic stimulation were characterized through measurement of 3-dimensional (3D) VOR eye movements using a magnetic scleral eye coil system that has been described in detail in [31], [32], [39]. Briefly, three pairs of wire coils were attached rigidly around the monkey chair, energized with sinusoidal currents at mutually prime frequencies, and oriented to generate three mutually orthogonal magnetic fields aligned to the head's nasooccipital $(\mathrm{X}, +\mathrm{anterior})$, interaural $(\mathrm{Y}, +\mathrm{left})$ and superoinferior $(\mathrm{Z}, +\mathrm{superior})$ axes. Fields generated by these coils in turn induce currents in each scleral coil that can be demodulated to yield signals proportional to the angle between the scleral coil's axis and the axis of each pair of field coils. By using two approximately orthogonal coils affixed to one eye, one can obtain the eye's 3D rotational position (with respect to a starting reference) and angular velocity through 3D rotational kinematics analysis using well-established methods described in detail in [40]–[42]. Trials including blinks were removed prior to further analysis. Positive and negative half-cycle gains (i.e., slow phase eye velocity divided by virtual head velocity during the excitatory or inhibitory cycles, respectively) were computed for responses to stimuli delivered by either of two systems: the standard MVP2 or the new MVP2A system.

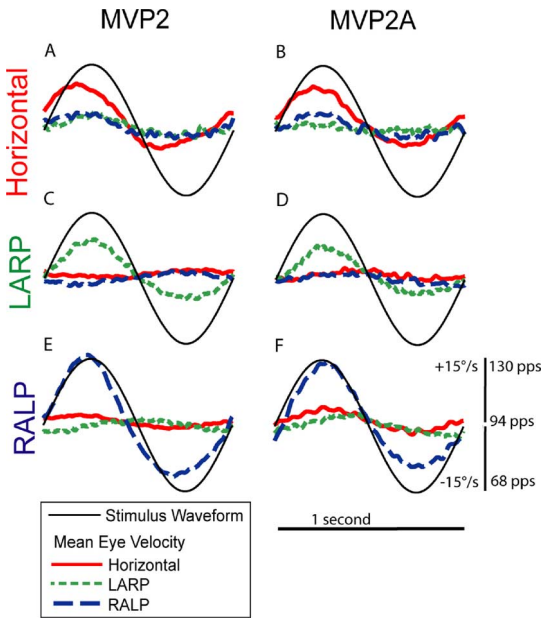

Fig. 7. Comparison of MVP2 and the ASIC-based MVP stimulator circuitry (MVP2A). Each panel shows cycle-averaged vestibulo-ocular reflex eye movement responses of a stationary, head-fixed monkey (F060738RhG) during 1 Hz sinusoidal modulation of stimulus pulse frequency between 68 and 130 pulses per second (pps) around a baseline of 94 pps (using stimulation parameters detailed in the text), which approximates neural activity that occurs during a 50°/s-peak 1 Hz rotation in normal monkeys [36]. (a, b) Stimulation targeting the horizontal semicircular canal elicits eye movements dominated by the horizontal component. (c, d) Stimulation targeting the left anterior (LA) canal elicits eye movements aligned with the left anterior and right posterior (LARP) SCCs. (e, f) Stimulation targeting the left posterior (LP) canal elicits eye movements aligned with the right anterior and left posterior (RALP) canals. Traces indicate cycle-averaged mean slow phase velocity after removal of saccades and smoothing with a nonlinear low pass filter. Standard deviations are $\leq \pm 2.4°/s$ for each trace at each point in time.

B. Physiological Results

A side-by-side comparison of cycle-averaged eye movement responses to 1 Hz stimulation delivered either by the MVP2 or the MVP2A is presented in Fig. 7. These eye movements were measured during 1 Hz sinusoidally pulse-frequency-modulated stimulation between 68 and 130 pps (comparable to the modulation of natural afferent firing rates during a 50°/s peak sinusoidal rotation in a normal monkey [36]). Delivered stimulation to electrodes implanted in the left horizontal SCC elicited predominantly eye movements in the horizontal plane [Fig. 7(a) and (b)], stimulation to the anterior SCC elicited eye movements aligned with the LARP plane [Fig. 7(c) and (d)], and stimulation to the posterior SCC elicited eye movements in the RALP plane [Fig. 7(e) and (f)]. The standard deviations for each cycle-averaged response are all $\leq \pm 2.4°/s$.

Fig. 8 shows averaged VOR gains at 0.1, 0.2, 0.5, 1, 2, and 5 Hz in each canal. Data are displayed separately for excitatory and inhibitory half-cycles. The MVP2 produced eye movement responses ranging from 1.9–16.7°/s (gains from 0.04–0.33) and the MVP2A evoked 2.0–14.2°/s (gains from 0.04–0.28). Standard deviations of all eye velocities were less than $\pm 4°/s$ at each data point. The ratio of the VOR gains elicited by the MVP2 to those by the MVP2A was used in a t-test of the hypothesis that the ratios come from a distribution with a mean equal to

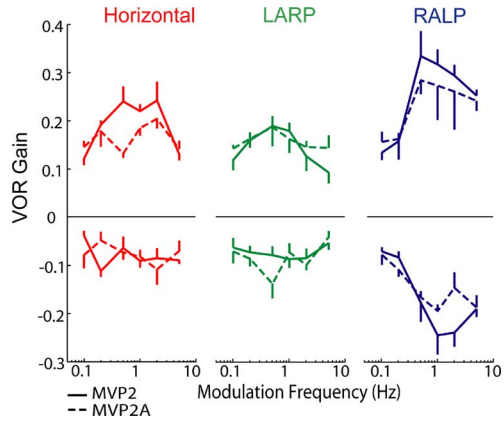

Fig. 8. Excitatory (top) and inhibitory (bottom) half-cycle gains for 3D vestibulo-ocular reflex eye movements of monkey F060738RhG evoked by a 0.1–5 Hz sinusoidal modulation of pulse frequency using the parameters described in Fig. 6. Mean responses ranged from 1.9 to 16.7°/s (gain of 0.04–0.33) with the 2nd generation multichannel vestibular prosthesis, MVP2 (solid) and from 2.0 to 14.2°/s (gain of 0.04–0.28) with the ASIC-based MVP system (MVP2A, dashed). Statistical analysis showed no detectable difference (t-test, $p = 0.34$) between the VOR gains produced by the MVP2 versus the MVP2A.

1 (where a ratio of 1 implies the same VOR gain for each device). The t-test indicated the null hypothesis that the mean of the ratios is equal to 1 cannot be rejected at the 5% significance level, suggesting no detectable difference between VOR gains produced by the MVP2 versus the MVP2A ($p = 0.34$, 95% CI $= [0.94, 1.17]$).

V. Discussion

The first generation MVP1 [Fig. 2(a)] was designed for initial proof of concept experiments in animals receiving chronic multichannel stimulation of vestibular afferents. While it proved effective for that purpose [5], its 100 mW power consumption and 31 mm × 31 mm × 11 mm size are both large compared to cochlear implants currently used in clinical practice [40]–[42]. The MVP2 [Fig. 2(b)] increased the number of possible electrode outputs and decreased size and power consumption to 29 mm × 29 mm × 5 mm with 70 mW, respectively, but to create a fully implantable device, further size and power reductions are needed [16].

Development of the ASIC-NI [Fig. 2(c)] is the first step in realizing our 3rd generation MVP (MVP3), which aims to be a fully implantable system that can fit into an existing cochlear implant hermetically sealed can [outlines pictured in Fig. 2(d)]. While the MVP2A system uses a commercially available microcontroller, further minimization could be accomplished by integrating the ASIC-NI with an on-chip microcontroller or a separate microcontroller mounted atop a hybrid substrate. This would avoid use of the 8 mm × 8 mm QFN package, shown in Fig. 2(c), which was chosen to simplify initial testing in the present design iteration. While ASIC-NI integration reduced the existing MVP system power consumption by 17%, off the shelf motion sensors are still the dominant factor in power consumption. Fortunately, market forces driven by the consumer products industry continue to drive the size and power consumption of inertial motion sensors downward. With the replacement of

existing MVP2 motion sensors (45 mW [16]) with a new Invensense MPU9250 sensor ($\sim$ 10 mW [43]) as well as the development of the ASIC (7.7 mW) replacing ($\sim$ 20 mW off the shelf components as determined by product specification documents), the overall power consumption can be reduced even further.

With 16 independent, accurate, and highly linear 9-bit DAC output channels that each produce up to 1.45 ± 0.06 mA across a load impedance of $\sim$ 10 kΩ (measured with a 20 kHz square wave delivered across electrode leads) and can be activated simultaneously to generate multipolar stimulus profiles that steer current toward target fibers while steering it away from non-target fibers, this ASIC-NI realization is well suited for prosthetic vestibular stimulation. The extended current range and additional electrodes provide opportunities to build upon the current prosthesis design to include multipolar stimulus configurations, stimulation of otoconial sensory organs (to encode linear accelerations and head orientation), stimulation of the semicircular canals in both ears, or to create a hybrid device that restores both cochlear and vestibular sensation (e.g., using eleven electrodes for the cochlear array, three electrodes for vestibular array, and two reference electrodes). Moreover, the ASIC-NI can also serve as a general purpose neuroelectronic interface for devices intended to stimulate other parts of the nervous system.

The ability to use a compliance voltage of up to 12V was realized with the high-voltage OnSemi C5F/N CMOS process, which employs HV transistors. While the high compliance voltage was specified to allow delivery of very brief stimulus pulses via the relatively small electrodes (such as those we have previously used in chinchillas [28], [44] and prior experiments with rhesus monkeys [45]), in the present study we typically observed robust responses to stimuli with pulse widths of 150 μs and current levels of 100–200 μA delivered across a load impedance of $\sim$ 10 kΩ (measured with a 20 kHz square wave delivered across electrode leads). A compliance voltage below 5 V could achieve these current levels and would have the advantage of allowing us to use a more generic CMOS process to fabricate the ASIC-NI and remove the need for a step-up convertor to generate a 12 V source. However, using a high compliance voltage offers some compensating advantages, because it allows delivery of sufficient charge during a shorter duration stimulus pulse. Stimulus pulses that are relatively brief and high current incur fewer timing clashes, require less charge per phase to excite vestibular afferents [44] and are more effective at stimulating cochlear afferents when incorporated into pseudo-monophasic, cathodic-first stimulus paradigms [46].

As is evident in Figs. 7 and 8, MVP2A stimulator and the MVP2 yielded very similar outcomes during *in vivo* experiments. This is not surprising, because bench tests demonstrated that both systems deliver the same stimulus current waveforms. Results for both stimulators also exhibit aspects that exemplify challenges that merit additional research to optimize electrode placement and stimulus protocols. Responses to stimulation of left posterior SCC afferents consistently produced larger magnitude eye responses in the corresponding RALP direction, compared to stimulation targeting the left anterior and horizontal SCCs. This larger response is due to the greater selectivity with which current can be delivered to the posterior SCC's ampullary nerve branch (which is relatively far from other vestibular nerve branches) compared to the anterior and horizontal SCCs' nerve branches (which are very close to each other, constraining the magnitude of current pulses that can be delivered without spurious activation of the other afferents).

Responses also exhibit a pronounced excitation-inhibition asymmetry, with responses to excitatory stimuli (representing head rotation toward the implanted ear) being larger than responses to inhibitory stimuli (representing head rotation away from the implanted ear). Excitation-inhibition asymmetry is a normal feature of many stages in the neural circuitry underlying the vestibulo-ocular reflex, most notably in vestibular afferent neurons' larger dynamic range for excitation (which can drive action potential rates from the $\sim$ 100 spike/s baseline to more than 400 spike/s) compared to inhibition (which can only down-modulate firing rates to zero). This inherent asymmetry is exacerbated during prosthetic stimulation because down-modulation of the rate of exogenously applied stimulus pulses cannot drive afferent spike rates below a floor set by nonzero spontaneous discharge rates [47]. Methods currently under study to reduce this asymmetry include bilateral implantation [48], [49], rehabilitation paradigms [50], [51], "safe DC" stimulation [52] and concurrent modulation of stimulus pulse amplitude and frequency [44], [45]. The ASIC-NI is especially well suited to enact the latter strategy, because its high compliance voltage allows delivery of brief, high current pulses.

The ASIC-NI presented in this paper provides a first step toward an MVP3 while maintaining compatibility with the existing MVP2 architecture. As ASIC-NI development continues, additional features can be integrated along with design changes that further reduce system size and power consumption. We envision an enhanced ASIC-NI that includes an integrated, on-chip microcontroller and an amplifier for neural response recording and measurement of electrode impedances *in vivo*. Addition of a telemetry unit, hermetic encapsulation, implantable battery and power management will be key components needed to complete a fully implantable system.

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Kristin N. Hageman received the B.S. degree in biomedical engineering (with a specialty in bioelectrical engineering) from Case Western Reserve University, Cleveland, OH, USA, in 2011.

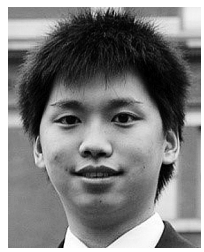
Currently, she is working toward the Ph.D. degree in biomedical engineering at Johns Hopkins University School of Medicine, Baltimore, MD, USA. Her research interests revolve around neural stimulation and medical device development. In the Vestibular NeuroEngineering Lab, she focuses on the circuit development of the next generation multichannel vestibular prosthesis.

Zaven K. Kalayjian (M'99) received the Ph.D. degree in electrical and computer engineering from Johns Hopkins University, Baltimore, MD, USA, in 1999.

He became a Postdoctoral Researcher at the Army Research Labs in the Sensors and Electron Devices Directorate, where he worked on VCSEL-based communications fabrics. He then went to work at Epygi Labs LLC, Armenia, as the Director of R&D, where he led two IC and fiber optics design groups. While in Armenia, he also taught computer architecture at the American University of Armenia, Yerevan, Armenia, as well as consulted for U.S.-based firms in the medical device field. After returning to the USA, he rejoined his colleagues at Johns Hopkins University to work on a vestibular prosthesis device. Also, he has been a Consultant at Booz Allen Hamilton and Principal Engineer at Applied Physical Sciences. Currently, he is a Senior Engineer at the Aerospace Corporation.

Francisco Tejada (M'00) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Johns Hopkins University, Baltimore, MD, USA, in 2000, 2001, and 2006, respectively.

His dissertation focused on developing optical transduction methods based in CMOS IC processes. In 2006, he founded Sensing Machines, Kingsville, MD, USA, which provides engineering design services for integrated circuit, printed circuit boards, and MEMS.



Bryce Chiang received the B.S. and M.S.E. degrees in biomedical engineering from Johns Hopkins University, Baltimore, MD, USA, in 2008 and 2009, respectively.

At Johns Hopkins, he worked on the development of the 2nd- and 3rd- multichannel vestibular prosthesis. Currently, he is working toward the M.D. degree at the Emory School of Medicine, Atlanta, GA . USA, and the Ph.D. degree in biomedical engineering at the Georgia Institute of Technology, Atlanta, GA, USA, where his work is focused on understanding the pharmacokinetics of suprachoroidal delivery using microneedles. His research interests include ocular drug delivery, neural engineering, medical device development, and translation of technology from bench to bedside.

Mehdi A. Rahman received the B.S. and M.S. degrees in biomedical engineering (with a concentration in instrumentation) from Johns Hopkins University, Baltimore, MD, USA, in 2009 and 2012, respectively.

In Summer 2009, he worked with a startup company in testing and designing embedded electronics for upper limb prosthetic application. Currently, he works for Labyrinth Devices, LLC, on enhancing the device design and user interface of the multichannel vestibular prosthesis.

Gene Y. Fridman received the M.S. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, and the Ph.D. degree in biomedical engineering (specializing in neural recording, stimulation, and micro-electro-mechanical systems), from the University of California, Los Angeles, Los Angeles, CA, USA, in 1995 and 2006, respectively.

His primary interest is in applied research toward implantable neural prosthetics. After 1995, he worked in industry for five years in R&D as a Software and Systems Engineer before deciding to engage in an academic career. He completed postdoctoral training at Johns Hopkins University, Baltimore, MD, USA, in 2010. He is an Assistant Professor of Otolaryngology–Head and Neck Surgery at the Johns Hopkins School of Medicine.

Chenkai Dai is an Assistant Professor in the Department of Otolaryngology–Head and Neck Surgery, John Hopkins School of Medicine, Baltimore, MD, USA.

His research focuses on development of Hopkins invented vestibular prosthesis, interaction/adaptation to chronic electrical stimulation, hearing outcomes after vestibular prosthesis electrode implantation, and development of novel rehabilitation paradigm for improving VOR compensation in patients with vestibular disorder.

Philippe O. Pouliquen (M'97) received the B.S.E. degree in biomedical engineering and the Ph.D. degree in electrical and computer engineering from Johns Hopkins University (JHU), Baltimore, MD, USA, in 1990 and 1997, respectively.

Currently, he is a Research Scientist in the Electrical and Computer Engineering Department at JHU. His research interests include low-power analog and digital ASICs, analog-to-digital and digital-to-analog computer, and CAD tools.

Julius Georgiou (M'98–SM'08) received the M.Eng degree in electrical and electronic engineering and the Ph.D. degree from Imperial College London, London, U.K., in 1998 and 2003, respectively.

Currently, he is an Assistant Professor at the University of Cyprus, Nicosia, Cyprus. He worked as Head of Micropower Design at Toumaz Technology, a startup company, for two years. In 2004, he joined Johns Hopkins University, Baltimore, MD, USA, as a Postdoctoral Fellow before becoming a faculty member at the University of Cyprus from 2005 to present. His research interests include low-power analog and digital ASICs, implantable biomedical devices, bioinspired electronic systems, brain-computer-interfaces, memristive devices, as well as inertial and optical sensors and related systems.

Dr Georgiou is a member of the IEEE Circuits and Systems Society and Vice-Chair of the BioCAS Technical Committee. Also, he is a member of the IEEE Circuits and Systems Society Analog Signal Processing Technical Committee. He served as the General Chair of the 2010 IEEE Biomedical Circuits and Systems Conference and is the Action Chair of the EU COST Action ICT-1401 on "Memristors-Devices, Models, Circuits, Systems and Applications – MemoCIS." He is an Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and the *Frontiers in Neuromorphic Engineering Journal*. He was the recipient of a Best Paper Award at the IEEE ISCAS 2011 International Symposium and at the IEEE BioDevices 2008 Conference.

Charles C. Della Santina received the Ph.D. degree in bioengineering from the University of California, Berkeley, Berkeley, CA, USA, and the M.D. degree from the University of California, San Francisco, San Francisco, CA, USA, in 1994 and 1997, respectively.

At UC Berkeley, his work focused on the development of micromachined silicon devices for chronic multi-unit interfacing to the auditory/vestibular nerve. Since 2002, when he completed his residency at the Johns Hopkins School of Medicine, Baltimore, MD, USA, he has been a Clinician-Scientist at Johns Hopkins, where he is Director of the Johns Hopkins Vestibular NeuroEngineering Lab and a Professor of Otolaryngology–Head and Neck Surgery and Biomedical Engineering. His research focuses on vestibular neurophysiology and development of a vestibular prosthesis for restoration of labyrinthine sensation. He holds a founding interest in Labyrinth Devices LLC.

Andreas G. Andreou (F'06) received the Ph.D. degree in electrical engineering and computer science from Johns Hopkins University (JHU), Baltimore, MD, USA, in 1986.

Currently, he is Professor of Electrical and Computer Engineering at JHU, Professor of Computer Science of the Whitaker Biomedical Engineering Institute, and cofounder of the JHU Center for Language and Speech Processing. His research interests include sensors, micropower electronics, heterogeneous microsystems, and information processing in biological systems.

Dr. Andreou is a distinguished lecturer of the IEEE Electron Devices Society.