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GND Plugs: A Superior Technology to Mitigate TSV-Induced Substrate Noise

Nauman H. Khan, *Member, IEEE,* Syed M. Alam, *Member, IEEE,* and Soha Hassoun, *Senior Member, IEEE*

***Abstract*— Through-silicon vias (TSVs) contribute to substrate noise in 3-D ICs, causing performance degradation of neighboring active devices and requiring keep-out zones. To mitigate TSV-induced substrate noise, we propose a new device, the ground (GND) plug, a TSV-like structure that connects to the ground and extends partially or completely through the substrate. We propose two types of GND plugs: a "front-side" plug, connecting to local interconnect of the same die, and a "back-side" plug, connecting to the GND from the substrate side of the die. We perform comprehensive analyses to evaluate the performance of GND plugs for two substrate types, a high-R bulk and a bulk with epitaxial layer. We compare the GND plug technique with existing noise mitigation techniques: a thicker dielectric liner, a guard ring, and a back-side ground plane. When compared with increased dielectric thickness, the front-side GND plug offers a relative 33% area reduction and allows a significantly reduced keep-out zone. The GND plug offers a more practical noise isolation approach than using a back-side ground plane. Our study demonstrates that the GND plug is a superior technology, effective in mitigating TSV-induced substrate noise by an order of magnitude when compared to the other techniques. The back-side GND plug does not compete with active devices for silicon area yet reduces substrate noise significantly.**

***Index Terms*— 3-D integrated circuits, integrated circuit noise, through silicon via.**

I. Introduction

3-D INTEGRATION offers opportunities to create unique high-performance systems. Dies from disparate technologies (analog, digital, mixed signals, sensors, and antenna) and from different technology nodes can be stacked to form a 3-D system-in-package (SiP) with higher bandwidth, low latency, low device power, and small form factor [1]–[3]. For the last decade, 3-D stacked-die integration has been primarily realized with wirebond technology. Driven by demands for higher vertical interconnect density and improved electrical performance, the industry is moving to through-silicon-via (TSV) based 3-D interconnect [4]. Signals traveling through TSVs however couple through the substrate to neighboring devices, causing performance degradation and potentially erroneous computations. Additionally, TSV noise increases leakage current, which increases static power consumption and can erroneously turn transistors from the "off" state to the "on" state [5]. A "keep-out" zone, specified through layout rules, is thus required to isolate devices from neighboring TSVs.

We propose, in this paper, a practical and effective element, a ground (GND) plug, to mitigate TSV-induced substrate noise. A GND plug is a TSV-like structure that extends partially or completely through the substrate and connects to circuit GND. Multiple GND plugs, fabricated around a signal TSV, provide effective grounding of the substrate and reduce the coupling impact between TSV and neighboring devices. A GND plug is different from a GND "substrate tie" that provides typical substrate or well connection to GND without substantial depth into the substrate. The major contributions of this paper are as follows.

1) A detailed study of GND plug size, placement, and connection to GND to understand noise suppression and area penalty tradeoffs for high-R bulk substrate and bulk with epitaxial layer.
2) A comparison of performance and area penalty of GND plugs with other noise mitigation techniques: thicker dielectric liner, back-side ground plane, and guard ring. A thicker dielectric liner provides shielding that results in reduced coupling between TSV and substrate. A back-side plane and a guard ring, electrically connected to circuit GND, ground the substrate.
3) Our analysis and evaluation framework use an extraction tool (Q3D Extractor) from Ansoft to extract lumped parasitics for our experimental design setups. Q3D Extractor is an industry-standard in extracting 3-D circuit parasitics.
4) More importantly, we show that the GND plug provides a superior advantage in reducing substrate noise and in minimizing the keep-out zone while utilizing small (or no) area.

The rest of this paper is organized as follows. We present an overview of TSV-induced noise and related work in Section II. We describe our evaluation framework used to perform lumped parasitic analysis in Section III. Using this framework, we study three noise mitigation techniques, thicker dielectric liner, back-side ground plane, and guard ring in Section IV. We evaluate different design variables for both types of GND plugs in Section V and compare their performance in terms of peak substrate noise and substrate area penalty in Section VI. We conclude our study in Section VII.

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N. H. Khan and S. Hassoun are with the Computer Science Department, Tufts University, Medford, MA 02155 USA (e-mail: nauman@cs.tufts.edu; soha@cs.tuft.edu).

S. M. Alam is with Everspin Technologies, Austin, TX 78750 USA (e-mail: salam@alum.mit.edu).

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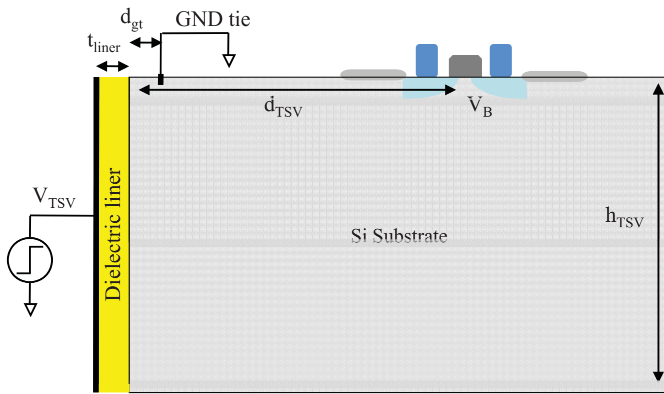

Fig. 1. Cross-sectional view illustrating TSV-to-device coupling.

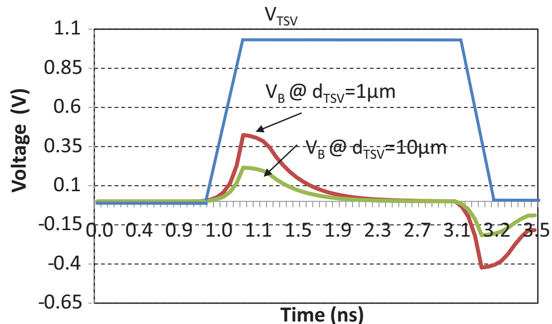

Fig. 2. Body voltage during TSV signal transition at different TSV distances, d_{TSV}, for $V_{TSV} = 1$ V square wave, $h_{TSV} = 20$ μm, $t_{liner} = 1$ μm, $d_{gt} = 0.5$ μm, signal transition time = 50 ps [6].

II. Overview of TSV-Induced Noise and Related Work

A TSV is a metallic (usually Cu) structure extending through the silicon substrate and isolated from it using dielectric and barrier materials. Fig. 1 shows a cross-sectional view of an Si substrate with a TSV and a MOSFET transistor. A signal transitioning through a TSV creates noise that can pass through the substrate and impact the performance of neighboring active devices and TSVs. Physical design considerations (shown in Fig. 1) that can be potentially exploited to mitigate TSV-induced substrate noise include: dielectric liner thickness (t_{liner}), TSV-to-device distance (d_{TSV}), and GND ties (conventional substrate/well ties, often referred to as substrate contacts). Fig. 2 shows variations in the device body voltage, V_B, at different distances from a TSV for a set of design parameters. These transitions are short-lived and occur only with a change in the signal passing through a TSV. For a 1-μm thick liner, the peak value of these transitions is significant (40% of VDD), despite including a GND tie at 0.5 μm from the TSV. To explore the impact of body voltage variations on device performance, we model a fan-out of 4 (FO4) inverter, in 32-nm technology node. We vary the peak body voltage while maintaining the shape of the waveform shown in Fig. 2. Fig. 3 shows the resulting variations in delay and dynamic power. It is evident from Fig. 2 and Fig. 3 that TSV-induced noise plays a significant role in determining device performance.

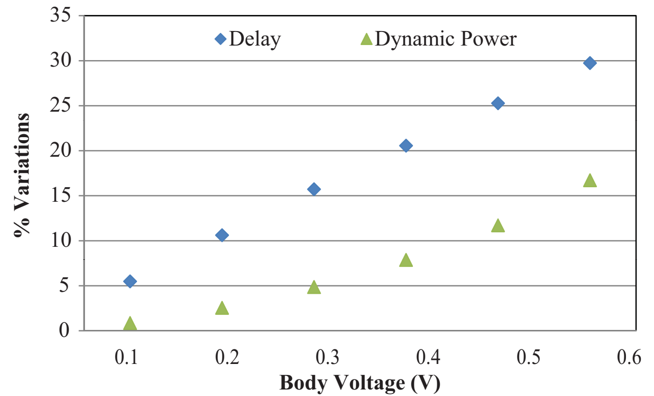

Fig. 3. Variations in performance and power of a fan-out-of-four CMOS inverter in 32-nm technology node due to body voltage noise.

Substrate noise is a well-studied problem in traditional 2-D IC design [7]. While substrate noise has not been a serious concern for digital circuits, analog circuits have always been a subject of higher scrutiny. Several noise isolation techniques, including split power planes, deep n-well process, and guard ring structure, have been employed in mixed-signal designs. For a 3-D IC design, the extent of TSV-induced substrate noise problem is directly related to the density of TSVs. Conventional noise mitigation techniques, such as isolated floorplanning of noise sensitive circuits with guard bands, are not feasible in 3-D designs with high TSV density as predicted by the ITRS roadmap [8].

Previous research efforts on TSV-induced substrate noise encompass noise modeling and noise-mitigation techniques. Banerjee *et al.* [9] developed compact analytical models to study electrical coupling from a TSV to the active regions. Dahaene *et al.* [10] created models based on physical parameters and material characteristics, and validated these models with numerical simulators. *Cho et al.* [11] utilized a unit-cell modeling approach where a TSV, substrate, and transistor layers are modeled as unit R, L, C elements. A 3-D mesh is formed for analysis and a wide range of frequencies is considered. A number of noise-mitigation techniques have been identified: thicker dielectric liner, back-side ground plane [6], guard ring structures [11], and co-axial TSVs [12]. Increasing the thickness of the dielectric liner is the simplest approach, and has already been shown to be insufficient in mitigating substrate noise [6]. Providing a back-side ground by placing a die on a grounded metal sheet is a common strategy to mitigate substrate noise in 2-D ICs. This strategy may not be practical for 3-D ICs for two reasons: 1) a metallic sheet between dies will introduce unnecessary inductive coupling, and 2) the design complexity will increase because TSVs must be isolated when passing through metallic sheets. Surrounding TSVs with guard rings is not effective because typical guard-ring depth is comparable to GND tie depth, which is too small to provide any significant isolation [11]. Lastly, using a co-axial TSV promises to mitigate noise [6]. However, manufacturing co-axial TSVs is more challenging and costly than comparable conventional TSVs due to the inherent structural complexity requiring additional manufacturing steps [13]. Desirable aspect ratios for smaller TSV footprints necessitate

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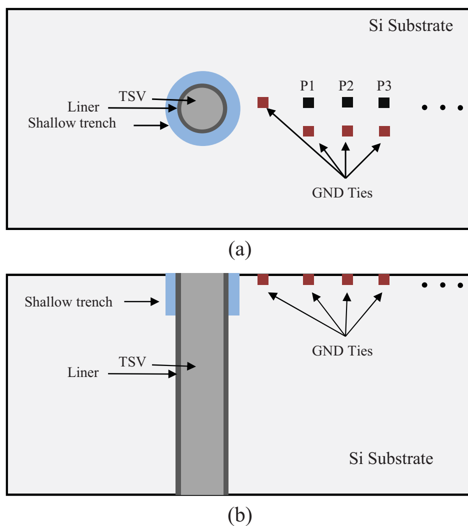

Fig. 4. TSV-induced noise analysis framework. The voltage at the observation points, e.g., P1, P2, and P3, represent body voltages of neighboring transistors while the GND ties are their neighboring conventional substrate ties. (a) Top view. (b) Side view.

novel fabrication methods [14]. We propose, in this paper, an alternative and more practical technique to reduce TSV-induced substrate noise by using GND plugs in the vicinity of TSVs. A GND plug is a TSV-like structure that is connected to circuit GND but unlike a TSV, the GND plug may not extend through the complete depth of the substrate. To quantify the effectiveness of the proposed technique and to investigate some of the critical physical design parameters, such as the placement and height of GND plugs, we first develop a lumped parasitic analysis framework.

III. Evaluation Framework

We use a 3-D evaluation framework composed of a Copper (Cu) TSV in Silicon (Si) substrate, ground ties, and voltage observation points. The top view and side view of this setup are shown in Fig. 4. Each component is defined below.

1) *Substrate:* We assume a high-R substrate, unless otherwise noted, with a resistivity of 10 Ω-cm and relative permittivity of 11.8. This type of substrate is used to fabricate low-cost, low performance devices like memory [15]. We assume a 50 × 50 μm substrate with the height of 20 μm. This cross section is sufficiently large when compared to the TSV and device sizes to enable capturing their interactions without worrying about complex boundary conditions. An outgoing zero-current was set at the edges of the substrate. The condition is in synergy with (a) multiple 50 × 50 μm modeled substrate neighboring each other from the die and (b) there is no interaction/interference between them.
2) *TSV:* We assume a cylindrical Cu TSV. Its height is the same as the substrate height (20 μm) and the diameter is fixed to 2 μm.
3) *Dielectric Liner:* We use an SiO_2-based liner that surrounds the TSV, with a resistivity 10^{16} Ω-cm and relative permittivity 3.9. The default thickness of the dielectric liner is assumed to be 0.1 μm, which is consistent with recent design studies [16].

TABLE I
Critical Parameters for Our TSV-Induced Noise Analysis Framework

Parameter	Value
Substrate height	20 μm
Substrate length	50 μm
Substrate width	50 μm
TSV height	20 μm
TSV diameter	2 μm
Liner thickness	0.1 μm
Shallow trench height	0.3 μm
Shallow trench width	0.9 μm
Resistivity of high-R substrate	10 Ω-cm
Dimension of observation point/GND tie	0.5 μm

4) *Shallow Trench:* Thermal stress is one of the most important factors shaping TSV technology. We assume an SiO_2-based shallow trench. Its thickness and depth (into the top surface of the substrate) are assumed to be 0.9 and 0.3 μm, respectively. These values are consistent with those in the ITRS roadmap [8].
5) *Observation Points:* We assume nine equally spaced observation points (P1, P2, ...) located 4 to 20 μm away from the center of the TSV. These observation points represent the body of the transistors. These points are modeled as small metallic cubes to enable extracting parasitics between TSV and devices at various distances from the TSV.
6) *GND Ties:* Placing GND ties throughout the circuit layout is the conventional approach to ground the substrate/wells, and to control the transistor body voltages; therefore, GND ties are considered in our setup. We assume a GND tie at a distance of 0.3 μm from the shallow trench edge. Also, we assume that there is at least one GND tie within a 1-μm distance of each observation point. This GND tie is not the proposed GND plug.

Table I shows the default values of parameters in our TSV-induced noise analysis framework, unless otherwise specified. To extract an equivalent SPICE circuit for our framework, we use a 3-D extraction tool (Q3D Extractor) from Ansoft. To perform the extraction, we use default extraction parameters. In particular, the solver residual specifying how close a field solution must satisfy the electro-magnetic field equation for the current mesh was set to zero. The maximum number of mesh refinement cycles was set to 20, while the minimum number was set to 2. The percent refinement per pass, which controls the adaptive refinement process, was set to the default value of 30%.

Fig. 5 shows a portion of the extracted circuit comprising a TSV, an observation point, a GND tie, and Si substrate. The RLC values of the extracted circuit depend upon the extraction frequency. In the Q3D Extractor Technical Notes [17] and shown in Fig. 6, three regions of operations are defined: dc, transient, and ac. In the dc region, resistance and inductance are nearly constant with frequency. In the

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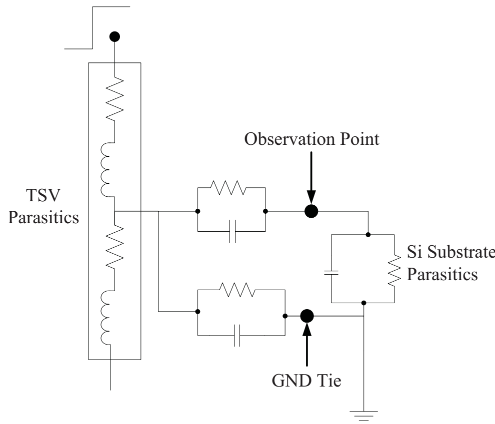

Fig. 5. Example extracted circuit comprising TSV parasitics, a single observation point, a GND tie, and Si substrate parasitics for coupling among the three elements.

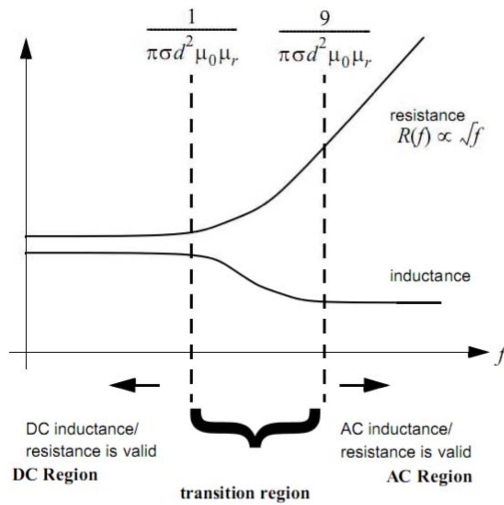

Fig. 6. Frequency regions of Q3D extractor [17].

ac region, inductance is nearly constant, but less than the dc counter-part due to skin effect reducing magnetic fields. Resistance in the ac region increases proportionally with the square root of frequency because of skin effect, which reduces the effective cross section of the current flow. The transition region spans about 1 decade of frequency where neither dc nor ac models are truly valid due to the skin depth being an appreciable fraction of the conductor depth. In Fig. 6, σ is the conductor's conductivity in S/m, μ_r is the conductor's relative permeability, μ_0 is the permeability of free space ($4\pi \times 10^{-7}$ H/m), and d is the conductor thickness. For our design configuration, the Cu TSV is the conductor with a diameter of 2 μm. The upper bound of dc region can be calculated to be 1.1 GHz. So, using an extraction frequency of 1 GHz is a valid assumption to extract the RLC circuit in the dc region. Hence, our results are valid for frequencies less than 1.1 GHz. We performed several extractions for frequencies up to 1.1 GHz, and indeed, the RLC values remain unchanged.

To perform transient analysis, a step input, with a rise time of 100 ps and peak voltage of 1 V, is applied at one of the TSV terminals. The other terminal is assumed to drive one

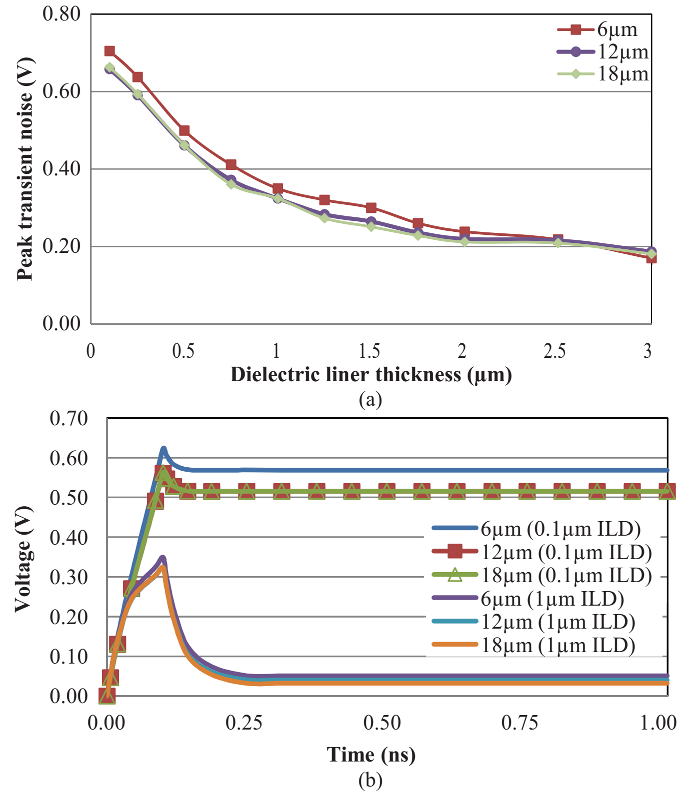

Fig. 7. Impact of increasing liner thickness. (a) Peak transient noise at different observation distances (6, 12, and 18 μm) from the TSV. (b) Waveforms for TSV noise for various liner thickness values.

or more MOSFET gate through metallic interconnect. This results in a capacitive load of a few femto Farads, and a very high resistive load to circuit GND due to gate leakage. We assume an open circuit as an approximation for this large impedance, and assume the other TSV terminal to be floating. After simulating the circuit using SPICE, peak noise at the observation points is reported.

IV. Noise Mitigation Techniques

A. Using Thicker Dielectric Liner

Thicker dielectric liner shields devices from TSV-induced noise at the cost of substrate area that can be otherwise used for devices. We vary liner thickness from 10nm to 3 μm in the default setup shown in Fig. 4 and extract an RLC circuit for each setup using Q3D Extractor. SPICE is used to observe peak transient noise at various observation points in the substrate. Fig. 7(a) plots peak transient noise for several liner thickness values at observation distances 6, 12, and 18 μm from the TSV. Fig. 7(b) shows the noise waveforms for two sample configurations with the liner thickness of 0.1 and 1 μm. We conclude the following.

1) Peak transient noise ranges from 0.18 to 0.7 V, across various distances from the TSV, for all examined values of liner thickness. This indicates that standard GND substrate ties are inadequate for creating a reference GND substrate in the presence of TSV-to-substrate coupling. Hence, using GND substrate ties alone is not effective in mitigating TSV-induced noise.

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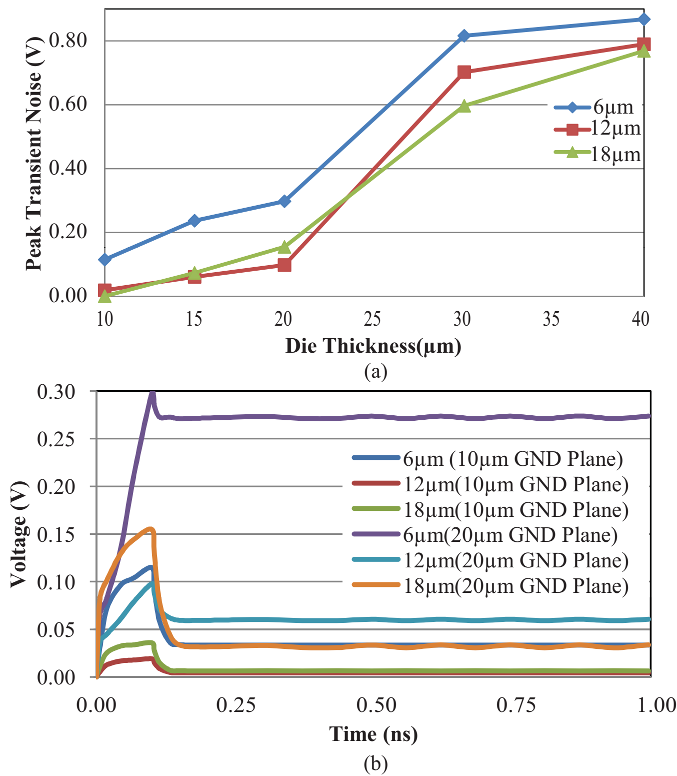

Fig. 8. Impact of back-side ground plane. (a) Peak transient noise at different observation distances (6, 12, and 18 μm) for different die thickness (distance from device to back-side ground) values. (b) Waveforms for TSV noise at various distances from TSV center for back-side ground planes at 10 and 20 μm.

2) Peak substrate noise decreases with increasing liner thickness. This trend is not uniform and can be divided into three segment. The impact of increasing liner thickness is maximum for liner thickness between 0.1 and 1 μm, reduces for liner thickness between 1 and 2 μm, and saturates after 2 μm.
3) Peak substrate noise is ≈18% of VDD for liner thickness of 3 μm. This huge 6× area penalty, for 2-μm diameter TSV, will create large interconnect blockages and will reduce the area available for active devices.

B. Using a Back-Side Ground Plane

During assembly and packaging stages, a 2-D die is placed on a grounded metal layer. The same idea can be extended to 3-D ICs where the substrate has a back-side grounded metal, in preferable plate or grid format, creating a strong GND reference for substrate. To model this technique, we add a Cu sheet in the default setup shown in Fig. 4. Sheet cross section is the same as substrate cross section and sheet thickness is assumed to be 2 μm. One side of the sheet connects to the substrate and the other side connects to GND. Substrate thickness, the distance between devices layer and the back-side ground, is the only variable of concern for substrate noise analysis. We vary the substrate thickness between 10 to 40 μm and extract the RLC circuit for each setup. We use SPICE to observe peak transient noise at the observation points. The results of this paper are shown in Fig. 8(a). The effectiveness of the back-side ground plane is a function of substrate thickness. The noise impact is minimal for thicker die. The back-side ground technique is, therefore, effective in technology generations where substrate heights can be aggressively reduced by substrate thinning. Fig. 8(b) shows the noise waveforms for two sample configurations with the back-side ground planes at 10 and 20 μm.

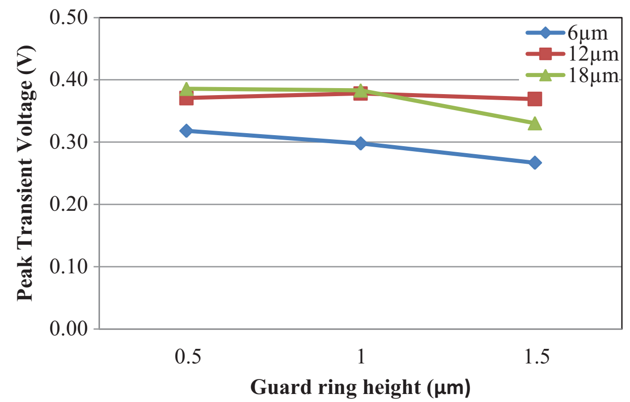

Fig. 9. Impact of guard ring height on peak transient noise at different observation distances (6, 12, and 18 μm). The guard ring thickness is fixed to 1 μm.

C. Using a Guard Ring

We extend the guard ring technique often used for noise isolation in 2-D circuits to use with 3-D circuits. We use the default design setup and add a guard ring at 3 μm from the center of the TSV. We vary guard ring depth into the substrate and observe its impact on TSV noise. The peak substrate noise at 6, 12, and 18 μm from the center of TSV is plotted in Fig. 9. We conclude the following.

1) Although increasing the guard ring height results in smaller TSV-induced substrate noise, guard ring is not able to localize the TSV-induced noise. The value of peak noise is larger at observation points away from TSV. The main reason for this behavior is that TSVs pass through the whole substrate and shielding only the top part of the substrate does not reduce the noise injected from the lower part of the TSV.
2) Using a guard ring of height 1.5 μm and width 1.5 μm results in an area penalty of 6.5× the TSV area whereas peak substrate noise is still greater than 30% of the input voltage.

V. GND Plug: A Superior Technology

Our analysis shows that shielding a TSV (thicker liner) and grounding limited to the top (guard ring) or bottom side (back-side ground plane) of the substrate are not sufficient to mitigate TSV-induced substrate noise. A better grounding solution would shield the TSV's entirety from neighboring devices. We propose a structure, the "GND Plug," a metallic structure that runs through the substrate in parallel to a TSV. While TSVs used for power delivery (power and GND TSVs) and for signal distribution

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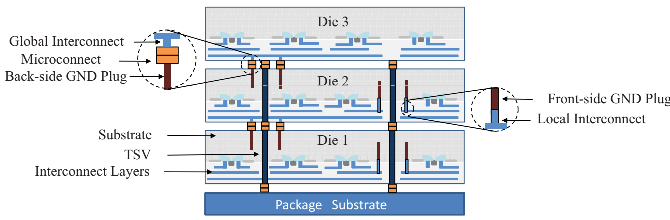

Fig. 10. Illustrative 3-D IC assuming face-to-back metallic bonding with microconnects. A "front-side GND plug" can be connected to a GND net in the same die. A "back-side GND plug" can be connected to a GND net in the neighboring die.

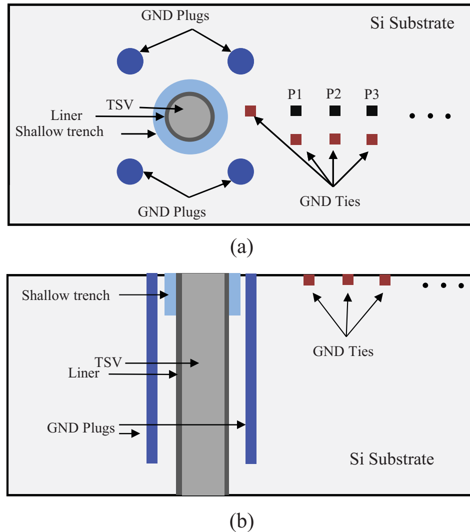

Fig. 11. TSV-induced noise analysis framework with GND plugs. (a) Top view. (b) Side view.

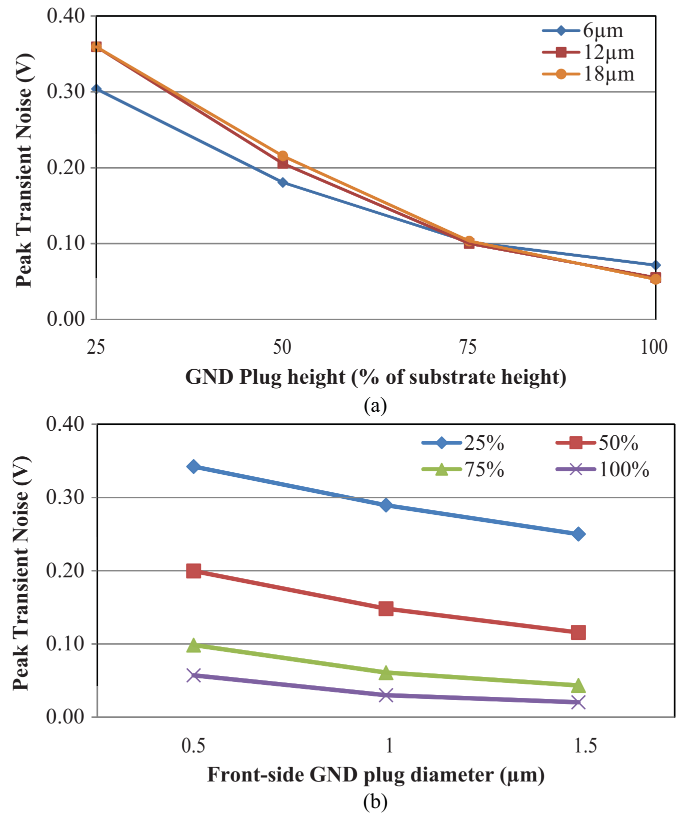

Fig. 12. Performance of front-side GND plugs. (a) Peak transient noise at observation distances (6, 12, and 18 μm) for different values of GND plug height (GND plug diameter = 0.5 μm). (b) Peak substrate noise at an observation distance of 10 μm for various combinations of GND plug height (percentage of substrate height) and GND plug diameter.

(signal TSV) connect circuitry of adjacent dies, the GND plug connects substrate to the circuit GND. A conventional TSV passes through the whole substrate and is connected on both ends (metal layers and/or microbumps). A GND plug, however, is local to a die and is connected only on one side to a metal layer or a microbump. A conventional TSV needs to have lower resistance and shielded from the substrate, while a GND plug does not have a strict requirement for the resistance and should not be shielded from the substrate.

We propose two types: a "front-side" and a "back-side" GND plug, and illustrate them in Fig. 10. A front-side GND plug is connected to the local interconnect (lower metal layers e.g., metal1, metal2) of the same die. A front-side GND plug occupies substrate area and reduces the available silicon area that can be used for active devices. A back-side GND plug is connected to the circuit ground from the back-side of substrate through microconnects and global interconnect (upper metal layers like metal7 and higher). Microconnects are small circuit elements, having a pitch of 20–60 μm, used to create vertical connection between the dies. Because the back-side GND plug extends only partially through the silicon, the silicon area devoted to active devices is not impacted.

GND plugs can be fabricated using any TSV fabrication technique using a variety of fill-material, including Copper (Cu), Tungsten (W), and Polysilicon (Poly). Although Cu is a better conductor, W or Poly is a better fill material for two reasons. First, a smaller coefficient of thermal expansion (CTE) mismatch of W/Poly and Silicon (Si), compared to Cu and Si, will result in less thermal stress in devices. Second, W/Poly does not require any diffusion barrier, such as Cu and will provide a direct connection between substrate and circuit ground resulting in better device shielding. W-filled TSVs have been demonstrated for the fabrication of 3-D LSI chips [18].

Fig. 11 shows our design setup with added GND plugs. We first evaluate the use of four GND plugs fabricated at 3 μm from the center of TSV. Noise isolation is improved by 2.46$\times$ when compared to using only two GND plugs. Therefore, we use four plugs for the rest of the analysis. Next, we explore the impact of two critical parameters: plug depth and plug diameter. RLC circuits for each setting are extracted using Q3D Extractor. Fig. 12 shows the SPICE simulation results plotting peak transient noise for different configurations of front-side GND plugs. We make the following observations.

1) A GND plug is effective in reducing peak noise. A deeper GND plug is more effective than a shallower one. Four GND plugs fabricated at 3 μm from the center of the TSV can reduce the peak substrate noise to 9% of the input voltage.
2) Fig. 12(b) shows the peak transient noise at a distance of 10 μm from the TSV for a variety of plug diameter and

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TABLE II
COMPARISON OF PEAK TRANSIENT NOISE AND AREA BLOCKAGE FOR TSV-INDUCED NOISE MITIGATION TECHNIQUES IN HIGH-R SUBSTRATE (RELATIVE TO THE BASELINE: TSV HEIGHT = 20 μm, LINER THICKNESS = 0.1 μm)

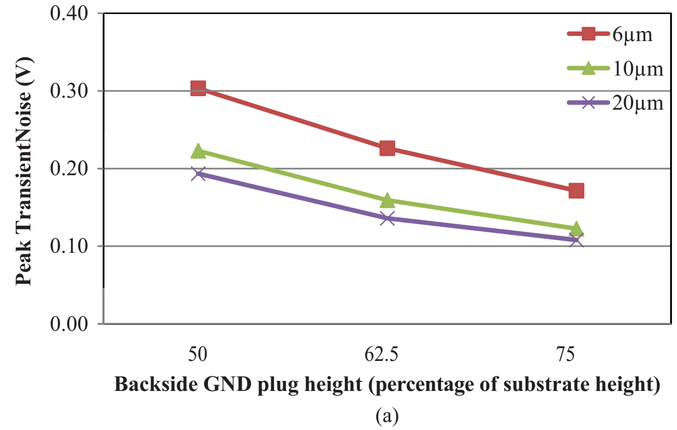
Technology	Peak Transient Noise (V)			Keep Out Area (Relative)
	6 μm	12 μm	18 μm	
Thicker liner (liner thickness = 1.5 μm)	0.426	0.402	0.379	2.890
Back-side ground plane	0.423	0.149	0.234	1.000
Guard ring (depth = 2 μm, width = 2 μm)	0.241	0.464	0.510	7.958
Front-side GND plug (diameter = 0.5 μm, height = 20 μm)	0.102	0.084	0.080	1.950
Back-side GND plug (diameter = 2 μm, height = 15 μm)	0.141	0.071	0.060	1.000

height. These results show that the impact of increasing height is more significant than increasing diameter. For a 3× increase in plug diameter, from 0.5 to 1.5 μm, noise reduction is only 10% whereas the same increase in plug height reduces noise by 25%.

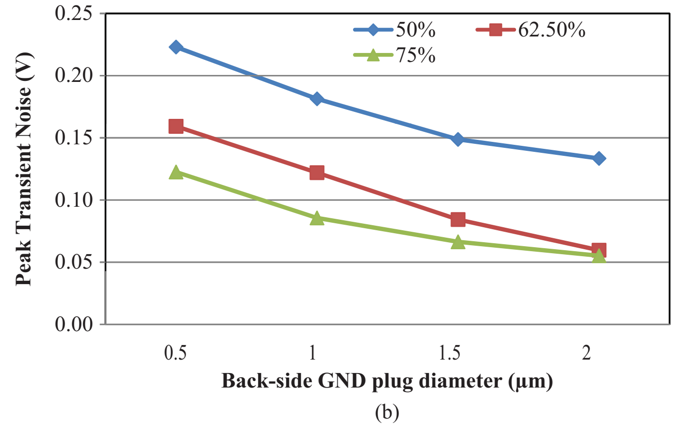
We repeat our analysis for the back-side GND plug, and show the results in Fig. 13. We make the following observations.

1) Back-side GND plugs are effective in reducing the substrate noise. Increasing the GND plug height or thickness reduces substrate noise. To meet a 10% noise budget, back-side GND plugs of 2-μm diameter and a height of 15 μm are required.
2) In contrast to front-side GND plugs, the back-side plugs are more capable of localizing the noise. If we consider Fig. 12(a) (front-side GND plug height 50%) and Fig. 13(a) (back-side GND plug height 50%), we can observe that only the back-side GND plug is capable of decreasing noise with increasing distance from the TSV. TSVs pass through the whole substrate. The upper part of the substrate is shielded by devices and grounded by ground ties. The lower part of the TSV is more responsible for noise injection into devices farther away from the TSV. So, for TSVs, grounding the lower part of substrate is equally important as grounding the top part. Devices further away from the TSV are more effectively shielded by the back-side GND plug resulting in better localization of noise as compared to front-side GND plugs.

The GND plug's diameter and depth are related due to aspect ratio limitations of deep trench formation and filling in the Si substrate. The results in Fig. 12 and Fig. 13 suggest the need for large-in-diameter yet deep GND plugs. Fabrication of W-filled TSVs with an aspect ratio of 50:1 and a diameter of 1 μm has been proposed [19], which suggests that the GND plug with a diameter of 0.5 μm and an aspect ratio of 40:1 is achievable. Kikuchi *et al.,* demonstrated W-filled TSV formation using deep-Si-trench etching and Tungsten chemical vapor deposition (CVD) where TSV diameter is maintained till 70% of substrate height for an aspect ratio of approximately 18:1 [18]. Interestingly, the proposed GND plug scheme does not require sidewall isolation nor high uniformity of plug diameter as a function of depth. A higher aspect ratio cone-shaped plug is thus possible, and warrants further investigation.



(a)



(b)

Fig. 13. Performance of back-side GND plugs. (a) Peak transient noise at observation distances (6, 12, and 18 μm) for different values of GND plug height (GND plug diameter = 0.5 μm). (b) Peak substrate noise at an observation distance of 10 μm for various combinations of GND plug height (percentage of substrate height) and GND plug diameter.

VI. GND PLUG COMPARISON WITH EXISTING NOISE MITIGATION TECHNIQUES

In addition to peak noise, area penalty is an important metric to evaluate the effectiveness of any noise mitigation technique. Assuming a baseline TSV setup, we evaluate peak noise and area penalty for each of the approaches. We use two substrate types: bulk (high-R) substrate and bulk with epitaxial layer (EPI substrate).

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TABLE III
COMPARISON OF PEAK TRANSIENT NOISE AND AREA BLOCKAGE FOR TSV-INDUCED NOISE MITIGATION TECHNIQUES FOR EPI SUBSTRATE (RELATIVE TO THE BASELINE: TSV HEIGHT = 20 μm, LINER THICKNESS = 0.1 μm)

Technology	Peak Transient Noise (V)		
	6 μm	12 μm	18 μm
Thicker liner (liner thickness = 1.5 μm)	0.345	0.346	0.351
Back-side ground plane	0.021	0.008	0.004
Guard ring (depth = 2 μm, width = 2 μm)	0.256	0.353	0.365
Front-side GND plug (diameter = 0.5 μm, height = 20 μm)	0.007	0.001	0.001
Back-side GND plug (diameter = 2 μm, height = 15 μm)	0.085	0.083	0.1

A. Bulk (High-R) Substrate

We assume a single layer of high-R substrate with 10 Ω-cm resistivity and a relative permittivity of 11.8. We utilize the default design parameters described in Table I and explore the relative merits of each technique. Table II reports peak transient noise and substrate area blockages for different noise mitigation techniques normalized to the baseline TSV case where no noise isolation technique is applied. The peak noise is reported at 6, 12, and 18 μm away from the TSV center. These results show that the front-side GND plug performs better than all the other techniques and reduces the peak noise by 90% at distance 6 μm from the TSV center. Moreover, the area penalty is less than the area penalty for thicker liner and guard ring. The back-side GND plug, on the other hand, does not require any area penalty and is capable of reducing noise by 86% at 6 μm from the TSV center.

B. EPI Substrate

EPI substrate consists of a heavily doped bulk substrate topped with a lightly doped epitaxial layer. We assume that the epitaxial layer spans the top 4 μm of the substrate and has a resistivity of 10 Ω-cm while the rest of the bulk substrate has a resistivity of 10 mΩ-cm. This type of configuration is mostly used to fabricate high performance chips, such as processors [15]. We utilize the default design parameters described in Table I and explore the relative merits of each technique. Peak transient noise at 6, 12, and 18 μm away from the TSV center is presented in Table III for different noise mitigation techniques. The area penalty for each of the techniques is same as the ones presented in Table II.

The results show that both types of GND plugs perform better than any other technique. Front- and back-side GND plugs can reduce the peak noise by 99 and 98% at 6 μm from the TSV center, respectively. More interestingly, in EPI substrate, the bottom 16 μm is low-R with $10^3\times$ smaller resistivity than the top 4 μm of the substrate. A single front-side GND plug of depth larger than 4 μm, or a single back-side GND plug of any height was sufficient to effectively GND the substrate. Since the resistivity of the bottom part of the substrate is very small, any contact to the circuit GND makes it act as a back-side GND plane with a substrate height of 4 μm.

VII. CONCLUSION

We proposed a novel noise mitigation technique, the GND plug, and compared its effectiveness against three other noise mitigation techniques: thicker dielectric liner, back-side ground plane, and guard ring for different substrate types: bulk and EPI. We assumed practical design parameters and utilized a 3-D solver to extract the equivalent SPICE netlist. Analysis of a 1.5-μm thick dielectric liner showed peak substrate noise of 30% of VDD, thus necessitating further increase in thickness or a significant increase in the keep-out zone. Furthermore, the resulting area penalty, 3× the size of a 2 μm diameter TSV, creates routing blockages and reduces the area available for active devices. While a back-side ground plane or mesh is effective with thinned dies, placing such a metal sheet or mesh between dies in 3-D ICs may not be practical. Guard rings require significant substrate area but provide insufficient substrate grounding. We showed that a front-side GND plug with an aspect ratio of 40:1 is effective in reducing noise by an order of magnitude with a smaller area penalty than a thick liner. The back-side GND plug does not incur any substrate area penalty and still results in significant noise reduction. The proposed GND plug technique thus offers a practical and promising solution to the difficult problem of providing device shielding against TSV-induced substrate noise. Our future work includes analyzing TSV-induced noise in the context of a noise-sensitive analog circuit, where multiple (signal and GND) TSVs and multiple GND plugs are utilized.

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Nauman H. Khan (M'07) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Engineering and Technology (UET), Lahore, Pakistan, in 2002 and 2006, respectively, and the Ph.D. degree in computer science from Tufts University, Medford, MA, USA, in 2011.

He is currently a CAD Engineer with Intel Corporation, Hillsboro, OR, USA. He was with the Electrical Engineering Department, UET, Lahore, and with Techlogix Inc., Lahore. His current research interests include computer-aided design (CAD) for integrated circuits and power delivery network (PDN) design and analysis for 2-D and 3-D integrated circuits.

Syed M. Alam (M'04) received the B.S. degree in electrical engineering from the University of Texas at Austin, Austin, in 1999, and the M.S. and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, in 2001 and 2004, respectively.

He is currently a Senior Member of Technical Staff with Everspin Technologies, Austin, a start-up from Freescale Semiconductor, where he is involved in research and development of various design aspects of standalone and embedded magnetic RAM. His current research interests include emerging memory design and test, 3-D integration technology, and nanomagnetic logic. He has authored or co-authored over 50 papers in refereed journals and conferences, and holds 26 patents issued or pending.

Dr. Alam was on the Technical Program Committee of DAC, ISQED, ICCAD, and DATE. He was on the Computer Architecture Panel of National Science Foundation. He is a member of the Sigma Xi Scientific Research Society. He has presented several invited talks including tutorials at ISQED, ICCAD, and GLSVLSI.

Soha Hassoun (SM'07) received the B.S.E.E. degree from South Dakota State University, Brookings, SD, USA, the Master's degree from the Massachusetts Institute of Technology, Cambridge, MA, USA, and the Ph.D. degree from the Department of Computer Science and Engineering, University of Washington, Seattle, WA, USA, in 1986, 1988, and 1997, respectively.

She is currently an Associate Professor with Tufts University, Medford, MA, where she is with the Department of Computer Science and the Department of Electrical and Computer Engineering. She was a Chip Designer with the Microprocessor Design Group, Digital Equipment Corporation, Hudson, MA. Her current research interests include developing algorithmic solutions to facilitate designing integrated circuits, and understanding the impact of new technologies such as double-gate devices, carbon nanotubes, and 3-D integration on design. Her other research includes computational methods for systems biology and metabolic engineering, including pathway analysis, modularity, pathway synthesis, and predictive modeling of biochemical networks.

Dr. Hassoun was a recipient of the NSF CAREER Award, and several awards from ACM/SIGDA for her service, including the Distinguished Service Award in 2000 and 2007, and the 2002 Technical Leadership Award. She was on the technical and executive committees of several conferences and workshops, including DAC, ICCAD, IWLS, TAU, and IWBDA. She was the ICCAD Technical Program Chair in 2005, the DAC Technical Program Co-Chair in 2011 and 2012, and the DAC Vice Chair in 2013, and she will be the DAC Chair in 2014. She was an Associate Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN and of the IEEE Design and Test magazine. She was on the Defense Science Study Group, affiliated with the Institute for Defense Analyses. She was on the IEEE's Council on Design Automation, and was the Director of Educational Activities for ACM's Special Interest Group on Design Automation for several years. She is a Fellow of Tau Beta Pi, ACM, and Eta Kappa Nu.