Noise Management in Highly Heterogeneous SoC Based Integrated Circuits

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***Abstract*—Noise coupling is one of the most fundamental issues in the design of highly heterogeneous, robust integrated systems. A two-step noise management methodology is proposed in this paper. In the first step, a methodology is described to efficiently analyze noise coupling in large scale circuits while maintaining sufficient accuracy. The second step consists of a methodology to significantly mitigate switching noise. The first step helps determining the required signal isolation and the efficacy of the noise reduction technique proposed in the second step. The two primary noise coupling paths in hybrid systems utilizing three dimensional (3-D) integration technology are also identified.**

I. INTRODUCTION

The ever increasing demand to integrate a higher number of devices by utilizing design paradigms such as system-on-chip (SoC) and system-in-package (SiP) has fundamentally changed the classical understanding of the integrated circuit (IC) design process. Existing tradeoffs among speed, power, and area have become significantly more complex since other design constraints such as noise, manufacturability, and reliability have also gained importance.

The evolution of integrated systems in terms of heterogeneity is illustrated in Fig. 1. In the first phase, a typical SoC is shown where heterogeneous computing is achieved. A processor coexists with a more specialized hardware, referred to as an accelerator, to achieve a specific functionality. This first phase of heterogeneity is limited by the computing methodology since the IC consists of primarily digital blocks with only CMOS technology.

In the second phase, as illustrated in Fig. 1(b), the IC consists of not only digital blocks, but also analog/RF functionalities integrated on the common substrate as in a monolithic transceiver. Analog/RF blocks, typically referred to as the victim circuit, are highly sensitive to switching noise generated by the aggressor digital blocks. In fact, in such mixed-signal systems, switching noise that couples to analog/RF circuits is typically several orders of magnitude greater than the device noise generated within the victim circuit [1].

In the third phase of heterogeneity, the IC consists of not only different functionalities such as analog/RF and digital, but also different technologies integrated within the same package utilizing SiP technology. Often, it is desirable to customize the technology based on the functionality of the circuit. For example, in a conventional transceiver circuitry, digital CMOS technology is preferred for data processing units due to higher noise margins and enhanced reconfigurability whereas gallium arsenide based devices are preferred for the front-end blocks such as power amplifier, mixer, voltage controlled oscillator, and low noise amplifier. Note that the heterogeneity is expected to radically increase with 3-D integration technology where electrical, optical, mechanical, and biochemical planes can be combined within a monolithic stack.

In these highly heterogeneous systems, one of the primary challenges is noise and interference management among diverse circuits with possibly different process technologies. The noise generated by the aggressor blocks, *i.e.*, switching noise, significantly affects the operation and performance of the sensitive circuits. The common substrate forms a conductive medium, permitting the switching noise to propagate throughout the die. A noise management methodology is proposed in this paper that consists of two phases: (1) efficient noise coupling analysis, and (2) noise mitigation. This methodology is further described in Section II. Challenges related to noise coupling in 3-D integrated systems are discussed in Section III. Finally, the paper is concluded in Section IV.

II. MANAGING NOISE COUPLING IN SOC BASED SYSTEMS

Noise management in a heterogeneous IC typically consists of two phases: (1) noise analysis and (2) noise mitigation. As depicted in Fig. 2, both noise analysis and noise mitigation are critical to obtain a robust system. An efficient noise analysis methodology is required to evaluate the dominant noise coupling paths and whether the system requires additional signal isolation. It is also helpful to determine the efficacy of various noise isolation strategies, permitting to choose a methodology that reduces the noise to a reasonable level while minimizing the cost in area and power dissipation. The lack of an efficient noise analysis methodology often produces a highly conservative circuit with unnecessarily large area and possibly higher power dissipation. Computationally efficient analysis of noise coupling is a challenging task in large scale circuits since multiple networks should be simultaneously considered. A methodology is described in Section II-A to efficiently analyze substrate coupling noise. In Section II-B, a noise mitigation technique is proposed to significantly reduce switching noise in heterogeneous circuits.

A. Efficient Verification of Noise Performance

Typically, extraction of the monolithic substrate is the bottleneck of noise coupling analysis since substrate should be treated as a 3-D entity that is common to each device within the system. Conventional extraction and analysis of a substrate network utilizes boundary element method (BEM)

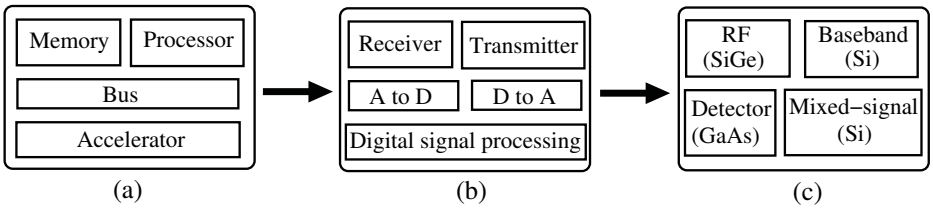

Fig. 1. **Evolution of heterogeneity in integrated systems: (a) SoC with heterogeneous computing, (b) Monolithic transceiver with heterogeneous computing and circuits, (c) System-in-package with heterogeneous computing, circuits, and devices.**

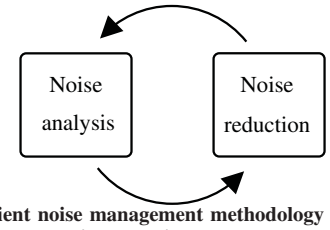

Fig. 2. **An efficient noise management methodology requires both noise analysis and noise reduction techniques.**

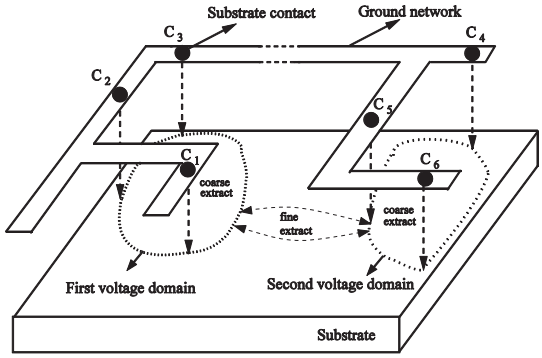

Fig. 3. **Identifying voltage domains on the substrate. C_1, C_2, and C_3 produce the first domain assuming $V_{C1} \approx V_{C2} \approx V_{C3}$. Similarly, C_4, C_5, and C_6 produce the second domain assuming $V_{C4} \approx V_{C5} \approx V_{C6}$.**

or finite difference method (FDM) which are not practical for large scale heterogeneous systems due to significantly higher computational complexity [2]. A methodology is described based on extracting only those regions of the substrate where there is significant current flow. The interaction between the ground and substrate networks is exploited to significantly reduce the computational complexity of the substrate extraction process. Specifically, small spatial voltage differences along the ground network are utilized to determine *voltage domains* on the substrate. Note these voltage domains on the substrate have approximately the same voltage. As illustrated in Fig. 3, these regions of the substrate are short-circuited by the ground network and therefore no major current flow exists in these domains. Since these regions are short-circuited, a coarse extraction is sufficient for these regions. This coarse extraction is achieved by reducing the number of substrate ports to only one. Note that a fine extraction is performed for those regions where there is significant current flow. An algorithm is proposed to identify these voltage domains. The proposed heterogeneous extraction of the substrate significantly reduces the computational complexity while maintaining a reasonable accuracy.

To evaluate the error in the estimated noise voltage and the

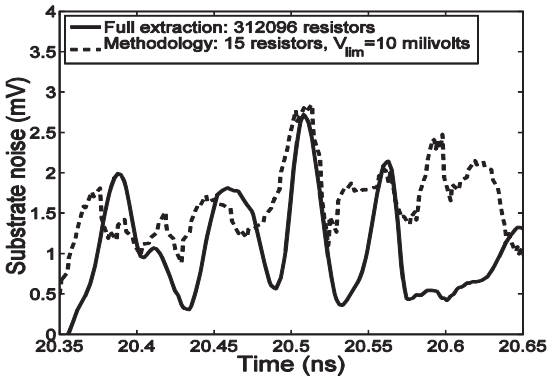

Fig. 4. **Comparison of the transient substrate noise at the victim node by simulating the fully extracted circuit and application of the methodology.**

improvement in computational complexity, the methodology is compared with a full extraction of the substrate achieved by Substrate-Noise-Analysis tool by Cadence [3]. An aggressor digital core located close to a sensitive block in an industrial transceiver circuit with a bulk type substrate is used for the analysis. Full extraction of the substrate using Cadence tool produces 312,096 resistors and requires approximately six hours to complete. Alternatively, the proposed heterogeneous extraction methodology reduces the number of substrate resistances to 15 under the same computation environment, achieving more than four orders of magnitude reduction and requires negligible time to perform. The accuracy of the methodology in estimating the substrate noise voltage is shown in Fig. 4. As illustrated in this figure, the peak noise voltage is accurately estimated with an error less than 5%. The overall agreement between the two waveforms is also reasonable where the rms error over several clock cycles is less than 10%. Note that even though the error is relatively higher at specific time instances, the methodology is significantly useful due to the great improvement in computational efficiency. The effect of noise reduction techniques can be evaluated and the iterations between the design and analysis cycle can be achieved in a reasonable amount of time. Note that the error has been evaluated with several different circuits and input patterns, producing similar results. The limitation of the methodology in terms of run time is the requirement to precharacterize each cell in the library for various input switching patterns and to perform a gate level simulation of the circuit to extract the required timing information.

B. Efficient Noise Reduction

Various approaches exist to reduce switching noise or alleviate the effect of switching noise on sensitive circuits. These

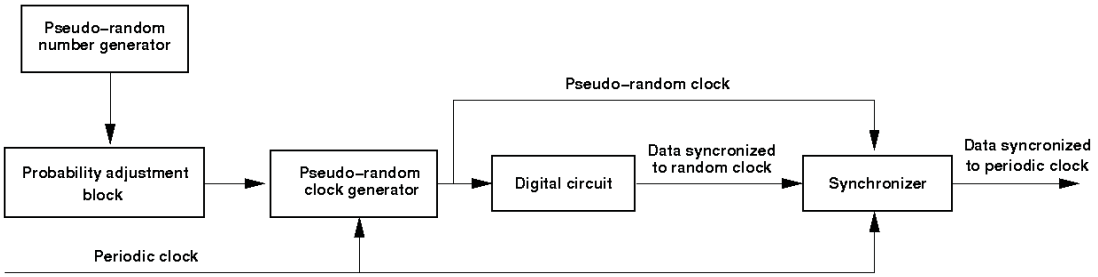

Fig. 5. **Pseudo-random clock generation to reduce switching noise and resynchronization with the periodic clock.**

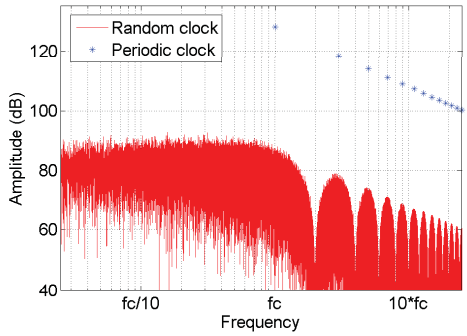

Fig. 6. **Comparison of the power spectral density of the periodic and random clock.**

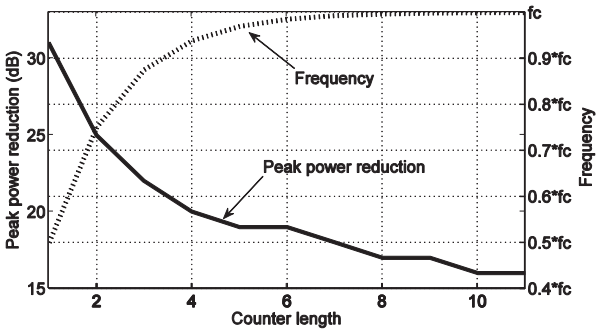

Fig. 7. **Tradeoff between the average frequency and reduction in noise.**

approaches can be classified under three primary categories [4]: (1) to reduce the input noise magnitude of the circuit such as reducing the parasitic inductance or using separate power/ground networks for analog and digital circuits, (2) to modify the noise transfer medium such as utilizing guard rings or a higher resistivity substrate, and (3) to reduce the sensitivity of the analog/RF circuit such as differential design. A methodology from the first category is described in this section to alleviate switching noise. Due to the complex noise coupling paths, radical noise reduction techniques are required to satisfy signal integrity constraints in heterogeneous systems. One of the approaches to significantly reduce switching noise is to adopt an asynchronous design methodology [5]. Unlike synchronous systems, an asynchronous circuit does not have a periodic clock signal. The absence of a clock signal significantly reduces the noise spikes that occur at the primary and harmonics of the clock frequency. Alternatively, asynchronous circuits are typically not well supported by computer-aided design tools and the additional area required by the handshaking protocols may not always be justified [6]. Due to these reasons, asynchronous design methodologies have had limited acceptance in practical applications.

The methodology proposed in this section provides similar advantages as asynchronous circuits while still utilizing a synchronous circuit with a clock signal. Specifically, rather than having a periodic clock signal, a pseudo-random clock is utilized where the power spectral density (PSD) of the clock signal is spread over the frequency spectrum, as depicted in Fig. 6. Note that spread spectrum is a well studied topic in communication theory. In this work, a similar approach is applied to reduce noise in heterogeneous systems. The block level representation of the proposed methodology is shown in Fig. 5. A linear feedback shift register produces a pseudo-random number sequence for the clock signal where the clock period is equal or greater than the original clock period. A probability adjustment block takes this pseudo-random number sequence as input to determine the amount of randomization. Next, the output of the probability adjustment block is used by the pseudo-random clock generator. This pseudo-random clock drives the aggressor circuitry rather than a standard periodic clock signal. Finally, the synchronizer unit synchronizes the data with the periodic clock.

As the randomization degree of the clock signal increases, the amount of noise reduction also increases since the PSD is further spread over the frequency spectrum. Alternatively, higher randomization produces a lower average clock frequency. In the proposed system, the probability adjustment block permits to determine the degree of the randomization. The appropriate randomization degree can be chosen based on the required noise reduction and minimum tolerable average frequency. This tradeoff between average frequency and reduction in noise is depicted in Fig. 7. Note that counter length is a parameter within the probability adjustment unit to determine the degree of randomization. The degree of randomization increases as the counter length is reduced, thereby achieving higher reduction in noise at the expense of reduced average clock frequency. Also note that even a sufficiently small degree of randomization can achieve a significant amount of reduction in noise. Specifically, for a counter length of 5, the frequency of the pseudo-random clock is 31/32 of the frequency of

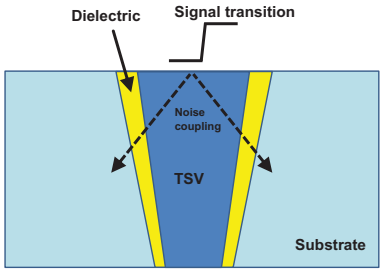

Fig. 8. **Cross section of a TSV carrying clock or data signals with high switching activity to illustrate noise injection into the substrate.**

the periodic clock. The reduction in speed is less than 4% of the periodic clock while achieving approximately 18 dB reduction in the peak spectral power. This characteristic of the dependence is exploited to significantly reduce switching noise while maintaining the average clock frequency within a reasonable value.

III. Noise Coupling in 3-D Integrated Systems

Several emerging opportunities exist at different levels of abstraction to satisfy stringent design constraints in next generation integrated systems. At the technology level, 3-D integration is a promising candidate to maintain the benefits of miniaturization by utilizing the vertical dimension [7]. In a monolithic 3-D IC, multiple planes or tiers are stacked on top of each other where through silicon vias (TSVs) are utilized to achieve communication among the planes [8]. 3-D technology is highly applicable to heterogeneous systems since each plane can serve as a platform for various functionalities such as electronics, optics, mechanics, and biochemistry.

It is typically assumed that a 3-D integrated system has enhanced noise coupling characteristics since each plane has a separate substrate, thereby improving signal isolation [7]. This assumption, however, is a falsified representation of reality in practical 3-D systems due to two primary reasons: (1) the TSVs carrying clock or data signals with high switching activity inject noise into the substrate of multiple planes, as shown in Fig. 8, and (2) since multiple planes need to share a common power and ground distribution network due to limited number of pads, the simultaneous switching noise on the ground network propagates across the planes. Furthermore, the substrate of each plane is essentially interconnected since the substrate is biased by the ground network, as depicted in Fig. 9.

Existing TSV placement methodologies primarily consider thermal stability and delay characteristics. Ignoring the effect of TSVs on the noise characteristics may significantly degrade the overall noise performance due to the noise injected into the substrate. Noise aware TSV placement methodologies should therefore be developed. For example, aggressor TSVs with high switching activity should be placed sufficiently far from the bulk node of the sensitive devices. These TSVs can also be shielded to further enhance noise isolation.

The second noise coupling mechanism is through the substrate networks of various planes that are indirectly connected. Assuming an aggressor circuit is placed on plane 1, the

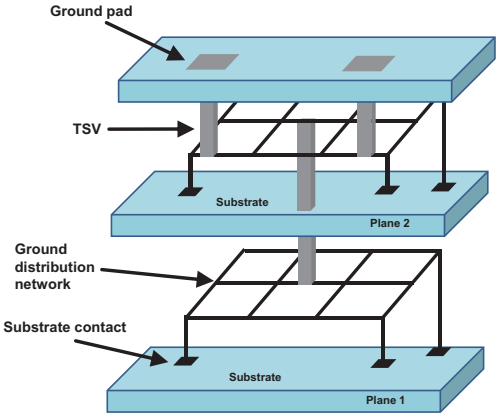

Fig. 9. **Common ground distribution network indirectly connects the substrate of the planes 1 and 2, degrading signal isolation among the planes.**

switching noise propagates to plane 2 through the common ground network. Furthermore, this noise can also be injected into the substrate of the second plane through the substrate contacts and TSVs, thereby propagating towards more sensitive analog/RF circuits and sensors. Due to these two coupling mechanisms, noise management emerges as a significant issue in heterogeneous 3-D systems despite the existence of separate substrates.

IV. Conclusions

A noise management methodology consisting of two primary steps has been described. The first step is the computationally efficient analysis of noise coupling in large scale heterogeneous systems. Small spatial voltage differences along the ground network are utilized to efficiently extract the substrate. The second step is a noise mitigation technique that significantly reduces the noise by utilizing a pseudo-random clock. A tight feedback loop between these two steps permits the integration of the proposed noise management methodology into existing design flows. Finally, the two primary noise coupling paths have been identified for next generation heterogeneous 3-D systems.

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