Optimization of Delta-Sigma ADC for Column-Level Data Conversion in CMOS Image Sensors

Alireza Mahmoodi and Dileepan Joseph

Department of Electrical and Computer Engineering, University of Alberta
9107 116th St NW, Edmonton, AB, T6G 2V4, Canada
Phone: +1 780 4929164, Fax: +1 780 4921811
Email: mahmoodi@ualberta.ca, dil.joseph@ualberta.ca

Abstract – *A delta-sigma analog-to-digital-converter (ADC) is designed, optimized and simulated for column-level data conversion in a CMOS image sensor. For a 0.18μm process, the design achieves 80dB of signal-to-noise ratio (SNR), including a 10dB margin for kTC noise not simulated, and consumes 210μW of power at a 50kHz sampling rate. Low power is realized mainly by using a first-order architecture and minimizing the capacitors. For the modulator, a boosted-folded-cascode operational transconductance amplifier (OTA) is optimized to achieve a gain of 90dB with a unity-gain bandwidth of 300MHz. The decimator is also optimized by placing part of the circuit at the chip level. Zero distortion is possible in the decimator due to the discrete-time nature of the input signal. The proposed ADC allows a reduction in the read-out nonlinearity of a CMOS image sensor, enabling a high SNR to be realized.*

I. INTRODUCTION

Nonlinearity and temporal noise of the analog read-out circuit are major constraints for achieving high signal-to-noise ratio (SNR) in low-voltage complementary-metal-oxide-semiconductor (CMOS) image sensors. As CMOS technology scales down to achieve higher speed and lower power consumption for digital circuits, analog circuits become more nonlinear and the lower supply voltage forces a lower dynamic range, at the input of the analog-to-digital converter (ADC), with respect to the temporal noise. These trends conspire, it seems, to lower the maximum-achievable SNR.

Unlike Nyquist rate ADCs, oversampled ADCs can filter the temporal noise without resorting to analog low-pass filters [1]. A reduction in temporal noise means the ADC can achieve a given SNR for a lower dynamic range. However, a lower dynamic range permits the read-out circuit to achieve a lower nonlinearity. Thus, the maximum-achievable SNR may be improved. This logic makes the delta-sigma ADC, which contributes very little nonlinearity of its own, an ideal choice for image sensors in low-voltage CMOS technology.

In image sensors, an ADC may be employed either at the chip level, the column level or the pixel level [2]. Pixel-level data conversion achieves a high SNR at the cost of a low pixel resolution. On the other hand, the chip-level approach achieves a high pixel resolution at the cost of a low SNR. Column-level data conversion presents a compromise between the two approaches [1]. A potential problem with column-level (or pixel-level) data conversion is that mismatch from one ADC to another introduces fixed pattern noise (FPN). Because delta-sigma ADCs are highly linear, the FPN will manifest as offset and gain variation only. With logarithmic-response image sensors, such variation is readily corrected [3].

For this paper, a delta-sigma ADC has been designed, optimized and simulated for column-level data conversion in a CMOS image sensor. Because a mega-pixel array has on the order of a thousand columns, the power consumption is critical and requires minimization. The ADC is designed to achieve an output SNR of 70dB at a frame rate of 50Hz. If there are 1000 pixels per column, a sampling frequency of 50kHz is therefore implied. Although not so important at the column level, the area usage also requires minimization in anticipation of a future delta-sigma design at the pixel level.

Sections II and III explain the design of the modulator and decimator, the two parts of any delta-sigma ADC. Section IV evaluates the design through simulation. Finally, Section V summarizes the paper and outlines future directions.

II. MODULATOR DESIGN

Assuming a switched-capacitor design, the power consumption and area usage of a delta-sigma modulator are directly proportional to the sizes of the capacitors. But the capacitors may not be made too small because of kTC noise and mismatch. A first-order modulator uses a higher oversampling ratio (OSR) than higher-order modulators. Thus, more kTC noise will be filtered during decimation, a feature that permits smaller capacitors. (Furthermore, a first-order modulator has a simple circuit, a property that minimizes area usage. The same may be said for the first-order decimator.)

More importantly, the first-order modulator is less sensitive to gain error of the integrator due to capacitor mismatch. In higher-order modulators, the precise output of the first integrator matters. Gain error due to capacitor mismatch will degrade the SNR. But the integrator output in a first-order modulator
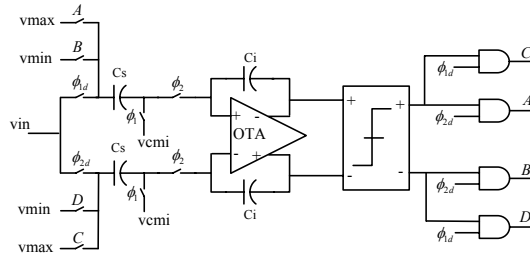
Fig. 1. Schematic of the switched-capacitor delta-sigma modulator.

drives a quantizer only. For single-bit quantization, chosen for linearity and compactness, any gain error will have negligible effect on SNR. By choosing a first-order modulator, the circuit will tolerate more capacitance mismatch and, therefore, smaller capacitors may be used to decrease the power consumption and area usage substantially.

A future direction of this work is to compare the performance of the analog modulator predicted by theory and simulation to that measured by experiment. Barring a layout mistake, the digital decimator is expected to work perfectly. Although an OSR of 500 is enough to achieve an SNR of 70dB with first-order modulation, an OSR of 1000 is chosen to ensure that quantization noise is not the dominant noise at the ADC output. In this way, the SNR derived by experiment will measure the performance of the modulator alone. In general, to optimize the ADC properly, the SNR should be limited equally by both the modulator and decimator.

At a 50kHz sampling rate, $20\mu s$ is available to sample each pixel in a column. Allowing for column bus capacitance, $5\mu s$ is budgeted for the pixel output to settle at the input of the ADC. Thus, there is actually $15\mu s$ available to digitize the output of each pixel. Since the OSR is 1000, the oversampling period of the modulator is 15ns. From this total, 7.5ns has been alloted to switched-capacitor sampling and the rest to integration.

Figure 1 shows the schematic of the switched-capacitor delta-sigma modulator. A differential architecture is used since it can reject the common-mode noise in the circuit. Since the pixel is single ended, a modulator with a single input is designed. The integrator is the most critical part of the modulator, while the operational transconductance amplifier (OTA) is the most critical part of the integrator [4]. The analog parts must be carefully designed because their nonidealities may limit the overall ADC performance.

In order to derive the specifications for the modulator, a threshold for input-referred noise is defined below based on the required SNR. The effect of a nonideality is then modeled as an input noise and circuit parameters are designed so that the noise contribution does not exceed the defined threshold.

A. Threshold noise calculation

The output signal of a delta-sigma modulator is equal to its input signal plus filtered quantization noise. Assume that the analog noise at the modulator input is white with power P_n and that it overpowers the quantization noise at the ADC output. Then the noise power at the decimator output P_{n-dec}, which determines the SNR, depends on a (causal) decimation filter $h_{dec}[n]$ according to Parseval's theorem, i.e.

$$P_{n-dec} = P_n \sum_{n=0}^{\infty} |h_{dec}[n]|^2. \tag{1}$$

The optimal decimation filter for first-order delta-sigma modulation, which will be discussed further in Section III, has a parabolic finite impulse response [5], i.e.

$$h_{dec}[n] = \begin{cases} h[n]/S, & 0 \leq n \leq OSR - 1 \\ 0, & \text{otherwise} \end{cases}, \tag{2}$$

where

$$h[n] = OSR + n(OSR - 1) - n^2 \tag{3}$$

and

$$S = \frac{OSR(OSR+1)(OSR+2)}{6}. \tag{4}$$

For large OSR, it can be shown using the above equations that the output noise is given to a good accuaracy by

$$P_{n-dec} = \frac{6P_n}{5 OSR} \tag{5}$$

Therefore, the SNR at the ADC output is given by

$$SNR = \frac{P_s}{P_{n-dec}} = \frac{5P_s OSR}{6P_n}, \tag{6}$$

where P_s is the signal power.

For an OSR of 1000, assuming a uniformly-distributed signal over a 0.7V range in each input branch, the input-referred noise P_n must be less than $1.36 \times 10^{-5}\text{V}^2$ to achieve an SNR of 70dB. Given that there are multiple uncorrelated noise sources that can be referred to the OTA input (switching noise, charge injection, clock feedthrough etc.), the power of each should be less than say one fifth of this figure, which is $2.72 \times 10^{-6}\text{V}^2$, to meet the specifications. Every noise source is thus referred to the input and compared to this threshold.

B. Specifications of the modulator

Modulator design involves determining the integrating capacitor C_i, sampling capacitor C_s, integrator gain g, peak-to-peak range of the OTA output V_{o-pp}, unity gain bandwidth (UGB) and slew rate (SLR) of the OTA, time-constant of the

integrator τ, and current in the OTA branches I. In the first-order modulator, the output range of the integrator with unity gain is twice the input range of the modulator. The gain is also a capacitance ratio [4], i.e.

$$g = \frac{C_s}{C_i} = \frac{V_{o-pp}}{2V_{i-pp}}. \tag{7}$$

Assuming a single dominant pole for the OTA, and assuming that the OTA is not slewing, the time constant of the integrator when responding to a step input is given by [4]

$$\tau \approx \frac{1}{\omega}\left(1 + \frac{C_s}{C_i}\right), \tag{8}$$

where ω is the UGB of the OTA. The minimum required SLR of the OTA is given by [6]

$$SLR = \frac{I}{C_i} > \frac{1.1V_{o-pp}}{2T}, \tag{9}$$

where T is the integration time.

Assume that the OTA has a single dominant pole. To ensure no slewing at the OTA output, the SLR should be chosen greater than the maximum possible slope, which is $V_{o-pp}/2\tau$. But designing the OTA with no slewing requires high current for the OTA and consequently would lead to a much higher UGB for the OTA, which is not required. The optimum solution is to have slewing at the OTA output which is compensated by a reasonable UGB and a corresponding τ.

The first-order structure is not sensitive to capacitance mismatch and the resulting gain error. The minimum value for the capacitors in the integrator is determined by kTC noise. Assuming that kTC noise from different capacitors are uncorrelated, the total kTC noise power referred to the input can be shown to equal

$$P_{n-kTC} = \frac{2kT}{C_i g^2} + \frac{2kT}{gC_i}. \tag{10}$$

Equations (7), (9) and (10) show that the integrator gain should be chosen based on the limitations on input-referred noise, SLR and dynamic range of the OTA. A smaller gain would result in more input-referred noise. Also, a higher gain would increase the required SLR and dynamic range of the OTA. Considering a maximum-achievable dynamic range, with high enough gain in a CMOS 0.18μm process, of around 0.6V, a gain of $1/3$ is chosen to meet both of the constraints. Therefore, the total kTC noise is

$$P_{n-kTC} = \frac{24kT}{C_i}. \tag{11}$$

From the discussion in Section II-A, the total kTC noise must be less than 2.72×10^{-6}V^2. Thus, the minimum value for the integrating capacitor C_i is 37fF. The integrating capacitor is chosen to be 60fF, leaving enough margin to account for any mismatch in the capacitors that would change the gain

and therefore affect the input-referred kTC noise power. The sampling capacitor C_i is chosen to be 20fF in order to achieve the gain of $1/3$ in the integrator.

Assuming the integrator output is uniformly distributed in its range, the settling error at the integrator output would be uniformly distributed over $\pm(2 \times 0.7/3)e^{-t/\tau}$. By referring the integrator output error to the input and comparing it to the threshold noise, it can be concluded that the integration interval must be at least 6.2 times greater than the integrator time constant. In our case, the integration interval is 7.5ns so the time constant must be less than 1.21ns. Considering the fact that switch resistances are not zero, the time constant is chosen to be 0.9ns. So the UGB of the OTA with no slewing can be derived from (8) to be 265MHz.

The input signal range V_{i-pp} is 0.7V. From (7), V_{o-pp} is therefore 0.47V. So the SLR should be between 34.2V/μs and 259V/μs. An SLR of 125V/μs with a UGB of 300MHz was chosen for the main OTA.

Although many specifications are determined theoretically, modeling the system in Simulink is very helpful [7]. The finite DC gain of the OTA introduces gain error and leakage in the integrator. Although gain error of the integrator is not a serious problem in a first-order modulator, leakage can greatly affect the output SNR. Therefore, an integrator with leakage was simulated to determine the required DC gain of the OTA. The simulation results showed that a gain of at least 65dB was needed for an SNR of 70dB.

Nonlinearity effects of the OTA are difficult to analyze [7]. But as long as the overall DC gain of the OTA including nonlinearity is higher than the desired threshold of 65dB, the performance will not degrade. Assuming a maximum of 15dB reduction in gain due to nonlinearity, a gain of 80dB is needed.

Thermal or flicker noise may also be present at the OTA input. The thermal noise of a long-channel MOS device can be modeled by a voltage source in series with the gate and having a power spectral density (PSD) of [8]

$$\overline{V_n^2} = \frac{4kT\gamma}{g_m}, \tag{12}$$

where k is Boltzmann's constant and γ is 2/3 for a long-channel device. The flicker noise can also be modeled as a voltage source in series with the gate, with a PSD of about [8]

$$\overline{V_n^2} = \frac{K}{C_{ox}WL} \cdot \frac{1}{f}, \tag{13}$$

where K is a process-dependent constant on the order of 10^{-25}. Even using minimum-size transistors with an overdrive voltage of at least 0.2V, one can ensure that the thermal and flicker noise of input transistors in the OTA are much less than the threshold and therefore will not degrade the performance of the ADC. Consequently, no correlated double-sampling circuit is needed to alleviate the flicker noise.

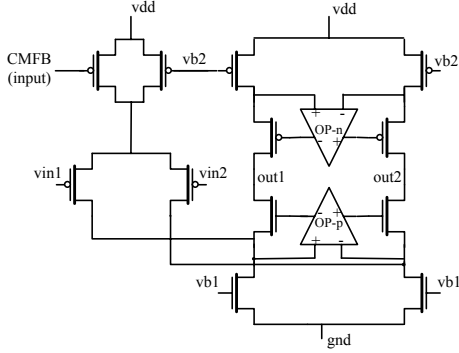Nonidealities due to the switches are mostly nonlinear resistance, clock feedthrough and charge injection [4].

Fig. 2. Schematic of the gain-boosted folded-cascode OTA.

Fig. 3. Schematic of the differential-difference common-mode feedback circuit.

TABLE I. Specifications of the designed OTA.

Power consumption	130μW
Dynamic range	0.6V
DC gain	90dB
Slew rate	125V$/\mu$s
Load capacitance	60fF
Unity gain bandwidth	300MHz
Phase margin	$60°$

A differential-mode integrator will greatly attenuate the common-mode noise, thereby decreasing the effect of charge injection and clock feedthrough. The transistors must be large enough so that the nonlinearity of their on-resistance does not affect the settling behavior.

Noise and distortion due to circuit nonidealities occurring after the integrator will be greatly attenuated when referred back through the integrator. Therefore the offset and hysteresis of the comparator used to implement the one-bit quantizer can be widely tolerated. A comparator offset would change the signal range that is fed back in the delta-sigma loop to the integrator. But as long as there is enough dynamic range at the integrator input, the comparator offset will not degrade the performance. This is taken into account by adding a 0.13V margin to the $0.47V$ dynamic range previously specified. Simulation shows that the comparator hysteresis must be less than 0.1V [4]. A regenerative latch was used as the comparator [4].

The effect of clock jitter in the ADC is mostly a variation in the sampling time of the analog input signal [7]. Since the input signal for our ADC is constant during the Nyquist interval, a variation of sampling time is not important.

C. Operational transconductance amplifier

The folded-cascode OTA structure is well known for switched-capacitor applications [8]. But its gain is insufficient for our ADC. The gain-boosting technique is therefore employed at the cost of requiring two supplementary OTAs [8]. This technique can raise two significant problems, i.e. doublets and instability. Thus, zero and pole locations must be designed carefully. Figure 2 shows the structure of the main OTA.

A differential-mode OTA has the advantage of rejecting the common-mode noise but it needs a common-mode feedback (CMFB) circuit to specify the output common mode. Conventional switched capacitor CMFB (SC-CMFB) circuits have high output swing with high accuracy and low static power consumption, and are preferred for switched-capacitor appli-
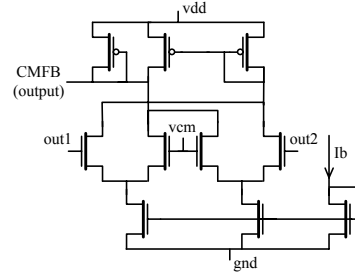
cations [8], but they load the output of the OTA, reducing its UGB and SLR. Also, SC-CMFB circuits occupy a large area.

Since it can offer enough swing and linearity with a small area, a differential-difference amplifier CMFB (DDA-CMFB), which is a continuous-time CMFB, is used in the main OTA [9]. Figure 3 shows the structure of the DDA-CMFB circuit. The same CMFB circuit is used for supplementary OTAs.

The OTAs were optimized to minimize the power consumption for the dynamic range of 0.6V. Any mismatch in the capacitors would modify the gain, and therefore the required dynamic range, but a 0.13V margin was included in Section II-B. Since process variation can affect the OTA performance, the OTAs were designed with enough margin to tolerate the process variation. Table I gives the specifications of the main OTA. Monte Carlo simulation was done to make sure that the OTA can meet the required specifications.

III. DECIMATOR DESIGN

In conventional continuous-input delta-sigma ADCs, decimation is often performed in several stages [4]. Many of the decimation filters are based on the comb filter for the first stage, which has a k-sample impulse response, where k is the decimation ratio of the first stage. The optimal decimation filter with a k-tap duration for the first-order modulator has a parabolic shape [5]. In practice, triangular filters are implemented since they are easier to implement while they can achieve an SNR very close to the optimal filter [4]. There is always some dis-
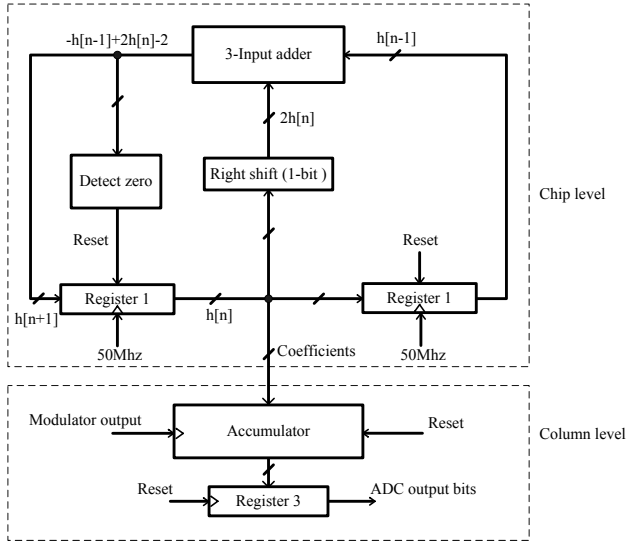
Fig. 4. Schematic of the decimator, including a chip-level coefficient generator and a column-level accumulator.

tortion of frequency components close to the Nyquist rate, although it is small for high OSRs.

For a discrete-input delta-sigma ADC, distortion may be avoided altogether if decimation is done with a one-stage OSR-tap FIR filter. As before, the optimal filter has the parabolic shape. Briefly, the reason there is no distortion is as follows. The analog part of the ADC outputs the input signal plus the shaped quantization noise. Since the input signal of the ADC is constant for exactly OSR samples, the output of an OSR-tap decimation filter depends only on one sample of the input. While filtering the quantization noise, the decimation filter at worst multiplies the input signal by a gain. If the sum of the impulse response coefficients of the decimation filter equals one then the gain of the decimation filter would also be one for the input signal. If the filter has more than OSR taps, distortion appears and it may limit the output SNR.

Different structures for the decimation filter with triangular shape have been reported in the literature but they have not been designed for column-level ADC in an image sensor. Figure 4 shows the structure of the proposed decimator, which implements the optimum filter, i.e. the impulse response in (2). The coefficients of the decimation filter are generated at the chip level. In each column, coefficients must be multiplied to the modulator output and accumulated. Since the modulator output is a stream of single bits, multiplication reduces to logical AND. However, if the bit stream from the modulator drives the clock of the accumulator, even the AND logic is not required. Therefore, the decimation filter is only an accumulator for the coefficients coming from the generator located at the chip level, and its clock is the output of the modulator. The accumulated value is dumped every OSR samples.

It can be shown that de-normalized coefficients $h[n]$ from

TABLE II. Specifications of the designed ADC.

Modulator power	150μW
Decimator power	60μW
Dynamic range	0.7V
Nyquist rate	50kHz
Oversampling ratio	1000
Signal-to-noise ratio	70–80dB

(3) obey the recurrence

$$h[n+1] = -h[n-1] + 2h[n] - 2. \qquad (14)$$

Registers 1 and 2 store $h[n]$ and $h[n-1]$ and are initialized to the OSR and zero. After one Nyquist interval of OSR samples, $h[n+1]$ will be zero according to the recurrence. Thus, zero detection may be used to create a reset signal. Registers 1 and 2 will be reset to the OSR and zero and the next Nyquist interval will begin. Therefore, no separate reset signal or counter is needed for the decimator.

The specifications of the ADC, obtained partly by simulation, are given in Table II. Although the coefficient generator consumes 200μW of power, it has not been included in the decimator figure as there is only one coefficient generator at the chip level, which is negligible in terms of total power when compared to the 1000 column-level accumulators.

As discussed before, the ADC is not working 25% of the time. Thus, 25% of the power consumption in the modulator could be saved by turning it off during this period. Last but not least, since the pixel cannot drive the current-hungry input of the ADC, a buffer has to be designed. A simple structure for the buffer is a source follower, which unfortunately has high nonlinearity. Therefore, a more linear buffer must be designed.

IV. SIMULATION RESULTS

Simulation of the proposed ADC was done for a 0.18μm CMOS process using Cadence and Simulink. Since a simulation of the whole circuit in Cadence would take a long time, the modulator was simulated in Cadence and the output bit stream was exported to Simulink for decimation and SNR calculation. One assumes that the digital part of the ADC would work without any degradation in performance. The ADC was also simulated using Simulink alone, by assuming an ideal integrator and quantizer, for comparison to the Cadence-Simulink results. A theoretical result for SNR may also be found, specific to the decimation filter in use.

Figure 5 shows the theoretical and simulation results for SNR versus OSR. The oversampling frequency always equals 50MHz. So, in effect, the sampling frequency depends inversely on the OSR in the figure. The modulator was designed to achieve an SNR of at least 70dB. Simulation shows that performance of the circuit is limited to 80dB as kTC noise was not
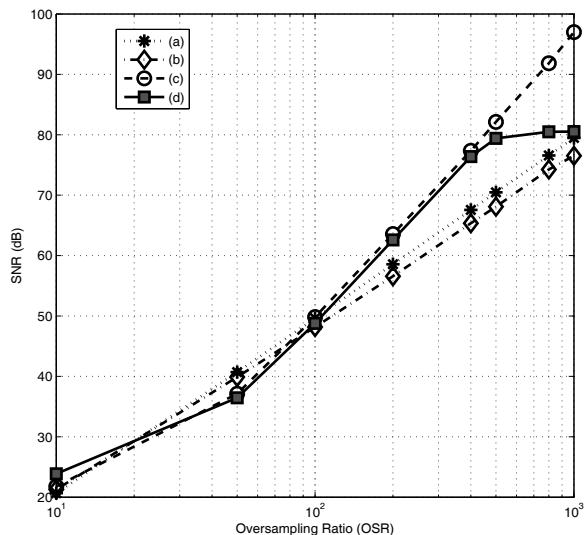
Fig. 5. SNR versus OSR of the proposed ADC based on: (a) theoretical calculation; (b) Simulink (modulator and decimator) using 5000 samples; (c) Simulink (modulator and decimator) using 50 samples; and (d) Cadence (modulator) and Simulink (decimator) using 50 samples. The samples are input voltages that are equally spaced over the dynamic range.

V. CONCLUSION

The design of a first-order delta-sigma ADC for column-level data conversion in an image sensor has been presented. Modulator design focused on capacitor minimization. Decimator design was influenced by the discrete-time nature of the ADC input signal, owing to the discreteness of pixels in a column. The proposed ADC has a very low power consumption.

Since the first-order modulator is not sensitive to gain error due to capacitor mismatch, minimum-size capacitors may be used to minimize the power consumption. A gain-boosted folded-cascode OTA finds good use in the integrator. Owing to the discrete input, the proposed decimator has zero distortion. Part of the decimator may be placed at the chip level.

Simulation results, using Cadence and Simulink, are very close to the theoretical values for SNR. Presently, the design is being laid out in a 0.18μm process, which will allow the area usage to be determined (it is also expected to be low). Ultimately, the design will be fabricated and tested.

included in the simulation. Differences between the theory and simulation occur because the latter involve a limited number of input voltages. Only 50 input voltages have been considered in Cadence because each transient simulation takes a long time. Simulation was done in Simulink with 5000 input voltages to show that the simulation results approach the theoretical ones with more samples.

In a first-order delta-sigma ADC, quantization noise power depends on voltage for constant inputs, varying by up to ± 10dB [4]. The simulations with 50 samples have higher SNRs compared to the theory. Hence, it appears the quantization noise for 50 equally-spaced input voltages over the dynamic range is lower than the expected noise over the whole range. Since the noise depends on input level, a 10dB margin was included in the 70dB SNR announced in Section I.

To evaluate the performance of the designed ADC, consider the usual figure-of-merit, which is defined as

$$FM = \frac{P}{2^b f_N}, \qquad (15)$$

where f_N is the Nyquist sampling rate, P is the power consumption, and b is the bit resolution of the ADC. The designed ADC has a figure-of-merit of 0.4pJ in the best case for the SNR of 80dB and 1.3pJ for the worst-case SNR of 70dB. This compares favorably with the reported state-of-the-art ADC with a figure-of-merit of 1.51pJ [10].

References

[1] J. Fortier, N.G. Tarr, A. Swaminathan, and C. Plett, "1.2 v 0.18 um cmos imager with column-level oversampling," in *Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27th European*, 18-20 Sept. 2001, pp. 105–108.

[2] A. El Gamal and H. Eltoukhy, "Cmos image sensors," *Circuits and Devices Magazine, IEEE*, vol. 21, no. 3, pp. 6–20, May-June 2005.

[3] D. Joseph and S. Collins, "Modeling, calibration, and correction of non-linear illumination-dependent fixed pattern noise in logarithmic cmos image sensors," *Instrumentation and Measurement, IEEE Transactions on*, vol. 51, no. 5, pp. 996–1001, Oct. 2002.

[4] S.R. Norsworthy, R. Schreier, and G.C. Temes, Eds., *Delta-sigma data-theory design and simulation*, IEEE Press, 1997.

[5] J. Candy, Y. Ching, and D. Alexander, "Using triangularly weighted interpolation to get 13-bit pcm from a sigma-delta modulator," *Communications, IEEE Transactions on [legacy, pre - 1988]*, vol. 24, no. 11, pp. 1268–1275, Nov 1976.

[6] B.E. Boser and B.A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *Solid-State Circuits, IEEE Journal of*, vol. 23, no. 6, pp. 1298–1308, Dec. 1988.

[7] H. Zare-Hoseini, I. Kale, and O. Shoaei, "Modeling of switched-capacitor delta-sigma modulators in simulink," *Instrumentation and Measurement, IEEE Transactions on*, vol. 54, no. 4, pp. 1646–1654, Aug. 2005.

[8] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Inc., 2000.

[9] L. Luh, J. Choma Jr., and J. Draper, "A continuous-time common-mode feedback circuit (cmfb) for high-impedance current mode application," in *Electronics, Circuits and Systems, 1998 IEEE International Conference on*, 7-10 Sept. 1998, vol. 3, pp. 347–350.

[10] M. Safi-Harb and G.W. Roberts, "Low power delta-sigma modulator for adsl applications in a low-voltage cmos technology," *Circuits and Systems I: Regular Papers, IEEE Transactions on [see also Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]*, vol. 52, no. 10, pp. 2075–2089, Oct. 2005.