Russell Tessier

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As a professor for 25 years, I have published 160 research papers in top conference proceedings and scientific journals. My research has been funded by government and industry groups, including the National Science Foundation, the National Institutes of Health, and the Massachusetts Department of Transportation.

APPOINTMENTS

Academic

University of Massachusetts, Amherst, MA
- **Department Head** of Electrical and Computer Engineering, July 2024 - present.
- **Professor** of Electrical and Computer Engineering, September 2012 - present.
- **Senior Associate Dean** of Engineering, September 2019 - July 2024.
- **Acting/Interim Department Head** of Chemical Engineering, August 2022 - September 2023.
- **Associate Dean** of Engineering, January 2017 - August 2019.
- **Acting Department Head** of Biomedical Engineering, February 2019 - May 2019.
- **Associate Professor** of Electrical and Computer Engineering, September 2004 - August 2012.
- **Project Leader**, CASA Engineering Research Center, October 2003 - December 2006.
- **Assistant Professor** of Electrical and Computer Engineering, January 1999 - August 2004.

Ruhr University, Bochum, Germany
- **Visiting Researcher**, May 2018 - June 2018.

Université de Rennes, Lannion, France
- **Visiting Researcher**, June 2013.

Université de Bretagne Sud, Lorient, France
- **Visiting Researcher**, June 2007, June 2008, July 2011.

University of Toronto, ON, Canada
- **Visiting Professor**, January 2005 - December 2005.

Massachusetts Institute of Technology, Cambridge, MA
- **Graduate Research Assistant**, January 1990 - October 1998.
- **Graduate Resident Tutor**, August 1990 - August 1997.

Industry

Mentor Graphics Corporation, Waltham, MA
- **Systems Design Consultant**, January 2008 - January 2009.
- **Software Engineer**, May 1996 - September 2001.

Altera Corporation, Toronto, ON, Canada
- **Software Engineer**, January 2005 - August 2005.
- **Legal Expert Witness**, October 2001 - April 2002.

Prosensing, Inc., Amherst, MA
- **Hardware Design Consultant**, September 2000 - January 2004.

Virtual Machine Works, Inc., Cambridge, MA
- **Founder and Principal Engineer**, January 1994 - May 1996.

BBN Corporation, Cambridge, MA
- **Hardware Engineer**, June 1992 - January 1994.

Data General Corporation, Westboro, MA

- **Software Engineer**, May 1989 - August 1989.

EDUCATION

Degrees

Massachusetts Institute of Technology, Cambridge, MA

- Ph.D. in Electrical Engineering and Computer Science, February 1999, Advisor: Stephen A. Ward,
  Dissertation: "Fast Place and Route Approaches for FPGAs."
- S.M. in Electrical Engineering and Computer Science, June 1992,
  Thesis: "A Sparc-based Processing Element for the NuMesh."

Rensselaer Polytechnic Institute, Troy, NY

- B.S. in Computer and Systems Engineering, May 1989.

Professional Development

Harvard Institutes for Higher Education, Harvard Graduate School of Education, Cambridge, MA

- Management Development Program (MDP), June 2019.

University of Massachusetts Amherst, MA

- Chancellor's Leadership Fellowship, September 2015 - May 2016.
- Lilly Teaching Fellowship, September 2002 - May 2003.

ADMINISTRATIVE EXPERIENCE

Department Head of Electrical and Computer Engineering (July 2024 - present)

Senior Associate Dean for Academic Affairs and Operations (September 2019 - July 2024)

Responsibilities: I served as the coordinator for all distance learning and Mt. Ida programs in the College of Engineering. This role involves the development of new programs and policies to facilitate distance and experiential learning. I advised the College's information technology group (3 staff, $600,000 budget), manage space allocation for the College's research programs, evaluated staff, and led strategic planning. In conjunction with the dean, I evaluated tenure, promotion, and reappointment cases for all faculty members in the College (150 professors and instructors) and supervise the selection of student, faculty, and staff award recipients. I led new faculty development programs in the College. I served as the primary College liaison in the design of the new Sustainable Engineering Laboratories building, scheduled to open in 2026.

Accomplishments: I worked with the Graduate School and the International Programs Office to create a policy that allows non-thesis international graduate students to participate in off-campus work experiences during the academic year. The policy was approved by the Graduate Council and the Faculty Senate. In conjunction with the Engineering Career Development and Experiential Learning Center, I remade the College's internship program to improve student experiential learning opportunities. Under my direction, the yearly gross income of the College's distance learning programs increased from $200,000 to $2.0M per year in seven years. I worked with academic departments to allocate research space to new faculty members and led the College's strategic planning efforts. To assist new faculty, I implemented a monthly seminar program that includes research, teaching, and proposal writing training. New faculty have received 24 NSF CAREER awards in the past seven years, including a College record of five awards in 2020. In conjunction with the College of Engineering Office of Diversity, Equity and Inclusion, I initiated a college-wide Diversity, Equity, and Inclusion Award. I worked with

architects to perform a site study and develop a concept design for the new Sustainable Engineering Laboratories building.

Acting/Interim Department Head of Chemical Engineering (August 2022 - September 2023)

Responsibilities: I led departmental activities for 20 faculty members and supervised seven staff members. I served as the coordinator for staff hiring, budgeting, personnel management, curriculum development, and student outreach.

Accomplishments: I evaluated a faculty member for tenure and promotion and developed the teaching and service schedule for the academic year. I organized and ran monthly faculty meetings and served as the liaison for the department's Industrial Advisory Board. Budgeting and facilities allocation were important aspects of the position. I nominated several faculty members for international, campus, and College of Engineering awards.

Acting Department Head of Biomedical Engineering (February 2019 - May 2019)

Responsibilities: I supervised staff and faculty hiring, budgeting, personnel management, curriculum development, and student outreach.

Accomplishments: I negotiated with and hired three tenure-track faculty members and one instructor. I made faculty teaching assignments, addressed personnel matters, and developed an operating budget. I initiated several student-focused events, including an all-department pizza party, and instituted an open-door policy for students and faculty to obtain feedback.

Associate Dean for Graduate Studies and Operations (January 2017 - August 2019)

Responsibilities: I assisted in the development of new degree and certificate programs and supervised their campus approval. I managed a graduate fellowship program and developed selection criteria for the awards. I selected and trained graduate students to serve as freshman seminar instructors and supervised all distance learning programs in the College of Engineering. In conjunction with the dean, I evaluated tenure, promotion, and reappointment cases for all faculty members in the College (120 professors and instructors). I led new faculty development and training programs in the College.

Accomplishments: I developed four graduate certificates in computer engineering and guided their campus approval. I refocused the College's graduate fellowship program on incoming students from diverse backgrounds. The program led to 42 new doctoral students joining the College over a three year period. I managed many of the day-to-day administrative activities of a new synchronous distance learning program for the College. I oversaw the opening the new Graduate Engineering Hub, a dedicated space for graduate students, and developed new faculty mentoring workshops on research group supervision and grant proposal writing.

Chancellor's Leadership Fellow (September 2015 - May 2016)

Responsibilities: I worked with Senior Vice Provost Carol Barr to develop student success strategies for the campus.

Accomplishments: I interviewed the undergraduate academic deans in colleges and schools across campus to better understand their perspectives on student success. I wrote a forty-page report on the state of student success initiatives on the campus and offered suggestions on potential improvements.

Graduate Resident Tutor (August 1990 - August 1997)

Responsibilities: As a graduate student at MIT, I served as a counselor and mentor in an undergradu-

ate residence hall.

Accomplishments: I managed the student activity budget for a residence hall of thirty undergraduate students and engaged in event planning, counseling, and academic tutoring.

AWARDS

External

- Best Paper Award, IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, 2023.
- Stamatis Vassiliadis Award, Best Paper, International Conference on Field Programmable Logic and Applications, 2019.
- Best Poster Award, IEEE International Symposium on VLSI, 2014.
- Most Significant Paper, 20th Anniversary, IEEE International Symposium on FCCMs, 2013.
- Best Paper Award, IEEE Conference on Communications and Network Security, 2013.
- Best Paper Award, ACM Great Lakes Symposium on VLSI, 2012.
- Best Paper Award, ACM Workshop on Virtualized Infrastructure Systems and Architectures, 2010.
- Keynote address, International Workshop on Security Proofs for Embedded Systems, 2022.
- Keynote address, Conference on Reconfigurable Communication-Centric SoCs, 2007.

Internal

- Outstanding Senior Faculty Award, College of Engineering, 2018.
- UMass Distinguished Teaching Award, nominee, 2010, 2011, 2018.
- Early tenure and promotion, 2004.
- Barbara A. and Joseph I. Goldstein Outstanding Junior Faculty Award, College of Engineering, 2002 - 2003.
- Outstanding Teaching Award, College of Engineering, 2003.
- Outstanding Faculty Award, IEEE Student Chapter, 2001.

FUNDED RESEARCH PROPOSALS

Research

G1. Emerging Security Challenges and a Solution Framework for FPGA-accelerated Cloud Computing (co-PI, PI S. Kundu)
Funding source: National Science Foundation
10/1/23-9/30/26
Total amount: $300,000, My share: $150,216

G2. Laboratory Information Materials Management System Development (PI, co-PI C. Ai, J. Gummeson)
Funding source: Massachusetts Department of Transportation
3/1/23-7/31/24
Total amount: $300,000, My share: $150,000

G3. Flexible Network Interface (FNI) Endpoint Development (sole-PI)
Funding source: LinQuest
9/1/22-8/31/24
Total amount: $172,940, My share: $172,940

G4. Development of a Salt Spreader Controller Program Using Machine-Sensed Roadway Weather Parameters (co-PI, PI C. Ai)
Funding source: MassDOT
4/25/22-4/24/24
Total amount: $125,000, My share: $62,500

G5. SNOWWI: Snow Water-equivalent Wide Swath Interferometer and Scatterometer (co-PI, PI P. Siqueira)
Funding source: NASA
3/1/22-2/28/25
Total amount: $675,000, My share: $100,000

G6. Hardware Security for Machine Learning and Supply Chain (co-PI, PI D. Holcomb)
Funding source: Raytheon Technologies
9/7/21-1/8/22
Total amount: $75,000, My share: $18,750

G7. FPGA Computer-Aided Design Security (sole-PI)
Funding source: AnTrust
8/2/21-8/1/22
Total amount: $347,000, My share: $347,000

G8. Global Network Access Terminals for the Space Combat Cloud (sole-PI)
Funding source: Applied Technology Associates
4/1/20-9/21/20
Total amount: $75,000, My share: $75,000

G9. Security of Reconfigurable Cloud Computing (PI, co-PI D. Holcomb)
Funding source: National Science Foundation
7/1/19-6/30/24
Total amount: $690,839, My share: $390,000

G10. Links and Networks for Space (sole-PI)
Funding source: Leidos Corporation
6/20/19-3/8/20
Total amount: $50,800, My share: $50,800

G11. Generation of Amazon EC2 F1 (PI, co-PI D. Holcomb)
Funding source: Gradient
6/1/19-12/31/19
Total amount: $20,000, My share: $10,000

G12. Satellite Communication Emulation Environment (sole-PI)
Funding source: Intelligent Fusion Technology
5/20/19-8/31/21
Total amount: $100,000, My share: $100,000

G13. Security for Multi-Tenant FPGAs (PI, co-PI D. Holcomb)
Funding source: Intel Corporation
11/1/17-10/31/21
Total amount: $365,000, My share: $200,000

G14. SecureDust – The Physical Limits of Information Security (co-PI, PI D. Holcomb)
Funding source: National Science Foundation / Semiconductor Research Corporation
9/1/16-8/31/20
Total amount: $462,212, My share: $150,000

G15. Hardware Security for Embedded Computing Systems (co-PI, PI T. Wolf)

Funding source: National Science Foundation
8/1/16-7/31/20
Total amount: $512,523, My share: $230,000

G16. Network Function Virtualization Using Dynamic Reconfiguration (PI, co-PI L. Gao)
Funding source: National Science Foundation
10/1/15-9/30/19
Total amount: $499,000, My share: $245,000

G17. New Architectures for Coarse-Grained Reconfigurable Arrays (sole-PI)
Funding source: Xilinx Corporation
9/1/15-12/31/16
Total amount: $40,000, My share: $40,000

G18. New Directions in FPGA Security (PI, co-PI C. Paar)
Funding source: National Science Foundation
10/1/13-9/30/17
Total amount: $432,000, My share: $215,000

G19. Evaluation of Portable Road Weather Information Systems (PI, co-PI S. Gao, D. Hardy)
Funding source: Massachusetts Department of Transportation
10/1/12-6/30/16
Total amount: $395,000, My share: $275,000

G20. Mass Casualty Management System (DIORAMA-II) (co-PI, PI A. Ganz)
Funding source: National Institutes of Health
9/30/12-8/31/16
Total amount: $1,600,000, My share: $200,000

G21. Migration of the DE5 to the NetFPGA and Linux (sole-PI)
Funding source: Altera Corporation
9/1/12-12/31/15
Total amount: $65,000, My share: $65,000

G22. Eliminating the Energy Efficiency Barrier of Reconfigurable Architectures for Diverse Signal Processing (PI, co-PI S. Kundu)
Funding source: National Science Foundation
6/1/12-5/31/16
Total amount: $264,953, My share: $132,500

G23. Securing the Router Infrastructure of the Internet (co-PI, PI T. Wolf)
Funding source: National Science Foundation
9/1/11-8/31/15
Total amount: $500,000, My share: $250,000

G24. Automated Counting of Pedestrians and Bicyclists on an Urban Roadside (PI, co-PI D. Ni)
Funding source: Massachusetts Department of Transportation
10/1/09-6/30/12
Total amount: $228,000, My share: $114,000.

G25. Migration of the DE4 to the NetFPGA (sole-PI)
Funding source: Altera Corporation
9/1/10-12/31/12
Total amount: $45,000, My share: $45,000

G26. On-Chip Sensing Strategies for Efficient Scalability in Many-Core Architectures (PI, co-PI W. Burleson)
Funding source: Semiconductor Research Corporation

8/1/10-7/31/13
Total amount: $300,000, My share: $150,000

G27. Vehicle Infrastructure Integration (VII): Exploring the Application of Disruptive Technology to Assist Older Drivers (co-PI, PI: D. Ni, co-PI: H. Pishro-Nik)
Funding source: New England University Transportation Consortium
9/1/09-12/31/10
Total amount: $100,000, My share: $33,000

G28. Reconfigurable, Next-Generation Network Monitoring (PI, co-PI: T. Wolf)
Funding source: Altera Corporation
9/1/09-12/31/11
Total amount: $25,000, My share: $12,500

G29. Low-Power High Bandwidth Receiver for Ka-Band Interferometry (co-PI, PI: P. Siqueira)
Funding source: NASA
3/1/09-2/28/12
Total amount: $1,088,000, My share: $200,000

G30. Network Virtualization Using Dynamic FPGA Reconfiguration (PI, co-PI: L. Gao)
Funding source: National Science Foundation
9/1/08-8/31/12
Total amount: $350,000, My share: $175,000

G31. CRI: CAD Tool and Compiler Repository for Reconfigurable Computing (sole-PI)
Funding source: National Science Foundation
8/1/07-7/31/11
Total amount: $157,500, My share: $157,500

G32. MNOC: A Network-on-Chip for Configurable Monitors (co-PI, PI: W. Burleson)
Funding source: Semiconductor Research Corporation
4/1/07-1/31/10
Total amount: $300,000, My share: $150,000

G33. X-Band IC Technologies for Low Cost Radars (co-PI, PI: R. Jackson)
Funding source: Raytheon Corporation
4/1/07-1/31/09
Total amount: $400,000, My share: $133,000

G34. FPGA-Based Image Processing Research (co-PI, PI: P. Kelly)
Funding source: Kollmorgen Corporation
1/1/07-1/01/08
Total amount: $77,000, My share: $38,000

G35. Scalable Parallel Processing Using Soft Multiprocessors
Funding source: Altera Corporation
8/1/06-12/31/07
Total amount: $25,000, My share: $25,000

G36. Power Consumption Comparison for FPGAs and Microprocessors (sole-PI)
Funding source: ST Microelectronics
8/1/04-12/31/06
Total amount: $13,000, My share: $13,000

G37. Power-Aware Logic Synthesis and Tech. Mapping for LUT-based FPGAs (sole-PI)
Funding source: Altera Corporation
1/1/04-12/31/05

Total amount: $35,000, My share: $35,000

G38. CASA Engineering Research Center (Investigator, PI: D. McLaughlin)
Funding source: National Science Foundation
10/1/03-12/31/06
Total amount: $16,000,000, My share: $200,000

G39. Reconfigurable Implementation of Software Radios (sole-PI)
Funding source: M/A-COM Corporation
1/1/03-12/31/03
Total amount: $36,000, My share: $36,000

G40. Architectures and Technology Mapping Issues for Hybrid FPGAs (sole-PI)
Funding Source: Xilinx Corporation
6/01/01-8/31/02
Total amount: $13,200, My share: $13,200

G41. Integration of JBits and VPR (sole-PI)
Funding Source: Xilinx Corporation
6/01/01-8/31/02
Total amount: $10,000, My share: $10,000

G42. Acquisition of Sensing Data on a Reconfigurable Platform (PI, co-PI: D. McLaughlin)
Funding source: Air Force Research Laboratory
12/1/00-6/31/02
Total amount: $69,936, My share: $69,936

G43. Reconfigurable, Time-aware Smartcard Technology (co-PI, PI: S. Desu)
Funding source: Sharp Corporation
12/1/00-11/31/02
Total amount: $200,000, My share: $100,000

G44. ITR/ACS: Adaptive Fault Recovery for Networked Digital Systems (sole-PI)
Funding Source: National Science Foundation
9/01/00-8/31/03
Total amount: $185,000, My share: $185,000

G45. Low-power Adaptive Systems on a Chip (co-PI, PI: W. Burleson)
Funding source: National Science Foundation
7/1/00-6/31/03
Total amount: $300,588, My share: $150,296

G46. Integration of SystemC with a VirtuaLogic Emulation System (sole-PI)
Funding source: Ikos Systems, Inc.
6/1/00-5/31/01
Total amount: $11,771, My share: $11,771

G47. Reconfigurable Computing with Tiled Architectures (sole-PI)
Funding source: UMass Healey Endowment Grant
5/1/99-5/31/00
Total amount: $9,000, My share: $9,000

PUBLICATIONS

Patents

P1. Russell Tessier, Vaughn Betz, Thiagaraja Golpalsamy, and David Neto, "Power-Aware RAM Processing." U.S. patent 9330733, May 3, 2016.

P2. Russell Tessier, Vaughn Betz, Thiagaraja Golpalsamy, and David Neto, "Power-Aware RAM Processing." U.S. patent 7877555, January 25, 2011.

P3. Anant Agarwal, Jonathan Babb, and Russell Tessier, "Virtual Interconnection for Reconfigurable Logic Systems." U.S. patent 5761484, June 2, 1998.

P4. Anant Agarwal, Jonathan Babb, and Russell Tessier, "Virtual Interconnection for Reconfigurable Logic Systems." U.S. patent 5596742, January 21, 1997.

Books

B1. Jakub Szefer and Russell Tessier, editors, Security of FPGA-Accelerated Cloud Computing Environments, Springer Nature, Berlin, Germany, 2023.

Book Chapters

B2. Shayan Moini[1], George Provelengios, Daniel Holcomb, and Russell Tessier "Active Countermeasures against Voltage Attacks in Multi-Tenant FPGAs", in Security of FPGA-Accelerated Cloud Computing Environments, Jakub Szefer and Russell Tessier, ed., Springer Nature, 2023.

B3. Russell Tessier, Tilman Wolf, Kekai Hu, and Harikrishnan Chandrikakutty, "Reconfigurable Network Router Security", in Reconfigurable Logic: Architecture, Tools and Applications, Pierre Gaillardon, ed., CRC Press, 2015.

B4. Russell Tessier, "Multi-FPGA Systems: Logic Emulation", in Reconfigurable Computing, Scott Hauck and André DeHon, eds., Morgan Kaufmann, pp. 637-670, 2008.

B5. Russell Tessier and Wayne Burleson, "Reconfigurable Computing and Digital Signal Processing: Past, Present, and Future", in Programmable Digital Signal Processors, Yu Wen Hu, ed., Marcel Dekker, pp. 147-186, 2002.

Journal Publications

J1. Nils Albartus, Maik Ender, Jan-Niklas Moller, Mark Fyrbiak, Christof Paar, and Russell Tessier, "On the Malicious Potential of Xilinx' Internal Configuration Access Port (ICAP)", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 17, no. 2, pp. 1-28, April 2024.

J2. Mirjana Stojilovic, Kasper Rasmussen, Francesco Regazzoni, Mehdi Tahoori, and Russell Tessier, "A Visionary Look at the Security of Reconfigurable Cloud Computing", *Proceedings of the IEEE*, vol. 111, no. 12, pp. 1548-1571, December 2023.

J3. Shayan Moini, Aleksa Deric, Xiang Li, George Provelengios, Wayne Burleson, Russell Tessier, and Daniel Holcomb, "Voltage Sensor Implementations for Remote Power Attacks on FPGAs", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 16, no. 1, pp. 11.1-11.21, March 2023.

[1]The names of Prof. Tessier's students are underlined

J4. Xiang Li, Peter Stanwicks, George Provelengios, Russell Tessier, and Daniel Holcomb, "Jitter-based Adaptive True Random Number Generation Circuits for FPGAs in the Cloud", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 16, no. 1, pp. 3.1-3.20, March 2023.

J5. Christophe Bobda, Joel Mandebi Mbongue, Paul Chow, Mohammad Ewais, Naif Tarafdar, Juan Camilo Vega, Ken Eguro, Dirk Koch, Suranga Handagala, Miriam Leeser, Martin Herbordt, Hafsah Shahzad, Peter Hofste, Burkhard Ringlein, Jakub Szefer, Ahmed Sanaullah, and Russell Tessier, "The Future of FPGA Acceleration in Datacenters and the Cloud", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 15, no. 3, pp. 1-42, September 2022.

J6. Florian Stoltz, Nils Albartus, Julian Speith, Simon Klix, Clemens Nasenberg, Aiden Gula, Marc Fyrbiak, Christof Paar, Tim Güneysu, and Russell Tessier "LifeLine for FPGA Protection: Obfuscated Cryptography for Real-World Security", *IACR Transactions on Cryptographic Hardware and Embedded Systems*, vol. 2021, no. 4, pp. 412-446, September 2021.

J7. George Provelengios, Daniel E. Holcomb, and Russell Tessier, "Mitigating Voltage Attacks in Multi-Tenant FPGAs", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 14, no. 2, pp. 1-24, August 2021.

J8. Shayan Moini, Shanquan Tian, Daniel Holcomb, Jakub Szefer and Russell Tessier, "Power Side-Channel Attacks on BNN Accelerators in Remote FPGAs", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 11, no. 2, pp. 357-370, June 2021.

J9. George Provelengios, Daniel E. Holcomb, and Russell Tessier, "Power Distribution Attacks in Multi-Tenant FPGAs", *IEEE Transactions on VLSI Systems*, vol. 28, no. 12, pp. 2685-2698, December 2020.

J10. Xuzhi Zhang, Xiaozhe Shao, George Provelengios, Naveen Kumar Dumpala, Lixin Gao, and Russell Tessier, "CoNFV: A Heterogeneous Platform for Scalable Network Function Virtualization", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 14, no. 1, pp. 1-29, November 2020.

J11. Marc Fyrbiak, Sebastian Wallat, Pawel Swierczynski, Max Hoffmann, Sebastian Hoppach, Matthias Wilhelm, Tobias Weidlich, Russell Tessier, and Christof Paar, "HAL - The Missing Piece of the Puzzle for Hardware Reverse Engineering, Trojan Detection and Insertion", *IEEE Transactions on Dependable and Secure Computing*, vol. 16, no. 3, pp. 498-510, May/June 2019.

J12. Mohammad A. Usmani, Shahrzad Keshavarz, Eric Matthews, Lesley Shannon, Russell Tessier, and Daniel E. Holcomb, "Efficient PUF-Based Key Generation in FPGAs Using Per-Device Configuration", *IEEE Transactions on VLSI Systems*, vol. 27, no. 2, pp. 364-375, February 2019.

J13. Naveen Kumar Dumpala, Shivukumar B. Patil, Daniel Holcomb, and Russell Tessier, "Loop Unrolling for Energy Efficiency in Low-Cost Field-Programmable Gate Arrays", *ACM Transactions on Reconfigurable Technology and Systems*, vol. 11, no. 4, pp. 26:1-26:3, January 2019.

J14. Marc Fyrbiak, Sebastian Wallat, Jonathan Dechelotte, Nils Albartus, Sinan Bocker, Russell Tessier, and Christof Paar, "On the Difficulty of FSM-based Hardware Obfuscation", *IACR Transactions on Cryptographic Hardware and Embedded Systems*, vol. 2018, no. 3, pp. 293-330, September 2018.

J15. Marc Fyrbiak, Simon Rokicki, Nicolai Bissantz, Russell Tessier, and Christof Paar, "Hybrid Obfuscation to Protect against Disclosure Attacks on Embedded Microprocessors", *IEEE Transactions on Computers*, vol. 67, no. 3, pages 307-321, March 2018.

J16. Vincent Migliore, Cédric Seguin, Maria Méndez Real, Vianney LaPotre, Arnaud Tisserand, Caroline Fontaine, Guy Gogniat, and Russell Tessier, "Hybrid Obfuscation to Protect against Disclosure Attacks on Embedded Microprocessors", *ACM Transactions on Embedded Computer Systems*, vol. 16, no. 5, pages 138:1-138:17, October 2017.

J17. Kekai Hu, Harikrishnan Chandrikakutty, Zachary Goodman[2], Russell Tessier, and Tilman Wolf,

[2]Undergraduate researcher

"Dynamic Hardware Monitors for Network Processor Protection", *IEEE Transactions on Computers*, vol. 65, no. 3, pages 860-872, March 2016.

J18. Tilman Wolf, Harikrishnan Chandrikakutty, Kekai Hu, Deepak Unnikrishnan, and Russell Tessier, "Securing Network Processors with High-Performance Hardware Monitors", *IEEE Transactions on Dependable and Secure Computing*, vol. 12, no. 6, pages 652-664, December 2015.

J19. Russell Tessier, Kenneth Pocek, and André DeHon, "Reconfigurable Computing Architectures", *Proceedings of the IEEE*, vol. 103, no. 3, pages 332-354, March 2015.

J20. Shiting (Justin) Lu, Russell Tessier, and Wayne Burleson, "Dynamic On-Chip Thermal Sensor Calibration Using Performance Counters", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 6, pages 853-866, June 2014.

J21. Deepak Unnikrishnan, Ramakrishna Vadlamani, Yong Liao, Jérémie Crenne, Lixin Gao and Russell Tessier, "Reconfigurable Data Planes for Scalable Network Virtualization", *IEEE Transactions on Computers*, vol. 62, no. 12, pages 2476-2488, December 2013.

J22. Shiting (Justin) Lu, Paul Siqueira, Vishwas Vijayendra, Harikrishnan Chandrikakutty, and Russell Tessier, "Real-Time Differential Signal Phase Estimation for Space-based Systems Using FPGAs", in *IEEE Transactions on Aerospace and Electronic Systems*, vol. 49, no. 2, pages 1192-1209, April 2013.

J23. Jérémie Crenne, Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Russell Tessier, and Deepak Unnikrishnan, "Configurable Memory Security in Embedded Systems", in *ACM Transactions on Embedded Computer Systems*, vol. 12, no. 3, pages 1-25, March 2013.

J24. Jia Zhao, Sailaja Madduri, Ramakrishna Vadlamani, Wayne Burleson, and Russell Tessier, "A Dedicated Monitoring Infrastructure for Multicore Processors", in *IEEE Transactions on VLSI Systems*, vol. 19, no. 6, pp. 1011-1022, June 2011.

J25. Tilman Wolf, Russell Tessier, and Gayatri Prabhu, "Securing the Data Path of Next-Generation Router Systems, in Computer Communications", in *Computer Communications*, vol. 31, no. 4, pp. 598-606, April 2011.

J26. Dong Yin, Deepak Unnikrishnan, Yong Liao, Lixin Gao, and Russell Tessier, "Customizing Virtual Networks with Partial FPGA Reconfiguration", in *ACM Computer Communication Review*, vol. 41, no. 1, pp. 125-132, January 2011.

J27. Weifeng Xu and Russell Tessier, "Tetris-XL: A Performance-Driven Spill Technique for Embedded VLIW Processors", in *ACM Transactions on Architecture and Code Optimization*, vol. 6, no. 3, pp. 1-40, September 2009.

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Conference Publications (< 40% accept rate)

C1. Dennis Gnad, Martin Gotthard, Jonas Krautter, Angeliki Kritikakou, Vincent Meyers, Paolo Rech, Josie E. Rodriguez Condia, Annachiara Ruospo, Ernesto Sanchez, Fernando Fernandes dos Santos, Olivier Sentieys, Mehdi Tahoori, Russell Tessier, and Marcello Traiola, "Reliability and Security of

AI Hardware", in *Proceedings: European Test Symposium*, The Hague, Netherlands, May 2024.

C2. Shayan Moini, Dhruv Kansagara, Daniel Holcomb, and Russell Tessier, "Fault Recovery from Multi-Tenant FPGA Voltage Attacks", in *Proceedings: ACM Great Lakes Symposium on VLSI*, Knoxville, TN, pp. 557-562, June 2023. (accept rate: 24%)

C3. Shanquan Tian, Shayan Moini, Daniel Holcomb, Russell Tessier, and Jakub Szefer, "A Practical Remote Power Attack on Machine Learning Accelerators in Cloud FPGAs", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Antwerp, Belgium, pp. 1-6, April 2023. (accept rate: 25%)

C4. Xiang Li, Russell Tessier, and Daniel Holcomb, "Precise Fault Injection to Enable DFIA for Attacking AES in Remote FPGAs", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, New York, NY, pp. 1-5, May 2022. (accept rate: 21%),

C5. Nils Albartus, Clemens Nasenberg, Florian Stoltz, Christof Paar, and Russell Tessier, "On the Design and Misuse of Microcoded (Embedded) Processors - A Cautionary Note", in *Proceedings: 30th Usenix Security Symposium*, virtual conference, pp. 267-284, August 2021. (accept rate: 19%)

C6. Shanquan Tian, Shayan Moini, Adam Wolnikowski, Daniel Holcomb, Russell Tessier, and Jakub Szefer, "Remote Power Attacks on the Versatile Tensor Accelerator in Multi-Tenant FPGAs", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, virtual conference, pp. 242-246, May 2021. (accept rate: 23%), **Best Paper Finalist**

C7. Shayan Moini, Shanquan Tian, Daniel Holcomb, Jakub Szefer, and Russell Tessier, "Remote Power Side-Channel Attacks on BNN Accelerators in FPGAs", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, virtual conference, pp. 1639-1644, February 2021. (accept rate: 24%)

C8. Xiang Li, Peter Stanwicks, George Provelengios, Russell Tessier, and Daniel Holcomb, "Jitter-based Adaptive True Random Number Generation for FPGAs in the Cloud", in *Proceedings: International Conference on Field-Programmable Technology*, virtual conference, pp. 112-119, December 2020. (accept rate: 25%), **Best Paper Finalist**

C9. George Provelengios, Daniel Holcomb, and Russell Tessier, "Power Wasting Circuits for Cloud FPGA Attacks", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, virtual conference, pp. 231-235, September 2020. (accept rate: 33%)

C10. George Provelengios, Daniel Holcomb, and Russell Tessier, "Characterizing Power Distribution Attacks in Multi-User FPGA Environments", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, Barcelona, Spain, pp. 194-201, September 2019. (accept rate: 19%), **Stamatis Vassiliadis Best Paper Award**

C11. George Provelengios, Chethan Ramesh, Shivukumar B. Patil, Ken Eguro, Russell Tessier, and Daniel Holcomb, "Characterization of Long Wire Data Leakage in Deep Submicron FPGAs", in *Proceedings: ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, Seaside, CA, pp. 292-297, February 2019. (accept rate: 18%)

C12. Jonathan Déchelotte, Dominique Dallet, Jérémie Crenne, and Russell Tessier, "Lynq: A Lightweight Software Layer for Rapid SoC FPGA Prototyping", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, Dublin, Ireland, pp. 372-375, August 2018. (accept rate: 29%)

C13. George Provelengios, Arman Pouraghily, and Russell Tessier and Tilman Wolf, "A Hardware Monitor to Protect Linux System Calls", in *Proceedings: IEEE International Symposium on VLSI*, Hong Kong, China, pp. 551-556, July 2018. (accept rate: 30%)

C14. Chethan Ramesh, Shivukumar B. Patil, George Provelengios, Siva Nishok Dhanuskodi, Daniel

Holcomb, and Russell Tessier, "FPGA Side Channel Attacks without Physical Access", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Boulder, CO, May 2018. (accept rate: 21%)

C15. Shivukumar B. Patil, Tianqi Liu, and Russell Tessier, "A Bandwidth-Optimized Routing Algorithm for Hybrid FPGA Networks-on-Chip", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Boulder, CO, May 2018. (accept rate: 15%), **Best Paper Finalist**

C16. Xuzhi Zhang, Xiaozhe Shao, George Provelengios, Naveen Kumar Dumpala, Lixin Gao, and Russell Tessier, "Scalable Network Function Virtualization for Heterogeneous Middleboxes", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 219-226, May 2017. (accept rate: 24%)

C17. Naveen Kumar Dumpala, Shivukumar B. Patil, and Russell Tessier, "Energy Efficient Loop Unrolling for Low-Cost FPGAs", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 117-120, May 2017. (accept rate: 23%)

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C19. Christophe Huriaux, Olivier Sentieys, and Russell Tessier, "Effects of I/O Routing through Column Interfaces in Embedded FPGA Fabrics", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, Lausanne, Switzerland, pp. 1-9, September 2016. (accept rate: 21%)

C20. Tedy Thomas, Arman Pouraghily, Kekai Hu, Russell Tessier, and Tilman Wolf, "Multi-Task Support for Security-Enabled Embedded Processors", in *Proceedings: IEEE International Conference on Application-specific Systems, Architectures and Processors*, Toronto, ON, pp. 136-143, July 2015. (accept rate: 25%)

C21. Shiting (Justin) Lu, Russell Tessier, and Wayne Burleson, "Reinforcement Learning For Thermal-Aware Many-Core Task Allocation", in *Proceedings: ACM Great Lakes Symposium on VLSI*, Pittsburgh, PA, pp. 379-384, May 2015. (accept rate: 28%)

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C24. Christophe Huriaux, Olivier Sentieys and Russell Tessier, "FPGA Architecture Support for Heterogeneous, Relocatable Partial Bitstreams", in *Proceedings: International Conference on Field-Programmable Logic and Applications*, Munich, Germany, pp. 1-6, September 2014. (accept rate: 22%)

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237, December 2013. (accept rate: 21%)

C27. Deepak Unnikrishnan, Sandesh Gubbi Virupaksha, Lekshmi Krishnan, Lixin Gao and Russell Tessier, "Accelerating Iterative Algorithms with Asynchronous Accumulative Updates on FPGAs", in *Proceedings: International Conference on Field-Programmable Technology*, Kyoto, Japan, pp. 66-73, December 2013. (accept rate: 21%)

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C31. Jia Zhao, Shiting (Justin) Lu, Wayne Burleson, and Russell Tessier, "Run-time Probabilistic Detection of Miscalibrated Thermal Sensors in Many-core Systems", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Grenoble, France, pp. 1395-1398, March 2013. (accept rate: 36%)

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C33. Y. Sinan Hanay, Wei Li, Russell Tessier, and Tilman Wolf, "Saving Energy and Improving TCP Throughput with Rate Adaptation in Ethernet", in *Proceedings: IEEE Conference on Communications*, Ottawa, Ontario, pp. 1249-1254, June 2012. (accept rate: 37%)

C34. Jia Zhao, Russell Tessier, and Wayne Burleson "Distributed Sensor Data Processing for Many-cores," in *Proceedings: ACM Great Lakes Symposium on VLSI*, Salt Lake City, Utah, pp. 159-164, May 2012. (accept rate: 17%), **Best Paper Award**

C35. Deepak Unnikrishnan, Justin Lu, Lixin Gao, and Russell Tessier, "ReClick - A Modular Dataplane Design Framework for FPGA-Based Network Virtualization", in *Proceedings: ACM/IEEE Symposium on Architectures for Networking and Communications Systems*, Brooklyn, NY, pp. 145-155, October 2011. (accept rate: 32%)

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C38. Ramakrishna Vadlamani, Jia Zhao, Wayne Burleson, and Russell Tessier, "Multicore Soft Error Rate Stabilization Using Adaptive Dual Modular Redundancy", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Dresden, Germany, pp. 27-32, March 2010. (accept rate: 30%)

C39. Deepak Unnikrishnan, Ramakrishna Vadlamani, Yong Liao, Abhishek Dwaraki, Jeremie Crenne,

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C40. Tilman Wolf and Russell Tessier, "Design of a Secure Router System for Next-Generation Networks", in *Proceedings: IEEE International Conference on Network and System Security*, Gold Coast, Australia, pp. 52-59, October 2009. (accept rate: 26%)

C41. Kevin Andryc, Russell Tessier, and Patrick Kelly, "An Interactive Approach to Timing-Accurate PCI-X Simulation", in *Proceedings: IEEE/IFIP International Symposium on Rapid Systems Prototyping*, Paris, France, pp. 181-187, June 2009. (accept rate: 35%)

C42. Sailaja Madduri, Ramakrishna Vadlamani, Wayne Burleson and Russell Tessier "A Monitor Interconnect and Support Subsystem for Multicore Processors", in *Proceedings: IEEE/ACM Design Automation and Test in Europe Conference*, Nice, France, pp. 761-766, April 2009. (accept rate: 23%)

C43. Deepak Unnikrishnan, Jia Zhao, and Russell Tessier, "Application-Specific Customization and Scalability of Soft Multiprocessors", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, California, pp. 123-130, April 2009. (accept rate: 30%)

C44. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Russell Tessier, Deepak Unnikrishnan, and Kris Gaj, "Memory Security Management for Reconfigurable Embedded Systems", in *Proceedings: International Conference on Field-Programmable Technology*, Taipai, Taiwan, pp. 153-160, December 2008. (accept rate: 23%)

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C46. Kevin Oo Tinmaung, David Howland, and Russell Tessier, "Power-aware FPGA Logic Synthesis Using Binary Decision Diagrams", *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, CA, pp. 148-155, February 2007. (accept rate: 24%)

C47. Russell Tessier, Vaughn Betz, David Neto, and Thiagaraja Gopalsamy, "Power-aware RAM Mapping for FPGA Embedded Memory Blocks", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 189-198, February 2006. (accept rate: 22%)

C48. Lilian Atieno, Jonathan Allen, Dennis Goeckel, and Russell Tessier "An Adaptive Reed-Solomon Errors-and-Erasures Decoder", in *Proceedings: ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, Monterey, California, pp. 150-158, February 2006. (accept rate: 22%)

C49. Jian Liang, Russell Tessier, and Dennis Goeckel, "A Dynamically-Reconfigurable, Power-Efficient Turbo Decoder", in *Proceedings: IEEE International Symposium on Field-Programmable Custom Computing Machines*, Napa, CA, pp. 91-100, April 2004. (accept rate: 27%)

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C52. Aiyappan Natarajan, David Jasinski, Wayne Burleson, and Russell Tessier, "A Hybrid Adiabatic Content Addressable Memory for Ultra-Low Power Applications", in *Proceedings: IEEE/ACM*

Great Lakes Symposium on VLSI, Washington, D.C., pp. 72-75, April 2003. (accept rate: 26%)

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C54. Murali Kudlugi, Charles Selvidge, and Russell Tessier, "Static Scheduling of Multi-Domain Memories for Functional Verification", in *Proceedings: International Conference on Computer Aided Design*, pp. 2-9, San Jose, California, November 2001. (accept rate: 29%)

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C58. Ian Harris and Russell Tessier, "Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures," in *Proceedings: International Conference on Computer Aided Design*, San Jose, California, pp. 49-54, November 2000. (accept rate: 30%)

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C61. Vijay Lakamraju and Russell Tessier, "Tolerating Operational Faults in Cluster-based FPGAs," in *Proceedings: ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, California, pp. 187-194, February 2000. (accept rate: 35%)

C62. Matthew Dahl, Jonathan Babb, Russell Tessier, Silvina Hanono, David Hoki, and Anant Agarwal, "Emulation of a SPARC Microprocessor with the MIT Virtual Wires Emulation System," in *Proceedings: IEEE Workshop on FPGAs for Custom Computing Machines,* Napa, California, pp. 14-22, April 1994.

C63. Russell Tessier, Jonathan Babb, Matthew Dahl, Silvina Hanono, and Anant Agarwal, "The Virtual Wires Emulation System: A Gate-Efficient ASIC Prototyping Environment," in *Proceedings: 2nd ACM/SIGDA International Workshop on Field Programmable Gate Arrays,* Berkeley, California, February 1994.

C64. Jonathan Babb, Russell Tessier, and Anant Agarwal, "Virtual Wires: Overcoming Pin Limitations in FPGA-based Logic Emulators," in *Proceedings: IEEE Workshop on FPGAs for Custom Computing Machines,* Napa, California, pp. 142-151, April 1993.

Conference Publications ($\geq$ 40% accept rate)

C65. Mohamed El Bouazzati, Russell Tessier, Philippe Tanguy, and Guy Gogniat, "A Lightweight Intrusion Detection System against IoT Memory Corruption Attacks", in *Proceedings: International*

Symposium on Design and Diagnostics of Electronic Circuits and Systems, Tallinn, Estonia, pp. 118-123, May 2023, **Best Paper Award**

C66. Tilman Wolf, Russell Tessier, Yadi Eslami, Christopher Hollot, and Bryan Polivka, "Challenges and Successes in Synchronous Cohort-Based International Education", in *Proceedings: ASEE Annual Conference and Exhibition*, virtual conference, July 2021.

C67. Xuzhi Zhang and Russell Tessier, "Service Chaining for Heterogeneous Middleboxes", in *Proceedings: International Conference on Field-Programmable Technology*, virtual conference, pp. 263-267, December 2020. (accept rate: 42%)

C68. Xuzhi Zhang, Narendra Prabhu, and Russell Tessier, "NestedNet: A Container-based Prototyping Tool for Hierarchical Software Defined Networks", in *Proceedings: International Workshop on Rapid System Prototyping*, virtual conference, pp. 1-7, October 2020.

C69. Shayan Moini, Xiang Li, Peter Stanwicks, George Provelengios, Wayne Burleson, Russell Tessier, and Daniel Holcomb, "Understanding and Comparing the Capabilities of On-Chip Voltage Sensors against Remote Power Attacks on FPGAs", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, virtual conference, pp. 941-944, August 2020.

C70. Tilman Wolf, Christopher Hollot, Russell Tessier, Bryan Polivka, and Yadi Eslami, "Scalable Synchronous Cohort-based International Education", in *Proceedings: ASEE Annual Conference and Exhibition*, virtual conference, June 2020.

C71. Tilman Wolf, Christopher Hollot, Russell Tessier, Bryan Polivka, Chris Hoehn-Saric, Janet Kang, and Katherine Newman, "Synchronous Cohort-Based International Education", in *Proceedings: ASEE Annual Conference and Exhibition*, Tampa, FL, June 2019.

C72. Lijuan Xia, Ahmed Soltan, Xuzhi Zhang, Andrew Jackson, Russell Tessier, and Patrick Degenaar, "Closed-Loop Proportion-Derivative Control of Suppressing Seizures in a Neural Mass Model", in *Proceedings: IEEE International Conference on Circuits and Systems*, Sapporo, Japan, pp. 1-5, May 2019.

C73. Arman Pouraghily, Tilman Wolf, and Russell Tessier, "Hardware Support for Embedded Operating System Security", in *Proceedings: IEEE International Conference on Application-specific Systems, Architectures and Processors*, Seattle, WA, pp. 61-66, July 2017. (accept rate: 51%)

C74. Shrikant Vyas, Naveen Kumar Dumpala, Russell Tessier, and Daniel Holcomb, "Improving the Efficiency of PUF-Based Key Generation in FPGAs Using Variation-Aware Placement", in *Proceedings: 26th International Conference on Field Programmable Logic and Applications*, Lausanne, Switzerland, pp. 1-4, September 2016. (accept rate: 42%)

C75. Kevin Andryc, Tedy Thomas, and Russell Tessier, "Soft GPGPUs for Embedded FPGAs: An Architectural Evaluation", in *Proceedings: Second Workshop on Overlay Architectures for FPGAs*, Monterey, CA, pp. 1-6, February 2016.

C76. Xiaobin Liu, Tedy Thomas, Alan Boguslawski[3], and Russell Tessier, "Adaptive MRAM-Based CGRAs", in *Proceedings: 25th International Conference on Field Programmable Logic and Applications*, London, England, pages 1-4, September 2015. (accept rate: 41%)

C77. Jia Zhao, Shiting (Justin) Lu, Wayne Burleson, and Russell Tessier, "A Broadcast-Enabled Sensing System for Embedded Multi-core Processors", in *Proceedings: IEEE International Symposium on VLSI*, Tampa, FL, pp. 190-195, July 2014. (accept rate: 46%)

C78. Cory Gorman, Paul Siqueira, and Russell Tessier, "An Open-Source SATA Core for Virtex-4 FPGAs", in *Proceedings: International Conference on Field-Programmable Technology*, Kyoto, Japan, pp. 454-457, December 2013.

[3]Undergraduate researcher

C79. Jeŕeḿie Crenne, Patrice Cotret, Guy Gogniat, Russell Tessier, and Jean-Philippe Diguet, "Efficient Key-Dependent Message Authentication in Reconfigurable Hardware", in *Proceedings: International Conference on Field-Programmable Technology*, New Delhi, India, pp. 1-6, December 2011. (accept rate: 52%)

C80. Emmanuel Seguin, Russell Tessier, Eric Knapp, and Robert W. Jackson, "A Dynamically-Reconfigurable Phased Array Radar Processing System", in *Proceedings: 21st International Conference on Field Programmable Logic and Applications*, Chania, Greece, pp. 258-263, September 2011. (accept rate: 48%)

C81. Ben Bovée, Mohammad Nekoui, Hossein Pishro-Nik and Russell Tessier, "Evaluation of the Universal Geocast Scheme For VANETs" in *Proceedings: IEEE Vehicular Technology Conference*, San Francisco, CA, September 2011. (accept rate: 50%)

C82. Vishwas Vijayendra, Paul Siqueira, Harikrishnan Chandrikakutty, Akilesh Krishnamurthy, and R. Tessier, "Real-Time Estimates of Differential Signal Phase for Spaceborne Systems Using FPGAs", in *Proceedings: NASA/ESA Conference on Adaptive Hardware and Systems*, San Diego, CA, pp. 121-128, June 2011. (accept rate: 48%)

C83. David Howland and Russell Tessier, "RTL Dynamic Power Optimization for FPGAs", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, Nashville, TN, pp. 714-717, August 2008. (accept rate: 69%)

C84. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Eduardo Wanderley, Russell Tessier, and Wayne Burleson, "Low Latency Solution for Confidentiality and Integrity Checking in Embedded Systems with Off-Chip Memory", in *Proceedings: International Conference on Reconfigurable Communication-centric SoCs*, Montpellier, France, pp. 146-153, June 2007.

C85. Romain Vaslin, Guy Gogniat, Jean-Philippe Diguet, Wayne Burleson, and Russell Tessier, "High-Efficiency Protection Solution for Off-Chip Memory in Embedded Systems", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, pp. 117-123, June 2007.

C86. Rishi Khasgiwale, Luko Krnan, Atchuthan Perinkulam, and Russell Tessier "Reconfigurable Data Acquisition System for Weather Radar Applications", in *Proceedings: IEEE Midwest Symposium on Circuits and Systems*, Cincinnati, OH, pp. 822-825, August 2005.

C87. Dragana Perkovic, Stephen Frasier, Russell Tessier, Mark Sletten, and Jakov Toporkov, "An Airborne Pod-based Dual Beam Interferometer" in *Proceedings: IEEE Aerospace Conference*, Big Sky, MT, pp. 1193-1201, March 2005.

C88. Andrew Laffely, Jian Liang, Wayne Burleson, and Russell Tessier, "Adaptive System on a Chip: A Backbone for Power-Aware Signal Processing Cores", in *Proceedings: IEEE Conference on Signal Processing*, Barcelona, Spain, pp. 105-108, September 2003.

C89. Ramaswamy Ramaswamy and Russell Tessier, "The Integration of SystemC and Hardware-assisted Verification", in *Proceedings: 12th International Conference on Field-Programmable Logic and Applications*, Montpelier, France, pp. 1007-1016, September 2002. (accept rate: 48%)

C90. Atul Maheshwari, Russell Tessier, and Wayne Burleson, "Trading Off Reliability and Power Consumption in Ultra-Low Power Systems", in *Proceedings: International Symposium on Quality Electronic Design*, San Jose, California, pp. 361-366, March 2002. (accept rate: 60%)

C91. Andrew Laffely, Jian Liang, Prashant Jian, Ning Weng, Wayne Burleson, and Russell Tessier, "Adaptive Systems on a Chip (aSoC) for Low-Power Signal Processing", in *Proceedings: Asilomar Conference on Signals, Systems, and Computers*, Monterey, California, pp. 1217-1222, November 2001.

C92. Murali Kudlugi and Russell Tessier, "Multi-domain Communication for FPGA-based Logic Emu-

lation", in *Proceedings of the 10th International Workshop on Logic and Synthesis*, Lake Tahoe, Nevada, June 2001.

C93. Wayne Burleson, Russell Tessier, Dennis Goeckel, Sriram Swaminathan, and Prashant Jain, "Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations for Improved Performance and Reduced Power" in *Proceedings: International Conference on Acoustics, Speech, and Signal Processing*, vol. 2, pp. 901-904, Salt Lake City, Utah, May 2001. (accept rate: 51%)

C94. Srini Krishnamoorthy, Sriram Swaminathan, and Russell Tessier, "Area-Optimized Technology Mapping for Hybrid FPGAs," in *Proceedings: 10th International Conference on Field Programmable Logic and Applications*, Villach, Austria, pp. 181-190, August 2000.

C95. Russell Tessier and Heather Giza[4], "Balancing Logic Utilization and Area Efficiency in FPGAs," in *Proceedings: 10th International Conference on Field Programmable Logic and Applications*, Villach, Austria, pp. 535-544, August 2000.

C96. Russell Tessier, "Frontier: A Fast Placement System for FPGAs," in *Proceedings: Tenth IFIP International Conference on VLSI*, Lisbon, Portugal, pp. 125-136, December 1999.

C97. Russell Tessier, "Incremental Compilation for Logic Emulation," in *Proceedings: IEEE International Workshop on Rapid System Prototyping*, Clearwater, Florida, pp. 236-241, June 1999.

C98. Russell Tessier, "Negotiated A* Routing for FPGAs," in *Proceedings: 5th Canadian Workshop on Field-Programmable Devices*, Montreal, Quebec, pp. 14-19, June 1998.

C99. Steven Ward, Karim Abdalla, Rajeev Dujari, Michael Fetterman, Frank Honore, Ricardo Jenez, Phillipe Laffont, Ken Mackenzie, Chris Metcalf, Milan Minsky, John Nguyen, John Pezaris, Gill Pratt, and Russell Tessier. "The NuMesh: A Modular, Scalable Communications Substrate", in *Proceedings: International Conference on Supercomputing*, pp. 123-132, July 1993.

Unrefereed/Invited Publications

C100. Marc Closa Tarres, Paul Siqueira, James M. Adam, Eric Sutherland, Joseph Maloyan, Takuya Seaver, Russell Tessier, Leung Tsang, Firoh Borah, HP Marshall, Elias Deeb, and Gordon Farquharson "First Results from a Dual KU- and C-band Airborne SAR for Snowpack Measurement", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Athens, Greece, 4 pages, July 2024.

C101. Kenneth Pocek, Russell Tessier, and André DeHon, "Birth and Adolescence of Reconfigurable Computing: A Survey of the First 20 Years of Field-Programmable Custom Computing Machines", in *Highlights of the First Twenty Years of the IEEE International Symposium on Field-Programmable Custom Computing Machines*, Seattle, WA, pp. 3-19, May 2013.

C102. Eric Knapp, Jorge Salazar, Rafael Medina, Akilesh Krishnamurthy and Russell Tessier, "Phase-Tilt Radar Antenna Array", in *Proceedings: European Microwave Week Conference*, Manchester, UK, 4 pages, October 2011.

C103. Krzysztof Orzel, Vijay Venkatesh, Robert Palumbo, Rafael Medina, Akilesh Krishnamurthy, Jorge Salazar, Eric Knapp, David McLaughlin, Russell Tessier and Steven Frasier, "Mobile X-Band Dual Polarization Phased Array Radar: System Requirements and Development", in *Proceedings: AMS Conference on Radar Meteorology*, Pittsburgh, PA, 4 pages, September 2011.

C104. Michael Todd, Wayne Burleson, and Russell Tessier, "The Design and Assessment of a Secure Passive RFID Sensor System", in *Proceedings: IEEE New Circuits and Systems Conference*, Bordeaux, France, pp. 494-497, June 2011.

C105. Salma Mirza, J. Blair Perot, and Russell Tessier, "Reconfigurable Sparse Matrix-Vector Multi-

[4]Undergraduate researcher

plication on FPGAs", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, 6 pages, July 2010.

C106. Romain Vaslin, Guy Gogniat, Jean-Pierre Diguet, Edward Wanderly, Russell Tessier, and Wayne Burleson, "Low Latency Solution for Confidentiality and Integrity Checking in Embedded Systems with Off-Chip Memory", in *Proceedings: International Conference on Reconfigurable Communication-centric SoCs*, Montpelier, France, 4 pages, June 2007.

C107. Romain Vaslin, Guy Gogniat, Jean-Pierre Diguet, Wayne Burleson, and Russell Tessier, "High-Efficiency Protection Solution for Off-Chip Memory in Embedded Systems", in *Proceedings: International Conference on Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, 6 pages, June 2007.

C108. Francesc Junyent, et al., "Salient Features of Radar Nodes of the First Generation NetRad System", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Seoul, Korea, 3 pages, July 2005.

C109. William Junek, Arun Ramanathan, Gordon Farquharson, Steven Frasier, Russell Tessier, David McLaughlin, Mark Sletten, and Jakov Toporkov, "First Observations with the UMass Dual-Beam InSAR", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Toulouse, France, 3 pages, July 2003.

C110. Ramshankar Ramanarayanan, Russell Tessier, and Ian G. Harris, "Self-Test Recompilation to Support Fault Tolerance in VLIW Processors", in *Proceedings: International Test Synthesis Workshop*, Santa Barbara, CA, 2 pages, March 2002.

C111. Arun Ramanathan, Russell Tessier, David McLaughlin, James Carswell, and Steven Frasier, "Acquisition of Sensing Data on a Reconfigurable Platform", in *Proceedings: International Geoscience and Remote Sensing Symposium*, Sydney, Australia, 2 pages, July 2001.

INVITED PRESENTATIONS

Keynotes

T1. "Security Challenges and Solutions for Multi-Tenant FPGAs", Keynote address, *International Workshop on Security Proofs for Embedded Systems*, Leuven, Belgium, September 2022.

T2. "Next-Generation Networking Using FPGAs", Keynote address, *Conference on the Engineering of Reconfigurable Systems and Algorithms*, Las Vegas, NV, July 2010.

T3. "Power-reduction Techniques for ReCoSoc: Technologies and Trends", Keynote address, *International Conference on Reconfigurable Communication-centric SoCs*, Montpellier, France, June 2007.

Presentations

T4. "Security Challenges and Solutions for Multi-Tenant FPGAs", *University of Pennsylvania*, on-line, April 2024.

T5. "Security Challenges and Solutions for Multi-Tenant FPGAs", *Tortuga Logic*, on-line, July 2022.

T6. "Security Challenges and Solutions for Multi-Tenant FPGAs", *Information Sciences Institute*, on-line, March 2022.

T7. "Fault-Recovery for Multi-Tenant FPGAs", *Intel Side Channel Academic Program*, on-line, September 2021.

T8. "Security Challenges and Solutions for Multi-Tenant FPGAs", *Raytheon Information Systems and*

Computing Technology Network Symposium, on-line, May 2021.

T9. "Evaluating Stratix 10 FPGA Susceptibility to Voltage Attacks", *Intel Side Channel Academic Program*, on-line, September 2020.

T10. "Security Challenges and Solutions with Emerging Computing Technologies: Multi-Tenant FPGAs", *Semiconductor Research Corporation Security Workshop*, on-line, August 2020.

T11. "Security and Privacy Concerns for the FPGA-Accelerated Cloud and Datacenters", *The Future of FPGA-Acceleration in Cloud and Datacenters Workshop, IEEE International Symposium on Field-Programmable Custom Computing Machines*, on-line, May 2020.

T12. "Power Distribution Attacks in Multi-Tenant FPGAs", *Intel Corporation*, San Jose, CA, April 2020.

T13. "C-to-FPGAs: An Introduction to High-Level Synthesis for FPGAs", *MIT Haystack Observatory*, Westford, MA, June 2019.

T14. "Security for Multi-Tenant FPGAs", *HiPEAC Secure Hardware, Architectures, and Operating Systems Workshop*, Valencia, Spain, January 2019.

T15. "Scalable Network Function Virtualization for Heterogeneous Middleboxes", *MITRE Corporation*, Bedford, MA, August 2018.

T16. "Scalable Network Function Virtualization for Heterogeneous Middleboxes", *Yale University*, New Haven, CT, October 2017.

T17. "Scalable Network Function Virtualization for Heterogeneous Middleboxes", *Ruhr University*, Bochum, Germany, September 2017.

T18. "Hard Hybrid and Time-Division Multiplexed NoCs for FPGAs", *Xilinx Corporation*, San Jose, CA, February 2017.

T19. "Hardware-Assisted Code Obfuscation for FPGA Soft Microprocessors", *Ecole Polytechnique de Lausanne (EPFL)*, Lausanne, Switzerland, March 2015.

T20. "Network Security Using Reconfigurable Hardware Monitoring", *Winter School on Design Technologies for Heterogeneous Embedded Systems*, Ottawa, ON, January 2014.

T21. "On-chip Monitoring Infrastructures and Strategies for Many-core Systems", *Advanced Micro Devices*, Boxborough, MA, September 2013.

T22. "Scalable Network Virtualization Using FPGAs", *University of Wisconsin*, Madison, WI, November 2012.

T23. "Scalable Network Virtualization Using FPGAs", *Microsoft Research*, Redmond, WA, August 2012.

T24. "Logic Emulation", *Nanjing Forestry University*, Nanjing, China, May 2012.

T25. "Scalable Network Virtualization Using FPGAs", *University of Toronto*, Toronto, ON, June 2011.

T26. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *University of Arkansas*, Fayetteville, AR, November 2010.

T27. "Scalable Soft Multiprocessor Generation from a High-level Language", *University of Rennes*, Lannion, France, December 2009.

T28. "Scalable Soft Multiprocessor Generation from a High-level Language", *LIRMM*, Montpellier, France, July 2009.

T29. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *University of New Hampshire*, Durham, NH, March 2009.

T30. "Hardware Core for Off-chip Memory Security Management in Embedded Systems", *Boston Uni-*

versity, Boston, MA, November 2008.

T31. "Reconfigurable Computing: Research and Curriculum", *University of North Carolina, Charlotte*, Charlotte, NC, May 2008.

T32. "Reconfigurable Data Acquisition System for Weather Prediction", *University of Connecticut*, Storrs, CT, February 2008.

T33. "Power-Reduction Techniques for FPGAs: Technologies and Trends", *Worcester Polytechnic Institute*, Worcester, MA, December 2007.

T34. "A Dynamically-Reconfigurable, Power-Efficient Turbo Decoder", *Xilinx Corporation*, Edinburgh, UK, July 2007.

T35. "Reconfigurable Data Acquisition System for Weather Prediction", *Imperial College*, London, UK, June 2007.

T36. "A Power-aware BDD Decomposition Algorithm for FPGAs", *University of Toronto*, Toronto, ON, March 2005.

T37. "aSoC: A Single-Chip Communications Architecture", *Altera Corporation*, San Jose, CA, February 2004.

T38. "aSoC: A Single-Chip Communications Architecture", *University of British Columbia*, Vancouver, British Columbia, August 2003.

T39. "Will FPGAs Take Over Systems-on-a-Chip?", *Northeast Workshop on Circuits and Systems panel discussion*, Montreal, Quebec, June 2003.

T40. "aSoC: A Single-Chip Communications Architecture", *Carnegie Mellon University*, Pittsburgh, PA., March 2003.

T41. "Technology Mapping Algorithms for FPGAs with LUTs and PLAs", *Altera Corporation*, Toronto, Ontario, February 2003.

T42. "aSoC: A Single-Chip Communications Architecture", *California Institute of Technology*, Pasadena, CA., January 2003.

T43. "A Dynamically-Reconfigurable Adaptive Viterbi Decoder", *Queens University*, Belfast, No. Ireland, August 2002.

T44. "Static Scheduling of Multiple Asynchronous Clock Domains for Logic Verification" *Tufts University CAD Seminar,* Somerville, MA., November 2001.

T45. "Fast Place and Route Approaches for FPGAs." *Xilinx Corporation,* San Jose, CA, February 1999.

T46. "Fast Place and Route Approaches for FPGAs." *University of California, Berkeley CAD Seminar,* Berkeley, CA., February 1999.

T47. "Cut-based FPGA Floorplanning for Reconfigurable Computing." *University of Toronto FPGA Research Review,* Peterborough, Ontario, June 1997.

TEACHING EXPERIENCE

Undergraduate

- ENGIN112: Introduction to Electrical and Computer Engineering
- ECE122: Introduction to Programming for Electrical and Computer Engineering
- ECE232/331: Hardware Organization and Design

- ECE242: Data Structures
- ECE354: Computer Systems Laboratory II
- ECE415/416: Senior Design Project (course coordinator)
- 6.004: Computation Structures (MIT)

Graduate

- ECE510: Foundations of Computer Engineering
- ECE636: Reconfigurable Computing
- ECE669: Parallel Computer Architecture
- ECE688F/ECE688P: Graduate Project
- ECE697T: Teaching Seminar
- ECE1718F: Reconfigurable Computing (University of Toronto)

ADVISING

Ph.D. Degree Thesis Advisees

1. Shayan Moini, "Security of Hardware Acelerators in Multi-Tenant FPGA Environments", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2022. (Position: Qualcomm). *Co-advised with Wayne Burleson. 2023 Ting-wei Tang Dissertation Prize, UMass Department of Electrical and Computer Engineering.*
2. George Provelengios, "Addressing Security Challenges in Embedded Systems and Multi-Tenant FPGAs", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2021. (Position: Xilinx). *2021 Ting-wei Tang Dissertation Prize, UMass Department of Electrical and Computer Engineering.*
3. Xuzhi Zhang, "System Design and Implementation for Hybrid Network Function Virtualization", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2020. (Position: Apple)
4. Kevin Andryc, "An Architecture Evaluation and Implementation of a Soft GPGPU for FPGAs" Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2018. (Position: L3)
5. Shiting (Justin) Lu, "On Thermal Sensor Calibration and Software Techniques For Many-Core Thermal Management", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Google)
6. Kekai Hu, "Securing Network Processors with Hardware Monitors", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Intel)
7. Deepak Unnikrishnan, "Reconfigurable Technologies for Next Generation Internet and Cluster Computing", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2013. (Position: Altera)
8. Jia Zhao, "On-Chip Monitoring Infrastructures and Strategies for Multi-Core and Many-Core Systems", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2012. (Position: Qualcomm)
9. Weifeng Xu, "Software Based Permanent Fault Recovery Techniques Using Inherent Hardware Redundancy", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2007. (Position: Qualcomm)

10. Murali Kudlugi, "Static Scheduling of Multi Domain Circuits for Functional Verification", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2005. (Position: Mentor Graphics)

11. Jian Liang, "Development and Verification of a System-on-a-Chip Communication Architecture", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2004. (Position: Qualcomm)

12. Srini Krishnamoorthy, "Design Mapping Algorithms for Hybrid FPGAs Containing LUTs and PLAs", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2004. (Position: Advanced Micro Devices)

Masters Degree Thesis Advisees

1. Vaishanavi Avhad, "Development of a Salt Spreader Controller Program Using Machine-Sensed Roadway Weather Parameters", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2024. (Position: Lucid Motors)

2. Andrew Hartnett, "Integration of Digital Signal Processing Block in SymbiFlow FPGA Toolchain for Artix-7 Devices", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2022. (Position: Draper Laboratories)

3. Anurag Muttur, "Formally Verifiable Synthesis Flow in FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2022. (Position: Boeing)

4. Aiden Gula, "Internet Infrastructures for Large Scale Emulation with Efficent HW/SW Co-Design", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2021. (Position: Apple)

5. Narendra Prabhu, "Network Virtualization and Emulation Using Docker, Open vSwitch, and Mininet-based Link Emulation", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2020. (Position: Dell)

6. Chethan Ramesh, "Crosstalk-based Side Channel Attacks in FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2020. (co-advised with Daniel Holcomb) (Position: Apple)

7. Shivukumar B. Patil, "On-Chip Communication and Security in FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2018. (Position: Apple)

8. Naveen Kumar Dumpala, "Energy-Efficient Loop Unrolling for Low-Cost FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2017. (Position: Intel)

9. Shrikant Vyas, "Variation Aware Placement for Efficient Key Generation using Physically Unclonable Functions in Reconfigurable Systems", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2016. (Position: Altera)

10. Sandesh Virupaksha, "Accelerated Iterative Algorithms with Asynchronous Accumulative Updates on a Hetergeneous Cluster", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2016. (Position: Oracle)

11. Meha Kainth, "Development of Prototypes of a Portable Road Weather Information System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Altera)

12. Tedy Thomas, "Hardware Monitors for Secure Processing in Embedded Operating Systems", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2015. (Position: Cavium)

13. Xiaobin Liu, "Energy Efficiency Exploration of Coarse-Grain Reconfigurable Architecture with Emerging Non-Volatile Memory", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2015. (Position: Arecont Vision)

14. Cory Gorman, "Design of an Open-Source SATA Core for Virtex-4 FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2013. (Position: IBM)

15. Harikrishnan Chandrikakutty, "Protecting Network Processors with High Performance Logic Based Monitors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2013. (Position: Juniper Networks)

16. Murtaza Merchant, "Testing and Validation of a Prototype GPGPU Design for FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2013. (Position: Marvell Electronics)

17. Gayatri Prabhu, "Automated Detection and Counting of Pedestrians on an Urban Roadside", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2012. (Position: Xilinx Corporation)

18. Akilesh Krishnamurthy, "Design of an FPGA-based Array Formatter for CASA Phase-Tilt Radar System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2012. (Position: Marvell Electronics)

19. Vishwas Vijayendra, "Design and Testing of a Prototype High Speed Data Acquisition System for NASA", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, August 2011. (Position: Altera Corporation)

20. Benjamin Bovée, "Simulating a Universal Geocast Scheme for Vehicular Ad Hoc Networks", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2011. (Position: BTP Systems)

21. Emmanuel Seguin, "Low Cost FPGA Based Digital Beamforming Architecture for CASA Weather Radar Applications", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2010. (Position: MIT Lincoln Labs)

22. Salma Mirza, "Scalable, Memory-Intensive Scientific Computing on Field Programmable Gate Arrays", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2010. (Position: Netronome)

23. Ramakrishna Vadlamani, "Approaches to Multiprocessor Error Recovery Using an On-Chip Interconnect Subsystem", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2010. (Position: Qualcomm)

24. Deepak Unnikrishnan, "Application-Specific Customization and Scalability of Soft Multiprocessors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2009. (UMass Ph.D. student)

25. Sailaja Madduri, "MNoC: A Network-on-Chip for Monitors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2008, (Position: Intel)

26. Kevin Andryc, "A Novel Approach to PCI Simulation Using ScriptSim", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2008. (UMass Ph.D. student)

27. Jonathan Allen, "Energy Efficient Adaptive Reed-Solomon Decoding System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2008. (Position: EMC)

28. David Howland, "RTL Dynamic Power Optimization for FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2007, (Position: Pratt and Whitney)

29. Kevin Oo Tinmaung, "Power-aware FPGA Logic Synthesis Using Binary Decision Diagrams", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2006, (Position: Guardian Life)

30. Rishi Khasgiwale, "Reconfigurable Data Acquisition System for Weather Radar Applications", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005. (Position: Mentor Graphics)

31. Lilian Atieno, "Run-Time Dynamically Reconfigurable Reed-Solomon Decoder System", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005. (Position: Marvell Electronics)

32. Eric Keller, "Programming Model for Network Processing on FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2005. (Ph.D., Princeton, Assistant Professor, University of Colorado, Boulder)

33. David Jasinski, "An Energy-Aware Active Smart-Card Architecture", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2003. (Position: Naval Underwater Warfare Center)

34. Ramshankar Ramanarayanan, "Self-Test and Reconfiguration to Support Fault Tolerance in VLIW Processors", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2003. (Position: Advanced Micro Devices)

35. Arun Ramanathan, "Acquisition of Sensing Data on a Reconfigurable Platform", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2003. (Position: Broadcom)

36. Vibhor Garg, "A PCI-X Bus Transactor Model for SOC Verification Using Co-Modeling", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, February 2002. (Position: Cadence Design Systems)

37. Sriram Swaminathan, "An FPGA Based Adaptive Viterbi Decoder", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2001. (Position: Cilantro Technologies)

38. Ramaswamy Ramaswamy, "Integration of SystemC with an Ikos VirtuaLogic Emulator", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, September 2001. (Ph.D., UMass, Position: Cisco Systems)

39. Navin Vemuri, "BDD-based Logic Synthesis for LUT-Based FPGAs", Master's Thesis, Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, May 2001. (Position: Intel)

Ph.D. Committee Memberships

1. Jason Anderson, University of Toronto, Canada, ECE.
2. Paul Beckett, RMIT University, Australia, ECE.
3. Brandon Cahoon, University of Massachusetts, Computer Science.
4. Danai Chasaki, University of Massachusetts, ECE.
5. Scott Chin, University of British Columbia, Canada, ECE.

6. Jérémie Crenne, University of South Brittany, France, ECE.
7. Basab Datta, University of Massachusetts, ECE.
8. Jonathan Dechelotte, University of Bordeaux, France, ECE.
9. Siva Nishok Dhanuskodi, University of Massachusetts, ECE.
10. Hao Dong, University of Massachusetts, ECE.
11. Mohamed El Bouazzati, University of South Brittany, France, ECE.
12. Maik Ender, Ruhr University, Bochum, Germany, Electrical Engineering and Inf. Sciences.
13. Jeongseon Euh, University of Massachusetts, ECE.
14. Marc Fyrbiak, Ruhr University, Bochum, Germany, Electrical Engineering and Inf. Sciences.
15. Andres David Garcia Garcia, Ecole Nationale Superieure des Telecommunications, France, ECE.
16. Ilias Giechaskiel, Oxford University, England, UK, Computer Science.
17. Christophe Huriaux, University of Rennes I, France, ECE.
18. Semih Ince, University of Brittany, Occidentale, France, ECE.
19. Priyank Kalla, University of Massachusetts, ECE.
20. Samamon Khemmarat, University of Massachusetts, ECE.
21. Martin Labrecque, University of Toronto, Canada, ECE.
22. Andrew Laffely, University of Massachusetts, ECE.
23. Vijay Lakamraju, University of Massachusetts, ECE.
24. Guy Lemieux, University of Toronto, Canada, ECE.
25. Shuo Li, University of Massachusetts, ECE.
26. Cao Liang, Worcester Polytechnic Institute, ECE.
27. Valovan Manohararajah, University of Toronto, Canada, ECE.
28. Vincent Migliore, University of South Brittany, France, ECE.
29. Muhammad Asim Mukhtar, Information Technology University, Pakistan, EE.
30. Hossein Omidian, University of British Columbia, ECE.
31. Sohan Purohit, University of Massachusetts, Lowell, ECE.
32. Diego Puschini, University of Montpellier II, France, ECE.
33. Rance Rodrigues, University of Massachusetts, ECE.
34. Renaud Santoro, University of Rennes, France, ECE.
35. Deshanand Singh, University of Toronto, Canada, ECE.
36. Sharad Singhai, University of Massachusetts, Computer Science.
37. Pawel Swierczynski, Ruhr University, Bochum, Germany, Electrical Engineering and Inf. Sciences.
38. Romain Vaslin, University of South Brittany, France, ECE.
39. Edward Walters, University of Massachusetts, Computer Science.
40. David Whelihan, Carnegie Mellon University, ECE.
41. Sadegh Yazdanshenas, University of Toronto, Canada, ECE.

SERVICE

Diversity, Equity, and Inclusion

- Organized curriculum for the Digital Ready program on the Mt. Ida campus, 2021.
- Led a faculty mentoring workshop for the Graduate School at the University of Florida, 2021.
- Co-initiated College of Engineering Diversity, Equity, and Inclusion Award, 2020.
- Participated in faculty development panels, ADVANCE program, 2020
- Led faculty recruitment team, GEM Consortium National Conference, 2019.
- College of Engineering representative, Spaulding Smith Fellowship committee, 2018 - 2019.
- Recruiter, Northeast Alliance for Graduate Education and Professoriate, 2007 - 2011.
- Supervised theses of five graduate students from underrepresented groups, 2006 - 2016.

Editorships

- Co-Editor, special issue: ACM Transactions of Reconfiguration Technology and Systems, 2019.
- Co-Editor, book: Highlights of the First Twenty Years of the IEEE Symposium on FCCMs, 2013.
- Co-Editor, special issue: EURASIP Journal of Embedded Systems, 2006.
- Co-Editor, special issue: Journal of VLSI Signal Processing, 2004.

Technical Committees

- Program Committee, ANCS'2012.
- Program Committee, ARC'2004 - 2008.
- Program Committee, CHES'2022 - 2023.
- Program Committee, DATE'2021.
- Panel Chair, FCCM'2021.
- Co-General Chair, FCCM'2010.
- Co-Program Chair, FCCM'2009.
- Program Committee, FCCM'2007 - 2018, FCCM'2020 - 2024.
- Finance Chair, FPGA'2005.
- General Chair, FPGA'2004.
- Program Chair, FPGA'2003.
- Publicity Chair, FPGA'2001, FPGA'2002.
- Program Committee, FPGA'2000 - 2005, FPGA'2007 - 2023.
- Program Committee, FPL'2006 - 2007, FPL'2009 - 2022, FPL'2024
- Co-Program Chair, FPT'2011.
- Program Committee, FPT'2002 - 2024.
- Program Committee, HPEC'2012 - 2014, HPEC'2016 - 2017.
- Special Sessions Chair, ICCD'2011.
- Program Committee, SIPS'2012.
- Panelist, National Science Foundation, 2002, 2005, 2009, 2010, 2014, 2016, 2017, 2019-2021, 2023.
- Chair, IEEE Springfield Chapter, 2000 - 2003.

University Service

- Member, Provost's Teaching and Learning Working Group, 2020.
- Member, Faculty Senate Information and Communication Technology Council, 2017 - 2021, 2023 - 2024.
- Chair, ECE Faculty Search Committee, 2014.
- Chair, ECE Instructional Development Committee, 2007 - 2013.
- Advisor, Eta Kappa Nu Honor Society, 2003 - 2004, 2006 - 2008.
- Member, Faculty Senate University Computer & Electronic Communications Committee, 2006 - 2009.
- Member, Faculty Senate International Studies Committee, 2010 - 2013.