

High Performance Bridge Style Full Adder Structure

Omid Kavehei^a Said F.Al-Sarawi^a Derek Abbott^a and Keivan Navi^b

^aCenter for High Performance Integrated Technologies and Systems (CHiPTec)
The University of Adelaide, SA 5005, Australia.

^bMicro&Nano-electronic Research Center, Shahid Beheshti University, Tehran, Iran.

ABSTRACT

Adders are the core element in arithmetic circuits like subtracters, multipliers, and dividers. Optimization of adders can be achieved at device, circuit, architectural, and algorithmic levels. In this paper we present a new optimized full adder circuit structure that provides an improved performance compared to standard and mirror types adder structures. The performance of this adder in terms of power, delay, energy, and yield are investigated. This paper also proposes a novel simulation setup for full adder cells that is suitable for analyzing full adder cells at the high frequency. The simulation results of this structure will take into account the process variations for a 90 nm CMOS process and present results based on post-layout simulation using Cadence and Synopsys tools.

Keywords: Full Adder, Bridge Style Adders, Process Variation, Parametric Yield.

1. INTRODUCTION

Adders play an important role in many applications, such as digital signal processing, multi-operand addition systems, multipliers and many complex arithmetic circuits. Many studies have been done to reduce area, delay, power, and energy of adder cells.¹⁻⁵ Many of these studies have been investigated different topologies to implement the cells with focus on delay-power trade-off without considering process variation.^{1,2}

As technology is scaling down challenges faced by the designers become more complex. Variability, leakage power dissipation, and thermal aspects are some of the big challenges in nanometer circuits and systems design.^{6,7} Today, circuit designers have to consider not only the trade-off between delay and power, but also the impact of process and environmental variations on the delay-energy and parametric yield trade-off. Consequently, delay of circuits, dynamic and static power consumption, and frequency are no longer deterministic and must be modeled statistically. To summarize, some performance criteria are considered in the design and evaluation of adder cells, design scalability, area, wiring complexity, delay, power consumption, robustness with respect to voltage and transistor scaling as well as varying process.^{1,8} As a matter of fact, circuit robustness is becoming a key aspect in nanometer scale VLSI, where variation ranges of many process and environment parameters will increase dramatically.^{1,8,9} CMOS design is robust against voltage and transistor sizing, however, using lower supply voltages can have a large impact on performance.¹⁰ Thus, simulations have to be performed in the presence of random parameter variations. In this paper, we consider these key issues in the simulations. The paper is organized as follows: Background studies are briefly discussed in Section 2. The mirror CMOS full adder and bridge style full adder cells are discussed in Section 3. Section 4 describes and compares the full adders cells. The proposed simulation-setup and statistical analysis are also discussed in Section 4. Finally, Section 5 concludes this paper.

2. BACKGROUND STUDIES

A full adder can be implemented by direct implementation of the sum and carry functions using conventional⁸ or complex/bridge style⁴ mirror CMOS structure. The conventional mirror full adder has been used for many years as a basic 1-bit full adder cell in digital signal processing and other applications. It is also usually used as an accepted benchmark for evaluating research outcomes in the area of adder design.^{1,2,4,5} This structure has 28 transistors which could cause more energy consumption and chip area. On the other hand, the mirror adder has a symmetric interconnections pattern for

Further author information: (Send correspondence to Omid Kavehei)

Omid Kavehei: E-mail: omid@eleceng.adelaide.edu.au

Said Al-Sarawi: E-mail: alsarawi@eleceng.adelaide.edu.au

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pull-up and pull-down networks which provide an improvement in performance compared to the conventional structure. Both of the conventional and mirror full adder structures can be found in Ref. 8. However, there is no symmetry between implementation of carry and sum functions.

Preliminary investigation to implement a fully symmetric 1-bit full adder cell with respect to the advantage of mirror structure is done in Ref. 5. The proposed class of CMOS circuits, called “bridge”, has limited advantages in term of the transistor count and power consumption. Therefore, another type of bridge style full adder have been presented in Ref. 4, where a dense and symmetric structure are proposed. The main advantage of these novel structures is a significant reduction in the number of transistors (4 transistors reduction). At first glance, after layout implementation this could be found that one of the proposed full adders, called “full bridge”, makes a symmetry between carry and sum layout implementations, which means that there are the same pattern for interconnections between NMOS (PMOS) transistors in carry and sum functions. This symmetry is very important from the manufacturing process point of view.⁸

This paper investigates the parametric yield and energy-delay-voltage trade-off for the proposed full adder structures to mention the reliability of the adder cells in the presence of process variation. This paper also compares the area and input parasitic capacitances of the different full adder cells.

3. SYMMETRIC SUM AND CARRY FULL ADDER CELL

Different logic styles can be investigated from different points of view. In other words, it is different design constraints imposed by the application that each logic style has its place in the cell library development. Even a selected style appropriate for a specific function may not be suitable for another one. For example, static approach presents robustness against noise effects, thus automatically provides a reliable operation. The issue of ease of design is not always attained easily.¹ The CMOS design style is not area-efficient for complex gates with large fan-ins,¹ hence, care must be taken when a static logic style is selected to realize a logic function. Pseudo NMOS technique is straightforward, yet it compromises noise margin and suffers from static power dissipation. Pass transistor logic (PTL) style is known to be a popular method for implementing some specific circuits such as multiplexers and XOR-based circuits, like adders. Dynamic logic circuits realize the fast, small and complex gates, however, this advantage is gained at the cost of parasitic effects such as charge sharing, noise sensitivity and leakage power dissipation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability.^{1,4,8}

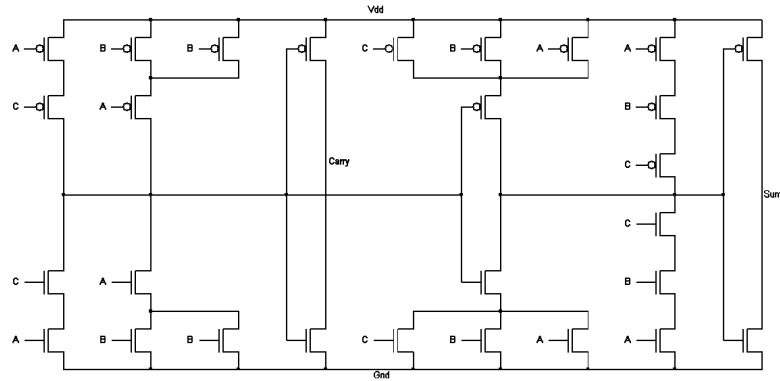
Fig. 1 shows the conventional (mirror) CMOS full adder with 28 transistors.⁸ This structure calls CFA (Conventional Full-Adder). Bridge style focuses on meshes, and connects each two adjacent mesh by a transistor, named *bridge transistor*. Bridge transistors provide the possibility of sharing transistors between two different paths to create a new path from supply rails to output. These transistors must be arranged in such a way that not only validate the correctness of the circuit, but also preserve pull-up and pull-down networks mutually exclusive.⁴ Sizing is an important issue for these transistors. More information about these transistors can be found in Ref. 5.

As mentioned above, the full bridge style adder cell has a fully symmetric structure. As shown in Fig. 2, topology of the carry and sum are exactly the same (there is only a different in inputs-transistors assignment). This full bridge style adder cell is named FB (Full Bridge). FB also provides a fully symmetric layout, as shown in Fig. 2.

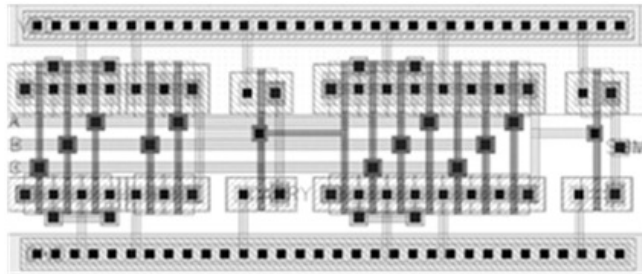
Replacing the carry part of FB with the carry section of CFA has also been demonstrated as another structure of full adders which is called HB (Half Bridge), for reducing the number of branches from supply voltage or ground rails to the output. The mentioned adder cell and its layout, are shown in Fig. 3.

Table 1 shows the clear improvement of the bridge schemes over the mirror cell in terms of transistor count, area and overall input parasitic capacitance. Reducing the overall parasitic capacitance at the inputs, affecting the total output nodes capacitance and the switching speed, especially in low voltage operations (Fig. 6). It is worth noting that the output capacitances in the three circuits are approximately the same. At first glance, these significant improvements clearly indicate great promise for better results in the post-layout simulation phase. The values in Table 1, were extracted from post-layout simulations for a 90 nm CMOS process.

The similarity in the design of full bridge, FB, full adder cell is very promising for introducing a standard cell library with a structure like (bridge) carry or (bridge) sum. With such library a 1-bit full adder is only implemented by using four gates (two inverters + two bridge gates). It is also interesting to extend the application of this structure to the field-programmable gate array (FPGA) area. The wide range of adder application in digital signal processing (DSP) and the mentioned possible potentials for standard cell design and FPGA shows the significance of the proposed cell.



(a) CFA Schematic



(b) CFA Layout

Figure 1. Conventional CMOS full-adder, CFA, schematic and layout

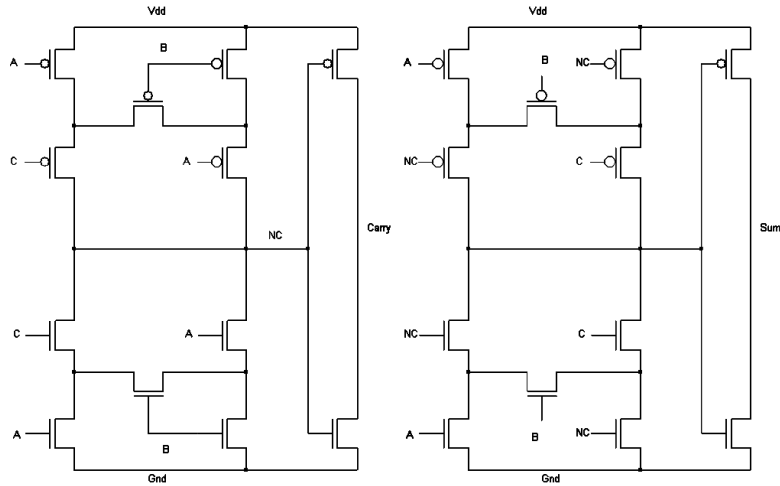
Table 1. Transistor count, Layout area, and Input parasitic capacitance comparisons, in a full-adder cell

Parameters	Cell Type		
	CFA	FB	HB
No. of Transistors	28	24 (14%)	24 (14%)
Layout area (μm^2)	38.30	36.32 (5%)	38.02
Input Parasitic capacitance (fF)	A	2.34	1.59 (32%)
	B	2.48	1.69 (32%)
	C	1.99	1.50 (25%)

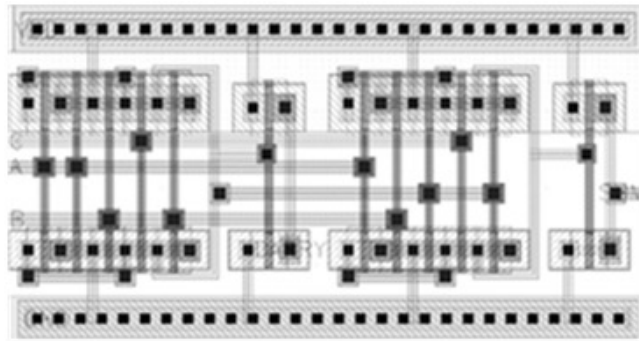
4. PERFORMANCE EVALUATION AND COMPARISON OF THE CIRCUITS

Recently, variability aware design has been gaining attraction in the field of IC design and become one of the main challenges for future CMOS design.¹¹ Process variations result from non-uniform conditions during the fabrication process. Variations in process parameters like the doping profiles, effective gate length, oxide thickness, and diffusion depths are different instances of the process variations. Variation in electrical parameters, such as threshold voltage and sheet resistance, have been caused by uncertainty in the manufacturing process. Generally, there are two types of process variations, inter-die (or die-to-die, D2D) and intra-die (or within-die, WID). The WID variations plays an increasingly important role in meeting the power and frequency constraints.^{12, 13} This paper investigates the impact of the global (D2D) variation on the three full adder cells.

It is well known that ring oscillator is used as a common test bench to analyze the impact of process variation. A ring oscillator comprises a chain of cascaded odd number of inverters. It is able to put the inverters at the highest possible frequency. Consequently, the power consumption of the inverters reaches its maximum level. Fig. 4 proposes a ring structure to simulate the full adder cells at maximum operating frequency, where En1 and En2 are control signals to switch between active and standby modes. A similar topology is briefly mentioned in Ref. 3. Using the two controlling signals, En1 and En2, and choosing the appropriate input vector for standby mode, the cells can be simulated in term of static power dissipation during its standby mode (in four possible input vectors - ABC: 000, 100, 011, 111). This can be achieved by implementing a combination of NAND and NOR circuits.



(a) FB Schematic



(b) FB Layout

Figure 2. Full Bridge, FB, CMOS full-Adder schematic and layout

The simulation results of these structures takes into account the process variations for a 90 nm CMOS process and present results based on post-layout simulation using Cadence and Synopsys tools.

This study also shows that the proposed adder cells are the most efficient in terms delay, power and energy in the presence of intra-die process variations. The technology specifications for the variation sources are collected in Table 2.¹⁴

Table 2. Technology specifications, where L_{INT} , W_{INT} , V_{TO} , and N_{DEP} are channel length offset, channel width offset, threshold voltage at zero bias, and doping concentration, respectively.

Parameters		μ (mean)	$3\sigma/\mu$ (%)
L_{INT} (nm)		7.50	20
W_{INT} (nm)		5.00	20
N_{DEP} ($10^{18}/\text{cm}^3$)	NMOS	2.02	15
	PMOS	1.53	20
V_{TO} (v)	NMOS	0.41	7
	PMOS	-0.36	8

Regarding to $3\sigma/\mu$ values for delay that will be reported later, the adder cells show 15% to 40% variations toward the means. Obviously, many different device parameters such as, the effective channel length and width, the surface potential and junction depth, the built-in voltage of the source/drain junctions and threshold voltage, will be varied with the variations of these parameters.

Fig. 5.a and 5.b shows μ_{delay} and σ_{delay} of the cells at different nominal V_{dd} (for 90 nm technology), respectively.

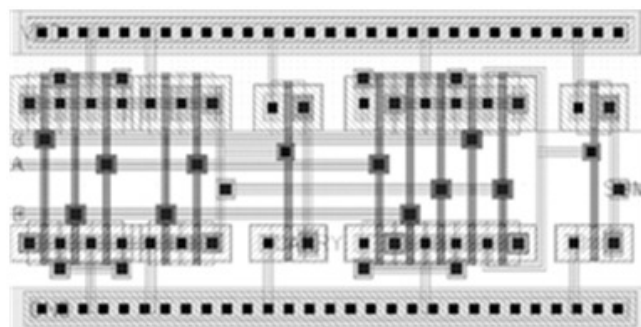
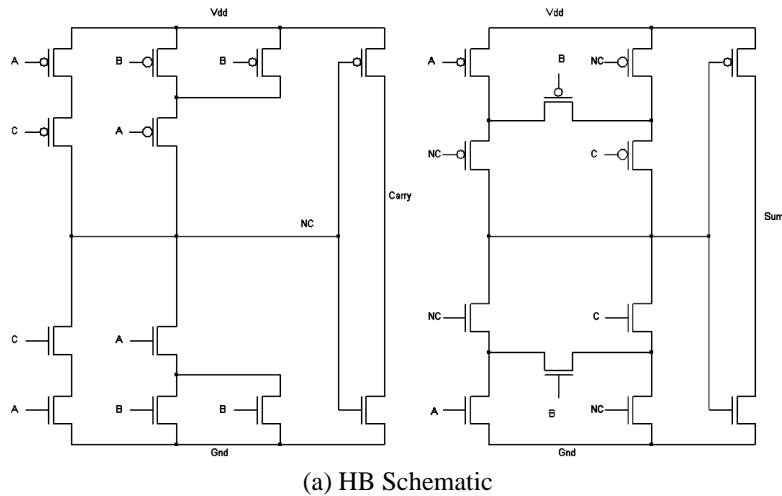
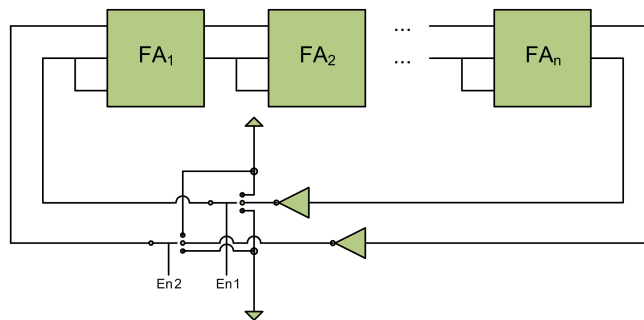


Figure 3. Half Bridge, HB, style CMOS full-adder, schematic and layout

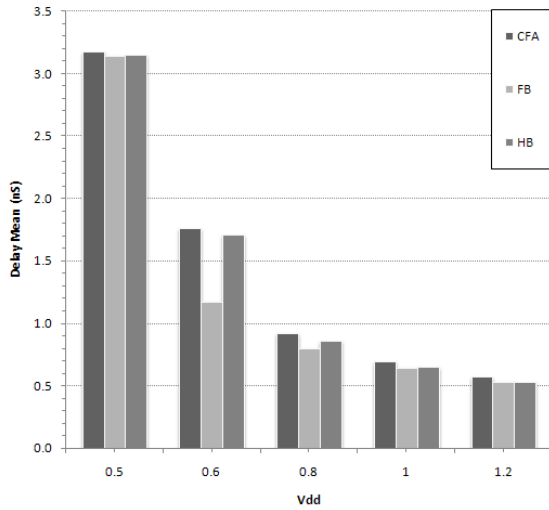


The results of this simulations are mentioned in Table 3.a, 3.b, and 3.c. Fig. 5 shows both μ_{delay} and σ_{delay} increase dramatically by the decreasing of the supply voltage.

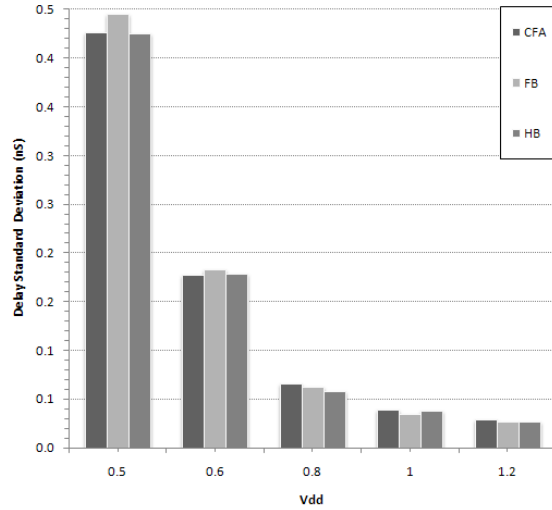
Fig. 5, and Table 3, show that bridge style cells reduce the mean value of delay. Between the two preferable candidates, FB also shows better performance than HB.

The average power dissipation in CMOS circuits is proportional to V_{dd}^2 , frequency, and output capacitance. Thus, an approach to reducing the power consumption of CMOS circuits is reduce the supply voltage. Note that, actually, switching power dissipation is proportional to $V_{\text{dd}} \times V_{\text{swing}}$. Here, V_{swing} , is output voltage swing and it is defined as the maximum peak voltage that the output can produce. In CMOS circuits it is equal to the supply voltage. Some design approaches, like pass-transistor logic (PTL) design, reduces the power consumption by using non-full-swing outputs.

As it is shown in Fig. 5, using low V_{dd} significantly increases both delay and delay variability, and hence, significant

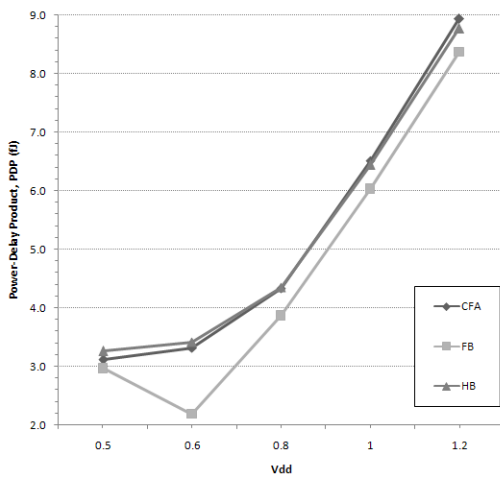


(a) Delay mean value, μ_{delay} vs V_{dd}

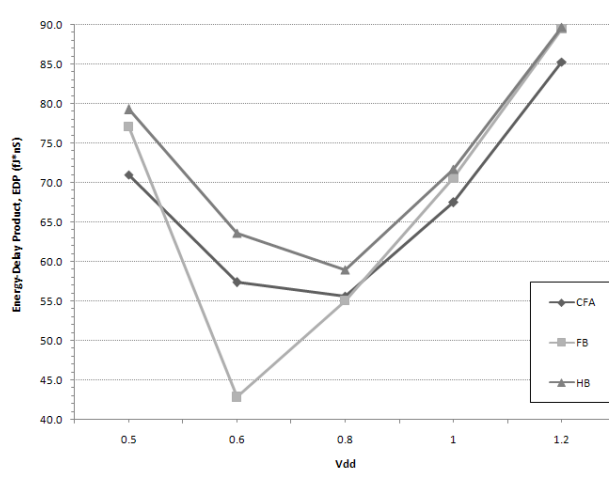


(b) Delay standard deviation, σ_{delay} vs V_{dd}

Figure 5. Delay mean, μ , and standard deviation, σ , for the full adder cells



(a) Power-Delay Product (PDP) vs V_{dd}



(b) Energy-Delay Product (EDP) vs V_{dd}

Figure 6. PDP and EDP of the cells

increase in terms of the overall performance yield loss; nevertheless, according to Ref. 15 and Ref. 16, voltage scaling is still susceptible to provide an improvement in power consumption with respect to the performance yield. In Ref. 17 the authors demonstrate that $V_{\text{dd}}/2$ is the best choice to satisfy both low-power and high-performance goals. Based on Ref. 17, if V_{dd} is scale down to $V_{\text{dd}}/2$, FB shows a considerable improvement in both power-delay product (PDP) and energy-delay product (EDP). These results are demonstrated in Fig. 6.a and 6.b.

As can be seen in Fig. 6.b, EDP of FB has been continued to vigorously decrease, after 0.8 volt to 0.6 volt, in contrary to the other cells. This means that, FB is a good candidate for a high-performance design with regard to the total power consumption.

Parametric yield loss is another important feature of the design. High-speed and low-power circuits design suffer from leakage, or static, power dissipation and low performance, respectively. As mentioned earlier, with advanced technologies, the circuit switching speed can be significantly increased at the cost of increased power dissipation. In other words, (dynamic) leakage power dissipation dominates the total power consumption in advanced technologies.⁷ Therefore, it can

Table 3. Mean (μ) and Standard deviation (σ) values for the adder cells in the presence of process variations, considering V_{dd} down-scaling

(a) CFA

V_{dd}		0.5	0.6	0.8	1.0	1.2
Delay (nS)	μ_D	3.178	1.765	0.917	0.696	0.571
	σ_D	0.426	0.177	0.066	0.039	0.030
Energy (fJ)	μ_E	22.32	32.50	60.63	96.95	149.3
	σ_E	1.117	1.492	2.281	3.033	5.504
Power (μ W)	μ_P	0.979	1.881	4.730	9.368	15.64
	σ_P	0.096	0.147	0.240	0.402	0.592
Yield (%)		73	80	87	92	93

(b) FB

V_{dd}		0.5	0.6	0.8	1.0	1.2
Delay (nS)	μ_D	3.147	1.170	0.800	0.646	0.531
	σ_D	0.445	0.183	0.063	0.034	0.027
Energy (fJ)	μ_E	24.49	36.57	68.80	109.2	168.6
	σ_E	1.350	1.707	2.866	3.625	6.083
Power (μ W)	μ_P	0.942	1.864	4.832	9.336	15.77
	σ_P	0.094	0.151	0.278	0.436	0.669
Yield (%)		72	78	85	94	95

(c) HB

V_{dd}		0.5	0.6	0.8	1.0	1.2
Delay (nS)	μ_D	3.151	1.711	0.864	0.652	0.533
	σ_D	0.425	0.179	0.058	0.037	0.027
Energy (fJ)	μ_E	25.15	37.15	68.16	110.0	168.1
	σ_E	1.353	1.587	2.521	3.407	5.935
Power (μ W)	μ_P	1.034	1.996	5.037	9.882	16.44
	σ_P	0.104	0.148	0.266	0.421	0.659
Yield (%)		76	77	87	92	93

be argued that a high-speed circuit should be a circuit with a huge amount of leakage currents, particularly in the nanometer circuits. On the contrary, in a low-power circuit, frequency constraint becomes a bottleneck in further reduction in power consumption. Power and frequency constraints are defined by coefficients of their nominal values. Parametric yield is also determined as the percentage of designs that satisfy the specified frequency and power constraints.⁷ These constraints can also be called *yield cut-offs*. Power constraint is the low yield cutoff and frequency constraint is the high yield cut-off.

Based on the preceding discussion, the parametric yield window has two-sided constraint. However, in this study, the leakage power dissipation effect on the parametric yield is neglected, so the yield window is defined as timing yield.¹⁴ Considering the impact of leakage power dissipation on the parametric yield could be investigate with a set of leakage reduction techniques as a future work. In this study we consider $0.9 \times f_{nom}$ as frequency constraint, where f_{nom} is the nominal frequency.⁷

Fig. 7 shows the timing/performance yield of the cells vs supply voltage. As shown in the figure, the curves are very close together on different supply voltages and this confirms the result of Ref. 14. Hence, EDP and PDP of the larger circuits will be significantly affected by using the proposed cells, without any significant degradation in the timing yield, but, it also seems possible that the parametric yield loss in that large circuits, like multipliers, would be significantly improved by using the cells.

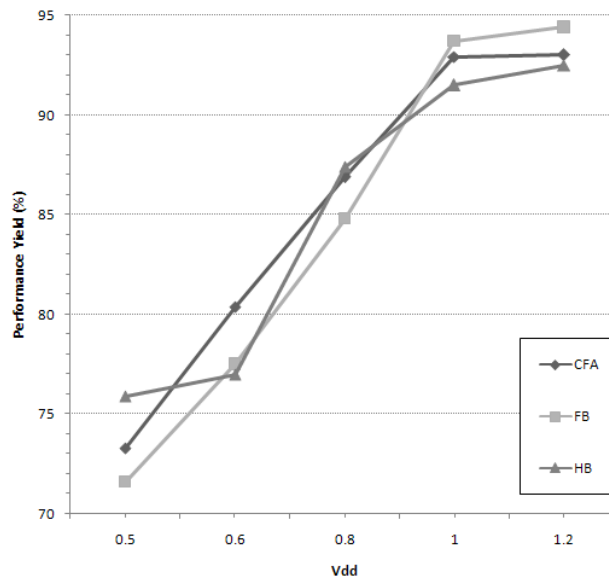


Figure 7. Performance Yield of the full adder cells vs V_{dd}

5. CONCLUSIONS AND FUTURE WORKS

This paper investigates the bridge style full adder cells in the presence of process variations. All of the cells have also been embedded in the novel simulation-setup to extract the results at a high operation frequency. The standard deviations (σ) and means (μ) of delay, power, and energy have been extracted based on a Monte-Carlo analysis. These results show that both of the energy-delay and power-delay products are significantly affected by using the full bridge style adder cell, without any considerable degradation in timing yield. Hence, energy saving in larger designs will be significantly improved with respect to the parametric yield loss. Considering, global and local variations, leakage power reduction techniques, and large circuits to investigate the It is also interesting to investigate the performance and parametric yield of such designs.

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