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MULTILAYER PRINTED WIRING BOARD INVESTIGATION

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ABSTRACT

Extensive testing of multilayer printed wiring boards obtained from six leading suppliers was conducted to provide data for reliability assessment of plated-through hole interconnections after soldering, soldering rework, vibration and temperature cycling. The program was undertaken to support the use of multilayer printed wiring boards for the Abort Electronics Assembly of the Lunar Excursion Module. A total of 9,370,000 joint-hours of temperature cycling and 7,877 joint-hours of vibration testing were completed. Additional tests and measurements such as insulation resistance after humidity, dielectric strength, thermal shock, hole location and registration were also made to ascertain the present level of multilayer printed wiring technology. It was concluded that requirements for multilayer circuit boards can be met with little difficulty if quality assurance measures are exercised.

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MULTILAYER PRINTED WIRING BOARD INVESTIGATION

INTRODUCTION

Present designs for spacecraft electronic assemblies requiring high reliability depend heavily on use of multilayer circuit boards for the mounting and circuit wiring of microminiature discrete component parts and integrated circuits. In support of electronic equipment designs for the Abort Guidance System of the Lunar Excursion Module, a test and evaluation program was undertaken (Ref 1) to provide data for use in reliability assessment of multilayer circuit boards.

The test program was divided into two phases. Phase I was a screening evaluation of two boards obtained from each of six suppliers. Based on Phase I performance, certain suppliers were selected for evaluation of ten additional boards in Phase II. Tests and procedures for the two portions of the program were the same. The only difference was the number of boards tested.

Fourteen companies were originally considered as potential suppliers for Phase I test boards. Based on informal and formal vendor surveys and a consideration of the program requirements, this list was reduced to the following six:

*1. Advanced Circuitry Division (Litton), Springfield, Mo.

2. Cinch-Graphik, City of Industry, California

3. Electralab Electronics Corporation, Encinitas, California

*4. Melpar, Inc., Falls Church, Virginia

5. National Technology, Inc., Santa Ana, California

*6. Photocircuits Corporation, Glen Cove, New York

Suppliers marked with an asterisk were subsequently chosen for Phase II testing.

All six suppliers were given formal vendor surveys except for National Technology which was setting up a new facility during the procurement cycle and appeared to be a promising source. Although Cinch-Graphik and Photocircuits failed to meet quality control requirements according to MIL-Q-9858A

and NPC 200-3 Phase II boards were procured from Photocircuits. However, this company has not complied to date and is not approved for LEM-AEA. Also, Photocircuits uses a pattern plating process exclusively which causes an increase in the outside pad diameter which, even if controlled by photographic procedures, would pose an undue hardship on design, drafting, and inspection. Phase II boards were not procured from Electralab because this company was already an approved source, and it was felt that confidence had been gained through past experience.

TEST OBJECTIVES

Objectives of the test program were to obtain data for assessment of:

1. Reliability of plated-through hole multilayer boards after soldering, soldering rework, vibration, and temperature cycling.

2. Variations in reliability among different suppliers.

3. Comparison of quality of multilayer circuit boards fabricated by leading suppliers.

TEST PLAN

1. Reliability

To obtain realistic failure rate information for high reliability electronic assemblies, it was assumed on the basis of experience and reports that failures are most likely to occur during soldering operations, soldering rework operations, vibration, or temperature cycling. To test the effect of these stresses on multilayer boards, the following conditions were established:

a. Soldering. In most present space electronic equipment designs utilizing multilayer circuit boards, the leads of integrated circuit flat packages are soldered into plated through holes with every hole filled with solder. For the test boards, the same procedure was followed except that six holes were left unsoldered for subsequent sectioning to determine plating thickness and appearance of the plated-through holes. For the soldering operation, the soldering iron, soldering tips, tip temperature, and soldering process were carefully controlled.

b. Soldering Rework. To simulate rework occurring on multilayer boards during actual assembly and repair of electronic equipment, 5% of the

leads in each test board were removed and resoldered three times. This amount of rework is equivalent to removing and resoldering ten integrated circuit flat packs on a multilayer board three times.

c. Vibration. The vibration input to give the same response on the multilayer board at resonance that would be experienced during a qualification sinusoidal vibration test was derived.

Each board was tested above this level for 30 minutes. The test boards without component parts and conformal coating had a high transmissibility (Q = 50); these units gave higher response levels than were obtained for assembled boards. The peak acceleration level on test boards at the natural frequency for the response level of 0.2 inch double amplitude was approximately 400 g. Continuity was monitored with an intermittency detector in the nanosecond range. Vibration tests followed the soldering and the soldering rework procedures.

d. Temperature Cycling. For the temperature cycling tests, the multilayer test boards were connected in series and electrical continuity was monitored with a current of 100 ma. The temperature was cycled between -55°C and +85°C with an hour at each temperature and an hour of transition time between temperatures. Temperature cycling followed soldering, soldering rework, and vibration testing.

2. Variations Among Suppliers

Although the processes for fabricating multilayer boards are generally the same throughout the industry, there are slight differences among suppliers that could affect reliability. Several of these differences are:

a. Cleaning Methods. Different methods of cleaning the holes after drilling and prior to plating-through are used by various manufacturers. Some suppliers use a chemical "etch back" process which dissolves the epoxy and glass cloth inside the hole. The etch removes epoxy from around the internal pads, permitting a more positive plated-through connection. It is necessary to balance the constituents in the chemical solution to effect the removal of epoxy and glass at the same rate, otherwise an irregularly plated hole results. A second method of cleaning holes is liquid honing. A third method in use is vapor blasting.

b. Nickel Plating. One multilayer manufacturer feels that nickel plating is necessary for the integrity of the plated-through hole interconnection and will not supply boards without nickel as an underplating. To observe any significant differences, particularly with regard to solder rework, test boards were procured with and without nickel.

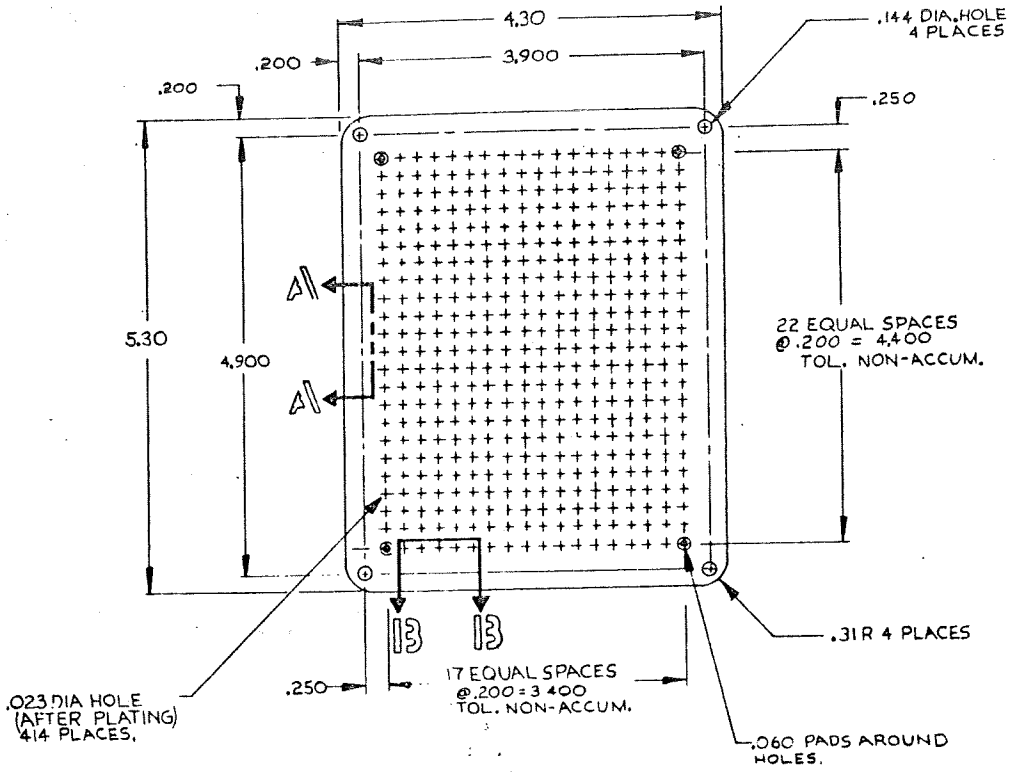
c. Pattern vs. Panel Plating. Test boards made by pattern plating, as well as panel plating, were procured and tested. Panel plated boards are made by plating the entire outside surfaces of the board with copper during the plated-through hole process. Pattern plated boards are made by plating the outside pads or circuitry only during the plated-through process. Evaluation of the differences between these two methods was scheduled as part of this investigation.

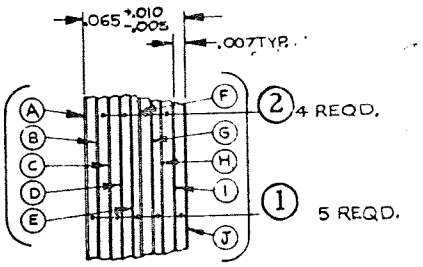
3. Quality Comparison

Achievement of quality in multilayer circuit board manufacture requires good process engineering and a high level of manufacturing skill. For the purpose of this evaluation, quality was determined through a comparison of physical measurements, physical appearance, and uniformity from one board to another. Typical physical measurements were: board thickness, hole diameter, hole location, layer registration, warp, and twist. Additional tests conducted to determine quality were: immersion in 500°F solder, insulation resistance after humidity conditioning, dielectric breakdown, and outgassing in vacuum.

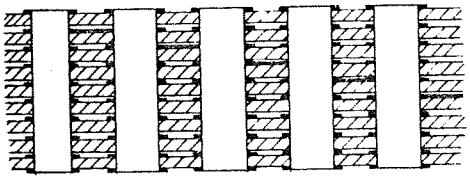
TEST SPECIMENS

The design used as the test board consisted of 414 plated through holes, 0.023 inch diameter and spaced on a 0.200 inch grid pattern (Figure 1). The holes were connected in series through eight internal layers except at the locations indicated in Figure 2 (A, B, C and D). These locations were left open to allow insulation resistance measurements between a conductor and a row of plated through holes with minimum spacing of 0.010 inch. During vibration and temperature cycling tests these holes were jumpered to permit the accumulation of a significant number of joint-hours during the test program.





SECTION A1 - A1



SECTION B3 - B3

KEY:

(1) Conductors, 0.007 to 0.0085 inch thick, double-sided one-ounce copper epoxy glass laminate (MIL-P-13949)

(2) Insulators, 0.006 inch thick, epoxy pre-preg

NOTE:

Holes copper plated to 0.0015 inch thick, nickel plated 0.0005 to 0.001 inch thick, and gold plated 50 to 100 x 10^{-6} inch thick.

Figure 1. Multilayer Circuit Board Test Specimen

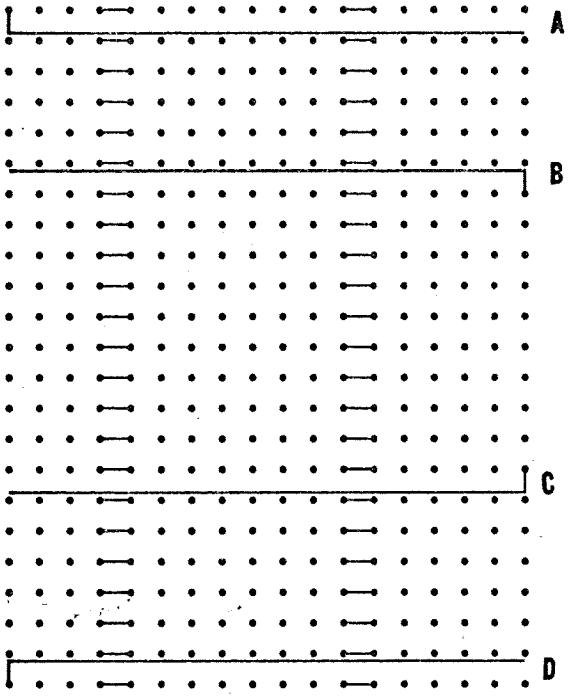


Figure 2. Circuit Layer for Insulation Resistance Measurements (4th Layer)

PHYSICAL AND ELECTRICAL EXAMINATION

A physical and electrical examination was made on every multilayer test board to obtain the pertinent information to evaluate supplier performance. The information is tabulated in Table I. The more difficult or destructive measurements such as layer registration, insulation resistance, and dielectric breakdown were not done on every board and must be taken as representative of the particular lot. A description of the physical appearance of the test boards as received is given in Table II. Table III is a tabulation of the number of boards from each supplier meeting the more important drawing and specification (PR7-8A) requirements.

1. Board Thickness

The requirement for board thickness tolerance was +0.010 and -0.005 inch. This tolerance should not be difficult in view of normal tolerances which are as follows:

Standard	$\pm$0.010
Special	$\pm$0.007
Premium	$\pm$0.005

The design allowed a considerable latitude in base material thickness which made up the multilayer composite. Measurements given in Table I are typical. Most boards varied 0.003 inch in thickness depending on where the measurement was made.

2. Pad Diameter (External)

As a general rule printed circuit suppliers will expand or reduce certain features of the artwork to take up etching or other manufacturing tolerances. The most common of these practices is to increase the pad size on the 1:1 artwork to allow for undercutting during etching. Suppliers, however, are limited in the extent of this "ballooning" by the minimum spacing allowed by the design and the limits of the photographic process.

If the artwork provided by the customer requires a reduction in pad size or line width to meet the minimum conductor spacing requirements, the artwork features are reduced. The minimum spacing is defined

TABLE I. PHYSICAL AND ELECTRICAL MEASUREMENTS OF TEST BOARDS COMPARED WITH SPECIFICATION (Sheet 1 of 2)

Supplier and Test Board Number	Board Thickness, Excluding Outer Pads	Board Thickness, Including Outer Pads	Pad Diameter	Hole Diameter	Hole Location	Minimum Pad Annulus	Layer Registration, Internal	Layer Registration, External	Warp or Twist
	0.060" to 0.075"	Not Specified	0.060"	0.023" ±.003	0.003" from true position	0.010"	0.005" from true position	Not Specified	2%
National Technology Inc.									
NT 1	0.069	0.071	0.065	0.029		0.009	0.005	0.007	0
NT 2	0.064	0.068	0.064	0.029		0.012	-	-	0
Photo-Circuits									
P 1	0.061	0.077	0.073	0.023			-	-	0
P 2	0.064	0.078	0.074	0.023			-	-	0
P 3	0.063	0.080	0.074	0.018			-	-	0
P 4	0.061	0.077	0.074	0.018			-	-	0.8%T
P 5	0.062	0.082	0.074	0.018	<0.003	0.021	-	-	0.2%T
P 6	0.063	0.078	0.074	0.018			-	-	0.3%T
P 7	0.063	0.077	0.074	0.018			-	-	0.8%T
P 8	0.062	0.077	0.074	0.018			-	-	0.3%T
P 9	0.063	0.083	0.074	0.018			-	-	0.3%T
P 10	0.065	0.082	0.074	0.018			-	-	0
P 11	0.063	0.082	0.074	0.018			-	-	0
P 12	0.064	0.081	0.074	0.018			-	-	0
Electra-lab									
E 1	0.062	0.071	0.056	0.026	<0.003	0.010	0.005	0.006	0
E 2	0.066	0.075	0.053	0.026	<0.003	0.015	-	-	0
Melpar									
M 1	0.087	0.092	0.062	0.026	<0.003	0.015	0.005	0.006	0
M 2	0.087	0.093	0.062	0.026	<0.003	0.015	-	-	0
M 3	0.063	0.074	0.067	0.025	<0.003	0.020	-	-	0.8%T
M 4	0.060	0.071	0.068	0.023	<0.003	0.020	-	-	0.8%T
M 5	0.065	0.076	0.065	0.023	<0.003	0.020	-	-	1.6%T
M 6	0.069	0.080	0.068	0.023	<0.003	0.020	-	-	0.8%T
M 7	0.067	0.078	0.067	0.023	<0.003	0.020	-	-	0.9%T
M 8	0.063	0.074	0.065	0.023	<0.003	0.020	0.007	0.006	0.4%T
M 9	0.062	0.073	0.066	0.023	<0.003	0.020	-	-	0.9%T
M 10	0.065	0.074	0.064	0.025	<0.003	0.020	-	-	0
M 11	0.065	0.075	0.064	0.025	<0.003	0.020	-	-	0.3%T
M 12	0.065	0.077	0.064	0.025	<0.003	0.020	-	-	0.8%T
Advanced Circuitry Division									
ACD 1	0.063	0.078	0.065	0.023	0.003	0.010	-	-	0
ACD 2	0.063	0.076	0.062	0.023	0.003	0.010	-	-	0
ACD 3	0.063	0.076	0.062	0.023	0.003	0.010	-	-	0
ACD 4	0.044	0.056	0.062	0.028	0.006	0.010	-	-	0
ACD 5	0.050	0.060	0.060	0.028	0.006	0.010	0.005	0.008	0
ACD 6	0.047	0.059	0.059	0.027	0.004	0.010	-	-	0
ACD 7	0.044	0.057	0.059	0.027	0.003	0.010	-	-	0
ACD 8	0.055	0.068	0.055	0.023	0.005	0.001	-	-	0
ACD 9	0.053	0.068	0.060	0.025	0.003	0.003	-	-	0.5%T
ACD 10	0.054	0.070	0.060	0.026	0.003	0.004	-	-	0.8%T
ACD 11	0.050	0.069	0.053	0.024	0.003	0.004	-	-	0
ACD 12	0.052	0.071	0.055	0.025	0.003	0.004	-	-	0
Cinch Graphik									
CG 1	0.060	0.066	0.057	0.026	0.003	0.010	-	-	0
CG 2	0.061	0.066	0.055	0.026	0.003	0.010	0.005	0.007	0

TABLE I. PHYSICAL AND ELECTRICAL MEASUREMENTS OF TEST BOARDS COMPARED WITH SPECIFICATION (Sheet 2 of 2)

Supplier and Test Board Number	Thermal Shock	Color	Continuity	Resistance, Ohms/ft	Insulation Resistance As Received, Ohms	Insulation Resistance After Humidity, Ohms	Dielectric Breakdown, Volts
	10 sec in 500°F Solder	Not Specified	100%	1 Ohm/ft	Not Specified	30×10^6 ohms	500 volts
National Technology Inc.							
NT 1	-					10^8	>2100
NT 2	-					10^8	-
Photo-Circuits							
P 1	Passed				10^{12}	10^8	>2400
P 2	-					-	-
P 3	-					-	-
P 4	-					-	-
P 5	-	Dark Brown	100%	0.3 ohm/ft		-	-
P 6	-					-	-
P 7	-					-	-
P 8	-					-	-
P 9	-					-	-
P 10	-					-	-
P 11	-					-	-
P 12	-					-	-
Electra-lab							
E 1	Passed	Lt. grn.			10^{11}	10^8	-
E 2	-	Lt. grn.			10^{11}	10^8	>3100
Melpar							
M 1	Passed	Grn.			10^{11}	10^9	>2300
M 2	-	Grn.			-	-	-
M 3	-	Grn.			-	-	-
M 4	-	Grn.			-	-	-
M 5	-	Lt. grn.	100%	0.3 ohm/ft	-	-	-
M 6	-	Lt. grn.			-	-	-
M 7	-	Lt. grn.			-	-	-
M 8	-	Lt. grn.			-	-	-
M 9	-	Lt. grn.			-	-	-
M 10	-	Lt. grn.			-	-	-
M 11	-	Lt. grn.			-	-	-
M 12	-	Lt. grn.			-	-	-
Advanced Circuitry Division							
ACD 1	-	Lt. grn.				-	>2100
ACD 2	-	Lt. grn.				-	-
ACD 3	-	Lt. grn.				-	-
ACD 4	-	Lt. grn.				-	-
ACD 5	-	Lt. grn.				10^9	-
ACD 6	-	Lt. grn.	100%	0.3 ohm/ft	10^{12}	-	-
ACD 7	-	Lt. grn.				-	-
ACD 8	-	Lt. grn.				-	-
ACD 9	-	Grn. brn.				-	-
ACD 10	Failed	Grn. brn.				-	-
ACD 11	-	Grn. brn.				-	-
ACD 12	-	Lt. grn.				-	-
Cinch Graphik							
CG 1	Passed	Grn. brn.				-	>1600
CG 2	-	Grn. brn.				10^9	-

TABLE II. PHYSICAL APPEARANCE OF TEST BOARDS

Supplier	Physical Appearance	Characteristics
Advanced Circuitry Division	Poor	Irregularly shaped pads. Color and texture of boards varied. Some internal bubbles.
Cinch-Graphik	Excellent	Color and texture of the boards were uniform. No voids. Pads were well defined.
Electralab	Fair	Color and texture of the boards were uniform. No voids. Pads were fairly well defined.
Melpar	Excellent	Color and texture of the boards were excellent. No voids. Pads were fairly well defined.
National Technology	Poor	Color and texture of the boards were poor due to post curing and resin starved areas. Pads were fairly well defined.
Photocircuits	Fair	Color and texture of the boards were fair. Boards from Photocircuits are purposely post cured to pass dip soldering and are brown in color. Pads were fairly well defined.

TABLE III. NUMBER OF BOARDS MEETING SPECIFICATION REQUIREMENTS

	Advanced Circuitry Division	Cinch Graphik	Electra-lab	Melpar	National Tech-nology	Photo-circuits
Number of Boards Measured or Tested	12	2	2	12	2	12
Board Thickness	3	2	2	10***	2	12
Hole Diameter	8	2	2	12	0	2
Hole Location	7	2	2	12	2	12
Continuity and Resistance	12	2	2	12	2	12
Warp or Twist	12	2	2	12	2	12
Layer Registration (Internal)	1*	1*	1*	1**	1*	-
Thermal Shock	0*	1*	1*	1*	1*	1*
Insulation Resistance	1*	1*	1*	1*	1*	1*
Dielectric Breakdown	1*	1*	1*	1*	1*	1*

* Test conducted on one board only
** Test conducted on two boards only
*** Requirement waived on two boards to facilitate delivery

by the 1:1 artwork, not by the degree of undercutting because conductor undercutting takes place in a trapezoidal manner.

The pads on the artwork provided for the test board were 0.060 inch diameter.

As shown in Table I, some suppliers expanded the pads and others did not. The enlarged pads on the Photocircuits boards resulted from pattern plating which causes external pads to grow. The pattern plating process requires a reduction of the pad size on the 1:1 artwork to more closely control final pad size.

3. Hole Diameter (Plated-through Holes)

The requirement for hole diameter tolerance of the test boards was $\pm$0.003 inch. This tolerance is considered premium by most suppliers since it requires more care in processing and results in lower yields. The normal tolerance is $\pm$0.005 inch. This tolerance, however, is too loose for most present electronic designs.

A wider latitude for hole size permits the supplier to drill the holes oversize and to plate to exceed the minimum thickness required in the holes. This practice allows a greater latitude in drilling and requires less control during plating.

Hole diameters were measured with a hole gage and a reticle microscope.

4. Hole Location

Measurements to establish hole location with respect to true position were made with a microscope adapted with a mechanical stage. The measurements were made between hole centers and difference from the 0.200 inch grid dimension was taken to be the deviation from true position. For example, a reading of 0.203 or 0.197 represented a true position error of 0.003 inch.

It was difficult to obtain very accurate measurements on hole location because the artwork accuracy in some instances may have contributed to the error. The accuracy of the measurement could not discriminate true position errors less than 0.003 inch; however, errors more than this are significant.

5. Minimum Pad Annulus (External)

The minimum pad annulus specified for external layers was 0.010 inch. The minimum annular ring of copper remaining around the hole depends on the pad and hole size in addition to a number of manufacturing tolerances. Measurements were made with a reticle microscope.

6. Registration

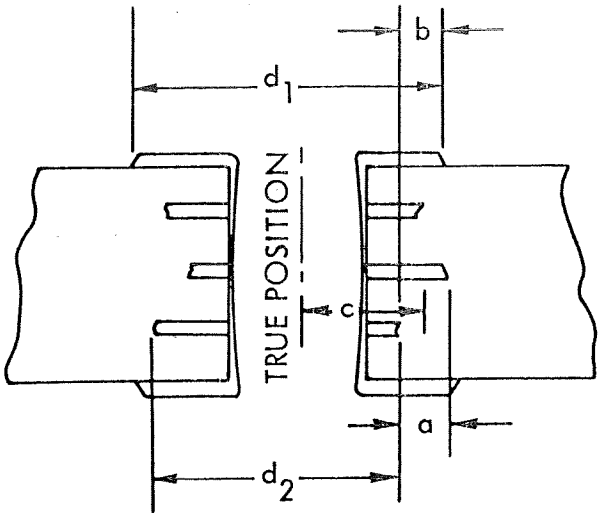
There are basically two processes in multilayer board manufacture that affect overall layer to layer registration. One of these is the laminating process which affects the registration of internal layers. The other is the process of applying the circuitry or pads to the two outside layers after laminating and plating-through. Two types of registration are required, both involving independent processes. These are referred to as "internal" and "external" registration. Internal registration is the maximum displacement between internal layers and external registration is the maximum displacement between an external and internal layer. Displacement is with respect to true position.

Internal registration depends on the accuracy of the original artwork and the accuracy of the tooling used to punch the film, drill the laminates, and position the circuit layers during laminating. Some of this accuracy depends on operator judgment and some on the accuracy and capability of the tooling. If external layers are applied by the silk screen method, registration depends mostly on operator judgment. The determining factors are the pad size and minimum pad annulus required around the hole. External layers may also be applied by photo resist methods in which case registration is determined by the accuracy of the tooling used to punch the film and drill the tooling holes.

Registration was measured in the following manner:

a. Cross sections of plated through holes were prepared in metallographical mounts and a comparison of the pad alignment on the various layers was made as shown in Figure 3.

b. The measurements (Figure 3) were taken on two perpendicular cross sections. A vector sum of the two measurements was made to obtain maximum misregistration. All measurements were made with a reticle microscope at 40X magnification.



a = Maximum internal pad misalignment

$b - \frac{d_1 - d_2}{2}$ = Maximum external pad misalignment

Registration = Vector sum of maximum misalignment on two perpendicular cross-sections

c = Pad radius with respect to true position

d_1 = Outside pad diameter

d_2 = Inside pad diameter

b = Offset between external and internal pads

Figure 3. Registration Measurements

Registration measurements could not be made on Photocircuit boards because of lack of pads on internal layers.

7. Warp or Twist

The requirement for warp or twist was 2%, and appears to be fairly liberal. The test boards were measured according to Method 6054 of Federal Test Method Standard No. 406.

8. Thermal Shock

Thermal shock consisted of floating the test board on the surface of 500°F solder for ten seconds. Only one board from each supplier was tested. All boards passed with the exception of ACD 10 which blistered and delaminated in several areas, and showed severe warpage.

9. Color

No requirement was specified to control the color of the test boards. The color, however, varies depending on the amount of post-cure. Photocircuits uses an exceptionally long post-cure to meet their own requirement for thermal shock (30 seconds in 500°F solder).

10. Continuity and Resistance

Continuity was checked on every board upon receipt. No opens were observed on any test board. The resistance of the entire pattern was measured initially and after soldering, thermal shock, vibration, temperature cycling, and humidity. No significant changes in resistance were observed on any test board.

11. Insulation Resistance

Insulation resistance measurements were made between the test points shown in Figure 2. The test pattern is continuous except at A, B, C and D where it is open permitting an insulation resistance measurement between a row of pads and a closely spaced conductor. The distance between the pads and conductors is 0.010 inch. Insulation resistance measurements were made with a Keithley 610B Electrometer and were made under the conditions listed below:

a. At room temperature as received. The results are shown in Table IV.

b. During humidity exposure as defined by MIL-E-5272 (95% relative humidity while the temperature was cycled between 20 and 71°C). Insulation resistance measurements were made after the test boards had been exposed to the specified conditions for 96 hours. The results are shown in Table V.

c. Within two hours of removal from the humidity chamber after condensed moisture on the surface of the test boards had dried. The results are shown in Table VI.

12. Dielectric Breakdown

Dielectric breakdown measurements were made between the test points shown in Figure 2. The requirement was 500 volts and the minimum spacing was 0.010 inch. The test was conducted with an Associated Research Model 404 Hypot and was run according to Method 4031 of Federal Test Method Standard 406. Breakdown did not occur internally on any of the test boards. The voltage was increased until arc over occurred between external pads.

TABLE IV. INSULATION RESISTANCE OF TEST BOARDS AS RECEIVED (Readings in Ohms)

Test Board Supplier	Test Point A	Test Point B	Test Point C	Test Point D
Advanced Circuitry Division	7×10^{11}	9×10^{11}	7×10^{11}	5×10^{11}
Cinch-Graphik	11×10^{11}	6×10^{11}	6×10^{11}	6×10^{11}
Electralab	8×10^{11}	4×10^{11}	1.5×10^{11}	6×10^{11}
Melpar	3×10^{11}	4×10^{11}	1.5×10^{11}	7×10^{11}
National Technology	9×10^{11}	6×10^{11}	4×10^{11}	8×10^{11}
Photocircuits	10×10^{11}	7×10^{11}	11×10^{11}	17×10^{11}

TABLE V. INSULATION RESISTANCE OF TEST BOARDS AT 95% RELATIVE HUMIDITY WITH CONDENSED MOISTURE ON SURFACE (Readings in Ohms)

Test Board Supplier	Test Point A	Test Point B	Test Point C	Test Point D
Advanced Circuitry Division	2×10^{5}	5×10^{4}	3×10^{5}	8×10^{4}
Cinch-Graphik	1×10^{7}	1.3×10^{6}	4×10^{6}	1.3×10^{6}
Electralab	1.7×10^{5}	3×10^{5}	1.7×10^{6}	1.6×10^{5}
Melpar	3.7×10^{5}	2.5×10^{5}	1.7×10^{6}	1×10^{5}
National Technology	1.8×10^{5}	6×10^{4}	5×10^{5}	5×10^{6}
Photocircuits	3×10^{4}	2.7×10^{4}	2.7×10^{4}	3.7×10^{4}

TABLE VI. INSULATION RESISTANCE OF TEST BOARDS AFTER HUMIDITY WITH SURFACE MOISTURE REMOVED (Readings in Ohms)

Test Board Supplier	Test Point A	Test Point B	Test Point C	Test Point D
Advanced Circuitry Division	6×10^{9}	3.5×10^{9}	5×10^{9}	7×10^{9}
Cinch-Graphik	8.5×10^{9}	6.8×10^{9}	5.6×10^{9}	5.6×10^{9}
Electralab	1.2×10^{9}	7.8×10^{8}	7.0×10^{8}	5.7×10^{8}
Melpar	1.3×10^{9}	3.6×10^{9}	1.2×10^{9}	3.7×10^{9}
National Technology	2×10^{8}	5×10^{7}	7×10^{7}	1×10^{8}
Photocircuits	1.0×10^{8}	5.7×10^{7}	8.7×10^{7}	1.7×10^{8}

SOLDERING

All multilayer test boards were examined for solderability and ability to withstand three complete repair cycles. In order to obtain consistently reliable solder joints and to minimize the possibility of damage to the boards the following controls (Ref 2) were established:

1. Soldering iron voltage: 17 watts.
2. Soldering iron tip size: 0.032 inch diameter bevel tip.
3. Input voltage to iron for correct tip temperature: 95 to 115 volts.
4. Repair procedure and associated tools.
    a. The solder was flowed and the lead wire was removed.
    b. The solder was withdrawn from the hole using a hollow heating tip and a continuous vacuum.
    c. A new lead wire was soldered into the hole.
    d. Steps a, b, and c were repeated for two additional cycles.

To approximate actual flat pack soldering conditions as closely as possible, 0.004 x 0.018 inch gold plated kovar leads were soldered into 407 holes on each of the boards. The leads were soldered on both sides of each of 42 test boards making 34,188 individual soldering operations. Five percent of the solder joints were unsoldered three times for an additional 5124 soldering operations or a total of 39,312 soldering operations.

The problem of poor solderability to gold plating was encountered in the two boards from Electralab and several boards from ACD. Poor wetting and very little capillary flow resulted on these, because of inadequate control during plating. Most of the boards exhibited fair wetting and capillary flow. With good capillary flow, the solder joint could be achieved in one operation rather than two.

The soldering of a test board is shown in Figure 4. The equipment and technique used for desoldering is shown in Figure 5. Comments on the solderability of the test boards from the various suppliers are given in Table VII.

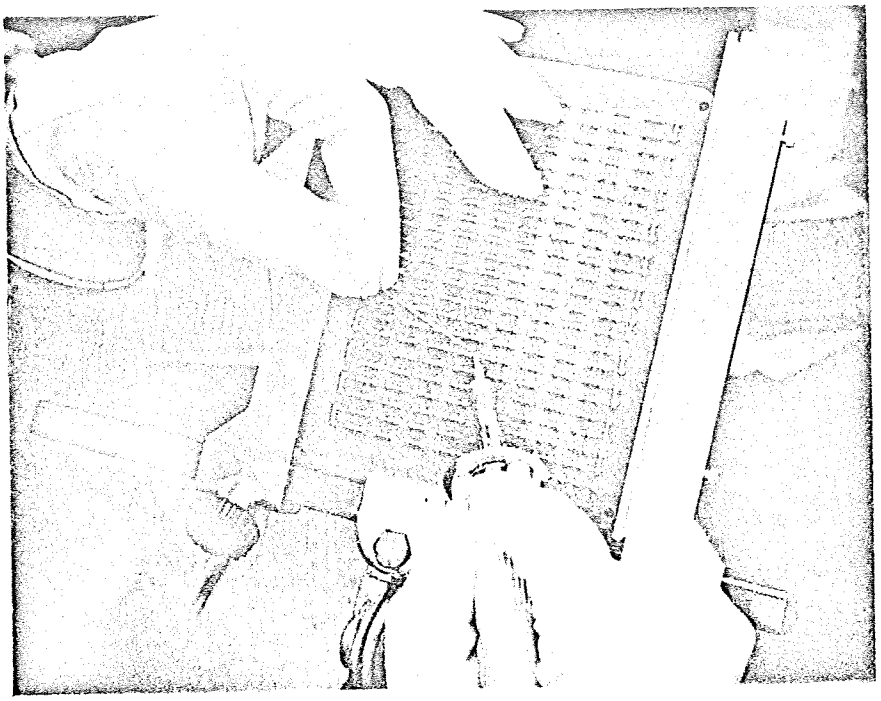


Figure 4. Soldering of Multilayer Test Board

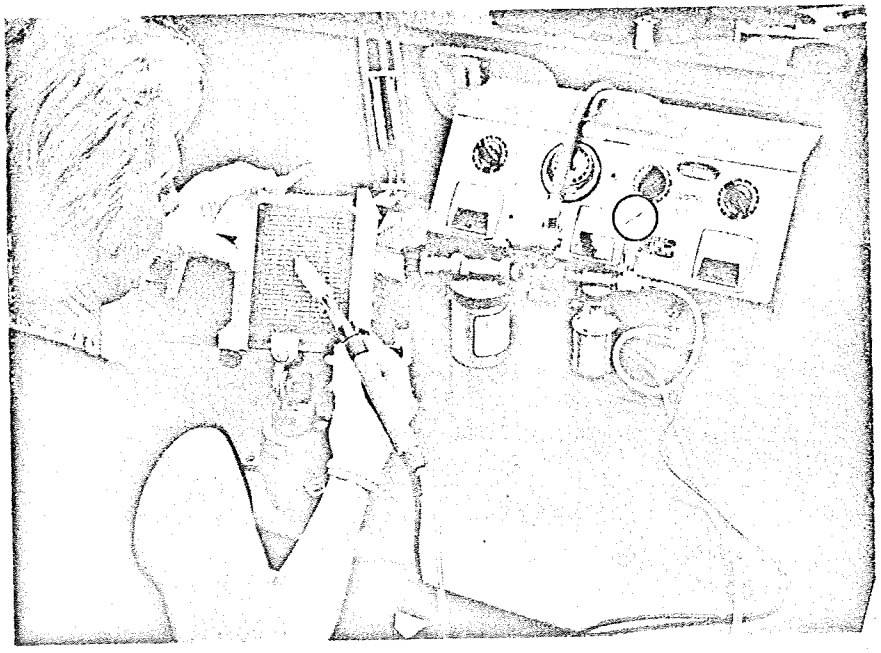


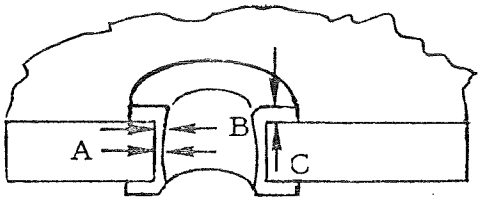
Figure 5. Desoldering of Multilayer Test Board Using a Hollow Heating Element Operating On a Continuous Vacuum

TABLE VII. SOLDERABILITY OF TEST BOARDS

Supplier	Solderability	Soldering Iron and Tip	Soldering Iron Voltage Input
Advanced Circuitry Division	Poor. Little or no capillary flow. Small solder globules formed during initial soldering cycle.	Hexacon H11 HT868D Tip	115v (Side 1) 110v (Side 2)
Cinch-Graphik	Fair. Fair wetting and capillary flow.	Hexacon H11 HT868D Tip	100v (Side 1) 105v (Side 2)
Electralab	Poor. Poor wetting and little or no capillary flow.	Hexacon H11 HT868 Tip	95v (Side 1) 95v (Side 2)
Melpar	Fair. Fair wetting and capillary flow.	Hexacon H11 HT868 Tip	110v (Side 1) 105v (Side 2)
National Technology	Fair wetting on pad. Poor capillary flow. Board appeared to soften and flow around pad during soldering.	Hexacon H11 HT868 Tip	100v (Side 1) 110v (Side 2)
Photocircuits	Excellent. Good wetting and capillary flow.	Hexacon H11 HT868D Tip	105v (Side 1) 100v (Side 2)

TABLE VIII. PLATING THICKNESS MEASUREMENTS

Supplier	Test Board	Location	Cu Plating (inch)	Ni Plating (inch)	Au Plating (inch)
Advanced Circuitry Division	ACD 5	A	0.00095	0.0005	0.00010
		B	0.0012	0.0012	0.00011
		C	0.0015	0.0014	0.00012
Cinch-Graphik	CG 1	A	0.0016	-	0.00018
		B	0.0017	-	0.00021
		C	0.0030	-	0.00022
Electralab	E 1	A	0.0016	-	0.00010
		B	0.0025	-	0.00010
		C	0.0032	-	0.00018
Melpar	M 9	A	0.0011	0.0004	0.00011
		B	0.0015	0.0003	0.00015
		C	0.0017	0.0015	0.00018
National Technology	NT 1	A	0.0003	0.0003	0.00011
		B	0.0008	0.0004	0.00012
		C	0.0012	0.0007	0.00013
Photocircuits	P 1	A	0.0017	0.0006	0.00005
		B	0.0026	0.0012	0.00006
		C	0.0050	0.0022	0.00006



Measurement Locations

METALLOGRAPHIC SECTIONING

Metallographic cross sections were made to determine the plating thickness and the appearance of plated-through holes before and after soldering.

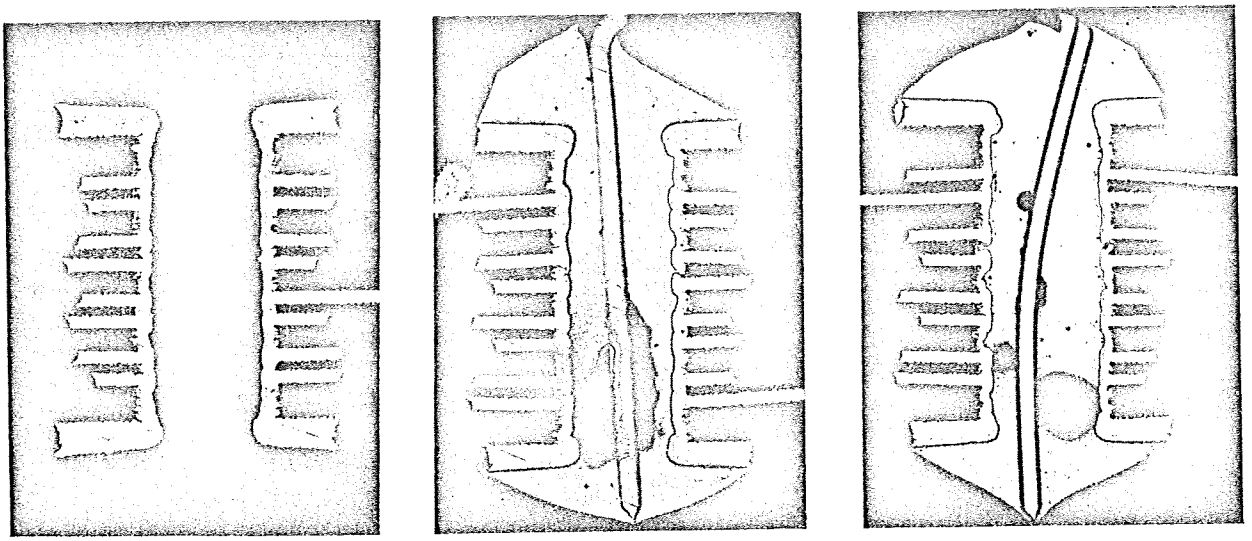
A requirement of a minimum copper plating thickness inside the hole was established at 0.0015 inch. This thickness requirement is arbitrary and was based on the fact that a certain degree of structural strength was required for component lead insertion and removal. It appears that in some instances this requirement should be 0.001 inch or less to allow for the tendency of the plating thickness to increase toward the outside of the hole. The conflict between hole sizes and internal conductor spacing requirements would then be minimized making hole size tolerances easier to achieve.

The requirement for nickel plating was 0.0003 inch minimum thickness. The gold plating thickness requirement was 0.000050 to 0.000080 inch. Suppliers prefer to plate 0.000100 to 0.000200 inch of gold to insure sufficient coverage for etching. Gold plating thicknesses greater than 0.000100 inch cause soldering difficulties because the excess gold in solution degrades the strength and appearance of the solder joint.

Plating thickness measurements are recorded in Table VIII. The measurements were made on sections selected at random and can only be used as an indication of the entire lot. Measurements were made at the locations shown.

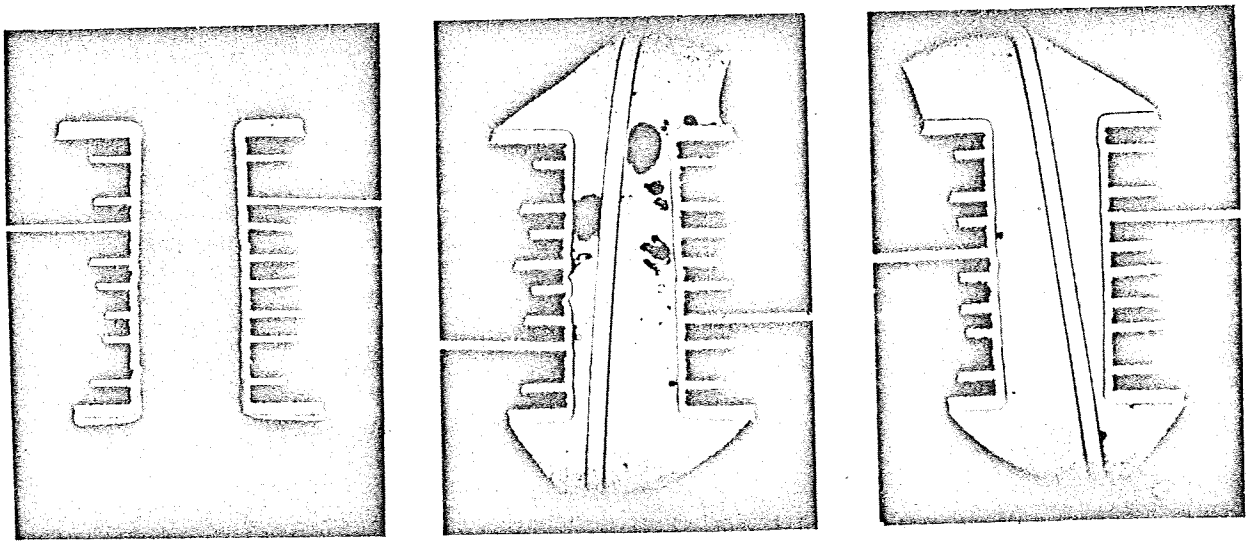
With a few exceptions, most of the measurements made for copper and nickel thicknesses met the specified requirements. Only one supplier, however, met the gold plating requirement.

Photomicrographs of plated through holes before and after soldering are shown in Figures 6 through 11.



Unsoldered | Soldered Once | Resoldered Three Times

Figure 6. Metallographic Sections, Advanced Circuitry Division (Litton) Plated-Through Holes (28X)



Unsoldered | Soldered Once | Resoldered Three Times

Figure 7. Metallographic Sections, Cinch-Graphik Plated-Through Holes (28X)

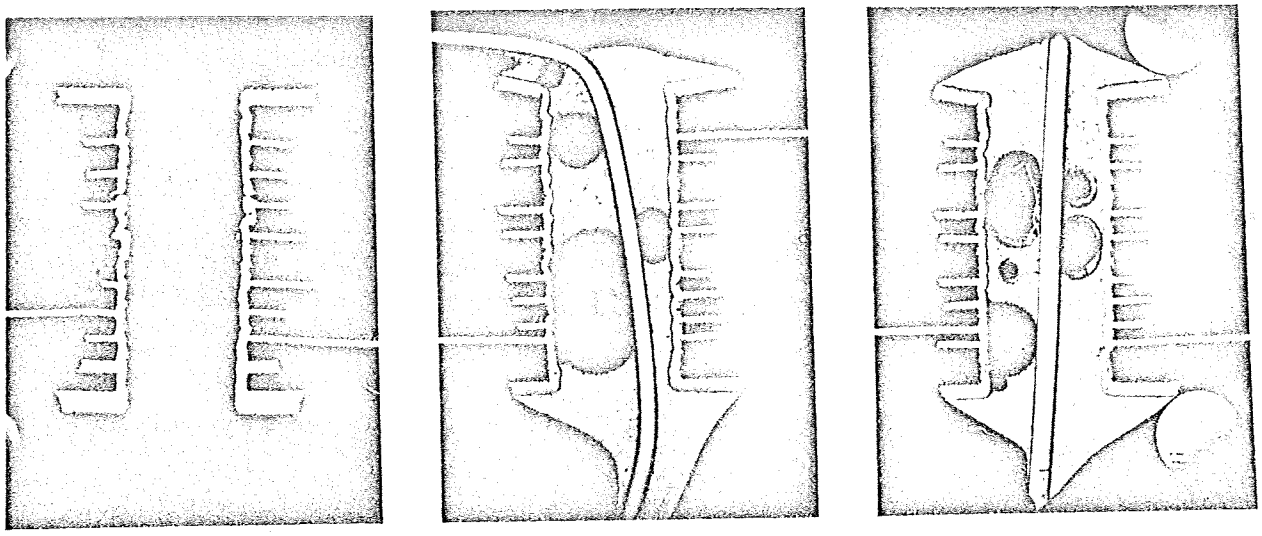


Figure 8. Metallographic Sections, Electralab Plated-Through Holes (28X)

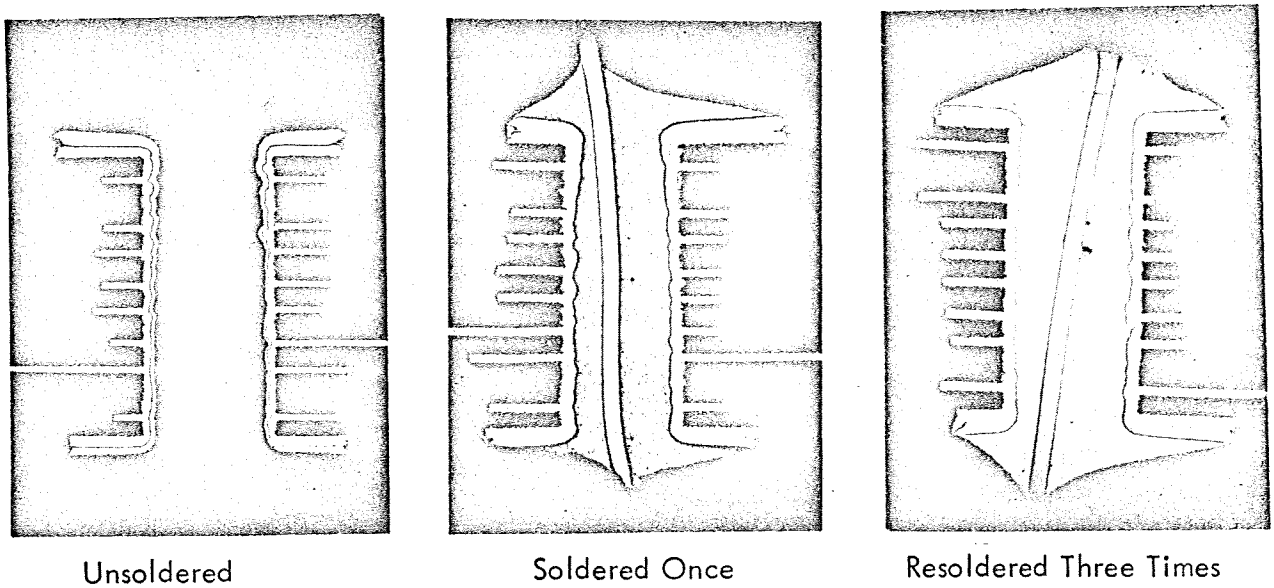
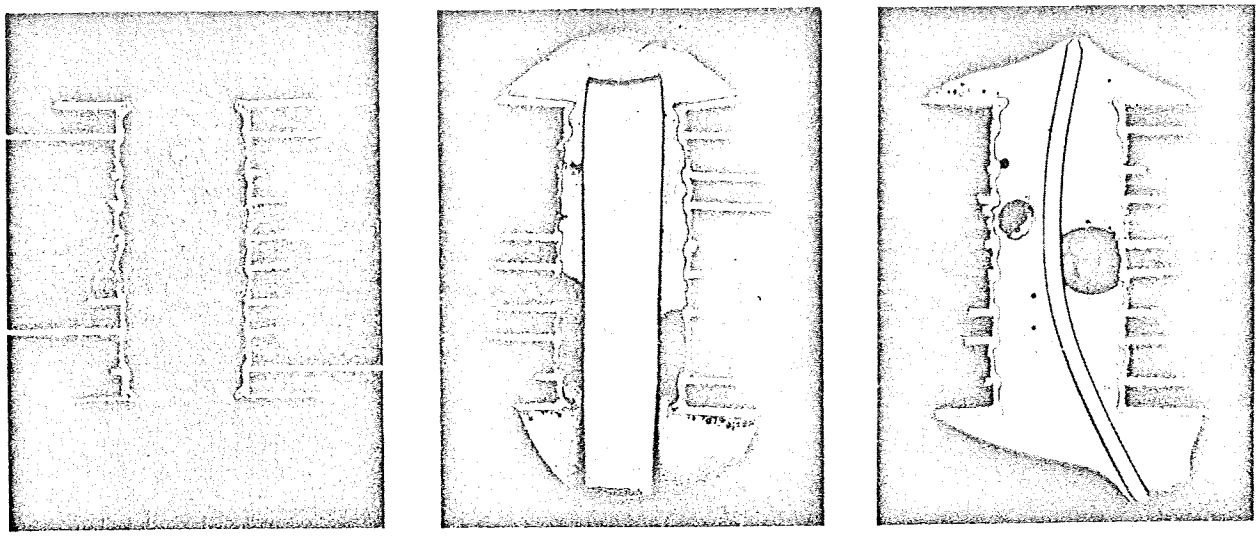
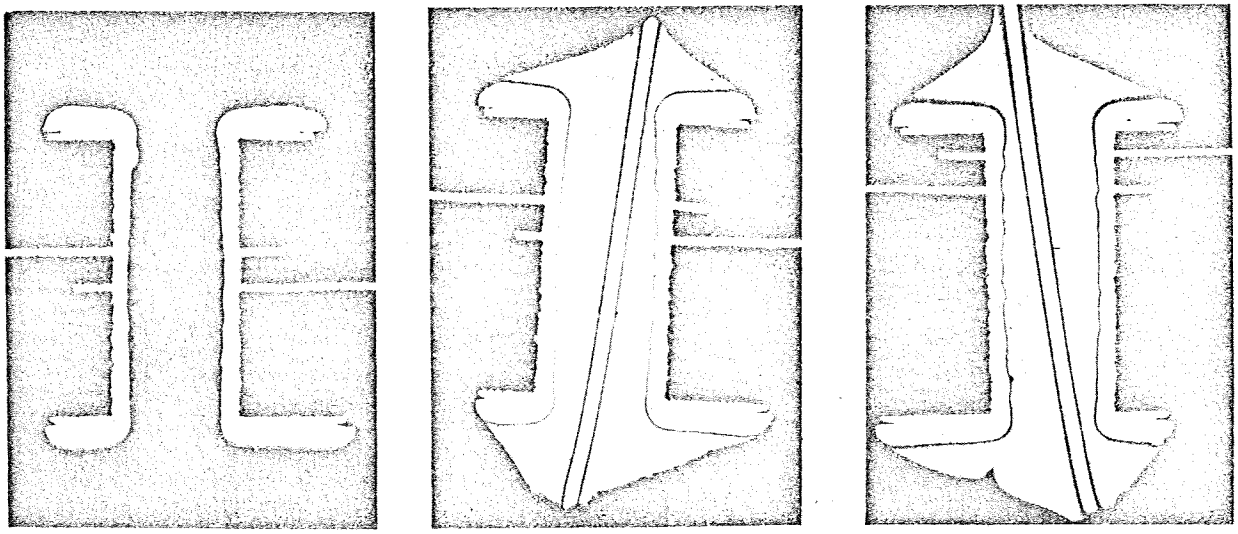


Figure 9. Metallographic Sections, Melpar Plated-Through Holes (28X)



Unsoldered Soldered Once Resoldered Three Times

Figure 10. Metallographic Sections, National Technology Plated-Through Holes (28X)



Unsoldered Soldered Once Resoldered Three Times

Figure 11. Metallographic Sections, Photocircuits Plated-Through Holes (28X)

TEMPERATURE CYCLING

Temperature cycling consisted of cycling the boards from +85°C to -55°C with one hour at temperature and one hour transition between temperatures. Continuity was monitored with 100 milliamperes of current flowing through each board. The test boards were temperature cycled following the soldering, resoldering, and vibration tests. A tabulation of the joint hours completed in these tests is listed in the Summary (page 26). Since all the boards were not available at the same time, several temperature cycling tests had to be scheduled. As a result, some boards accumulated a greater number of hours in the chamber. It was necessary to accumulate a maximum of four million joint hours to form a basis for the reliability assessment. Approximately twice that number was provided from the combined tests.

VIBRATION

Vibration tests higher than the levels defined for LEM-AEA were conducted on all 42 test boards. A sweep test was performed on each sample to determine the natural frequency and the transmissibility of each board (Table IX). Once these values were determined, the input to give the same response on the board at resonance that would be experienced during the qualification sinusoidal vibration test was computed. Each board was then tested at this level for thirty minutes. The transmissibility of the test boards was approximately 50 which was much higher than expected. In practice, the transmissibility of the boards will be approximately 17 because of the damping provided by attached components and conformal coating. The boards were mounted to the vibration table by standoffs as shown in Figure 12. All boards were monitored with a nanosecond intermittency detector during test. No continuity failures (Ref 3) were observed during vibration testing.

In the testing of board M1, the first item tested, the response accelerometer amplifier became saturated during the sweep test at a low level acceleration. As a result this one unit was greatly overtested for a period of ninety minutes, but no failure occurred. The response levels for this unit were 0.25, 0.375, and 0.5 inch in double amplitude for thirty minutes each. The corresponding response acceleration levels at the sample natural frequency of 300 cps (Ref 4) were 1150, 1730 and 2310 G peak.

TABLE IX. NATURAL FREQUENCY (F_n) AND TRANSMISSIBILITY (Q) OF TEST BOARDS

Supplier	Test Board Number	F_n (cps)	Q
Advanced Circuitry Division	ACD 1	200	45
	ACD 2	190	50
	ACD 3	180	55
	ACD 4	130	30
	ACD 5	140	35
	ACD 6	160	50
	ACD 7	130	25
	ACD 8	155	50
	ACD 9	160	45
	ACD 10	165	55
	ACD 11	140	25
	ACD 12	160	65
Cinch Graphik	CG 1	177	52
	CG 2	180	50
Electralab	E 1	185	50
	E 2	200	50
Melpar	M 1	275	53
	M 2	290	65
	M 3	190	55
	M 4	200	70
	M 5	210	75
	M 6	205	70
	M 7	195	65
	M 8	190	60
	M 9	205	55
	M 10	200	65
	M 11	200	70
	M 12	200	70
National Technology	NT 1	210	90
	NT 2	225	65
Photocircuits	P 1	190	52
	P 2	195	55
	P 3	200	40
	P 4	200	47
	P 5	200	50
	P 6	195	46
	P 7	210	50
	P 8	200	52
	P 9	210	53
	P 10	210	46
	P 11	215	55
	P 12	195	40

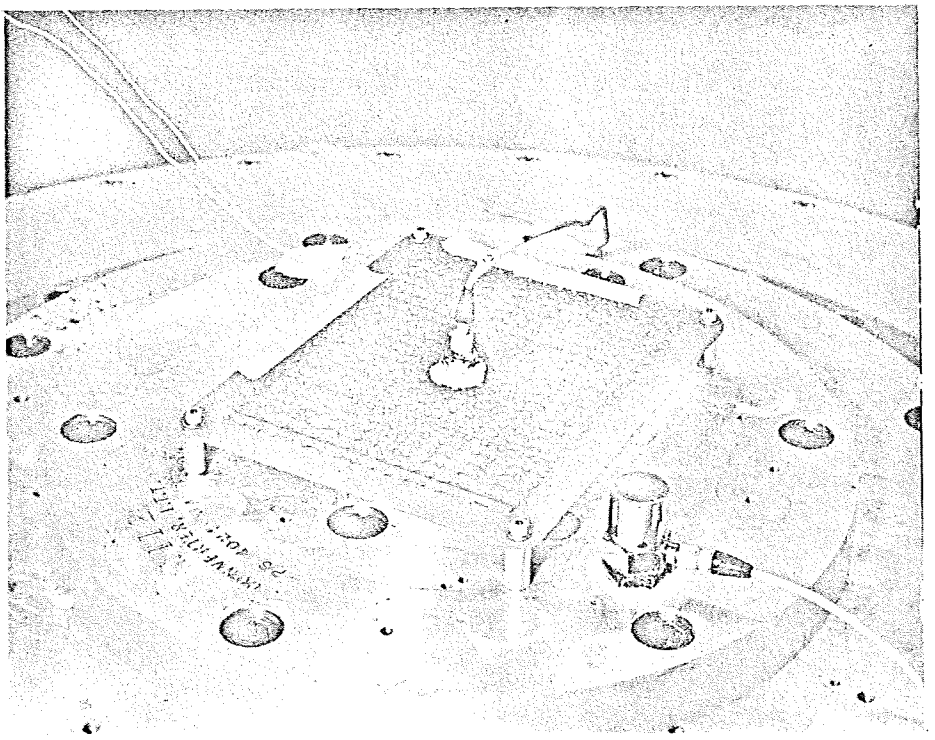


Figure 12. Mounting of Test Board for Vibration

The peak acceleration level on the test boards at the unit natural frequency for the response level of 0.2 inch double amplitude is given in Figure 13. A representative transmissibility curve (Ref 5) is shown in Figure 14.

VACUUM TESTING

Samples of four of the multilayer test boards were checked for outgassing at 10^{-7} torr at 200°F. The sublimation rates were recorded over a period of 200 hours and are shown in Figure 15.

SUMMARY OF TESTING

Forty-two multilayer circuit test boards have accumulated a total of 9,370,000 joint-hours of temperature cycling and a total of 7,877 joint-hours of vibration testing.

TABLE X. SUMMARY OF TESTS COMPLETED

Supplier	Soldering and Rework	Temperature Cycling 25 cycles (100 hours)	Temperature Cycling 130 Cycles (520 hours)	Vibration
ACD	12	0	12	12
Cinch-Graphik	2	2	2	2
Electralab	2	2	2	2
Melpar	12	2	12	12
National Technology	2	0	2	2
Photocircuits	12	2	12	12
Total Number of Test Boards	42	8	42	42

MISSION RELIABILITY EVALUATION (Ref 6)

For meaningful reliability evaluation, test data must first be reduced to a form equivalent to mission application. The following analysis, based upon the given assumptions, reduces the test data to mission equivalent hours for an Abort Electronics Assembly of the Lunar Excursion Module.

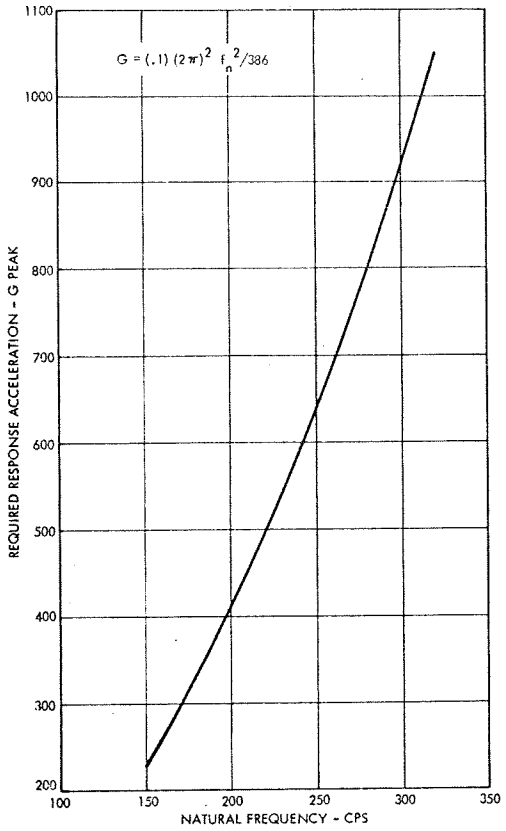


Figure 13. Natural Frequency Vs Response Acceleration for Response Double Amplitude of 0.2 Inch

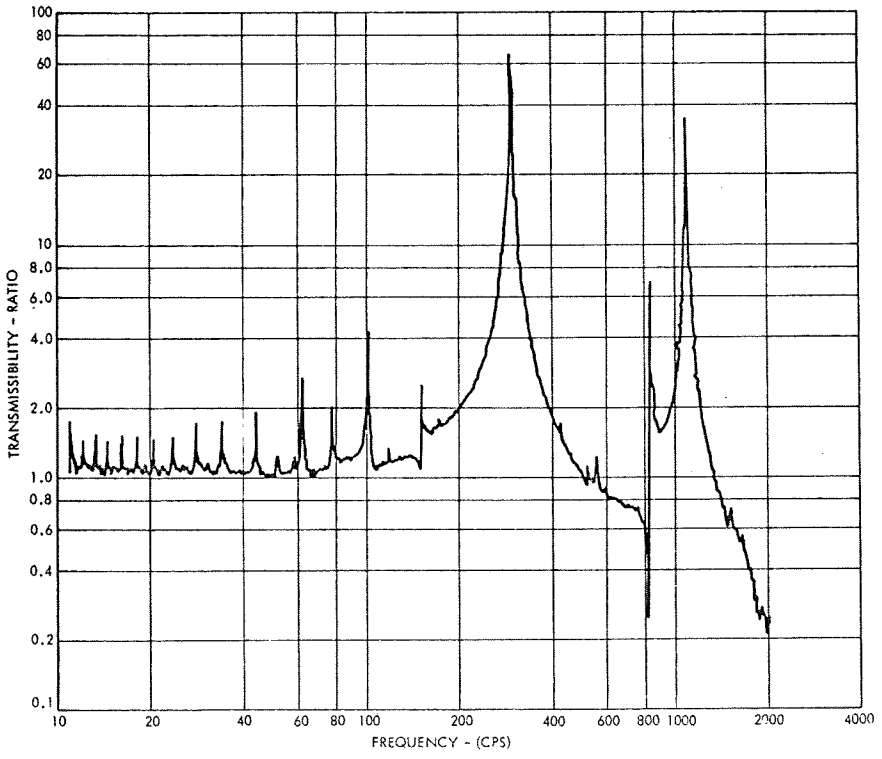
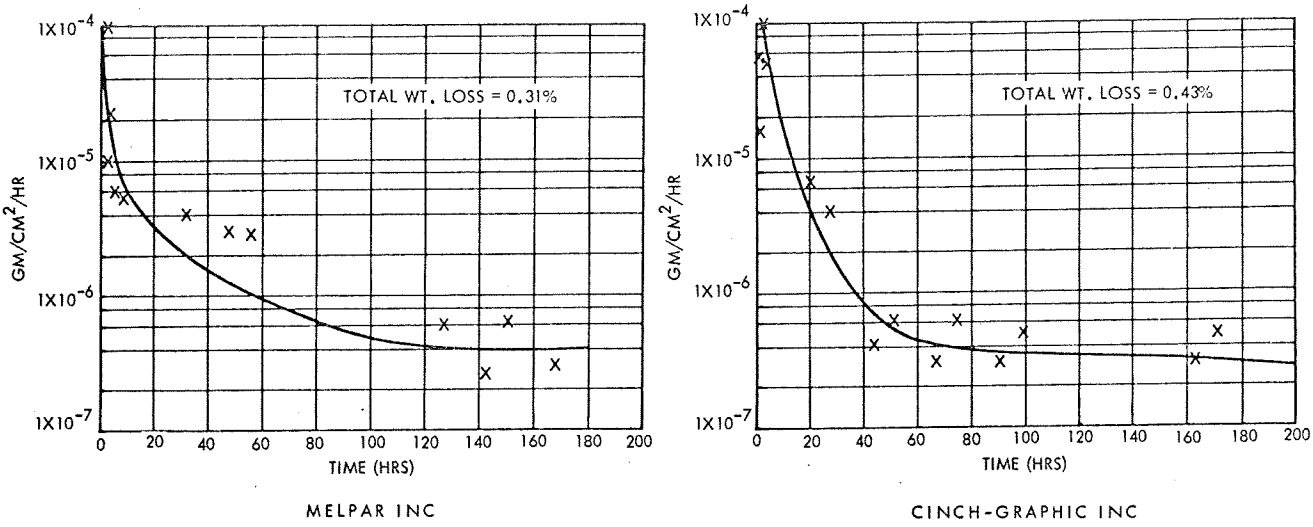


Figure 14. Vibration Transmissibility Curve



MULTILAYER CIRCUIT BOARD SAMPLES

TEST TEMPERATURE: 200°F

TEST PRESSURE: 10^{-7} TORR

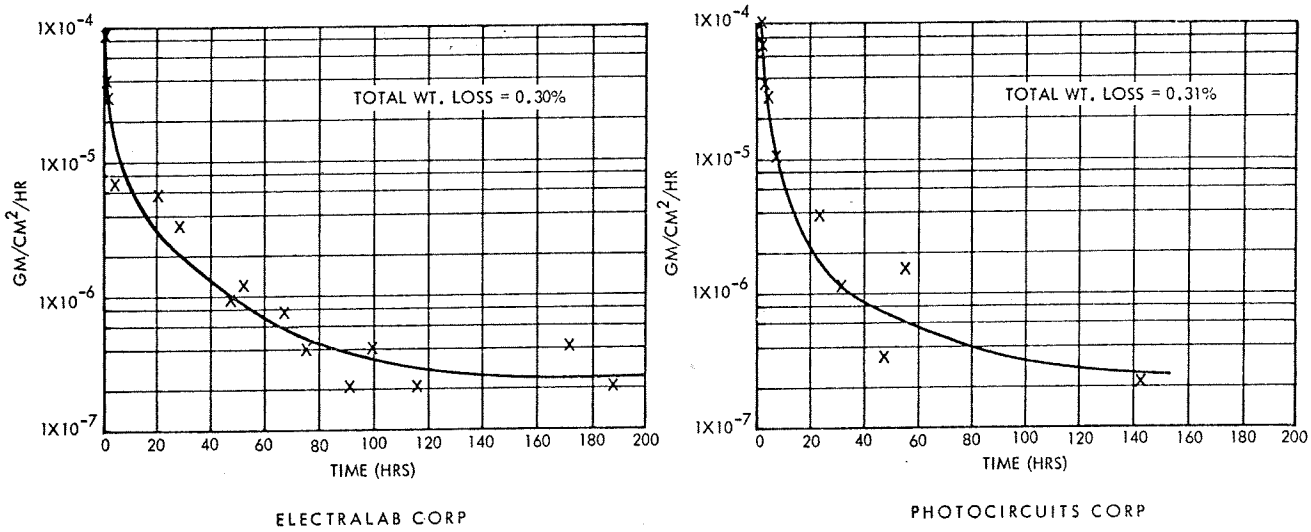


Figure 15. Sublimation Rate as a Function of Time in Vacuum Test Environment

Two factors entering into computation of mission equivalent time are number of cycles and cycling extremes. Since each temperature cycle is four hours, the total joint-hours of time may be converted to total joint cycles by dividing time by 4. And since there are three such cycles per Lunar Orbiting Rendezvous mission, the equivalent missions are the number of joint cycles divided by 3. Also a mission is approximately 120 hours, thus a final figure for number of cycles is obtained by multiplying by 120.

The second factor, cycling extremes, requires an acceleration factor to compensate for the more severe temperature range encountered in mission applications. The test temperature range is approximately double that for the mission (-55 to +85 versus 0 to 70 degrees C). Assuming that the stresses are proportional to the ΔT we should use a value of K_e of 2. This is conservative since the stress rises at a non-linear rate over this temperature range and the actual stresses are probably more than twice the required level (or mission level).

Combining the above considerations, we have the following computation:

Mission Equivalent Time (Thermal) =

$$\frac{9{,}370{,}000 \times 120 \times 2}{3 \times 4} = 187{,}400{,}000 \text{ hours}$$

At a 60% confidence level, this value of time (with zero failures) yields a failure rate of 0.0049 per 10^6 hours.

The vibration test levels employed accelerate failure rates by 6 to 15 times, or an average of about 10. The duration of vibration in the mission profile is 39 minutes or about 2/3 hour. Thus, the mission equivalent time for vibration is computed as 7866 x 3/2 x 10 = 118,000 hours. This does not significantly alter the value of failure rate but does lend a measure of confidence in the results.

This computation, while showing a relatively low failure rate, is not considered to be optimistic. One factor is that the actual number of joints per position on a test board is two rather than one, as assumed in computing joint-hours. Also, the stress factor due to temperature is conservative. Further testing will be required to establish lower failure rates to meet the desired goal of 0.001 per 10^6 hours. This added testing will also permit computation of failure rates at a higher level of confidence (Ref. 6).

CONCLUSIONS

1. No outstanding differences in reliability or quality of plated-through hole interconnections were observed on any of the 42 test boards.

2. The solderability of the boards varied from excellent to poor. All Photocircuits boards showed excellent solderability. The boards from Melpar, Cinch Graphik and National Technology generally exhibited fair solderability. Poor solderability was observed on some Advanced Circuitry Division and Electralab boards.

3. The quality of the boards based on appearance and physical measurements varied from good to poor. None of the suppliers were able to meet all of the drawing and specification requirements. The major discrepancies noted were hole sizes, hole location, over etched pads, and overall board thickness.

The performance of Electralab, Cinch Graphik, Melpar, and Photocircuits was generally good. The performance of National Technology and Advanced Circuitry Division was generally somewhat inferior.

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3. "Vibration Testing of LEM Multilayer Circuit Boards," R. L. Mac Gregor, February 16, 1965, TRW Systems IOC 9372.1-513.

4. "Resonance Testing of LEM Multilayer Circuit Boards," R. L. Mac Gregor, June 11, 1965, TRW Systems IOC 9372.1-633.

5. "LEM/AEA Multilayer Circuit Board Vibration Tests," R. C. Keidel, September 20, 1965, TRW Systems IOC 9522.3-408.

6. "Mission Reliability Evaluation," M. A. Grossman, TRW Systems Internal Communication.

EXPLANATORY NOTE

The testing described in this report was performed by TRW Systems for Grumman Aircraft Engineering Corporation under P. O. 2-24485 as a part of the Lunar Excursion Module program, Contract NAS 9-1100. The contents of this report are being submitted to Grumman in essentially identical form under a separate report number.