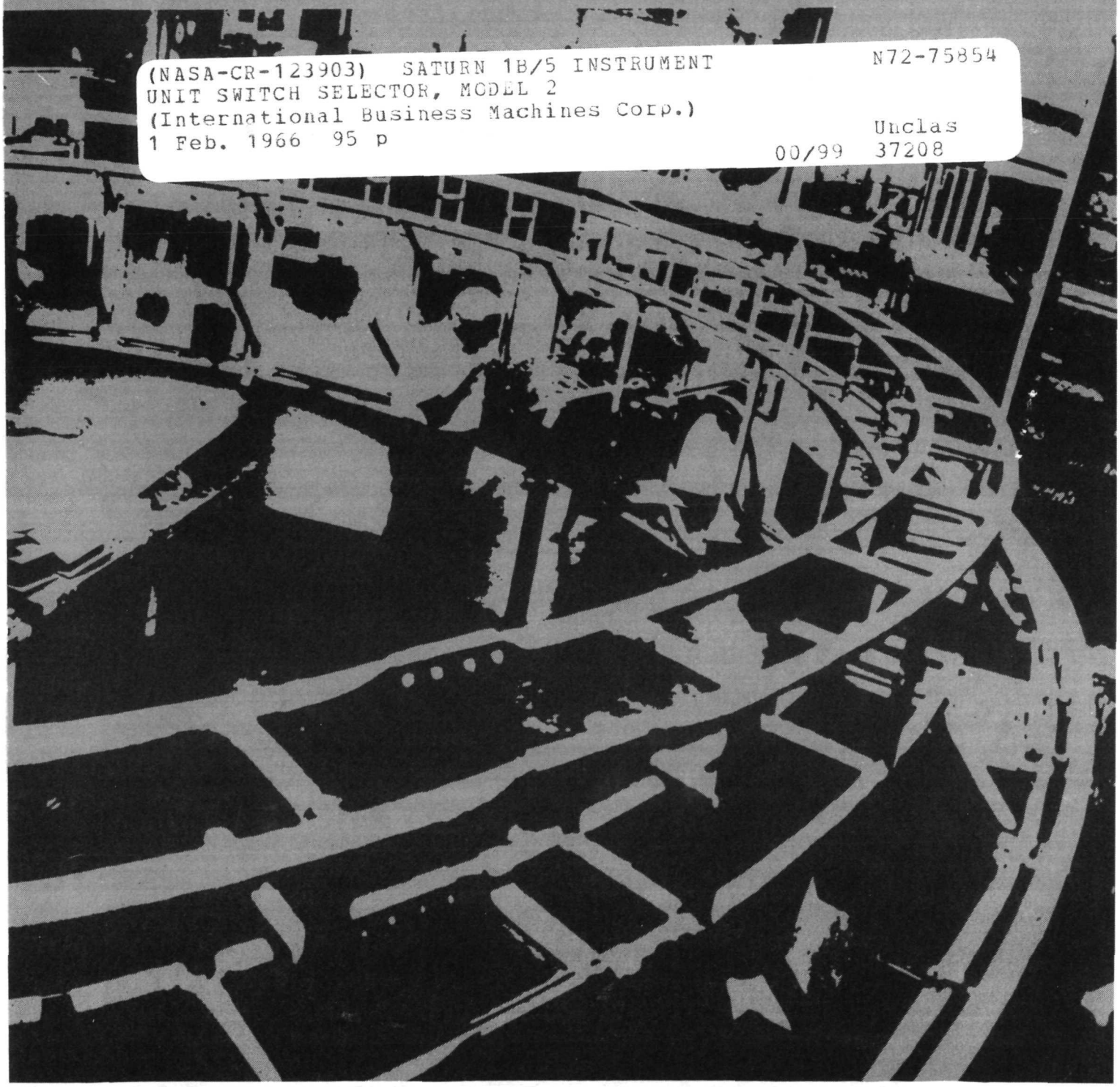
IBM

Saturn IB/V - Instrument Unit

Technical Manual

MSFC No. III-5-510-9
IBM No. 66-966-0001

Switch Selector, Model II



MSFC No. III-5-510-9

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TECHNICAL MANUAL

SATURN IB/V INSTRUMENT UNIT SWITCH SELECTOR, MODEL II

Prepared under Contract

NAS 8-14000

by

International Business Machines Corporation

Federal Systems Division

Huntsville, Alabama

1 February 1966

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LIST OF RELATED DOCUMENTS

The manuals listed below have been published under NASA contracts as source and reference information on IU systems and/or components.

Title	Number		Published Date	Changed Date
	IBM	MSFC		
Saturn IB/V Instrument Unit Structure Repair Manual	65-966-0011H	III-5-510-1	1 September 1965	
Auxiliary Power Distributors	65-966-0013H	III-5-510-2	1 October 1965	
Power Distributor	65-966-0014H	III-5-510-3	1 October 1965	
Emergency Detection System Distributor	65-966-0015H	III-5-510-4	1 October 1965	
Control Distributor	65-966-0016H	III-5-510-5	1 October 1965	
Measuring Distributors	65-966-0017H	III-5-510-6	1 October 1965	
56 Volt Power Supply	65-966-0018H	III-5-510-7	1 October 1965	1 January 1966
5 Volt Measuring Voltage Supply	65-966-0019H	III-5-510-8	1 October 1965	
Saturn IB/V Instrument Unit Instrumentation System Description	65-966-0021H	III-5-509-1	1 November 1965	1 January 1966
Switch Selector, Model II	66-966-0001	III-5-510-9	1 February 1966	

LIST OF SPECIFICATIONS AND PROCEDURES
FOR SWITCH SELECTOR, MODEL II

Title	Number
Schematic	6101534
Switch Selector (Top Drawing)	6101400 (50M67864)
Design Specification	6009026
Acceptance Test Plan	373-66644-05
Qualification Test Plan	373-66644-06
Unit Outline	6101487

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ILLUSTRATIONS

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TABLES

SECTION I

INTRODUCTION AND DESCRIPTION

1-1 INTRODUCTION

This technical manual defines the principles of operation, packaging procedures, and maintenance and repair instructions for the Model II Switch Selector (see Figure 1-1).

The Switch Selector is a combination solid state and electromechanical component which provides interstage mode and sequence control between the Launch Vehicle Digital Computer/Launch Vehicle Data Adapter (LVDC/LVDA) and the stage distributors. One Switch Selector is located in each stage and in the Instrument Unit of the Saturn Launch Vehicles.

By utilizing a digital coding-decoding technique, each Switch Selector can activate, one at a time, 112 different circuits in the stage in which it is located. Coding of the flight sequence commands and the decoding of these commands by the stage Switch Selectors has the following advantages: the number of interface lines between stages is reduced; flexibility of the system with respect to timing and sequencing is increased; and the discrete output circuitry of the LVDC/LVDA is conserved.

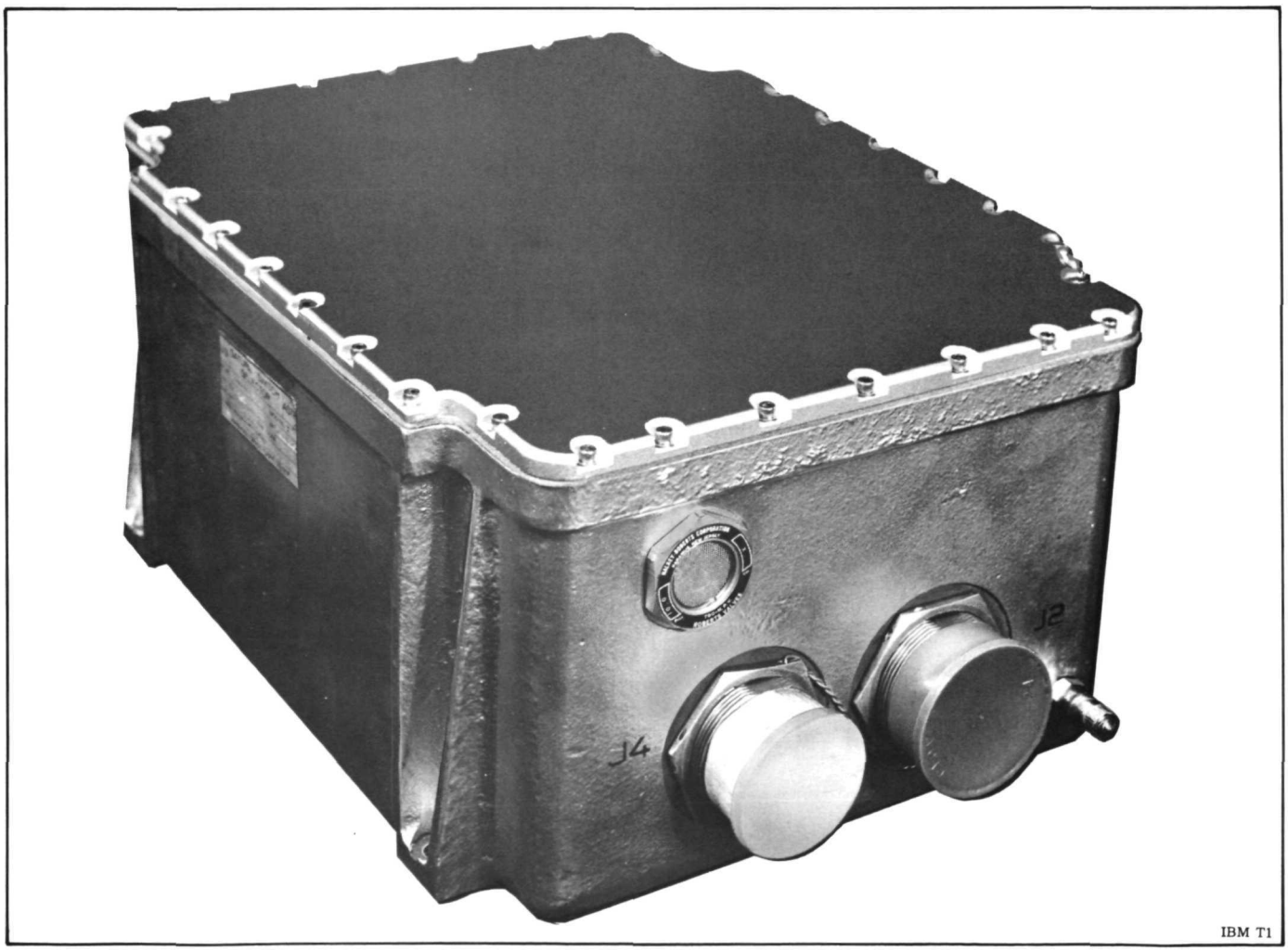

Figure 1-1. Switch Selector, Model II (Three-Quarter View)

1-2 DESCRIPTION

1-3 MECHANICAL DESIGN

The mechanical design of the Switch Selector is comprised of a housing, cover, cover gasket, and an electrical assembly. The electrical assembly consists of two panel assemblies, a harness assembly, two RFI filters, and 34 circuit modules. There are 4,684 discrete electrical components packaged in the circuit modules.

Circuit Modules

Figure 1-2 shows a typical Switch Selector circuit module. Electrical components (transistors, resistors, diodes, relays) are mounted between two epoxy-glass insulator plates which serve primarily as a holding fixture. Rectangular nickel wire (0.010 inch thick by 0.020 inch wide) is welded to the component leads to provide the circuit interconnections. Dual wires with separate welds for each wire are used where required, for circuit interconnections to improve reliability. A Fiberite FM-4005 molded connector is mounted at the bottom of the assembly. The connector contains 22 dual pins. Each pin is formed to a 90° bend such that one end of the pin protrudes from the side of the connector and the other end of the pin protrudes from the bottom of the connector. The interconnection wire is welded to the dual pins on the sides of the connector to provide inputs and outputs through the pins to the bottom of the module. Another connector is mounted to the top of the module and is utilized for testing to the detailed part and circuit function level. The interconnection wires to the test connector are simplex. The connectors on the top and bottom of the module are identical except that the pins on the test connector are cut to 0.015 inch to prevent interference. Two threaded inserts in the bottom of the module connector are used for attachment of the module to the panel assembly. Specific unused pins are cut off to provide polarized mounting for each module type.

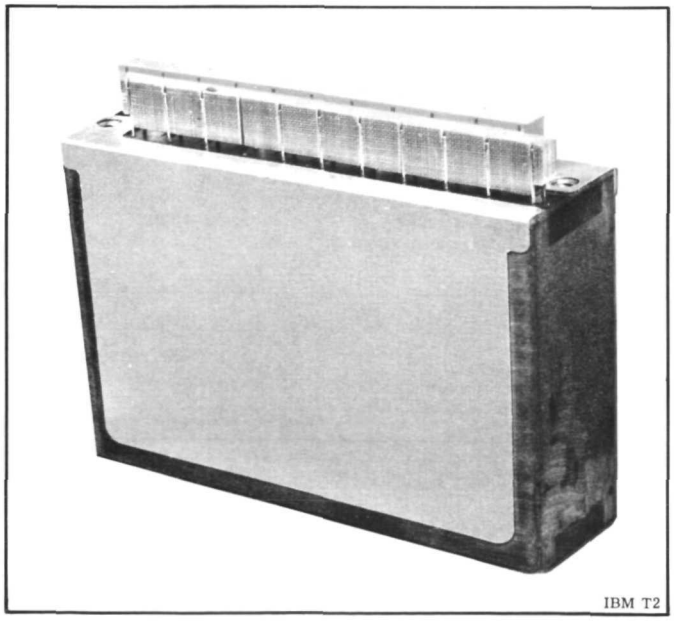

Figure 1-2. Switch Selector Circuit Module

The module is completely cast in Stycast 1090 except for the top surface of the test connector and the bottom surface of the module connector. Aluminum foil heat sinks, 0.10 inch thick are formed to the sides and bottom of the module and bonded in place.

The overall size of the module is 3.00 inches long by 0.80 inch wide by 2.00 inches high. The Switch Selector utilizes 13 of the 16 available types of modules to make up the 34 modules required for each Switch Selector. Table 1-1 lists the various types of modules and their function.

Table 1-1. Types and Use of Switch Selector Circuit Modules

Module	Function	Number Required per Switch Selector
Type 1	Decode - provides row and column decode capability	7
Type 2	Output driver	14
Type 3	Read command	2
Type 4	Stage select	3 until S/N 118, 2 on subsequent S/N's
Type 5	Automatic reset - RC Network and thermistors	1
Type 6	AG Logic drivers	1
Type 7	Decode	1
Type 8	Miscellaneous drivers	1
Type 9	Miscellaneous drivers	None after prototype 3
Type 10	Relay module	None after prototype 3

Table 1-1. Types and Use of Switch Selector Circuit Modules (Cont)

Module	Function	Number Required per Switch Selector
Type 11	Relay module	1
Type 12	Miscellaneous driver	None after S/N 104
Type 13	Relay module	1
Type 14	Relay module	1
Type 15	Decode - switch power, zero indicate, and column 02	1
Type 16	Relay module	1 after S/N 117

Panel Assemblies

The two panel assemblies (see Figure 1-3) provide electrical interconnections, thermal conduction, and mounting support for the circuit modules. A panel assembly consists of a printed wiring board, a heat-sink plate, harness supports, and harness connection terminals.

The printed wiring board is 0.062 inch thick glass-epoxy laminate with a wiring pattern on both sides and "plated through" holes. The harness connection terminals are swaged and soldered into specific "plated through" holes in the printed wiring board.

The heat-sink plate is magnesium alloy 0.091 inch thick. The plate has machined rectangular openings at each circuit module and harness terminal location which provide electrical clearance around the module pins and harness terminals. The plate is coated with a polyurethane resin for additional electrical insulation. The heat-sink plate is bonded with epoxy resin to the top side of the printed wiring board.

Two harness supports made of magnesium alloy are mounted at right angles to each other over the rows of harness terminals and between the circuit module locations and bolted to the panel assembly.

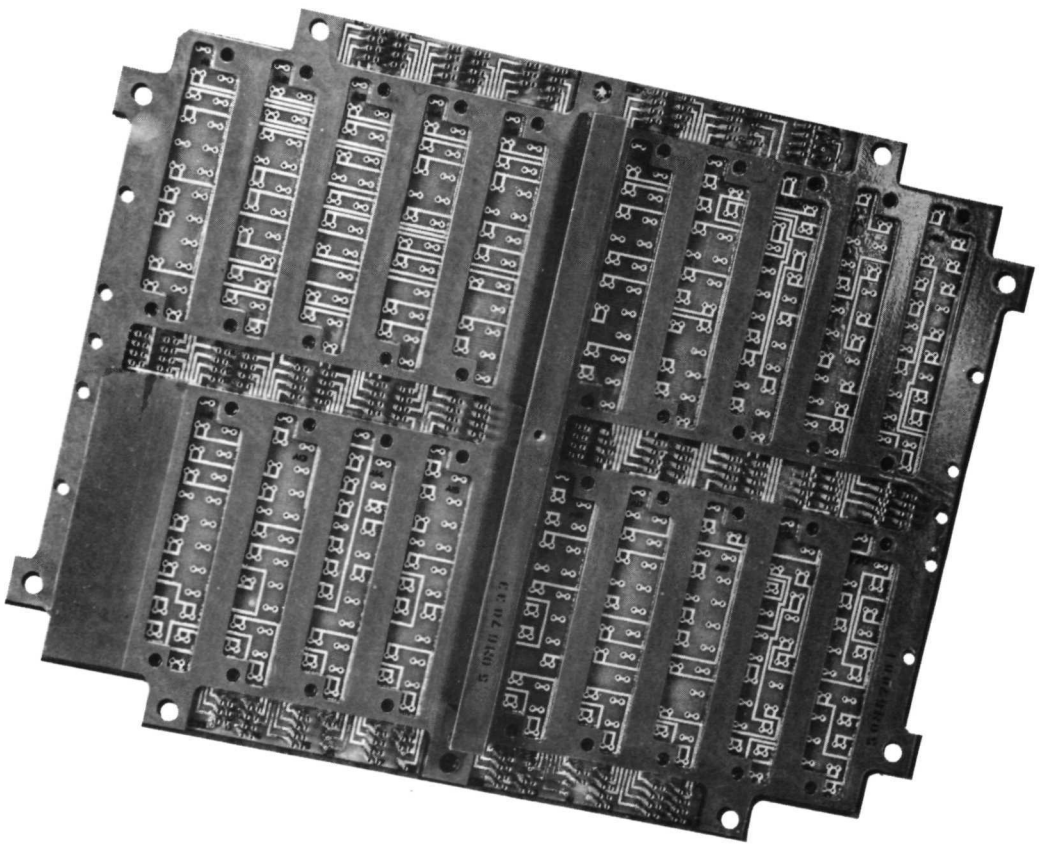

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Figure 1-3. Switch Selector Panel Assembly

Harness Assembly

The harness is a conventional branched type utilizing 26 AWG tinned copper, polyolefin insulated, wire. The harness is layed out, formed, laced, and unit connectors attached prior to installation on the electrical assembly.

Harness wires are dual redundant for increased reliability. At the unit connector, each pair of redundant wires is terminated in one contact with a crimp and a solder connection. The back of the unit connectors are potted with a polyurethane compound to provide a seal and strain relief for the wires.

Electrical Assembly

The electrical assembly (see Figure 1-4) combines the harness, circuit modules, and the two panel assemblies on a frame for pre-acceptance electrical test prior to insertion of the assembly into the unit housing.

The panels are arranged so that the bottom sides face each other. The harness is assembled to the top side of each panel assembly and laced to the harness supports. The harness wires are inserted through a hole in the center of each connection terminal and soldered on the bottom side of the panel assembly. Shrink sleeving, assembled over the harness wire and terminal, provides strain relief on the wire. The harness assembly is branched at one end of the panel assemblies so that the panel assemblies may be opened to 90° for the solder operations and inspection.

The circuit modules are mounted on top of the heat sink. Each module is secured with 2 screws through the printed wiring board and the heat sink to the threaded inserts in the module connector. The module pins extend through the "plated through" holes in the printed wiring board and are soldered from the bottom side of the printed wiring board.

There are 19 circuit modules and a filter mounted on the top panel assembly and 15 circuit modules and a filter mounted on the bottom panel assembly. The filters are the same size as a circuit module. Each filter is secured with 4 screws to the panel assembly. Harness wires are soldered to 4 terminals on each end of the filter. Stage +28 Vdc and stage common (ground) are inputs to the unit in a common shield to one line filter. IU +28 Vdc and signal return (ground) are inputs to the unit in a common shield to the other line filter. These are the only shielded wires in the unit.

Six magnesium rails are bolted together to form a mounting frame. The frame is inserted between the bottom surfaces of the panel assemblies.

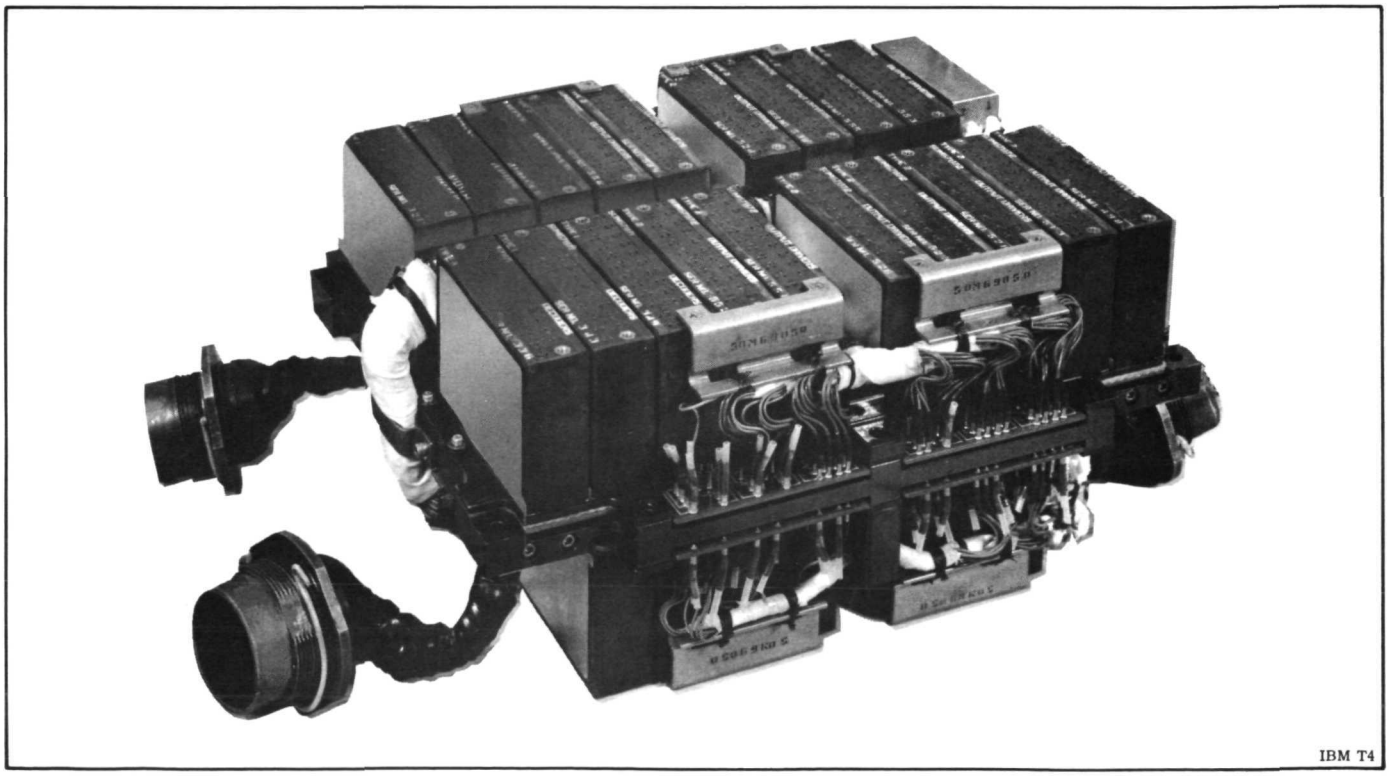


Figure 1-4. Switch Selector Electrical Assembly

The panel assemblies are bolted to the frame. A temporary test harness is attached to the electrical assembly for pre-acceptance testing. The test harness wires are attached to 61 terminals on the panel assemblies in the same manner as the system harness. After completion of pre-acceptance test, the test harness wires are cut off just above the test terminals and the harness is removed. Shrink sleeving is applied over the test terminals to seal them.

Housing, Cover, and Gasket

The component housing is a magnesium alloy casting. There are four unit mounting bosses with 0.281-inch diameter mounting holes at each corner of the casting. The bottom of the bosses is on the same plane as the bottom surface of the casting. The bosses are 0.250 inch thick. There are mounting holes for a 32-contact connector, a 62-contact connector, a pressure relief valve, and a purging valve in one end of the casting. In the other end of the casting there are mounting holes for a 32-contact connector, a 61-contact connector, and a purging valve. The top edge of the four side walls of the casting have 32 tapped holes for cover mounting. Inside the casting there are ten bosses which extend from the bottom surface and side walls. These bosses have one tapped hole in each for mounting the electrical assembly. On the bottom inside surface of the casting, four silicone sponge pads are bonded with adhesive. These pads are compressed by the circuit modules when the electrical assembly is inserted and thereby provide additional support and dampening under mechanical environment. The casting is treated with iridite and coated with aluminum paint.

The unit cover is a machined magnesuim alloy plate with 32 clearance holes for mounting. Four silicone pads are bonded to the bottom surface of the cover. These pads are compressed when the cover is assembled to the housing by the circuit modules of the electrical assembly and serve the same purpose as the pads inside the housing. The cover is treated with iridite and painted with aluminum paint.

The cover gasket material is silicone filled stainless steel which provides both a pressure seal and RFI shielding. The gasket is 0.062 inch thick by 0.312 inch wide and forms a rectangle to fit the top edge of the housing. There are 32 clearance holes for the cover mounting screws.

Component Assembly

The electrical assembly is inserted through the top of the housing (see Figure 1-5). The harness

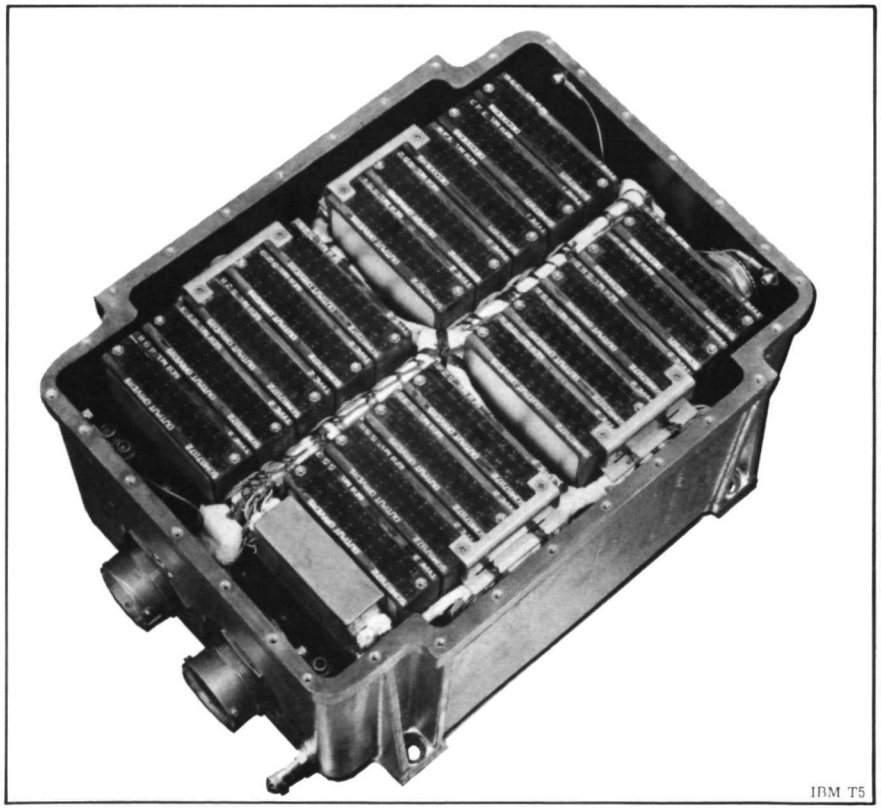


Figure 1-5. Switch Selector, Model II (Internal View)

connectors are drawn through their mounting holes and secured with hexagonal nuts and safety wire. The electrical assembly is bolted in 10 places to the bosses in the bottom of the housing. The shield ground wires are secured to the inside surface of the housing wall with screws and lock washers. The pressure relief valve, which is preset for a "cracking" pressure of 10 psi, and the two purging valves are assembled in their mounting holes. The cover gasket and cover are mounted on top of the housing and secured with 32 screws.

1-4 ELECTRICAL CHARACTERISTICS

The electrical characteristics of the Switch Selector Model II are specified in Table 1-2.

1-5 DIMENSIONS AND WEIGHT

The Switch Selector has the following physical characteristics:

Height:	5.29 inches maximum
Width:	8.56 inches maximum
Length:	12.50 inches maximum
Weight:	19.8 pounds (approx)

Table 1-2. Electrical Characteristics

Input Voltages	
Verification	28 ±4 Vdc
Stage supply voltage	28 ±2 Vdc
Input Power	
Peak	17.6 Watts
Standby	1.9 Watts
Input Signals	
Stage select Read command Reset 8-bit coded input	Up level: 17.5 Vdc (min) to 32.0 Vdc (max) Down level: open circuit clamped to gnd for negative suppression.
Output Signals	
Register verification	28 Vdc
Channel outputs	28 Vdc
Zero indicate	28 Vdc
Register test	28 Vdc
Telemetry	
No channel active	0.2 Vdc
One channel active	2.0 Vdc
More than one channel active	3.0 Vdc
Operating Temperature	-25 °C (-13 °F) to +100 °C (+212 °F) in a partial vacuum of not greater than 10^{-4} mm of mercury.
Electrical Isolation	100 Megohms between all points not connected by a conductor.
Heat Dissipation	3.0 Watts

SECTION II

PRINCIPLES OF OPERATION

2-1 GENERAL OPERATION

2-2 SYSTEM DESCRIPTION

Each stage, and the Instrument Unit, of the Saturn Launch Vehicle are equipped with a Switch Selector. The Switch Selector consists of electronic and electromechanical components which decode digital flight sequence commands from the LVDA/ LVDC and activate the proper stage circuits to execute the commands.

Each Switch Selector can activate, one at a time, 112 different circuits in its stage. The selection of a particular stage Switch Selector is accomplished through the command code. Coding of flight sequence commands and decoding of the stage Switch Selectors reduces the number of interface lines between stages and increases the flexibility of the system with respect to timing and sequence. In the Saturn V Launch Vehicle, which contains 4 Switch Selectors, 448 different functions can be controlled using only 28 lines from the LVDA. (Two IU + 28-volt and two signal return lines from the Control Distributor are also used.) Flight sequence commands may be issued at time intervals of 100 milliseconds.

Figure 2-1 illustrates the Saturn V Switch Selector configuration. As shown, all Switch Selector control lines are connected through the Control Distributor in the IU to the LVDA and the electrical support equipment.

To maintain power isolation between vehicle stages, the Switch Selector is divided into two sections: The input section (relay circuits) of each Switch Selector receives its power from the IU; the output section (decoding circuitry and drivers) of each Switch Selector receives its power from the stage in which the Switch Selector is located. The input and output are coupled together through a diode matrix. This matrix decodes the 8-bit input code and activates a PNP output driver, thus producing a Switch Selector output.

Each Switch Selector is connected to the LVDA through 28 lines:

- Stage select lines - 8
- Read command lines - 2
- Reset (forced) lines - 2
- Bit register output lines - 8
- Verification lines - 8

In addition, there are 2 lines for IU +28 Vdc and 2 lines for signal return between the Control Distributor and the Switch Selectors.

The wire pairs for stage select, read command, forced reset, IU + 28 Vdc, and signal return are redundant. Only one of each pair is required for normal operation.

All connections between the LVDA and the Switch Selectors, with the exception of the stage select inputs, are connected in parallel as shown in Figure 2-2.

The output signals of the LVDA switch selector register, with the exception of the 8-bit command, are sampled at the Control Distributor in the IU and sent to IU PCM telemetry. Each Switch Selector also provides 3 outputs to the telemetry system within its stage.

The Switch Selector is designed to execute flight sequence commands given by the 8-bit code or by its complement. This feature increases reliability and permits operation of the system despite certain failures in the LVDA switch selector register, line drivers, interface cabling, or Switch Selector relays.

The flight sequence commands are stored in the LVDC memory and are issued according to the flight program. When a Programmed Input/Output (PIO) instruction is given, the LVDC loads the 15-bit switch selector register with the computer data. The LVDA switch selector register word format is shown in Figure 2-3.

Switch selector register bits 1 through 8 represent the flight sequence command. Bits 9 through 13 select the Switch Selector to be activated. Bit 14 resets all the relays in the Switch Selectors in the event data transfer is incorrect as indicated by faulty verification information received by the LVDA. Bit 15 activates the addressed Switch Selector for execution of the command. The LVDC loads the switch selector register in two passes; bits 1 through 13 are loaded during the first pass and, depending on the feedback code, either bit 14 or bit 15 is loaded during the second pass.

After the Switch Selector input relays have been "picked" by the 8-bit command, the complement of the received code is sent back to the LVDA/LVDC over eight parallel lines. The feedback (verification information) is returned to the digital input multiplexer of the LVDA and is subsequently compared with the original code in the LVDC. If the feedback agrees with the original code, a read command is given. If the feedback does not agree with the original code, a reset command is given (forced reset), and the LVDC/LVDA reissues the 8-bit command in complement form.

A typical operation cycle, to initiate a given function in a particular stage, is accomplished as follows:

- The 8 verify lines are sampled to ensure that all stage select relays have been reset, thereby ensuring an unwanted stage is not selected. Zero voltage on all lines indicates that this condition exists. The presence of IU + 28 Vdc on the verify lines indicates that the verify lines are enabled because a stage Switch Selector is not reset. Having detected this situation, the LVDC commands a "force reset" and then rechecks the verify lines.
- The LVDC inserts the 8-bit flight command into the LVDA switch selector register. At the same time, a stage select command is sent to the appropriate Switch Selector. Application of the stage select command completes the signal return path for the input relays and allows the 8-bit command to be stored in the Switch Selector input relays.
- The verification lines are sampled to determine if the command transfer was correct.
- If the verification is correct, the LVDC sends a read command to the Switch Selector; activating it, and causing the proper output to occur.
- If the verification is not correct, the LVDC initiates a reset command to prepare the Switch Selector to receive the complement of the original command.
- After the forced reset is completed, the LVDC loads the stage select command, and the complement of the previously sent command, into the LVDA switch selector register.
- Neglecting the verification information that occurs after the complement command is inserted, the LVDC initiates a read command which produces an output from the selected switch selector channel. The read command also energizes the automatic reset circuitry which returns the Switch Selector to the reset condition to prepare it for a new cycle.

2-3 COMPONENT DESCRIPTION

A description of Switch Selector operation is given in the following paragraphs (refer to the simplified schematic diagram shown in Figure 2-4). The circuit functions of the Switch Selector are as follows:

Stage select

Input relays

Verification

Reset (forced)

Read command

Reset (automatic)

Decoding matrix

Output matrix and telemetry

Test outputs

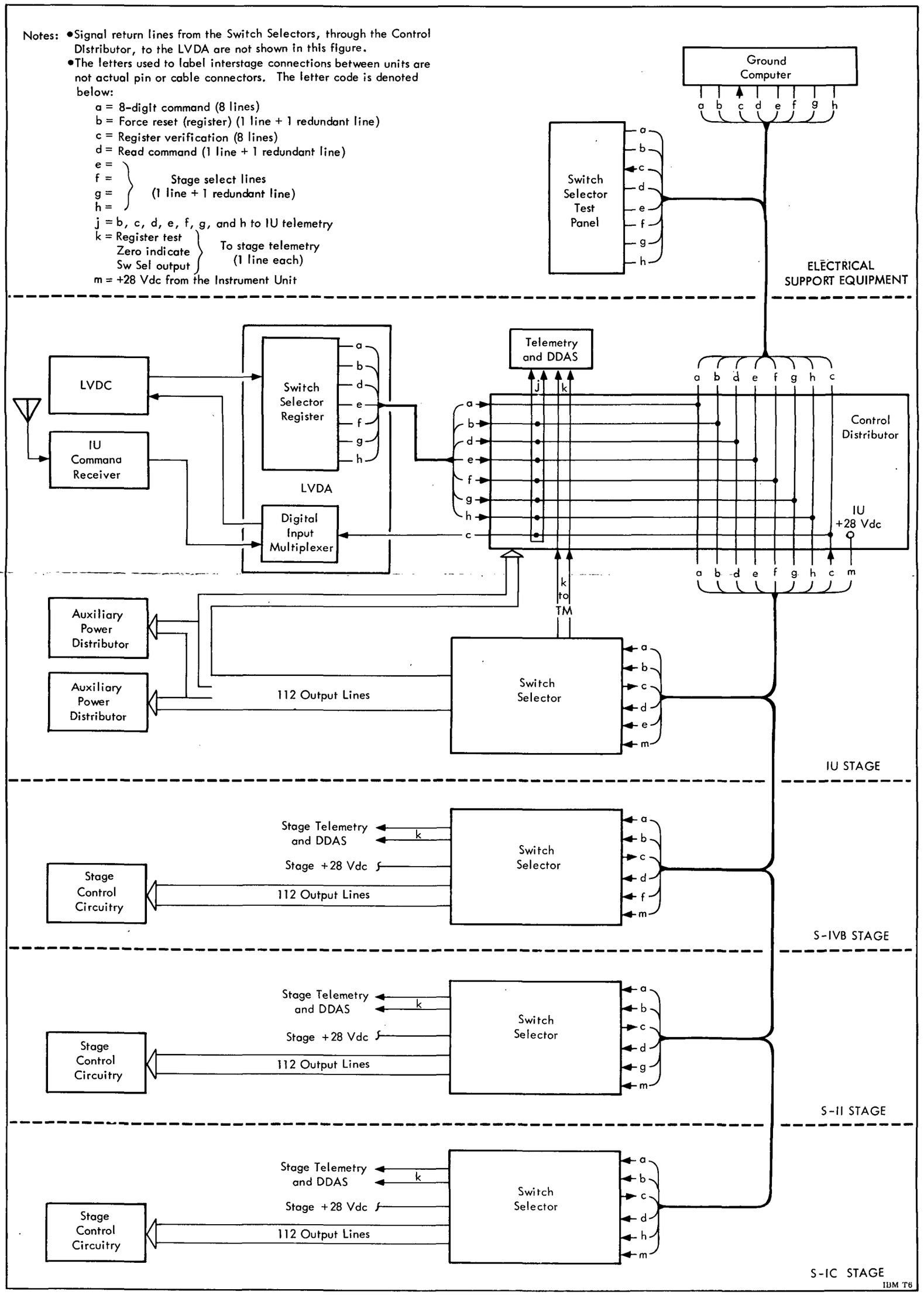


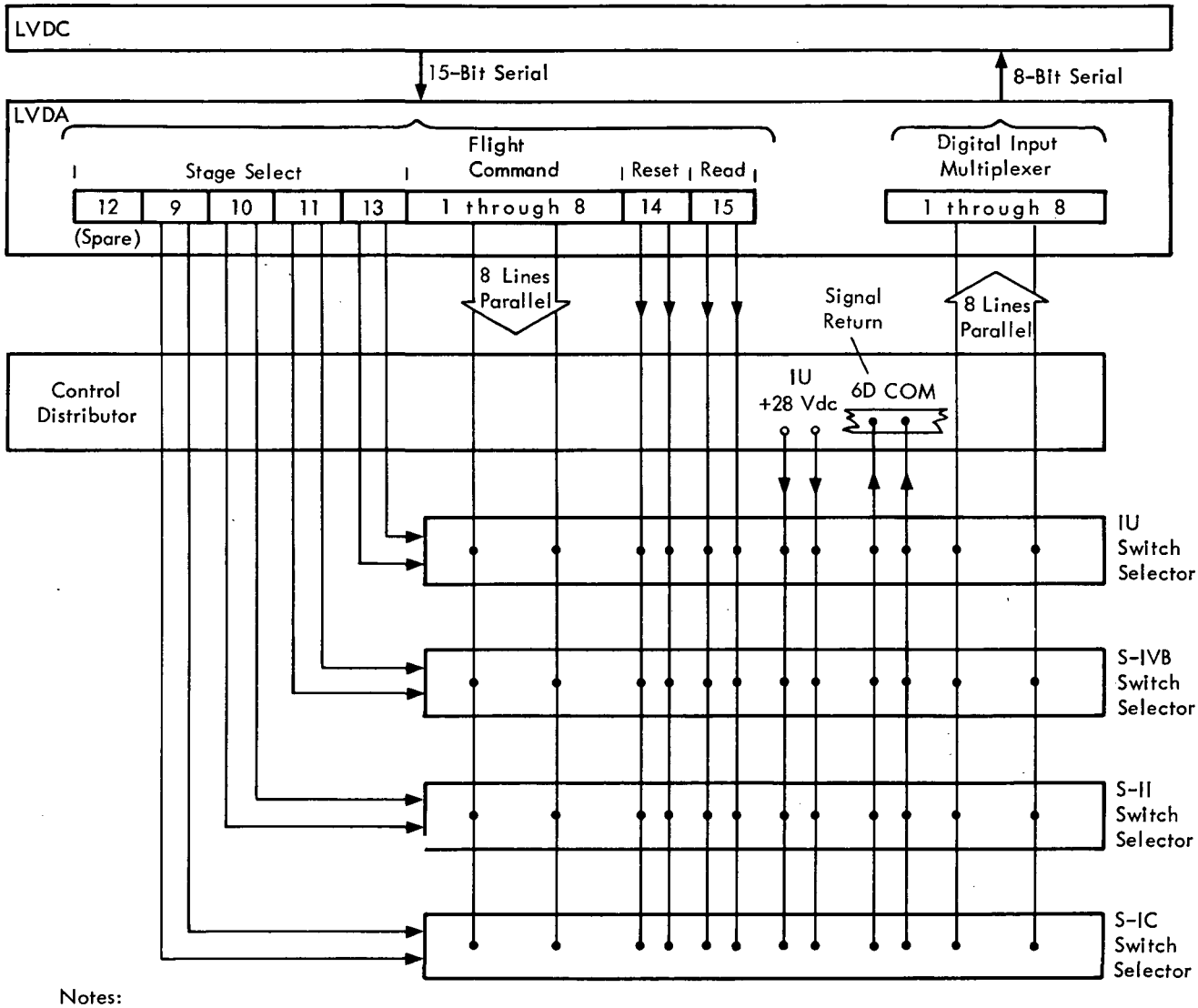
Figure 2-1. Saturn V Switch Selector Configuration

The Switch Selector operates on positive logic (i. e., + 28 Vdc for a binary "1" and 0 Vdc for a binary "0").

Stage Select

The purpose of the stage select command is to enable the desired Switch Selector to receive the coded flight sequence command from the LVDA. The stage select command (1 bit) is transmitted individually on a separate line to each Switch Selector. Because of the danger of overloading the LVDA, no more than 2 Switch Selectors can be addressed simultaneously.

The stage select command sets three magnetic latch relays in the addressed Switch Selector. The setting of these relays completes a ground path



Notes:

1. 22 lines between each Switch Selector and LVDA.
2. 26 lines between all Switch Selectors and LVDA (Saturn IB) (3 Switch Selectors).
3. 28 lines between all Switch Selectors and LVDA (Saturn V) (4 Switch Selectors).
4. 30 lines (maximum number) available to Switch Selectors from LVDA (5 Switch Selectors).
5. 4 lines (IU +28 Vdc and signal return) to all Switch Selectors from Control Distributor (Saturn IB and V).

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Figure 2-2. LVDC - Switch Selector Interconnection Diagram

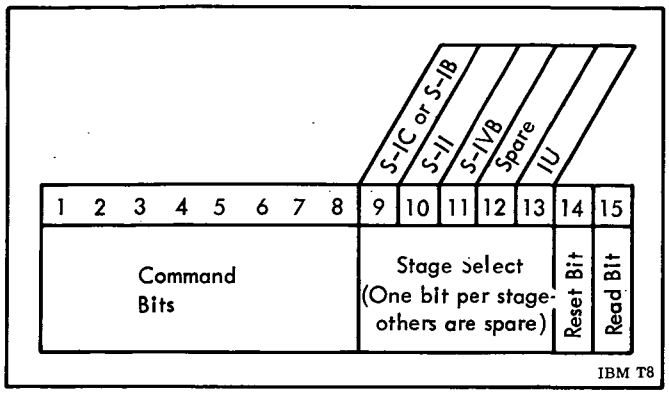


Figure 2-3. Switch Selector Register Word Format

for the read command relay, the set side of the input relays, and the verify power relay (see Figure 2-4). This action conditions the read and input relays to receive commands from the LVDA and energizes the verify power relay. When the verify power relay contacts close, IU + 28 Vdc power is applied through a set of stage select contacts to the verify relay contacts; and stage + 28 Vdc is applied to the verify relays. The Switch Selector can now accept the 8-bit command from the LVDA, store it in the input relays, and make verification information available to the LVDA.

Input Relays

The input register of the Switch Selector is made up of eight magnetic latch relays, controlled by the 8-bit coded command from the LVDA. The coded command (consisting of 8 bits in parallel) is available to the Switch Selector during the same period of time the stage select signal is present. As soon as the stage select relays are set, a signal return path is provided for the coded command through the input relay coils (see Figure 2-4). This allows the coded command to be stored in the input register.

Once the coded command is stored in the input register, binary information is available to the verification register, column decoder, row decoder, and the AND gate generator.

Verification

A feedback circuit is used to provide verification information back to the LVDC. This circuit consists of 8 relays, and is controlled by the input relay contacts. When a "1" is applied to the input relay set coil, stage ground is switched to the verify relay set coil causing the normally closed verify relay contact to open; indicating a "0" to the LVDC. When a "0" is applied to the input relay set coil, the input relay contacts remain in the reset condition. Stage ground remains applied to one side of the verify relay reset coil, causing the verify relay contact to remain in its normally closed position. Therefore, the verification output of a Switch Selector is the complement of the input command.

Read Command

Immediately after verification of the original command, the read command is initiated. If verification of the original command proved to be false, the read command will not be initiated by the LVDC until the forced reset, stage select, and complemented command have been transmitted to the Switch Selector.

Three conventional (non-latching) relays are picked when the read command is received from the LVDA. One side of the coils of these relays is connected to the read command signal, the other side is connected to the IU signal return through the stage select relay contacts. Thus, a stage select signal must have been received before a read command relay can be energized. When the read relay contacts close, stage ground is applied to the switch power inverters (SPWRA and SPWRC) in the decoder matrix. These inverters generate voltages (SPWRA and SPWRC) which activate the AND gate generators and the column decoder circuitry allowing the coded command to be decoded and an output to occur.

Reset (Forced)

A forced reset is initiated by the LVDC when the LVDC determines that the verification information is not the complement of the given command. The reset signal is applied to the forced reset relay coil causing the forced reset contacts to close. This action applies stage + 28 Vdc to the stage select and input relay reset coils forcing the Switch Selector into the reset condition shown in Figure 2-4. After the forced reset has been completed, the stage select command and the complement of the original flight sequence command are transmitted to the Switch Selector. The complement command is not verified by the LVDC before the read command is issued.

Reset (Automatic)

An automatic reset pulse is generated when stage power is initially applied to the Switch Selector and when the read command is issued. The

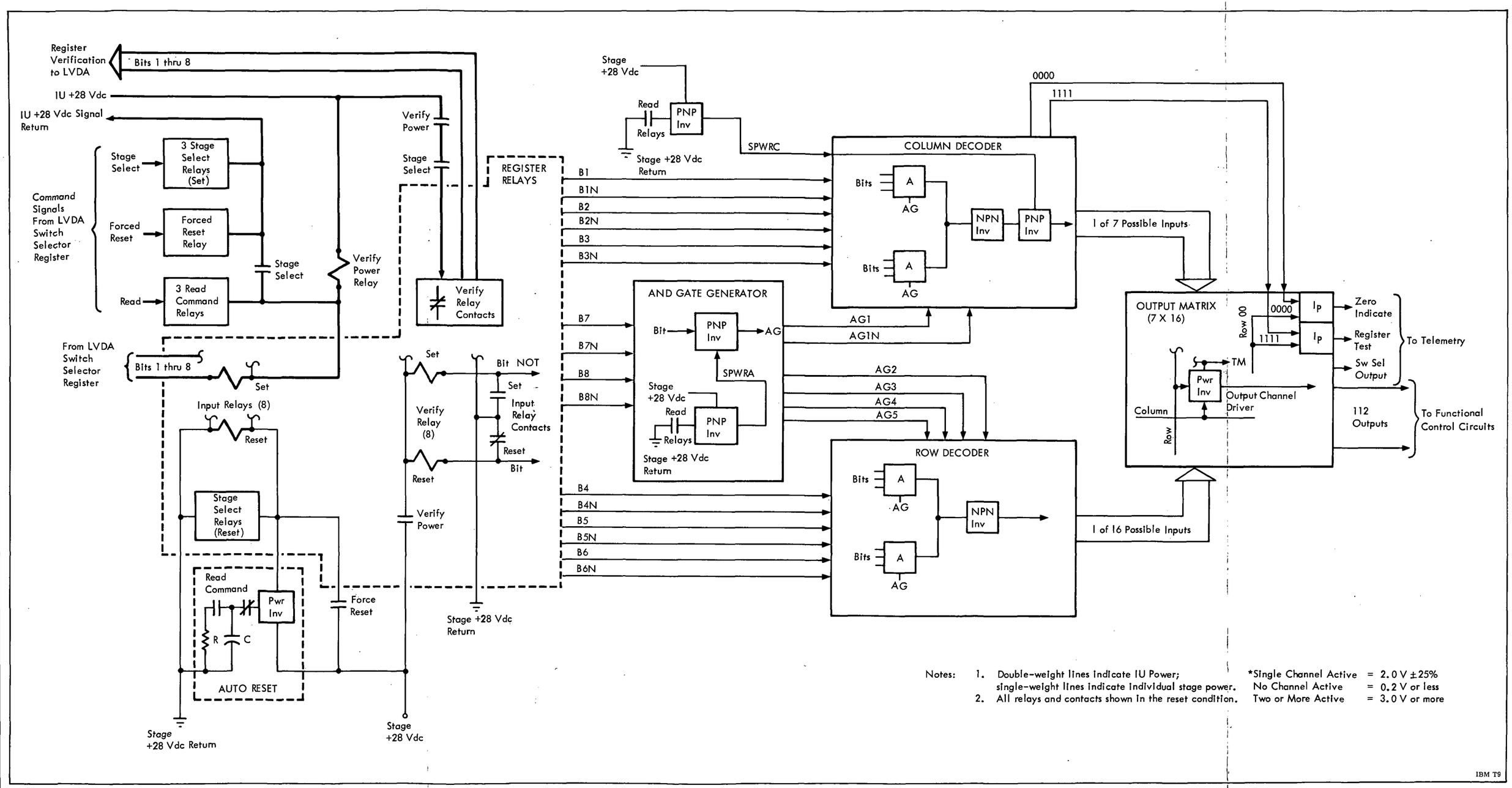


Figure 2-4. Switch Selector (Model II) Simplified Diagram

automatic reset circuitry consists of a power inverter, an RC network, and a set of read command contacts.

Activation of the read command relay contacts is not required to produce the "Power ON" reset pulse. Prior to the application of stage power to the Switch Selector, the read command contacts are in the reset condition (as shown in Figure 2-5) and capacitor C is in a discharged state. When power is applied to the Switch Selector, stage 28 Vdc is applied to the emitter of the power inverter and capacitor C begins to charge through base resistor (R3) and thermistor (RT1). Under these conditions the power inverter turns on, producing an output of approximately 28 Vdc at the collector. This output is applied across the input relay reset coils and the stage select reset coils forcing the Switch Selector into a reset condition.

The duration of the reset pulse is determined by the charge time of capacitor C through base resistor R3 and thermistor RT1. When C charges sufficiently, the power inverter is turned off and the reset pulse is removed from the reset coils.

The automatic reset pulse initiated by the read command is developed exactly the same as the "Power ON" reset pulse. When the read command is issued, the normally open read command relay contact closes, and the normally closed read command relay contact opens. This allows capacitor C to discharge through resistor R1. The power inverter remains turned off (due to lack of base drive)

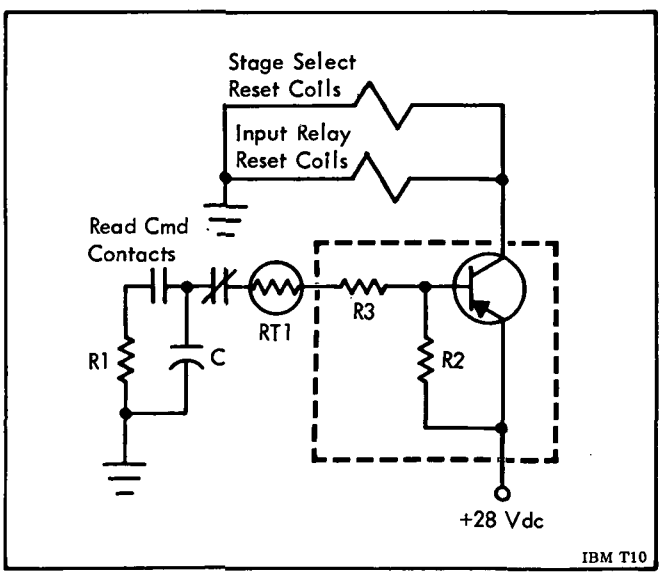


Figure 2-5. Automatic Reset Circuitry, Simplified Diagram

until the read command is removed. When the read command is removed, the read command relay contacts return to the reset condition. At this time, capacitor C begins to charge providing base drive for the power inverter. The power inverter turns on, producing an output of approximately 28 Vdc at the collector. The output is applied across the input relay and stage select relay reset coils forcing the Switch Selector into the reset condition as shown in Figure 2-4.

As previously stated, the duration of the reset pulse is determined by the charge time of capacitor C through base resistor R3 and thermistor RT1. When C is sufficiently charged, the power inverter is turned off and the reset pulse is removed from the reset coils.

Decoding Matrix

The decoding matrix is comprised of PNP inverters, NPN inverters, and AND circuits arranged so that selection of a particular output channel can be made by either the true or complement input code.

This matrix can be divided into three sections as follows (see Figure 2-4):

AND gate circuitry

Row decoder

Column decoder

The object of these circuits is to generate a particular column and row signal for each input code and to send these signals to the output matrix upon receipt of the read command signal.

The 8-bit coded command is transferred to the decoding matrix by operation of the input relay contacts. When a binary "1" is applied to an input relay set coil, the normally open input relay contact closes and the normally closed input relay contact opens.

This causes stage ground to be switched from the verify relay reset coil to the verify relay set coil. The bit NOT input to the decoding matrix is now tied to stage ground, while the bit input line to the decoding matrix is at stage + 28 Vdc. When a binary "0" is applied to an input relay set coil, the input relay contacts remain in the reset condition. With the input relay contacts in the reset

condition, the bit NOT input to the decoding matrix is at stage + 28 Vdc and the bit input to the decoding matrix is a 0 Vdc.

The 8-bit command is sub-divided into groups for decoding and output driver selection. The least three significant bits (1, 2 and 3) are decoded to enable the column selection circuitry. The next three bits (4, 5 and 6) are decoded to enable the row selection circuitry. Bits 7 and 8 and SPWRA (controlled by read command relays) are applied to the AND gate generator where they are decoded to supply the appropriate AND gates to the column and row decoders. Bit 8 is applied to the AND gate generator where it is decoded to determine whether the coded command is a true or complement word. The listing below illustrates the Boolean expressions for decoding bits 7 and 8.

$$AG1 = B8 \cdot \text{Read Command}$$
$$AG1N = B8N \cdot \text{Read Command}$$
$$AG2 = AG1 \cdot B7$$
$$AG3 = AG1 \cdot B7N$$
$$AG4 = AG1N \cdot B7N$$
$$AG5 = AG1N \cdot B7$$

where: B8 = Bit 8 = Bit 8 is a binary "1".

B8N = Bit 8 NOT = Bit 8 is a binary "0".

When decoding a typical word (01010101) where bits 8 through 1 are arranged from left to right, the column is determined by bits 8, 3, 2 and 1, or 0101, or more completely by $AG1N \cdot B3 \cdot B2N \cdot B1$. Similarly, the row is determined by bits 8, 7, 6, 5, and 4, or 01010, or more completely $AG5 \cdot B6N \cdot B5 \cdot B4N$. However, if the input register transfer circuitry shows a failure, the complement of the original word must select the same output channel in the output matrix. Therefore, the location defined by 01010101 must also be defined by 10101010. This complement code is decoded in the same manner as the original code. The column is determined by bits 8, 3, 2, and 1, or 1010, or more completely by $AG1 \cdot B3N \cdot B2 \cdot B1N$. The row is determined by 8, 7, 6, 5, and 4, or 10101, or more completely by $AG3 \cdot B6 \cdot B5N \cdot B4$. Therefore, the total expression to define this particular output channel is:

$$\text{Channel XY} = AG1N \cdot AG5 \cdot B6N \cdot B5 \cdot B4N \cdot B3 \cdot B2N \cdot B1 + AG1 \cdot AG3 \cdot B6 \cdot B5N \cdot B4 \cdot B3N \cdot B2 \cdot B1N$$

Output Matrix and Telemetry

The 112 output channels of the Switch Selector are arranged in a 7 by 16 matrix configuration (7 columns and 16 rows). The coordinate selection is similar to the X-Y coincidence method common to core memory technology. An output channel driver (PNP inverter) with the location X-Y in the matrix is activated when the row decoder circuitry (X) and the column decoder circuitry (Y) are turned ON by application of the read command. When activated, the output channel driver produces a + 28 Vdc output to the control circuitry of the selected function.

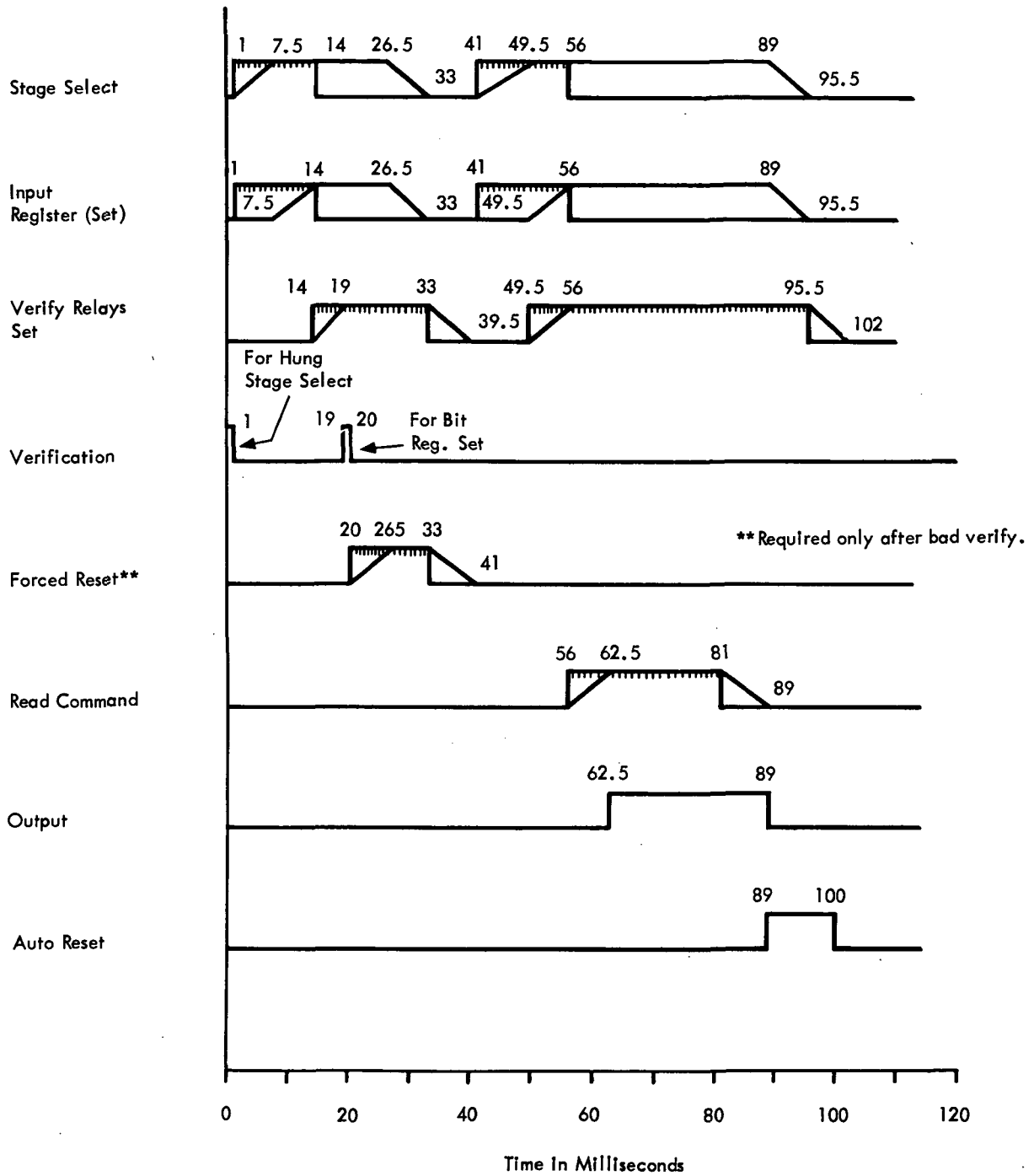
In addition to producing an output voltage, each output channel driver also produces a separate telemetry output. The 112 telemetry outputs are tied together to produce one switch selector telemetry output signal. This signal is transmitted via PCM and DDAS telemetry. The telemetry signal indicates whether none, one, or more than one output channel is ON at any given time. If one output channel is activated, the telemetry signal will have a magnitude of 2.0 Vdc ± 20 per cent; if no output channel is active, the telemetry signal will have a magnitude of 0.2 Vdc or less; and if more than one output channel is activated, the telemetry signal will have a magnitude of 3.0 Vdc or more. When the Switch Selector is operating properly, only one output channel will be active an any given time.

Test Outputs

In addition to the telemetry output described, each Switch Selector has two telemetry outputs which are used to verify that the input selection relays can be set and reset properly. These signals (register test and zero indicate) are special outputs of the output matrix. The register test output is generated by an output driver when the input address selection is all ones and the read command has been issued. The zero indicate output is generated when the input address selection is all zeros (read command is not required). The zero indicate and register test signals are transmitted via PCM and DDAS telemetry.

2-4 DETAILED OPERATION

This section contains a more detailed description of the Switch Selector. During this discussion, reference will be made to the timing diagram, Figure 2-6, the simplified schematic diagrams, Figures 2-7 through 2-15, and to the detailed schematic diagram, Figure 2-16.



Notes:

1. Register set is delayed because it requires stage select to provide ground return.
2. Latching relays remain set after power is removed. They remain set until their reset coils are energized.
3. Relay pick and fall times reflect high temperature conditions (125°C).

Indicates voltage is applied to relay set coils

Indicates relay switching. Relay may be in either state during slope time.

IBM T11

Figure 2-6. Typical Switch Selector Timing Diagram

2-5 STAGE SELECT

The stage select command is the signal which conditions a particular Switch Selector to receive the flight sequence command from the LVDA. Stage select relays K20, K21, and K22 (see Figure 2-16) are magnetic latch relays. One side of each relay coil is attached to the input line carrying the stage select command from the LVDA. The other side of each coil is connected to IU signal return.

Application of the stage select command energizes the set coils of the stage select relays. After a 5-millisecond relay pick time, the stage select relay contacts close (see Figure 2-6). Closure of contacts K20-2, K21-1, K21-2 and K22-2 (see Figure 2-16) complete the circuits for (1) the input relays (K1S through K8S), (2) the read relays (K17, K18, K19), and (3) the verify power relay (K24), by tying one side of the relay coils to IU signal return. When relay K24 is energized, contacts K24-2 close completing the circuit that applies stage + 28 Vdc to one side of the set and reset coils of the verify relays (K9 through K16). Operation of relay contacts K22-1 and K24-1 results in IU + 28 Vdc being applied to the contacts of the verify relays (K9 through K16). Thus, operation of the stage select relays allows the 8-bit flight sequence command to be stored in the input relays and prepares the Switch Selector to generate verification information.

The stage select relays are double-pole, double-throw relays which are wired in a modified triple modular redundant configuration (see Figure 2-7).

This configuration will allow any one of the coils or contacts to fail and still provides a means to effect the desired function. It can be seen that transfer is effected by the proper operation of either K21-1 and K20-2, K22-2 and K21-2, or K20-2 and K22-2 and the diodes. The diodes prevent a failure in the event relay contacts K21-1 and K21-2 fail to open during the reset cycle.

The remaining set of stage select contacts, K22-1, is wired in a simplex configuration (see Figure 2-16). This set of contacts does not require additional redundancy because of the true and complement decoding capability of the Switch Selector. If K22-1 fails to close upon command, the Switch Selector will lose its verify capability and be forced to operate in the complement mode. Stage select contacts K20-1 are not used.

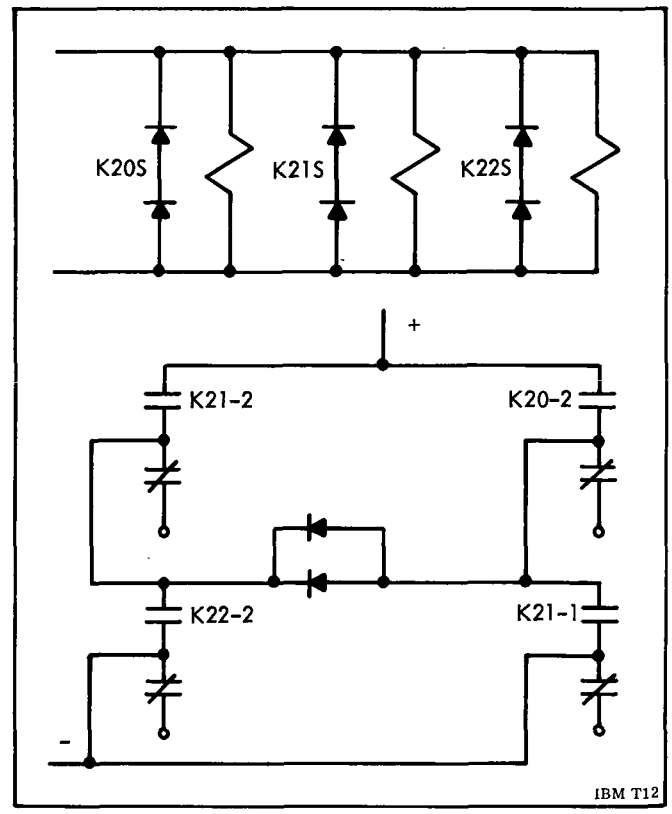


Figure 2-7. Stage Select Relay Configuration

2-6 INPUT RELAYS

The input relays (K1 through K8) are the relays which receive the coded address from the LVDA (see Figure 2-8). The set coils of these relays are wired between the switch selector register in the LVDA and IU signal return. The reset coils are wired in parallel between stage ground and two separate sources of reset power; the PNP inverters in the automatic reset circuit and stage + 28 Vdc via the forced reset relay contacts K23-1 and K23-2. The contacts of the input relays are located between the decoding matrix and the verify relay coils. Therefore, the condition of the input relay contacts (set or reset) determines the input to the decode matrix and the operation of the verify relay set and reset coils.

The input relay contacts are connected to the verify relay set and reset coils as follows:

Input Relay Contacts	Verify Relay Coil Energized
Reset closed: Set open	Reset
Reset open : Set closed	Set

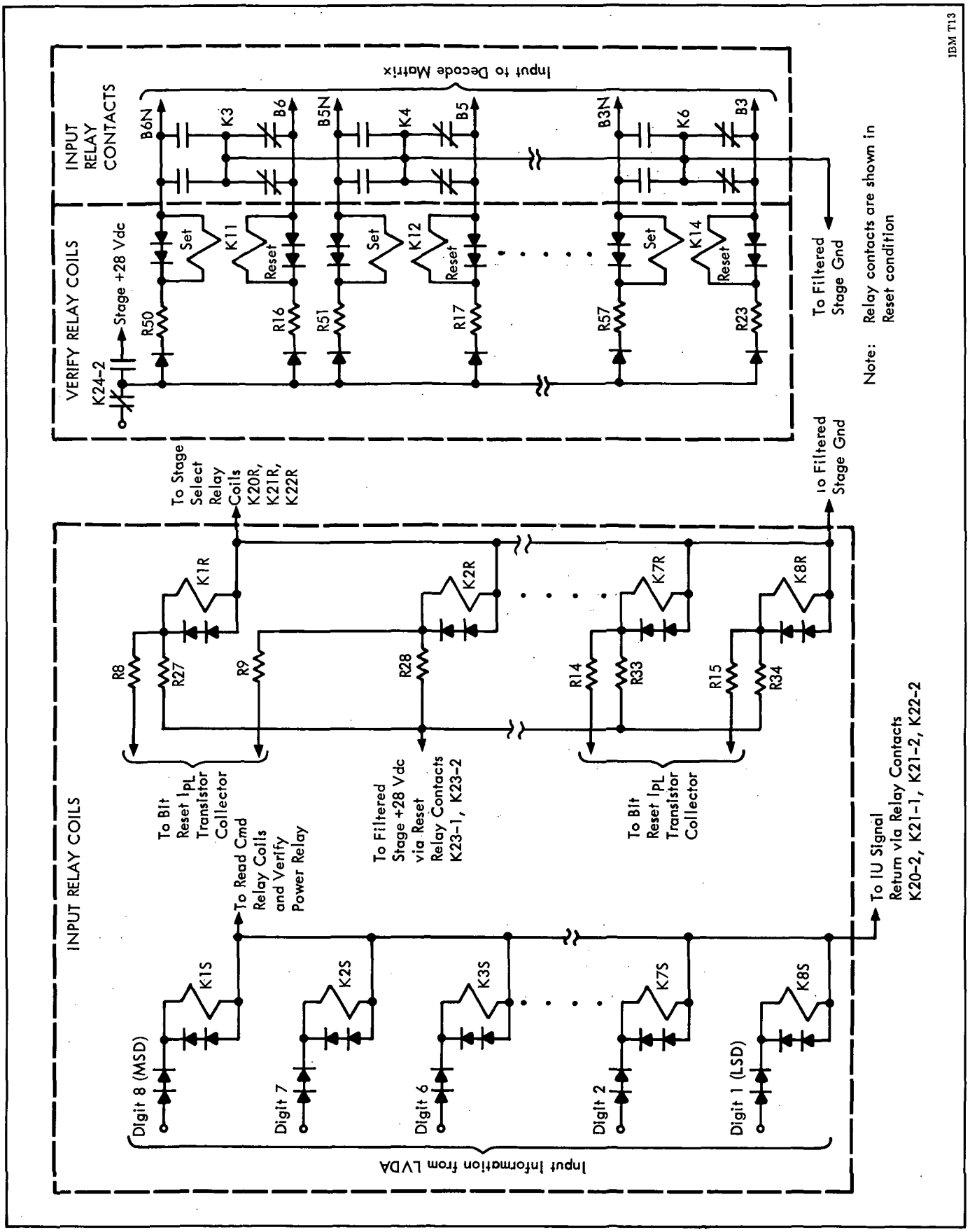


Figure 2-8. Input and Verify Relay Circuitry

The input relay contacts connect stage ground to one side of either the set or reset coils of the verify relays. This completes the circuit through the coils to stage + 28 Vdc, thereby providing verification information to the LVDA. In addition, the input relay contacts determine how the bit and bit NOT input lines to the decode matrix are conditioned. The following table shows the relationship between the input relay contacts and the inputs to the decode matrix.

Input Relay Contacts	Bit Function	Bit NOT Function
Reset closed: Set open	Down level (0 Vdc)	Up level (+28 Vdc)
Reset open: Set closed	Up level (+28 Vdc)	Down level (0 Vdc)

A down level voltage is obtained on a decode matrix input line when that line is tied to stage ground through the input relay contacts, and an up level voltage exists on the matrix input line which is not tied to stage ground. In the event relay contact K24-2 fails to close, an open circuit at the input to the decode matrix is considered to be an up level voltage.

It should be noted that the stage select command and the coded input command are sent from the LVDA at the same time (see Figure 2-6). However, the input relays will not pick until a maximum of 6.5 milliseconds after the initiation of these signals. The delay is due to the pick time of the stage select relays. It then takes a maximum of 6.5 milliseconds to pick the input relays. This means that after a maximum of 13 milliseconds after initial receipt of the stage select command, power will be applied to the verify relay coils. The power is applied in such a manner that the information contained in the verify relay coils is the coded input command held in the input relays.

The input relays are wired in a simplex configuration. Redundancy is provided by the true or complement decoding capability of the Switch Selector.

Resetting of the input relays will be discussed later under the headings RESET (FORCED) and RESET (AUTOMATIC).

2-7 VERIFICATION

Verification is the process by which the Switch Selector automatically informs the LVDC (through the LVDA) that the correct input command is stored in the input relays of the Switch Selector.

This process is controlled by the operation of the stage select and input relays (see Figure 2-16). The stage select command results in stage + 28 Vdc being applied to the set and reset coils of the verify relays (K9 through K16) and IU + 28 Vdc being applied to the normally closed verify relay contacts (see paragraph 2-5, STAGE SELECT). The coded input address results in the input relay contacts being set to reflect the input address. Upon successful acceptance of the stage select command and the input address, the Switch Selector is fully conditioned to send verification information to the LVDA.

The information sent to the LVDA is determined by the condition of the input relay contacts (see Figure 2-8). When the input relay contacts are in the reset position, the verify relay reset coils are energized and the verify relay contacts remain in their normally closed position. When the input relay contacts are in the set position, the verify relay set coils are energized and the verify relay contacts are switched to the open position.

Thus, to energize the set coil of a verify relay, allowing no voltage to be sent to the LVDA, the corresponding input relay must be set, indicating a binary "1" for that particular bit of the input command. Conversely, to energize the reset coil of a verify relay, allowing + 28 Vdc to be sent to the LVDA, the corresponding input relay must be reset, indicating a binary "0" for that particular bit of the input command. The verification output is therefore the complement of the input command.

Power will be applied to the verification output circuitry a maximum of 13 milliseconds after receipt of the stage select command (see Figure 2-6). However, the verification output for a given input command will not be present until a maximum of 18 milliseconds after the stage select command has been received. This is due to the relay pick times of the stage select, input, and verify relays.

2-8 RESET (FORCED)

One conventional double-pole, double-throw relay, K23, is used to control forced resetting of a

Switch Selector (see Figure 2-16). The forced reset command is issued only if a false verification has been received by the LVDC. When this occurs, it is necessary to clear the information stored in the input relays in order to prepare them to receive the complement of the original input command.

Forced reset is initiated upon receipt of the reset command from the LVDA. The reset command is applied to one side of the reset relay coil, K23. The other side is connected to IU signal return. When the coil of K23 is energized, normally open contacts K23-1 and K23-2 close, applying stage + 28 Vdc to one side of the stage select relay reset coils (K20R through K22R), and to one side of the input relay reset coils (K1R through K8R). Since relays K1R through K8R and K20R through K22R have the other side of their coils connected to stage ground, these relays will be reset. Series limiting resistors R24-R34 protect the reset relay coils agains current surges.

Resetting of the stage select and input relays results in stage ground being applied to the verify relay reset coils K9R through K16R, and power being removed from verify power relay K24. Under these conditions power will be applied to the verify relay reset coils for a period of time equal to the relay fall time of K24. During this time, the verify relays (K9 through K16) will be reset. The Switch Selector is now reset and ready to receive the complement of the original command. The reset cycle is completed 19. 5 milliseconds after application of the forced reset command (see Figure 2-6).

2-9 READ COMMAND

The read command initiates two separate functions in the Switch Selector. First, the read command enables the decode matrix, allowing an output to be generated. Second, the read command initiates the automatic reset cycle.

Three conventional relays, K17 through K19, receive the read command from the LVDA (see Figure 2-16). One side of the relay coils is connected to the read command signal; the other side of the coils is tied to IU signal return through stage select relay contacts K20-2, K21-1, K21-2 and K22-2. Because the read command relays are connected to IU signal return through the stage select relays, it can be seen that a stage select command must be received by the Switch Selector before a read command can be accepted.

When the read relays are energized, the normally open contacts of K17-1, K18-1, K18-2, and K19-1 close resulting in stage ground being applied to the base circuits of the switch power inverters (SPWRA and SPWRC) in the AG portion of the decode matrix. This allows the decoding process to take place and an output to be generated. The Switch Selector output is present a maximum of 6. 5 milliseconds after receipt of the read command and remains until the read command is removed and the read command contacts open (see Figure 2-6).

The read relays are wired in a modified triple modular redundant configuration (see Figure 2-9). This configuration allows any one of the coils or contacts to fail and still provides a means by which the desired function can be accomplished. It can be seen that transfer is effected by the proper operation of either K18-2 and K19-1, K17-1 and K18-1, or K17-1 and K19-2 and the diodes. The diodes prevent a failure in the event relay contacts K18-1 and K18-2 remain closed after the read command has been removed.

Read relay contacts K17-2 and K19-2 are used to control the automatic reset circuitry. The automatic reset function will be discussed in the following paragraph.

2-10 RESET (AUTOMATIC)

Automatic reset is accomplished by a pulse generated within the Switch Selector. The pulse is

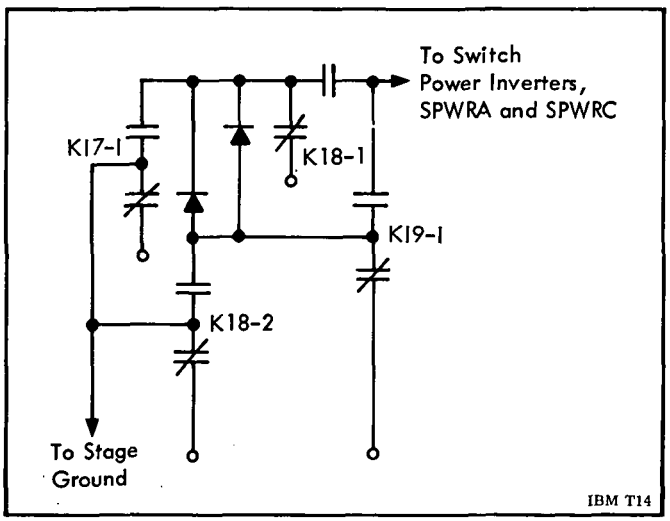


Figure 2-9. Read Command Relay Configuration

initiated by operation of read command relay contacts K17-2 and K19-2 and accomplishes the same function as the forced reset.

A series-parallel network of capacitors, C1 through C26, is connected as shown in Figure 2-10. One side of the network is tied to stage ground; the other side is connected to read command relay contacts K17-2 and K19-2. When these contacts are in their normally closed position, the capacitor network is connected through four parallel thermistors, RT1 through RT4, to the base circuits (A) of three parallel PNP inverters (IP_{LC}). (See paragraph 2-14 for a description of the inverter circuit.) If the capacitors are discharged, the inverters will be activated causing the output (B) to go to approximately stage + 28 Vdc. This condition allows the capacitors to charge to stage + 28 Vdc present at the gated input (C) of the inverters. The charge path is through the transistor, transistor base resistor, and the thermistors. The charge time is determined by the equivalent value of these resistances and the equivalent value of the capacitance of the capacitor network. When the capacitors have charged to a voltage equivalent to that needed to shut off the inverter, the voltage at B drops to 0 Vdc. The pulse thus generated at B of the inverters is the automatic reset pulse. These pulses are connected to reset coils K1R through K8R and K20R through K22R through series limiting resistors R5 through R15. The pulse width is equivalent to the time between turn ON and turn OFF of the inverters.

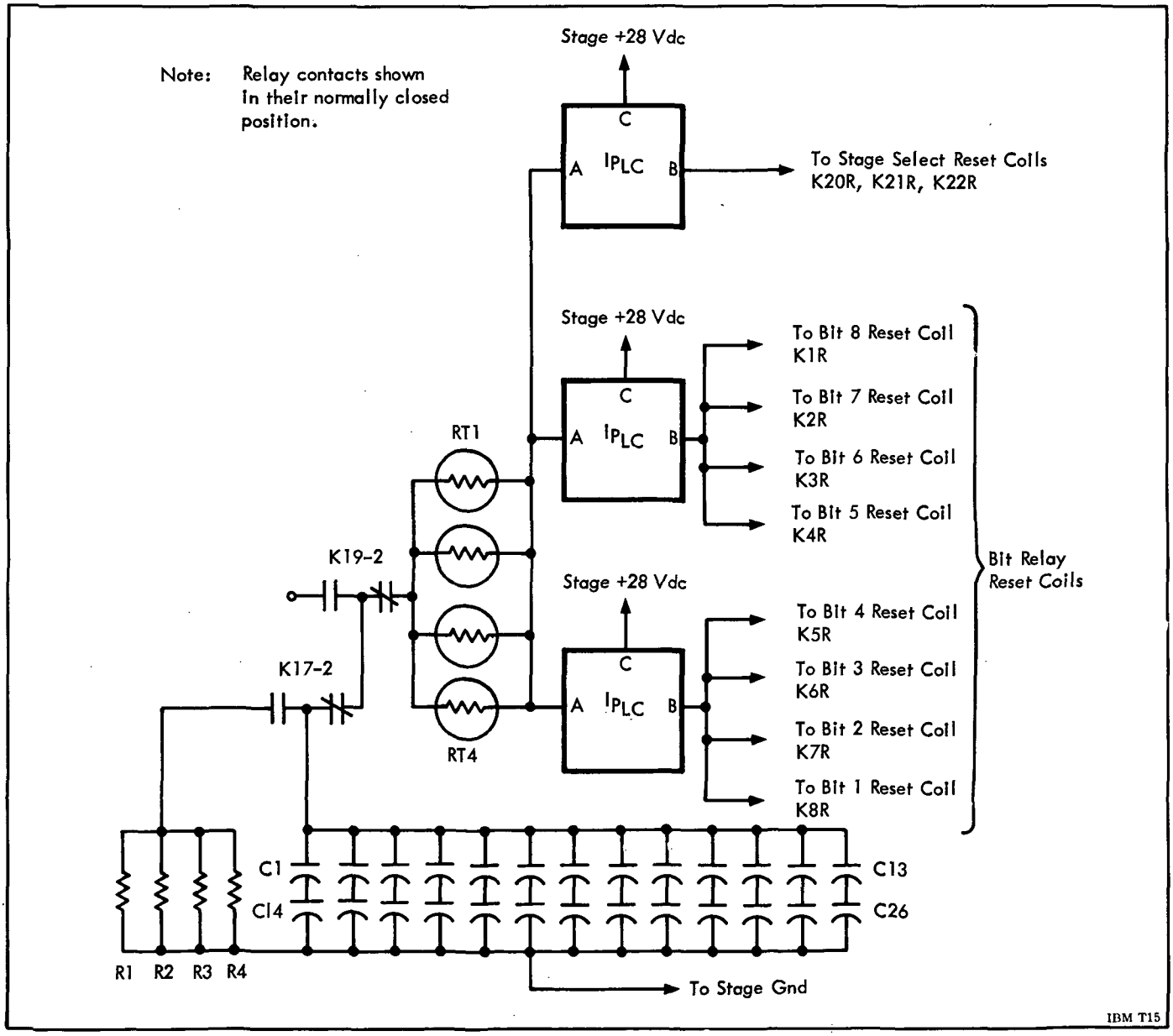


Figure 2-10. Automatic Reset Circuitry

The capacitor network is discharged through resistors R1 through R4 during the read command. When relay contacts K17-2 and K19-2 close, the high side of the capacitor network is connected to one side of the resistor network. The other side of the resistor network is tied to stage ground. The discharge time is determined by the RC time constant of the equivalent resistance of the resistor network and the equivalent capacitance of the capacitor network.

Because the output of the inverters (B) may vary with temperature, 4 thermistors, RT1 through RT4, were placed in the base circuits of the inverters. The thermistors compensate for output variations due to temperature change by adding or reducing resistance in the base circuit, thereby increasing or decreasing the base drive of the circuit as necessary. The effect of this compensation is to maintain a constant charge time and thereby maintain the width of the automatic reset pulse within the allowable design range of 3-1/2 to 12 milliseconds. The RC charge time determines the time duration between turn ON and turn OFF of the inverters.

The capacitor network was purposely made large so that a failure of one capacitor within the network can be tolerated without the automatic reset pulse width being forced out of tolerance, causing the Switch Selector to fail.

The automatic reset pulse commences 8 milliseconds after the read command has been removed (see Figure 2-6). This is due to the time required for the contacts of read command relays K17-2 and K19-2 to return to their normally closed positions.

2-11 DECODING MATRIX

The decoding matrix is comprised of PNP inverters, NPN inverters, and AND logic circuits (see paragraph 2-14 for description of electronic circuits). The circuits are arranged so that the input address can be decoded in either its true or complement form.

The output matrix is divided into three sections as follows:

AG generation logic

Row logic

Column logic

The object of these three sections is to generate column and row signals for each input code and to transfer these signals to the output matrix upon receipt of the read command.

AG Generation Logic

The AND gate circuitry (see Figure 2-11) develops the control signals for the output section of the Switch Selector. These signals (AG1 through AG5) are applied as gated inputs to the row and column decoders, which in turn condition the output matrix to produce the desired Switch Selector output.

Operation of the read command relays ties the inputs (A) of the switch power inverters to stage ground, resulting in the generation of the SPWRA and SPWRC signals.

The output of the SPWRA inverter is supplied as the gated input to the PNP inverters (I_{P_L}) that generate AG1 and AG1N signals. The binary value of bit 8 of the input code determines whether AG1 or AG1N is generated. Refer to paragraph 2-6, INPUT RELAYS, to determine the manner in which the input relays transfer the input code to the decoding matrix.

If bit 8 (B8) is a binary "1", approximately + 28 Vdc is applied to the input (A) of the I_{P_L} that generates AG1N. Since the input is + 28 Vdc, the inverter is turned OFF and the output (B) will be 0 Vdc, thus AG1N is a binary "0". If bit 8 (B8) is a binary "1", bit 8 NOT (B8N) is a binary "0" placing 0 Vdc on the input (A) of the inverter that generates AG1. With the input of the inverter at 0 Vdc, the inverter is turned ON and the output (B) will be + 28 Vdc, thus AG1 is a binary "1".

If the binary values of B8 and B8N are reversed, the inverter action described above will be reversed and the binary value of the AG1 signals will be reversed.

The AG1 and AG1N signals are sent to other I_{P_L}'s to generate the AG2 through AG5 signals. The AG1 signal is applied as the gated input to the I_{P_L}'s that generate the AG2 and AG3 signals. The AG1N signal is applied as the gated input to the I_{P_L}'s generating AG4 and AG5 signals. Therefore, regardless of the binary value of B8 of the input code, two of the four inverters that generate AG2, AG3, AG4, and AG5 are supplied with a gated input.

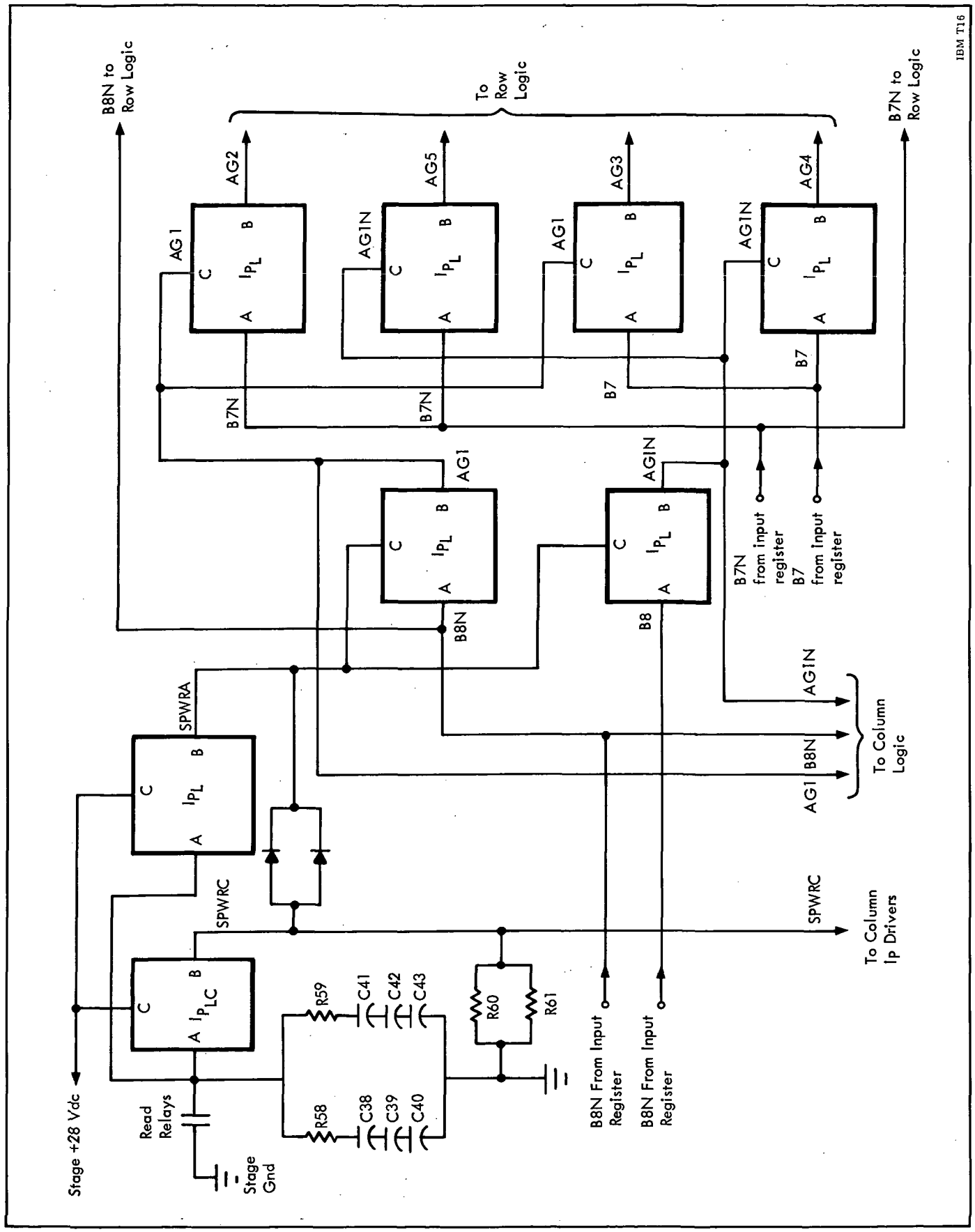


Figure 2-11. AG Signal Generation Logic

However, it is the binary value of B7 that determines which of the inverters supplied with a gated input is activated.

When B7 is a binary "1" and AG1 is present, + 28 Vdc is applied to the input (A) of the inverter that generates AG3. This signal (+ 28 Vdc) maintains the AG3 inverter in the OFF state making AG3 a binary "0". However, under these same conditions, B7N is a binary "0". When this signal (0 Vdc) is applied to the input of the AG2 inverter, the inverter is activated making AG2 a binary "1".

If the binary value of B7 is zero, the inverter action described above will be reversed making AG2 a binary "0" and AG3 a binary "1".

If B7 is a binary "0" and AG1N is present, the above description will be true for the inverters generating AG4 and AG5 signals. The AG2, AG3, AG4, and AG5 signals are applied as gated inputs to the AND gates in the logic circuits developing the row NOT signals.

SPWRC is applied to the column I_P drivers approximately 300 microseconds after the generation of the AG signals, thereby allowing the row and column logic to be conditioned before the column I_P drivers are conditioned. This delay prevents the possible generation of extraneous Switch Selector outputs. The time delay is accomplished by installing a 0.82 microfarad capacitor between the base and emitter of each transistor in the SPWRC inverter.

The filter circuit (R58, R59 and C38-C43) on the input of the switch power inverters serves to reduce 28 volt fluctuations caused by chatter in the read relays. The filter causes the SPWRA and SPWRC signals to rise more smoothly, thereby preventing the possibility of voltage spikes being coupled to the output logic causing extraneous Switch Selector outputs.

The purpose of the diodes located between SPWRA and SPWRC is to make the turn off time of SPWRC inverter equal to the turn off time of SPWRA inverter. (SPWRC will lag SPWRA because of the capacitors on the input of the SPWRC inverter.) If SPWRC is allowed to lag SPWRA, the column I_P drivers will remain gated once the SPWRA signal is removed; making it possible to energize the NPN inverters in the column logic producing extraneous Switch Selector outputs. In addition to the diodes, resistors R60 and R61 serve as line discharge resistors for SPWRC voltage.

Row Logic

There are 16 row NOT signals generated. A portion of the generation of these signals is shown in Figure 2-12. Each row NOT signal is generated by a pair of AND gates and a NPN inverter. The AND gates sense either the true or complement code of bits 4, 5, and 6. The code of bits 7 and 8 have previously been determined by generation of the AG signal. Only one of the two AND gates can be qualified at one time, and that particular AND gate then activates the inverter which generates the desired row NOT signal.

As an example, the following discussion will show how the row 10 NOT signal is generated. (Row signals are designated in octal.) The bottom AND gate in the row 10 NOT circuitry has the AG3 signal as its gated supply. The inputs to this AND gate are B4, B5, and B6. In order to qualify this AND gate, the AG3, B4, B5 and B6 lines must all be at an up level. This requires that bits 4, 5, 6, 7 and 8 have the following binary values:

B4, B5, B6 = Binary "1"

B7 = Binary "0"

B8 = Binary "1"

When the input code is as stated above, the bottom AND gate will be qualified producing an up level voltage to the input of the NPN inverter. With an up level on the input, the output of the inverter will be clamped to ground producing a row 10 NOT signal.

If the verification shows an error, the complement of the input code will be sent to the Switch Selector.

The combination of B7 and B8 now combine to produce an AG5 signal. B4, B5, and B6 are in a down level condition, resulting in the B4N, B5N and B6N lines to the AND gate being conditioned at an up level. Thus, the inputs to the top AND gate in the row 10 NOT circuitry are all up level producing an up level input to the NPN inverter. The up level on the input of the inverter causes the output of the inverter to be clamped to stage ground producing a row 10 NOT signal. Thus, a failure in the input relays can be tolerated without generating an erroneous row NOT signal thereby causing a Switch Selector failure.

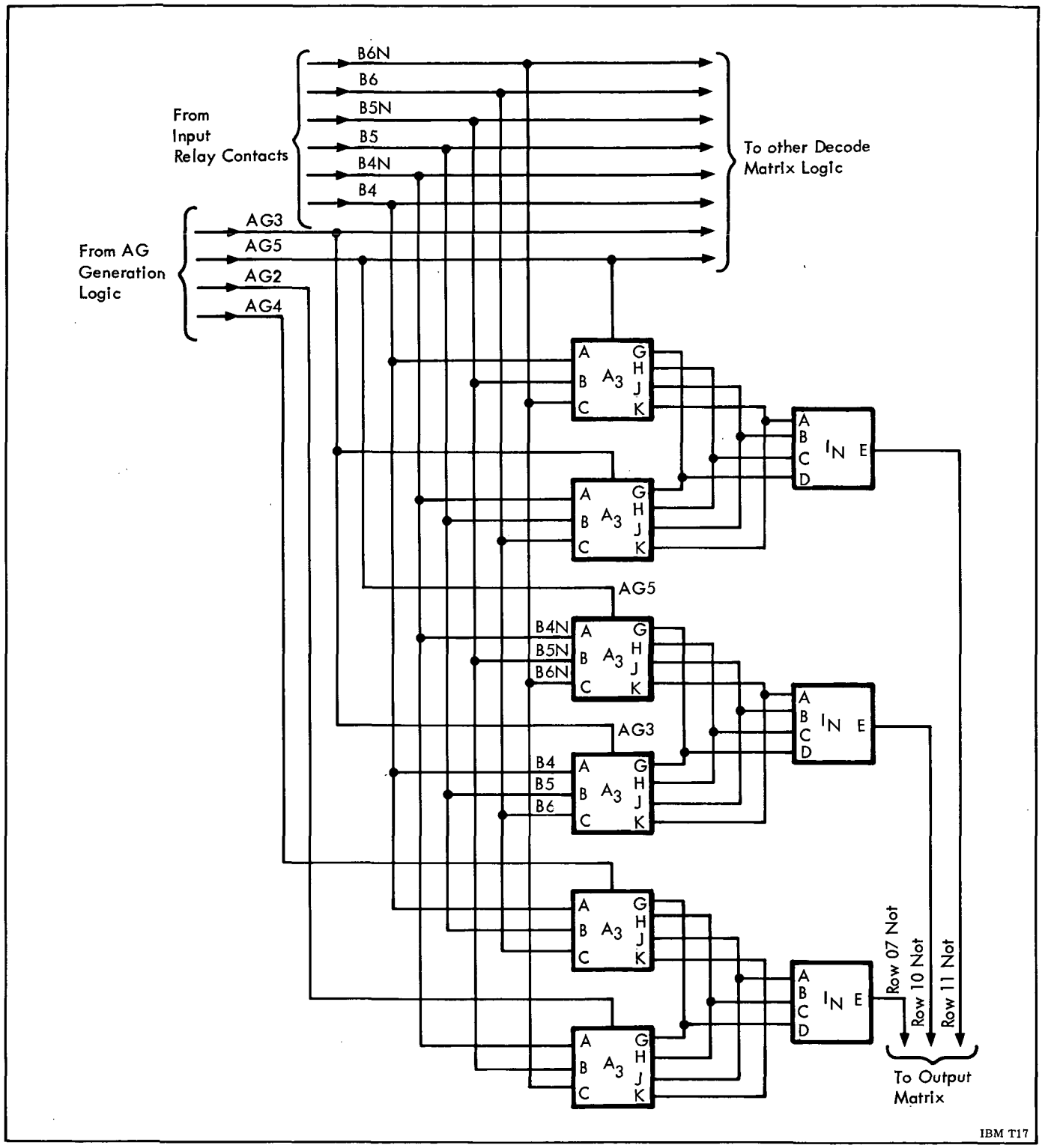


Figure 2-12. Portion of Row NOT Signal Generation Logic

Each row NOT signal is generated in the same manner, using different AG signals in conjunction with different combinations of B4, B5, B6, B4N, B5N, and B6N covering all possible input conditions allowed. The row NOT signals are fed directly to the output matrix logic.

Column Logic

In addition to the row NOT signals, there are seven column signals generated in the decoding matrix. Figure 2-13 illustrates a portion of the column signal generation logic. These signals are generated in a manner similar to the row NOT signals. Two AND gates, one NPN inverter, and one PNP inverter are used to produce the column signal which is fed directly to the output matrix logic. The difference stems from the use of different AG signals, different input signals, and an additional inverter (PNP type). The bias gating signals used in the column circuitry are AG1 and AG1N, and the input signals are B1, B2, B3, B1N, B2N and B3N. The additional inverter in the column circuitry results in the generated column signal being an up level signal, whereas the row NOT signal is a down level signal.

2-12 OUTPUT MATRIX AND TELEMETRY

Output Matrix

The output matrix consists of 112 PNP inverters (I_P's) arranged in a 16 row by 17 column matrix (see Figure 2-16). Each allowed input command will select 1 of the 112 I_P's and produce a Switch Selector output. Each row NOT signal from the row logic is connected to the base input (A) of seven output I_P's. Likewise, each column signal from the column logic is connected to the gated input (C) of 16 output I_P's.

Control of any 1 of the 112 output drivers is accomplished as follows: An output driver is conditioned for an up level output (+28 Vdc) by the presence of a down level (0 Vdc) at the base input and an up level at the gated input. These input conditions cause the PNP transistors in the selected I_P to conduct, causing the +28 Vdc gated input to appear across the output of the I_P. All other input conditions cause the I_P drivers to remain off, resulting in a down level output.

Thus, an up level voltage on the column line and a down level voltage on the row NOT line will cause the output driver at the intersection of these two lines to be at an up level voltage. All remaining output drivers will remain in the down level stage as conditioned by their inputs.

Telemetry

The PNP inverters used in the output matrix are modified to provide a special telemetry output (see Figure 2-18). The outputs are connected to a common telemetry line and sent to stage telemetry (see Figure 2-16). An up level on any one of the output drivers results in an up level telemetry signal, indicating to the ground equipment the presence of a Switch Selector output. The magnitude of the telemetry signal is determined by a resistive network. The telemetry signals of 8 I_P's are connected through one 12K resistor to stage ground. Therefore, the effective telemetry resistance is the equivalent of fourteen 12K resistors in parallel, or approximately 806 ohms.

2-13 TEST OUTPUTS

The Switch Selector has two telemetry outputs which are used to verify that the input selection relays can be set and reset properly. These signals, zero indicate and register test, are special outputs of the output matrix.

Zero Indicate

The presence of an all zero binary input command results in an up level voltage at the zero indicate output (see Figure 2-14). The I_P that produces the zero indicate signal is conditioned at its gated input (C) by three series connected logic elements; a four input AND gate (A4), a NPN inverter (I_N), and a PNP inverter (I_{P_L}). An all zero input code yields an up level voltage output from the AND gate. This up level is applied to the input of the NPN inverter resulting in its output being clamped to ground. The down level NPN inverter output is applied to the base input (A) of the PNP inverter resulting in an up level output. This up level becomes the gated input for the zero indicate I_P.

The input (A) of the zero indicate (I_P) is conditioned by two series connected logic elements; a five input AND gate (A_5) and an NPN inverter. The all zero input code causes an up level AND gate output which when applied to the NPN inverter, results in a down level inverter output. This down level is the input (A) of the zero indicate I_P driver.

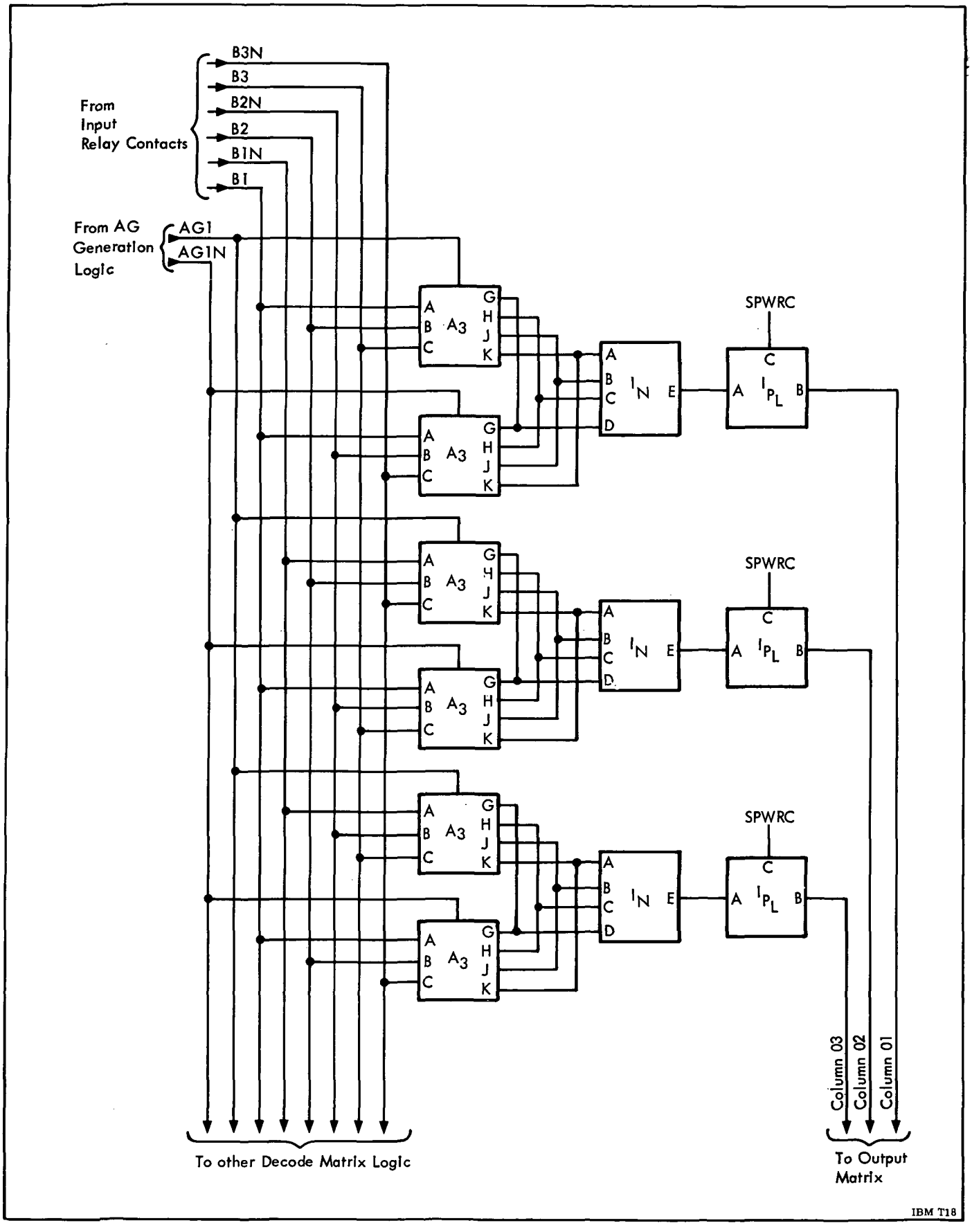


Figure 2-13. Portion of Column Signal Generation Logic

The up level gated input, and the down level base input maintain the zero indicate I_P at an up level state. Conversely, during non-zero input codes, the zero indicate I_P is maintained at a down level output. Note that the read command is not required for zero indicate.

Register Test

The presence of all ones in the input code and the application of the read command results in an up level voltage at the register test output (see Figure 2-15). Similar to zero indicate, the register test I_P is conditioned at the gated input (C) by three series logic elements; a three input AND gate (A_3), an I_N inverter, and an I_P inverter. The input (A) is conditioned by two series connected logic elements; a three input AND gate (A_3), and an I_N inverter. This operation requires that the read command be issued. The read command initiates generation of the AG1 and AG2 gates. The AG1 and AG2 signals condition the AND gates that generate the signals which are supplied to the gated input (C) and base input (A) of the register test (I_P). Conversely, during the all zero input code, the register test I_P maintains a down level output.

2-14 CIRCUIT DESCRIPTION

This section contains a description of the circuits and relays which make up the modules used in the Switch Selector. The Switch Selector uses three

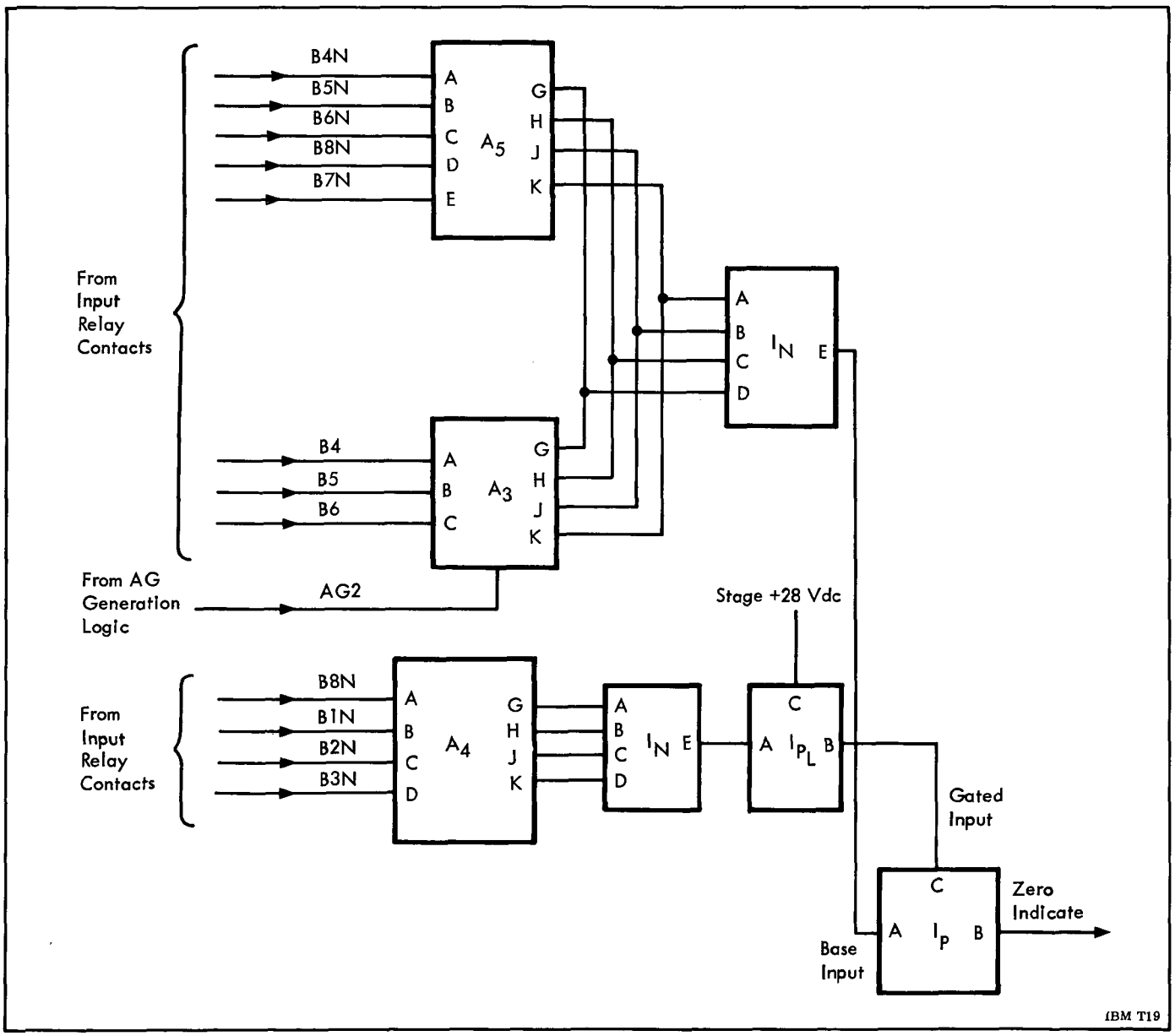


Figure 2-14. Zero Indicate Logic

basic logic circuits whose functions are AND and INVERT. There are two different types of inverters, one type uses PNP transistors and is designated I_P, the other type uses NPN transistors and is designated I_N.

AND Circuit

The passive AND gate may have from four (A_4) to six (A_6) inputs. The gated input for an AND circuit may be supplied directly from a + 28 Vdc source, or by a + 28 Vdc signal from a PNP inverter.

The AND circuits have a quad-redundant configuration (see Figure 2-17 for an example of a quad-redundant four input AND circuit). Operation of an AND circuit will not be affected by the malfunction of any detail part in the circuit.

Logical operation of the AND circuit is as follows: With an up level (+ 28 Vdc) on the gated input, and an up level on all of the remaining inputs, the AND circuit produces an up level output. A down level voltage (0 Vdc) at any of the AND circuit inputs, including the gated input, forces the output of the AND circuit to be clamped to the down level input.

PNP Inverter (Ip)

The I_P inverter uses four transistors to provide a quad-redundant configuration (see Figure 2-18). Operation of the inverter will not be affected by the malfunction of any detail part in the circuit. The gated input may be supplied directly from a + 28 Vdc source or by a + 28 Vdc signal from a preceeding Ip circuit.

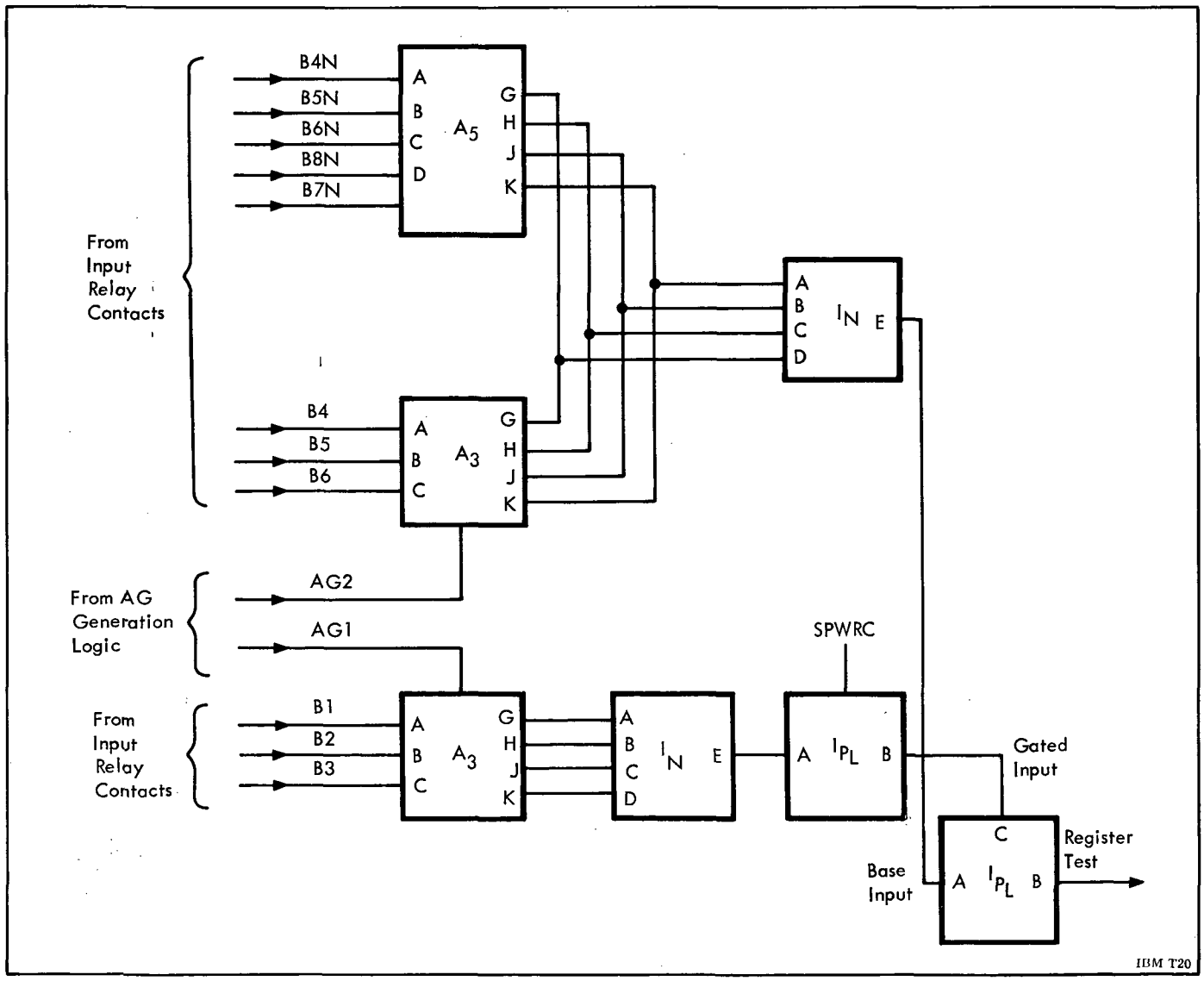
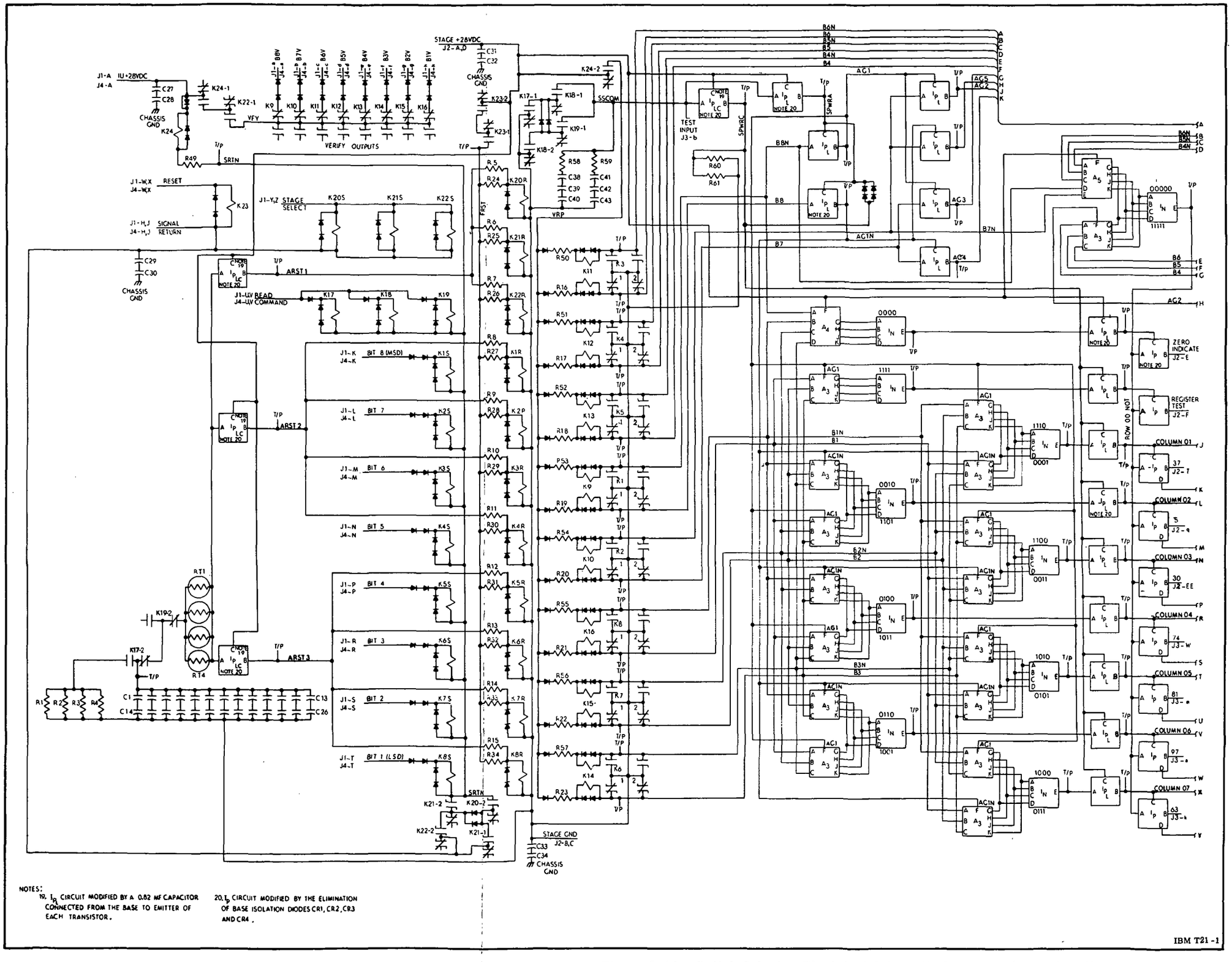


Figure 2-15. Register Test Logic



NOTES:

19. I_{PL} CIRCUIT MODIFIED BY A 0.82 MF CAPACITOR CONNECTED FROM THE BASE TO EMITTER OF EACH TRANSISTOR.

20. I_P CIRCUIT MODIFIED BY THE ELIMINATION OF BASE ISOLATION DIODES CR1, CR2, CR3 AND CR4.

Figure 2-16. Switch Selector Electrical Schematic Diagram (Sheet 1 of 2)

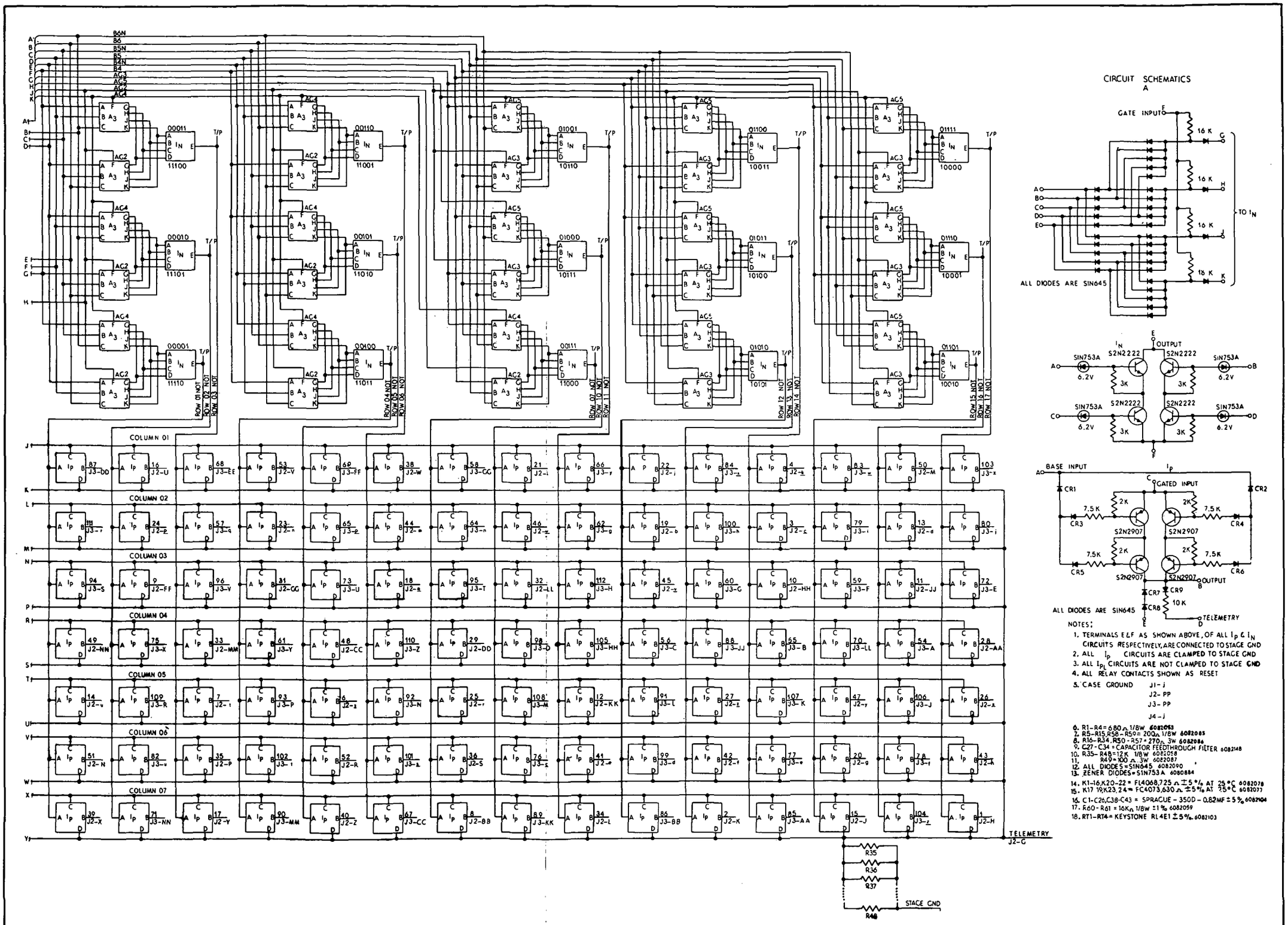


Figure 2-16. Switch Selector Electrical Schematic Diagram (Sheet 2 of 2)

Logical operation of an I_P inverter is as follows: An up level gated input (C) and a down level base input (A) causes the four PNP transistors to saturate. The low collector to emitter impedance of the transistors allows the up level gated input to be seen at the output (B), resulting in an up level I_P output. All other inputs cause the transistor to have a high impedance from collector to emitter, maintaining the output of the I_P at a down level voltage.

The I_P inverters are used in the AG signal generation circuits, the decode matrix circuits, and the output matrix circuits. The I_P circuits are classified into three groups due to modification in the output circuits of the I_P's. See Figure 2-18.

I_P Driver - A telemetry output is coupled to the output of the I_P driver. An up level I_P output will result in an up level telemetry output. One 12K telemetry load resistor is associated with each eight I_P driver circuits. The output of the I_P driver is clamped to stage ground through two series diodes. The switch selector output matrix is made up of this type of inverter.

I_{P_L} Driver (unclamped) - The I_{P_L} inverter differs from the I_P inverter in that it has no telemetry output and the series clamping diodes have been removed. This type of inverter is used in the AG signal generation circuitry and as column signal drivers.

$I_{P_{LC}}$ Driver - The $I_{P_{LC}}$ inverter differs from the I_{P_L} inverter in that the $I_{P_{LC}}$ has been modified by installing a 0.82-microfarad capacitor in parallel with the 2K resistor from the base to emitter of each transistor. This capacitance provides a 300-microsecond delay at the output of the $I_{P_{LC}}$. These inverters are used in the AG signal generation circuitry and the automatic reset circuitry.

NPN Inverters (I_N)

The I_N inverter uses four quad-redundant NPN transistors (see Figure 2-19). Operation of the inverter will not be affected by the malfunction of any detail part in the circuit. The I_N inverter is preceeded by a quad-redundant AND circuit and followed by an I_P inverter circuit. The bias voltages for the I_N inverters are obtained from the I_P inverters which they drive.

Logical operation of an I_N inverter is as follows: an up level input from the AND gate applied to the bases of the NPN transistors will cause them to conduct, clamping the output at ground or down level. A down level input will maintain the transistor in the OFF state and present a high-impedance output or up level to the following I_P circuit.

A Zener diode is provided on each input line of the I_N to ensure the transistors remain OFF when the output of the AND gate is at the down level. The Zener diodes prevent the NPN transistors from being turned ON by the voltage across the diodes in the AND gate.

Relays

The Switch Selector uses both latch and conventional type relays. Table 2-4 lists the Switch Selector relay functions.

Latch Type - The latch type relay (see Figure 2-20) has two relay coils, K1S and K1R, associated with a pair of relay contacts, K1-1 and K1-2. The relay contacts are controlled through the medium of a magnetic field and operate in unison. A pulse of voltage, of sufficient magnitude and duration,

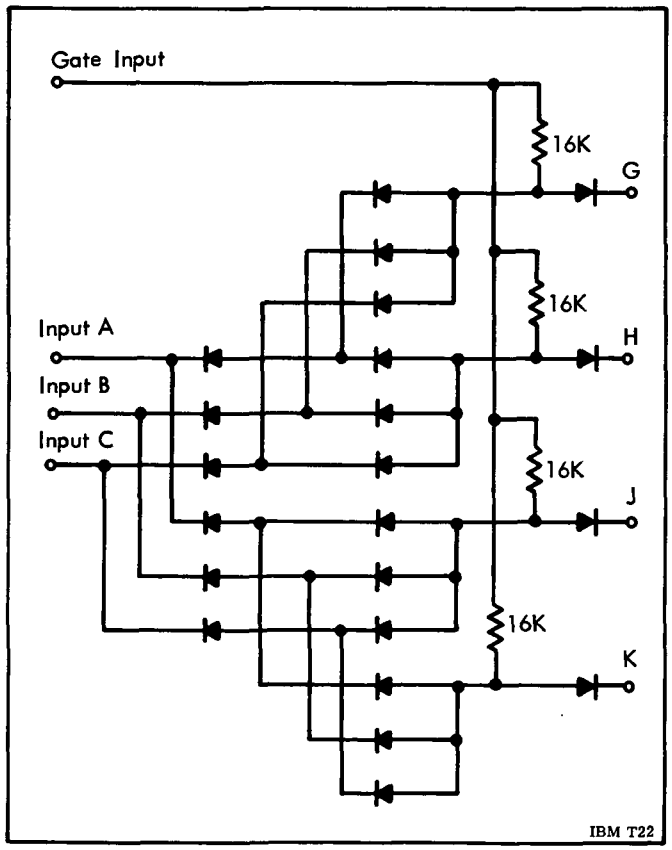


Figure 2-17. Four Input AND Circuit (A_4)

applied across a relay coil will cause the relay contacts to set or reset depending upon whether the set (K1S) or reset (K1R) coil is pulsed. The relay contacts will remain in the set or reset position after excitation is removed because of the latch capability of the relays. Transient suppressor diodes parallel the coils. The maximum set and reset (pick and fall) time for latch type relays is 6.5 milliseconds at high temperature conditions (125 °C).

Conventional Type - The conventional relay (see Figure 2-21) has a single relay coil (K2) associated with a pair of relay contacts (K2-1 and K2-2). The pair of relay contacts operate in unison. Excitation of the coil will cause the contacts to close; continued excitation is necessary for the contacts to remain closed. When the excitation is removed, the contacts will return to the normally open position. Transient suppressor diodes parallel the coils. The maximum pick time for the conventional type relay is five milliseconds, and the maximum fall time is 8 milliseconds at high temperature conditions (125 °C).

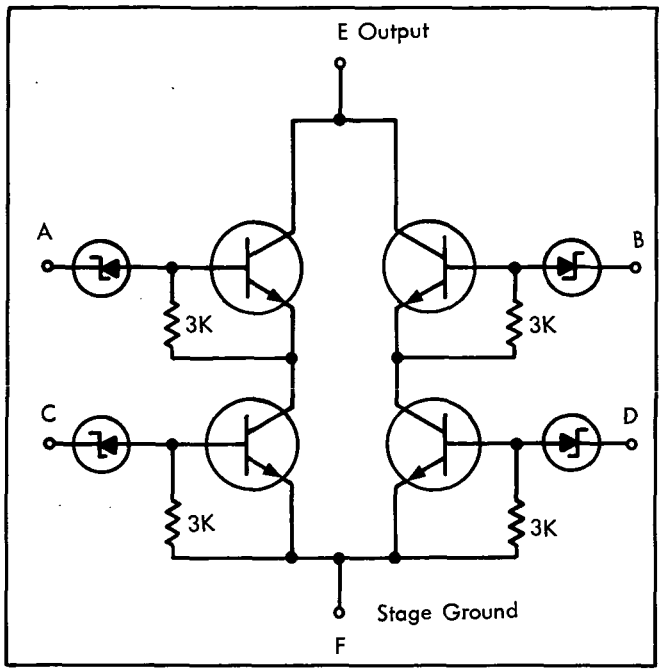


Figure 2-19. NPN Inverter Schematic Diagram

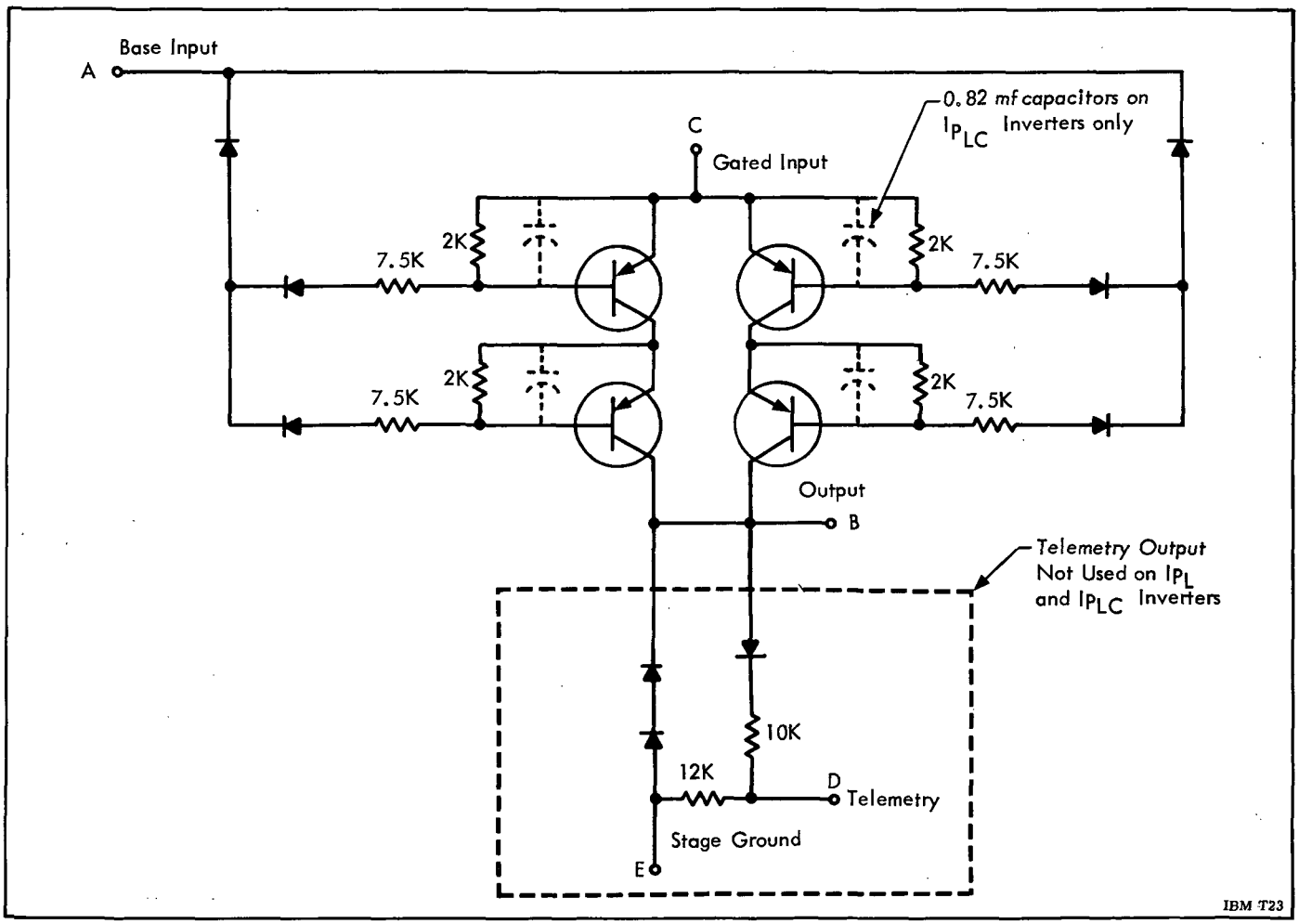


Figure 2-18. PNP Inverter Schematic Diagram

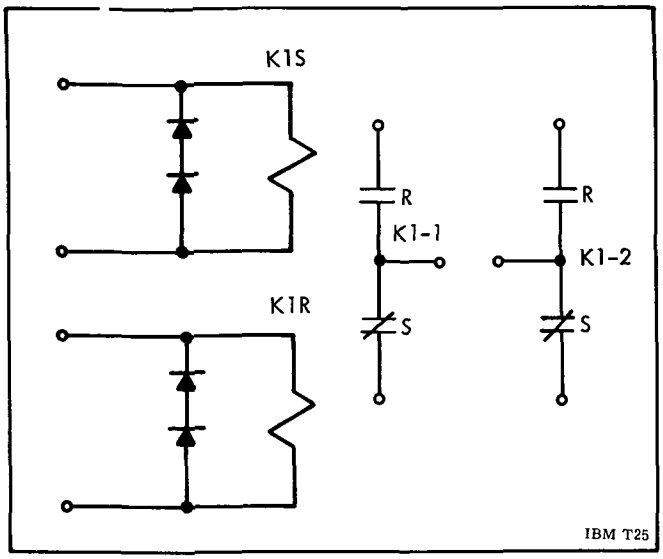


Figure 2-20. Latching Relay Schematic Diagram

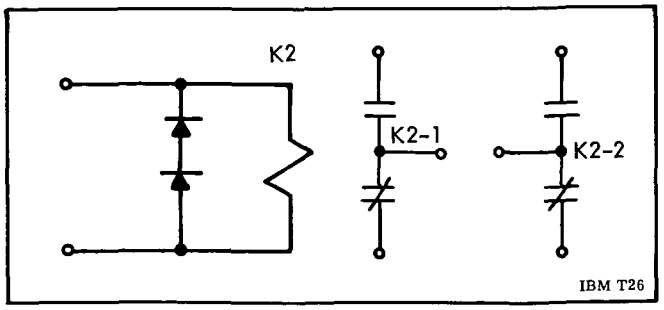


Figure 2-21. Conventional Relay Schematic Diagram

Table 2-1. Switch Selector Relay Functions

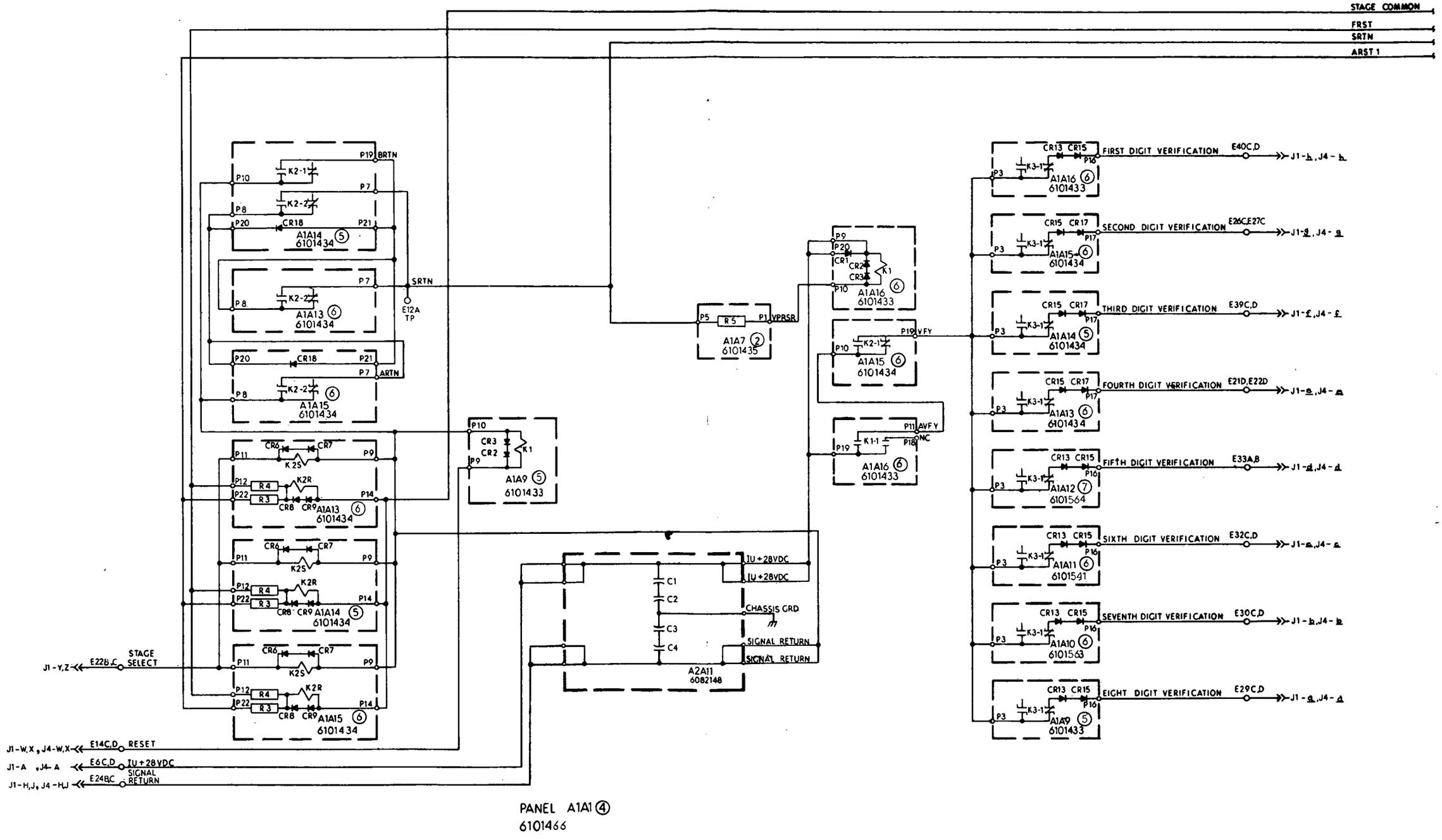
Relay	Contacts	Function
K1S thru K8S	K1-1, K1-2 thru K8-1, K8-2	Bit relay contacts - Used to store the flight command in the input register. Transfers command code to the AG and decode circuitry. Also applies power to the proper verify relay coils allowing verification information to be returned to the LVDA. These relays are magnetic latch relays.
K1R thru K8R	K1-1, K1-2 thru K8-1, K8-2	Bit relay contacts are reset when K1R through K8R coils are energized, returning the input register to its reset condition.
K9S thru K16S	K9 thru K16	When latch type relays K9S through K16S are energized, the NC verify relay contacts, K9 through K16, are opened. This removes IU +28 Vdc from the verification lines going to the LVDA.
K9R thru K16R	K9 thru K16	Verify relay reset relays. When the reset coils are energized, the verify contacts K9 through K16 return to their NC position, applying IU +28 Vdc to the verification lines.
K17	K17-1	Read command relay contact K17-1 is 1 of 4 sets of relay contacts which close when the read command is given applying stage +28 Vdc to the AG circuitry.
	K17-2	One of the three read command relays - When the read command is given, relay contact K17-2 closes initiating the automatic reset cycle.
K18	K18-1 K18-2	Read command relay - When energized in conjunction with K17 and K19, K18-1 and K18-2 apply stage +28 Vdc to AG circuitry.
K19	K19-1	Read command relay - When energized in conjunction with K17 and K18, K19-1 applies stage +28 Vdc to the AG circuitry.
	K19-2	Same as K17-2.

Table 2-4. Switch Selector Relay Functions (Cont)

Relay	Contacts	Function
K20S	K20-1	Not used
	K20-2	One of the four sets of relay contacts required to complete the signal return path for the input relays (K1S through K8S) and the read command relays. Energized by the stage select command.
K21S	K21-1 K21-2	Stage select relay - K21-1 and K21-2 are two of the four sets of contacts required to complete the signal return path for the input relays and the read command relays. This is a magnetic latching relay.
K22S	K22-1	Stage select relay - One of the two sets of relay contacts which, upon application of the stage select command, applies IU + 28 Vdc to the verify output relay contacts. This is a magnetic latching relay.
	K22-2	One of the four sets of contacts which, upon application of the stage select command, completes the signal return path for the input relays and the read command relays.
K20R thru K22R	K20-1, K20-2 thru K22-1, K22-2	Stage selet reset relays - When K20R, K21R and K22R are energized, the noted relay contacts return to their normally open position thereby removing the signal return path from the input relays and read command relay; removes stage +28 Vdc from the AG circuitry; and interrupts IU +28 Vdc to the verify output relay contacts.
K23	K23-1, K23-2	Reset relay coil - Upon application of the reset command, stage +28 Vdc is applied, via K23-1 and K23-2, to the input relay reset coils and the stage select relay reset coils.
K24	K24-1 K24-2	Verify power relay - This relay is energized upon closure of the stage select contacts completing IU signal return circuit, and applies IU +28 Vdc to the verify relay contacts and stage +28 Vdc to the verify relay coils.

2-15 REFERENCE MATERIAL

This section contains reference material which will prove helpful to personnel involved in trouble analysis of the Switch Selector. Figure 2-22 (sheet 1 through sheet 6) is the complete logic diagram for the Switch Selector. Figures 2-23 through 2-38 are the electrical schematic diagrams for the 16 different circuit modules used in Model II Switch Selectors.



IBM Drawing No.: 6101498
Revision: D

IBM T27-1

Figure 2-22. Switch Selector Logic Diagram (Sheet 1 of 6)

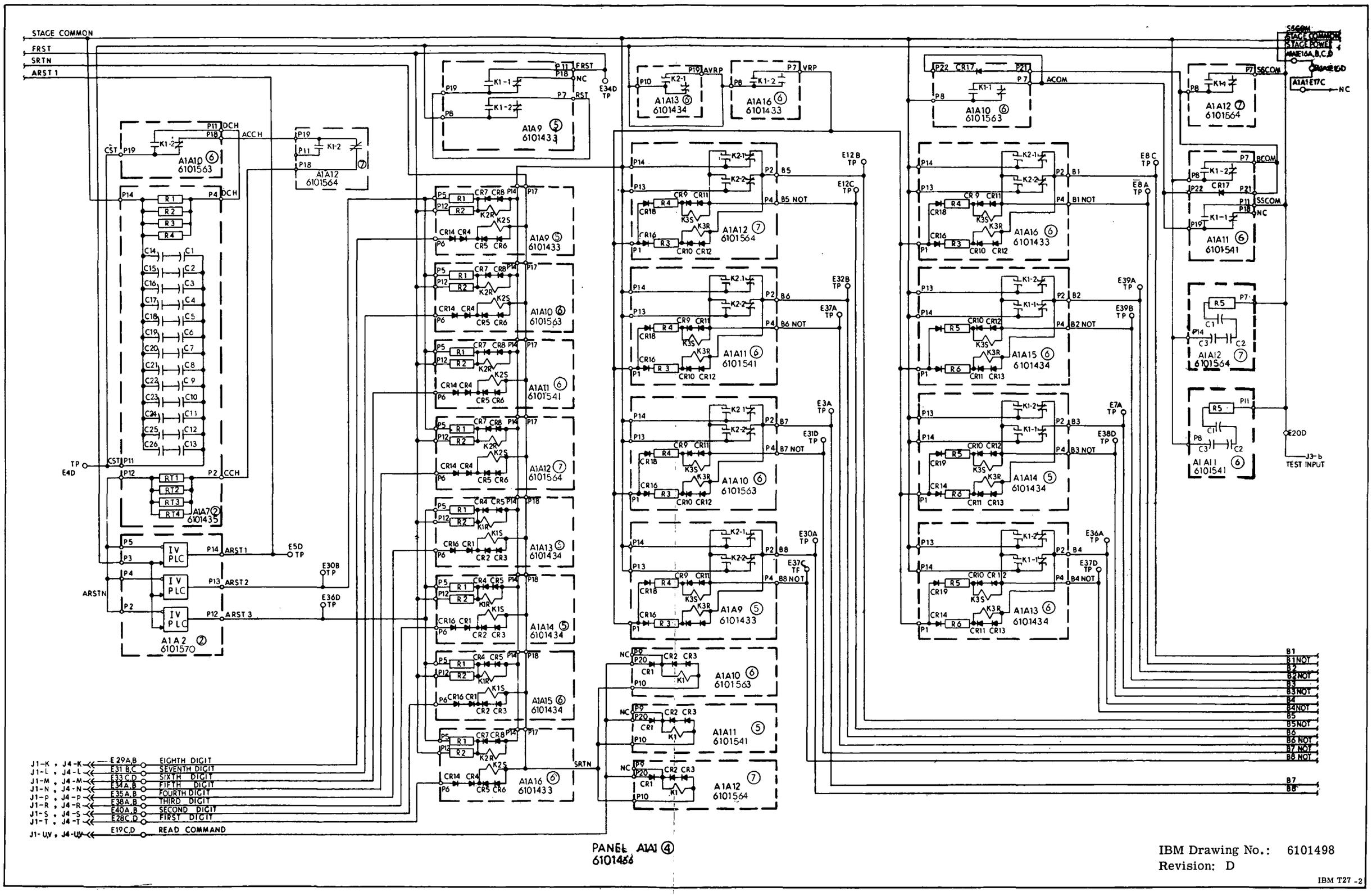
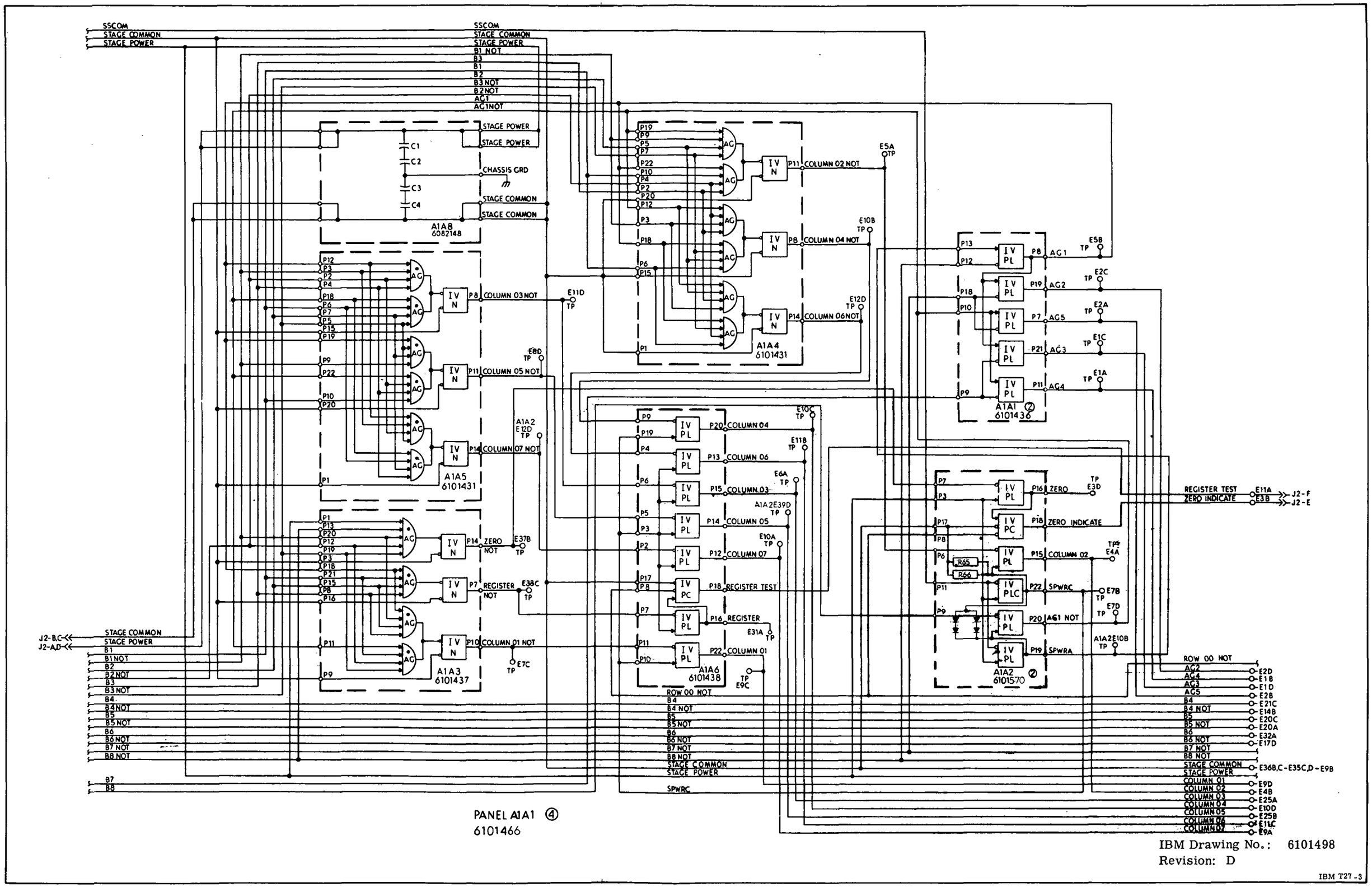


Figure 2-22. Switch Selector Logic Diagram (Sheet 2 of 6)



IBM Drawing No.: 6101498
Revision: D

IBM T27-3

Figure 2-22. Switch Selector Logic Diagram (Sheet 3 of 6)

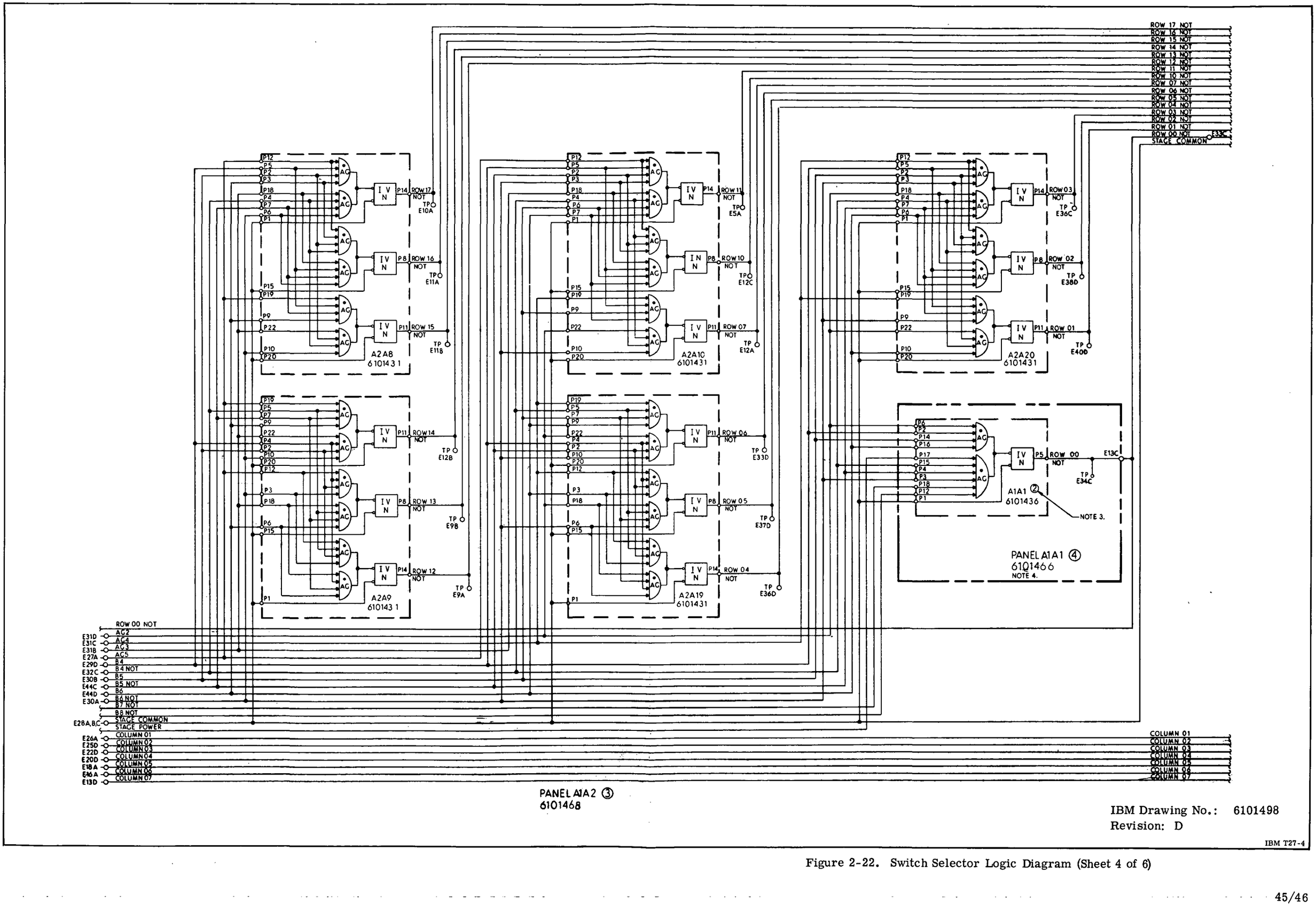
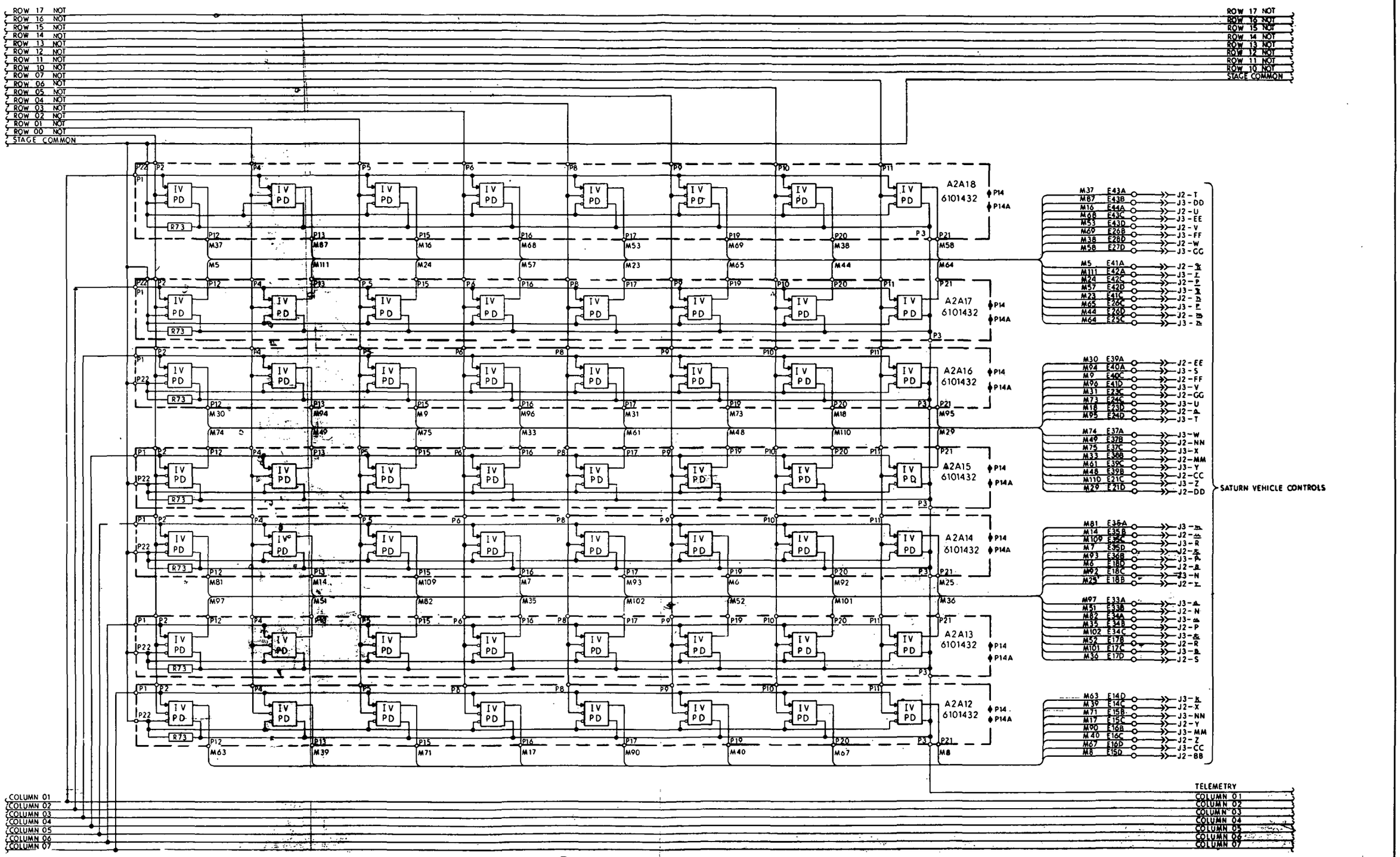


Figure 2-22. Switch Selector Logic Diagram (Sheet 4 of 6)



IBM Drawing No.: 6101498
Revision: D

IBM T27-5

Figure 2-22. Switch Selector Logic Diagram (Sheet 5 of 6)

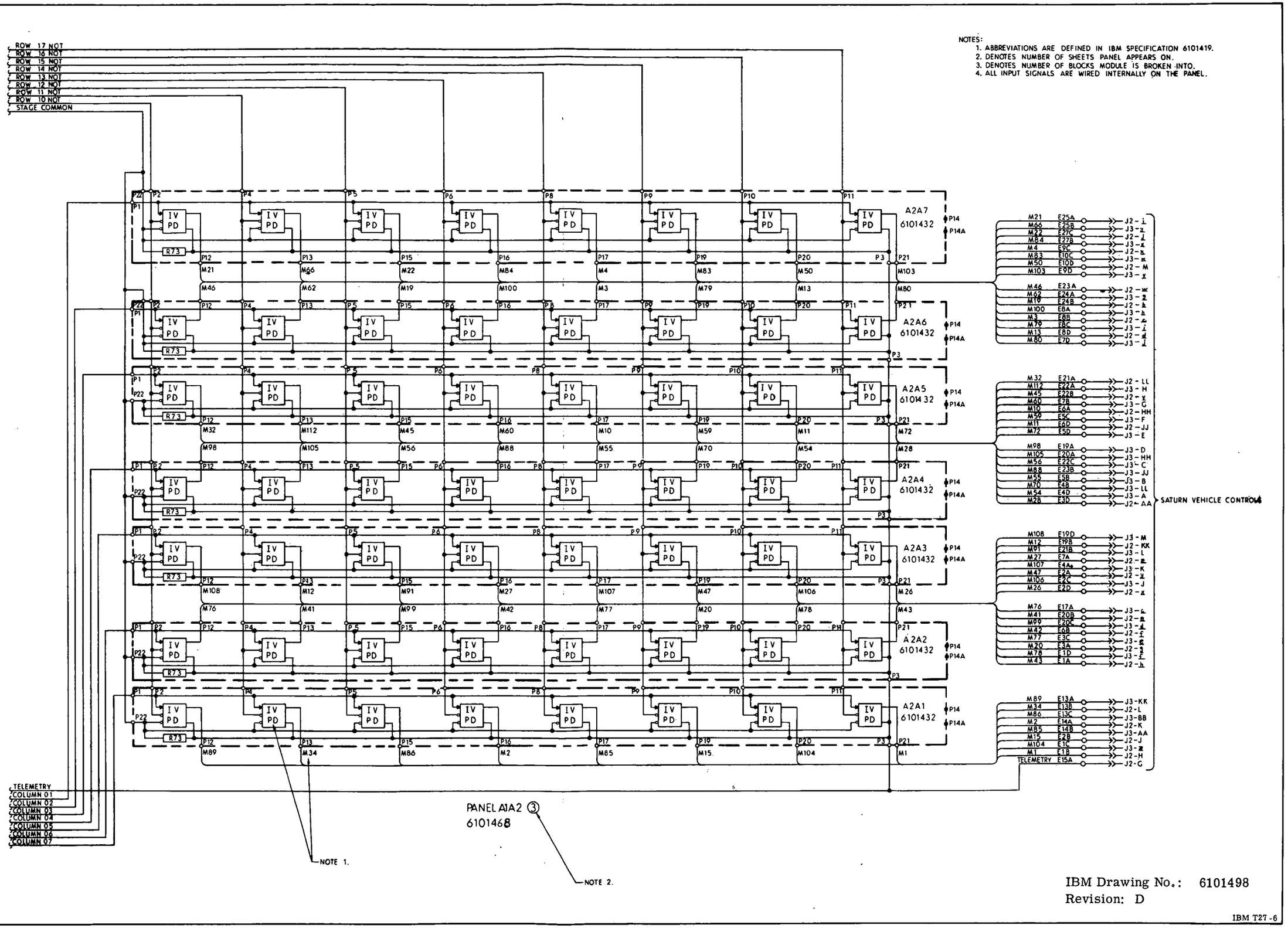
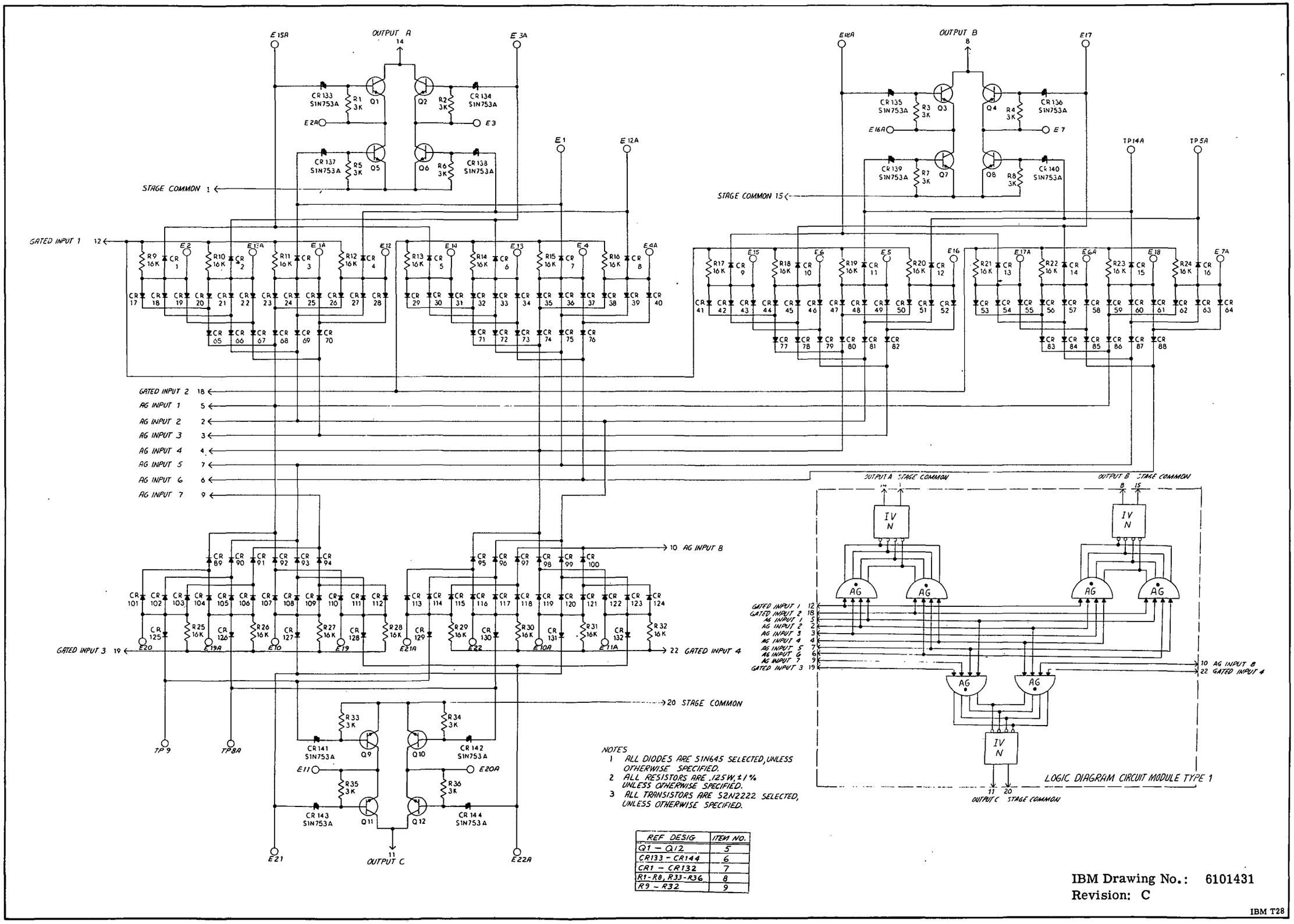


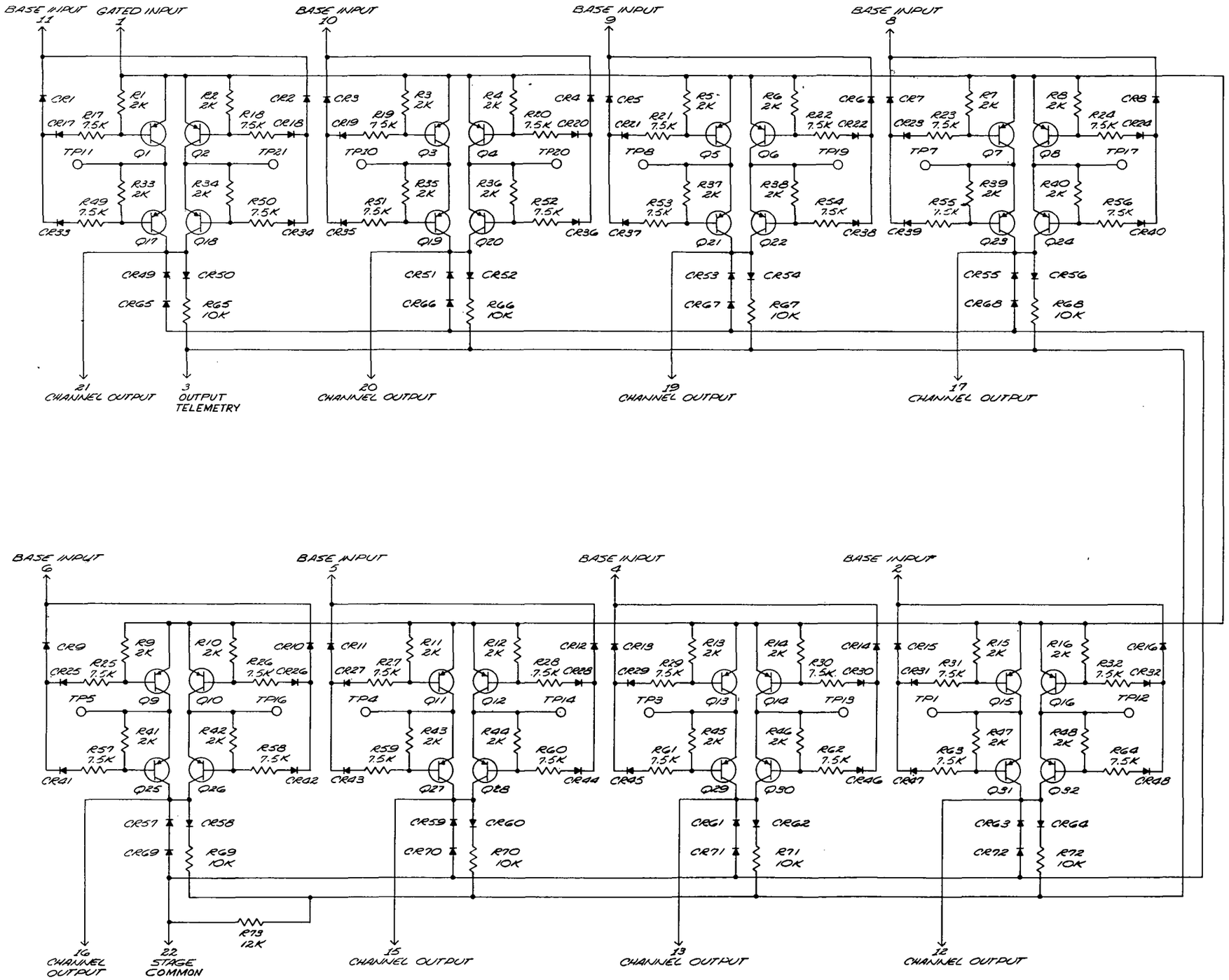
Figure 2-22. Switch Selector Logic Diagram (Sheet 6 of 6)

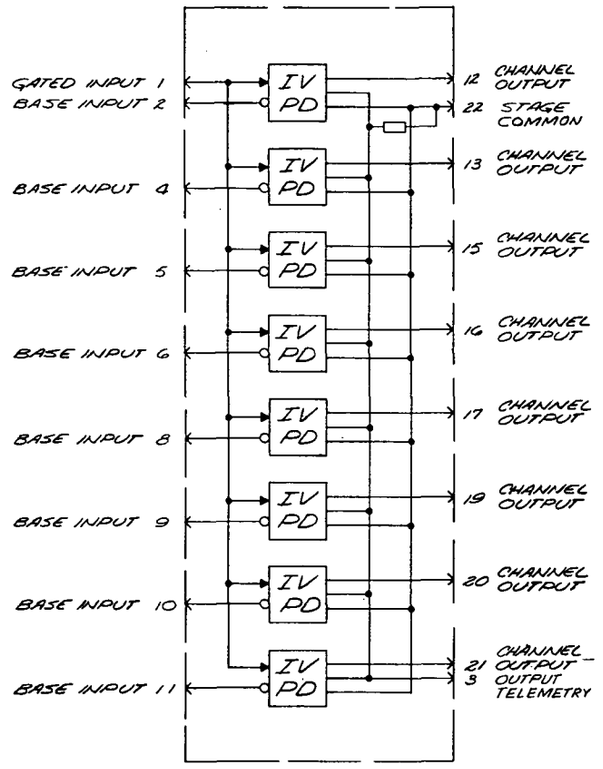


REF DESIG	ITEM NO.
Q1 – Q12	5
CR133 – CR144	6
CR1 – CR132	7
R1-R8, R33-R36	8
R9 – R32	9

IBM Drawing No.: 6101431
Revision: C

Figure 2-23. Electrical Schematic, Circuit Module Type 1, Decode





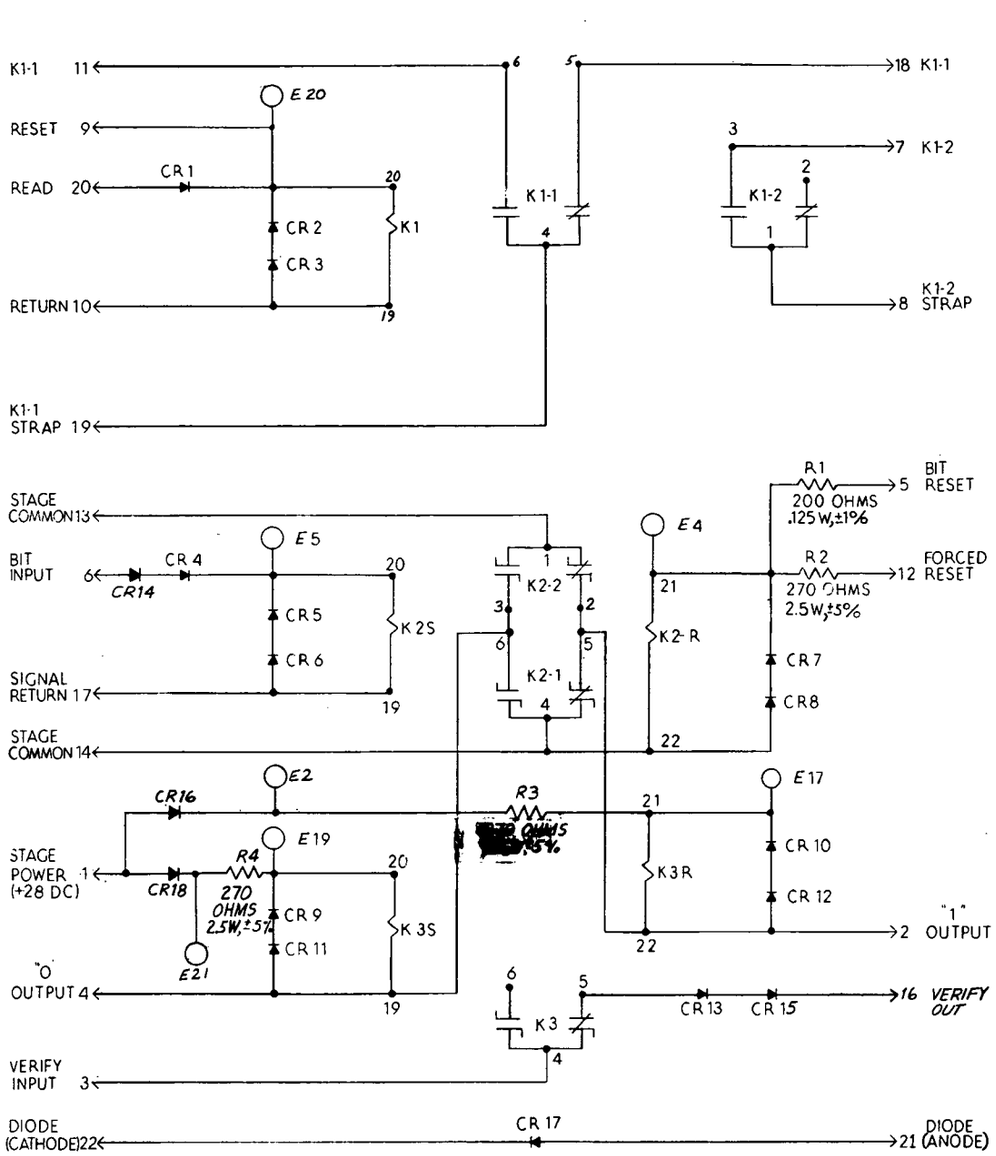
REFERENCE DESIGNATION	ITEM NO.
CR1 - CR72	8
Q1 - Q32	9
R1 THRU R16	6
R33 THRU R48	6
R17 THRU R32	5
R49 THRU R64	5
R65 THRU R72	7
R73	10

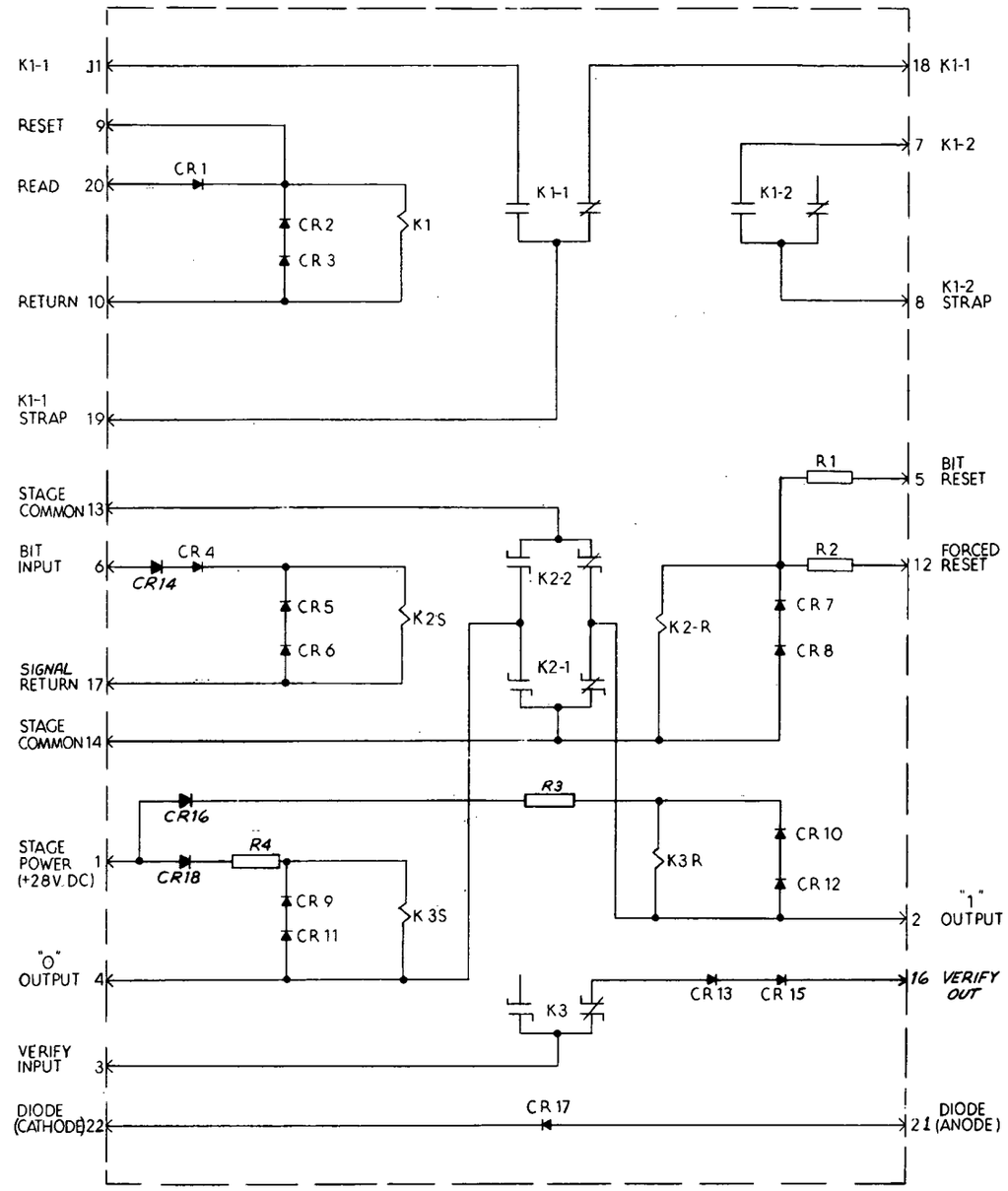
NOTE:
1. ALL DIODES S1N645 SELECTED, UNLESS OTHERWISE SPECIFIED
2. ALL TRANSISTORS S2N2907 SELECTED, UNLESS OTHERWISE SPECIFIED
3. ALL RESISTORS .125 WATT, ±1% UNLESS OTHERWISE SPECIFIED

IBM Drawing No.: 6101432
Revision: D

IBM T29

Figure 2-24. Electrical Schematic, Circuit Module Type 2, Output Driver





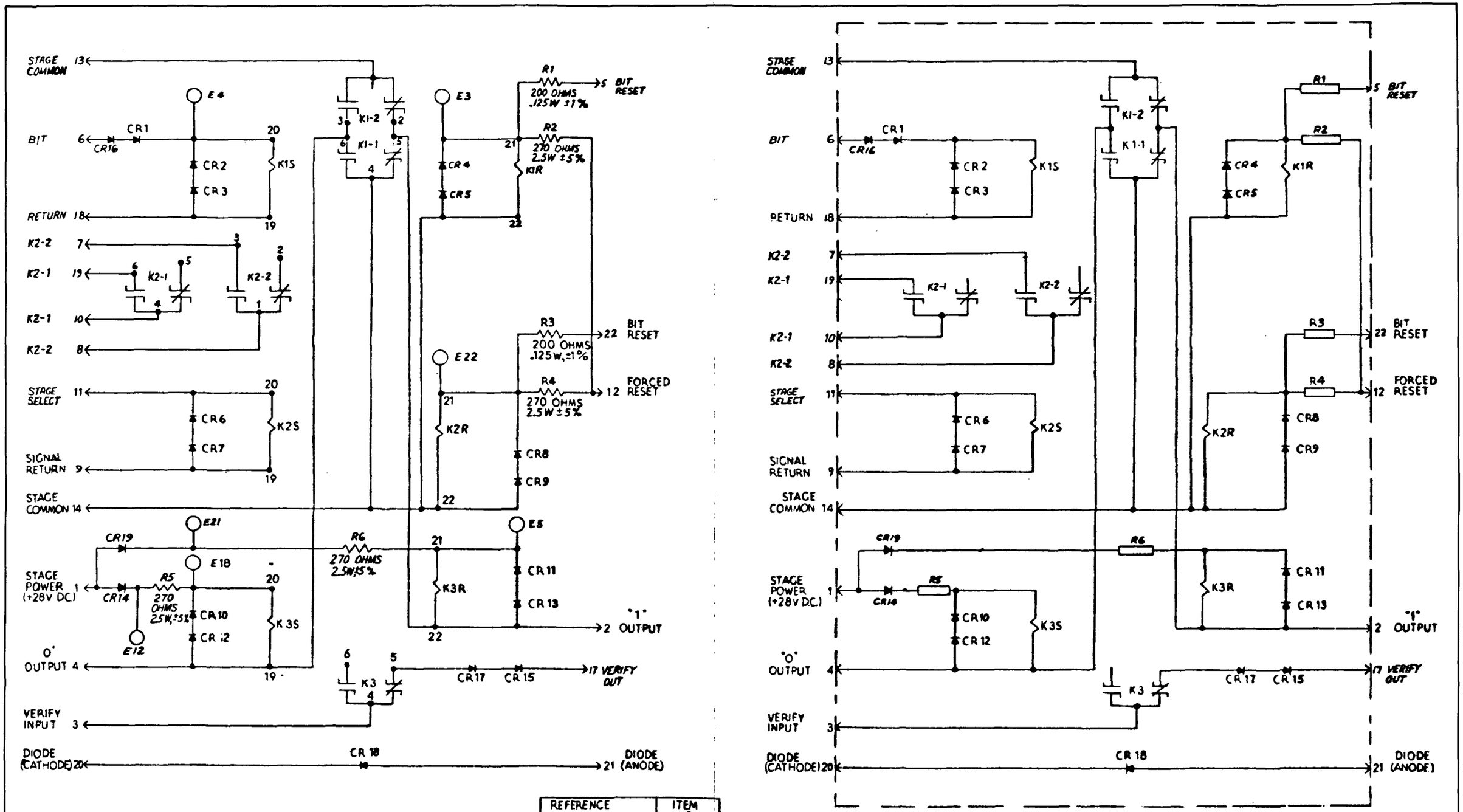
REFERENCE DESIGNATION	ITEM NO
CR1 - CR18	4
R1	6
R2 - R4	5
K1	7
K2, K3	8

NOTES:
1 ALL DIODES ARE S1N645 SELECTED, UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101433
Revision: E

IBM T30

Figure 2-25. Electrical Schematic, Circuit Module Type 3, Read



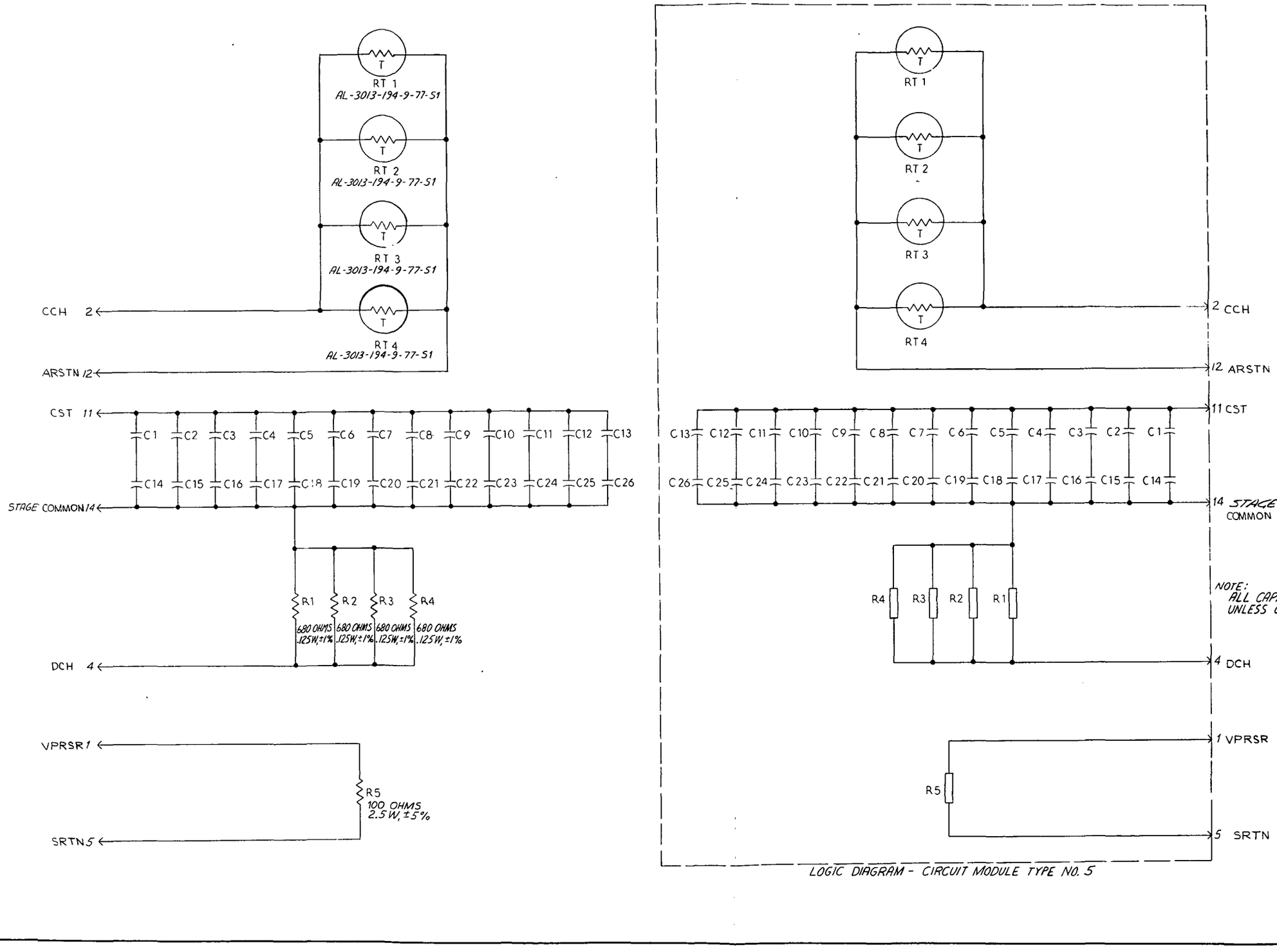
REFERENCE DESIGNATION	ITEM NO
CR1-CR19	4
R1, R3	6
R2, R4, R5, R6	5
K1, K2, K3	7

NOTES:
1 ALL DIODES ARE SIN645 SELECTED UNLESS OTHERWISE SPECIFIED

IBM Drawing No.: 6101434
Revision: D

IBM T31

Figure 2-26. Electrical Schematic, Circuit Module Type 4, Stage Select



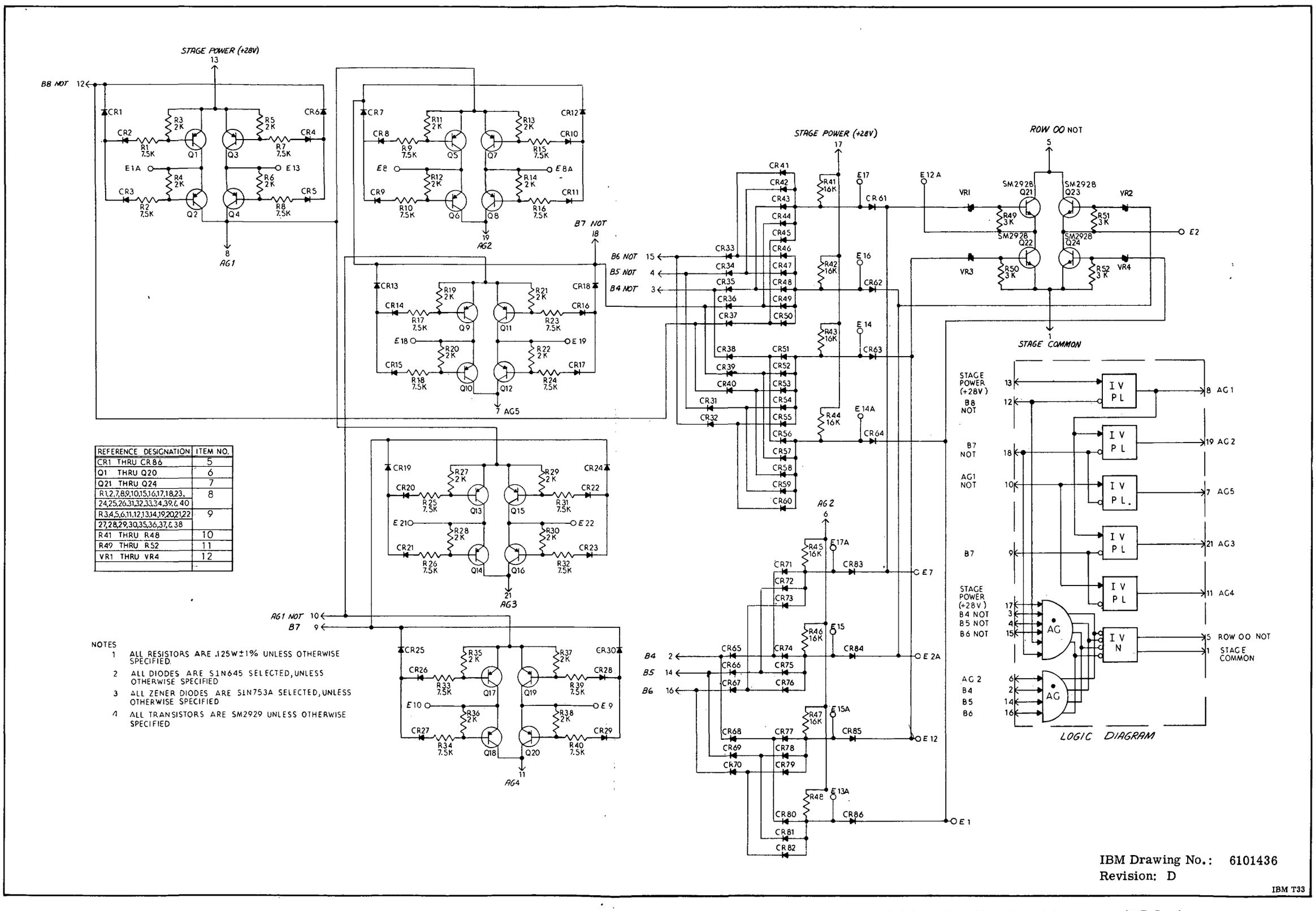
REF DESIG	ITEM NO
R1 - R4	4
R5	5
RT1 - RT4	6
C1 - C26	7

LOGIC DIAGRAM - CIRCUIT MODULE TYPE NO. 5

IBM Drawing No. 6101435
Revision: E

IBM T32

Figure 2-27. Electrical Schematic, Circuit Module Type 5, Auto Reset



REFERENCE DESIGNATION	ITEM NO.
CR1 THRU CR86	5
Q1 THRU Q20	6
Q21 THRU Q24	7
R1,2,7,8,9,10,15,16,17,18,23, 24,25,26,31,32,33,34,39,& 40	8
R3,4,5,6,11,12,13,14,19,20,21,22 27,28,29,30,35,36,37,& 38	9
R41 THRU R48	10
R49 THRU R52	11
VR1 THRU VR4	12

NOTES
1. ALL RESISTORS ARE .125W±1% UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES ARE S1N645 SELECTED, UNLESS OTHERWISE SPECIFIED
3. ALL ZENER DIODES ARE S1N753A SELECTED, UNLESS OTHERWISE SPECIFIED
4. ALL TRANSISTORS ARE SM2929 UNLESS OTHERWISE SPECIFIED

IBM Drawing No.: 6101436
Revision: D

IBM T33

Figure 2-28. Electrical Schematic, Circuit Module Type 6, AND Logic

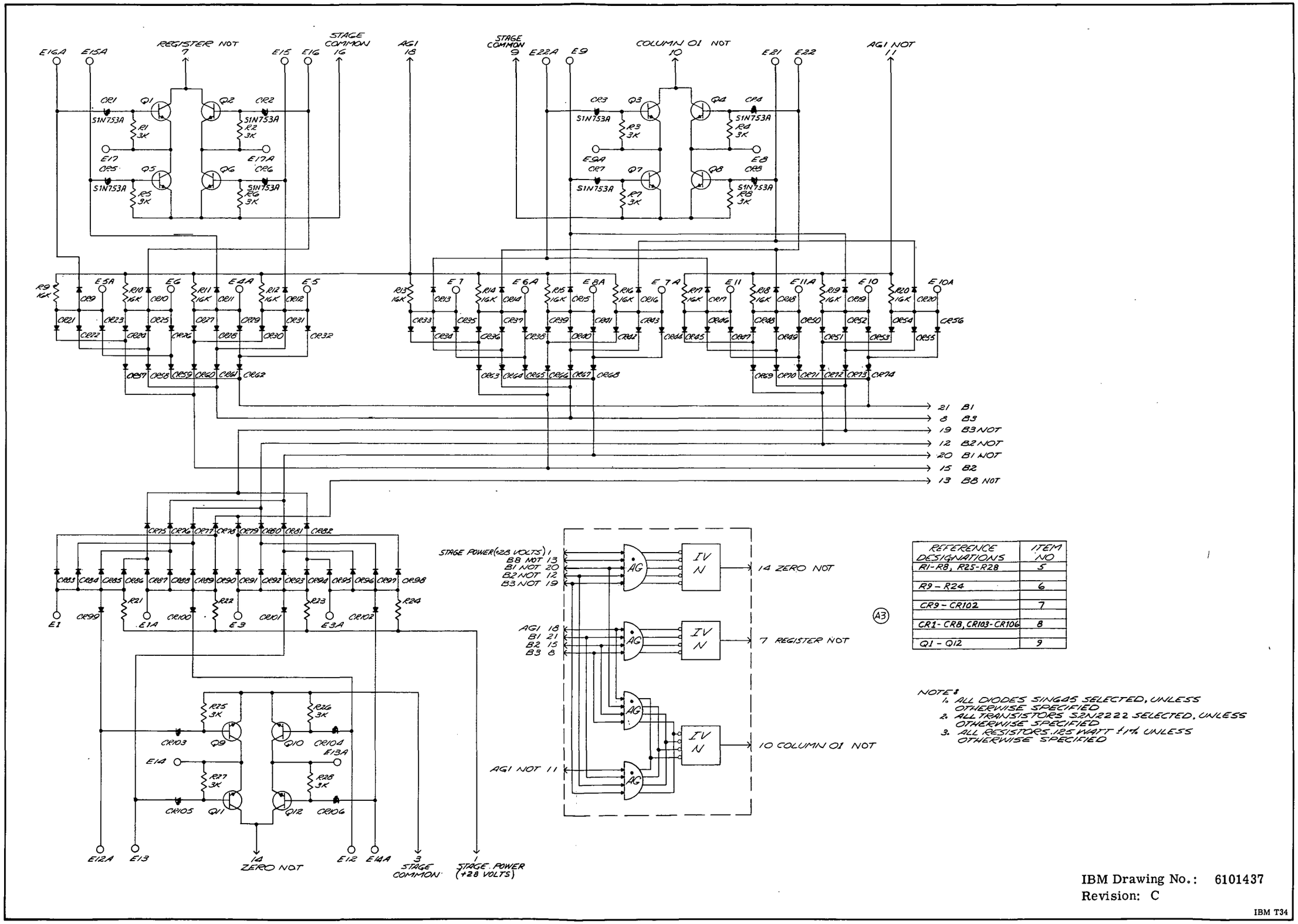
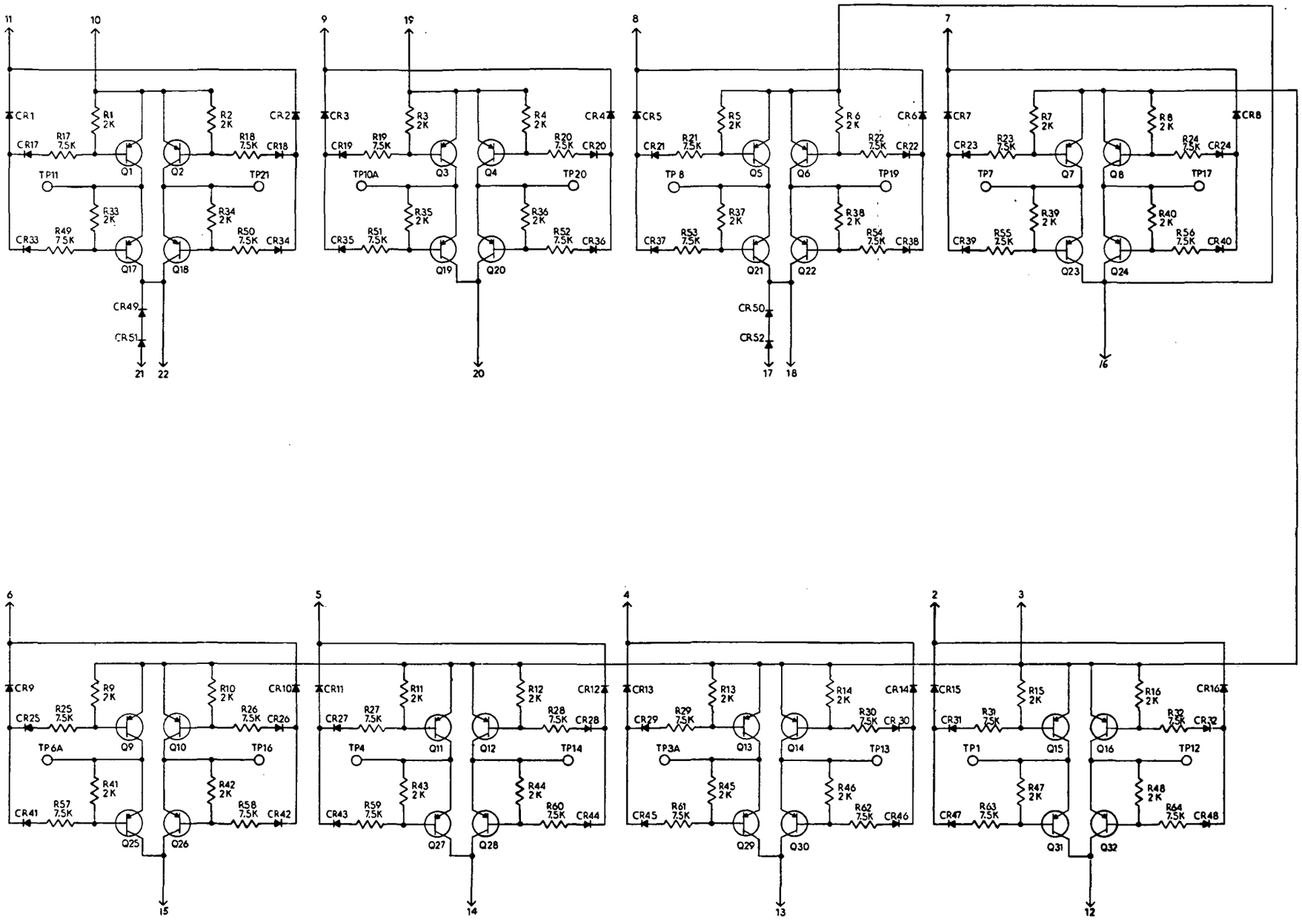


Figure 2-29. Electrical Schematic, Circuit Module Type 7, Decode



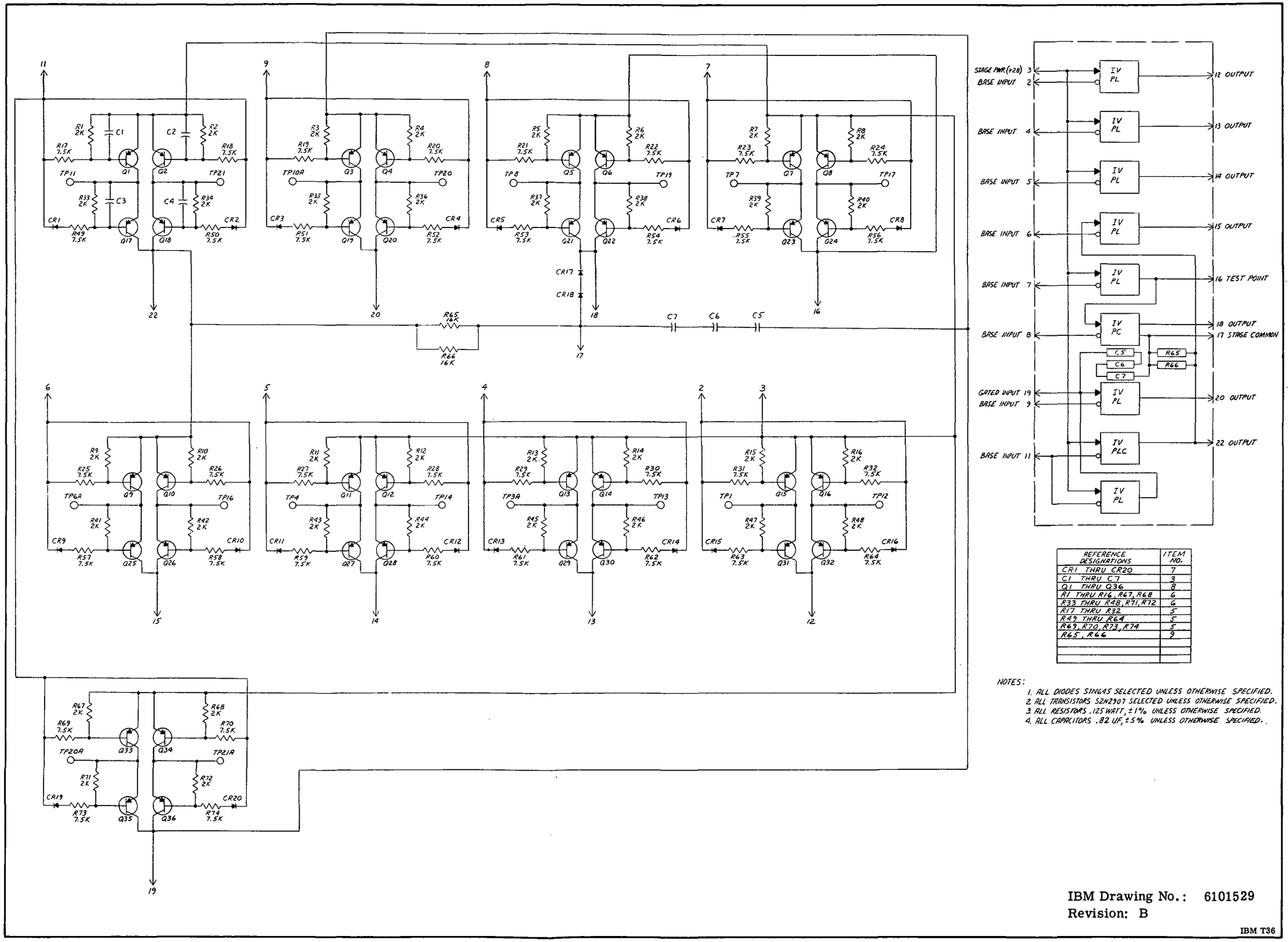
REFERENCE DESIGNATIONS	ITEM NO.
CR1 THRU CR52	7
Q1 THRU Q32	8
R1 THRU R16	6
R33 THRU R48	6
R17 THRU R32	5
R49 THRU R64	5

NOTES:
1. ALL DIODES 1N645 SELECTED, UNLESS OTHERWISE SPECIFIED
2. ALL TRANSISTORS 2N2907 SELECTED, UNLESS OTHERWISE SPECIFIED
3. ALL RESISTORS .125 WATT, ±1% UNLESS OTHERWISE SPECIFIED

IBM Drawing No.: 6101438
Revision: D

IBM T35

Figure 2-30. Electrical Schematic, Circuit Module Type 8, Miscellaneous Driver



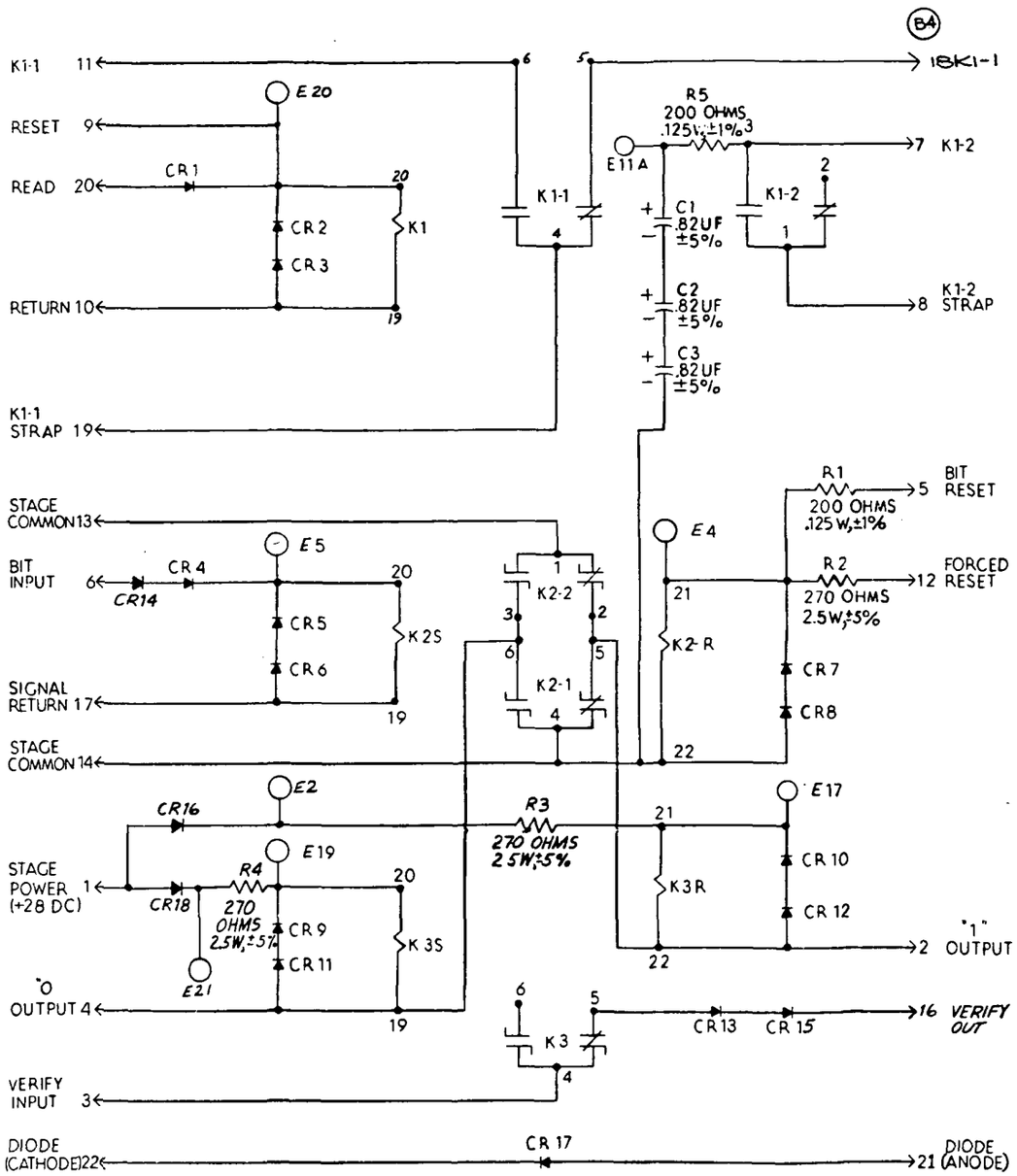
REFERENCE DESIGNATIONS	ITEM NO.
CR1 THRU CR20	7
C1 THRU C7	3
Q1 THRU Q36	8
R1 THRU R16, R67, R68	6
R33 THRU R48, R71, R72	6
R17 THRU R32	5
R49 THRU R64	5
R69, R70, R73, R74	5
R65, R66	9

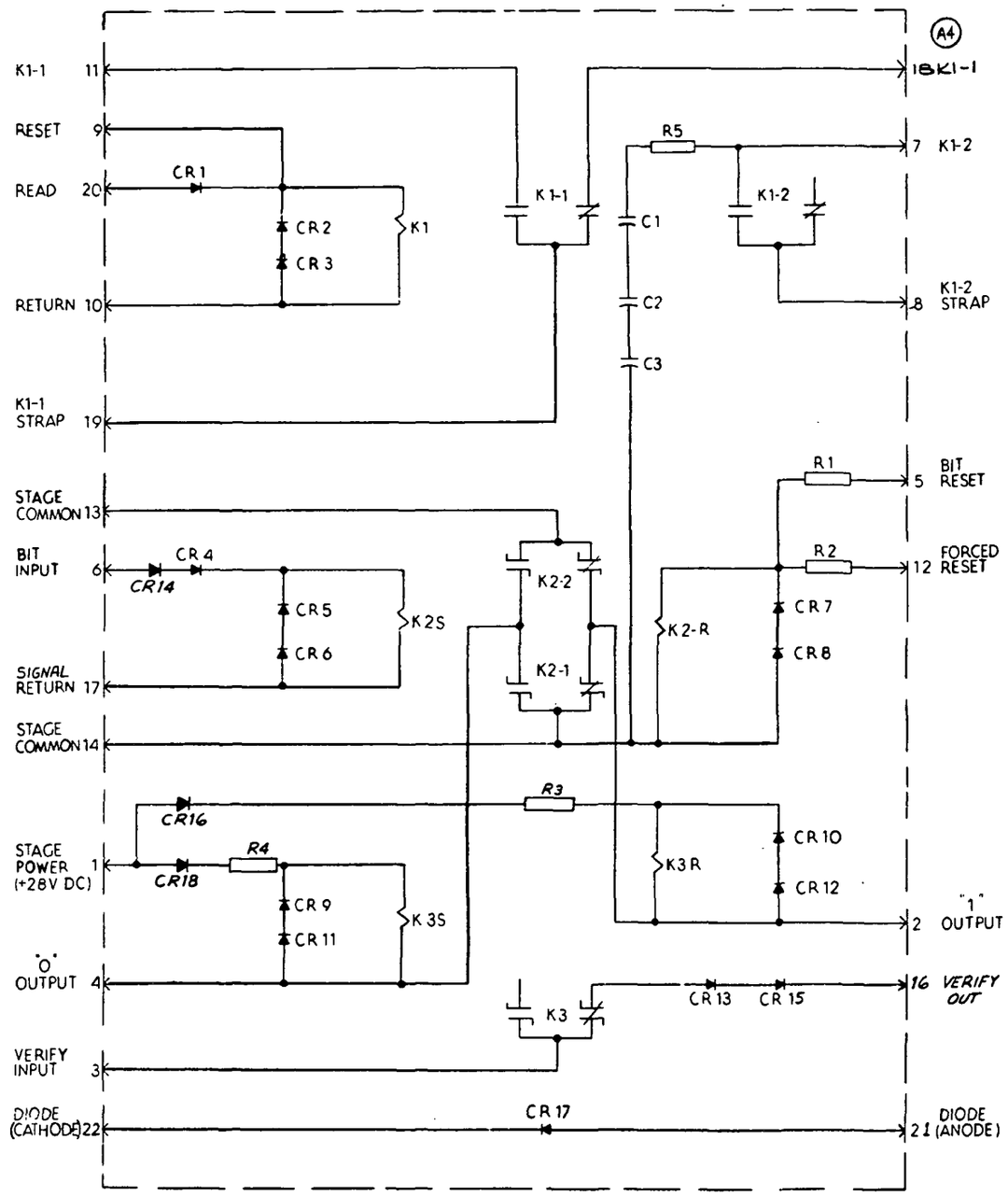
NOTES:
1. ALL DIODES SING45 SELECTED UNLESS OTHERWISE SPECIFIED.
2. ALL TRANSISTORS S2N2907 SELECTED UNLESS OTHERWISE SPECIFIED.
3. ALL RESISTORS .125 WATT, ±1% UNLESS OTHERWISE SPECIFIED.
4. ALL CAPACITORS .82 UF, ±5% UNLESS OTHERWISE SPECIFIED..

IBM Drawing No.: 6101529
Revision: B

IBM T36

Figure 2-31. Electrical Schematic, Circuit Module Type 9, Miscellaneous Driver





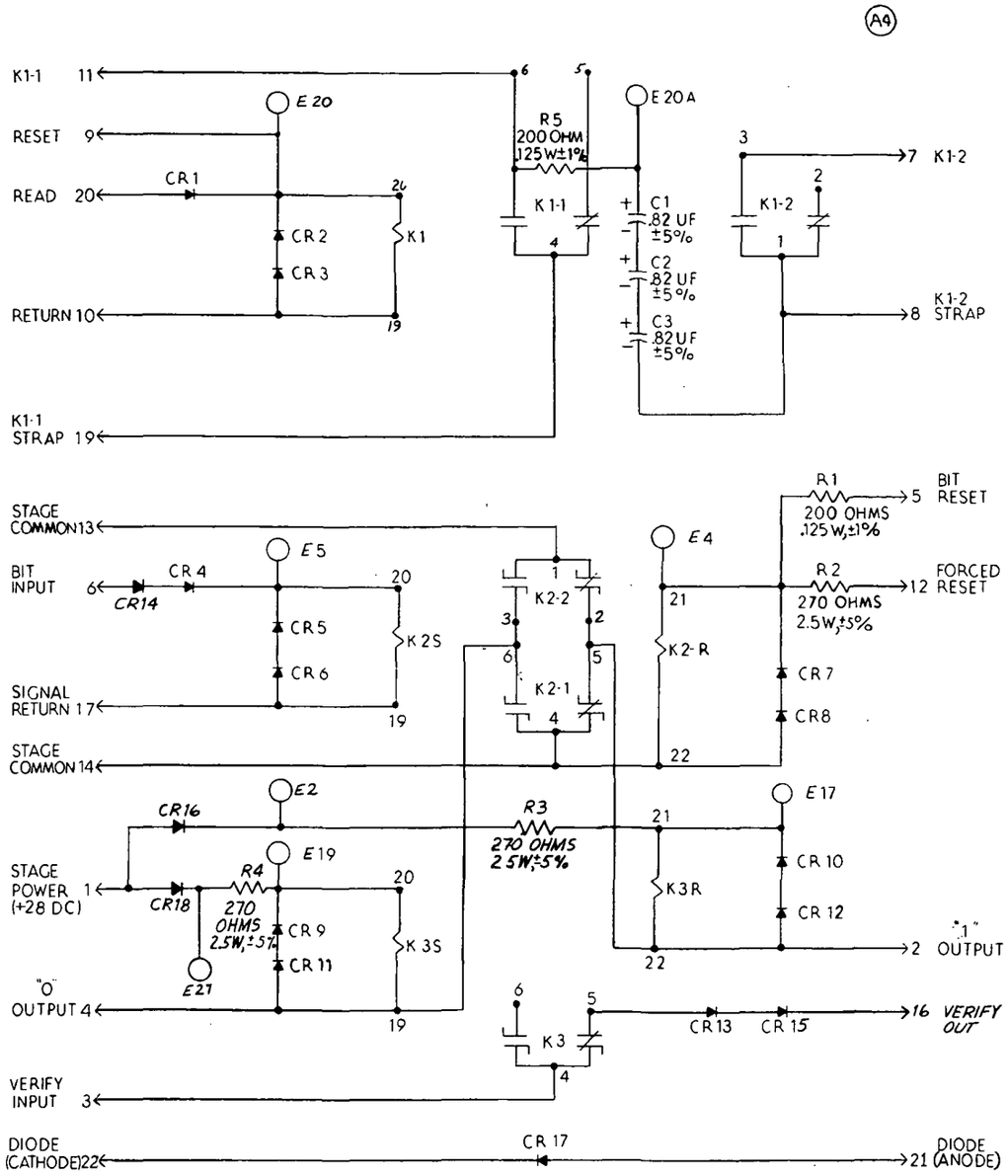
REFERENCE DESIGNATION	ITEM NO.
CR1 - CR18	4
R1, R5	6
R2 - R4	5
K1	7
K2, K3	8
C1, 2, 3	20

NOTES:
1 ALL DIODES ARE S1N645 SELECTED, UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101540
Revision: B

IBM T37

Figure 2-32. Electrical Schematic, Circuit Module Type 10, Read



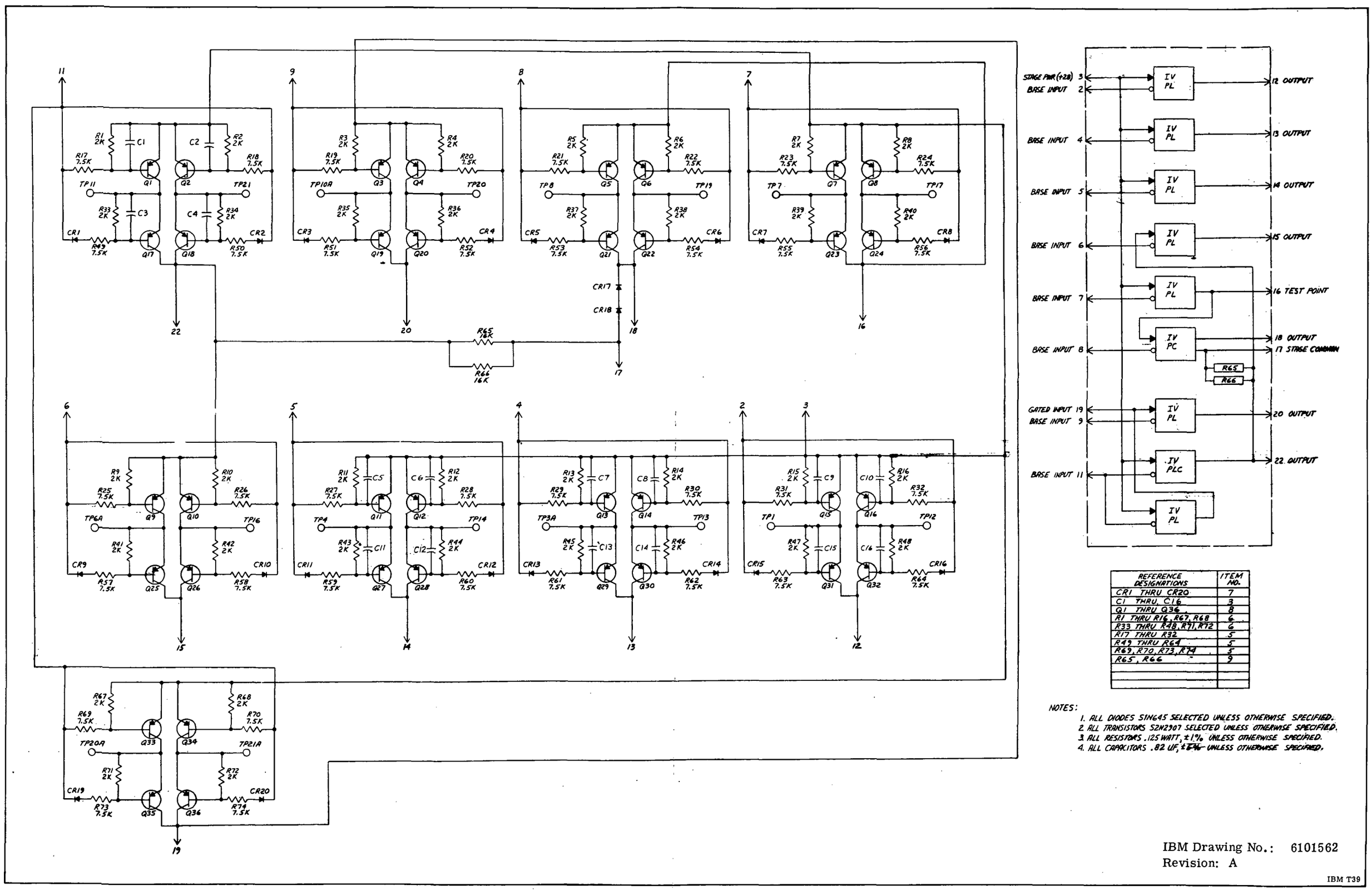
REFERENCE DESIGNATION	ITEM NO.
CR1 - CR18	4
R1, R5	6
R2 - R4	5
K1	7
K2, K3	8
C1, 2, 3	20

NOTES:
1 ALL DIODES ARE S1N645 SELECTED, UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101541
Revision: A

IBM T38

Figure 2-33. Electrical Schematic, Circuit Module Type 11, Read



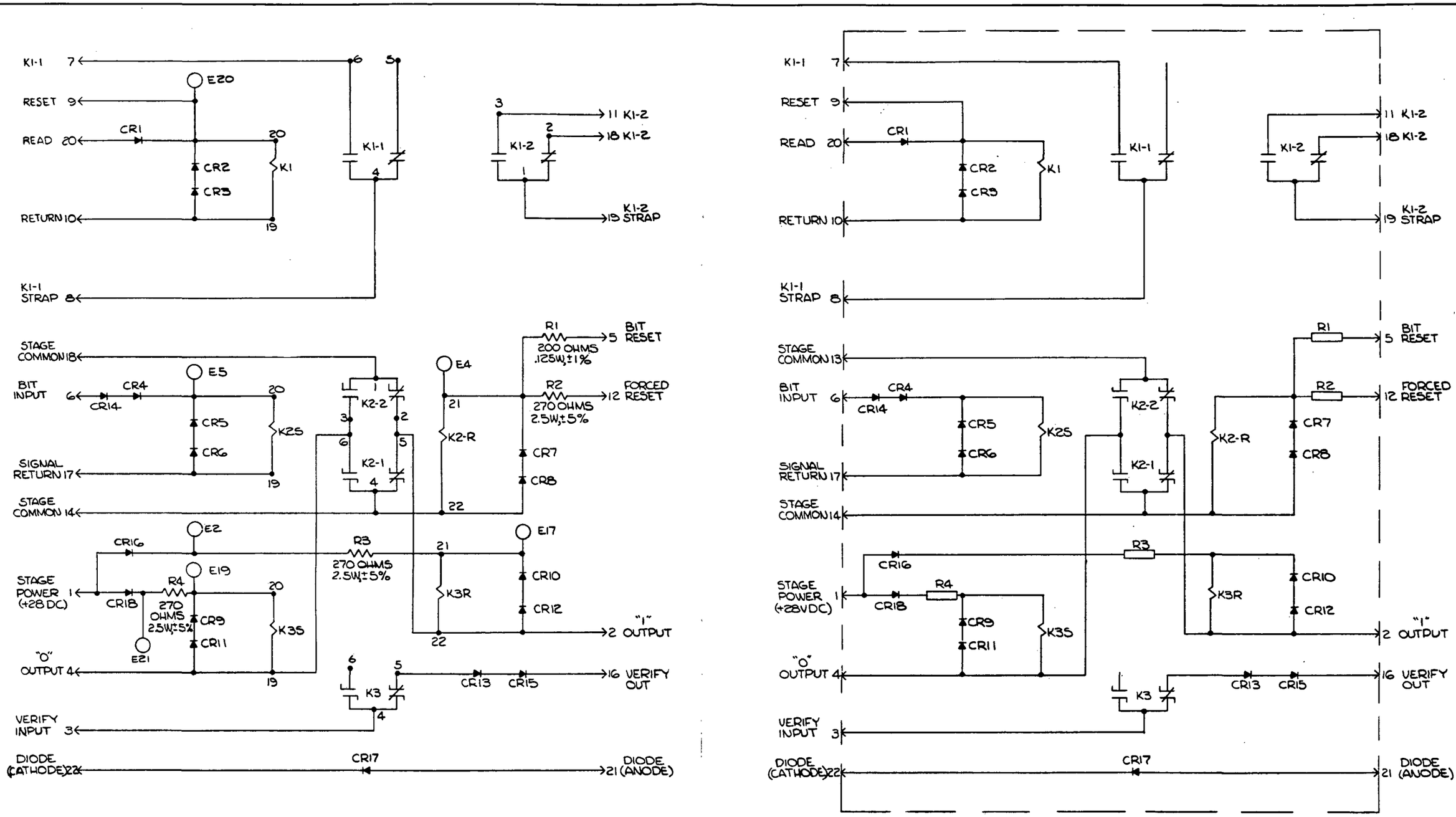
REFERENCE DESIGNATIONS	ITEM NO.
CR1 THRU CR20	7
C1 THRU C16	3
Q1 THRU Q36	8
R1 THRU R16, R67, R68	6
R33 THRU R48, R71, R72	6
R17 THRU R32	5
R49 THRU R64	5
R69, R70, R73, R74	5
R65, R66	9

NOTES:
1. ALL DIODES SING45 SELECTED UNLESS OTHERWISE SPECIFIED.
2. ALL TRANSISTORS S2N2907 SELECTED UNLESS OTHERWISE SPECIFIED.
3. ALL RESISTORS .125 WATT, ±1% UNLESS OTHERWISE SPECIFIED.
4. ALL CAPACITORS .82 UF, ±~~5%~~ UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101562
Revision: A

IBM T39

Figure 2-34. Electrical Schematic, Circuit Module Type 12, Miscellaneous Driver



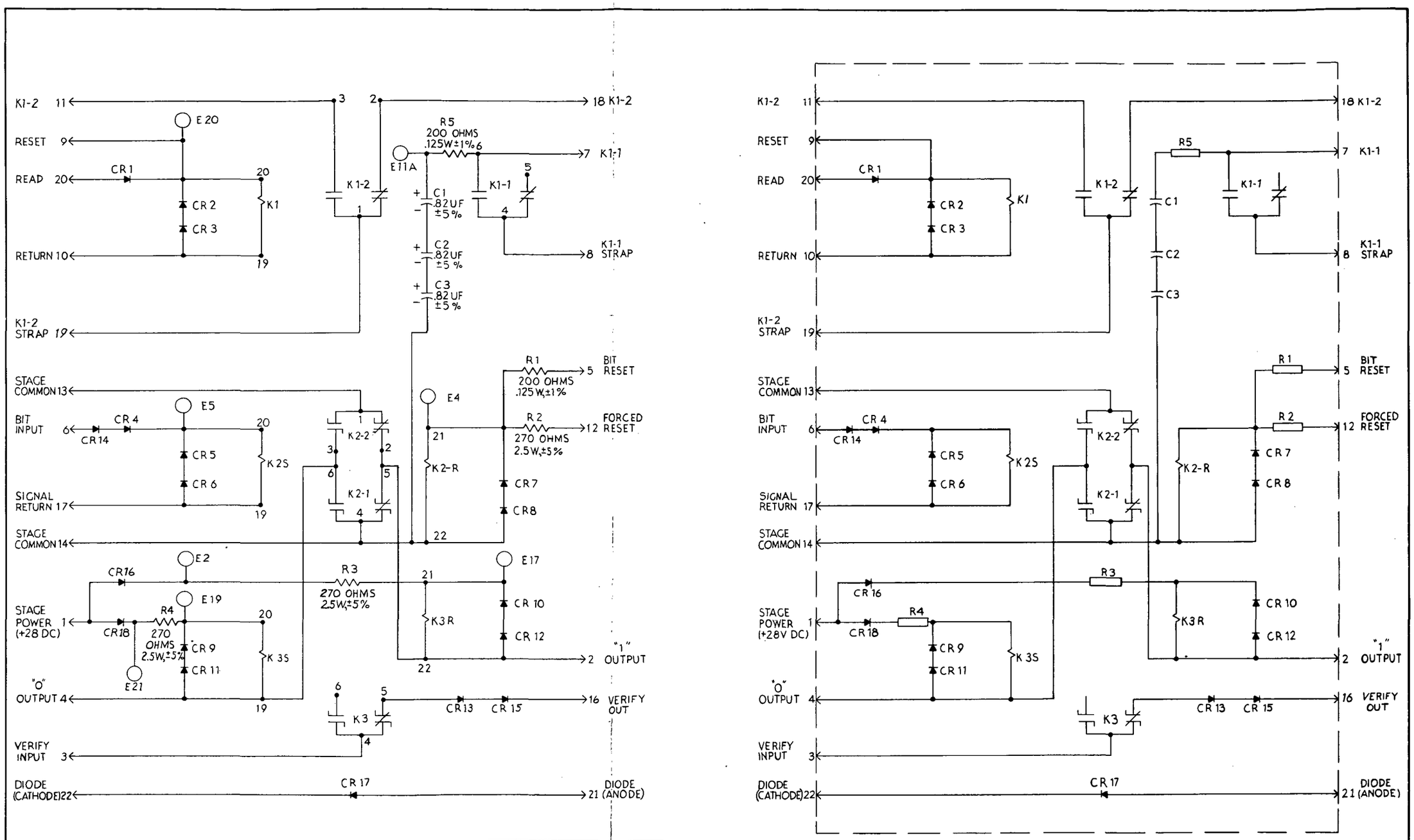
REFERENCE DESIGNATION	ITEM NO.
CR1-CR18	4
R1	6
R2-R4	5
K1	7
K2,K3	8

NOTES:
1. ALL DIODES ARE SING45 SELECTED, UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101563
Revision: A

IBM T40

Figure 2-35. Electrical Schematic, Circuit Module Type 13, Read



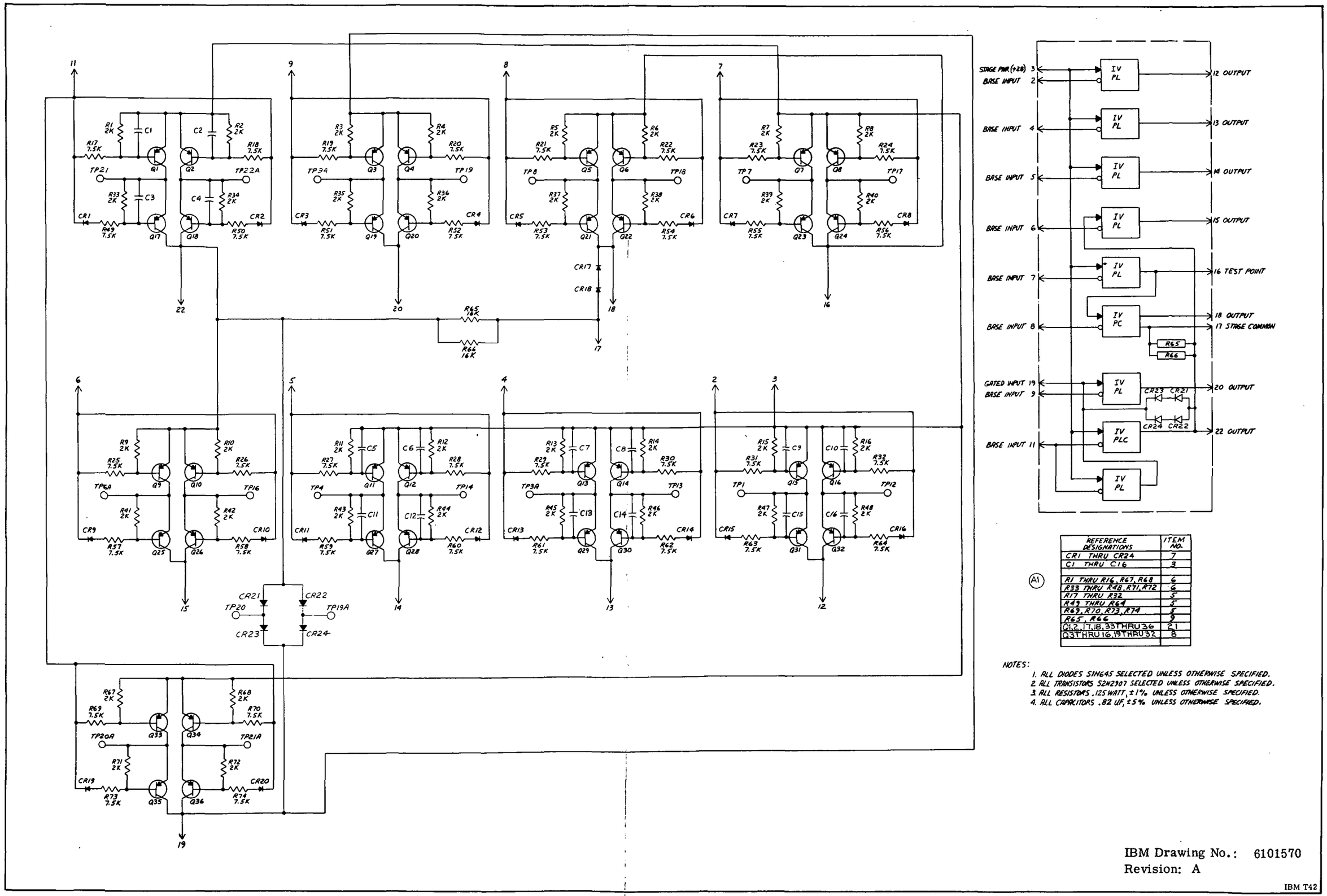
REFERENCE DESIGNATION	ITEM NO.
CR1-CR18	4
R1,R5	6
R2 - R4	5
K1	7
K2,K3	8
C1,2,3	20

NOTES:
1 ALL DIODES ARE S1N645 SELECTED, UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101564
Revision: "None"

IBM T41

Figure 2-36. Electrical Schematic, Circuit Module Type 14, Read



REFERENCE DESIGNATIONS	ITEM NO.
CR1 THRU CR24	7
C1 THRU C16	3
R1 THRU R16, R67, R68	6
R33 THRU R48, R71, R72	6
R17 THRU R32	5
R49 THRU R64	5
R69, R70, R73, R74	5
R65, R66	9
Q1,2,17,18,33 THRU 36	21
Q3 THRU 16, 19 THRU 32	8

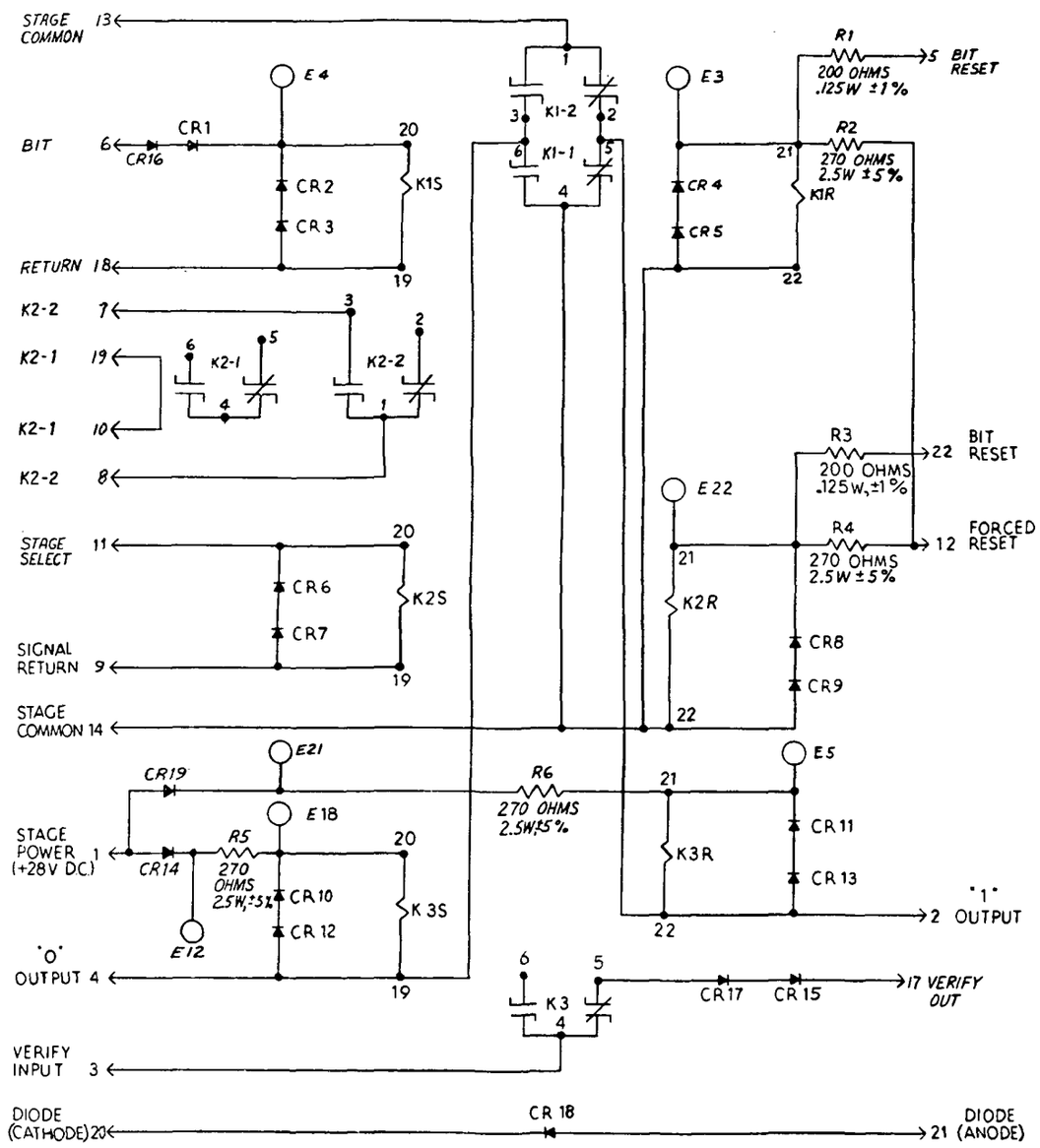
(A1)

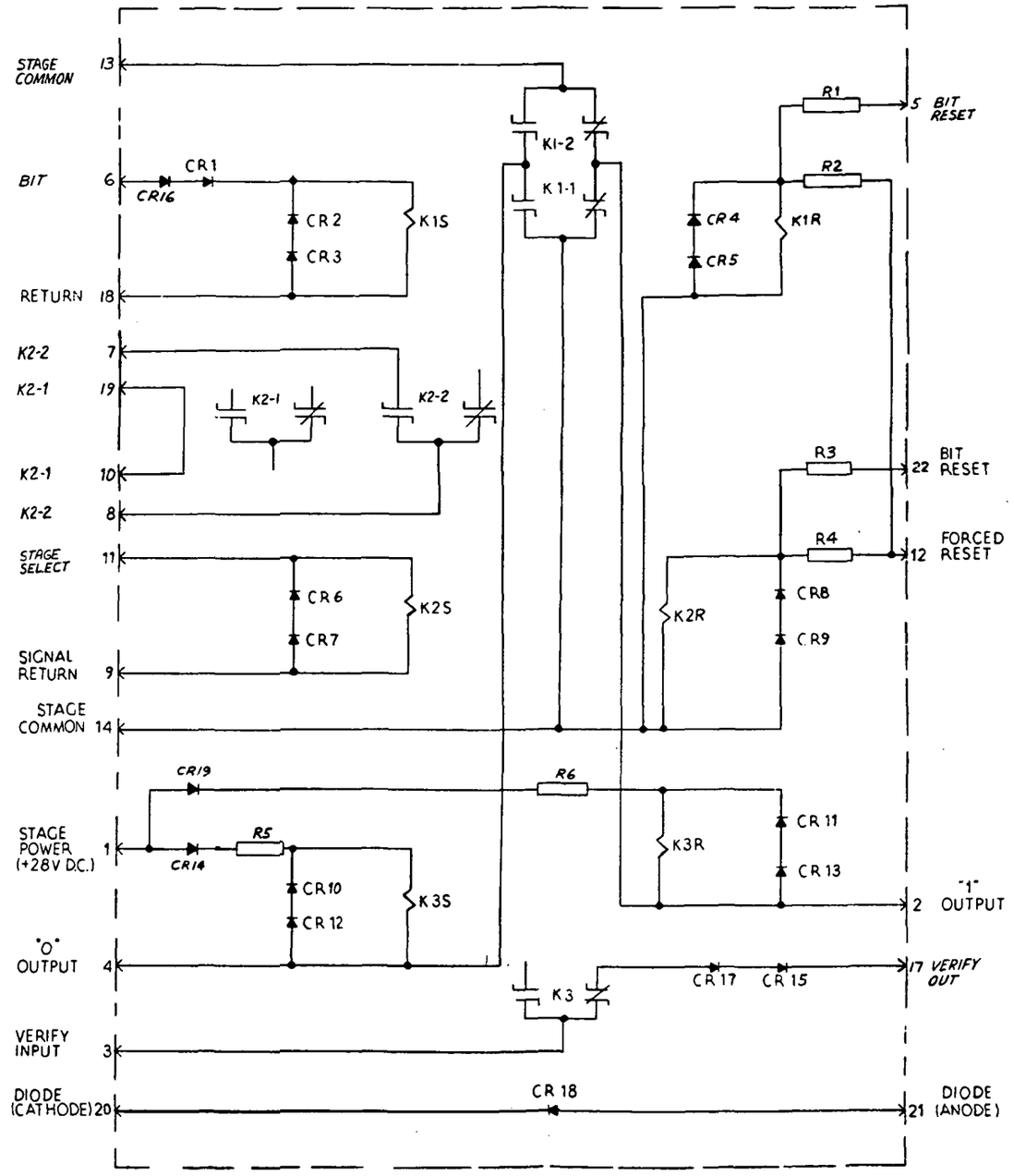
NOTES:
1. ALL DIODES SIN645 SELECTED UNLESS OTHERWISE SPECIFIED.
2. ALL TRANSISTORS S2N2907 SELECTED UNLESS OTHERWISE SPECIFIED.
3. ALL RESISTORS .125 WATT, ±1% UNLESS OTHERWISE SPECIFIED.
4. ALL CAPACITORS .82 UF, ±5% UNLESS OTHERWISE SPECIFIED.

IBM Drawing No.: 6101570
Revision: A

IBM T42

Figure 2-37. Electrical Schematic, Circuit Module Type 15, Decode





REFERENCE DESIGNATION	ITEM NO
CR1-CR19	4
R1, R3	6
R2, R4, R5, R6	5
K1, K2, K3	7

NOTES:
1 ALL DIODES ARE S1N645 SELECTED UNLESS OTHERWISE SPECIFIED

IBM Drawing No.: 6101578
Revision: "None"

IBM T43

Figure 2-38. Electrical Schematic, Circuit Module Type 16, Stage Select

SECTION III

PREPARATION FOR USE AND SHIPMENT

3-1 PREPARATION FOR USE

To remove the Switch Selector from its shipping container proceed as follows:

CAUTION

This is a reusable shipping container. Therefore, use care during the unpacking procedure to ensure the container is not damaged.

a. Slit tape on outer carton, and open carton.

b. Cut overwrap and moisture-vaporproof barrier bag so that the top of the inner carton is exposed.

c. Slit tape on inner carton, and open carton.

d. Check humidity indicator. The humidity indicator has three blue indicators, graduated to indicate thirty, forty, and seventy percent humidity. These indicators will turn pink when their respective percent of humidity has been reached. If the seventy percent indicator has turned pink, it is recommended that the Switch Selector be returned to the laboratory for inspection and testing.

e. Remove the taped fiberboard from around the Switch Selector.

f. Lift Switch Selector and plywood base from inner cartons.

g. Remove the 1-inch, 1/4 -20, socket-head cap screws securing the Switch Selector to the plywood base.

h. Unbolt Switch Selector from plywood base and remove Switch Selector from plywood base.

i. Place all parts of the shipping container, with the exception of the paper overwrap and moisture-vaporproof barrier bag, in the outer carton of the shipping container and retain. Discard the paper overwrap and moisture-vaporproof barrier bag.

j. Visually inspect the Switch Selector for physical damage and corrosion.

k. Remove dust covers and visually inspect the connectors for physical damage and corrosion

l. Replace dust covers until unit is ready for use.

3-2 PREPARATION FOR SHIPMENT

3-3 PACKAGING

The Switch Selector shall be packaged in accordance with Method IA-14 or Method III of Military Specification MIL-P-116. Determination of whether to use Method IA-14 or Method III is dependent upon the degree of protection required. Method III is to be used for local shipments when there will be no storage required. Method IA-14 shall be used for all other cases.

Items 1 through 4, of Figure 3-1, are required to package per Method III. Proceed as follows:

a. Bolt Switch Selector to plywood base using 1/4-20 x 1-inch, socket-head cap screws.

b. Install dust covers on connectors.

c. Place polyurethane pad on the bottom of the inner carton.

d. With Switch Selector secured, place plywood base on top of polyurethane pad.

e. Place taped fiberboard around Switch Selector.

f. Seal carton using pressure sensitive tape.

Except for markings, this completes the packaging procedure for Method III. If Method IA-14

is to be used, complete steps a. through f. and proceed with step g. Method IA-14 requires items 1 through 8 of Figure 3-1.

g. Blunt corners of inner carton to prevent damage to barrier bag.

h. Place inner carton in barrier bag.

i. Place humidity indicator on top of inner carton, inside the barrier bag. When the barrier bag is sealed, the humidity indicator will be between the inner carton and the barrier bag.

j. Heat seal the barrier bag when packaging a qualified Switch Selector. When packaging a defective unit, the barrier bag may be sealed with waterproof tape.

k. Overwrap the barrier bag with wrapping paper. Hold wrapping paper in place with pressure sensitive tape.

l. Apply a Method IA-14 process label on top of the wrapped inner carton. Record packaging data on label.

m. Place a Handi-pad cushion at each corner of the wrapped inner carton and place inner carton in outer carton.

n. Seal outer carton with 3-inch Kraft tape.

3-4 MARKING

Markings containing the following information shall be applied to the Switch Selector shipping container as follows:

Method III

A Switch Selector packaged per Method III shall have the following markings applied to the shipping container:

a. Print or stamp component part number on the taped fiberboard.

b. Print or stamp the following information on the top and both ends of carton:

- MSFC Number
- Item Description
- Quantity
- Contract Number
- Level of Preservation and Date
- Serial Number

c. Apply a Fragile label (IBM Part No. 7904880) to both ends of carton.

Method IA-14

The marking to be applied to a Method IA-14 shipping container is as follows:

a. Print or stamp component part number on taped fiberboard.

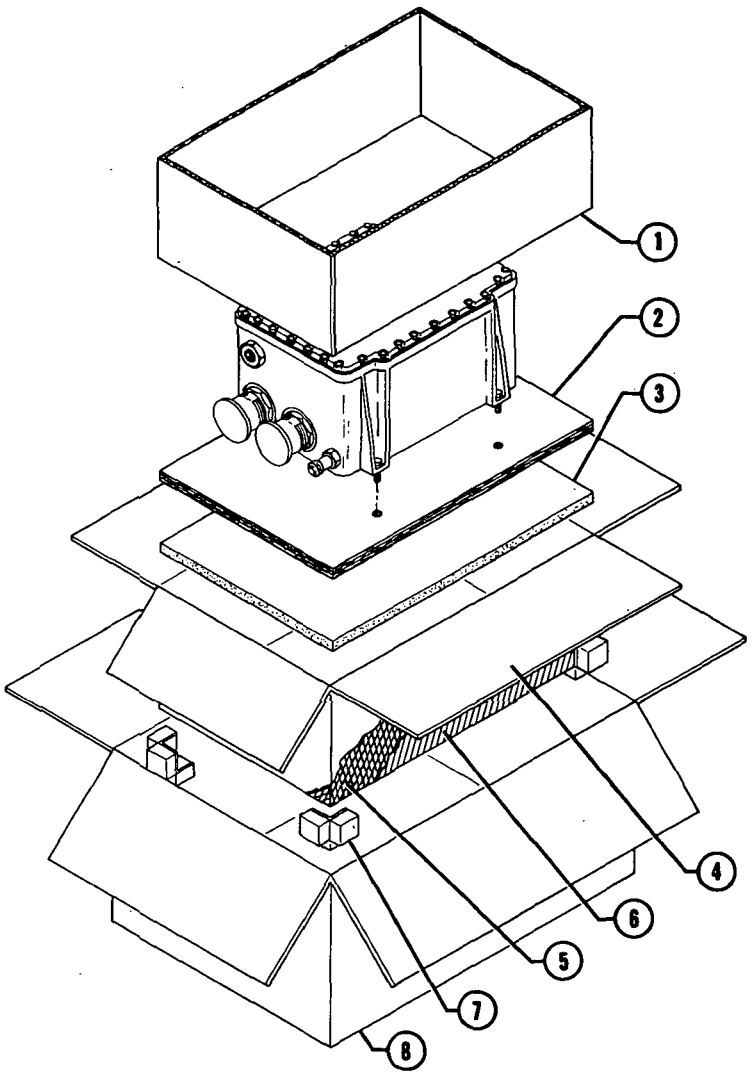
b. Apply markings containing the following information to the top of the inner carton. These markings shall be visible when inner carton is placed in the barrier bag.

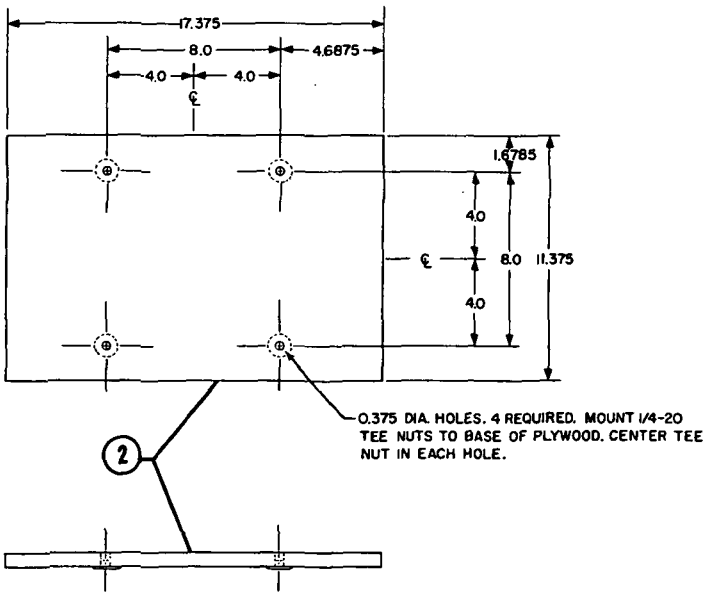
- MSFC Number
- Item Description
- Quantity
- Contract Number
- Level of Preservation and Date
- Serial Number

c. Apply the same markings applied in step b. to the paper overwrap covering the inner carton. Thes markings shall be visible when the inner carton is placed in the outer carton.

d. Apply the same marking applied in step b. to the top and both ends of outer carton.

e. Apply a Fragile label (IBM Part No. 7904880) to both ends of outer carton.





METHOD III

1 Taped Fiberboard
Material: "TWBC" flute corrugated fiberboard. 275 lb. test, per PPP-F-320, type CF, Class Dom.
IBM Drawing No. 6021004
Dimensions:
Length: 16.5 inches
Width: 10.5 inches
Height: 6.0 inches

2 Plywood Base
Material: 1/2 inch plywood per NN-P-515, type III, class I.
IBM Drawing No. 6021006
Dimensions: See detail drawing.

3 Polyurethane Pad
Material: Polyurethane foam cushioning, 4 lbs/cu ft density, per MIL-P-26514, type I, class II
IBM Drawing No. 6021005
Dimensions:
Length: 17.375 inches
Width: 11.375 inches
Thickness: 0.5 inches

4 Carton
Material: "TWBC" flute, 275 lb. test, per PPP-B-636, type I, class I
Style: RSC
IBM Drawing No. 6021002
Inside Dimensions:
Length: 17.5 inches
Width: 11.5 inches
Height: 7.0 inches

METHOD IA-14

Complete items **1** through **4**, then continue with item **5**

5 Water-vaporproof Barrier Bag
Material: MIL-B-117, type I, class E
Style: Envelope
IBM Drawing No. 6019460
Dimensions: 31.75 X 42.50 inches

6 Overwrap
Material: MIL-B-121, grade A wrapping paper
IBM Drawing No. 6019790
Dimensions: As required

7 Shock Cushions
Material: Hardi-pad cushioning, MIL-P-26514 type I, class II
IBM Drawing No. 6019490

8 Carton
Material: "TWBC" flute corrugated fiberboard. 275 lb. test, PPP-B-636, type I, class I.
Style: RSC
IBM Drawing No. 6021003
Inside Dimensions:
Length: 20.25 inches
Width: 14.25 inches
Height: 10.00 inches

IBM T44

Figure 3-1. Packaging Instructions for Switch Selector Mod II

SECTION IV

PREVENTIVE MAINTENANCE AND REPAIR

4-1 PREVENTIVE MAINTENANCE (Not Applicable)

4-2 REPAIR

All repairs to the Switch Selector will be accomplished by component replacement. If failure analysis determines repair is possible, the component shall be returned to the manufacturer for repair.

IBM®

Space Systems Center
Huntsville, Alabama

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