SATURN V

Laboratory Maintenance Instruction for LTE

Volume IV

LVDA Manual Exerciser

DRA

IBM

Federal Systems Division
Owego, New York

VOLUME IV OF V

Laboratory Maintenance Instructions

SATURN V
LAUNCH VEHICLE DIGITAL COMPUTER AND LAUNCH VEHICLE DATA ADAPTER TEST EQUIPMENT

International Business Machines Corporation

Contract NAS 8-11561

VOLUME IV

Launch Vehicle Data Adapter Manual Exerciser (IBM Part No. 6942000)

5 MARCH 1965

LIST OF EFFECTIVE PAGES

INSERT LATEST CHANGED PAGES. DESTROY SUPERSEDED PAGES.

TOTAL NUMBER OF PAGES IN VOLUME IV OF THIS PUBLICATION IS 620
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LIST OF RELATED MANUALS

Equipment	Manufacturer	Manual Title
Analog-Digital Converter VR13-AB/NE	Adage, Inc.	VR13-AB/NE/VMX40B/VMX8DB Instruction Manual
Multiplexer VMX40B/VMX8DB	Adage, Inc.	
Automated Logic Diagrams	IBM Corporation	Saturn V LTE-LVDA Manual Exerciser Automated Logic Diagrams

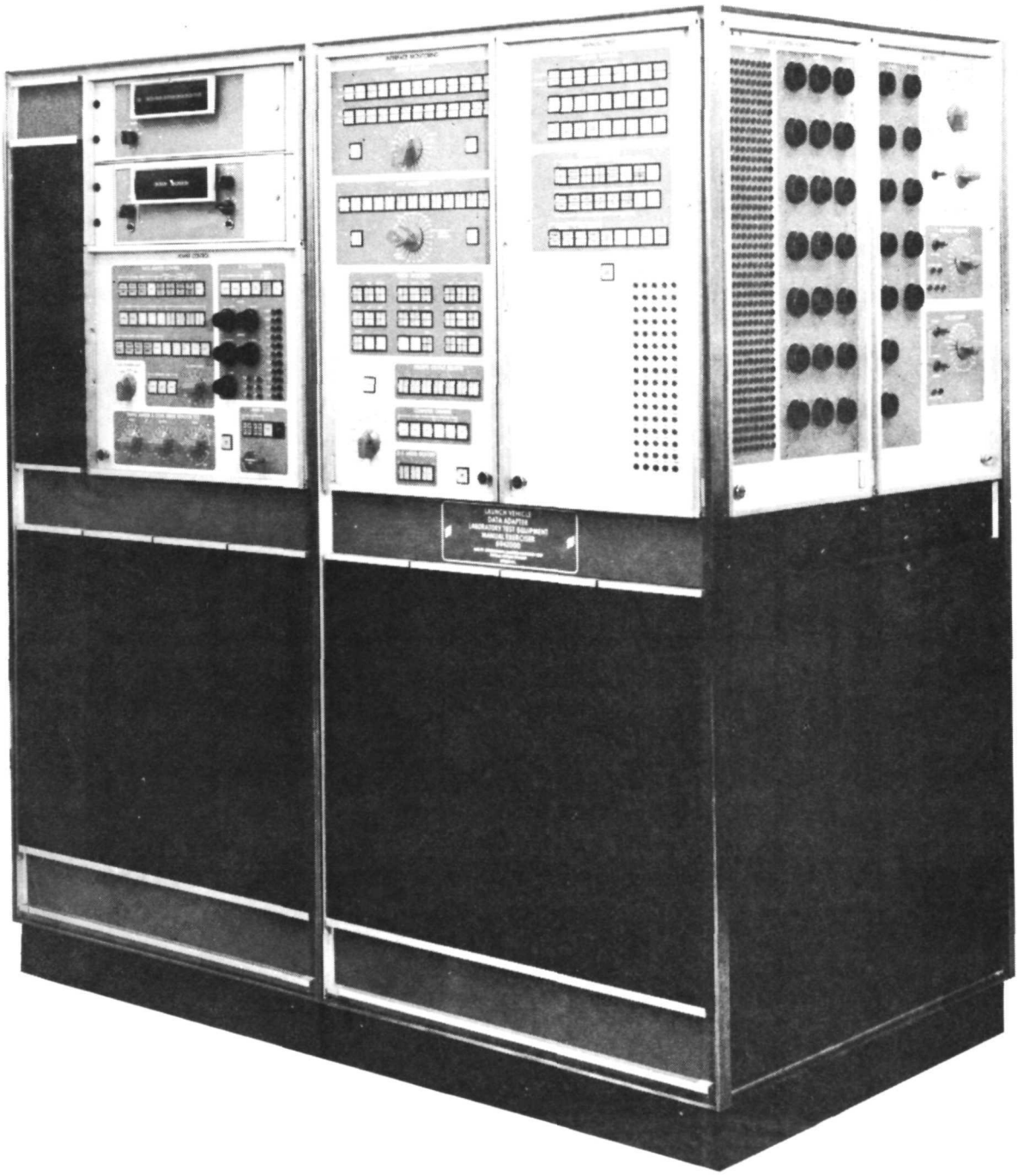


Figure 1-1. Launch Vehicle Data Adapter Manual Exerciser (LVDAME)

SECTION I

INTRODUCTION AND DESCRIPTION

1-1. SCOPE.

1-2. This section outlines the contents of this volume and specifies related publications and documents. This section also presents a general physical description of the Launch Vehicle Data Adapter Manual Exerciser and its major component assemblies.

1-3. INTRODUCTION.

1-4. PURPOSE OF THIS VOLUME.

1-5. This volume of the manual provides operating and maintenance instructions for the Saturn V Launch Vehicle Data Adapter Manual Exerciser (LVDAME), IBM part number 6942000, shown on figure 1-1. The LVDAME is manufactured by the International Business Machines Corporation, Federal Systems Division, Rockville, Maryland.

1-6. CONTENTS. This volume is composed of ten sections as follows:

Section I Introduction and Description

Section II Theory of Operation

Section III Interface and Controls

Section IV Test Equipment and Special Tools

Section V Preparation for Use, Storage and Shipment

Section VI Preventive Maintenance

Section VII Calibration

Section IX Repair

Section X Diagrams

At the beginning of each section a paragraph labeled SCOPE describes the contents of the section and relates the contents of the section to applicable contents of other sections.

1-7. A glossary and index are located at the back of the volume. The glossary lists signal names and acronyms in alphabetical order. (Standard abbreviations in this volume conform with military standard MIL-STD-12B.) The topical index indicates the page or pages on which the discussion of a topic begins.

1-8. RELATED MANUALS. Maintenance information for LVDAME assemblies not built or modified by the Federal Systems Division is not included in this volume. This information is contained in commercial manuals. The List of Related Manuals in the front of this volume lists the titles and source of supply for these manuals.

1-9. Four copies of LVDAME Automated Logic Diagrams (ALD's) are also supplied by the IBM Corporation; the title of the books containing these diagrams is included in the List of Related Manuals.

1-10. LOGIC SYMBOLS. The logic symbols used in this volume and on the ALD's are defined in the table of logic symbols. A discussion of the physical layout and interpretation of the ALD's is included in Section X.

1-11. PART SYMBOLS. Symbols for standard electrical and electronic parts conform with military standard MIL-STD-15-1.

1-12. REFERENCE DESIGNATIONS. Reference designations for standard electrical and electronic parts conform with military standard MIL-STD-16B.

1-13. PURPOSE OF THE LVDAME.

1-14. The purpose of the LVDAME is to evaluate a Launch Vehicle Data Adapter by either the ADAPT or ASTEC laboratory test configurations. (Refer to Volume I of this manual for information concerning these test configurations.)

1-15. The Launch Vehicle Data Adapter models to which the LVDAME can be connected are manufactured by the IBM Federal Systems Division. The NASA and IBM part numbers of these units are as follows:

Type and Model Number	NASA Part Number	IBM Part Number
Engineering Breadboard No. 2	50M35011	6112070
Triple-Modular-Redundant No. 1		6112000
Triple-Modular-Redundant No. 2		
Triple-Modular-Redundant No. 3		6139800
Triple-Modular-Redundant No. 4		
Production No. 1		6139400

1-16. DESCRIPTION.

1-17. BASIC CONSTRUCTION.

1-18. The LVDAME is composed of two frames (01 and 02) bolted together to form a unit 58 inches wide, 31 inches deep and 60 inches high that weighs approximately 1900 pounds. Frames 01 and 02 are composed of cubic modules. The upper module in each frame is designated module A; the lower module in each frame is designated module B.

1-19. Each module is composed primarily of hinged or slide mounted assemblies that can be pulled out from the frame to facilitate servicing the LVDAME. The side covers of each module can be removed to facilitate servicing assemblies that are fixed to the LVDAME frames.

1-20. Filtered openings at the base of the LVDAME permit the intake of cooling air. The cooling air is circulated through the LVDAME by fans and expelled through screened openings in the top of the LVDAME.

1-21. Casters at the bottom of each frame facilitate moving the LVDAME.

1-22. MAJOR ASSEMBLIES.

1-23. Each LVDAME assembly has a reference designation which identifies its location in the LVDAME. Each major assembly is referenced by a four-character designation that identifies the frame (01 or 02), module (A or B), and module assembly number (1 through 8) of the assembly. For example, the reference designation for assembly 1 in module A of frame 02 is 02A1.

1-24. The assignment of numbers for assemblies in a typical module is shown on figure 1-2. A movable assembly in position 1, 2, 3, or 4 opens to the front of the module; a movable assembly in position 5, 6, 7, or 8 opens to the rear of the module.

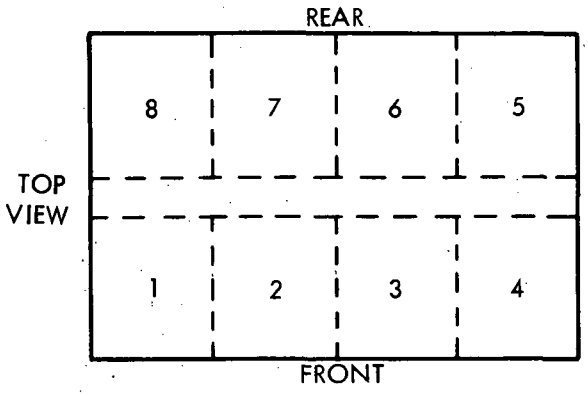


Figure 1-2. Numbering System for Module Assemblies

1-25. The location of each major LVDAME assembly is shown on figure 1-3. The assembly name and reference designation of each assembly is shown in the legend for figure 1-3.

1-26. A brief description of each assembly shown on figure 1-3 is given in figure 1-4.

1-27. GATE ASSEMBLIES. The swinging gate assemblies contain the many printed circuit board assemblies that constitute the LVDAME logic circuitry. The gate assemblies and printed circuit board assemblies are discussed in detail in the following paragraphs.

1-28. Mechanical Features of the Gate Assemblies. The gate assemblies are hinged as shown on figure 1-5. Gate assemblies in B modules swing up to open; those in A modules swing down.

1-29. Figure 1-6 illustrates a module B gate assembly in its fully extended position. The gate assembly is extended from the frame by pulling handle 2 toward handle 1 (to release the holding mechanism shown on figure 1-9) and pulling the gate assembly to the desired position in its arc; the gate assembly is stopped in its arc when handle 2 is released.

(Text continued on page 1-10.)

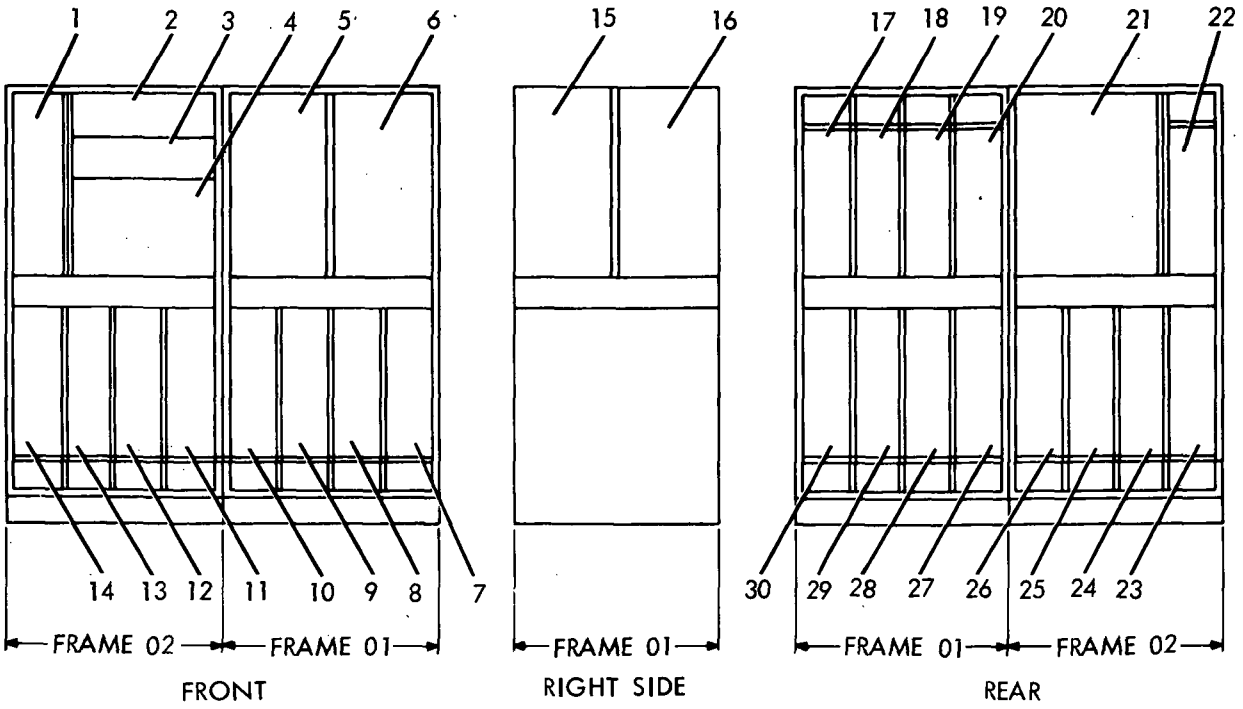


Figure 1-3. LVDAME Assembly Locations

Legend for Figure 1-3

Index Number	Assembly Name and Reference Designation
1	Power Supply Assembly (02A1)
2	Analog/Digital Converter (02A2)
3	Multiplexer (02A3)
4	Power Control Panel Assembly (02A6)
5	Interface Monitoring Panel Assembly (01A1)
6	Manual Test Panel Assembly (01A2)
7	Gate Assembly (01B4)
8	Gate Assembly (01B3)
9	Gate Assembly (01B2)
10	Gate Assembly (01B1)

Legend for Figure 1-3 (cont)

Index Number	Assembly Name and Reference Designation
11	Gate Assembly (02B4)
12	Gate Assembly (02B3)
13	Gate Assembly (02B2)
14	Power Supply Assembly (02B1)
15	Data Adapter Interface Panel Assembly (01A3)
16	Self-Test Panel Assembly (01A4)
17	Cover (01A5)
18	Gate Assembly (01A6)
19	Gate Assembly (01A7)
20	Gate Assembly (01A8)
21	Power Supply Assembly (02A7)
22	Power Supply Assembly (02A8)
23	AC Power Box Assembly (01B8)
24	Gate Assembly (02B7)
25	Relay Chassis Assembly (02B6)
26	Gate Assembly (02B5)
27	Gate Assembly (01B8)
28	Gate Assembly (01B7)
29	Gate Assembly (01B8)
30	Gate Assembly (01B5)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturer's Designation	Manufacturer	Description
01B7	28	Gate Assembly	6940800	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
01B8	27	Gate Assembly	6940900	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
02A1	1	Power Supply Assembly	6943500	IBM Corp.	Slide mounted. Supplies -12 VDC and +12 VDC for LVDAME logic circuits
02A2	2	Analog/Digital Converter	Model VR13-AB/NE (6942330)	Adage, Inc.	Secured to mounting rack by four screws; front panel is hinged at left. Converts LVDA analog outputs and special simulation lab signals to a digital format.
02A3	3	Multiplexer	Model VMX40B/VMX8DB (6942340)	Adage, Inc.	Secured to mounting rack by four screws; front panel is hinged at left. Provides signal selection of 48 channels for application to the Analog/Digital Converter.
02A6	4	Power Control Panel Assembly	6941100	IBM Corp.	Hinged on right side. Contains controls, indicators, and voltage monitoring test points for controlling the power applied to the LVDAME and the LVDA under test. (Refer to figure 3-7 for the description of each control and indicator on this panel.)
02A7	21	Power Supply Assembly	6943300	IBM Corp.	Hinged on left side. Supplies -6VDC and -36 VDC for LVDAME logic circuits.
02A8	22	Power Supply Assembly	6943400	IBM Corp.	Slide mounted. Supplies -12 VDC for LUDAME logic circuits.
02B1	14	Power Supply Assembly	6941200	IBM Corp.	Fixed to frame; accessible when side panel is removed. Contains regulators for three-phase AC power.
02B2	13	Gate Assembly	6941300	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
02B3	12	Gate Assembly	6941400	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
02B4	11	Gate Assembly	6941500	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
02B5	26	Gate Assembly	6941600	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
02B6	25	Relay Chassis Assembly	6941700	IBM Corp.	Hinged on top. Contains relays that control sequencing of voltages during power-up and power-down operations.

Figure 1-4. LVDAME Assemblies (Sheet 1 of 3)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturer's Designation	Manufacturer	Description
01A1	5	Interface Monitoring Panel Assembly	6942300	IBM Corp.	Hinged on left side. Contains controls and indicators for monitoring the performance of the LVDA under test. (See figure 3-7 for the description of each control and indicator on this panel.)
01A2	6	Manual Test Panel Assembly	6942400	IBM Corp.	Hinged on right side. Contains controls and indicators for manually testing the LVDA. The test points on this panel are for monitoring certain LVDAME signals. (See figure 3-7 for the description of each control and indicator on this panel.)
01A3	15	Data Adapter Interface Panel Assembly	6942500	IBM Corp.	Hinged on right side. Contains connectors for cables to the LVDA under test and test points for monitoring selected signals from the LVDA under test. (See figure 3-7 for the drawings that indicate the signal at each connector pin or test point.)
01A4	16	Self-Test Panel Assembly	6942600	IBM Corp.	Hinged on left side. Contains controls used to operate the LVDAME in the self-test mode and connectors for cables to the LVDA under test. (See figure 3-7 for the description of each control on this panel.)
01A5	17	Cover	597342	IBM Corp.	Dummy gate assembly cover. The self-test panel assembly occupied the space that would be occupied by a gate assembly in this position.
01A6	18	Gate Assembly	6942700	IBM Corp.	Hinged on bottom. Contains LVDAME logic circuits.
01A7	19	Gate Assembly	6942800	IBM Corp.	Hinged on bottom. Contains LVDAME logic circuits.
01A8	20	Gate Assembly	6942900	IBM Corp.	Hinged on bottom. Contains LVDAME logic circuits.
01B1	10	Gate Assembly	6940200	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
01B2	9	Gate Assembly	6940300	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
01B3	8	Gate Assembly	6940400	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
01B4	7	Gate Assembly	6940500	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
01B5	30	Gate Assembly	6940600	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
01B6	29	Gate Assembly	6940700	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.

Figure 1-4. LVDAME Assemblies (Sheet 2)

Reference Designation	Index Number (Figure 1-3)	Name	Part Number or Manufacturer's Designation	Manufacturer	Description
02B7	24	Gate Assembly	6941800	IBM Corp.	Hinged on top. Contains LVDAME logic circuits.
02B8	23	AC Power Box Assembly	6941900	IBM Corp.	Fixed to frame; accessible when side panel is removed. Contains AC power control circuits for power supplies and fans; contains elapsed time meter.

Figure 1-4. LVDAME Assemblies (Sheet 3)

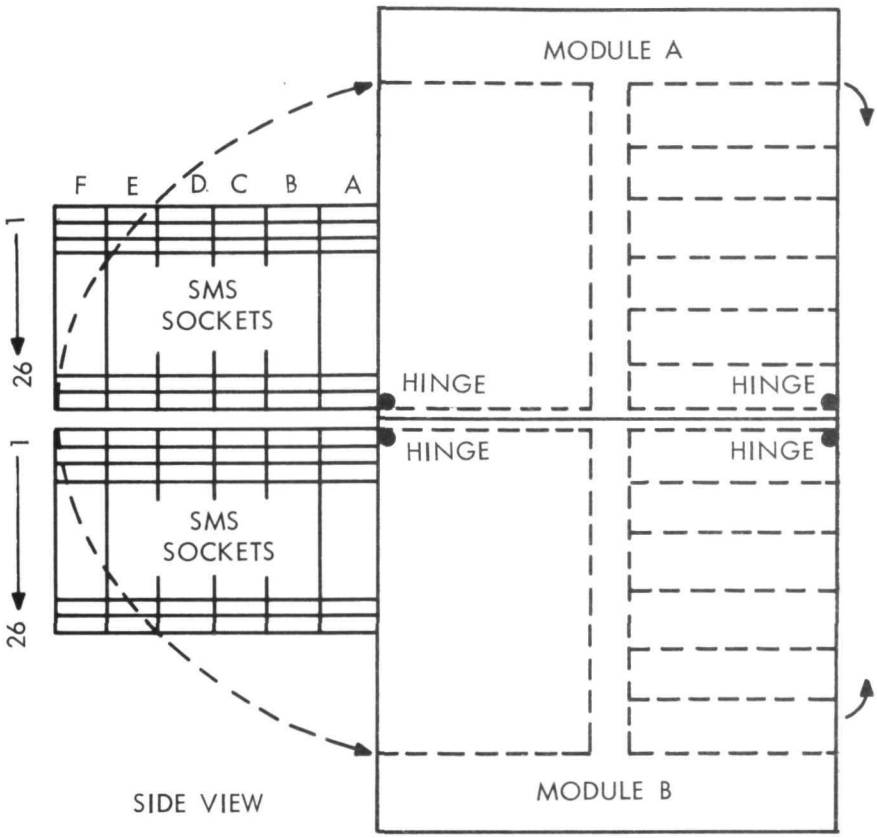


Figure 1-5. Gate Assembly Movement

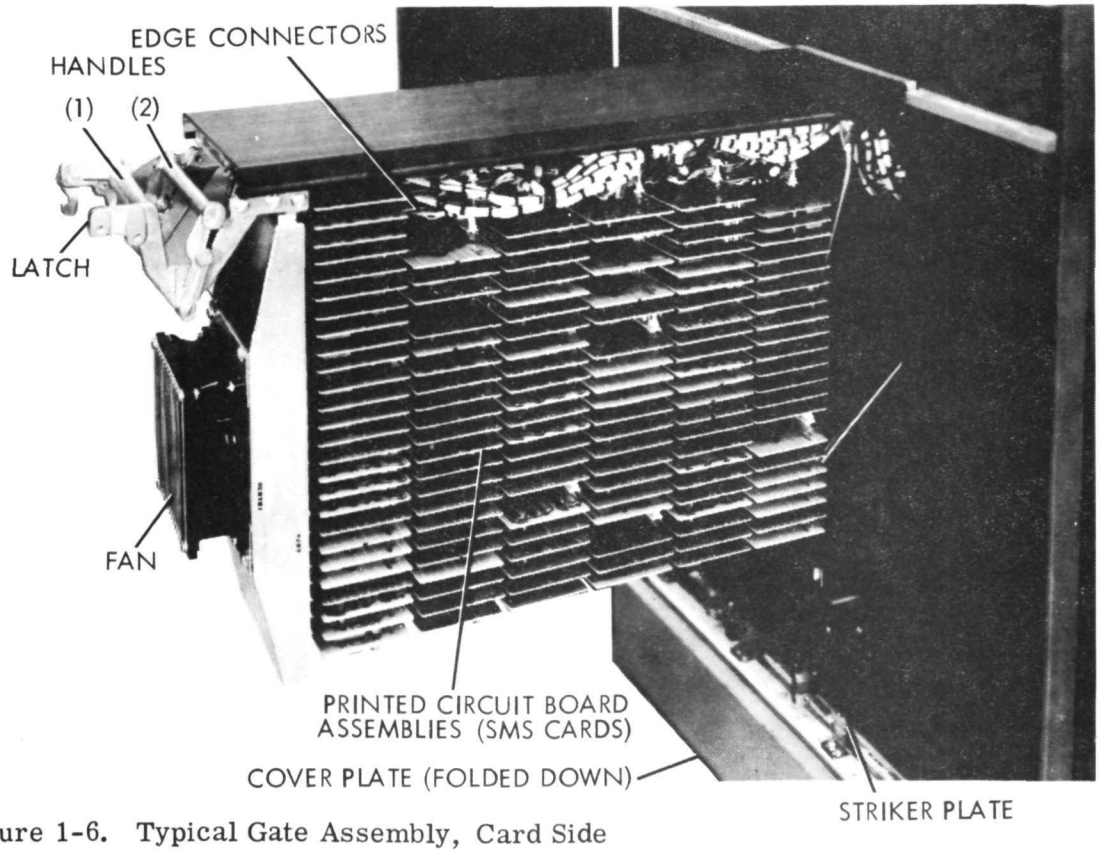


Figure 1-6. Typical Gate Assembly, Card Side

1-30. Access to the gate assembly handles is gained by rotating the cover plate away from the gate assembly. Cover plates for gate assemblies in B modules must be turned down, as shown on figure 1-6; those for assemblies in A modules must be turned up. The cover plate cannot be returned to its normal position until the gate assembly is returned into the frame. The latch engages the striker plate to hold the gate assembly in the frame.

1-31. As indicated on figure 1-6, a fan is mounted on the gate assembly to force cooling air over the logic circuits on the printed circuit board assemblies. The fans for module A gate assemblies are mounted on the tops of the gate assemblies, fans for module B gate assemblies are mounted on the bottom of the gate assemblies.

1-32. Each gate assembly contains 156 card sockets arranged in six columns and 26 rows. These sockets are the receptacles for the printed circuit board assemblies. Normally, the sockets in rows 1 and 2 of gate assemblies in the B modules and the sockets in rows 25 and 26 of gate assemblies in the A modules are used for cable connectors. The cables that plug into these sockets are called edge connectors, since they make their connections at the edges of the gate assemblies.

1-33. Standard Modular System (SMS) Logic Cards. The logic circuits in the LVDAME are contained on printed circuit board assemblies called IBM Standard Modular System (SMS) cards. These pluggable printed circuit cards contain all the components and printed wiring necessary for a particular electronic function. A special program cap on some SMS printed circuit cards gives additional flexibility to this form of packaging, and reduces the number of cards required for field servicing. Each card is identified by a four-character card type code and a six-or seven-digit IBM part number. (See figure 1-7.)

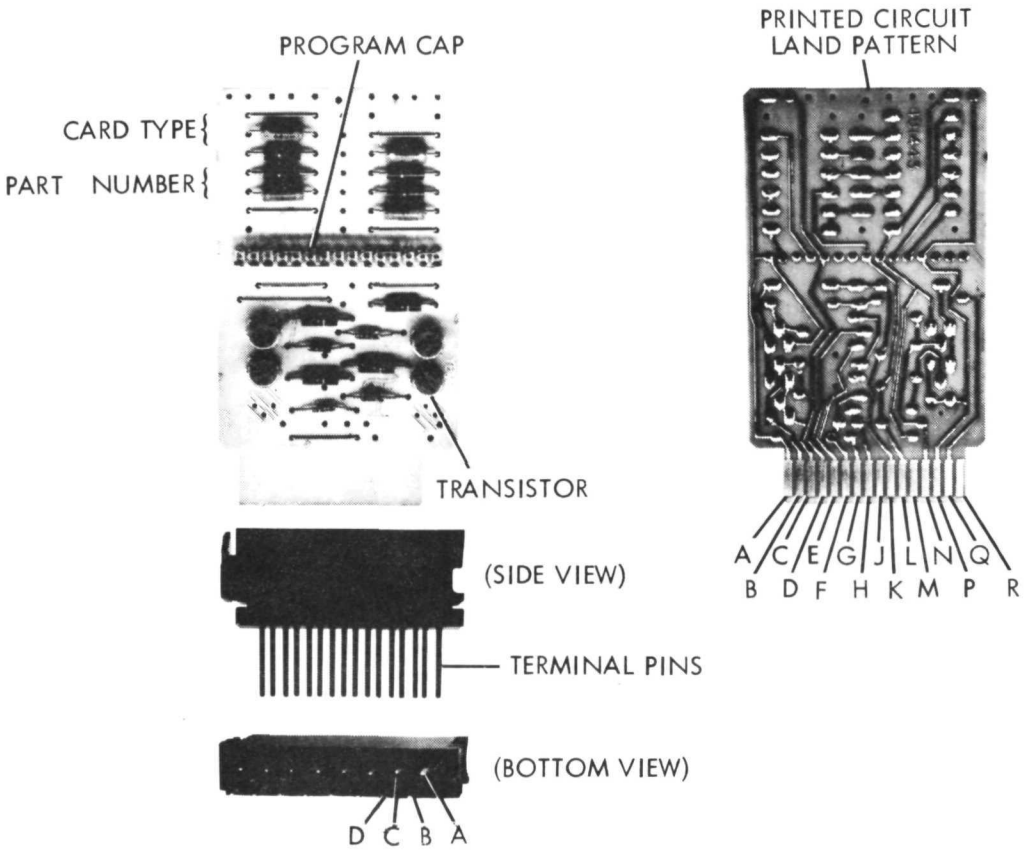


Figure 1-7. SMS Printed Circuit Card and Single-Position Receptacle

1-34. The SMS single card, the kind used in the LVDAME, is made of an epoxy paper laminate material; it is approximately 1/16 inch thick, 4-1/2 inches long, and 2-1/2 inches wide. All of the electronic components and the program cap, if used, are mounted on the front side of the SMS card form. Connections to the components and program cap are made on the back side of the SMS card form by printed wiring patterns that terminate at contacts at the bottom of the card. These contacts, labeled A through R, couple the signals and voltages to the circuit components when the card is inserted into its receptacle. The printed circuit wiring (land pattern) depends on the type of circuit on the card.

1-35. The program cap on the front of some SMS cards comprises two conductor rails which, in the pre-cut state, connect to tabs on the printed circuit land pattern. By cutting the program cap, various jumpering (cap) connections are made to the tabs to allow one SMS card to be used in several circuit configurations.

1-36. SMS Card Receptacles. The pluggable printed circuit cards are inserted into SMS card receptacles. The receptacles used in the LVDAME are the single-position type, shown on figure 1-7, and the eight-position type, which serves as a common receptacle for eight SMS cards, as shown on figure 1-8. Although the contacts are all in line on the card insertion side of the receptacle, they pass through the receptacle in a staggered arrangement. This arrangement allows additional room for wire-wrapping or soldering of wires to the terminal pins, as shown on figure 1-9.

1-37. Figure 1-9 shows how the pins of each SMS card (and receptacle) are identified, using an extension of the reference designation discussed previously.

1-38. Voltage Distribution Assemblies. Figure 1-9 also illustrates the standard position for a voltage distribution assembly in a module B gate assembly. A typical voltage distribution assembly is shown on figure 1-10.

1-39. Each voltage distribution assembly contains a primary group of eight terminals and six secondary groups of eight terminals. Power is distributed within the assembly from the primary terminals to the secondary terminal of the same number; for example, power applied to the number 1 primary terminal is distributed to the eight number 1 secondary terminals of the voltage distribution assembly. Each secondary group of terminals transfers power to one row of SMS cards by jumpers from the secondary terminals to the SMS card receptacle pins. The jumpers from the secondary terminals are usually connected only to the pin of the nearest receptacle in which the voltage is used. From this first receptacle a voltage bus transmits the power to the pins of other receptacles in that row. Usually a particular voltage is restricted to pins of the same letter; for example, the K pin of most receptacles is connected to -6 VDC.

1-40. CONTROL PANELS. Each LVDAME control panel is divided into areas in which associated controls and indicators are mounted. The function of each group of controls and indicators is indicated by a prominent title in each area. Figure 3-7 (in Section III) lists and briefly describes all controls and indicators on these panels.

1-41. POWER SUPPLIES. The power supplies that furnish DC power to the LVDAME and the data adapter under test are housed in the LVDAME and the Equipment Test Stand (ETS).

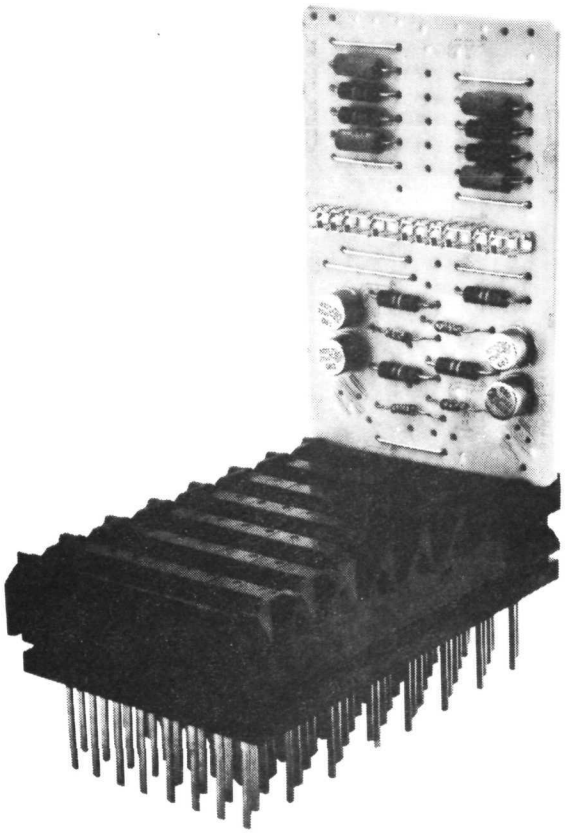


Figure 1-8. SMS Printed Circuit Card Inserted in Eight-Position Receptacle

NOTE

The Equipment Test Stand (IBM part number 6943000) shown on figure 1-11 is discussed in Volume II of this manual.

1-42. The LVDAME contains the controls, indicators, and test points for controlling the power supplies in the LVDAME and the ETS. Resistor networks in the LVDAME allow the output voltages of the ETS power supplies to be varied plus or minus one volt. The potentiometers in these resistor networks are mounted on the POWER CONTROL panel.

1-43. ELECTRICAL, MECHANICAL, AND ENVIRONMENTAL CHARACTERISTICS.

1-44. Figure 1-12 lists the salient electrical, mechanical, and environmental characteristics of the LVDAME.

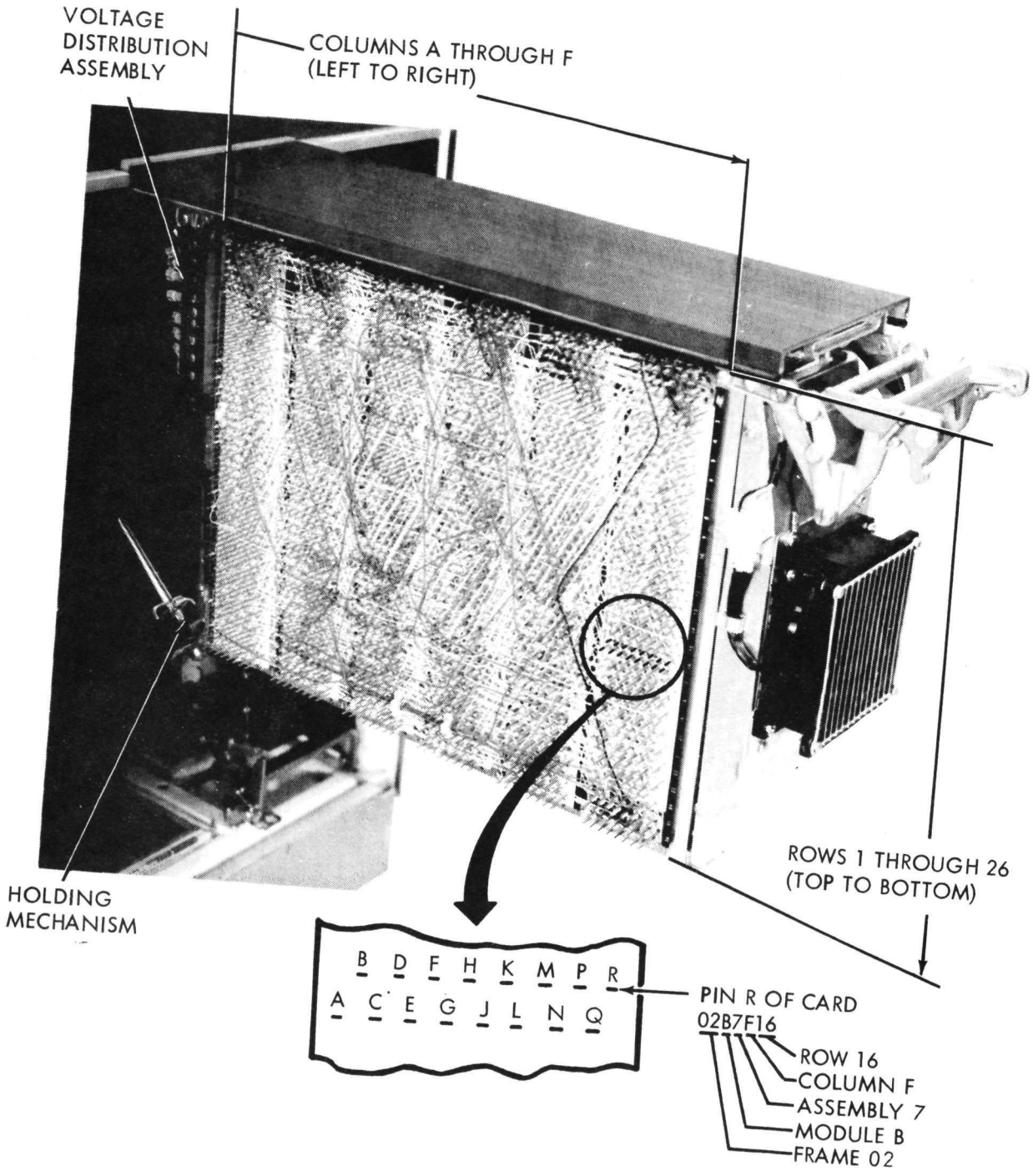


Figure 1-9. Typical Gate Assembly, Wiring Side

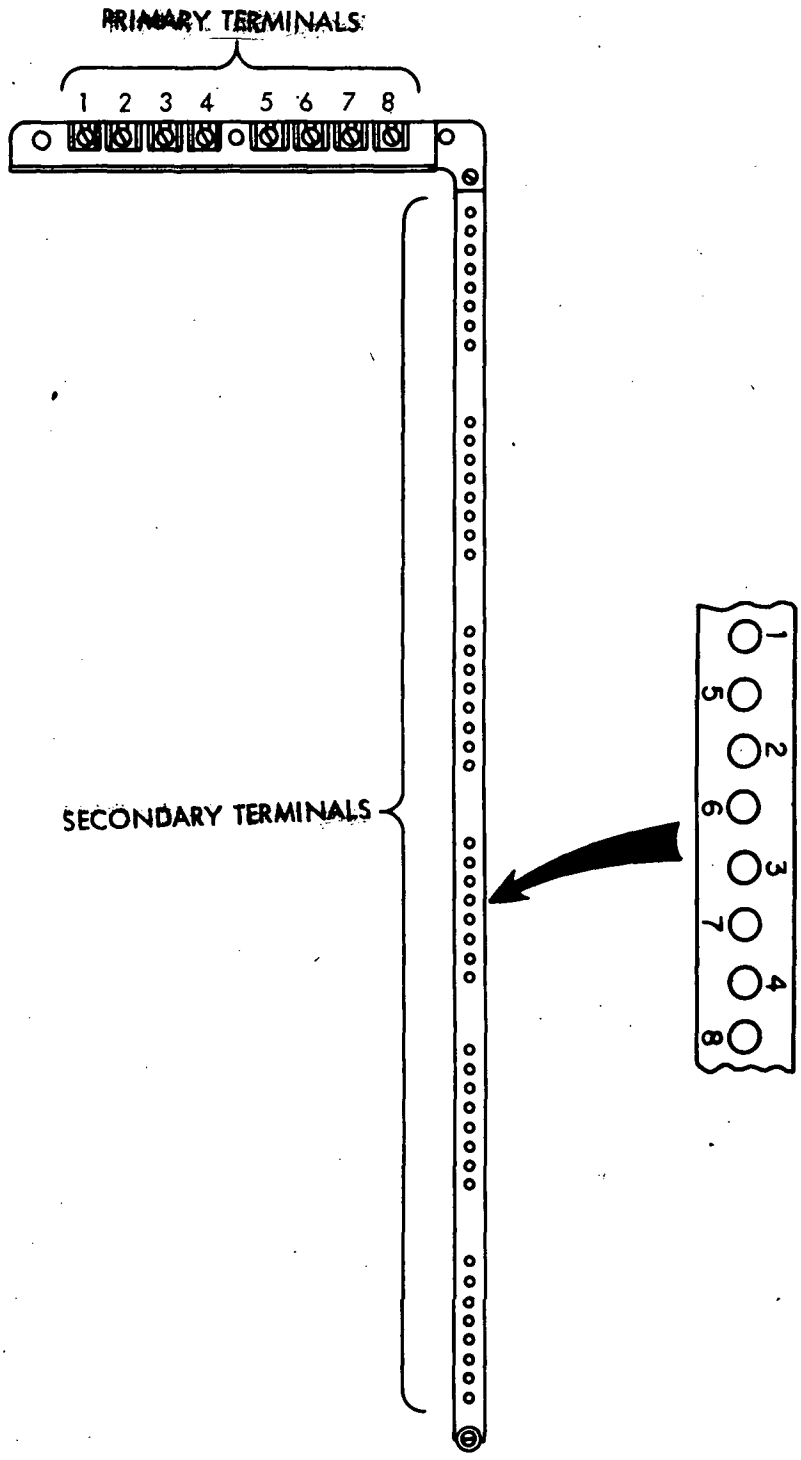


Figure 1-10. Typical Voltage Distribution Assembly

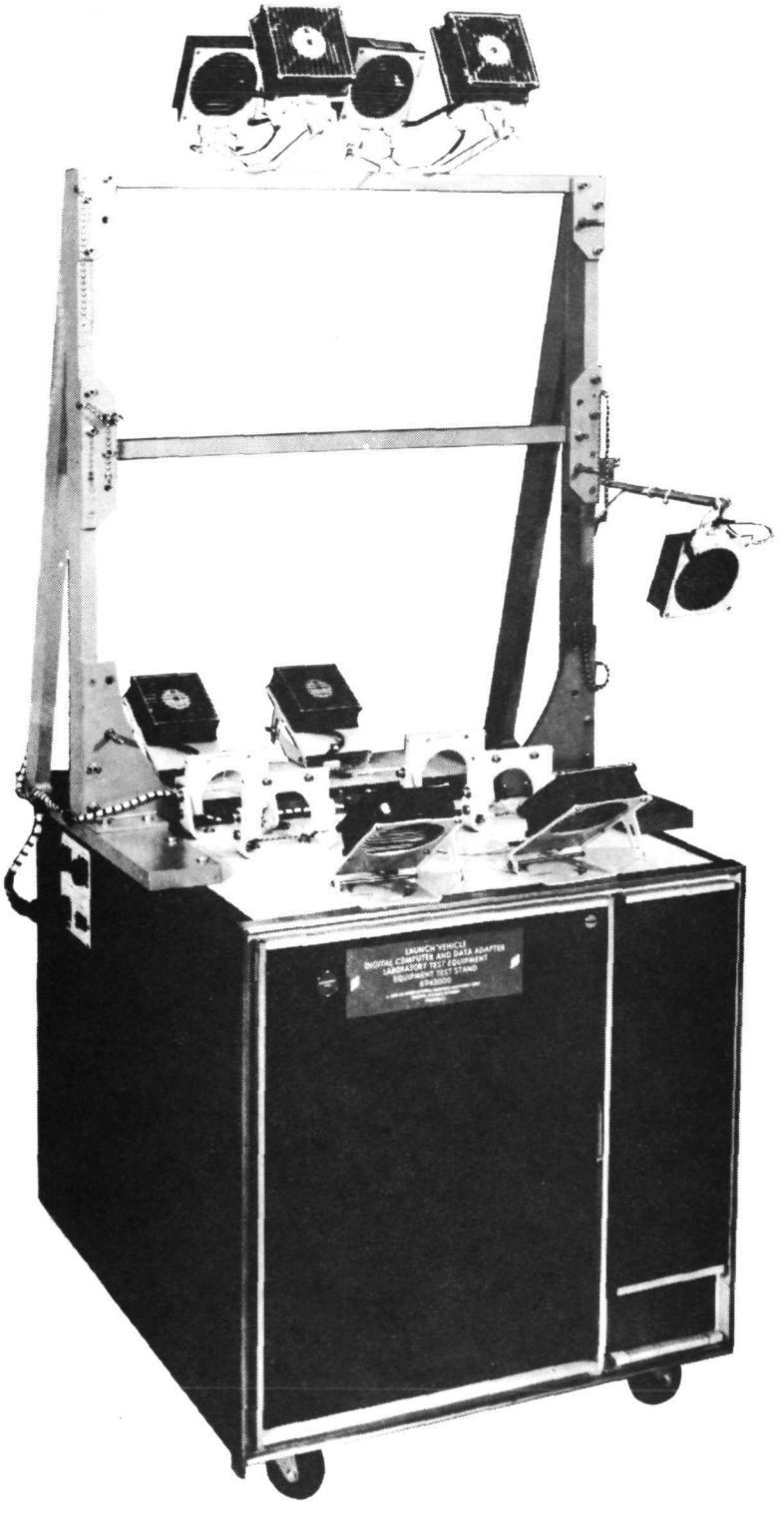


Figure 1-11. Equipment Test Stand (ETS)

Input Power	Phase: 3 phase, 5 wire; wye connected; phase sequence is A B C Frequency: 60 (±5) cycles/second Voltage: 115 (±11.5) VAC (line to neutral) Current: 20 (minimum) to 30 (maximum) amperes/phase
Packaging	Basic Packaging: IBM SMS Module I design. Cabinet: Two frames mechanically and electrically bonded together. Size: Height - 60 inches Width - 58 inches Depth - 31 inches Weight: 1900 pounds (approximately) Logic Chassis Design: Hinged on one edge for easy access to the logic circuits; a fan is mounted on each chassis for circulating cooling air over the circuits. Printed Circuit Cards: The basic logic circuit subassembly is the SMS printed circuit card.
Environment	Ambient Temperature: +60 to +95 degrees Fahrenheit Relative Humidity: 10 to 80 percent Fungus: The LVDAME does not contain any material that is a nutrient to fungus growth in its normal environment.

Figure 1-12. Electrical, Mechanical, and Environmental Characteristics

SECTION II

THEORY OF OPERATION

2-1. SCOPE.

2-2. This section contains the functional descriptions of the LVDAME circuits. The circuits are discussed in three major groups as follows:

1. Basic Circuits.

   a. Circuits not directly concerned with any LVDAME interface.

   b. Circuits concerned with more than one LVDAME interface.

2. Interface Simulation Circuits.

3. Interface Monitoring Circuits.

NOTE

Figures in Section X are referenced in the following paragraphs. Some of the figures in Section X have zone coordinates used to designate areas on the figures. Vertical coordinates A through E (bottom to top) are on the sides of each figure; horizontal numerical coordinates are on the top and bottom of each figure. For example, zone C1 designates the area defined by vertical coordinate C and horizontal coordinate 1.

2-3. BASIC CIRCUITS.

2-4. POWER DISTRIBUTION.

2-5. AC POWER DISTRIBUTION. As shown on figure 10-4, sheet 1, primary power (115 VAC, 3 phase, 60 cycle) is applied to connector 9420 J33 on the 02B8 assembly. Each phase is applied through circuit breaker 02B8CB4 to movable contacts of the main power relay 02B8K2; phase C is also applied through circuit breakers 02B8CB1 and 02B8CB2 to convenience outlets 9420 J44 and 9420 J45.

2-6. When primary power (115 VAC, 3 phase, 60 cycle) is applied to the Equipment Test Stand (ETS, discussed in Volume II of this manual), phase C is applied to a transformer that develops 24 VAC. This 24 VAC is applied to the LVDAME through connector 9420 J32 to terminals 1 and 4 of terminal board 01A10TB2 (figure 10-4, sheet 1, zone C11). This voltage is applied through the normally closed contacts of POWER

OFF switch 02A6S29 and the normally closed contacts of relay 02B8K2 to POWER OFF lamps 02A6DS38. This voltage forces the POWER OFF lamps to light.

2-7. When POWER ON switch 02A6S30 is pressed, 24 VAC is applied through the normally open contact of the switch to POWER ON lamps 02A6DS39, forcing the POWER ON lamps to light; this voltage also energizes relay 02B8K2, causing the following to occur:

1. POWER OFF lamps 02A6DS38 are extinguished.

2. POWER ON lamps 02A6DS39 become lit.

3. Three phase power is routed through the normally open contacts of relay 02B8K2 and distributed as follows:

Phase A - 0A lamp 02A6DS40

Analog/Digital converter 02A2 (through connector 02B8J3)

Multiplexer 02A3 (through connector 02B8J4)

Phase B - 0B lamp 02A6DS40

Elapsed time meter 02B8M1

FAN lamp 02A6DS40 (through circuit breaker 02B8CB3)

All fan motors (through terminal boards 01A10TB4 and 02A9TB1, shown on figure 10-4, sheet 2)

Phase C - 0C lamp 02A6DS40 (shown on figure 10-4, sheet 1)

2-8. When relay 02B8K2 is energized, three phase power is also applied to the movable contacts of relay 02B8K1. When relay 02B8K1 is energized, three phase power is applied through voltage regulators to the LVDAME power supplies.

2-9. Relay 02B8K1 is energized when DC ON switch 02A6S3 is pressed. (See figure 10-4, sheet 5, zones D56, D57, E56, E57.) The conditions existing before DC ON switch 02A6S3 is pressed are described in the following paragraphs.

2-10. When primary power is applied to the ETS, the -26.5 VDC power supply is turned on. This voltage is applied through interface connections to DC OFF switch 02A6S1. The -26.5 VDC is applied through the normally closed contacts of DC OFF switch 02A6S1, contacts 1 and 3 of relay 02B6K22, and contacts 8 and 6 of relay 02B6K14 to DC OFF lamps 02A6DS1, forcing them to light.

2-11. When DC ON switch 02A6S3 is pressed, -26.5 VDC energizes relay 02B6K14; the relay is held by the -26.5 VDC through its contacts 1 and 4. When contacts 8 and 5 of relay 02B6K14 close, -26.5 VDC is removed from DC OFF lamps 02A6DS1 and applied to the SMS PWR CONT line and the TRANSLATE AND DA PWR CONT line (through contacts 8 and 6 of relay 02B6K17).

2-12. When -26.5 VDC is applied to the SMS PWR CONT line, relay 02B8K1 is energized and three phase power is applied to the LVDAME power supplies (figure 10-4, sheet 2) as follows.

Phase A -	-12 VDC power supply 02A8PS2
(through voltage regulator 02B1VR3)	
Phase B -	-12 VDC power supply 02A1PS1
(through voltage regulator 02B1VR2)	-12 VDC power supply 02A8PS1
	-36 VDC power supply 02A7PS2
Phase C -	+12 VDC power supply 02A1PS2
(through voltage regulator 02B1VR1)	- 6 VDC power supply 02A7PS1

2-13. When -26.5 VDC is applied to the TRANSLATE AND DA PWR CONT line, a relay in the ETS is energized, and AC power is applied to the ETS +28 VDC DA, +28 VDC I, +6 VDC, and -3 VDC power supplies.

2-14. DC POWER DISTRIBUTION. When DC ON switch 02A6S3 is pressed, -26.5 VDC is applied through contacts 8 and 6 of relay 02B6K22 and the normally closed contacts of POWER SUPPLY ERROR switch 02A6S2 to the one second time delay relay pair 02B6K11 and 02B6K15 (figure 10-4, sheet 5, zones E53, E54). When this relay pair becomes energized one second later, -26.5 VDC is applied to contact 8 of relay 02B6K23. The -26.5 VDC then passes through the normally closed contacts (8 and 6) of relays 02B6K23, 02B6K19, 02B6K20, and 02B6K21 to relay 02B6K18 and to DC ON lamps 02A6DS3, forcing the lamps to light. The -26.5 VDC energizes relay 02B6K18, which is held energized by the -26.5 VDC through its contacts 1 and 4; this relay places SIG RET ("0") on the -Y RESET line and allows -12 VDC ("1") to enter the +Y RESET line.

2-15. The distribution of the DC power in the LVDAME is shown on figure 10-4, sheets 3 and 4. The copper bus assemblies 01A9W1, 01A9W2, 02A9W1, and 02A9W2 and their cables distribute the DC voltages to the primary terminals of the gate voltage distribution assemblies shown at the top and bottom of each sheet. (Refer to paragraphs 1-38 and 1-39 for the description of the gate voltage distribution assemblies.) The voltage on each line of the power distribution cables is noted on figure 10-4, sheet 3, zones C31 and C32, and sheet 4, zones A47 and A48.

2-16. LVDAME POWER SUPPLY ERROR DETECTION. If the output voltage of an LVDAME power supply (except the -36 VDC power supply 02A7PS2) exceeds its tolerance, one of the error detection circuits shown on figure 10-4, sheet 5, zones B56-B60 and C56-C60, will turn off all DC power in the LVDAME and the ETS (except the -26.5 VDC power supply in the ETS). The error detection circuit for each power supply includes a differential relay operated in the null condition, so that if the power supply output deviates (either positively or negatively) beyond the established tolerance, the relay is energized, and -26.5 VDC is applied to relay 02B6K22.

2-17. The -26.5 VDC energizes relay 02B6K22, thus opening contacts 1 and 3 and removing the -26.5 VDC from the holding circuit of relay 02B6K14 (contacts 1 and 4 of relay 02B6K14). This action de-energizes relay 02B6K14, thus removing the -26.5 VDC from the SMS PWR CONT and TRANSLATE AND DA PWR CONT lines and de-energizing the relays that transfer AC power to the power supplies in the LVDAME and ETS. The DC OFF lamps 02A6DS1 become lit when the one second time delay relay pair 02B6K10 and 02B6K13 becomes de-energized, allowing -26.5 VDC to be applied to the lamps through contacts 8 and 6 of relay 02B6K14. The DC ON lamps 02A6DS3 are extinguished when the one second time delay relay pair 02B6K11 and 02B6K15 becomes de-energized (since contacts 8 and 6 of relay 02B6K22 are now open).

2-18. DC power can be restarted in the LVDAME by pressing DC ON switch 02A6S3.

2-19. ETS POWER SUPPLY ERROR DETECTION. If the output voltage of the +6 VDC, -3 VDC, +28 VDC DA or +28 VDC I power supply in the ETS exceeds its tolerance, one of the error detection circuits shown on figure 10-4, sheet 5, zones B51-B56, C51-C56, D51-D54, E51-E54, will turn of the DC power supplies in the ETS (except the -26.5 VDC power supply). The error detection circuit for each power supply includes a differential relay operated in the null condition, so that if the power supply output deviates (either positively or negatively) beyond the established tolerance, the relay is energized, and -26.5 VDC is applied to a slave relay.

2-20. When a slave relay (02B6K19, 02B6K20, 02B6K21, or 02B6K22) is energized, contacts 3 and 4 send a pair of signals (a "1" and a "0") to the logic circuits shown on figure 10-50, sheet 12, zones B9, B10, C8-C10, D8-D10, E8. The four error indication latches (in zones B10, C10, and D10) control the four POWER SUPPLY ERROR lamps 02A6DS2; these latches are interconnected so that only the first power supply error will be indicated by the lamps.

NOTE

The DC ON lamps 02A6DS3 (figure 10-4, sheet 5, zone E56) remain lit because -26.5 VDC is applied to them through the normally open contacts of the one second time delay relay pair 02B6K11 and 02B6K15 and contacts 1 and 4 of relay 02B6K18.

2-21. When a slave relay is energized, -26.5 VDC is applied through contacts 8 and 5 of the slave relay to energize the one second time delay relay pair 02B6K12 and 02B6K17. After one second this relay pair removes the -26.5 VDC from the TRANSLATE AND DA PWR CONT line, thus de-energizing the relay that transfers AC power to the ETS power supplies.

2-22. When a slave relay is energized, -26.5 VDC is also applied to relay 02B6K18; this voltage energizes relay 02B6K18. Relay 02B6K18 is then held energized by the -26.5 VDC that is applied to the coils of the one second time delay relay pair 02B6K11 and 02B6K15.

2-23. The error indication latches can be reset and AC power reapplied to the ETS power supplies by pressing and releasing POWER SUPPLY ERROR switch 02A6S2. When this switch is pressed, the -26.5 VDC is removed from the coils of the one second time delay relay pair 02B6K11 and 02B6K15. When this relay pair is de-energized, relay 02B6K18 is de-energized, thus removing -26.5 VDC from DC ON lamps 02A6DS3 and applying SIG RET to the +Y RESET line, which resets the error indication latches; the one second time delay relay pair 02B6K12 and 02B6K17 is de-energized, thus reapplying -26.5 VDC to the TRANSLATE AND DA PWR CONT line; relay 02B6K18 is also de-energized.

2-24. When the POWER SUPPLY ERROR switch is released, -26.5 VDC is again applied to the one second time delay relay pair 02B6K11 and 02B6K15, and after one second the error detection circuits are again ready. The -26.5 VDC is applied through contacts 8 and 6 of each slave relay to DC ON lamps 02A6DS3 and to relay 02B6K18, which applies SIG RET to the -Y RESET line and allows -12 VDC to enter the +Y RESET line.

2-25. POWER TURN-OFF. The DC power in the LVDAME and ETS is normally turned off by pressing DC OFF switch 02A6S1. This action removes the -26.5 VDC from the SMS PWR CONT and TRANSLATE AND DA PWR CONT lines, thus deenergizing the relays that apply AC power to the power supplies in the LVDAME and ETS.

2-26. The AC power in the LVDAME is normally turned off by pressing PWR OFF switch 02A6S29. This action removes the 24 VAC from relay 02B8K2 (figure 10-4, sheet 1, zone D18), thus removing the three phase power from the LVDAME.

2-27. Emergency Power Turn-Off. In an emergency all power can be turned off in the LVDAME, the ETS, and any other interconnected equipment by pulling EMERGENCY PULL switch 02A6S35 on the LVDAME or a similar switch on other test equipment. When one of these switches is pulled, the 24 VAC line from the transformer in the test stand is opened; this action de-energizes the main power relay in each test equipment (relay 02B8K2 in the LVDAME), thus removing all input AC power from the test equipment.

2-28. TIMING.

2-29. The basic timing in the LVDAME is identical to that used in the computer and data adapter. Each operation cycle consists of three phases - A, B, and C; each phase consists of 14 bit gates - BG1 through BG14; each bit gate consists of four clock-times - W, X, Y, and Z. (See figure 2-1.)

NOTE

In this section, timing intervals are usually referenced by a three-part notation that designates the phase, bit gate, and clock-time of the interval. For example, B-1-X denotes phase B, bit gate 1, clock-time X. If the clock-time is not specified, a two-part notation is used; for example, C-12 denotes phase C, bit gate 12.

2-30. The LVDAME timing generator is composed of the master timing generator and the slaved timing generator. The outputs of the master timing generator are used by the data adapter under test without a computer. The outputs of the slaved timing generator are used by the logic circuits in the LVDAME; the slaved timing generator is controlled by the outputs of the timing circuits in the data adapter. Each generator consists of a clock generator, a bit gate generator, and a phase generator.

2-31. MASTER CLOCK GENERATOR. As shown on figure 10-50, sheet 4, zones BS-B10, C5-C10, D5, D6, this generator consists basically of a 2.048 MC oscillator, three interconnected triggers, four delays, and four angle shots. The output waveforms of these circuits are shown on figure 2-2.

2-32. As indicated on figure 2-2, the triggers divide the frequency of the oscillator output. The state of trigger T_A is complemented by the positive transition of the inverter output signal. The state of trigger T_B is complemented by the positive transition of the set output of trigger T_A; the state of trigger T_C is complemented by the positive transition of the reset output of trigger T_A.

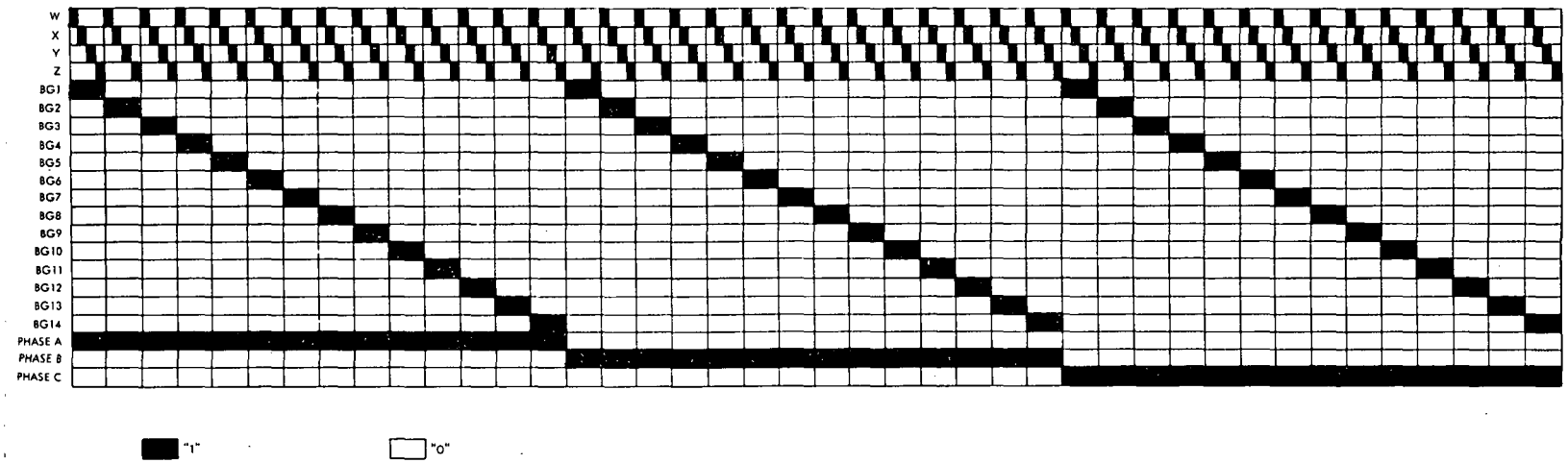
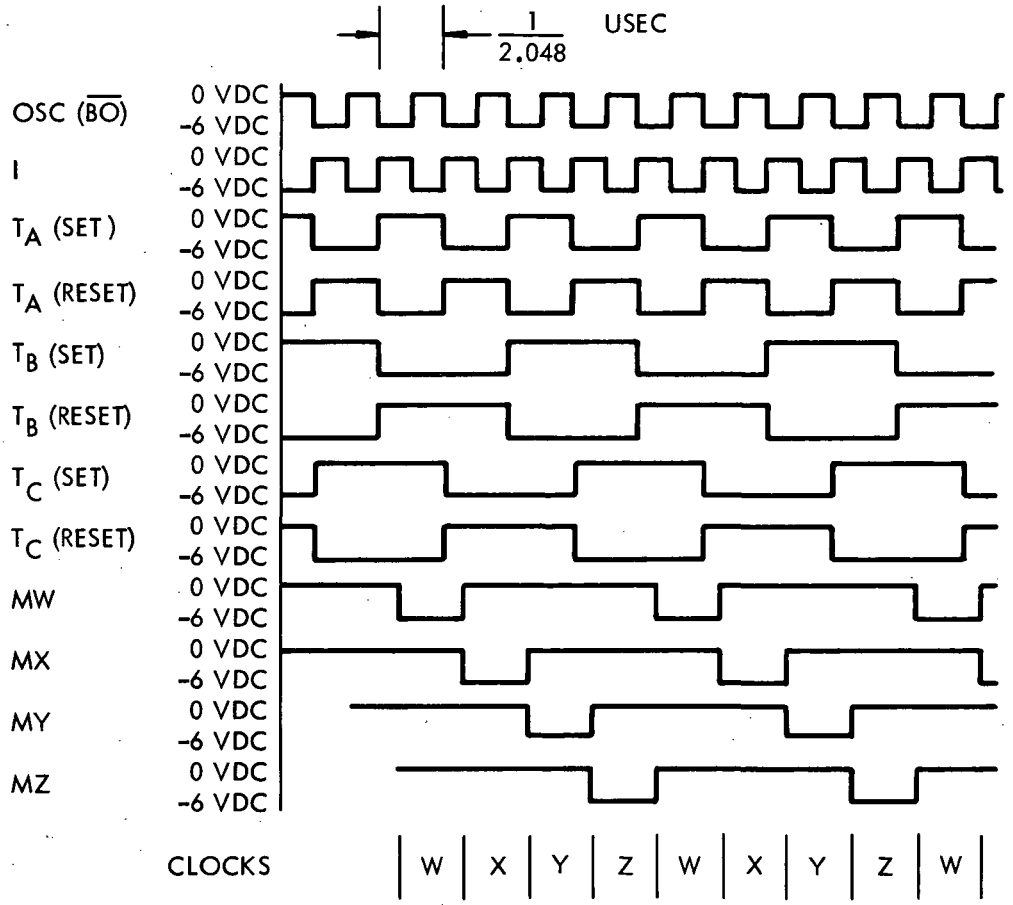


Figure 2-1. Basic LVDAME Timing



NOTE: THE T_A WAVEFORMS ARE THE OUTPUTS OF THE LEFTMOST TRIGGERS ON FIGURE 10-4, SHEET 4. THE T_B AND T_C WAVEFORMS ARE THE OUTPUTS OF THE UPPER AND LOWER TRIGGERS, RESPECTIVELY, IN THAT FIGURE.

Figure 2-2. Master Clock Generator Waveforms

2-33. Each DLY circuit delays its input for approximately 170 NSEC, so that the clocks generated by the single shots occur approximately 170 NSEC after the negative transistor of the controlling trigger output.

2-34. The outputs of the master clock generator are applied in TMR form to the data adapter by the triplicator circuits shown on figure 10-50, sheet 4, zones B2-B4, B8-B10, C2-C4, D2-D4, E2-E4.

2-35. MASTER BIT GATE GENERATOR. The master bit gate generator consists of a seven-bit shift register and a shift register control circuit. These circuits are shown on figure 10-50, sheet 4, zones A8-A10, B8-B10, C8-C10, D6-D10, E6-E9.

2-36. The shift register control circuit prevents the contents of the register from rippling through when the register is stepped. This control circuit is composed of two latches that form a binary counter; the outputs of the control circuit are shown with the outputs of the shift register on figure 2-3.

2-37. The only master bit generator output used by the data adapter is the MG5 NOT signal; this signal is applied in TMR form to the data adapter by the triplicator shown on figure 10-50, sheet 5, zones B6, B7, C6, C7.

2-38. MASTER PHASE GENERATOR. The master phase generator is a three step ring counter composed of three latches, MPA, MPB, and MPC (figure 10-50, sheet 5, zones D1-D5, E1-E5). The ring counter is stable when one latch is set and the other two are reset; the set condition is then stepped around the ring counter in alphabetical sequence at bit 1 time. At W clock-time of each bit 1 time, the next latch in the sequence is set; at the following Y clock-time the preceding latch is reset. During a W clock when a latch is being set, the reset output of the latch for the previous phase time prevents the set condition from "rippling" into the third latch of the ring.

2-39. The "anti-ripple" signals also help the ring counter to reach its normal configuration. If two latches in the ring counter are set at the same time, the "anti-ripple" signals prevent the third latch from being set at the W clock-time of the next bit 1 time. One latch is then reset at Y clock-time of each bit 1 time until the normal configuration is reached.

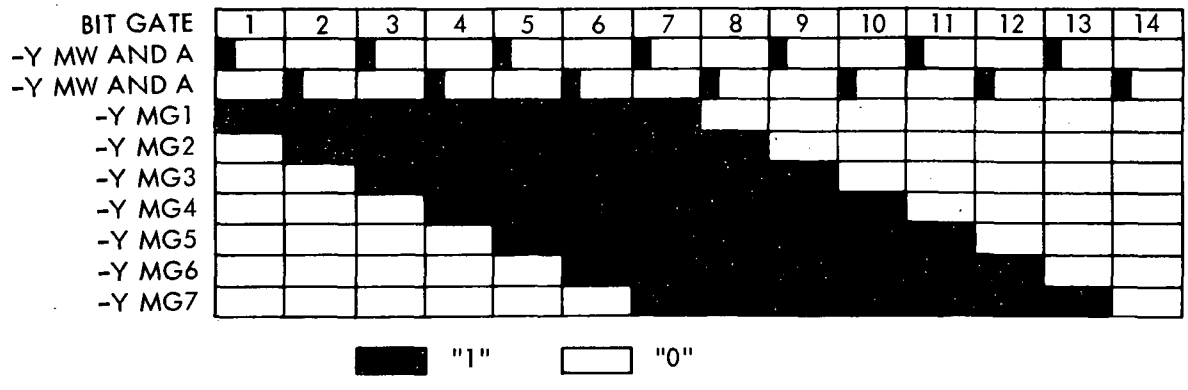


Figure 2-3. Master Bit Gate Shift Register and Shift Register Control Circuit Outputs

2-40. The only master phase generator output used by the data adapter is the MPB NOT signal; this signal is applied in TMR form to the data adapter by the triplicator shown on zones B3-B5, C3-C5.

2-41. SLAVED CLOCK GENERATOR. The slaved clock generator is shown on figure 10-50, sheet 6; a simplified form of the generator is shown on figure 2-4. The generator uses the TMR W clock outputs of the data adapter under test as its driving source. The voter output is delayed two clock-times by DLY 1; this delayed W clock then triggers SS1, which produces the slaved Y clock (-Y AD EY).

2-42. The DLY 2 circuit delays the delayed W clock for another clock-time. (The total delay of DLY 1 and DLY 2 is three clock-times.) The output of DLY 2 triggers SS2, which forms the slaved Z clock (-Y AD EZ).

2-43. The DLY 3 circuit delays the delayed W clock for two clock-times. (The total delay of DLY 1 and DLY 3 is four clock-times.) The output of DLY 3 triggers SS3, which produces the slaved W clock (-Y AD EW).

2-44. The DLY 4 and DLY 5 circuits delay the delayed W clock three clock-times. (The total delay of DLY 1, DLY 4, and DLY 5 is five clock-times.) The output of DLY 5 triggers SS4, which produces the slaved X clock (-Y AD EX).

2-45. SLAVED BIT GATE GENERATOR. This generator consists of a seven-bit shift register, a shift register control circuit and a bit gate decoder. These circuits are shown on figure 10-50, sheet 7.

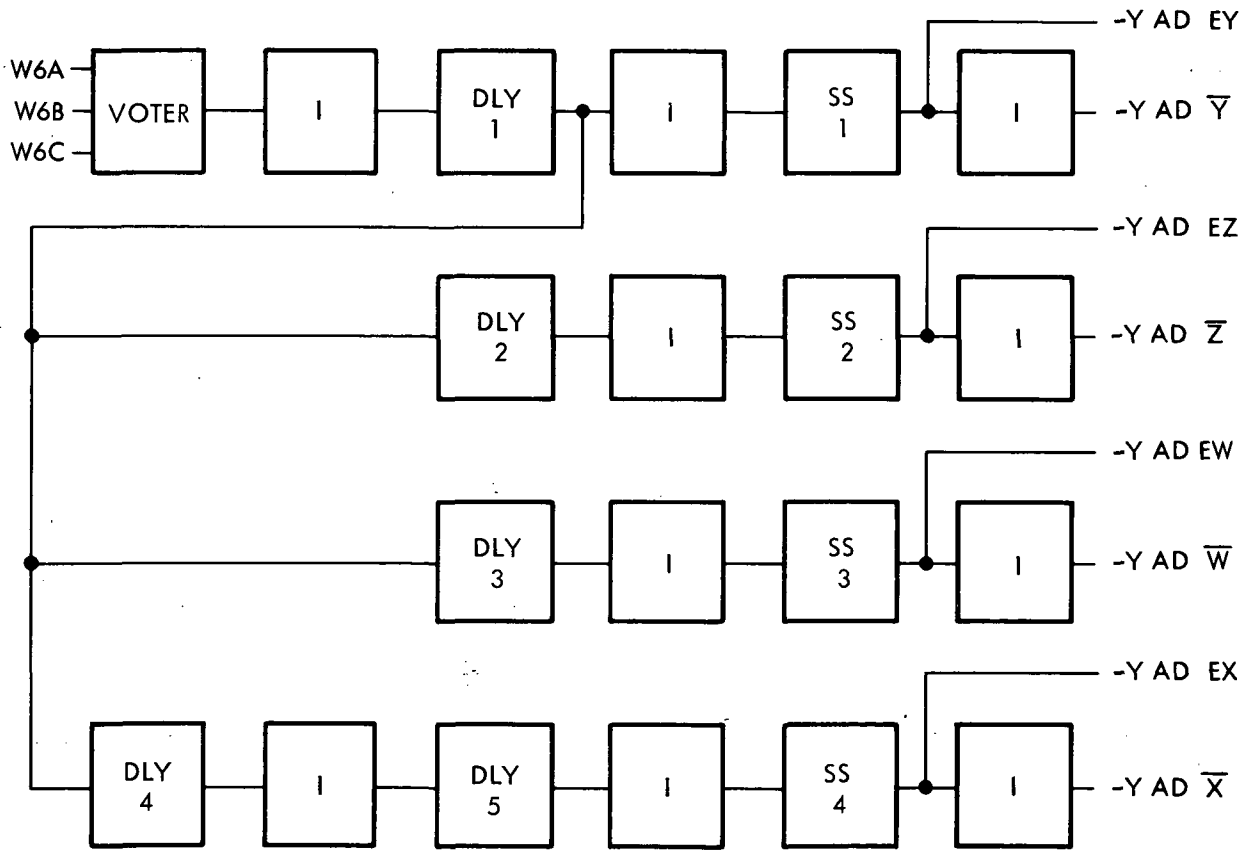


Figure 2-4. Simplified Slaved Clock Generator

2-46. The seven-bit shift register and its control circuit function in the same manner as the master bit gate shift register and its control circuit; the outputs of these circuits are identical to those shown on figure 2-3 for the master circuits.

2-47. However, these slaved circuits are controlled by the -Y TIME SYNC signal which insures that the master and slave circuits are properly synchronized. As shown on figure 10-50, sheet 9, zones D8-D10, the signal is generated by passing the translated Phase B NOT signal from the data adapter through an inverter, a single shot, a second inverter, and a second single shot. These circuits delay the input signal so that -Y TIME SYNC becomes a "1" at B-2-W time.

2-48. The bit gate decoder generates the slaved bit gate signals (-Y AD BG1 through -Y AD BG14) by essentially ANDing the reset output of each shift register latch with the set output of the previous shift register latch. For example, -Y AD BG1 is a "1" while -Y AD G1 and -Y AD G2 NOT are "1's"; -Y AD BG2 is a "1" while -Y AD G2 and -Y AD G3 NOT are "1's".

2-49. SLAVED PHASE GENERATOR. As shown on figure 10-50, sheet 9, the slaved phase generator consists basically of two interconnected tratches whose outputs are synchronized with the phase signals in the data adapter under test by the -Y TIME SYNC signal. The tratch at the left is normally controlled by the outputs of the slaved clock generator and the slaved bit gate generator; the state of this tratch is normally changed at Y clock-time of every BG14. The state of the other tratch is then changed at the following W clock-time (1-W time of the next phase). If the slaved phase generator gets "out-of-sync" with the phase signals in the data adapter under test, the -Y TIME SYNC signal forces both tratches to their proper states at B-2-W time.

2-50. DATA BIT GENERATOR.

2-51. The data bit generator provides 26 signals (data bits) that are used for loading the output registers. The data bits come from the PTC accumulator when the LVDAME is operated in the ADAPT, ASTEC or SELF TEST modes, or from the OUTPUT REGISTERS-COMD switches when the LVDAME is operated in the manual test mode.

2-52. Figure 2-5 is the circuit for the portion of the data bit generator that generates -Y DATA BIT S. The other data bits (-Y DATA BIT 01 through 25) are generated in a similar manner.

2-53. When the LVDAME is in the manual test mode, +Y MAN SW is a "0" and the output of the DT is a "1". When OUTPUT REGISTERS-COMD switch S is pressed, -Y MAN BIT S SW becomes a "1". Five usec after the OUTPUT REGISTERS-INSERT switch is pressed, -Y MANUAL LOAD GATE also becomes a "1" and -Y DATA BIT S is generated for a period of five USEC.

2-54. When the LVDAME is in a mode other than manual test, +Y MAN SW is a "1", and the PTC accumulator sign bit (-C ACC S) appears on the -Y DATA BIT S line.

2-55. CONTROL BIT GENERATOR.

2-56. The control bit generator provides 26 signals (control bits) that are used throughout the LVDAME for control purposes. The control bits come from the PTC accumulator when the LVDAME is operated in the ADAPT, ASTEC or SELF TEST modes, or from the OUTPUT REGISTERS-COMD switches when the LVDAME is operated in the manual test mode.

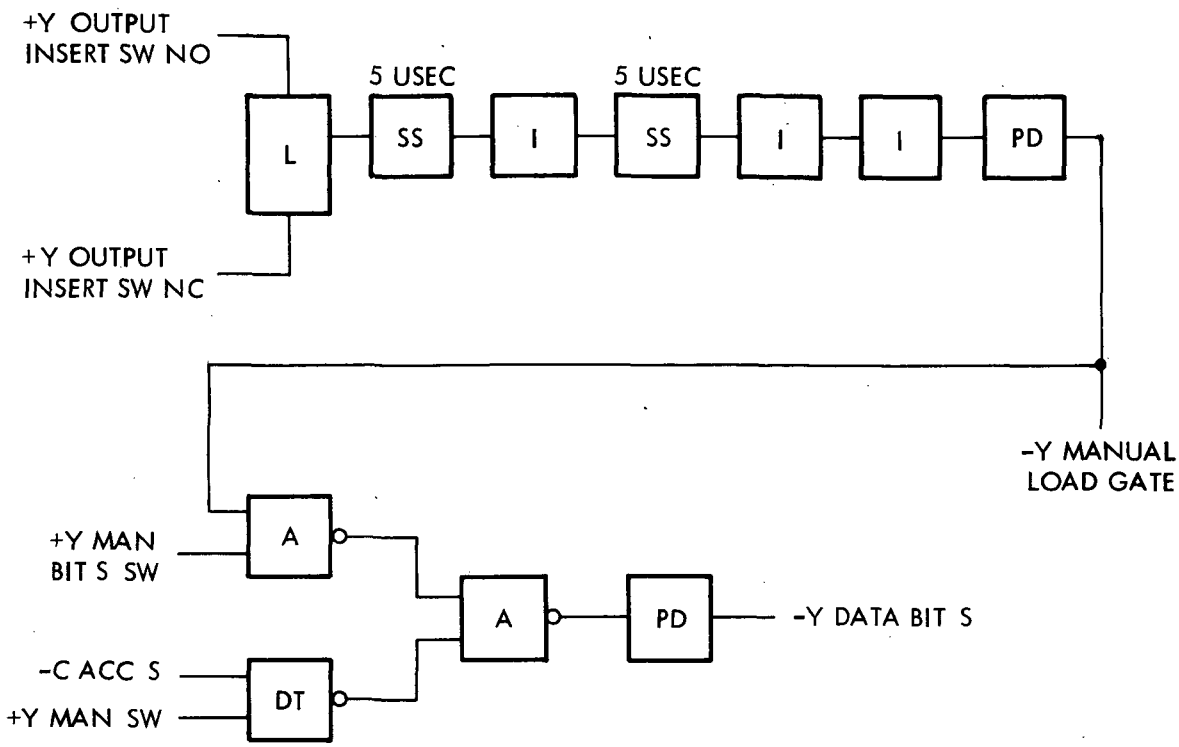


Figure 2-5. Sign Data Bit Generator

2-57. Figure 2-6 is the circuit for the portion of the control bit generator that generates -Y CONTROL BIT S. The other control bits (-Y CONTROL BIT 1 through 25) are generated in a similar manner.

2-58. When the LVDAME is in the manual test mode, +Y MAN SW is a "0", and the output of the DT is a "1". Every bit gate 2 during phase A time, if a CIO cycle is initiated, the content of the DIN register sign position will appear at -Y CONTROL BIT S.

2-59. When the LVDAME is in a mode other than manual test, +Y MAN SW is a "1", and the PTC accumulator sign bit (-C ACC S) appears on the -Y CONTROL BIT S line.

2-60. DISAGREEMENT DETECTORS.

2-61. Each data adapter signal that appears at the LVDAME in TMR form is applied to a disagreement detector. The disagreement detector monitors the three signals in the TMR trio, and lights an error lamp whenever a disagreement occurs among the three signals. The lighted lamp indicates which type of data and which channel is at fault.

2-62. Figure 2-7 shows a typical disagreement detector in which TMR signals A1X, A2X and A3X are compared. The disagreement detector works on the principle that if one signal in a TMR trio disagrees with the other two, it must match the inverses of the other two.

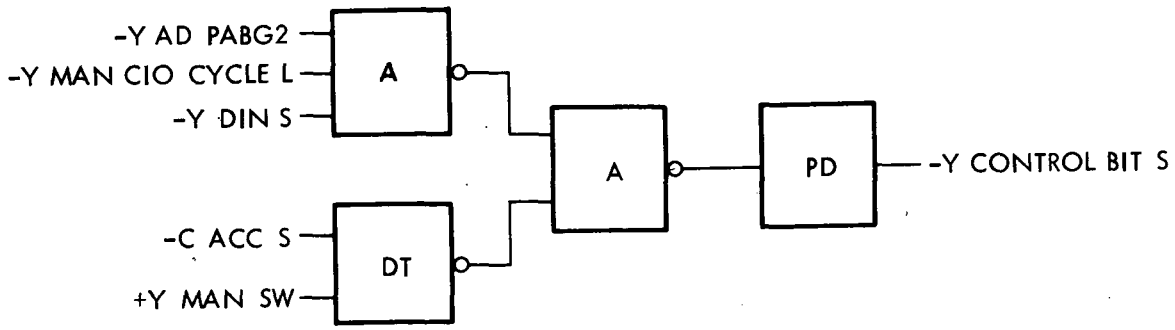


Figure 2-6. Sign Control Bit Generator

2-63. If A1X does not match A2X and A3X, AO-1 or AO-2 will have two "1" inputs, and L-1 will set. Since A2X matches A3X, AO-3 and AO-4 will each have at least one "0" input, L-2 will not set. IO-1 and IO-2 will each have a "0" input, and their "1" output will light the X channel-1 indicator.

2-64. If A2X does not match A1X and A3X, one AO for each latch will have two "1" inputs, and both latches will set. IO-3 and IO-4 will each have "0" inputs, and their "1" output will light the X channel 2 indicator. IO-2 and IO-5 will each have a "1" input, and the "0" at the output of these inverters keep the X channel-1 and X channel-3 indicators from lighting.

2-65. If A3X does not match A1X and A2X, AO-3 and AO-4 will both have two "1" inputs, and L-2 will set. Since A1X matches A2X, AO-1 and AO-2 will each have at least one "0" input, L-1 will not set. IO-5 and IO-6 will each have a "0" input, and their "1" output will light the X channel-3 indicator.

2-66. Disagreement detectors are provided for the following types of LVDA signals:

DATAV	INFOV
LDATAV	PCINFV
AI3V	INTCV
TRSV	LINTCV
HALTV	PBAVN
ADV	G5DVN
PIODV	A1V through A9V

2-67. INTERFACE VOTERS.

2-68. All data adapter signals that appear at the LVDAME in TMR form are processed to form simplex signals for use within the LVDAME. Processing is performed by the interface voters which provide simplex signals that correspond to the majority of the signals in the TMR trio.

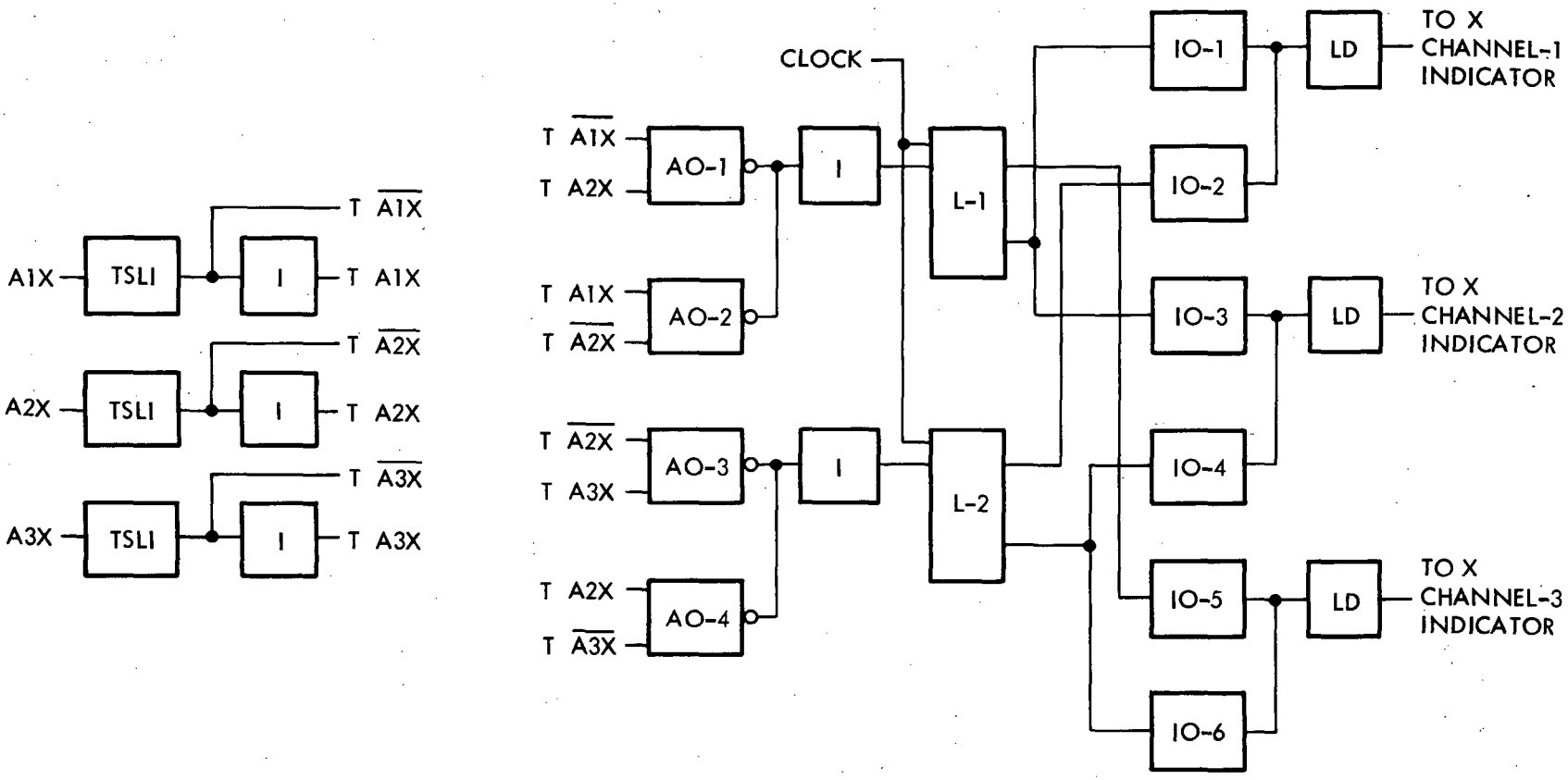


Figure 2-7. Typical Disagreement Detector

2-69. Figure 2-8 shows a typical interface voter which produces -Y X from TMR signals A1X, A2X and A3X. If two (or more) inputs to the voter are "1's", each AND-inverter will have at least one "0" input. The voter output (-Y X) will therefore be a "1". If two (or more) inputs to the voter are "0's", at least one AND-inverter will have two "1" inputs, and the voter output will be a "0".

2-70. Interface voters are provided for the following types of data adapter signals:

DATAV	PIODV
LDATAV	INTCV
AI3V	LINTCV
TRSV	PBAVN
HALTV	G5DVN
ADV	A1V through A9V

2-71. TRIPLICATORS AND I/O CHANNEL CONTROL.

2-72. All simulated TMR computer signals are provided to the data adapter by the LVDAME. These signals, which originate in simplex form within the LVDAME, must be changed to TMR form before being applied to the data adapter. This function is performed by triplicators. Figure 2-9 shows a typical triplicator in which simplex signal XX is changed into TMR signal A1XX-A2XX-A3XX. If CSA0 NOT, CSB0 NOT or CSC0 NOT is a "0" the corresponding output signal will be held to a "0"; if CSA1 NOT, CSB1 NOT or CSC1 NOT is a "0" the corresponding output signal will be held to a "1".

2-73. The I/O channel control circuit simultaneously disables one channel of all simulated computer TMR signals by controlling the six channel control signals. These signals are generated manually by the COMPUTER CHANNEL switches or automatically by CIO 603 and certain control bits as shown in figure 2-10.

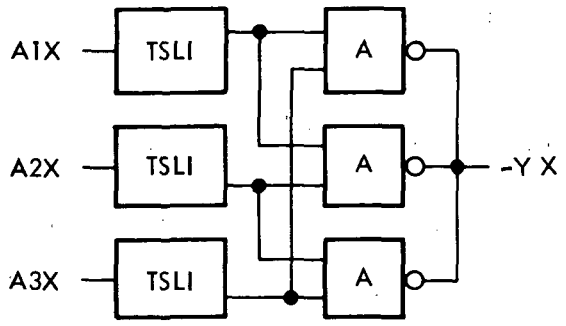


Figure 2-8. Typical Voter

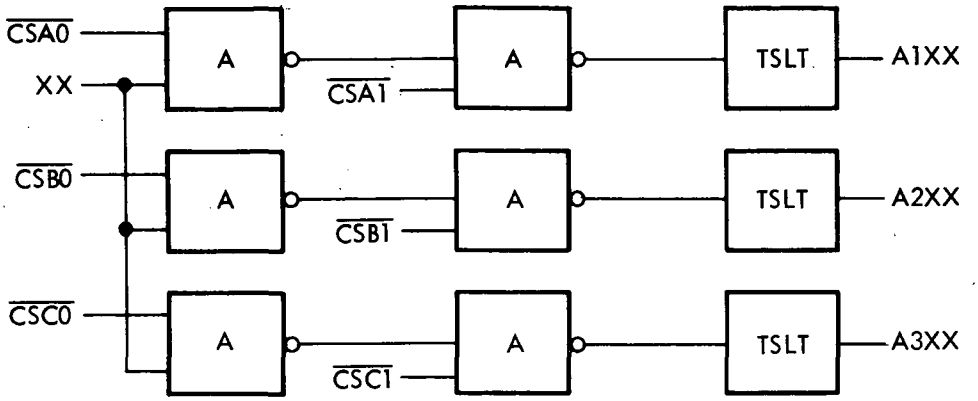


Figure 2-9. Typical Triplicator

2-74. Referring to figures 2-9 and 2-10, if ACTIVE-123 were pressed and INACTIVE-0 were pressed, CSB0 NOT and CSC0 NOT would be "1's" and CSA0 NOT would be a "0". The simplex signal XX would therefore appear at A2XX and A3XX, and A1XX would be a "0". Similarly it can be seen that whenever an ACTIVE pushbutton is pressed, one channel will be disabled. The disabled channel will be set to "1" or "0" depending on which INACTIVE pushbutton is pressed.

2-75. Triplicators and associated channel control are provided for the following LVDAME signals:

1. Clocks from the master clock generator.
2. BON from the master clock generator.
3. G5DVN from the master bit gate generator.
4. PBAVN from the master phase generator.
5. PIOV from PIO manual controls.
6. Address bits from PIO simulation.
7. AI3V from input multiplexer serializer.
8. TRSV from input multiplexer serializer.

2-76. DATA ADAPTER CHANNEL SWITCHING.

2-77. The LVDAME controls LVDA channel selection with channel switching pulses GCOE, GCOF, GCOG and GCOR. The circuits that produce these pulses are shown on figure 10-50, sheets 15 and 16. Channel switching may be controlled manually by the CHANNEL SELECT pushbuttons or automatically under CIO and control bit control.

CIO 603 and Control Bits	Computer Channel		Channel Control Signals Forced to "1"
	Active	Inactive	
22, 24, 21	$\bar{1}23$	0	$\overline{CSB0}$ and $\overline{CSC0}$
22, 24, 20	$\bar{1}23$	1	$\overline{CSA1}$, $\overline{CSB0}$ and $\overline{CSC0}$
22, 25, 21	$1\bar{2}3$	0	$\overline{CSA0}$ and $\overline{CSC0}$
22, 25, 20	$1\bar{2}3$	1	$\overline{CSB1}$, $\overline{CSA0}$ and $\overline{CSC0}$
23, 24, 21	$12\bar{3}$	0	$\overline{CSA0}$ and $\overline{CSC0}$
23, 24, 20	$12\bar{3}$	1	$\overline{CSC1}$, $\overline{CSA0}$ and $\overline{CSB0}$

Figure 2-10. Channel Control Signals

2-78. The channel switching circuit is comprised mainly of four latches and a pulse generator. The four latches are interconnected so that only one may be set at a time. The pulse generator produces pulses GCOR and -Y TEST SET whenever a CHANNEL SELECT pushbutton is pressed or a channel switching CIO is issued. Output -Y TEST SET from the pulse generator, gated by the output from one of the channel select latches, appears at the interface as GCOE, GCOF or GCOG. Output GCOR (which occurs 10 MS before -Y TEST SET) resets LVDA channel operation to TMR before a new channel is selected. The pulses that are generated whenever channel switching is commanded by the LVDAME are as follows:

Channel	Pulses Generated
1	GCOR, GCOE and GCOF
2	GCOR, GCOE and GCOG
3	GCOR, GCOF and GCOG
TMR	GCOR

2-79. Two lamps are provided to indicate each of the channel switching conditions except TMR. A single lamp is provided for TMR. The CHANNEL SELECT-COMD lamps indicate that the corresponding channel latch is set. The TMR lamp indicates that the TMR latch is set. The channel switching pulse lines are fed back from the interface and applied to a circuit that decodes the pulses as follows:

GCOE and GCOF - Channel 1

GCOE and GCOG - Channel 2

GCOF and GCOG - Channel 3

The outputs from the decoding circuit are applied to latches which light one CHANNEL of the CHANNEL SELECT-CTRL lamps.

2-80. Channels may be selected by pressing CHANNEL SELECT-COMD switches or using CIO 613 and control bits as follows:

Channel	Channel Select Switch	Control Bit
1	COMD 1	17
2	COMD 2	16
3	COMD 3	15
TMR	TMR	14

2-81. POWER TESTS.

2-82. The LVDAME controls data adapter power tests with power test levels GCOA, GCOB, GCOC, GCOD and GCOR. The circuits that produce these levels are shown on figure 10-50, sheets 15 and 16. Power tests may be accomplished manually with the POWER SUPPLY AND DISCRETE OUTPUT pushbuttons or automatically under CIO and control-bit control. Power tests may be selected by pressing POWER SUPPLY AND DISCRETE OUTPUT pushbuttons or by using CIO 613 and control-bits as follows:

Power Test	POWER SUPPLY AND DISCRETE OUTPUT Switch	CIO 613 and Control Bit
1	COMD 1	21
2	COMD 2	20
3	COMD 3	19
4	COMD 4	18

2-83. The power test circuit is comprised mainly of eight latches and a pulse generator. Latches PT1 through PT4 are interconnected so that only one may be set at a time. The latches store the commanded power test. The pulse generator generates GCOR and -Y TEST SET whenever a POWER SUPPLY AND DISCRETE OUTPUT pushbutton is pressed or a power tests CIO is issued. The -Y TEST SET output from the pulse generator (gated by the output of PT1, PT2, PT3 or PT4) sets two of the following latches: GCOA, GCOB, GCOC and GCOD. The latches that set as a result of setting the PT latches are as follows:

PT Latch	GC Latch Set
PT1	GCOA and GCOB
PT2	GCOA and GCOC
PT3	GCOB and GCOD
PT4	GCOC and GCOD

2-84. Two lamps are provided for each power test condition. The POWER SUPPLY AND DISCRETE OUTPUT-COMD lamps are connected to the corresponding PT latch and indicate (when lit) that the corresponding PT latch is set. The POWER SUPPLY AND DISCRETE OUTPUT-CTRL lamps are connected to a circuit that decodes power test conditions from the interface power test levels as follows:

GCOA and GCOB -- PT1

GCOA and BCOC -- PT2

GCOB and GCOD -- PT3

GCOC and GCOD -- PT4

2-85. SIMPLEX OUTPUT REGISTERS.

2-86. The LVDAME contains 10 simplex output registers that provide digital data to the data adapter. Each register consists of latches that set when the correct CIO code and data bit is present. The CIO codes that control the output registers are simulated in the manual mode by the OUTPUT REGISTERS selector switch; in other modes the CIO codes originate in the PTC. Figure 2-11 lists the simplex output registers and the CIO codes that control their loading.

2-87. One set of outputs from the output register are applied to a display multiplexer which selects one of the output registers for display in the OUTPUT REGISTERS-REG lamps. The output register to be displayed in selected by the OUTPUT REGISTERS selector switch. The outputs from the output registers are also applied (as possible inputs) to the input multiplexer.

2-88. Pertinent data concerning each of the output registers is listed in figure 2-11. Additional data concerning the CR/GC, optisyn, EM and COD registers is given in subsequent paragraphs.

2-89. CR/GC REGISTER. The CR/GC register is a dual register that simulates CR1 through CR14 from the Command Receiver or GC1 through GC14 from the RCA 110. The CR and GC data is taken from opposite sides of the latches and therefore are always complements of each other.

2-90. OPTISYN REGISTER. The optisyn register may also be loaded with data from the accelerometer simulator. The outputs from the optisyn register simulate the accelerometer outputs from the platform.

2-91. EM REGISTER. The EM register may also be loaded with serial data from the LDATAV interface voter. (See figure 2-12.) LDTAV is first delayed 1/2 bit time and the delayed serial data (LDATAVD) is inserted into bit positions 5 through 16 of the EM register. Timing gates sequentially load successive EM register latches with the data on the LDATAVD line.

2-92. The outputs from the EM register are not applied directly to the data adapter, but are used to generate simulated error pulses that are sent to the data adapter. Error pulse simulation is described in paragraph 2-107.

Output Register	Data Bits																								
	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
SSFB								08	07	06	05	04	03	02	01											
CR/GC	14	13	12	11	10	09	08	07	06	05	04	03	02	01												
DDAS	10	09	08	07	06	05	04	03	02	01																
NA DIS																			08	07	06	05	04	03	02	01
INT			10	09	08	07	06	05	04	03	02	01														
EM	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01										
DIN	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	2A	01	2B	25
DIS	08	07	06	05	04	03	02	01																		
OPTISYN															X1Q	X1R	X2Q	X2R	Y1Q	Y1R	Y2Q	Y2R	Z1Q	Z1R	Z2Q	Z2R
COD																11	10	09	08	07	06	05	04	03	02	01

Figure 2-11. Output Register Bits

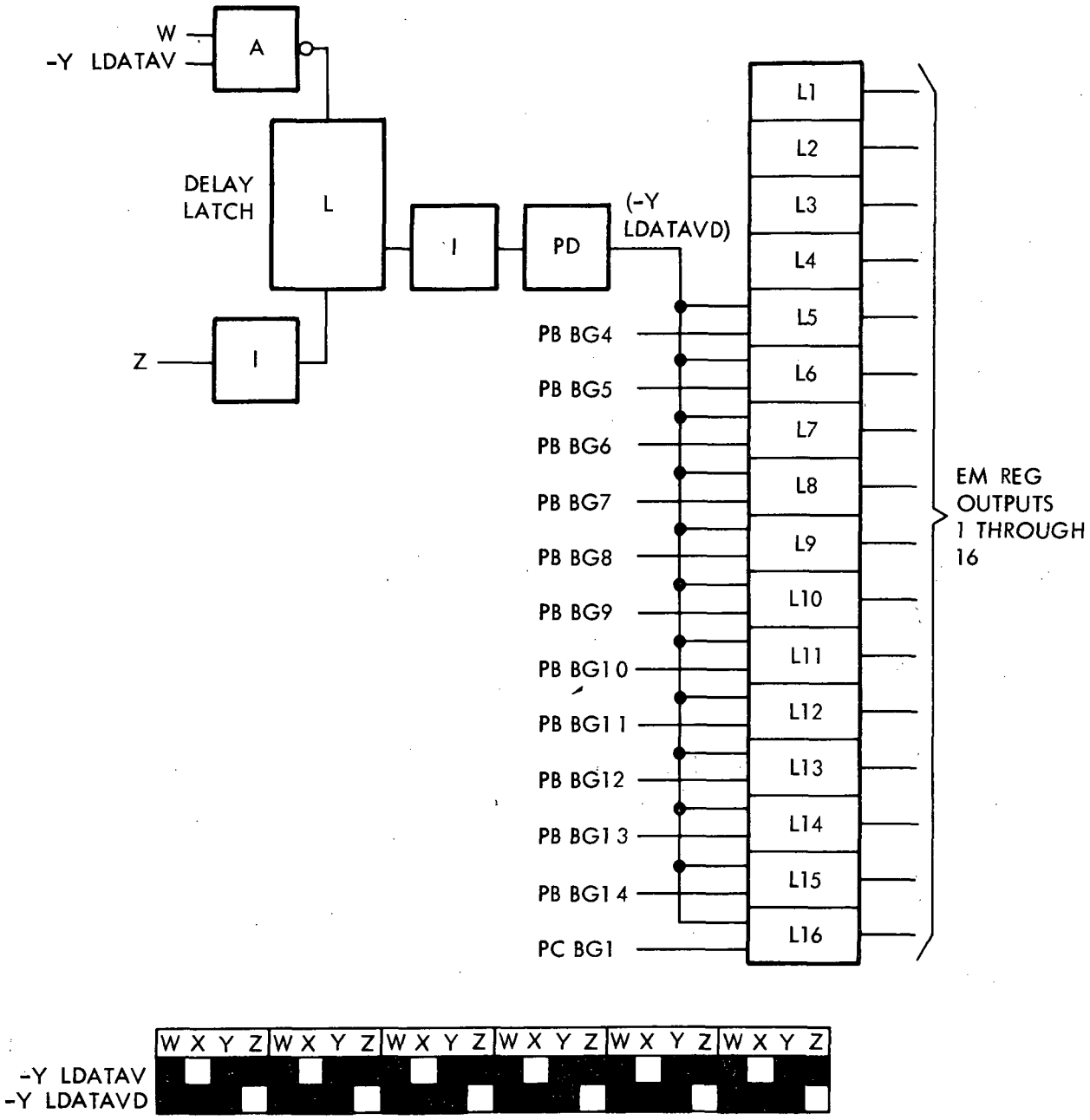


Figure 2-12. EM Register

2-93. COD REGISTER AND COD SERIALIZER. The COD register outputs are not applied directly to the data adapter. As shown on figure 10-50, sheet 54, zones A4, A5, B1-B5, C1-C5, these outputs are first passed through the COD serializer where they are serialized as follows:

COD Bit	Bit Gate	COD Bit	Bit Gate
01	2	07	8
02	3	08	9
03	4	09	10
04	5	10	11
05	6	11	12
06	7		

The COD serializer outputs (TE3A and TE3B) are then applied to the data adapter.

2-94. INPUT MULTIPLEXER.

2-95. The input multiplexer is a 26-bit latch register that is loaded by data from an output register or any one of several other sources. The source of data for insertion into the input multiplexer is selected either by the INPUT MULTIPLEXER selector switch or by certain input CIO codes. When a source is selected no other type of data can be loaded. Figure 2-13 lists the various sources of inputs to the input multiplexer and the bit positions that the data from these sources occupy in the multiplexer.

2-96. MODE REGISTER AND DISCRETE OUTPUT REGISTER DISPLAYS.

2-97. Five of the six outputs from the data adapter mode register (MOD1 and MOD3 through MOD6) are applied to circuits that light corresponding D A MODE REGISTER lamps on the LVDAME. The 13 outputs from the data adapter discrete output register are applied to circuits that light corresponding DISCRETE OUTPUT REGISTER lamps. Both lamp registers continuously display the contents of the respective data adapter registers.

2-98. ADDRESS REGISTER AND ADDRESS REGISTER DISPLAYS.

2-99. The address register is a nine-bit latch register that is loaded manually by the ADDRESS REGISTER-COMMAND switches or automatically by PIO address bits (A1V through A9V) from the interface voters. The PIO address bits are gated into the address register by -Y ADAPT PIODV NOT which is the output of the PIODV interface voter. The loading of PIO address bits is inhibited whenever an interrupt 9 or interrupt 10 is generated.

2-100. Address register outputs -Y SIM A1 through -Y SIM A9 are applied to the PIO simulator (paragraph 2-108.) Address register outputs -Y SIM A1 MULT through -Y SIM A9 MULT are applied to the input multiplexer. Address register bits are read into the input multiplexer as a result of -Y CIO (CIO 125).

2-101. The ADDRESS REGISTER-COMMAND lamp register displays the contents of the address register. The ADDRESS REGISTER-FEEDBACK lamp register displays the configuration of the address register bits from the interface voters.

Type of Data	CIO	Input Multiplexer Bits																							
		S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
GC	GC	14	13	12	11	10	09	08	07	06	05	04	03	02	01												
CR	CR	14	13	12	11	10	09	08	07	06	05	04	03	02	01												
DIN	DIN	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	2A	01	2B	25
DIS	DIS	08	07	06	05	04	03	02	01																		
CIU	DDAS	10	09	08	07	06	05	04	03	02	01																
EM	EM	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01										
ADCO	ADCO	S									S	01	02	03	04	05	06	07	08	09	10	11	12	13			
DATA VD																											
GCA	IGCA	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
GC MODR	IGCB	06	05	04	03	02	01																				
GC RTR	IGCB							01																			
GC TAGR	IGCB								08	07	06	05	04	03	02	01											
DOR	DOR	13	12	11	10	09	08	07	06	05	04	03	02	01													
SSR	SSR	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01											
TEL DA	TEL DA	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
DDAS	IDDAS	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
NA SIM	NA SIM	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
TEL TPB	TEL DB		01																								
TEL RTR	TEL DB			05	04	03	02	01																			
TEL TAGR	TEL DB								08	07	06	05	04	03	02	01											
INT	INT			10	09	08	07	06	05	04	03	02	01														
SSFB	SSFB								08	07	06	05	04	03	02	01											
OPTISYN																X1Q	X1R	X2Q	X2R	Y1Q	Y1R	Y2Q	Y2R	Z1Q	Z1R	Z2Q	Z2R
SIM	ADR																		A9	A8	A7	A6	A5	A4	A3	A2	A1
OOC	OOC																										OOC

Figure 2-13. Input Multiplexer Inputs

2-102. INTERFACE SIMULATION.

2-103. The LVDAME simulates each of the interfaces shown on figure 2-14. Only the inputs to the data adapter are described in this portion of Section II; the monitoring of data adapter outputs are described later under Interface Monitoring.

2-104. COMPUTER INTERFACE SIMULATION.

2-105. The following types of computer signals are simulated by the LVDAME:

1. Timing gates
2. Error pulses
3. Address bits
4. PIOV

2-106. TIMING SIMULATION. Computer timing gates are simulated by the master timing generator. (Refer to paragraphs 2-28 through 2-40.)

2-107. ERROR PULSE SIMULATION. Computer error pulses EP01 through EP13, EAMV, EBMV and TLC are simulated by the circuit shown on figure 10-50 sheet 74. Data from the EM register is gated to the data adapter interface at B-7-X time. Error pulses EP01 through EP13, EAMV and EBMV are supplied to the interface in simplex form; TLC is applied to a triplicator whose TMR output is applied to the interface.

2-108. ADDRESS BIT SIMULATION. Simulated computer address bits are produced by the PIO simulator. The PIO simulator is controlled manually from the LVDAME MT panel or automatically by the PTC address bits.

2-109. When the LVDAME is operated in the MAN TEST mode, the PIO simulator (figure 2-15) includes the PIO and REPEAT switches, the PIO cycle generator and the LVDAME address register. If the PIO switch is pressed when the REPEAT switch is off (REPEAT lamp is not lit), a single MAN PIO CYCLE pulse is generated that lasts from A-12-Y time till A-6-Y time. If the PIO switch is pressed when the REPEAT switch is on, MAN PIO CYCLE pulses are continuously produced. The MAN PIO CYCLE pulse(s) gate address bits from the LVDAME address register to triplicators whose outputs are applied to the data adapter interface.

2-110. When the LVDAME is operated in a mode other than MAN TEST, the PIO simulator (figure 2-16) triplicates PTC address bits and applies the TMR outputs to the data adapter interface. Note that in modes other than MAN TEST, the +Y MAN SW signat is always a "1".

2-111. POWER DISTRIBUTOR INTERFACE SIMULATOR.

2-112. The power distributor interface is simulated by the three +28 VDC power supplies located in the ETS. Power is applied to the data adapter on 12 lines as shown on figure 2-17.

2-113. Power distributor failures are simulated by the D A POWER SUPPLY switch. Failures are simulated by either opening or shorting to ground one of the three groups of data adapter voltage lines. When the D A POWER SUPPLY switch is in position 1,

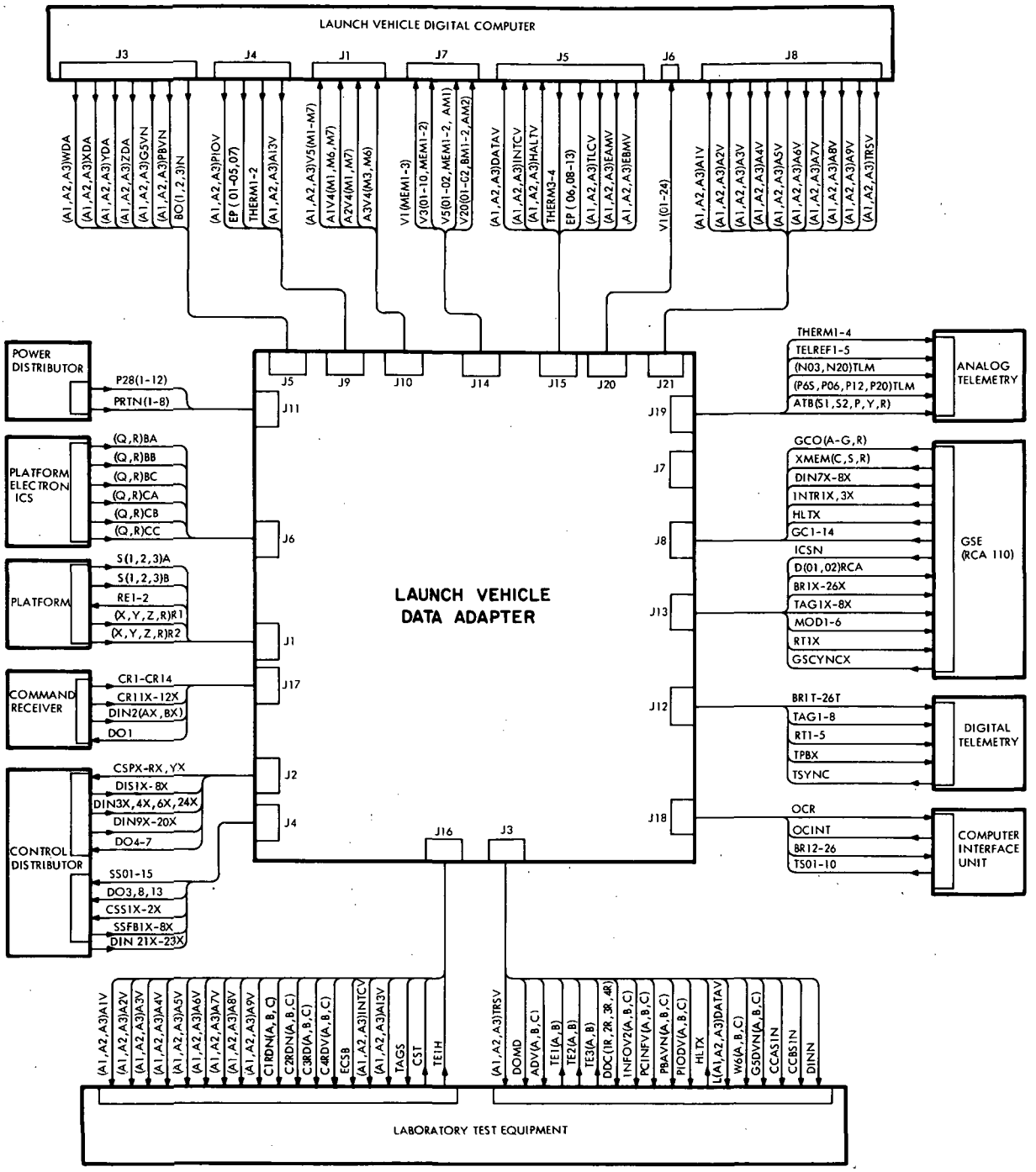
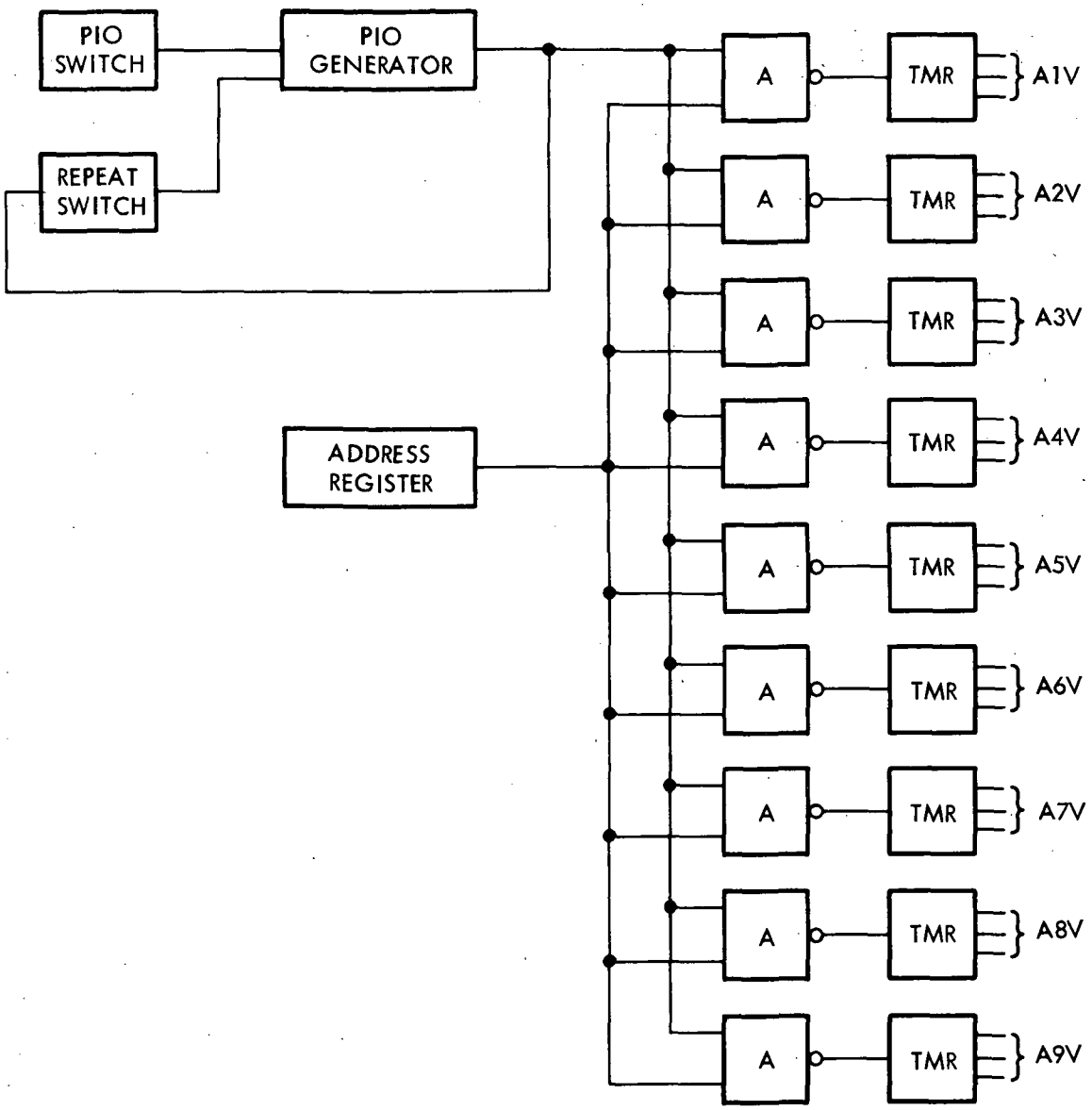
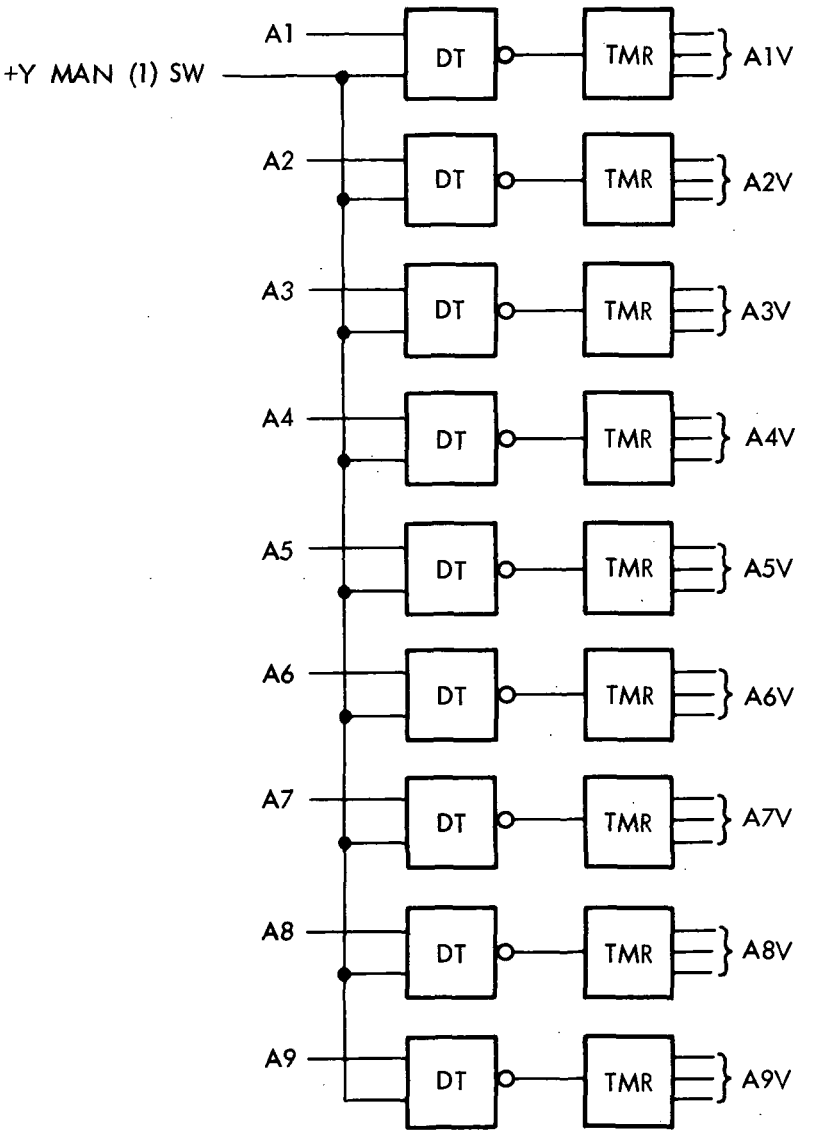


Figure 2-14. Interface Block Diagram



NOTE: EACH TMR BLOCK REPRESENTS A TRIPLICATOR.

Figure 2-15. PIO Simulator in MAN TEST Mode



NOTE: EACH TMR BLOCK REPRESENTS A TRIPLICATOR.

Figure 2-16. PIO Simulator in Modes Other Than MAN TEST

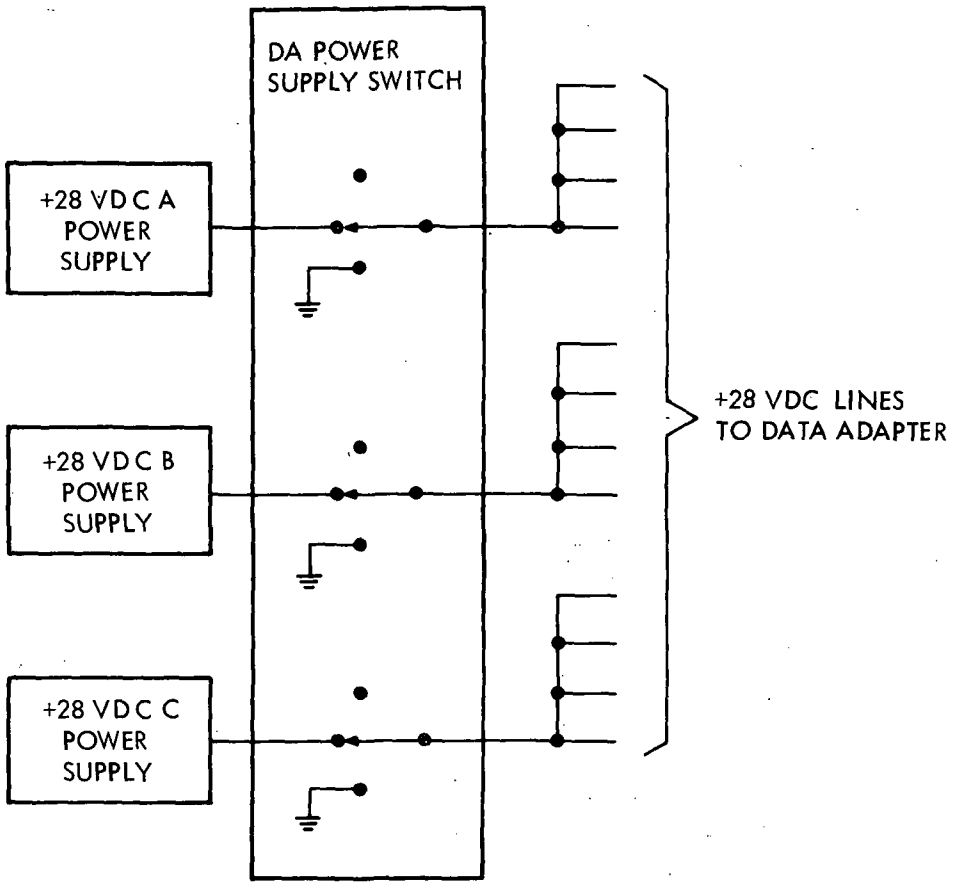


Figure 2-17. +28 VDC Power Distribution

voltages are normally applied to the data adapter; when D A POWER SUPPLY switch is in positions 2, 3, 4, 5, 6 or 7, a power distributor failure is being simulated. The data adapter should continue to operate properly under simulated power distributor failure.

2-114. PLATFORM ELECTRONICS INTERFACE SIMULATION.

2-115. The entire platform electronics interface is simulated by the three accelerometer (optisyn) simulators. Each accelerometer simulator consists of an input register, a subtractive counter, a gray code generator and a two bit output register. The speed at which the gray code generator (and hence the output register bits) is stepped is controlled by the contents of the input register. The output register bits simulate the Q and R outputs from a platform optisyn.

2-116. A single time-shared delay line serves as the three input registers and a portion of the three subtractive counters. Since each type of data (register and counter) is inserted into the delay line at different clock times, the delay line may be considered to be six separate delay lines.

2-117. INPUT REGISTERS. The three input registers (figure 2-18) receive serial data (-Y REG INFO) from the multiplexer serializer when the LVDAME is operated in the MAN TEST mode or from the PTC accumulator when the LVDAME is operated in other modes. REG INFO is inserted into a delay line only if the corresponding delay

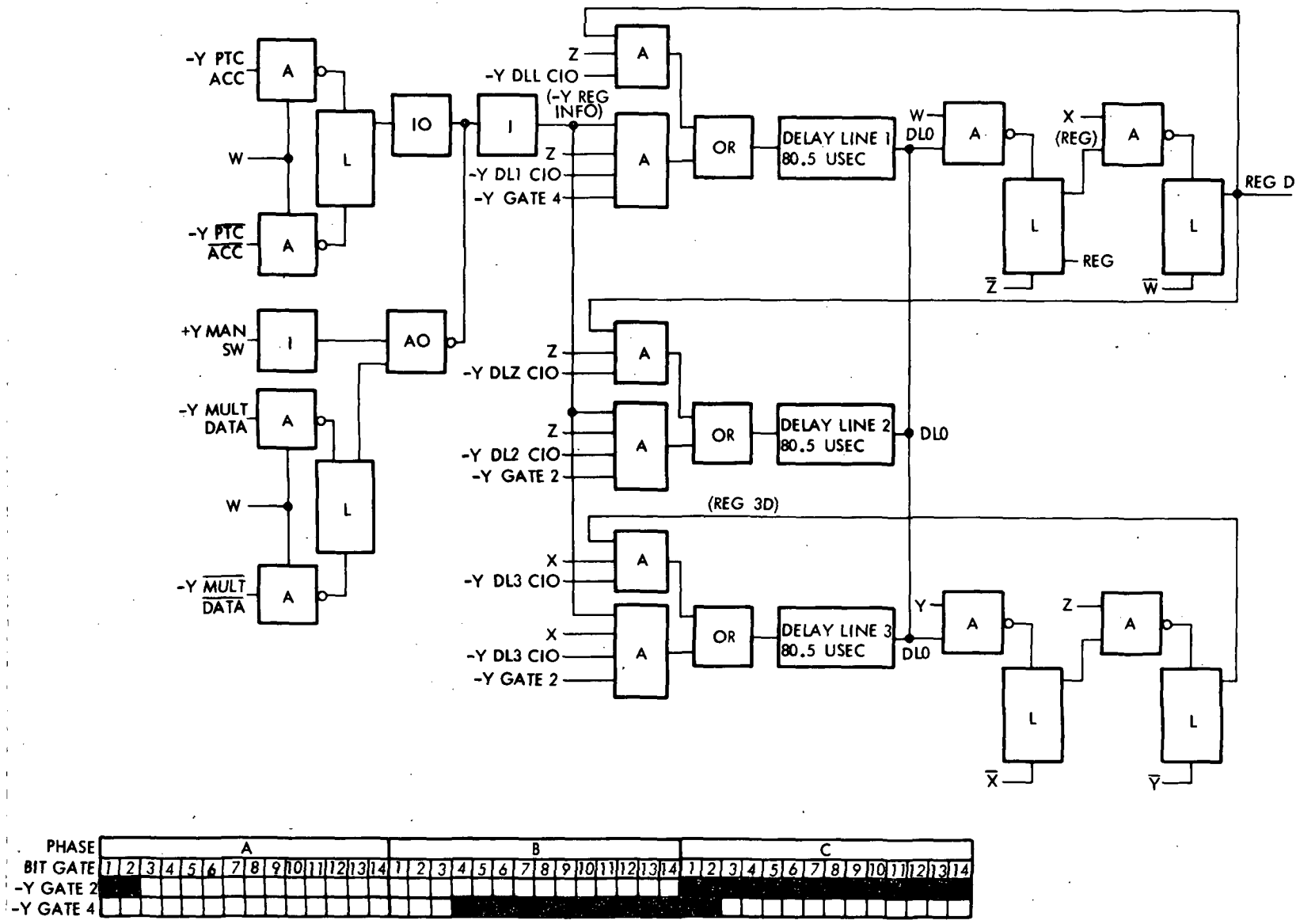


Figure 2-18. Accelerometer Simulator Input Registers

line load CIO is issued. The following paragraph describes the loading of delay line 1 (input register 1). Delay lines 2 and 3 are loaded in a similar manner.

2-118. If a load accelerometer DL1 CIO is issued, -Y DL1 CIO is a "1". The following Z clock during gate 4, -Y REG INFO begins to load delay line 1. After 80.5 USEC (three phase times minus three clock times) serial data appears at the output of delay line 1 each W time. After a three-clock delay, serial data (REG D) is reinserted into delay line 1 and -Y REG INFO is effectively stored in the input register.

2-119. SUBTRACTIVE COUNTERS. The three subtractive counters are each initially loaded with the same data that is in the corresponding input registers. Every program cycle (three phases) a binary "1" is subtracted from the contents of the counters. The subtraction is accomplished by complementing each bit that appears at the delay line output until the first "1" appears. After a "1" appears, the remaining bits are not complemented. For instance, if 0101000 is applied to the counter, 0100111 will result. The result of the subtraction is inserted into the delay line in place of the original number. As soon as the contents of the subtractive counter reach zero, a pulse (-Y URCTR 1, -Y URCTR 2 or -Y URCTR 3) is sent to the gray code generator.

2-120. Subtraction in the subtractive counters is inhibited whenever an INH ACC SUB CIO is issued and the following control bits are "1's":

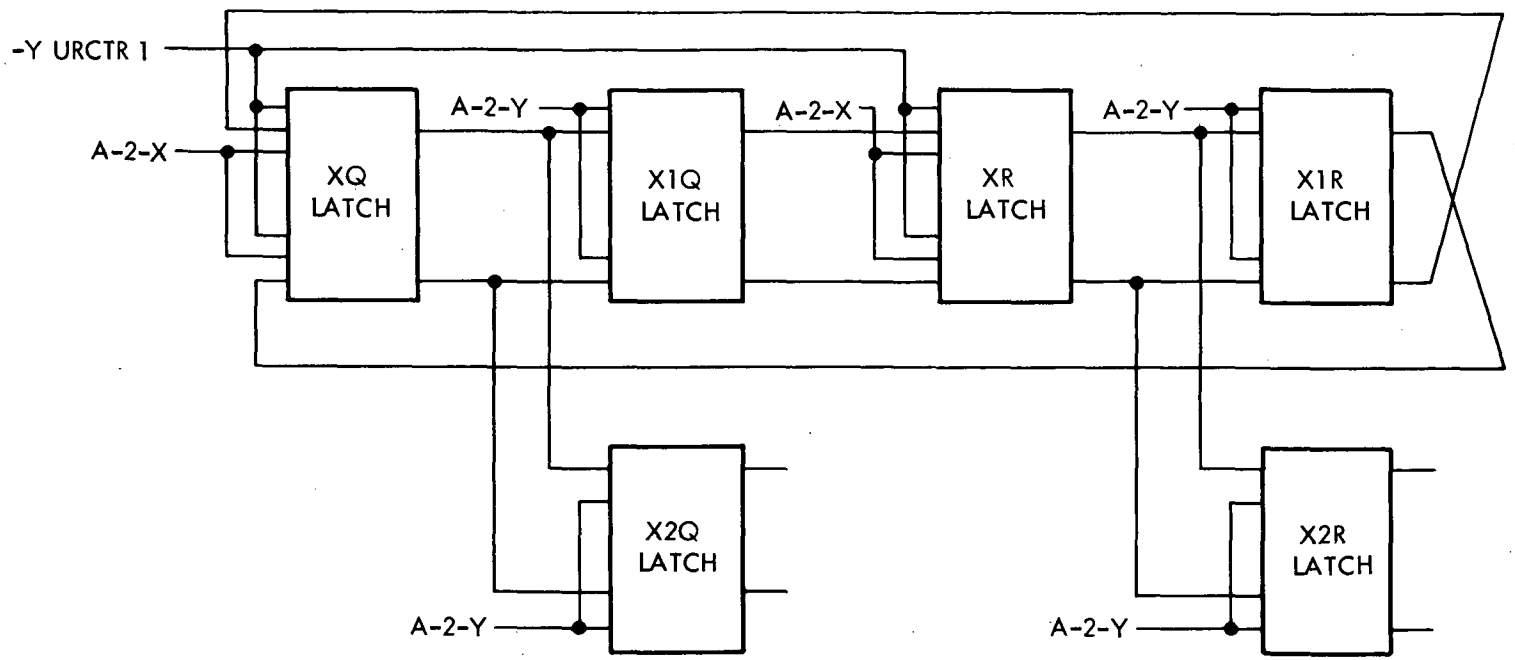
Control Bit	Subtractive Counter Inhibited
23	Counter 1
24	Counter 2
25	Counter 3

2-121. If the associated load accelerometer CIO is not present, the contents of the subtractive counter is discarded. The next time the associated input register is loaded, the contents of the input register are loaded into the subtractive counter.

2-122. GRAY CODE GENERATORS AND OUTPUT REGISTERS. The gray code generator consists of three sign-control circuits and 12 latches. The sign-control circuits determine the direction of simulated acceleration for the X, Y and Z accelerometer simulators. The 12 latches provide storage for the Q and R bits of the X, Y and Z accelerometer simulators. The following paragraphs describe the operation of the X gray code generator. The operation of the Y and Z gray code generators is similar.

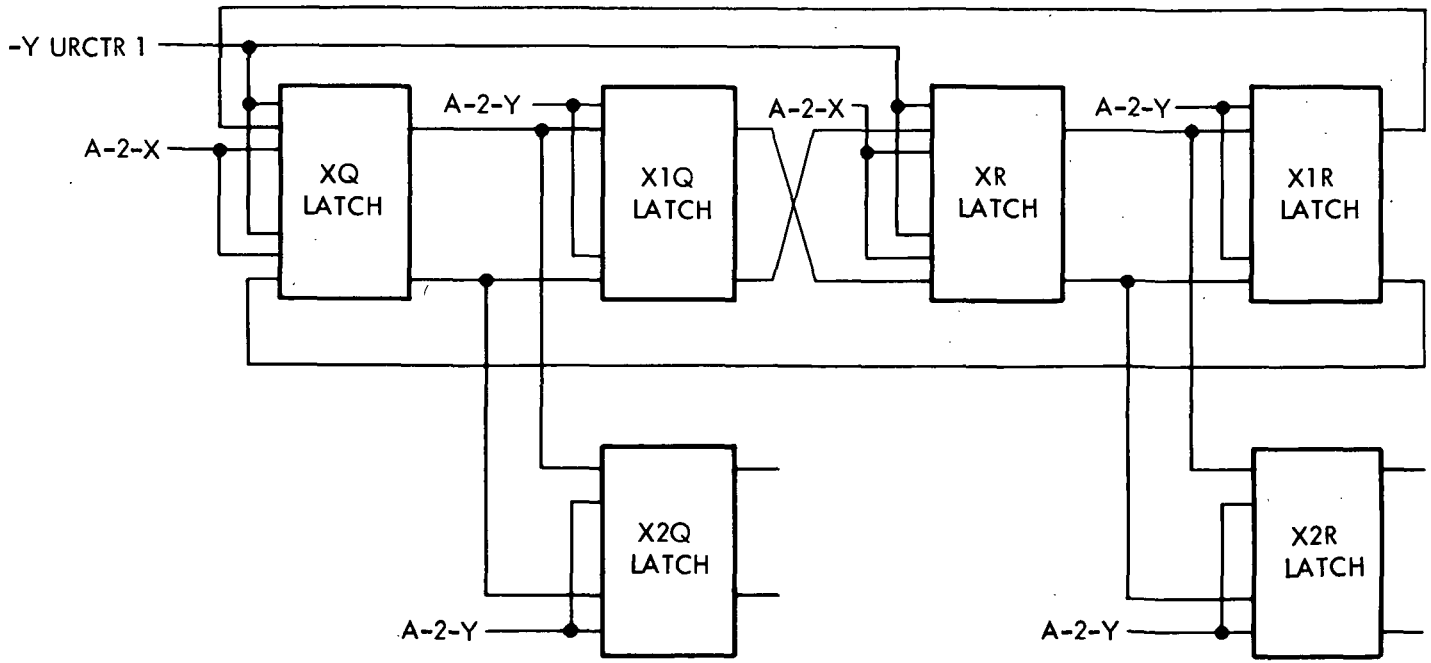
2-123. If an ACCEL P OR M CIO is issued and control bit 23 is a "1", each time a -Y URCTR 1 pulse is generated by subtractive counter 1, a "1" will appear on the -Y PLUS 1 line. This will cause the four X latches to be effectively connected as shown on figure 2-19. Successive -Y URCTR 1 pulses will cause the latches to set and reset as shown on figure 2-19. The outputs of the X1Q and X1R latches represent an increasing gray code count.

2-124. If an ACCEL P OR M CIO is issued and control bit 23 is a "0", each time a -Y URCTR 1 pulse is generated, a "1" will appear on the -Y MINUS 1 line. This will cause the four X latches to be effectively connected as shown on figure 2-20. Successive -Y URCTR 1 pulses will cause the latches to set and reset as shown on figure 2-20. The outputs of the X1Q and X1R latches represent a decreasing gray code count.



-Y URCTR 1	XQ	XR	X1Q	X1R	X2Q	X2R
1	0	0	0	0	0	0
2	0	1	0	1	0	1
3	1	1	1	1	1	1
4	1	0	1	0	1	0
SEQUENCE REPEATS FOR SUBSEQUENT -Y URCTR 1 PULSES.						

Figure 2-19. Gray Code Generator (PLUS Acceleration)



-Y URCTR 1	XQ	XR	X1Q	X1R	X2Q	X2R
1	0	0	0	0	0	0
2	1	0	1	0	1	0
3	1	1	1	1	1	1
4	0	1	0	1	0	1
SEQUENCE REPEATS FOR SUBSEQUENT -Y URCTR 1 PULSES.						

Figure 2-20. Gray Code Generator (MINUS Acceleration)

2-125. The X1Q and X1R latches form the output register for the X1 accelerometer simulator. The X2Q and X2R latches, which contain the same information as the X1Q and X1R latches respectively, form the output register for the X2 accelerometer simulator. The output registers provide signals to the data adapter interface as follows:

Latch	Interface Signal	Latch	Interface Signal
X1Q	QBA	Y2Q	QCA
X1R	RBA	Y2R	RCA
Y1Q	QBB	Z2Q	QCB
Y1R	RBB	Z2R	RCB
Z1Q	QBC	X2Q	QCC
Z1R	RBC	X2R	RCC

2-126. PLATFORM INTERFACE SIMULATION.

2-127. The platform resolver signals are simulated by the resolver simulator, which provides 18 sets of simulated resolver outputs to the data adapter COD's. Each set of outputs consists of a sine, a cosine and a reference signal. Simulated resolver outputs are generated under CIO control, or (in the absence of CIO control) are derived from a fixed source. In the latter case, each of the 18 sets of simulated resolver outputs represents a fixed resolver angle.

2-128. The resolver simulator (figure 2-21) consists basically of a supply select circuit, a tapped transformer, two sine simulators, two cosine simulators and a relay matrix. The tapped transformer provides the fixed resolver outputs and the sine and cosine simulators provide the CIO-controlled resolver outputs.

2-129. SUPPLY SELECT CIRCUIT. Excitation for the resolver simulator is provided by one of two data adapter 26-volt 1016 cycle power supplies. The supply select circuit (figure 2-22) selects one of these two power supplies and connects the power supply to the remainder of the resolver simulator. The supply select circuit consists of a CIO decoding circuit and two relays. Whenever CIO 007 is issued and control bit 07 is a "1", both relays pick and power supply number 2 is selected. Whenever CIO 007 is issued and control bit 07 is a "0", both relays drop and supply number 1 is selected.

2-130. TAPPED TRANSFORMER. The tapped transformer is a step-down transformer with 18 pairs of taps. The 18 pairs of outputs represent specific resolvers set at specific angles Each pair of taps is selected so that the voltages that appear at these taps bear the following relation:

$$V_1^2 + V_2^2 = K^2$$

NOTE

With 26 VAC applied to the primary of the tapped transformer, K = 5.

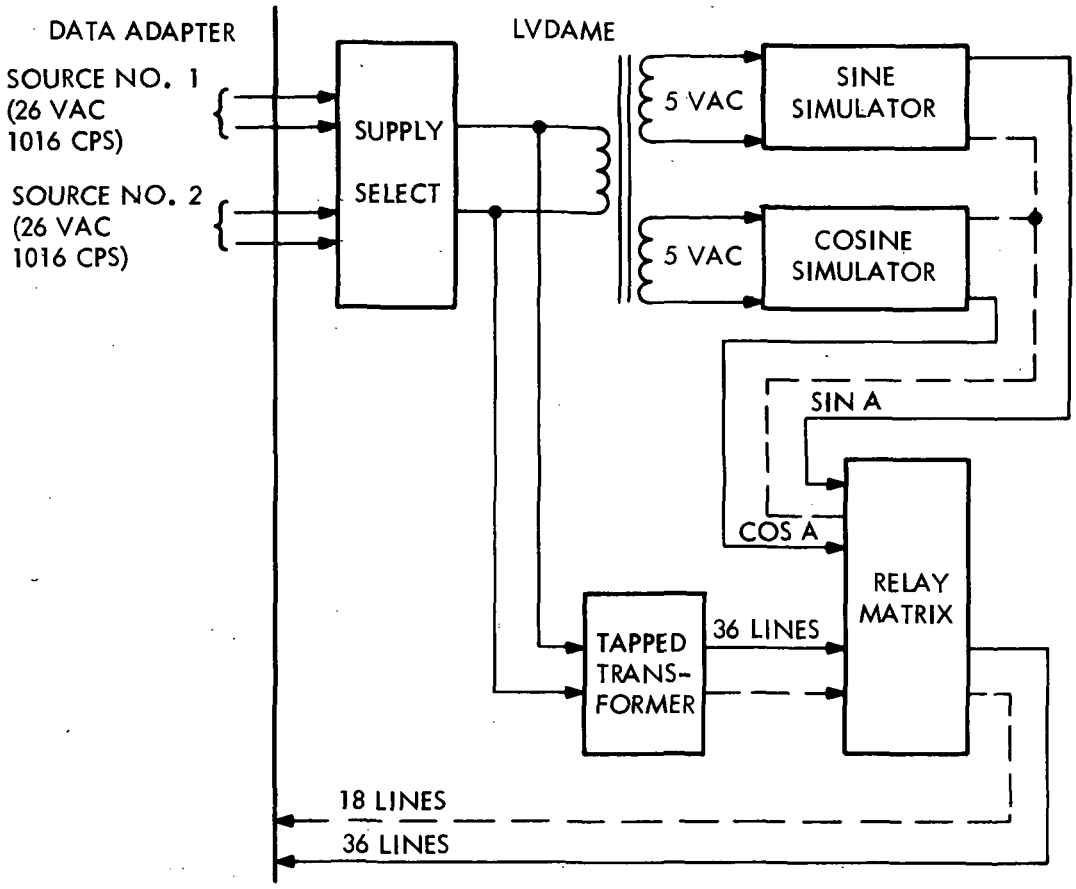


Figure 2-21. Resolver Simulator

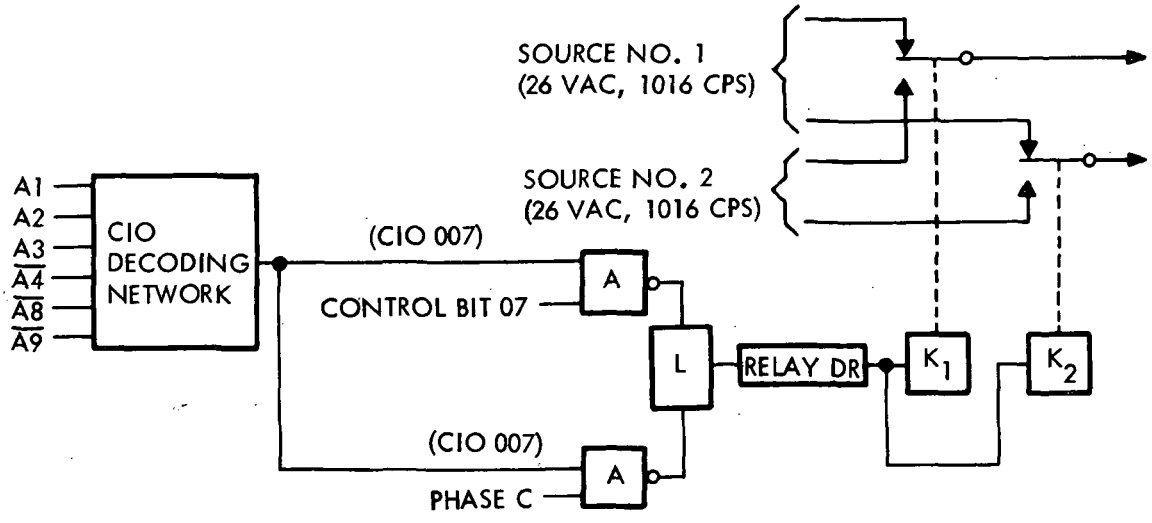


Figure 2-22. Supply Select Circuit

This is the same relationship that exists between the sine and cosine outputs of a platform resolver.

2-131. SINE AND COSINE SIMULATORS. The sine and cosine simulators provide a means of setting any simulated sine or cosine output to a value other than that provided by the tapped transformer. The sine and cosine simulators each consist of a phase select circuit, a ratio transformer and a transient suppression circuit.

2-132. Phase Select Circuits. Each phase select circuit consists of a relay which (when picked) reverses the polarity of the 5 VAC signal applied to its associated ratio transformer. The phase select relays are controlled by control bits S and 01 and a CIO decoding circuit that produces signals PHSA, PHSB and PHSC for specific CIO codes. CIO codes produce these signals as follows:

CIO Code	PHSA	PHSB	PHSC
037	1	0	0
057	0	1	0
077	1	1	0
137	1	0	1
157	0	1	1

2-133. PHSA, PHSB and PHSC and control bits S and 01 set latches that pick combinations of the four phase selection relays as follows:

Signal	Control Bit	Phase Relay(s) Picked
PHSA	S	COS A
PHSA	01	SIN A
PHSB	S	COS B
PHSB	01	SIN B
PHSC	S	SIN A and SIN B
PHSC	01	COS A and COS B

2-134. By combining the data in paragraphs 2-132 and 2-133, it can be seen that CIO-control bit combinations will pick phase select relays as follows:

CIO	Control Bit S	Control Bit 01	Phase Relays Picked
037	0	1	SIN A
	1	0	COS A
	1	1	SIN A and COS A
057	0	1	SIN B
	1	0	COS B
	1	1	SIN B and COS B
077	0	1	SIN A and SIN B
	1	0	COS A and COS B
	1	1	SIN A, COS A, SIN B and COS B
137	0	1	SIN A, COS A and COS B
	1	0	SIN A, COS A and SIN B
	1	1	SIN A, COS A, SIN B and COS B
157	0	1	COS A, SIN B and COS B
	1	0	SIN A, SIN B and COS B
	1	1	SIN A, COS A, SIN B and COS B

2-135. When a phase select relay picks, the phase of the excitation voltage for the subsequent stages of the simulator is reversed, and considered negative. The phase of each simulator is therefore positive or negative, depending on the state of the corresponding phase select relay. Once a phase select relay has been picked, it remains picked until a CIO 007 is issued or a CIO 623 and one of the following control bits is issued:

Control Bit	Relay Dropped
20	COS B
21	COS A
22	SIN B
23	SIN A

A CIO 007 sets the outputs of each similator (SIN A, COS A, SIN B and COS B) to the positive state. A CIO 623 and control bit 20, 21, 22 or 23 set the output of the associated simulator to the positive state.

2-136. Ratio Transformer. Figure 2-23 shows the SIN A ratio transformer. The SIN B, COS A and COS B ratio transformers are identical. Each ratio transformer consists of four tapped autotransformers and a 12 bit relay register. The taps on each autotransformer are set at 12.5, 25, 37.5, 50, 75, 87.5 and 100 percent of the total winding. The seven taps from each autotransformer are connected to a matrix comprised of the contacts of three relays. The relay contacts are arranged so that in the first group of three relays, the following voltages are selected as the relays are picked:

Relay(s) Picked	Tap Used	Voltage Selected
1, 2 and 3	100%	5.000 V
1 and 2	87.5%	4.375 V
1 and 3	75%	3.750 V
1	62.5%	3.125 V
2 and 3	50%	2.500 V
2	37.5%	1.875 V
3	25%	1.250 V
none	12.5%	0.625 V

2-137. The voltage from the first set of relay contacts is applied to the next autotransformer where the next group of relays select a percentage of the input voltage. The third and fourth stages operate in the same way, and the output voltage from the ratio transformer may be expressed as follows:

$$E_{out} = E_{ex} (R_4 + 1/8)(R_3 + 1/8) (R_2 + 1/8) (R_1 + 1/8)$$

where E_{ex} is the excitation voltage (5 VAC) and R_4, R_3, R_2 and R_1 are the octal contents of relay groups 4, 3, 2, and 1, respectively.

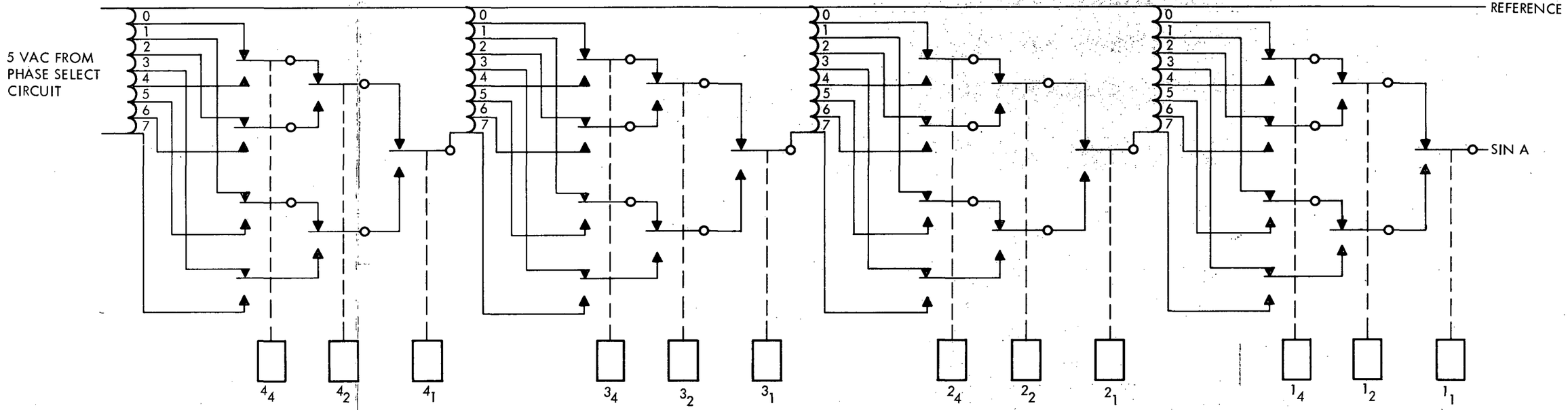


Figure 2-23. SIN A Ratiotransformer

2-138. There are 4096 different relay configurations for the 12 relays, and therefore 4096 different voltages that may appear on each ratiotransformer output line.

2-139. Each 12-bit relay register is controlled by a 12-bit latch register. The latch registers are loaded by CIO 037, 057, 077, 137 or 157. When one of these CIO's is issued, one sine latch register (SIN A or SIN B) and one cosine latch register is loaded with control bit data. Control bits 2 through 13 control latches in the cosine register, and control bits 14 through 25 control latches in the sine register.

2-140. Each successive CIO 037, 057, 177, 137, or 157, causes the alternate sine and cosine registers to be loaded. For instance if SIN A and COS A were loaded as a result of one of the above CIO's, the next CIO in this group that is issued would cause SIN B and COS B to be loaded.

2-141. The outputs from the sine simulator (SIN A and SIN B) are applied to the sine transient suppression circuit; the output from the cosine simulator (COS A and COS B) are applied to the cosine transient suppression circuit.

2-142. Transient Suppression Circuits (see figure 2-24.) The transient suppression circuits (both identical) are relay sequencing circuits that selects one of the two ratiotransformer outputs for application to the relay matrix. The four relays that comprise the sequencing circuit pick in such an order that the single output never is less than the smallest ratiotransformer output nor greater than the largest.

2-143. If the SIN B ratiotransformer were originally selected, the transient suppression circuit would select SIN A as follows:

1. K1 picks connecting SIN A to output through R1.
2. K4 picks connecting SIN B to output through R2.
3. K2 picks connecting SIN A directly to output.
4. K3 picks disconnecting SIN B from output.

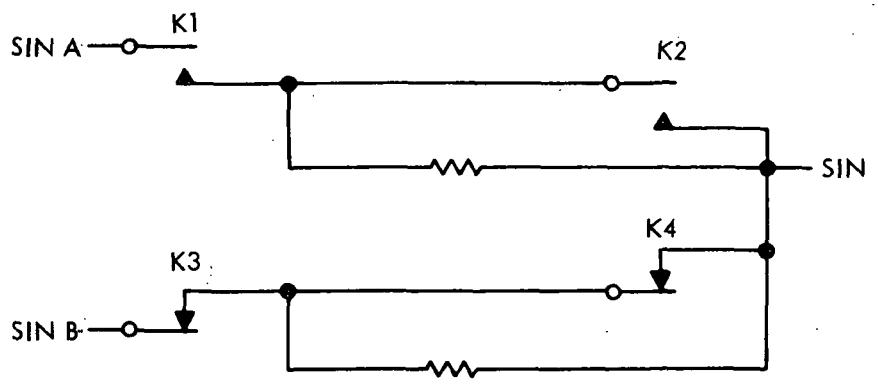


Figure 2-24. Sine Transient Suppression Circuit

2-144. If the SIN A ratiotransformer were originally selected, the transient suppression circuit would select SIN B as follows:

1. K3 drops, connecting SIN B to output through R2.

2. K2 drops, connecting SIN A to output through R1.

3. K4 drops, connecting SIN B directly to output.

4. K1 drops, disconnecting SIN A from output.

2-145. RELAY MATRIX. The 36 outputs of the tapped transformer and the two outputs from the transient suppression circuits are applied to the relay matrix. The relay matrix either allows the tapped transformer outputs to go to the data adapter interface, or connects selected simulated resolver lines to the outputs of the transient suppression circuit. When one relay picks, sine, cosine and reference for the associated simulated resolver line is connected to the output of the transient suppression circuit. This permits that particular simulated resolver to be controlled by the phase select and ratiotransformer circuits. When a relay is not picked, the fixed tapped transformer output is applied to the simulated output lines.

2-146. The relays in the relay matrix are controlled by CIO 007 and the following control bits:

*Control Bit	Relay	*Control Bit	Relay
25	1	16	10
24	2	15	11
23	3	14	12
22	4	13	13
21	5	12	14
20	6	11	15
19	7	10	16
18	8	09	17
17	9	08	18

*When the control bit is a "1" and CIO 007 is issued, the relay picks.

2-147. COMMAND RECEIVER INTERFACE SIMULATION.

2-148. The command receiver interface is simulated by translated outputs from the CR and DIN registers.

2-149. CONTROL DISTRIBUTOR INTERFACE SIMULATION.

2-150. The control distributor interface is simulated by translated outputs from the DIS, DIN and SSFB output registers.

2-151. COMPUTER INTERFACE UNIT SIMULATION.

2-152. The computer interface unit is simulated by translated outputs from the INT and DDAS output registers. OCINT is the translated bit 10 from the INT register; the 10 TS pulses are translated bits from the 10-bit DDAS register.

2-153. DIGITAL TELEMETRY INTERFACE SIMULATION.

2-154. The TSYNC signal from digital telemetry is simulated by the TSYNC generator shown on figure 10-50, sheet 62.

2-155. RCA 110 INTERFACE SIMULATION.

2-156. The generation of channel switching and power test pulses (GCOA through GCOG and GCOR) is described in paragraphs 2-76 through 2-84. The DIN, INTR and GC bits are simulated by translated outputs from the DIN, INT and CR/GC output registers respectively. The GCSYNCX and ICSN signals are simulated by the circuits on figure 10-50, sheet 62.

2-157. INTERFACE MONITORING.

2-158. All the signals leaving the data adapter that are shown on figure 2-14 are monitored or tested by LVDAME circuits. The following paragraphs describe the monitoring of some of these signals.

2-159. Channel switching logic levels to the computer interface are monitored by the circuit shown on figure 10-50, sheets 63 and 64. These logic levels are provided on 42 lines that select the two channel switching voltages used in the three TMR channels of the seven computer modules. If the wrong level appears on any one of the 42 lines for a particular commanded channel, one ERROR, one CHANNEL and one MODULE lamp on the POWER CONTROL panel will light indicating a data adapter channel switching failure.

2-160. All TMR signals to the computer interface are monitored by disagreement detectors. Disagreement detectors are described in detail in paragraphs 2-60 through 2-66.

2-261. The ladder signals to the control distributor interface are monitored by the A/D converter. The digital representation of the ladder voltage is displayed in the A/D converter display register.

2-162. The remaining data adapter digital outputs are monitored by loading them into the input multiplexer and observing the INPUT MULTIPLEXER display register. Figure 2-13 lists the bit locations in the input multiplexer for the various types of inputs.

SECTION III

INTERFACE AND CONTROLS

3-1. SCOPE.

3-2. This section describes the locations of the LVDAME interface connectors and references the drawings on which the interface signals are shown. This section also contains drawings of the LVDAME control panels and a description of each control or indicator on these panels.

3-3. INTERFACE

3-4. All of the LVDAME interface signals appear at pins of connectors located on the 9420 areas of the Data Adapter Interface Panel (01A3, figure 3-1), the Self Test Panel (01A4, figure 3-2), the right side and rear feature strips (figure 3-3). The interface signals and connectors are shown on the Cable Interface Electrical Schematic Diagrams in Section X (figures 10-12 through 10-39).

3-5. CONTROLS AND INDICATORS.

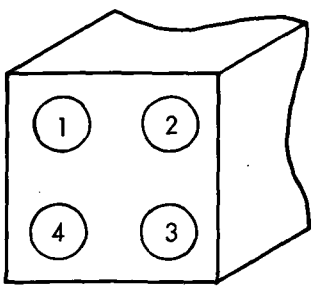
3-6. The LVDAME control panels are shown on figures 3-1, 3-2, 3-4, 3-5, and 3-6; the controls, indicators, test points, and connectors on these panels are described in figure 3-7. The location of each control panel on the LVDAME is shown on figure 1-2.

NOTE

The controls and indicators on the multiplexer and A/D converter are described in the commercial manual for these items. Refer to the list of related manuals in the front of this volume.

3-7. In addition to the controls and indicators described in figure 3-7, the AC Power Box (02B8) at the rear of the LVDAME contains an elapsed time meter (9999.9 hour) and the circuit breakers for the LVDAME AC input power.

3-8. Many of the LVDAME controls and indicators are pushbutton switches housed with four lamp bulbs that light under certain conditions. The four bulbs (1, 2, 3 and 4) are arranged as shown here:



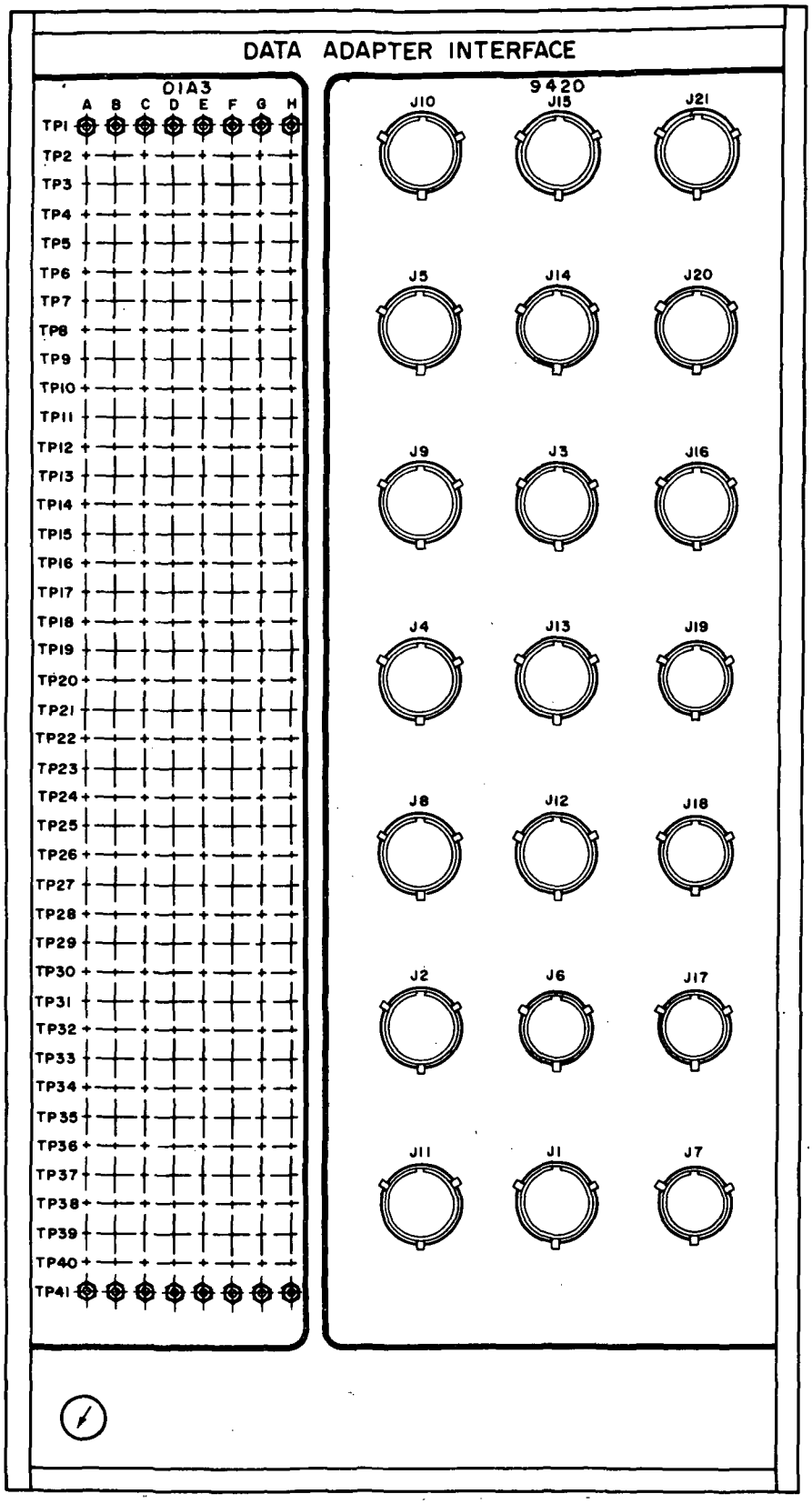


Figure 3-1. Data Adapter Interface Panel (01A3)

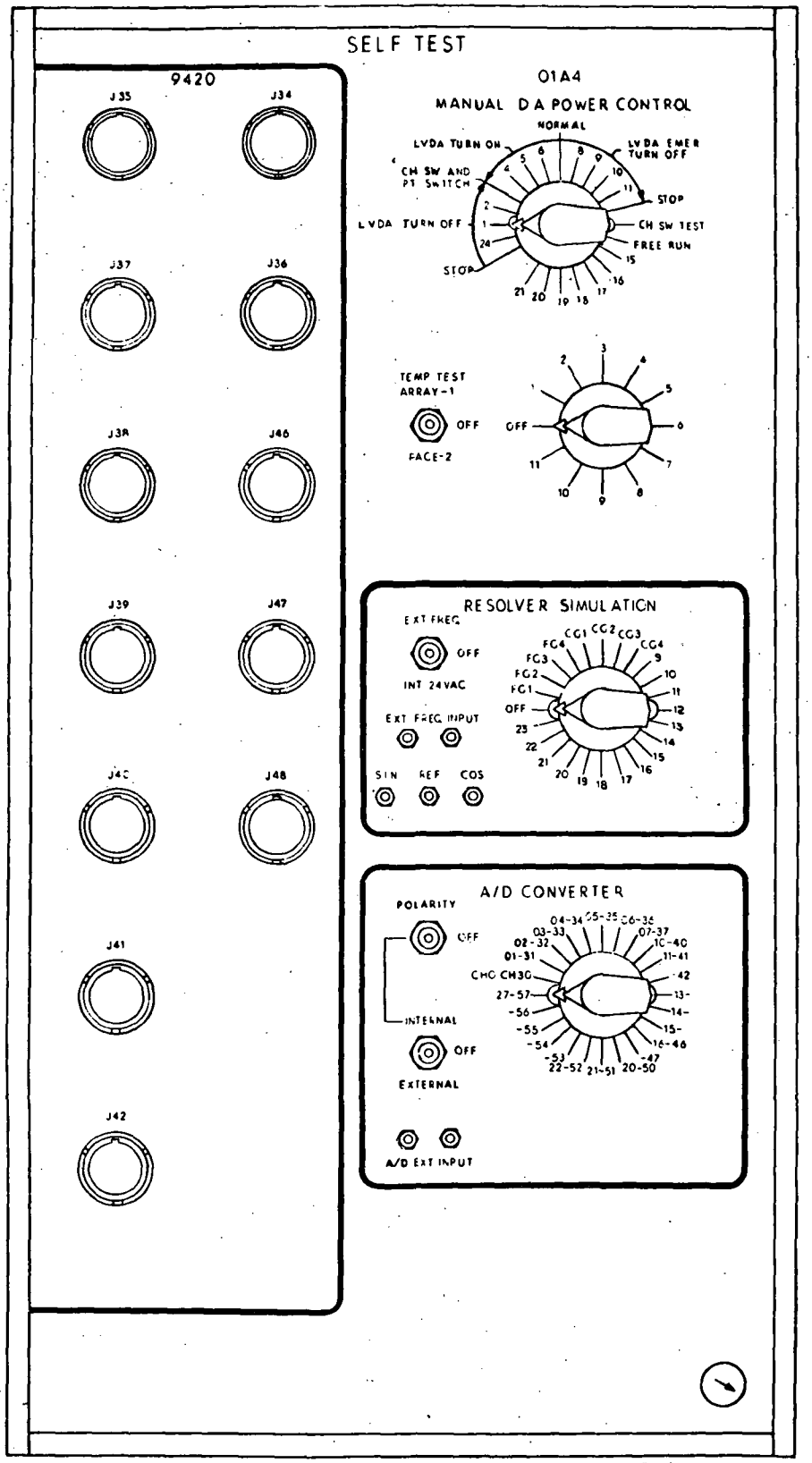
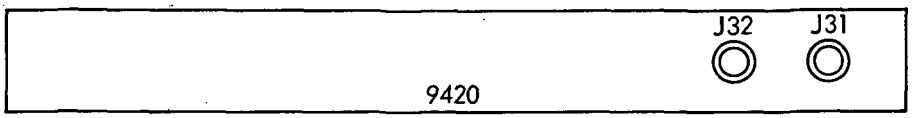
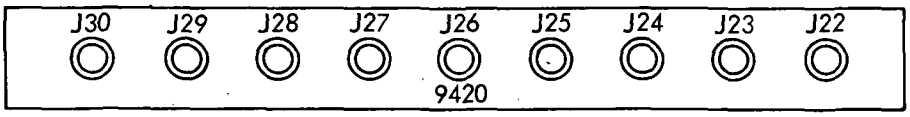


Figure 3-2. Self Test Panel



A. 9420 CONNECTORS ON RIGHT SIDE FEATURE STRIP OF 01 FRAME



B. 9420 CONNECTORS ON REAR FEATURE STRIP OF 01 FRAME

C. 9420 CONNECTOR ON REAR FEATURE STRIP OF 02 FRAME

Figure 3-3. 9420 Connectors on Feature Strips

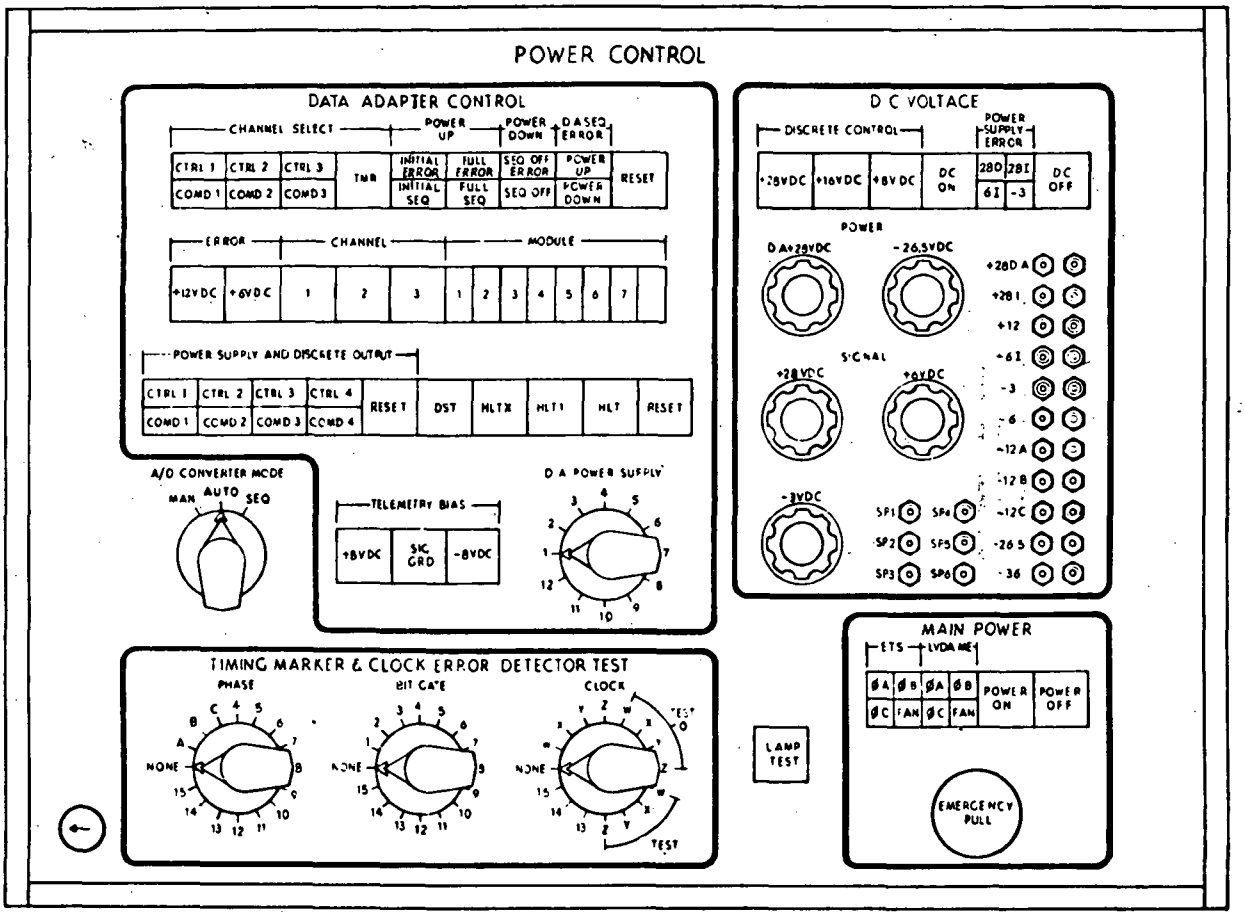


Figure 3-4. Power Control Panel (02A6)

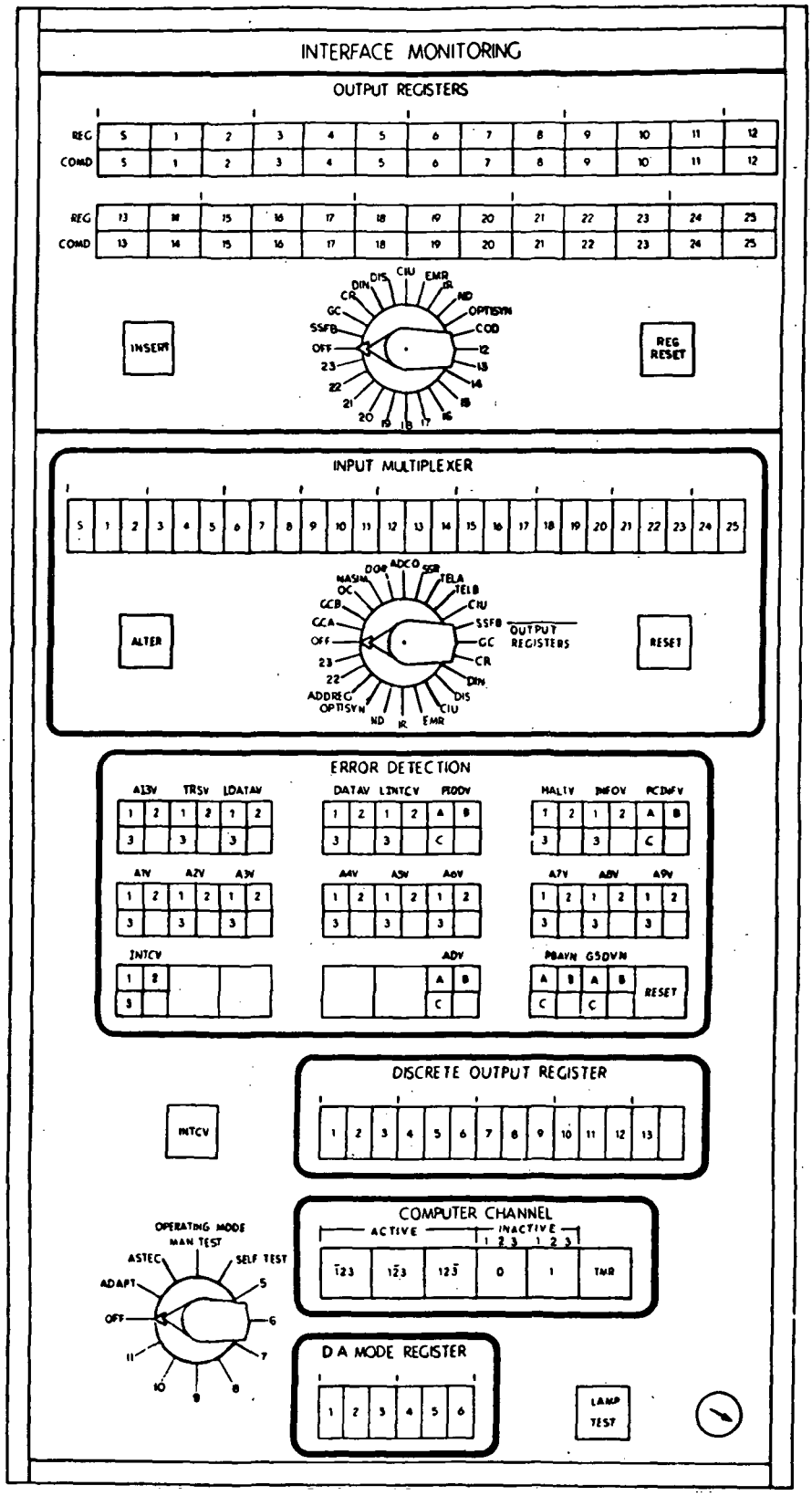


Figure 3-5. Interface Monitoring Panel (01A1)

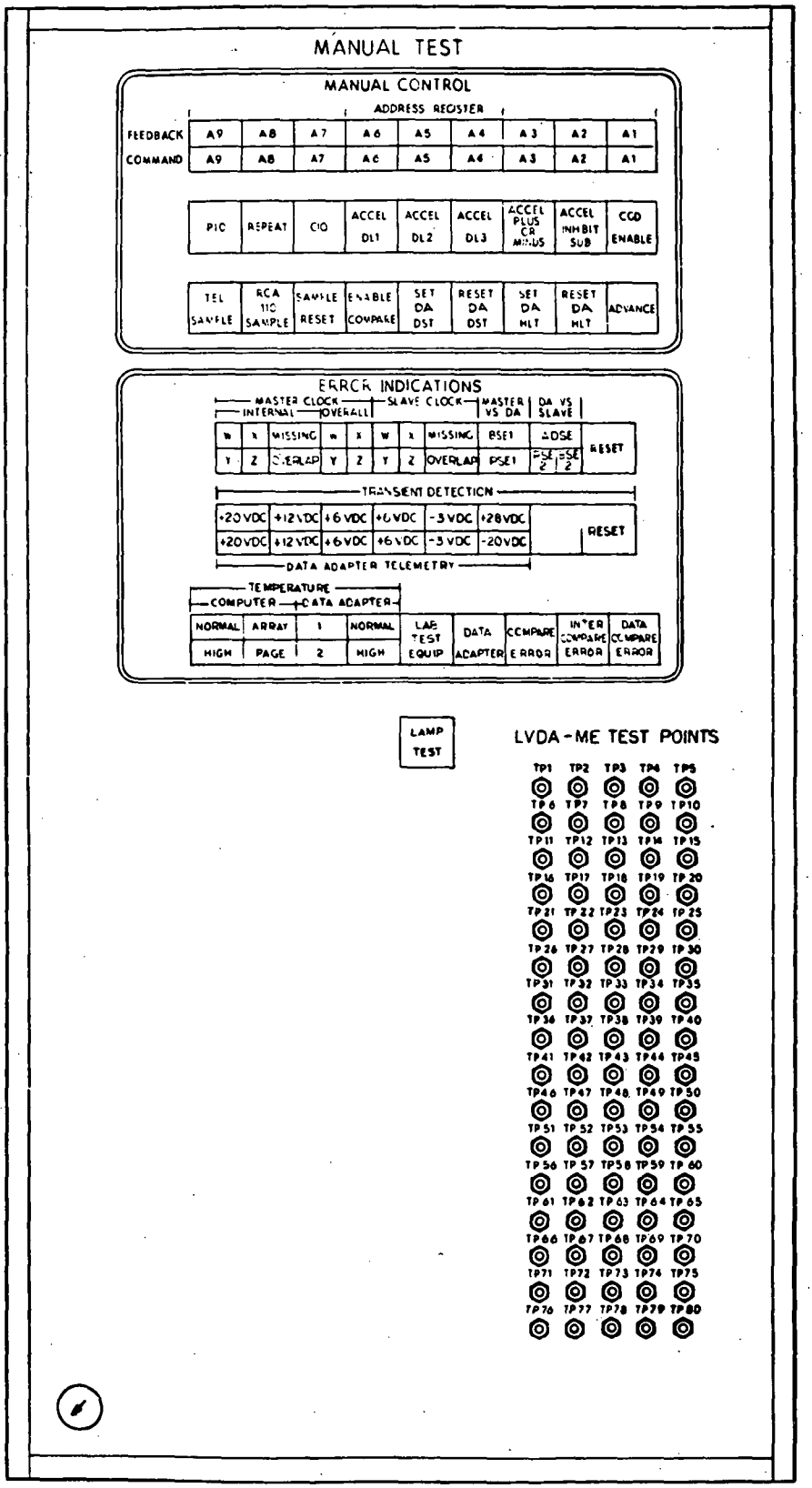


Figure 3-6. Manual Test Panel (01A2)

3-9. These bulbs can be wired in many configurations; the following five configurations are used on the LVDAME:

1. Bulbs 1 and 3 or bulbs 1 and 4 constitute one indication.

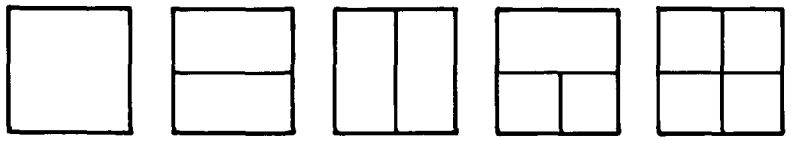
2. Bulb 1 or bulb 2 constitutes one indication; bulb 3 or bulb 4 constitutes a second indication.

3. Bulb 1 or bulb 4 constitutes one indication; bulb 2 or bulb 3 constitutes a second indication.

4. Bulb 1 or bulb 2 constitutes one indication; bulb 3 constitutes a second indication; and bulb 4 constitutes a third indication.

5. Each lamp constitutes a different indication.

3-10. The wiring configurations listed in paragraph 3-7 correspond to the following patterns on the switch faces:



NOTE

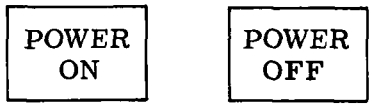
Some indicators are housed with switches to which they are not electrically connected. These indicators are explained in figure 3-7.

3-11. PUSHBUTTON SWITCH NOMENCLATURE. The nomenclature discussed in the following paragraphs is used on figure 3-7.

3-12. Momentary Action Pushbutton. A momentary action pushbutton is a momentary action pushbutton switch. The function controlled by the switch is a "1" only while the switch face (button) is being pressed.

3-13. Momentary Action Pushbutton/lamp. A momentary action pushbutton/lamp is a momentary action pushbutton switch housed with lamp bulbs. The function controlled by the switch is in the "1" state only while the bulbs within the switch assembly are lit. Normally the bulbs become lit when the switch face (button) is pressed and remain lit

until another switch is pressed, forcing the bulbs of the first switch to be extinguished. For example, the POWER ON and POWER OFF switches shown here operate in this manner:



When LVDAME power is off, POWER OFF is lit, and POWER ON is not lit. When POWER ON is pressed, POWER OFF becomes not lit and POWER ON becomes lit. When POWER OFF is again pressed, POWER ON becomes not lit and POWER OFF becomes lit.

NOTE

More than two switches may be connected in this manner, so that only one can be lit at any time.

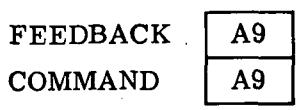
3-14. As noted in paragraph 3-8, some of the bulbs housed in certain switch assemblies are not electrically connected to the switches in these assemblies. In some cases certain bulbs are independent of the state of the switch with which they are housed while the others in that housing are directly controlled by the switch. In other cases the bulbs become lit when errors occur, and the switch in that assembly is used to reset the error indication circuit that controls the bulbs; a momentary action switch is normally used for this purpose. These special switch configurations are described on figure 3-7.

3-15. Alternate Action Pushbutton/lamp. An alternate action pushbutton/lamp is a DPDT pushbutton switch housed with lamp bulbs; the state of the switch is complemented by pressing the switch face. The lamp bulbs may be wired in one of the following ways:

1. Bulbs within the switch are lit only when the function it controls is a "1". For example, the LAMP TEST alternate action pushbutton/lamp shown here is lit only while a lamp test operation is in progress.

When LAMP TEST is pressed while its bulbs are lit, the lamp test operation ceases and the bulbs are turned off. When LAMP TEST is pressed again, another lamp test operation occurs and the bulbs are again lit.

2. The type of indication discussed in item 1 can be restricted to one half of a switch face. For example, in the A9/A9 switch shown here, the bulbs in the lower (COMMAND) portion are lit only when the function controlled by the switch in in the "1" state.



The bulbs in the upper portion only indicate the A9 signal fed back from the data adapter ("1" if lit, "0" if not lit). The bulbs in the upper portion are not electrically connected to the switch.

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
POWER CONTROL (figure 3-4) NOTE All reference designators for parts on this panel must be prefixed by 02A6, the reference designator for this panel.	DATA ADAPTER CONTROL	CHANNEL SELECT – CTRL 1/COMD 1, CTRL 2/COMD 2, and CTRL 3/ COMD 3	S14, DS15; S13, DS14; S12, DS13	Momentary action pushbutton/lamps that select channel 1, 2, or 3 operation. Lower (COMD) lamps indicate that channel 1, 2, or 3 operation has been commanded; upper (CTRL) lamps indicate that the proper combination of lines (GCOE, GCOF, or GCOG) has been selected. The output from only one of these three switches (or the TMR switch) can be a "1" at any time.
		TMR		Momentary action pushbutton/lamp that selects TMR LVDA operation. The TMR lamp automatically becomes lit when DC power is available in the LVDAME.
		POWER UP – INITIAL ERROR/ INITIAL SEQ	S10, DS11	Momentary action pushbutton/lamp that starts the LVDA power-up sequence (except the +20 VDC for the LVDC memory). When INITIAL SEQ is lit, all initial power sequencing is completed; when INITIAL ERROR is lit, an error has occurred in the initial power sequencing.
		POWER UP – FULL ERROR/ FULL SEQ	S9, DS10	Momentary action pushbutton/lamp that completes LVDA power-up sequencing by applying the memory +20 VDC. When FULL SEQ is lit, power-up sequencing is completed; when FULL ERROR is lit, an error has occurred in sequencing from the initial sequence condition to the full sequence condition.

Figure 3-7. Controls and Indicators (Sheet 1 of 22)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
POWER CONTROL (figure 3-4)	DATA ADAPTER CONTROL	POWER DOWN – SEQ OFF ERROR/SEQ OFF	S8, DS9	Momentary action pushbutton/lamp that starts the LVDA power down sequencing. When SEQ OFF is lit, LVDA power-down sequencing has been completed; when SEQ OFF ERROR is lit, an error has occurred in the power-down sequencing.
		DA SEQ ERROR – POWER UP/ POWER DOWN	DS8	Lamps that indicate that errors have occurred in power-up or power-down sequencing.
		RESET	S7	Momentary action pushbutton that resets all power sequencing error indications.
		ERROR – +12 VDC	DS24	Lamp that indicates that +12 VDC channel switching voltage is missing.
		ERROR – +6 VDC	DS23	Lamp that indicates that +6 VDC channel switching voltage is missing.
		CHANNEL – 1, 2, 3	DS22, DS21, DS20	Lamps that indicate a channel switching error in channel 1, 2, or 3.
		MODULE – 1 through 7	DS19 through DS16	Lamps that indicate module switching errors in the corresponding modules.
		MODULE – Blank		Not used.
		POWER SUPPLY AND DISCRETE OUTPUT – CTRL 1/COMD 1 through CTRL 4/COMD 4	S23, DS34 through S20, DS31	Momentary action pushbutton/lamps that command any one of four power tests and TMR discrete output tests; these switches also determine the channels in which +20 VDC is supplied to the

Figure 3-7. Controls and Indicators (Sheet 2)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
POWER CONTROL (figure 3-4)	DATA ADAPTER CONTROL	POWER SUPPLY AND DISCRETE OUTPUT – CTRL 1/COMD 1 through CTRL 4/COMD 4 (cont)	S23, DS34 through S20, DS31	computer. When one of these buttons is pressed, one of each duplexed pair of LVDA power supplies is disabled and one amplifier in the remaining power supplies is disabled. The lower (COMD) lamps indicate which test is being performed; the upper (CTRL) lamps indicate that the power test condition lines (GCOA, GCOB, GCOC, or GCOD) to the LVDA have been enabled. The output from only one of these switches can be a "1" at any time.
		POWER SUPPLY AND DISCRETE OUTPUT – RESET	S19	Momentary action pushbutton that resets any power test condition commanded by the four POWER SUPPLY AND DISCRETE OUTPUT switches.
		DST	S18, DS29	Momentary action pushbutton/lamp that forces the LVDA and LVDAME into the single-step mode of operation.
		HLTX	S17, DS28	Momentary action pushbutton/lamp that stops LVDA operation. (Used to test the HLTX line to the LVDA.)
		HLT1	S16, DS27	Momentary action pushbutton/lamp that stops LVDA operation. (Used to test the HLT1 line to the LVDA.)
		HLT	DS26	Lamp that indicates that LVDA operation has been halted.

Figure 3-7. Controls and Indicators (Sheet 3)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
POWER CONTROL (figure 3-4)	DATA ADAPTER CONTROL	RESET	S15	Momentary action pushbutton that resets the HLTX and HLT1 conditions and extinguishes the HLT lamp.
		TELEMETRY BIAS – -8 VDC, SIG GRD, and +8 VDC	S27, DS37; S26, DS36; S25, DS25	Momentary action pushbutton/lamps that connect the telemetry signal return to -8 VDC, signal ground, or +8 VDC.
		DA POWER SUPPLY	S24	Rotary switch that forces certain +28 VDC power supply output lines to open or ground when in positions 2 through 7. Switch positions 8 through 12 are not used.
	None	A/D CONVERTER MODE	S28	Rotary switch that selects manual (MAN), automatic (AUTO), or sequential (SEQ) A/D converter operation.
	TIMING MARKER & CLOCK ERROR DETECTOR TEST	PHASE	S34	Rotary switch that selects phase portion of timing marker; switch positions 4 through 15 are not used.
		BIT GATE	S33	Rotary switch that selects bit gate portion of timing marker; switch position 15 is not used.
		CLOCK	S32	Rotary switch that selects clock portion of timing marker or simulates any one of eight clock errors; switch positions 13, 14, and 15 are not used.

Figure 3-7. Controls and Indicators (Sheet 4)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
POWER CONTROL (figure 3-4)	DC VOLTAGE	DISCRETE CONTROL – +28 VDC, +16 VDC, and +8 VDC	S6, DS6; S5, DS5; S4, DS4	Momentary action pushbutton/lamps that apply +28 VDC, +16 VDC, or +8 VDC to the LVDAME translation circuits.
		DC ON	S3, DS3	Momentary action pushbutton/lamp that applies dc power to the LVDAME logic. When DC ON is lit, DC OFF is not lit, and vice versa.
		POWER SUPPLY ERROR – 28D/ 28I/6I/-3	S2, DS2	Momentary action pushbutton/lamp. The lamps in this assembly indicate failures in the corresponding interface power supplies. When this button is pressed, the power supply sense error circuits are reset and the lamps are extinguished.
		DC OFF		Momentary action pushbutton/lamp that removes DC power from the LVDAME logic. When DC OFF is lit, DC ON is not lit, and vice versa.
		POWER – DA +28 VDC, -26.5 VDC	R4, R3	Adjustments for varying the outputs of the corresponding power supplies.
		SIGNAL – +28 VDC, +6 VDC, -3 VDC	R2, R1, R7	Adjustments for varying the outputs of the corresponding power supplies.
		+28 DA, +28 I +12, +6I, -3, -6, -12A, -12B, -12C, -26.5, -36	TP1 through TP18, TP21, TP22, TP25, TP26	Pairs of test points for monitoring the outputs of the corresponding power supplies.

Figure 3-7. Controls and Indicators (Sheet 5)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
POWER CONTROL (figure 3-4)	DC VOLTAGE	SP1 through SP6	TP19, TP20, TP23, TP24, TP27, TP28	Test jacks for monitoring special power voltages; see figure 10-9, sheet 4, for voltages at each point.
	MAIN POWER	ETS – 0A/0B/0C/ FAN	DS41	Lamps that indicate that 0A, 0B, 0C and fan voltages are available in the ETC.
		LVDAME – 0A/0B/ 0C/FAN	DS40	Lamps that indicate that 0A, 0B, 0C and fan voltages are available in the LVDAME.
		POWER ON	S30, DS39	Momentary action pushbutton/lamp that applies main power to the LVDAME circuits. When POWER ON is lit, POWER OFF is not lit and vice versa.
		POWER OFF	S29, DS38	Momentary action pushbutton/lamp that removes main power from the LVDAME circuits. When POWER OFF is lit, POWER ON is not lit, and vice versa.
		EMERGENCY PULL	S35	When pulled, the emergency switch removes all power from the LVDAME.
	None	LAMP TEST	S31, DS42	Alternate action pushbutton/lamp that lights all indicator lamps on the POWER CONTROL PANEL.
INTERFACE MONITORING (figure 3-5)	OUTPUT REGISTERS	S/S through 25/25	S13, DS13 through S1, DS1 and S26, DS26 through S14, DS14	Alternate action pushbutton/lamps that select data to be loaded into a selected output register. Lower (COMD) lamps indicate that commanded data bits; upper (REG) lamps indicate the actual contents of the selected register.

Figure 3-7. Controls and Indicators (Sheet 6)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
INTERFACE *MONITORING* (figure 3-5) NOTE All reference designators for parts on this panel must be prefixed by 01A1, the reference designator for this panel.	OUTPUT *REGISTERS*	INSERT	S29	Momentary action pushbutton that transfers *the contents of the COMD switches* into the selected output register.
		Selector Switch	S28	Rotary switch that selects output register to be loaded and/or displayed as follows: OFF - No register selected SSFB - Switch Selector Feedback GC - Ground Computer or RCA 110 CR - Command Receiver DIN - Discrete Input DIS - Discrete Input Spares CIU - Computer Interface Unit EMR - Error Monitor Register IR - Interrupt Register ND - NASA Discretes OPTISYN - Accelerometer Register COD - Crossover Detector Switch positions 12 through 23 are not used.
		REG RESET	S27	Momentary action pushbutton that resets all output registers.
	INPUT MULTIPLEXER	S through 25	DS41 through DS29	Lamps that display the contents of the multiplexer register.
		ALTER	S32	Momentary action pushbutton that transfers data from the selected source into the multiplexer register.

Figure 3-7. Controls and Indicators (Sheet 7)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
INTERFACE MONITORING (figure 3-5)	INPUT MULTIPLEXER	Selector Switch	S31	Rotary switch that selects the input data source for the multiplexer register as follows: OFF - No source selected GCA - Ground Computer A GCB - Ground Computer B OC - Orbital Checkout NASIM - NASA Simulation DOR - Discrete Output Register ADCO - A/D Converter SSR - Switch Selector Register TELA - Telemetry A TELB - Telemetry B CIU - Computer Interface Unit SSFB - Switch Selector Feedback GC - Ground Computer or RCA 110 CR - Command Receiver DIN - Discrete Inputs DIS - Discrete Input Spares CIU - Computer Interface Unit EMA - Error Monitor Register IR - Interrupt Register ND - NASA Discretes OPTISYN - Accelerometer Register ADDREG - Address Register Switch positions 22 and 23 are not used.
		RESET	S30	Momentary action pushbutton that clears the multiplexer register.

Figure 3-7. Controls and Indicators (Sheet 8)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
INTERFACE MONITORING (figure 3-5)	ERROR DETECTION	A13V – 1/2/3/Blank	DS52	Lamps that indicate disagreement at the TMR interface. The nomenclature above each group of three lamps (and a blank) indicate the TMR source in which the error occurred. The lamps (1, 2, or 3; or A, B, or C) indicate the channel in which the error occurred.
		TRSV – 1/2/3/Blank	DS51	
		LDATAV – 1/2/3/ Blank	DS50	
		DATAV – 1/2/3/ Blank	DS49	
		LINTCV – 1/2/3/ Blank	DS48	
		PIODV – 1/2/3/ Blank	DS47	
		HALTV – 1/2/3/ Blank	DS46	
		INFOV – 1/2/3/ Blank	DS45	
		PCINFV – A/B/C/ Blank	DS44	
		A1V – 1/2/3/Blank through A9V – 1/2/3/Blank	DS61 through DS53	
		INTCV – 1/2/3 Blank	DS70	
		ADV – A/B/C/Blank	DS65	
		PBAVN – A/B/C/ Blank	DS64	
		G5DVN – A/B/C/ Blank	DS63	
		Blank (4)		Not used.
		RESET	S33	Momentary action pushbutton that turns off all indicator lamps in the ERROR DETECTION area.
	None	INTCV	S34, DS78	Lamp that lights when a "1" appears on the LINTCV line. (Switch is not used.)

Figure 3-7. Controls and Indicators (Sheet 9)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
INTERFACE MONITORING (figure 3-5)	DISCRETE OUTPUT REGISTER	1 through 13	DS77 through DS71	Lamps that continuously display the contents of the LVDA discrete output register.
		Blank		Not used.
	COMPUTER CHANNEL	ACTIVE – $\overline{1}23$, $1\overline{2}3$, $12\overline{3}$	S40, DS84; S39, DS83; S38, DS82	Momentary action pushbutton/lamps that select a channel to be disabled (1, 2, or 3, respectively). The output from only one of the ACTIVE switches can be a "1" at any time.
		INACTIVE – 1 2 3 – 0	S37, DS81	Momentary action pushbutton/lamp that disables the selected channel by forcing that channel to a "0". The output from only one of the INACTIVE switches can be a "1" at any time.
		INACTIVE – 1 2 3 – 1	S36, DS80	Momentary action pushbutton/lamp that disables the selected channel by forcing that channel to a "1". The output from only one of the INACTIVE switches can be a "1" at any time.
		TMR	S35, DS79	Momentary action pushbutton/lamp that enables the channel disabled by the ACTIVE and INACTIVE switches and permits TMR LVDA operation. Lamps in the ACTIVE and INACTIVE switch assemblies are extinguished when TMR is pressed.

Figure 3-7. Controls and Indicators (Sheet 10)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
INTERFACE MONITORING (figure 3-5)	None	OPERATING MODE	S41	Rotary switch that selects the LVDAME operating mode; switch positions 5 through 11 are not used.
	DA MODE REGISTER	1 through 6	DS88 through DS86	Lamps that continuously display the contents of the LVDA mode register.
	None	LAMP TEST	S42, DS85	Alternate action pushbutton/lamp that lights all indicator lamps on the INTERFACE MONITORING PANEL.
MANUAL TEST (figure 3-6) NOTE All reference designators for parts on this panel must be prefixed by 01A2, the reference designator for this panel.	MANUAL CONTROL	ADDRESS REGISTER — A9/A9 through A1/A1	S9, DS9, through S1, DS1	Alternate action pushbutton/lamps used to insert PIO/CIO address information into the address register. Lower (COMMAND) lamps indicate the contents of the address register; upper (FEEDBACK) lamps indicate the voted address bits (A1V through A9V) from LVDA.
		PIO	S18, DS18	Momentary action pushbutton that simulates the PIO operation code.
		REPEAT	S17, DS17	Alternate action pushbutton/lamp that places the LVDAME in the REPEAT mode. (In the REPEAT mode a PIO or CIO instruction is continuously repeated as long as PIO or CIO is depressed.)
		CIO	S16	Momentary action pushbutton that simulates the CIO operation code.

Figure 3-7. Controls and Indicators (Sheet 11)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	MANUAL CONTROL	ACCEL DL1 ACCEL DL2 ACCEL DL3	S15 S14 S13	Momentary action pushbuttons that load the contents of the Multiplexer Serializer into the REG #1, REG #2, or REG #3 positions of the Accelerometer Delay Line.
		ACCEL PLUS OR MINUS	S12	Momentary action pushbutton whose output is ANDed with certain DIN Register bits to cause either positive or negative accelerations for the Q and R generators.
		ACCEL INHIBIT SUB	S11	Momentary action pushbutton that inhibits subtraction in the counters so that velocity remains constant.
		COD ENABLE	S10	Momentary action pushbutton/lamp that disables the COD counters in the data adapter and allows serial data to enter the duplex data adapter COD serializers.
		TEL SAMPLE	S27	Momentary action pushbutton whose output is ANDed with a certain DIN Register bit to generate the 192 usec TSYNC pulse applied to the data adapter.
		RCA 110 SAMPLE	S26	Momentary action pushbutton whose output is ANDed with a certain DIN Register bit to generate the 192 usec GCSYNC pulse applied to the data adapter.

Figure 3-7. Controls and Indicators (Sheet 12)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	MANUAL CONTROL	SAMPLE RESET	S25	Momentary action pushbutton that enables continuous generation of TSYNC or GCSYNC at a repetition rate of 240 pulses per second.
		ENABLE COMPARE	S24	Momentary action pushbutton/lamp that is used with a DIN Register bit to permit a comparison of PTC AI3 data with the output of either the data adapter DATA line of the LVDAME Multiplexer Serializer line.
		SET DA DST	S23	Momentary action pushbutton that places the data adapter in the single step mode of operation.
		RESET DA DST	S22	Momentary action pushbutton that removes the data adapter from the single step mode of operation.
		SET DA HLT	S21	Momentary action pushbutton that applies the HALT signal to the data adapter.
		RESET DA HLT	S20	Momentary action pushbutton that removes the HALT signal from the data adapter.
		ADVANCE	S19	Momentary action pushbutton that allows a program in single step to be advanced one instruction step.
	ERROR INDICATIONS	MASTER CLOCK — INTERNAL — W/X/Y/Z	DS35	Lamps that indicate master W, X, Y, or Z clock failure.

Figure 3-7. Controls and Indicators (Sheet 13)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	ERROR INDICATIONS	MASTER CLOCK – INTERNAL – MISSING/OVERLAP	DS34	Lamps that indicate the type of master clock failure (missing or overlapping) that occurred for the clock indicated by the MASTER CLOCK – INTERNAL – W/X/Y/Z lamps.
		MASTER CLOCK – OVERALL – W/X/Y/Z	DS33	Lamps that indicate feedback W, X, Y, or Z clock failure (via self test cables only).
		SLAVE CLOCK – W/X/Y/Z	DS32	Lamps that indicate slave W, X, Y, or Z clock failure.
		SLAVE CLOCK – MISSING/OVERLAP	DS31	Lamps that indicate the type of slave clock failure (missing or overlapping) that occurred for the clock indicated by the SLAVE CLOCK – W/X/Y/Z lamps.
		MASTER VS DA – BSE1/PSE1	S30, DS30	Momentary action pushbutton/lamp. The BSE1 lamp becomes lit when the master and LVDA bit generators are out of synchronization. The PSE1 lamp becomes lit when the master and LVDA phase generators are out of synchronization. The switch is used to test the BSE1 and PSE1 error indication latches; when the button is pressed, the switch output sets the MASTER VS DA latches, thus forcing the BSE1 and PSE1 lamps to light.

Figure 3-7. Controls and Indicators (Sheet 14)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	ERROR INDICATIONS	DA VS SLAVE — ADSE/PSE2/BSE2	S29, DS29	Momentary action pushbutton/lamp. The ADSE lamp becomes lit when the LVDA timing signal ADV is out of synchronization with that of the LVDAME; the PSE2 lamp becomes lit when the LVDA and slave phase generator go out of synchronization; the BSE2 lamp becomes lit when the LVDA and slave bit generators go out of synchronization. The switch is used to test the ADSE, PSE2, and BSE2 error indication latches; when the button is pressed the switch output sets the DA VS SLAVE latches, thus forcing the ADSE, PSE2, and BSE2 lamps to light.
		RESET	S28	Momentary action pushbutton that resets all timing error indication latches that control lamps in this row.
		TRANSIENT DETECTION — +20 VDC +12 VDC +6 VDC +6 VDC -3 VDC +28 VDC	DS43 through DS38	Lamps that indicate detection of transients on the corresponding voltage line.
		TRANSIENT DETECTION — Blank		Not used.

Figure 3-7. Controls and Indicators (Sheet 15)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	ERROR INDICATIONS	TRANSIENT DETECTION – RESET	S31	Momentary action pushbutton that resets transient detection indications and data adapter telemetry voltage failure indications given by lamps in this row.
		DATA ADAPTER TELEMETRY – +20 VDC +12 VDC +6 VDC +6 VDC -3 VDC -20 VDC	DS43 through DS38	Lamps that indicate that the corresponding telemetry voltage supplies have failed.
		TEMPERATURE – COMPUTER – NORMAL/HIGH	DS52	Lamps that indicate whether the computer temperature is normal or high.
		TEMPERATURE – COMPUTER – ARRAY/PAGE	S38, DS51	Momentary action pushbutton/lamp that resets the computer temperature error indications; when the HIGH portion of COMPUTER – NORMAL/HIGH is lit, the bulbs in this indicator show whether the computer array or page temperature is high.
		TEMPERATURE – DATA ADAPTER – 1/2	S37, DS50	Momentary action pushbutton/lamp that resets LVDA temperature error indications. When the HIGH portion of DATA ADAPTER – NORMAL/HIGH is lit, the lamps in this indicator show the location of the high temperature.

Figure 3-7 Controls and Indicators (Sheet 16)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	ERROR INDICATIONS	TEMPERATURE — DATA ADAPTER — NORMAL/HIGH	DS49	Lamps that indicate whether the data adapter temperature is normal or high.
		LAB TEST EQUIP	S36, DS48	Momentary action pushbutton/lamp. An LTE error is indicated when the lamp is lit; when the button is pressed, the LTE error indication circuit is reset, and the lamp is extinguished.
		DATA ADAPTER	S35, DS47	Momentary action pushbutton/lamp. An LVDA error is indicated when the lamp is lit; when the button is pressed, the LVDA error circuit is reset, and the lamp is extinguished.
		COMPARE ERROR	S34, DS46	Momentary action pushbutton/lamp. A lit lamp indicates that the PTC accumulator data does not match the multiplexer serializer or LVDA data; when the button is pressed, the COMPARE ERROR circuit is reset, and the lamp is extinguished.
		INTER COMPARE ERROR	S33, DS45	Momentary action pushbutton/lamp. A lit lamp indicates that INTCV data does not match LINTCV data; when the button is pressed, the INTER COMPARE ERROR circuit is reset, and the lamp is extinguished.

Figure 3-7. Controls and Indicators (Sheet 17)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
MANUAL TEST (figure 3-6)	*ERROR INDICATIONS*	*DATA COMPARE ERROR*	*S32, DS44*	*Momentary action pushbutton/lamp. A lit* lamp indicates that DATAV data does not match LDATAV data; when the button is pressed, the DATA COMPARE ERROR circuit is reset, and the lamp is extinguished.
		LAMP TEST	S39, DS53	Alternate action pushbutton/lamp that lights all indicator lamps on the MANUAL TEST PANEL.
		LVDA - ME TEST POINTS — TP1 through TP80	TP1 through TP80	Test points for monitoring certain LVDAME signals. See figure 10-8, sheet 5 for the signal at each test point.
DATA ADAPTER INTERFACE (figure 3-1)	01A3	TP1-A through H through TP41-A through H	TP1-A through H through TP41-A through H	Test points for monitoring certain interface signals. See figure 10-40 for the signal at each test point.
NOTE Reference designators for test points this panel must be prefixed by 01A3, the reference designator for this panel.	9420	Connectors	J1	See figure 10-18 for signal at each pin
			J2	See figure 10-19 for signal at each pin
			J3	See figure 10-20 for signal at each pin
			J4	See figure 10-21 for signal at each pin
			J5	See figure 10-22 for signal at each pin
			J6	See figure 10-23 for signal at each pin
			J7	See figure 10-24 for signal at each pin

Figure 3-7. Controls and Indicators (Sheet 18)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
DATA ADAPTER INTERFACE (figure 3-1)	9420	Connectors (cont)	J8	See figure 10-25 for signal at each pin
			J9	See figure 10-26 for signal at each pin
			J10	See figure 10-27 for signal at each pin
			J11	Not used.
			J12	See figure 10-28 for signal at each pin
			J13	See figure 10-29 for signal at each pin
			J14	See figure 10-5 for signal at each pin
			J15	See figure 10-30 for signal at each pin
			J16	See figure 10-31 for signal at each pin
			J17	See figure 10-32 for signal at each pin
			J18	See figure 10-33 for signal at each pin
			J19	See figure 10-34 for signal at each pin
			J20	See figure 10-5 for signal at each pin
			J21	See figure 10-35 for signal at each pin
SELF TEST (figure 3-2)	9420	Connectors	J34	See figure 10-44 for signal at each pin
			J35	See figure 10-44 for signal at each pin
			J36	See figure 10-45 for signal at each pin

Figure 3-7. Controls and Indicators (Sheet 19)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
SELF TEST (figure 3-2) NOTE All reference designators for parts (except connectors) on this panel must be prefixed by 01A4, the reference designator for this panel.	9420	Connectors (cont)	J37	See figure 10-46 for signal at each pin
			J38	See figure 10-46 for signal at each pin
			J39	See figure 10-43 for signal at each pin
			J40	See figure 10-48 for signal at each pin
			J41	See figure 10-42 for signal at each pin
			J42	See figure 10-42 for signal at each pin
			J46	See figure 10-49 for signal at each pin
			J47	See figure 10-49 for signal at each pin
			J48	See figure 10-47 for signal at each pin
	None	MANUAL DA POWER CONTROL	S1	Rotary switch for manually controlling data adapter power sequencing (in switch positions STOP through STOP). In the CH SW TEST position, the switch output tests the logic circuits that monitor the module switching lines at the data adapter interface. In the FREE RUN position the switch output enables automatic exercising of the logic circuits for data adapter power sequencing. Switch positions 15 through 21 are not used.
		Selector Switch	S2	Rotary switch used to test the DA *POWER SEQUENCE ON/OFF CHECK* logic circuits.

Figure 3-7. Controls and Indicators (Sheet 20)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
SELF TEST (figure 3-2)	None	TEMP TEST – ARRAY-1/OFF/ PAGE-2	S5	Three-position toggle switch that simulates computer array and data adapter 1 temperature errors in the ARRAY-1 position and computer page and data adapter 2 temperature errors in the PAGE-2 position.
	RESOLVER SIMULATION	EXT FREQ/OFF/ INT 24 VAC	S6	Three-position toggle switch that selects the source for exciting the ratio transformer in the resolver simulator.
		EXT FREQ INPUT	TP1, TP2	Test points for applying an external frequency source to the ratio transformer.
		Selector Switch	S3	Rotary switch that selects resolver output to be applied to test points SIN and COS; switch positions 9 through 23 are not used.
		SIN, REF, COS	TP3, TP4, TP5	Test points for monitoring the resolver simulator's SIN and COS outputs as selected by Selector Switch S3.
	A/D CONVERTER	POLARITY	S7	Three-position toggle switch that selects polarity of two signals being fed into the A/D Converter when the INTERNAL/ OFF/EXTERNAL switch is in the INTERNAL position.
		INTERNAL/OFF/ EXTERNAL	S8	Three-position toggle switch that selects either external or internal input to the A/D Converter.

Figure 3-7. Controls and Indicators (Sheet 21)

Panel	Area	Control/Indicator	Ref. Des.	Description and Function
SELF TEST (figure 3-2)	A/D CONVERTER	A/D EXT INPUT	TP6, TP7	Test points for input of external source to A/D Converter.
		Selector Switch	S4	Rotary switch that selects the channels to be tested in the A/D Converter. The voltage applied to a selected channel is determined by the INTERNAL/OFF/ EXTERNAL and POLARITY switches.

Figure 3-7. Controls and Indicators (Sheet 22)

SECTION IV

TEST EQUIPMENT AND SPECIAL TOOLS.

4-1. SCOPE.

4-2. This section contains the lists of standard and special test equipment recommended for maintenance of the LVDAME. The applications of this test equipment are described in the calibration procedures in Section VII; similar applications of this test equipment are necessary in performing the troubleshooting operations discussed in Section VIII.

4-3. This section also contains the list and illustrations of the special tools recommended for maintenance of the LVDAME. The applications of these tools are briefly described in this section; many of these applications are further described in the repair procedures in Section IX.

4-4. TEST EQUIPMENT.

4-5. STANDARD TEST EQUIPMENT.

4-6. Figure 4-1 is the list of standard test equipment recommended for maintenance of the LVDAME. This equipment is not supplied with the LVDAME. Equipment having the same range and accuracy as those listed in figure 4-1 may be substituted for the items listed.

4-7. SPECIAL TEST EQUIPMENT.

4-8. Figure 4-2 is the list of special test equipment recommended for maintenance of the LVDAME. With the exception of the Differential Relay Self-Test Assembly (IBM part number 6942200), all of the equipment listed on figure 4-2 is supplied with the LVDAME.

4-9. SPECIAL TOOLS.

4-10. Figure 4-3 is the list of special tools recommended for maintenance of the LVDAME; these tools are illustrated in figure 4-4. These tools are not supplied with the LVDAME. Equivalent tools may be substituted for the items listed.

Name	Model or Type	Vendor
Oscilloscope	585A	Tektronix, Inc.
Plug-in Unit	M	Tektronix, Inc.
Plug-in Adapter	81	Tektronix, Inc.
Differential Voltmeter AC/DC	803-B	John Fluke Mfg. Co., Inc.
Digital Voltmeter	456	Kintel Division, Cohu Electronics, Inc.
AC Converter	452	Kintel Division, Cohu Electronics, Inc.
Digital Readout	473A	Kintel Division, Cohu Electronics, Inc.
Volt-Ohm-Ammeter	630-A	Triplett Electrical Instrument Co.
Volt-Ohmmeter	269	Simpson Electric Co.
Capacitance Bridge	650-A	General Radio Co.

Figure 4-1. Recommended Standard Test Equipment

Equipment	IBM Part Number	Equipment	IBM Part Number
Contact Strip	216259	Printed Circuit	6941161
Jumper Plug	6940017	Board Assembly	6941162
	6940018		6941163
	6940019		6941164
Printed Circuit	6941135		6941165
Board Assembly	6941136		6941166
	6941137		6941167
	6941138		6941168
	6941139		6942140
	6941140	Cable Assembly	6942051
	6941141		6942052
	6941142		6942053
	6941144		6942054
	6941145		6942055
	6941146		6942056
	6941151		6942057
	6941155		6942058
	6941156		6942188
	6941157	Differential Relay	6942200
	6941158	Self-Test	
	6941159	Assembly	

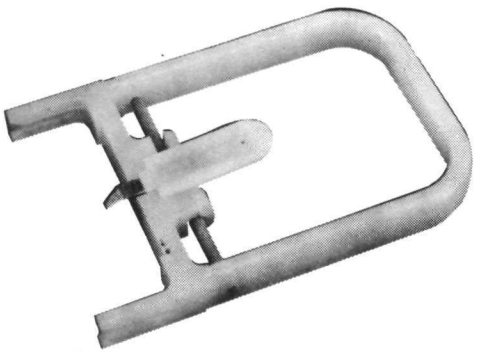
Figure 4-2. List of Special Test Equipment

Name	Vendor Part No.	Application	Illustration Figure 4-3
SMS Card Puller	IBM 6072429	Facilitates insertion or removal of SMS cards.	Part A
SMS Card Contact Lubricant	IBM 6072430	Insures low contact resistance and reduces wear of the gold-plated SMS card contact surfaces.	Part B
SMS Card Extender	IBM 6072431	Allows access to the components and wiring of an SMS card while the card is connected into the system.	Part C
SMS Card Socket Terminal Extractor	IBM 6072432	Used to remove SMS card socket terminals (contacts).	Part D
Soldering Handle	Hexacon P25	Handle for soldering tip.	Part E
Soldering Tip	Hexacon HT248D	Used to remove or install SMS card socket terminals that are soldered to a printed circuit overlay or a voltage chain.	Part F
Hand Wire-Wrap Tool	IBM 6072438	A manual, squeeze-type wire-wrap tool used to wire-wrap SMS card socket terminals.	Part G
Wrapping Bit-22	Keller A-18632	Used with hand wire-wrap tool to wrap AWG22 wire.	Part H
Wrapping Bit-20	Keller A-18633	Used with hand wire-wrap tool to wrap AWG20 wire.	
Wrapping Bit-24	Keller A-26232	Used with hand wire-wrap tool to wrap AWG24 wire.	
Wrapping Bit-26	Keller A-27611	Used with hand wire-wrap tool to wrap AWG26 wire.	
Sleeve - 26	Keller A-17611-2	Used with hand wire-wrap tool to wrap AWG24-26 wire.	Part I
Sleeve - 22, 24	Keller A-18840	Used with hand wire-wrap tool to wrap AWG22 wire.	
Sleeve - 20	Keller A-18285	Used with hand wire-wrap tool to wrap AWG20 wire.	
Unwrap Tool	IBM 6072437	Used to unwrap both right and left-hand wraps.	Part J
Crimping Tool Kit	Bendix 11-7295	Used to crimp size 12, 16 and 20 type connector contacts.	Part K
Insertion Tool	Bendix 11-6781-16	Used to insert size 16 contacts in Bendix type connectors.	Part L

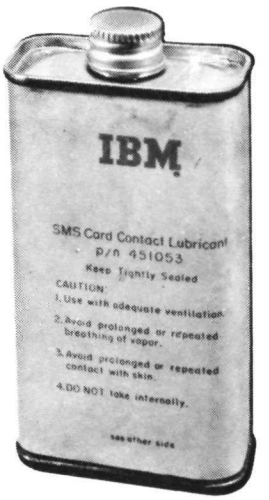
Figure 4-3. List of Recommended Special Tools (Sheet 1 of 2)

Name	Vendor Part No.	Application	Illustration Figure 4-3
Insertion Tool	Bendix 11-8107-20	Used to insert size 20 contacts in Bendix type connectors.	Part M
Contact Removing Tool Kit	Bendix 11-6900	Used to remove size 16 and 20 contacts in Bendix type connectors.	Part N
Spanner Wrench	Bendix 11-3544	Used on Bendix type connector spanner nuts.	Part O
Connector Pliers	Bendix 6147-1	Used to hold knurled or serrated surfaces on Bendix type connectors.	Part P
Crimping Tool	AMP 59501	Used to crimp AWG22-24 solid or stranded wire.	Part Q
Crimping Tool	Berg HT-3-20	Used to crimp AWG20 solid or stranded wire to a slip-on terminal.	Part R
Crimping Tool	Berg HT-3-22	Used to crimp AWG22 solid or stranded wire to a slip-on terminal.	
Crimping Tool	Berg HT-3-24	Used to crimp AWG24 solid or stranded wire to a slip-on terminal.	
Attenuator Probe	Tektronix P-6017	General purpose probe with nine-foot cable terminating at a UHF connector.	Part S
Current Probe	Tektronix P-6016	Special purpose probe used when monitoring current characteristics.	Part T
Passive Termination	Tektronix 011-028	Used with the current probe when monitoring current characteristics.	Part U
Switch Assembly Wrench	IBM 6900017	Facilitates removal of switches from switch housings.	Part V
Switch Assembly Extractor	IBM 6900020	Facilitates removal of screens and light modules from switch housings.	Part W
Tool Case	IBM 6445032	Used for carrying tools.	Part X
Intercase	IBM 6445698	Used for carrying tools.	Part Y

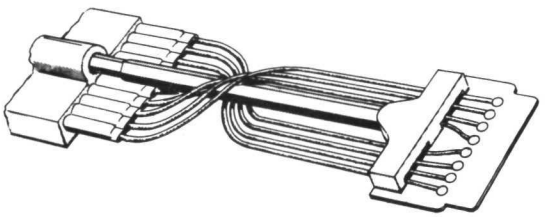
Figure 4-3. List of Recommended Special Tools (Sheet 2)



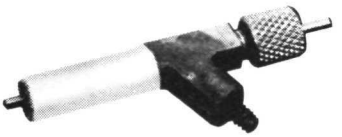
Part A. SMS Card Puller



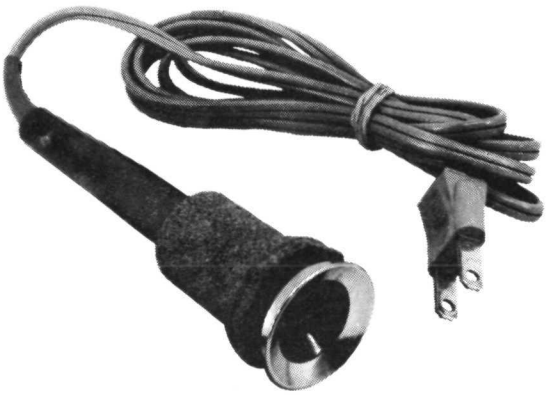
Part B. SMS Card Contact Lubricant



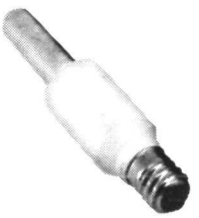
Part C. SMS Card Extender



Part D. SMS Card Socket Terminal Extractor



Part E. Soldering Handle



Part F. Soldering Tip

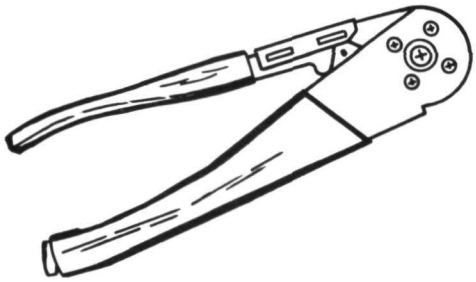
Figure 4-4. Recommended Special Tools (Sheet 1 of 4)

Part G. Hand Wire-Wrap Tool

Part H. Wrapping Bit (Typical)

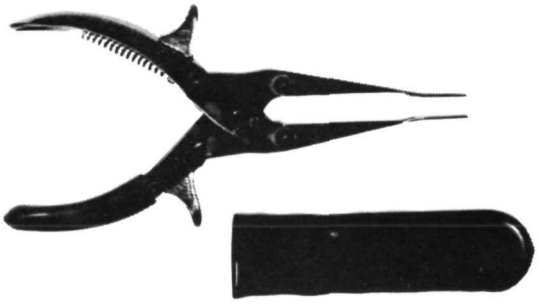
Part I. Sleeve (Typical)

Part J. Unwrap Tool

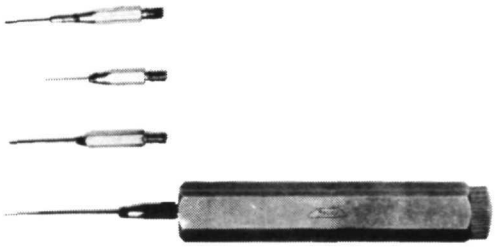


Part K. Crimping Tool Kit

Part L. Insertion Tool

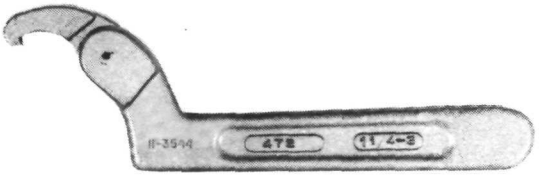


Part M. Insertion Tool



Part N. Contact Removing Tool Kit

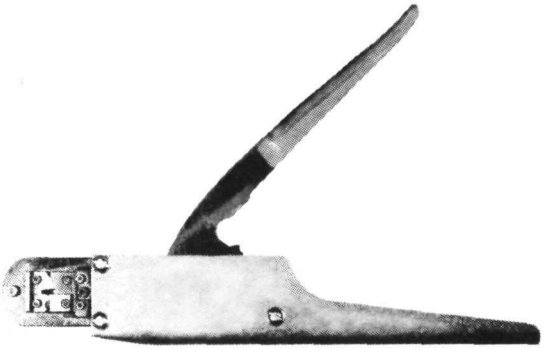
Figure 4-4. Recommended Special Tools (Sheet 2)



Part O. Spanner Wrench

Part P. Connector Pliers

Part Q. Crimping Tool



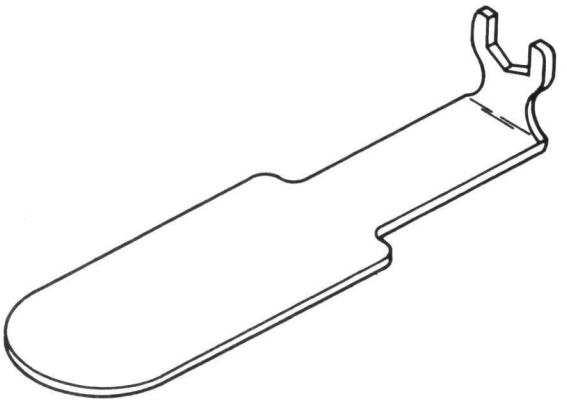
Part R. Crimping Tool (Typical)

Part S. Attenuator Probe

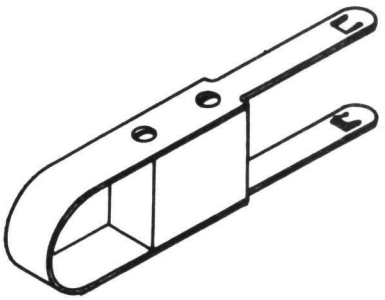
Part T. Current Probe

Figure 4-4. Recommended Special Tools (Sheet 3)

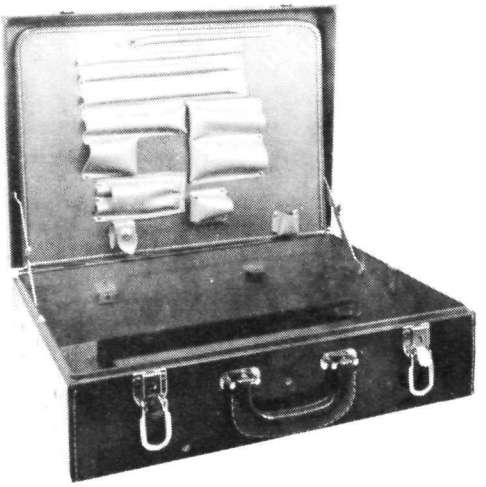
Part U. Passive Termination



Part V. Switch Assembly Wrench



Part W. Switch Assembly Extractor



Part X. Tool Case

Part Y. Intercase

Figure 4-4. Recommended Special Tools (Sheet 4)

SECTION V

PREPARATION FOR USE, STORAGE, AND SHIPMENT

5-1. SCOPE.

5-2. This section describes the procedures for preparing the LVDAME for use, storage, and shipment.

5-3. PREPARATION FOR USE.

5-4. UNPACKING.

5-5. The LVDAME is not packed for shipment. No unpacking is necessary.

5-6. INSPECTION.

5-7. The LVDAME should be inspected for evidence of damage caused by improper handling during shipment. Access to the interior of the LVDAME is explained in Section I (figure 1-4).

5-8. The loose parts shipped with the LVDAME should be checked against those listed in figure 5-1.

Equipment	IBM Part Number	Equipment	IBM Part Number
Contact Strip	216259	Printed Circuit	6941161
Jumper Plug	6940017	Board Assembly	6941162
	6940018		6941163
	6940019		6941164
Printed Circuit	6941135		6941165
Board Assembly	6941136		6941166
	6941137		6941167
	6941138		6941168
	6941139		6942140
	6941140	Cable Assembly	6942051
	6941141		6942052
	6941142		6942053
	6941144		6942054
	6941145		6942055
	6941146		6942056
	6941151		6942057
	6941155		6942058
	6941156		6942188
	6941157		
	6941158		
	6941159		

Figure 5-1. List of Loose Parts Shipped with the LVDAME

5-9. ASSEMBLY.

5-10. The LVDAME is assembled before shipment. No assembly is necessary.

5-11. INSTALLATION.

5-12. Refer to Volume I of this manual for installation instructions.

5-13. TESTS.

5-14. Before using the LVDAME, perform all calibration checks as described in Section VII.

5-15. PREPARATION FOR STORAGE.

5-16. Prepare the LVDAME for storage as follows:

a. Close all hinged panels and card gates.

b. Disconnect the LVDAME from the data adapter, test stand, and any other test equipment.

c. Disconnect the LVDAME from the AC power source.

d. Install dust caps on all connectors.

e. Cover the LVDAME with a dust cover.

f. Inventory loose parts as described in paragraph 5-8 and store parts in a carton near the LVDAME.

5-17. PREPARATION FOR SHIPMENT.

5-18. Prepare the LVDAME for shipment as described in steps a through e of paragraph 5-16. Inventory loose parts as described in paragraph 5-8 and package the parts in a carton for shipment.

SECTION VI

PREVENTIVE MAINTENANCE

6-1. SCOPE.

6-2. This section describes the recommended inspection and preventive maintenance for the LVDAME.

6-3. INSPECTION.

6-4. There is no recommended daily inspection schedule for the LVDAME. However, if exterior damage, obstruction to airflow, or deterioration or discoloration of panel markings is noted during daily use of the LVDAME, repair the fault as described in Section IX.

CAUTION

Never allow an object to obstruct the openings in the base and top of the LVDAME which permit the intake and exhaust of cooling air.

6. 5. PREVENTIVE MAINTENANCE.

6-6. Because the LVDAME uses SMS cards, preventive maintenance is held at a minimum. Figures 6-1 and 6-2 prescribe the preventive maintenance for the LVDAME. These figures list the items to be maintained, the location of each item, the frequency at which each item should be inspected, and the method of inspection and maintenance.

ASSEMBLY LVDAME (6942000) General
REFERENCE MANUAL None

Item	Location	Frequency	Observe	Clean	Lubricate	Notes
Air Filters	Bottom of frames 01 and 02.	Monthly.	Check for cleanliness.			Replace if necessary.
Fans	One in each gate assembly and power supply assembly.	Monthly.	Check for cleanliness; check for any obvious faults such as noisy operation or wear.	Clean with hose type vacuum cleaner if necessary.		Replace if necessary.

Figure 6-1. LVDAME General Preventive Maintenance

ASSEMBLY A/D Converter (01A2) and Multiplexer (01A3) Adage Models VR13-AB/NE and VMX40B/VMX8DB
REFERENCE MANUAL VR13-AB/NE/VMX40B/VMX8DB Instruction Manual

Item	Location	Frequency	Observe	Clean	Lubricate	Notes
Entire unit	Entire unit	Two Months	Check for cleanliness.	Clean with hose type vacuum cleaner.		
Switches	Front panels	Two Months			Lightly apply a high quality switch cleaner/lubricant* to the contact areas of the switches.	Perform lubrication only if the switches are used frequently.

*Super Wissh with Silicone 7, Workman Electronic Products, Inc., or equivalent.

Figure 6-2. A/D Converter (01A2) and Multiplexer (01A3) Preventive Maintenance

SECTION VII

CALIBRATION

7-1. GENERAL.

7-2. This section contains the calibration procedures for the LVDAME. Since the LVDAME cannot operate without the Equipment Test Stand (ETS), calibration procedures for the ETS are also included in this section. Calibration consists of those checks and adjustments needed to ensure the operability of the LVDAME and ETS.

7-3. CALIBRATION FREQUENCY.

7-4. All calibration procedures (figures 7-1 through 7-36) must be performed at least once a month. All calibration procedures or any one check may be performed at any time for trouble isolation. The procedures are presented in such a manner that they may be performed in the sequence given, or any check may be performed by itself. Lamp tests (figure 7-2) should be performed before any LVDA test or LVDAME calibration check is performed.

7-5. CALIBRATION PROCEDURES.

7-6. Calibration procedures are divided into check procedures and adjustment procedures. The check procedures are found in figures 7-1 through 7-29; the adjustment procedures are found in figures 7-30 through 7-36.

7-7. CHECK PROCEDURES.

7-8. The check procedures are as follows:

Figure	Procedure Name
7-1	Power Checks
7-2	Lamp Tests
7-3	Discrete Control Check
7-4	LVDA Power Supply Check
7-5	LVDA Power Control Check
7-6	Channel Switching and Power Test Checks
7-7	Telemetry Return Check
7-8	Timing Checks
7-9	Data Compare Error Check
7-10	Output Registers and Input Multiplexer Checks

Figure	Procedure Name
7-11	COD Serializer Check
7-12	LVDA Interface Feedback Check
7-13	Multiplexer Serializer Check
7-14	Load of EM Register from LDATAV Line Check
7-15	Error Detection and Computer Channel Control Checks
7-16	Address Register Feedback Check
7-17	Input Multiplexer Load from Address Register Check
7-18	TSYNC, GCSYNCX and ICSN Checks
7-19	Enable Compare Check
7-20	CST, DST and HLT Checks
7-21	CIO Codes Manual Check
7-22	Interrupt Checks
7-23	COD Enable and TE1H Checks
7-24	A/D Converter Manual Check
7-25	Temperature Indicators Check
7-26	Interrupt Compare Error Check
7-27	Resolver Simulator Check
7-28	Interrupt 15 and Power Sequencing Telemetry Checks
7-29	Optisyn Simulator Check

7-9. ADJUSTMENT PROCEDURES.

7-10. The adjustment procedures are as follows:

Figure	Procedure Name
7-30	DC Adjustments
7-31	Data Adapter Control Adjustments
7-32	Output Register Insert Single-Shot Adjustment
7-33	TSYNC and GCSYNCX Adjustments
7-34	Input Multiplexer Alter Single-Shot Adjustment

Figure	Procedure Name
7-35	A/D Multiplexer Trigger Adjustment
7-36	Resolver Simulator Adjustments

7-11. PANEL AND SWITCH DESIGNATIONS.

7-12. The following abbreviations are used in the Panel column of the figures in this section:

Abbreviation	Panel
PC	POWER CONTROL
IM	INTERFACE MONITORING
MT	MANUAL TEST
ST	SELF TEST
DAI	DATA ADAPTER INTERFACE
ADC	A/D Converter
ADM	A/D Multiplexer

• 7-13. The following are the switches that cannot be located by the usual (panel, area, and switch name) method:

Switch Name	Panel	Location
Power Error-RESET	PC	Adjacent to D A SEQ ERROR
DST/HLT-RESET	PC	Adjacent to HLT
TRANSIENT SUPPRESSION-RESET or DATA ADAPTER TELEMETRY-RESET	MT	Adjacent to blank button in ERROR INDICATION area
Timing Error-RESET	MT	Adjacent to DA VS SLAVE lamps
Self Test	ST	Unmarked rotary switch below MANUAL D A POWER CONTROL

7-14. LAMP INDICATIONS.

7-15. Whenever the POWER SUPPLY ERROR switch is pressed, only the following lamps should be lit: (This lamp display is referred to in the calibration procedures as the normal lamp display.)

Panel	Lamps Lit
PC	CHANNEL SELECT-TMR
PC	SEQ OFF
PC	SIG GRD
PC	+28VDC
PC	DC ON
PC	ETS-ϕA, ϕB, ϕC and FAN
PC	LVDA ME-ϕA, ϕB, ϕC and FAN
IM	TMR
MT	COMPUTER-NORMAL
MT	DATA ADAPTER-NORMAL

NOTE

OUTPUT REGISTERS-COMD, ADDRESS REGISTER-COMMAND or REPEAT lamps may or may not be lit.

7-16. Generally, lamps not specifically called out in the procedures should be ignored. However, if a red lamp lights and the procedure does not call for it to be lit, a failure has occurred and troubleshooting is in order.

7-17. If a lamp specified to light in the calibration procedures does not light, the lamps test for the corresponding panel should be performed. (Refer to figure 7-2.)

7-18. INITIAL SWITCH POSITIONS.

7-19. Before starting any of the procedures in this section, rotary and toggle switches should be set as follows:

Panel	Switch	Position
PC	A/D CONVERTER MODE	AUTO
PC	D A POWER SUPPLY	1
PC	PHASE	NONE

Panel	Switch	Position
PC	BIT GATE	NONE
PC	CLOCK	NONE
IM	OUTPUT REGISTERS Selector	OFF
IM	INPUT MULTIPLEXER Selector	OFF
IM	OPERATING MODE	MAN TEST
ST	MANUAL D A POWER CONTROL	NORMAL
ST	Self Test	OFF
ST	TEMP TEST	OFF
ST	EXT FREQ/OFF/INT 24VAC	OFF
ST	RESOLVER SIMULATION Selector	OFF
ST	POLARITY	OFF
ST	INTERNAL/OFF/EXTERNAL	OFF
ST	A/D CONVERTER Selector	27-57

7-20. SELF-CHECK CABLE CONNECTIONS.

7-21. The self-check cables shall be connected as shown on Illustration A of figure 7-1.

7-22. POWER-UP PROCEDURE.

7-23. The power-up procedure is given in figure 7-1. This procedure contains many intermediate steps designed to check interlocks and power sequencing. The following procedure is a simplified power-up procedure to be used when a simple calibration procedure is to be performed:

a. Press POWER ON.

b. Verify that the following lamps light:

POWER ON

ETS-ϕA, ϕB, ϕC and FAN

LVDA ME-ϕA, ϕB, ϕC and FAN

DC OFF

c. Press DC ON.

d. Verify that DC ON lights.

7-24. NORMAL POWER-DOWN PROCEDURE.

7-25. The normal power-down procedure is as follows:

a. Press DC OFF.

b. Verify that DC OFF lights.

c. Press POWER OFF.

d. Verify that POWER OFF is the only LVDAME lamp that is lit.

7-26. EMERGENCY POWER-DOWN PROCEDURE.

7-27. To remove all power from the LVDAME, pull either the LVDAME or ETS EMERGENCY PULL switch. No LVDAME lamps will be lit at this time. The EMERGENCY PULL switches are reset by pressing them in. At this time, the POWER OFF lamp will light.

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.0		Power Tests.		
EXP		The following procedure ensures that all LVDAME and ETS interlocks (including the EMERGENCY PULL switches) will remove power from the LVDAME. The power conditions for all subsequent tests are also provided.		
1.1		Verify that cables are connected as shown on illustration A.		
1.2		Verify that shorting cap is connected to ETS 9430 J2.		
1.3		Verify that shorting cap is connected to LVDAME 9420 J24.		
1.4		Connect ETS 3-phase power plug to power source.		
1.5		Connect LVDAME 3-phase power plug to power source.		
1.6	PC	Press EMERGENCY PULL.		
1.7	ETS	Press EMERGENCY PULL.		
1.8		Remove bottom left end panel from LVDAME.		
1.9		Verify that all circuit breakers are set to ON.		
1.10		Record elapsed-time indicator reading.		

A B C D E F G H I J K L M N O P Q R PAGE OF PAGES NUMBER A-

Figure 7-1. Power Checks (Sheet 1 of 12)

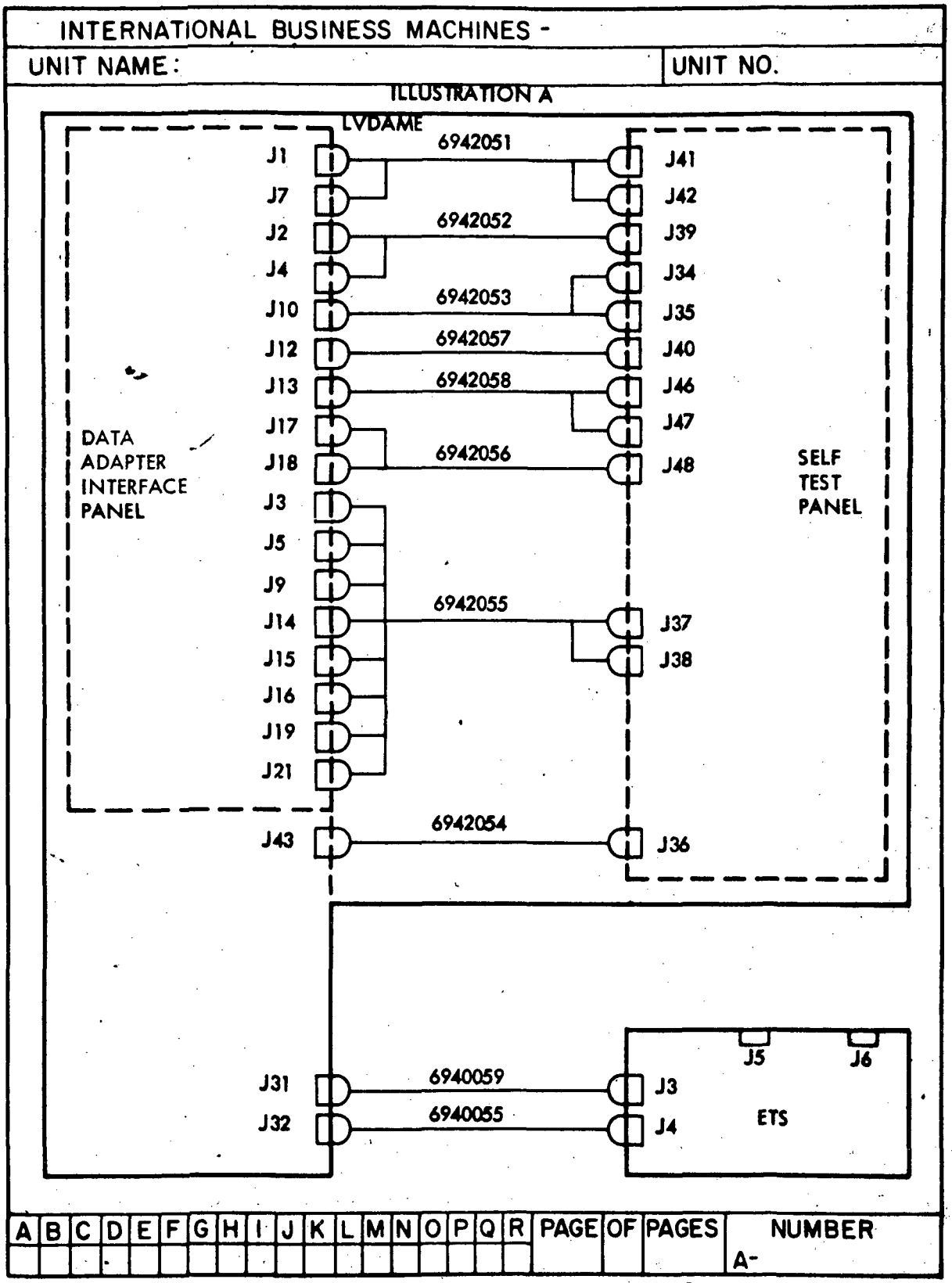


Figure 7-1. Power Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.11		Remove back panel from ETS.		
1.12		Record elapsed time indicator reading.		
1.13		Verify that all circuit breakers are set to ON.		
1.14		Manually close interlock on back of ETS.		
1.15	PC	Observe POWER OFF lamp.	Lit	———
1.16	PC	Press and release POWER ON.		
1.17	PC	Observe following lamps:		
		POWER OFF	Not lit	
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA-ME-ØA, ØB, ØC and FAN	Lit	———
		DC OFF	Lit	———
1.17.1	PC	If LAMP TEST is lit, press and release LAMP TEST.		
1.17.2	PC	Observe LAMP TEST.	Not lit	———
1.18		Observe ETS and LVDAME elapsed time indicators.	Running	———
1.19		Replace bottom left end panel on LVDAME.		

A B C D E F G H I J K L M N O P Q R PAGE ___ OF ___ PAGES NUMBER A-

Figure 7-1. Power Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
1.19.1		Verify that fans at the following locations are running: LVDAME 02A1 02B7 01A6 02A8 02B5 01A7 02A7 01B5 01A8 02B2 01B6 01B1 02B3 01B7 01B2 02B4 01B8 01B3 01B4 Rear of A/D Converter Rear of A/D Multiplexer ETS Three fans to left of 01A4 panel.		
1.20		Manually open interlock on back of ETS.		
1.21		Observe following lamps: POWER OFF all others	 Lit Not lit	 ——— ———
1.22		Replace ETS back panel.		
1.23		Press and release POWER ON.		

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Figure 7-1. Power Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.24		Observe following lamps:		
		POWER OFF	Not lit	———
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		DC OFF	Lit	———
1.25		Open right hand side panel on ETS.		
1.26	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.27		Replace right hand ETS side panel.		
1.29	PC	Press and release POWER ON.		
1.30	PC	Observe following lamps:		
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		POWER OFF	Not lit	———
		DC OFF	Lit	———
1.31		Open left hand ETS side panel.		
1.32	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.33		Replace left hand ETS side panel.		
1.34	PC	Press and release POWER ON.		
1.35	PC	Observe following lamps:		
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		POWER OFF	Not lit	———
		DC OFF	Lit	———

A B C D E F G H I J K L M N O P Q R PAGE OF PAGES NUMBER A-

Figure 7-1. Power Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.36		Open front ETS door.		
1.37	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.38		Close front ETS door.		
1.39		Press and release POWER ON.		
1.40	PC	Observe following lamps:		
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		POWER OFF	Not lit	———
		DC OFF	Lit	———
1.41	PC	Pull EMERGENCY PULL switch.		
1.42		Observe all LVDAME lamps.	None lit	———
1.43	PC	Press in EMERGENCY PULL switch.		
1.44	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.45	PC	Press and release POWER ON.		
1 46	PC	Observe following lamps:		
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		POWER OFF	Not lit	———
		DC OFF	Lit	———
1.47	ETS	Pull EMERGENCY PULL switch.		

A B C D E F G H I J K L M N O P Q R PAGE OF PAGES NUMBER A-

7-1

Figure 7-1. Power Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.48		Observe all LVDAME lamps.	None lit	———
1.49	ETS	Press in EMERGENCY PULL switch.		
1.50	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.51	PC	Press and release POWER ON.		
1.52	PC	Observe following lamps:		
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		POWER OFF	Not lit	———
		DC OFF	Lit	———
1.53		Remove shorting cap from LVDAME 9420 J24.		
1.54		Observe all LVDAME lamps.	None lit	———
1 55		Reconnect shorting cap to LVDAME 9420 J24.		
1.56	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.57	PC	Press and release POWER ON.		
1.58	PC	Observe following lamps:		
		POWER OFF	Not lit	———
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		DC OFF	Lit	———

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Figure 7-1. Power Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.58.1		Remove shorting cap from ETS 9430 J2.		
1.58.2		Observe all LVDAME lamps.	None lit	———
1.58.3		Reconnect shorting cap to ETS 9430 J2.		
1.58.4	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.58.5	PC	Press and release POWER ON.		
1.58.6	PC	Observe following lamps:		
		POWER OFF	Not lit	———
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDAME-ØA, ØB, ØC and FAN	Lit	———
		DC OFF	Lit	———

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Figure 7-1. Power Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.59		Press and release POWER OFF.		
1.60		Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
EXP		The following steps check the voltages at the DC voltage test jacks and ensure that when the 28I, 28D, 6I or -3 volt power supplies are turned off, the corresponding POWER SUPPLY ERROR lamp lights.		
1.61		Press and release POWER ON.		
1.62	PC	Observe following lamps:		
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		POWER OFF	Not lit	———
		DC OFF	Lit	———
1.63	PC	Press and release DC ON.		
1.63.1	PC	Observe following lamps:		
		DC OFF	Not lit	———
		DC ON	Lit	———
EXP		Allow 15 minute warm-up before performing following steps.		

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Figure 7-1. Power Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.64	PC	Using digital voltmeter, measure voltage at each of the following points:	Refer to Operation column.	
		Test Point / Voltage / Tolerance		
		+28DA / +28 V / ±280 mv		———
		+28I / +28 V / ±280 mv		———
		+12 / +12 V / ±120 mv		———
		+6I / +6 V / ±60 mv		———
		-3 / -3 V / ±30 mv		———
		-6 / -6 V / ±60 mv		———
		-12A / -12 V / ±120 mv		———
		-12B / -12 V / ±120 mv		———
		-12C / -12 V / ±120 mv		———
		-26.5 / -26.5 V / ±265 mv		———
		-36 / -36 V / ±360 mv		———
1.65	PC	Press and release POWER OFF.		
1.66	PC	Observe following lamps:		
		POWER OFF	Lit	———
		all others	Not lit	———
1.67		Open ETS front door and manually set interlock.		
1.68	PC	Press and release POWER ON.		
1.69		Observe following lamps:		
		POWER OFF	Not lit	———
		POWER ON	Lit	———
		ETS-ØA, ØB, ØC and FAN	Lit	———
		LVDA ME-ØA, ØB, ØC and FAN	Lit	———
		DC OFF	Lit	———
1.70	PC	Press and release DC ON.		
1.71	PC	Observe following lamps:		
		DC OFF	Not lit	———
		DC ON	Lit	———

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Figure 7-1. Power Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.72	ETS	Set POWER ON switch on topmost ETS power supply (28I supply) to OFF.		
1.73	PC	Observe POWER SUPPLY ERROR -28I.	Lit	———
1.74	ETS	Set POWER ON switch on topmost ETS power supply to ON.		
1.75	PC	Press and release POWER SUPPLY ERROR.		
1.76	PC	Observe POWER SUPPLY ERROR -28I.	Not lit	———
1.77	ETS	Set POWER ON switch on third from top ETS power supply (28D supply) to OFF.		
1.78	PC	Observe POWER SUPPLY ERROR -28D.	Lit	———
1.79	ETS	Set POWER ON switch on third from top ETS power supply to ON.		
1.80	PC	Press and release POWER SUPPLY ERROR.		
1.81	PC	Observe POWER SUPPLY ERROR -28D.	Not lit	———
1.82	ETS	Set POWER ON switch on fourth from top ETS power supply (6I supply) to OFF.		

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Figure 7-1. Power Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.83	PC	Observe POWER SUPPLY ERROR-6I.	Lit	———
1.84	ETS	Set POWER ON switch on fourth from top ETS power supply to ON.		
1.85	PC	Press and release POWER SUPPLY ERROR.		
1.86	PC	Observe POWER SUPPLY ERROR-6I.	Not lit	———
1.87	ETS	Set POWER ON switch on bottom ETS power supply (-3 supply) to OFF.		
1.88	PC	Observe POWER SUPPLY ERROR -3.	Lit	———
1.89	ETS	Set POWER ON switch on bottom ETS power supply to ON.		
1.90	PC	Press and release POWER SUPPLY ERROR.		
1.91	PC	Observe POWER SUPPLY ERROR -3.	Not lit	———

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Figure 7-1. Power Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
2 0		Lamp Test		
Exp		This procedure ensures that the three LAMP TEST pushbuttons can light and extinguish all lamps on their respective panels.		
2 1	PC	Press and release POWER SUPPLY ERROR.		
2 2	IM	Set all OUTPUT REGISTERS-COMD switches to off		
2 3	MT	Set all ADDRESS REGISTER-COMMAND switches to off		
2 4	MT	If REPEAT is lit, press and release REPEAT		
2.5	MT	Observe REPEAT.	Not lit	
		Note At this time only the following lamps will be lit: Panel — Lamps PC CHANNEL SELECT-TMR PC SEQ OFF PC SIG GRD PC +28VDC PC DC ON PC ETS ØA, ØB, ØC and FAN PC LVDAME ØA, ØB, ØC and FAN IM TMR MT COMPUTER-NORMAL MT DATA ADAPTER-NORMAL		

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Figure 7-2. Lamp Tests (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
2.6	PC	Press and release LAMP TEST.		
2 7	PC	Observe all lamps on this panel.	All lit	———
		Note The three RESET buttons and all unetched buttons on this panel are not lamps		
2 8	PC	Press and release LAMP TEST.		
2 9	PC	Observe all lamps on this panel	Refer to Note in step 2 5.	———
2 10	IM	Press and release LAMP TEST.		
2 11	IM	Observe all lamps on this panel	All lit	———
		Note The following buttons on this panel are not lamps: OUTPUT REGISTERS-INSERT OUTPUT REGISTERS-REG RESET INPUT MULTIPLEXER-ALTER INPUT MULTIPLEXER-RESET ERROR DETECTION-RESET ALL UNETCHED BUTTONS		
2.12	IM	Press and release LAMP TEST.		
2 13	IM	Observe all lamps on this panel.	Refer to Note in step 2 5.	———
2 14	MT	Press and release LAMP TEST.		

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Figure 7-2. Lamp Test (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
2 15	MT	Observe all lamps on this panel. Note The ADDRESS REGISTER lamps, REPEAT, COD ENABLE and ENABLE COMPARE are the only lamps in the MANUAL CONTROL area. The two ERROR DETECTION RESETS and all unetched buttons are not lamps	All lit	———
2-16	MT	Press and release LAMP TEST.	Refer to Note in step 2.5.	———

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Figure 7-2. Lamp Test (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
3.0		Discrete Control		
Exp.		This procedure ensures that the +28VDC, +16VDC and +8VDC push-buttons can select +28VDC, 16VDC or +8VDC (respectively) as a discrete supply voltage		
3.1	PC	Press and release POWER SUPPLY ERROR.		
3.2	PC	Connect digital voltmeter between +28I test points		
3.3	PC	Perform tests 1 through 10 of Table I	Refer to Table I	Record data on Table I

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Figure 7-3. Discrete Control Check (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Table I

Test	Press and release	Lamp lit	Lamps not lit	Voltage (VDC)	Data
1	+16VDC	+16VDC	+28VDC and +8VDC	+16(±1)	____
2	+8VDC	+8VDC	+28VDC and +16VDC	+8(±1)	____
3	+16VDC	+16VDC	+28VDC and +8VDC		____
4	+28VDC	+28VDC	+16VDC and +8VDC		____
5	+8VDC	+8VDC	28VDC and +16VDC		____
6	+28VDC	+28VDC	+16VDC and +8VDC		____
7	+8VDC	+8VDC	+28VDC and +16VDC		____
8	POWER SUPPLY ERROR	+28VDC	+16VDC and +8VDC		____
9	+16VDC	+16VDC	+28VDC and +8VDC		____
10	POWER SUPPLY ERROR	+28VDC	+16VDC and +8VDC		____

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Figure 7-3. Discrete Control Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
4.0		LVDA Power Supply.		
Exp.		This procedure ensures that +28V is available at each of twelve LVDA interface points when power tests are not being performed. Voltages are measured by the A/D converter.		
4.1		Disconnect cable 6940036 if connected between ETS 9430 J6 and 9430 J5.		
4.2	PC	Press and release POWER SUPPLY ERROR.		
4.3	ST	Set MANUAL DA POWER CONTROL to CH SW AND PT SWITCH.		
4.4	PC	Set DA POWER SUPPLY to 1.		
4.5	PC	Set A/D CONVERTER MODE to AUTO.		
4.6	ADC	Set TRIGGER to EXT.		
4.7	ADM	Set TRIGGER to EXT.		
4.8	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A8, A6, A5, A2 and A1 to on all others to off.		
4.9	MT	Press and release CIO.		
4.10	ADM	Observe A/D Multiplexer display	26_8	———

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Figure 7-4. LVDA Power Supply Check (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
4.11	ADC	Observe A/D Converter display, and record octal value in Data column.	Greater than 14400_8, less than 15020_8	———
4.12	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A8, A5, A4, A2 and A1 to on all others to off.		
4.13	MT	Press and release CIO.		
4.14	ADM	Observe A/D Multiplexer display.	23_8	———
4.15	ADC	Observe A/D Converter display, and record octal value in Data column.	Greater than 14400_8, less than 15020_8	———
4.16	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A8, A6, A2 and A1 to on all others to off.		
4.17	MT	Press and release CIO.		
4.18	ADM	Observe A/D Multiplexer display.	24_8	———
4.19	ADC	Observe A/D Converter display, and record octal value in Data column.	Greater than 14400_8, less than 15020_8	———

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Figure 7-4. LVDA Power Supply Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
4.20	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A8, A6, A4, A2 and A1 to on all others to off.		
4.21	MT	Press and release CIO.		
4.22	ADM	Observe A/D Multiplexer display.	25_8	———
4.23	ADC	Observe A/D Converter display, and record octal value in Data column.	Greater than 14400_8, less than 15020_8	———
4.24	ST	Set MANUAL DA POWER CONTROL to 5.		
4.25		Connect cable X between ETS 9430-J5 and 9430-J6.		
4.26	ST	Set MANUAL D A POWER CONTROL to CH SW AND PT SWITCH.		
4.27		Repeat steps 4.7 through 4.26, verify that the new octal values in steps 4.11, 4.16, 4.21 and 4.25 do not differ from the first readings by more than 165_8.	Refer to Operation column.	———

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Figure 7-4. LVDA Power Supply Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
4.28	PC	Connect digital voltmeter return (black) lead to test point SP3.		
4.29	PC	Performs tests 1 through 21 of Table I.	Refer to Table I.	Record data on Table I.
4.30		Remove cable 6940036 from ETS 9430 J6 and 9430 J5.		
4.31	PC	Set D A POWER SUPPLY to 1.		
4.32	ST	Set MANUAL D A POWER CONTROL to NORMAL.		

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Figure 7-4. LVDA Power Supply Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: UNIT NO.

Table I

Test	Set DA POWER SUPPLY to	Measure voltage at	Voltage (VDC)	Data
1	1	SP1	+28 (±1)	
2	1	SP2	+28 (±1)	
3	1	SP4	+28 (±1)	
4	2	SP1	+28 (±1)	
5	2	SP2	0 (±1)	
6	2	SP4	+28 (±1)	
7	3	SP1	+28 (±1)	
8	3	SP2	0 (±1)	
9	3	SP4	+28 (±1)	
10	4	SP1	+28 (±1)	
11	4	SP2	+28 (±1)	
12	4	SP4	0 (±1)	
13	5	SP1	+28 (±1)	
14	5	SP2	+28 (±1)	
15	5	SP4	0 (±1)	
16	6	SP1	0 (±1)	
17	6	SP2	+28 (±1)	
18	6	SP4	+28 (±1)	
19	7	SP1	0 (±1)	
20	7	SP2	+28 (±1)	
21	7	SP4	+28 (±1)	

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Figure 7-4. LVDA Power Supply Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.0		LVDA Power Control.		
EXP.		This procedure checks the power control signals (XMEMS, XMEMC and XMEMR) during power-up, power-down and free-run operation.		
5.1	PC	Press and release POWER SUPPLY ERROR.		
5.2	PC	Observe following lamps:		
		INITIAL SEQ	Not lit	_____
		INITIAL ERROR	Not lit	_____
		FULL SEQ	Not lit	_____
		FULL ERROR	Not lit	_____
		SEQ OFF	Lit	_____
		SEQ OFF ERROR	Not lit	_____
5 3	DAI	With oscilloscope, observe signals at following points:		
		Test Point / Signal Name		
		TP27A — XMEMC	0V level	_____
		TP27B — XMEMS	0V level	_____
		TP27C — XMEMR	0V level	_____
		TP27D — HLT X	0V level	_____
5.4	ST	Set MANUAL D A POWER CONTROL rotary switch to FREE RUN.		
5.5	IM	Set OPERATING MODE to MAN TEST.		
5.6	PC	Make sure that D A POWER SUPPLY rotary switch is set to 1		
5.7	PC	Observe following lamps:		
		DA SEQ ERROR-POWER UP	Lit	_____
		DA SEQ ERROR-POWER DOWN	Lit	_____
		HLTX	Flashing on and off	_____
		INITIAL SEQ, FULL ERROR, FULL SEQ and SEQ OFF	Flashing on and off in sequence	_____

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Figure 7-5. LVDA Power Control Check (Sheet 1 of 15)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.8	MT	Sync oscilloscope from TP26; use negative trigger and set time base for 10 MS/CM.		
5.9	DAI	Observe signals at following points:		
		TP27C (XMEMR)	Illustration A	_____
		TP27D (HLTX)	Illustration B	_____
5.10	MT	Sync oscilloscope from TP34; use negative trigger and set time base for 10 MS/CM.		
5.11	DAI	Observe signals at following points:		
		TP27A (XMEMC)	Illustration C	_____
		TP27B (XMEMS)	Illustration D	_____
		TP27D (HLTX)	Illustration E	_____
5.12	ST	Set MANUAL D A POWER CONTROL rotary switch to NORMAL.		
5.13	PC	Press and release POWER SUPPLY ERROR.		
5.14	PC	Press and release INITIAL SEQ.		
5.15	PC	Observe following lamps:		
		INITIAL SEQ	Lit	_____
		SEQ OFF	Not lit	_____
		INITIAL ERROR	Not lit	_____
		HLTX	Lit	_____
5.16	PC	Press and release FULL SEQ.		

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Figure 7-5. LVDA Power Control Check (Sheet 2)

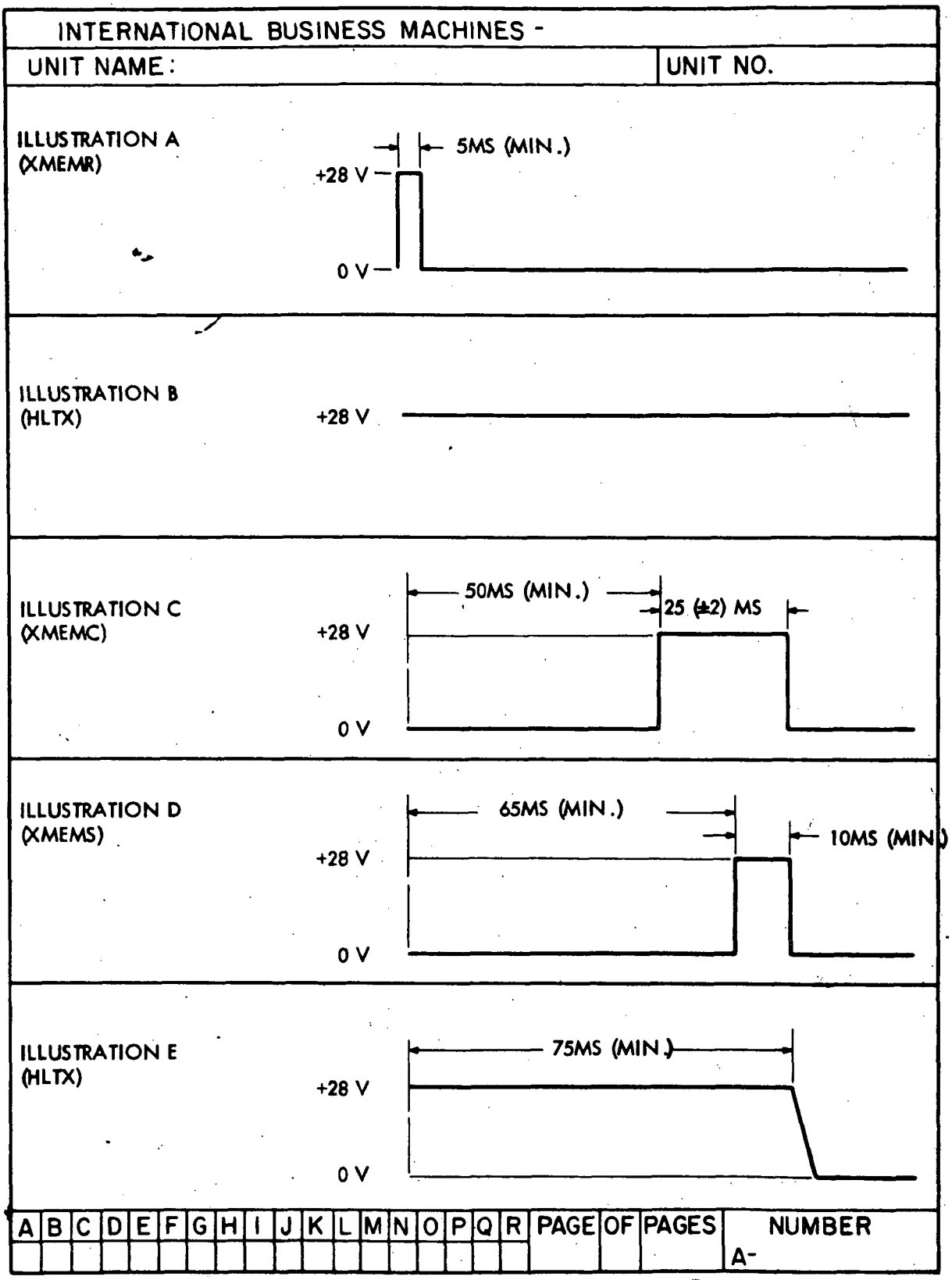

Figure 7-5. LVDA Power Control Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.17	PC	Observe following lamps:		
		FULL ERROR	Lights then goes out	_____
		FULL SEQ	Lit	_____
		INITIAL SEQ	Not lit	_____
		HLTX	Not lit	_____
		DA SEQ ERROR-POWER UP	Lit	_____
5.18	PC	Press and release SEQ OFF.		
5.19	PC	Observe following lamps:		
		HLTX	Lights then goes out	_____
		SEQ OFF	Lit	_____
		FULL SEQ	Not lit	_____
		POWER DOWN	Lit	_____
5.20	DAI	Observe signals at following points: TP27A (XMEMC), TP27B (XMEMS), TP27C (XMEMR) and TP27D (HLTX)	0V levels	_____
5.21	MT	Sync oscilloscope from TP26; use negative trigger and set time base for 1 MS/CM.		
5.22	PC	Press and release INITIAL SEQ while observing signal at TP27C (XMEMR). Press and release SEQ OFF. (Repeat step if necessary.)	Illustration A (whenever INITIAL SEQ is pressed)	_____
5.23	DAI	Observe signal at TP27D (HLTX)	+28V level	_____
5.24	MT	Sync oscilloscope from TP34; use negative trigger and set time base for 10 MS/CM. (Use chopped sweep.)		
5.25	DAI	Connect oscilloscope probes as follows: Probe 1 to TP27A (XMEMC) Probe 2 to TP27B (XMEMS) Probe 3 to TP27D (HLTX)		

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Figure 7-5. LVDA Power Control Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.26	PC	Press and release FULL SEQ while observing oscilloscope display Press and release INITIAL SEQ. (Repeat step if necessary.)	Illustration F (whenever FULL SEQ is pressed)	_____
5.27	MT	Sync oscilloscope from TP27; use negative trigger and set time base for 5 MS/CM. (Use chopped sweep.)		
5.28	DAI	Connect oscilloscope probes as follows: Probe 1 to TP27D (HLTX) Probe 2 to TP27C (XMEMR) Probe 3 to TP33 (DA PW ON)		
5.29	PC	Press and release FULL SEQ; press and release SEQ OFF while observing oscilloscope display. (Repeat step if necessary.)	Illustration G (whenever SEQ OFF is pressed	_____
5.30		Set oscilloscope time base for 50 MS/CM.		
5.31	PC	Press and release FULL SEQ; press and release SEQ OFF while observing signal at TP27D (HLTX). (Repeat step if necessary.)	Illustration H (whenever SEQ OFF is pressed.	_____
5.32	IM	Set OPERATING MODE to ASTEC.		
5.33	PC	Press and release INITIAL SEQ.		
5.34	PC	Observe following lamps:		
		INITIAL SEQ	Lit	_____
		SEQ OFF	Not lit	_____
		FULL SEQ	Not lit	_____
		HLTX	Lit	_____

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Figure 7-5. LVDA Power Control Check (Sheet 5)

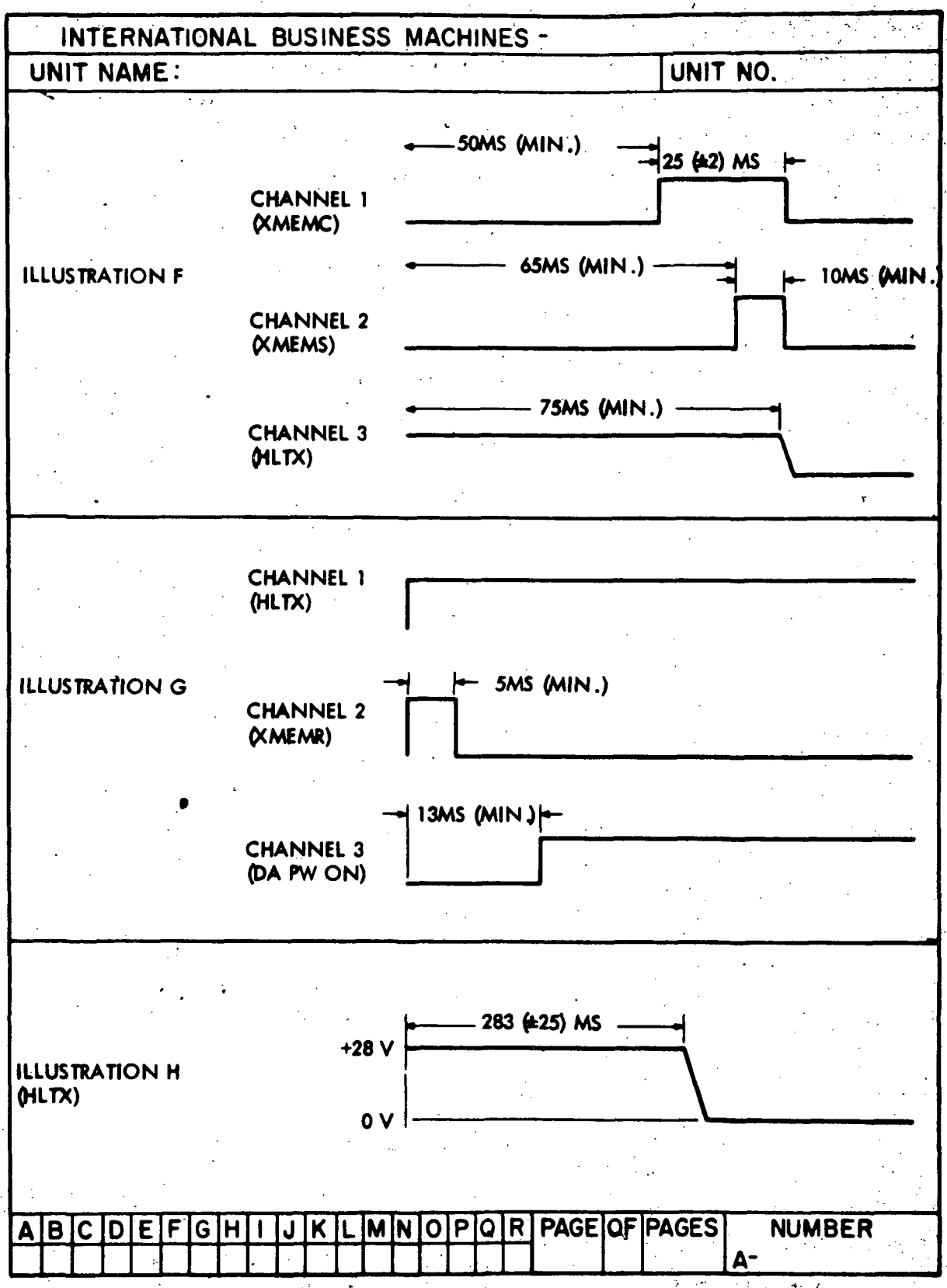

Figure 7-5. LVDA Power Control Check (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.35	PC	Press and release FULL SEQ.		
5.36	PC	Observe following lamps:		
		FULL SEQ	Lit	———
		INITIAL SEQ	Not lit	———
		SEQ OFF	Not lit	———
		HLTX	Not lit	———
5.37	PC	Press and release SEQ OFF.		
5.38	PC	Observe following lamps:		
		HLTX	Lights then goes out	———
		SEQ OFF	Lit	———
5.39	IM	Set OPERATING MODE to ADAPT.		
5.39.1	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	———
5.40	PC	Press and release INITIAL SEQ.		
5.41	PC	Observe HLTX and INITIAL SEQ.	Both lit	———
5.42	IM	Set OPERATING MODE TO MAN TEST.		
5.42.1	PC	Observe ERROR, CHANNEL and MODULE lamps.	None lit	———
EXP		The following steps check the DA SEQ ERROR lamp circuits. Errors are simulated by the MANUAL D A POWER CONTROL rotary switch (referred to as the Self Check switch).		
5.43	PC	Press and release DC OFF.		
5.44	PC	Observe DC OFF.	Lit	———
5.45	PC	Press and release POWER OFF.		

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Figure 7-5. LVDA Power Control Check (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.46	PC	Observe following lamps:		
		DC OFF	Not lit	_____
		POWER OFF	Lit	_____
5.47		Remove paddle card 02B2A02 and reinsert in location 02B2A04.		
5.48		Insert self-test paddle cable between 02B2A02 and 02B2A03.		
5.49	IM	Set OPERATING MODE to ADAPT.		
5.50	ST	Set Self-Check switch to 1.		
5.51	PC	Press and release POWER ON.		
5.52	PC	Observe POWER ON.	Lit	_____
5.53	PC	Press and release DC ON.		
5.54	PC	Observe DC ON.	Lit	_____
5.54.1	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	_____
5.54.2	PC	Press and release POWER SUPPLY ERROR.		
5.54.3	PC	Observe ERROR, CHANNEL and MODULE lamps.	None lit	_____
5.54.4	PC	Press and release FULL SEQ.		
5.55	PC	Observe following lamps:		
		FULL SEQ	Lit	_____
		DA SEQ ERROR-POWER UP	Not lit	_____
		SEQ UP	Not lit	_____
5.56	PC	Press and release SEQ OFF.		
5.57	PC	Observe following lamps:		
		SEQ OFF	Lit	_____
		DA SEQ ERROR-POWER DOWN	Not lit	_____
		POWER DOWN	Lit	_____

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Figure 7-5. LVDA Power Control Check (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP.		The following steps simulate a -3V LVDA power supply error.		
5.58	ST	Set Self-Check switch to 2.		
5.59	PC	Press and release FULL SEQ.		

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Figure 7-5. LVDA Power Control Check (Sheet 9)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.60	PC	Observe following lamps: FULL SEQ DA SEQ ERROR-POWER UP	 Lit Lit	 _____ _____
5.61	PC	Press and release SEQ OFF.		
5.62	PC	Observe following lamps: SEQ OFF	 Lit	 _____
5.63	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps)		
5.64	PC	Observe following lamps: DA SEQ ERROR-POWER UP DA SEQ ERROR-POWER DOWN	 Not lit Not lit	 _____ _____
EXP.		The following steps simulate a +6V LVDA power supply error.		
5.65	ST	Set Self-Check switch to 3.		
5.66	PC	Press and release FULL SEQ.		
5.67	PC	Observe following lamps: FULL SEQ DA SEQ ERROR-POWER UP	 Lit Lit	 _____ _____
5.68	PC	Press and release SEQ OFF.		
5.69	PC	Observe following lamps: SEQ OFF DA SEQ ERROR-POWER DOWN	 Lit Lit	 _____ _____
5.70	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		

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Figure 7-5. LVDA Power Control Check (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.71	PC	Observe following lamps:		
		-DA SEQ ERROR-POWER UP	Not lit	_____
		DA SEQ ERROR-POWER DOWN	Not lit	_____
EXP.		The following steps simulate a +20V LVDA power supply error.		
5.72	ST	Set Self-Check switch to 4.		
5.73	PC	Press and release FULL SEQ.		
5.74	PC	Observe following lamps:		
		FULL SEQ	Lit	_____
		DA SEQ ERROR-POWER UP	Lit	_____
5.75	PC	Press and release SEQ OFF.		
5.76	PC	Observe following lamps:		
		SEQ OFF	Lit	_____
		DA SEQ ERROR-POWER DOWN	Lit	_____
5.77	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		
5.78	PC	Observe following lamps:		
		DA SEQ ERROR-POWER UP	Not lit	_____
		DA SEQ ERROR-POWER DOWN	Not lit	_____
EXP.		The following steps simulate a +12V LVDA power supply error.		
5.79	ST	Set Self-Check switch to 5.		
5.80	PC	Press and release FULL SEQ.		
5.81	PC	Observe following lamps:		
		FULL SEQ	Lit	_____
		DA SEQ ERROR-POWER UP	Lit	_____

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Figure 7-5. LVDA Power Control Check (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.82	PC	Press and release SEQ OFF.		
5.83	PC	Observe following lamps:		
		SEQ OFF	Lit	_____
		DA SEQ ERROR-POWER DOWN	Lit	_____
5.84	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		
5.85	PC	Observe following lamps:		
		DA SEQ ERROR-POWER UP	Not lit	_____
		DA SEQ ERROR-POWER DOWN	Not lit	_____
EXP.		The following steps simulate a +20 memory 1 power supply error.		
5.86	ST	Set Self-Check switch to 6.		
5.87	PC	Press and release FULL SEQ.		
5.88	PC	Observe following lamps:		
		FULL SEQ	Lit	_____
		DA SEQ ERROR-POWER UP	Lit	_____
5.89	PC	Press and release SEQ OFF.		
5.90	PC	Observe following lamps:		
		SEQ OFF	Lit	_____
		DA SEQ ERROR-POWER DOWN	Lit	_____
5.91	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps)		
5.92	PC	Observe following lamps:		
		DA SEQ ERROR-POWER UP	Not lit	_____
		DA SEQ ERROR-POWER DOWN	Not lit	_____
EXP.		The following steps simulate a +20 memory 2 power supply error		

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Figure 7-5. LVDA Power Control Check (Sheet 12)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.93	ST	Set Self-Check switch to 7.		
5.94	PC	Press and release FULL SEQ.		
5.95	PC	Observe following lamps:		
		FULL SEQ	Lit	_____
		DA SEQ ERROR-POWER UP	Lit	_____
5.96	PC	Press and release SEQ OFF.		
5.97	PC	Observe following lamps:		
		SEQ OFF	Lit	_____
		DA SEQ ERROR-POWER DOWN	Lit	_____
5.98	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		
5.99	PC	Observe following lamps:		
		DA SEQ ERROR-POWER UP	Not lit	_____
		DA SEQ ERROR-POWER DOWN	Not lit	_____
EXP.		The following steps simulate a failure in which +20 for MEM 1 comes up too soon and stays up too long.		
5.100	ST	Set Self-Check switch to 8.		
5.101	PC	Press and release FULL SEQ.		
5.102	PC	Observe following lamps:		
		FULL SEQ	Lit	_____
		DA SEQ ERROR-POWER UP	Lit	_____
5.103	PC	Press and release SEQ OFF.		
5.104	PC	Observe following lamps:		
		SEQ OFF	Lit	_____
		DA SEQ ERROR-POWER DOWN	Lit	_____

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Figure 7-5. LVDA Power Control Check (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.105	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		
5.106	PC	Observe following lamps: DA SEQ ERROR-POWER UP DA SEQ ERROR-POWER DOWN	 Not lit Not lit	 _____ _____
EXP		The following steps simulate a failure in which +20V for MEM 2 comes up too soon and stays up too long.		
5.107	ST	Set Self-Check switch to 9.		
5.108	PC	Press and release FULL SEQ.		
5.109	PC	Observe following lamps: FULL SEQ DA SEQ ERROR-POWER UP	 Lit Lit	 _____ _____
5.110	PC	Press and release SEQ OFF.		
5.111	PC	Observe following lamps: SEQ OFF DA SEQ ERROR-POWER DOWN	 Lit Lit	 _____ _____
5.112	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		
5.113	PC	Observe following lamps: DA SEQ ERROR-POWER UP DA SEQ ERROR-POWER DOWN	 Not lit Not lit	 _____ _____
EXP		The following steps simulate the HALTV signal going to 0V.		
5.114	ST	Set Self-Check switch to 10.		

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Figure 7-5. LVDA Power Control Check (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
5.115	PC	Press and release FULL SEQ.		
5.116	PC	Observe following lamps: FULL SEQ DA SEQ ERROR-POWER UP	 Lit Lit	 _____ _____
5.117	PC	Press and release SEQ OFF.		
5.118	PC	Observe following lamps: SEQ OFF DA SEQ ERROR-POWER DOWN	 Lit Lit	 _____ _____
5.119	PC	Press and release RESET (adjacent to POWER UP and POWER DOWN lamps).		
5.120	PC	Observe following lamps: DA SEQ ERROR-POWER UP DA SEQ ERROR-POWER DOWN	 Not lit Not lit	 _____ _____
5.121	IM	Set OPERATING MODE to MAN TEST		
5.122	ST	Set Self-Check switch to OFF.		
5.123	PC	Press and release DC OFF.		
5.124	PC	Press and release POWER OFF.		
5.125		Remove self-test paddle cable from 02B2A02 and 02B2A03.		
5.126		Remove paddle card from 02B2A04, and reinsert at 02B2A02.		
5.127	PC	Press and release POWER ON.		
5.128	PC	Observe POWER ON.	Lit	_____
5.129	PC	Press and release DC ON.		
5.130	PC	Observe DC ON.	Lit	_____

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Figure 7-5. LVDA Power Control Check (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.0		Channel Switching and Power Test		
EXP		This procedure checks the channel switching and power test indicators and the ERROR, CHANNEL and MODULE indicators. Channel switching and power test pulses GCOA through GCOG and GCOR are also checked		
EXP		The following steps check the CHANNEL SELECT indicators		
6.1	DAI	Connect resistors between TP27H and the following test points:		
		Test Point — Resistance (ohms) TP26A (GCOA) — 900 TP26B (GCOB) — 900 TP26C (GCOC) — 900 TP26D (GCOD) — 900 TP26E (GCOE) — 450 TP26F (GCOF) — 900 TP26G (GCOG) — 450 TP26H (GCOR) — 110		
6.2	PC	Press and release POWER SUPPLY ERROR.		
6.3	PC	Perform tests 1 through 20 of Table I.	Refer to Table I.	_____
EXP		The following step checks the POWER SUPPLY AND DISCRETE OUTPUT indicators.		
6.4	PC	Perform tests 1 through 30 of Table II.	Refer to Table II.	_____

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 1 of 19)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

Test	Press and Release CHANNEL SELECT-	CHANNEL SELECT Lamps Lit
1	COMD 1	COMD 1 and CTRL 1
2	COMD 2	COMD 2 and CTRL 2
3	COMD 1	COMD 1 and CTRL 1
4	COMD 3	COMD 3 and CTRL 3
5	COMD 1	COMD 1 and CTRL 1
6	TMR	TMR
7	COMD 1	COMD 1 and CTRL 1
8	COMD 2	COMD 2 and CTRL 2
9	COMD 3	COMD 3 and CTRL 3
10	COMD 2	COMD 2 and CTRL 2
11	TMR	TMR
12	COMD 2	COMD 2 and CTRL 2
13	COMD 3	COMD 3 and CTRL 3
14	TMR	TMR
15	COMD 3	COMD 3 and CTRL 3
16	*POWER SUPPLY ERROR	TMR
17	COMD 1	COMD 1 and CTRL 1
18	*POWER SUPPLY ERROR	TMR
19	COMD 2	COMD 2 and CTRL 2
20	*POWER SUPPLY ERROR	TMR

*Located on PC panel.

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table II

Test	Press and release POWER SUPPLY AND DISCRETE OUTPUT-	POWER SUPPLY AND DISCRETE OUTPUT Lamps Lit
1	COMD 1	COMD 1 and CTRL 1
2	COMD 2	COMD 2 and CTRL 2
3	COMD 1	COMD 1 and CTRL 1
4	COMD 3	COMD 3 and CTRL 3
5	COMD 1	COMD 1 and CTRL 1
6	COMD 4	COMD 4 and CTRL 4
7	COMD 1	COMD 1 and CTRL 1
8	COMD 2	COMD 2 and CTRL 2
9	COMD 3	COMD 3 and CTRL 3
10	COMD 2	COMD 2 and CTRL 2
11	COMD 4	COMD 4 and CTRL 4
12	COMD 2	COMD 2 and CTRL 2
13	COMD 3	COMD 3 and CTRL 3
14	COMD 4	COMD 4 and CTRL 4
15	COMD 3	COMD 3 and CTRL 3
16	*POWER SUPPLY ERROR	none
17	COMD 1	COMD 1 and CTRL 1
18	*POWER SUPPLY ERROR	none
19	COMD 2	COMD 2 and CTRL 2
20	*POWER SUPPLY ERROR	none
21	COMD 4	COMD 4 and CTRL 4
22	*POWER SUPPLY ERROR	none

*Located on PC panel.

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table II (cont.)

Test	Press and release POWER SUPPLY AND DISCRETE OUTPUT-	POWER SUPPLY AND DISCRETE OUTPUT Lamps Lit
23	COMD 1	COMD 1 and CTRL 1
24	RESET	none
25	COMD 2	COMD 2 and CTRL 2
26	RESET	none
27	COMD 3	COMD 3 and CTRL 3
28	RESET	none
29	COMD 4	COMD 4 and CTRL 4
30	RESET	none

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP		The following steps check the characteristics of the channel switching and power test signals (GCOA through GCOG and GCOR).		
6.5	PC	Press and release CHANNEL SELECT COMD 1 while observing signal at TP26H (GCOR)	Illustration A	_____
6.6	PC	Press and release CHANNEL SELECT COMD 1 while observing signal at TP26E (GCOE)	Illustration B	_____
6.7	PC	Press and release CHANNEL SELECT COMD 1 while observing signal at TP26F (GCOF).	Illustration B	_____
6.8	PC	Press and release CHANNEL SELECT COMD 2 while observing signal at TP26E (GCOE)	Illustration B	_____
6.9	PC	Press and release CHANNEL SELECT COMD 2 while observing signal at TP26G (GCOG)	Illustration B	_____
6.10	PC	Press and release CHANNEL SELECT COMD 3 while observing signal at TP26F (GCOF).	Illustration B	_____
6 11	PC	Press and release CHANNEL SELECT COMD 3 while observing signal at TP26G (GCOG).	Illustration B	_____
6 12	PC	Press and release CHANNEL SELECT TMR while observing signal at TP26E (GCOE).	0V level	_____
6 13	PC	Press and release CHANNEL SELECT TMR while observing signal at TP26F (GCOF)	0V level	_____

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.14	PC	Press and release CHANNEL SELECT-TMR while observing signal at TP26G (GCOG).	0V level	_____
6.15	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 1 while observing signal at TP26A (GCOA)	Illustration C	_____
6.16	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 1 while observing signal at TP26B (GCOB)	Illustration C	_____
6.17	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 2 while observing signal at TP26A (GCOA)	Illustration C	_____
6.18	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 2 while observing signal at TP26C (GCOC)	Illustration C	_____
6.19	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 3 while observing signal at TP26B (GCOB)	Illustration C	_____
6.20	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 3 while observing signal at TP26D (GCOD)	Illustration C	_____
6.21	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 4 while observing signal at TP26C (GCOC)	Illustration C	_____

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 6)

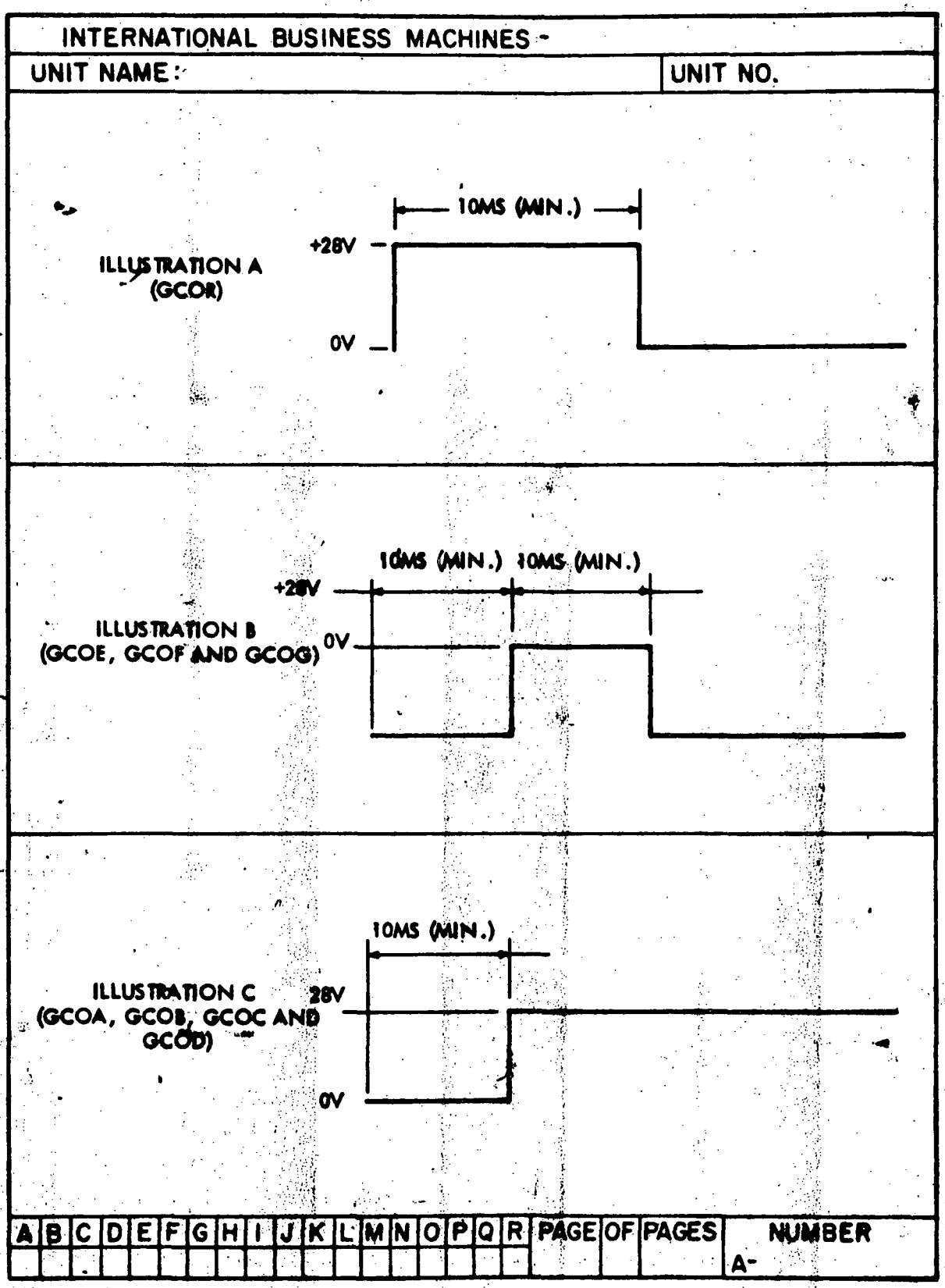

Figure 7-6. Channel Switching and Power Test Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.22	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 4 while observing signal at TP26D (GCOD)	Illustration C	_____
6.23	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-RESET while observing signal at TP26H (GCOR)	Illustration A	_____
EXP		The following steps check the ERROR, CHANNEL and MODULE indicators.		
6.24	PC	Press and release POWER SUPPLY ERROR		
6.25	IM	Set OUTPUT REGISTERS-selector switch to DIN		
6.26	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 to on all others to off		
6.27	IM	Press and release INSERT.		
6.28	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 all others	 Lit Not lit	 _____ _____
6.29	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on all others to off (613)		
6.30	MT	Press and release CIO.		
6.31	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	_____

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.32	PC	Press and release CHANNEL SELECT COMD 1.		
6.32.1	PC	Observe following CHANNEL SELECT lamps: COMD 1 and CTRL 1 all others	 Lit Not lit	 _____ _____
6.32.2		Perform all tests of Table III. (Refer to following explanation.)	Refer to Table III.	_____
EXP.		For each line in Table III, proceed as follows: 1. Load EM REG: a. Set OUTPUT REGISTERS selector switch to EM REG. b. Set OUTPUT REGISTERS-COMD switches as shown in EM REG column. c. Press and release INSERT. 2. Load DIN REG: a. Set OUTPUT REGISTERS selector switch to DIN. b. Set OUTPUT REGISTERS-COMD switches as shown in DIN REG column. c. Press and release INSERT. 3. Observe Displays: a. CHANNEL SELECT lamps b. ERROR lamps c. CHANNEL lamps d. MODULE lamps Note The EM REG and DIN REG bit configurations change only slightly between successive steps. It may not be necessary to load both registers for each step.		

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.32.3	PC	Press and release CHANNEL SELECT-COMD 2.		
6.32.4	PC	Observe following CHANNEL SELECT lamps: COMD 2 and CTRL 2 all others	 Lit Not lit	 _____ _____
6.32.5		Perform all tests of Table IV.	Refer to Table IV.	_____
6.32.6	PC	Press and release CHANNEL SELECT-COMD 3.		
6.32.7	PC	Observe following CHANNEL SELECT lamps: COMD 3 and CTRL 3 all others	 Lit Not lit	 _____ _____
6.32.8		Perform all tests of Table V.	Refer to Table V.	_____
6.32.9	PC	Press and release CHANNEL SELECT-TMR.		
6.32.10	PC	Observe following CHANNEL SELECT lamps: TMR all others	 Lit Not lit	 _____ _____
6.32.11		Perform all tests of Table VI.	Refer to Table VI.	_____
6.33	IM	Press and release OUTPUT REGISTERS-REG RESET.		

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table III

EM REG BITS															DIN REG BITS																									ERROR	CHANNEL	MODULE
S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25			
1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	1	1
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	1	2
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	1	3
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	1	4
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12 VDC	1	5
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	1	6
1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	1	7
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	+6 VDC	1	1
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	+6 VDC	1	2
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	+6 VDC	1	3
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	+6 VDC	1	4
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	+6 VDC	1	5
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	+6 VDC	1	6
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	+6 VDC	1	7
1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	1
1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	2
1	1	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	3
1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	4
1	1	1	1	1	1	1	0	0	1	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	5
1	1	1	1	1	1	1	0	1	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	6
1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	2	7
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	1
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	2
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	3
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	4
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	5
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	6
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	2	7
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	1
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	2
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	3
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	4
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	5
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	6
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12 VDC	3	7
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	1
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	2
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	3
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	4
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	5
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	6
1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6 VDC	3	7

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER
																					A-

Figure 7-6. Channel Switching and Power Test Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table IV

EM REG BITS															DIN REG BITS																									ERROR	CHANNEL	MODULE
S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	1	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	1	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	1	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	1	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	1	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	1	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	+6VDC	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0	+6VDC	1	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	0	+6VDC	1	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	1	1	0	+6VDC	1	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	0	+6VDC	1	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	0	+6VDC	1	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	0	+6VDC	1	7
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	1
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	2
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	3
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	4
1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	5
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	6
1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	2	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	2	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+12VDC	3	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	7

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	PAGE	OF	PAGES	NUMBER
																					A-

Figure 7-6. Channel Switching and Power Test Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table V

EM REG BITS																DIN REG BITS																									ERROR	CHANNEL	MODULE
S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	1	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	+6VDC	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	+6VDC	1	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	+6VDC	1	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0	+6VDC	1	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	+6VDC	1	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	0	1	1	1	1	0	+6VDC	1	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	0	+6VDC	1	7
1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	1
1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	2
1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	3
1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	4
1	1	1	1	1	1	1	1	1	0	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	5
1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	6
1	1	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	2	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	2	7
1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	1
1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	2
1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	3
1	1	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	4
1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	5
1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	6
0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+12VDC	3	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	+6VDC	3	7

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table VI

EM REG BITS																DIN REG BITS																									ERROR	CHANNEL	MODULE
S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25			
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-12VDC	1	2
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-12VDC	1	3
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-12VDC	1	4
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	1	5
1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	1	6
1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-12VDC	1	7
1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	1	1
1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	1	2
1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	1	3
1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	1	4
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	1	5
1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	1	6
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	1	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	2	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-12VDC	2	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	2	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	2	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	2	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	2	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+12VDC	2	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	2	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	2	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	2	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	2	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-6VDC	2	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	2	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	2	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	-12VDC	3	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	+12VDC	3	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	-12VDC	3	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	-12VDC	3	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	+12VDC	3	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	+12VDC	3	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	+12VDC	3	7
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	+6VDC	3	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	+6VDC	3	2
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	+6VDC	3	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	+6VDC	3	4
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	+6VDC	3	5
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	+6VDC	3	6
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	+6VDC	3	7

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.34	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	_____
6.35	IM	Set OPERATING MODE to ADAPT.		
6.36	PC	Observe ERROR, CHANNEL and MODULE lamps	All lit	_____
6.37	IM	Set OPERATING MODE to MAN TEST.		
6.38	PC	Observe ERROR, CHANNEL and MODULE lamps	All lit	_____
6.39	IM	Set OUTPUT REGISTERS selector switch to DIN.		
6.40	IM	Set OUTPUT REGISTERS-COMD switches as follows: 15 to on all others to off		
6.41	IM	Press and release INSERT.		
6.42	IM	Observe following OUTPUT REGISTERS-REG lamps: 15 all others	 Lit Not lit	 _____ _____
6.43	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A2 and A1 to on all others to off		
6.44	MT	Press and release CIO.		
6.45	PC	Observe ERROR, CHANNEL and MODULE lamps.	None lit	_____
6.46	IM	Set OPERATING MODE to ADAPT.		

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.47	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	———
6.48	IM	Set OPERATING MODE to MAN TEST.		
EXP		The following steps ensure that channel switching and power tests are inhibited in the ADAPT mode when the LVDAME is in FULL SEQ. These steps also ensure that channel switching and power tests can be accomplished in other modes.		
6.49	PC	Press and release POWER SUPPLY ERROR.		
6.50	ST	Set Self Test rotary switch to OFF.		
6.51	ST	Set MANUAL D A POWER CONTROL to NORMAL.		
6.52	IM	Set OPERATING MODE to ASTEC.		
6.53	PC	Press and release FULL SEQ.		
6.54	PC	Observe following lamps: FULL SEQ POWER UP	 Lit Lit	 ——— ———
6.55	PC	Observe following CHANNEL SELECT lamps: TMR all others	 Lit Not lit	 ——— ———
6.56	PC	Observe POWER SUPPLY AND DISCRETE OUTPUT lamps.	None lit	———
6.57	PC	Press and release CHANNEL SELECT-COMD 1.		

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.58	PC	Observe following CHANNEL SELECT lamps: TMR all others	 Lit Not lit	 ____ ____
6.59	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 1		
6.60	PC	Observe POWER SUPPLY AND DISCRETE OUTPUT lamps.	None lit	____
6.61	PC	Press and release CHANNEL SELECT-COMD 2.		
6.62	PC	Observe following CHANNEL SELECT lamps: TMR all others	 Lit Not lit	 ____ ____
6.63	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 2.		
6.64	PC	Observe POWER SUPPLY AND DISCRETE OUTPUT lamps	None lit	____
6.65	PC	Press and release CHANNEL SELECT-COMD 3		
6.66	PC	Observe following CHANNEL SELECT lamps: TMR all others	 Lit Not lit	 ____ ____
6.67	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 3.		
6.68	PC	Observe POWER SUPPLY AND DISCRETE OUTPUT lamps.	None lit	____

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 17)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.69	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 4.		
6.70	PC	Observe POWER SUPPLY AND DISCRETE OUTPUT lamps.	None lit	———
6.71	PC	Press and release INITIAL SEQ.		
6.72	PC	Observe INITIAL SEQ and HLTX.	Both lit	———
6.73	PC	Press and release CHANNEL SELECT-COMD 1.		
6.74	PC	Observe following CHANNEL SELECT lamps:		
		CTRL 1 and COMD 1	Lit	———
		all others	Not lit	———
6.75	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 1.		
6.76	PC	Observe following POWER SUPPLY AND DISCRETE OUTPUT lamps.		
		CTRL 1 and COMD 1	Lit	———
		all others	Not lit	———
6.77	IM	Set OPERATING MODE to ADAPT.		
6.77.1	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	———
6.78	PC	Press and release CHANNEL SELECT-COMD 2.		
6.79	PC	Observe following CHANNEL SELECT lamps:		
		CTRL 2 and COMD 2	Lit	———
		all others	Not lit	———
6.80	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 2.		

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 18)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
6.81	PC	Observe following POWER SUPPLY AND DISCRETE OUTPUT lamps.		
		CTRL 2 and COMD 2	Lit	_____
		all others	Not lit	_____
6.82	PC	Press and release FULL SEQ.		
6.83	PC	Observe FULL SEQ.	Lit	_____
		HLTX	Not lit	_____
6.84	PC	Press and release CHANNEL SELECT-COMD 3		
6.85	PC	Observe following CHANNEL SELECT lamps:		
		CTRL 3 and COMD 3	Lit	_____
		all others	Not lit	_____
6.86	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-COMD 3.		
6.87	PC	Observe following POWER SUPPLY AND DISCRETE OUTPUT lamps:		
		CTRL 3 and COMD 3	Lit	_____
		all others	Not lit	_____
6.88	PC	Press and release SEQ OFF.		
6.89	PC	Observe SEQ OFF. and DA SEQ ERROR-POWER DOWN.	Both lit	_____
6.90	IM	Set OPERATING MODE to MAN TEST		

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Figure 7-6. Channel Switching and Power Test Checks (Sheet 19)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
7.0		Telemetry Return.		
EXP		The following procedure ensures that the telemetry return is connected to +8V, ground and -8V when the corresponding TELEMETRY RETURN switch is pressed.		
7.1	PC	Press and release POWER SUPPLY ERROR.		
7.2	DAI	Connect negative lead of digital voltmeter to TP15H; connect positive lead of digital voltmeter to TP14G		
7.3		Disconnect self-test cable from LVDAME 9420J19. Disregard any lighted DATA ADAPTER TELEMETRY lamps.		
7.4		Perform tests 1 and 2 of Table I.	Refer to Table I.	Record data on Table I
7.5		Disconnect digital voltmeter; connect negative lead of digital voltmeter to TP14G; connect positive lead of digital voltmeter to TP15H.		
7.6		Perform test 3 of Table I	Refer to Table I	Record data on Table I.
7.7		Disconnect digital voltmeter.		
7.8		Perform tests 4 through 10 of Table I.	Refer to Table I	Record data on Table I
7.9		Replace cable removed in step 7.3.		

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Figure 7-7. Telemetry Return Check (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

Test	Press and Release	Lamp Lit	Lamps Not Lit	Voltage	Data
1	+8VDC	+8VDC	-8VDC, SIG GRD	+8(.0 8)V	_____
2	SIG GRD	SIG GRD	-8VDC, +8VDC	0(.0 5)V	_____
3	-8VDC	-8VDC	SIG GRD, +8VDC	-8(.0 8)V	_____
4	SIG GRD	SIG GRD	-8VDC, +8VDC		_____
5	+8VDC	+8VDC	-8VDC, SIG GRD		_____
6	-8VDC	-8VDC	SIG GRD, +8VDC		_____
7	+8VDC	+8VDC	-8VDC, SIG GRD		_____
8	POWER SUPPLY ERROR	SIG GRD	-8VDC, +8VDC		_____
9	-8VDC	-8VDC	SIG GRD, +8VDC		_____
10	POWER SUPPLY ERROR	SIG GRD	-8VDC, +8VDC		_____

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Figure 7-7. Telemetry Return Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.0		Timing Tests		
EXP		The following procedures ensure that the slave and master timing generators are operating correctly		
EXP		The following steps check the master clock error indicators.		
8.1	IM	Set OPERATING MODE to SELF TEST.		
8.1.1	MT	Observe DATA COMPARE ERROR.	Lit	
8.2	PC	Press and release POWER SUPPLY ERROR.		
8.3	PC	Set CLOCK switch to NONE		
8.4	MT	Press and release Timing Error RESET switch		
8.5	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Not lit	
8.6	PC	Set CLOCK switch to TEST O-W		
8.7	MT	Observe the following lamps:		
		OVERALL-W	Lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Not lit	
8.8	PC	Set CLOCK switch to TEST O-X		
8.9	MT	Press and release Timing Error RESET switch		

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Figure 7-8. Timing Checks (Sheet 1 of 13)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.10	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Not lit	
8.11	PC	Set CLOCK switch to TEST O-Y.		
8.12	MT	Press and release Timing Error RESET switch.		
8.13	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Lit	
		OVERALL-Z	Not lit	
8.14	PC	Set CLOCK switch to TEST O-Z.		
8.15	MT	Press and release Timing Error RESET switch.		
8.16	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Lit	
8.17	PC	Set CLOCK switch to TEST 1-W.		
8.18	MT	Press and release Timing Error RESET switch.		
8.19	MT	Observe following lamps:		
		OVERALL-W	Lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Not lit	

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Figure 7-8. Timing Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.20	PC	Set CLOCK switch to TEST 1-X.		
8.21	MT	Press and release Timing Error RESET switch.		
8.22	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Not lit	
8.23	PC	Set CLOCK switch to TEST 1-Y.		
8.24	MT	Press and release Timing Error RESET switch.		
8.25	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Lit	
		OVERALL-Z	Not lit	
8.26	PC	Set CLOCK switch to TEST 1-Z		
8.27	MT	Press and release Timing Error RESET switch		
8.28	MT	Observe following lamps:		
		OVERALL-W	Not lit	
		OVERALL-X	Not lit	
		OVERALL-Y	Not lit	
		OVERALL-Z	Lit	
8.29	PC	Set CLOCK switch to NONE.		
8.30	MT	Press and release Timing Error RESET switch		

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Figure 7-8. Timing Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.31	MT	Observe following lamps:		
		OVERALL-W	Not lit	———
		OVERALL-X	Not lit	———
		OVERALL-Y	Not lit	———
		OVERALL-Z	Not lit	———
8.32 thru 8.35		(Deleted)		
8.36	MT	Observe following lamps:		
		INTERNAL-W	Not lit	———
		INTERNAL-X	Not lit	———
		INTERNAL-Y	Not lit	———
		INTERNAL-Z	Not lit	———
		INTERNAL-MISSING	Not lit	———
		INTERNAL-OVERLAP	Not lit	———
		Note In the following step, press and release the Timing Error RESET switch each time the CLOCK switch position is changed.		
8.37		Perform Tests 1 through 8 of Table I.	Refer to Table I.	Record data on Table I.
8.38	PC	Set CLOCK to NONE.		
8.39	MT	Press and release Timing Error RESET switch.		
8.40	MT	Observe all Timing Error lamps.	None lit	———

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Figure 7-8. Timing Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

Test	*CLOCK Switch Position	MASTER CLOCK-INTERNAL						Data
		W	X	Y	Z	MISSING	OVERLAP	
1	TEST O-W	1	0	0	0	1	0	
2	TEST O-X	0	1	0	0	1	0	
3	TEST O-Y	0	0	1	0	1	0	
4	TEST O-Z	0	0	0	1	1	0	
5	TEST 1-W	1	0	0	0	0	1	
6	TEST 1-X	0	1	0	0	0	1	
7	TEST 1-Y	0	0	1	0	0	1	
8	TEST 1-Z	0	0	0	1	0	1	

*After setting CLOCK switch to position indicated, press and release Timing Error RESET switch

Note: "1" indicates that lamp is lit;
"0" indicates that lamp is not lit.

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Figure 7-8. Timing Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP		The following steps check the characteristics of master timing signals that go to the LVDA interface		
8.41		Disconnect self-check cable from 9420 J5. (disregard clock error indications.		
8.42		With oscilloscope, observe signals at test points listed in Table II	Refer to Table II	Record data on Table II.
8.43		Re-connect self-check cable to 9420 J5.		
8.43.1		Press and release Timing Error RESET.		
8.44		With oscilloscope, observe signals at following points:		
		01B4 C22G (-Y FBW)	-Y W clock	
		01B4 C23G (-Y FBX)	-Y X clock	
		01B4 C24P (-Y FBY)	-Y Y clock	
		01B4 C25P (-Y FBZ)	-Y Z clock	
		01B4 C26E (-Y SCFBMCA)	-Y square wave, down W to Y, period 1.95 microseconds.	
		01B4 C26Q (-Y SCFBMCB)	-Y square wave, down X to Z, period 1.95 microseconds	
EXP		The following steps check the slave clock error indicators and the characteristics of the slave clock generator.		

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Figure 7-8. Timing Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table II

Test	Circuit Point	Signal Name	Characteristics
1	01B4 A02D	A1WDA	
2	01B4 A02E	A2WDA	
3	01B4 A02F	A3WDA	
4	01B4 A02G	A1XDA	
5	01B4 A02H	A2XDA	
6	01B4 A02K	A3XDA	
7	01B4 A02L	A1YDA	
8	01B4 A02M	A2YDA	
9	01B4 A02N	A3YDA	
10	01B4 A02P	A1ZDA	
11	01B4 A02Q	A2ZDA	
12	01B4 A02R	A3ZDA	
13	01B4 C21E	MA	
14	01B4 C02A	A1GVN	
15	01B4 C02B	A2GVN	
16	01B4 C02C	A3GVN	
17	01B4 B02A	STADVA	
18	01B4 B02B	STADVB	
19	01B4 B02C	STADVC	
20	01B4 C02D	A1PBVN	
21	01B4 C02E	A2PBVN	
22	01B4 C02F	A3PBVN	

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Figure 7-8. Timing Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.45	PC	Set CLOCK switch to NONE.		
8.46	PC	Press and release POWER SUPPLY ERROR.		
8.47	MT	Observe following lamps:		
		SLAVE CLOCK-W	Not lit	
		SLAVE CLOCK-X	Not lit	
		SLAVE CLOCK-Y	Not lit	
		SLAVE CLOCK-Z	Not lit	
		SLAVE CLOCK-MISSING	Not lit	
		SLAVE CLOCK-OVERLAP	Not lit	
		Note In the following step, press and release the Timing Error RESET switch each time the CLOCK switch position is changed		
8.48		Perform Tests 1 through 8 of Table III	Refer to Table III.	Record data on Table III
8.49	PC	Set CLOCK switch to NONE.		
8.50	PC	Press and release POWER SUPPLY ERROR.		
8.51		With oscilloscope, observe signals at test points listed in Table IV	Refer to Table IV	Record data on Table IV.
EXP		The following steps check the operation of the MASTER VS DA and DA VS SLAVE sync error detectors.		

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Figure 7-8. Timing Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table III

Test	*CLOCK Switch Position	SLAVE CLOCK						Data
		W	X	Y	Z	MISSING	OVERLAP	
1	TEST O-W	1	0	0	0	1	0	
2	TEST O-X	0	1	0	0	1	0	
3	TEST O-Y	0	0	1	0	1	0	
4	TEST O-Z	0	0	0	1	1	0	
5	TEST 1-W	1	0	0	0	0	1	
6	TEST 1-X	0	1	0	0	0	1	
7	TEST 1-Y	0	0	1	0	0	1	
8	TEST 1-Z	0	0	0	1	0	1	

*After setting CLOCK switch to position indicated, press and release Timing Error RESET switch.

Note: "1" indicates that lamp is lit;
"0" indicates that lamp is not lit

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Figure 7-8. Timing Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table IV

Test	Circuit Point	Signal Name	Characteristic	Data
1	01B3 B20B	-Y AD EW	-Y W clock	_____
2	01B3 B20H	-Y AD EX	-Y X clock	_____
3	01B3 B20D	-Y AD EY	-Y Y clock	_____
4	01B3 B20P	-Y AD EZ	-Y Z clock	_____
5	01A2 TP3	-Y TP $\overline{\text{TIME SYNC}}$		

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Figure 7-8. Timing Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.52	PC	Press and release Timing Error RESET switch.		
8.53	MT	Observe following lamps: BSE1, PSE1, ADSE, PSE2 and BSE2.	Not lit	———
8.54	MT	Press and release BSE1/PSE1.		
8.55	MT	Observe following lamps: BSE1	Lit	———
		PSE1	Lit	———
8.56	PC	Press and release Timing Error RESET switch.		
8.57	MT	Observe following lamps: BSE1, PSE1, ADSE, PSE2 and BSE2.	Not lit	———
8.58	MT	Press and release ADSE/PSE2/ BSE2.		
8.59	MT	Observe following lamps: ADSE, PSE2 and BSE2.	Lit	———
8.60	PC	Press and release Timing Error RESET switch.		
8.61	MT	Observe following lamps: BSE1, PSE1, ASDE, PSE2 and BSE2.	Not lit	———
8.62	IM	Set OPERATING MODE to ASTEC.		
8.63	MT	Observe DATA COMPARE ERROR.	Not lit	———
8.64	MT	Press and release BSE1/PSE1.		

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Figure 7-8. Timing Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
8.65	MT	Observe following lamps: BSE1 and PSE1.	Not lit	———
EXP		The following steps check the operation of the timing marker generator.		
8.66		Connect oscilloscope probe to 01B3 D16D (-Y AD timing marker).		
8.67	PC	Sequentially set CLOCK, BIT GATE and PHASE switches as shown in Table I, and observe wave shape displayed on oscilloscope.	Refer to Table V	———
8.68	IM	Set OPERATING MODE to MAN TEST.		

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Figure 7-8. Timing Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table V

Test	CLOCK	BIT GATE	PHASE	Characteristics
1	NONE	NONE	NONE	-6 volt level
2	W	NONE	NONE	-Y delayed W clock
3	X	NONE	NONE	-Y delayed X clock
4	Y	NONE	NONE	-Y delayed Y clock
5	Z	NONE	NONE	-Y delayed Z clock
6	NONE	1	NONE	-Y delayed BG1
7	NONE	2	NONE	-Y delayed BG2
8	NONE	3	NONE	-Y delayed BG3
9	NONE	4	NONE	-Y delayed BG4
10	NONE	5	NONE	-Y delayed BG5
11	NONE	6	NONE	-Y delayed BG6
12	NONE	7	NONE	-Y delayed BG7
13	NONE	8	NONE	-Y delayed BG8
14	NONE	9	NONE	-Y delayed BG9
15	NONE	10	NONE	-Y delayed BG10
16	NONE	11	NONE	-Y delayed BG11
17	NONE	12	NONE	-Y delayed BG12
18	NONE	13	NONE	-Y delayed BG13
19	NONE	14	NONE	-Y delayed BG14
20	NONE	NONE	A	-Y delayed phase A
21	NONE	NONE	B	-Y delayed phase B
22	NONE	NONE	C	-Y delayed phase C

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Figure 7-8. Timing Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
9.0		Data Compare Error.		
EXP		This procedure checks the DATA COMPARE ERROR circuit.		
9.1	PC	Press and release POWER SUPPLY ERROR.		
9.2	MT	If REPEAT is lit, press and release REPEAT.		
9.3	IM	Set OPERATING MODE to ADAPT.		
9.4	MT	If DATA COMPARE ERROR is lit press and release DATA COMPARE ERROR.		
9.5	IM	Set OPERATING MODE to MAN TEST.		
9.6	MT	Press and release REPEAT.		
9.7	MT	Observe REPEAT.	Lit	———
9.8	MT	Press and release PIO.		
9.9	IM	Set OPERATING MODE to ADAPT.		
9.9.1	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	———
9.10	MT	Observe DATA COMPARE ERROR.	Lit	———
9.11	MT	Press and hold DATA COMPARE ERROR.		
9.12	MT	Observe DATA COMPARE ERROR.	Not lit	———
9.13	MT	Release DATA COMPARE ERROR.		

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Figure 7-9. Data Compare Error Check (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
9.14	MT	Observe DATA COMPARE ERROR.	Lit	_____
9.15	IM	Set OPERATING MODE to ASTEC.		
9.16	MT	Observe DATA COMPARE ERROR.	Not lit	_____
9.17	IM	Set OPERATING MODE to SELF TEST.		
9.18	MT	Observe DATA COMPARE ERROR.	Not lit	_____
9.19	IM	Set OPERATING MODE to MAN TEST.		
9.20	MT	Press and release REPEAT.		
9.21	MT	Observe REPEAT.	Not lit	_____
9.22	IM	Set OPERATING MODE to ADAPT.		
9.23	MT	Observe DATA COMPARE ERROR.	Lit	_____
9.24	MT	Press and release DATA COMPARE ERROR.		
9.25	MT	Observe DATA COMPARE ERROR.	Not lit	_____
9.26	IM	Set OPERATING MODE to MAN TEST.		

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Figure 7-9. Data Compare Error Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.0		Output Registers and Input Multiplexer.		
EXP.		The following procedure checks the manual insertion of data into the output registers and the transfer of data from the output registers to the input multiplexer.		
10.1	PC	Press and release POWER SUPPLY ERROR.		
10.2	IM	Set all OUTPUT REGISTERS-COMD switches to off.		
10.3	IM	Load pattern A (table 1) into OUTPUT REGISTERS-COMD register by pressing and releasing switches for which "ones" are shown.		
10.4	IM	Set OUTPUT REGISTERS selector switch to SSFB.		
10.5	IM	Press and release INSERT.		
10.6	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern B	_____
10.7	IM	Set INPUT MULTIPLEXER selector switch to SSFB.		
10.8	IM	Press and release ALTER.		
10.9	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern B	_____
10.10	IM	Press and release OUTPUT REGISTERS-REG RESET.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 1 of 16)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.11	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.12	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.13	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.14	IM	Set OUTPUT REGISTERS selector switch to GC.		
10.15	IM	Press and release INSERT.		
10.16	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern C	_____
10.17	IM	Set INPUT MULTIPLEXER selector switch to GC.		
10.18	IM	Press and release ALTER.		
10.19	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern C	_____
10.20	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.21	IM	Observe INPUT MULTIPLEXER display lamps	Not lit	_____
10.22	IM	Set OUTPUT REGISTERS selector switch to CR.		
10.23	IM	Press and release INSERT.		
10.24	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern D	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.25	IM	Set INPUT MULTIPLEXER selector switch to CR.		
10.26	IM	Press and release ALTER.		
10.27	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern D	_____
10.28	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.29	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.30	IM	Set OUTPUT REGISTERS selector switch to DIN.		
10.31	IM	Press and release INSERT.		
10.32	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern E	_____
10.33	IM	Set INPUT MULTIPLEXER selector switch to DIN.		
10.34	IM	Press and release ALTER.		
10.35	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern E	_____
10.36	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.37	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.38	IM	Press and release INPUT MULTIPLEXER-RESET.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.39	IM	Observe all INPUT MULTIPLEXER display lamps	Not lit	_____
10.40	IM	Set OUTPUT REGISTERS selector switch to DIS.		
10.41	IM	Press and release INSERT.		
10.42	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern F	_____
10.43	IM	Set INPUT MULTIPLEXER selector switch to DIS.		
10.44	IM	Press and release ALTER.		
10.45	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern F	_____
10.46	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.47	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.48	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.49	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.50	IM	Set OUTPUT REGISTERS selector switch to CIU.		
10.51	IM	Press and release INSERT.		
10.52	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern G	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.53	IM	Set INPUT MULTIPLEXER selector switch to CIU.		
10.54	IM	Press and release ALTER.		
10.55	IM	Observe INPUT MULTIPLEXER display lamp.	Pattern G	_____
10.56	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.57	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.58	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.59	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.60	IM	Set OUTPUT REGISTERS selector switch to EMR.		
10.61	IM	Press and release INSERT.		
10.62	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern H	_____
10.63	IM	Set INPUT MULTIPLEXER selector switch to EMR.		
10.64	IM	Press and release ALTER.		
10.65	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern H	_____
10.66	IM	Press and release OUTPUT REGISTERS-REG RESET.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.67	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.68	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.69	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.70	IM	Set OUTPUT REGISTERS selector switch to IR.		
10.71	IM	Press and release INSERT.		
10.72	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern I	_____
10.73	IM	Set INPUT MULTIPLEXER selector switch to IR.		
10.74	IM	Press and release ALTER.		
10.75	IM	Observe INPUT MULTIPLEXER display lamps	Pattern I	_____
10.76	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.77	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.78	IM	Press and release INPUT MULTIPLEXER-RESET.		
10 79	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.80	IM	Set OUTPUT REGISTERS selector switch to ND.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.81	IM	Press and release INSERT.		
10.82	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern J	_____
10.83	IM	Set INPUT MULTIPLEXER selector switch to ND.		
10.84	IM	Press and release ALTER.		
10.85	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern J	
10.86	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.87	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.88	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.89	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.90	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
10.91	IM	Press and release INSERT.		
10.92	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern K	_____
10.93	IM	Set INPUT MULTIPLEXER selector switch to OPTISYN.		
10.94	IM	Press and release ALTER.		
10.95	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern K	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.96	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.97	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	____ ____
10.98	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.99	IM	Observe all INPUT MULTIPLEXER display lamps.	Not lit	____
10 100	IM	Set OUTPUT REGISTERS selector switch to COD.		
10 101	IM	Press and release INSERT.		
10.102	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern L	____
10.103		Press and release OUTPUT REGISTERS-REG RESET.		
10.104		Observe OUTPUT REGISTERS-REG lamps.	Not lit	____
10.105	IM	Load pattern M into OUTPUT REGISTERS-COMD lamp register. Note Pattern M may be loaded by pressing and releasing each OUTPUT REGISTERS-REG/COMD switch		
10.106	IM	Set OUTPUT REGISTERS selector switch to SSFB.		
10.107	IM	Press and release INSERT.		
10.108	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern N	____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.109	IM	Set INPUT MULTIPLEXER selector switch to SSFB.		
10.110	IM	Press and release ALTER.		
10.111	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern N	_____
10.112	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.113	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.114	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.115	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.116	IM	Set OUTPUT REGISTERS selector switch to GC.		
10.117	IM	Press and release INSERT.		
10.118	IM	Observe OUTPUT REGISTER-REG lamps.	Pattern O	_____
10.119	IM	Set INPUT MULTIPLEXER selector switch to GC.		
10.120	IM	Press and release ALTER.		
10.121	IM	INPUT MULTIPLEXER display lamps	Pattern O	_____
10.122	IM	Press and release INPUT MULTIPLEXER-RESET.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.123	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.124	IM	Set OUTPUT REGISTERS selector switch to CR		
10.125	IM	Press and release INSERT.		
10.126	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern P	_____
10.127	IM	Set INPUT MULTIPLEXER selector switch to CR.		
10.128	IM	Press and release ALTER.		_____
10.129	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern P	_____
10.130	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.131	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.132	IM	Set OUTPUT REGISTERS selector switch to DIN.		
10.133	IM	Press and release INSERT.		
10.134	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern Q	_____
10.135	IM	Set INPUT MULTIPLEXER selector switch to DIN.		
10.136	IM	Press and release ALTER.		
10.137	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern Q	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.138	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.139	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.140	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.141	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.142	IM	Set OUTPUT REGISTERS selector switch to DIS.		
10.143	IM	Press and release INSERT.		
10.144	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern R	_____
10.145	IM	Set INPUT MULTIPLEXER selector switch to DIS.		
10.146	IM	Press and release ALTER.		
10.147	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern R	_____
10.148	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.149	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.150	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.151	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.152	IM	Set OUTPUT REGISTERS selector switch to CIU.		
10.153	IM	Press and release INSERT.		
10.154	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern S	_____
10.155	IM	Set INPUT MULTIPLEXER selector switch to CIU.		
10.156	IM	Press and release ALTER.		
10 157	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern S	_____
10.158	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.159	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.160	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.161	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.162	IM	Set OUTPUT REGISTERS selector switch to EMR.		
10 163	IM	Press and release INSERT.		
10.164	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern T	
10 165	IM	Set INPUT MULTIPLEXER selector switch to EMR.		
10 166	IM	Press and release ALTER.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.167	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern T	_____
10.168	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.169	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.170	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.171	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.172	IM	Set OUTPUT REGISTERS selector switch to IR.		
10.173	IM	Press and release INSERT.		
10.174	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern U	_____
10.175	IM	Set INPUT MULTIPLEXER selector switch to IR.		
10.176	IM	Press and release ALTER.		
10.177	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern U	_____
10.178	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.179	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.180	IM	Press and release INPUT MULTIPLEXER-RESET.		

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.181	IM	Observe INPUT MULTIPLEXER display lamps	Not lit	_____
10.182	IM	Set OUTPUT REGISTERS slector switch to ND.		
10.183	IM	Press and release INSERT.		
10.184	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern V	_____
10.185	IM	Set INPUT MULTIPLEXER selector switch to ND.		
10.186	IM	Press and release ALTER.		
10.187	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern V	_____
10.188	IM	Press and release OUTPUT REGISTERS-REG RESET		
10.189	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.190	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.191	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	_____
10.192	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
10.193	IM	Press and release INSERT.		
10.194	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern W	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
10.195	IM	Set INPUT MULTIPLEXER selector switch to OPTISYN.		
10.196	IM	Press and release ALTER.		
10.197	IM	Observe INPUT MULTIPLEXER display lamps.	Pattern W	_____
10.198	IM	Press and release OUTPUT REGISTERS-REG RESET.		
10.199	IM	Observe all OUTPUT REGISTERS-REG lamps.	Not lit	_____
10.200	IM	Press and release INPUT MULTIPLEXER-RESET.		
10.201	IM	Observe all INPUT MULTIPLEXER display lamps.	Not lit	_____
10.202	IM	Set OUTPUT REGISTERS selector switch to COD.		
10.203	IM	Press and release INSERT.		
10.204	IM	Observe OUTPUT REGISTERS-REG lamps.	Pattern X	_____
10.205	IM	Press and release OUTPUT REGISTERS-REG RESET		
10.206	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	_____

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Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 15)

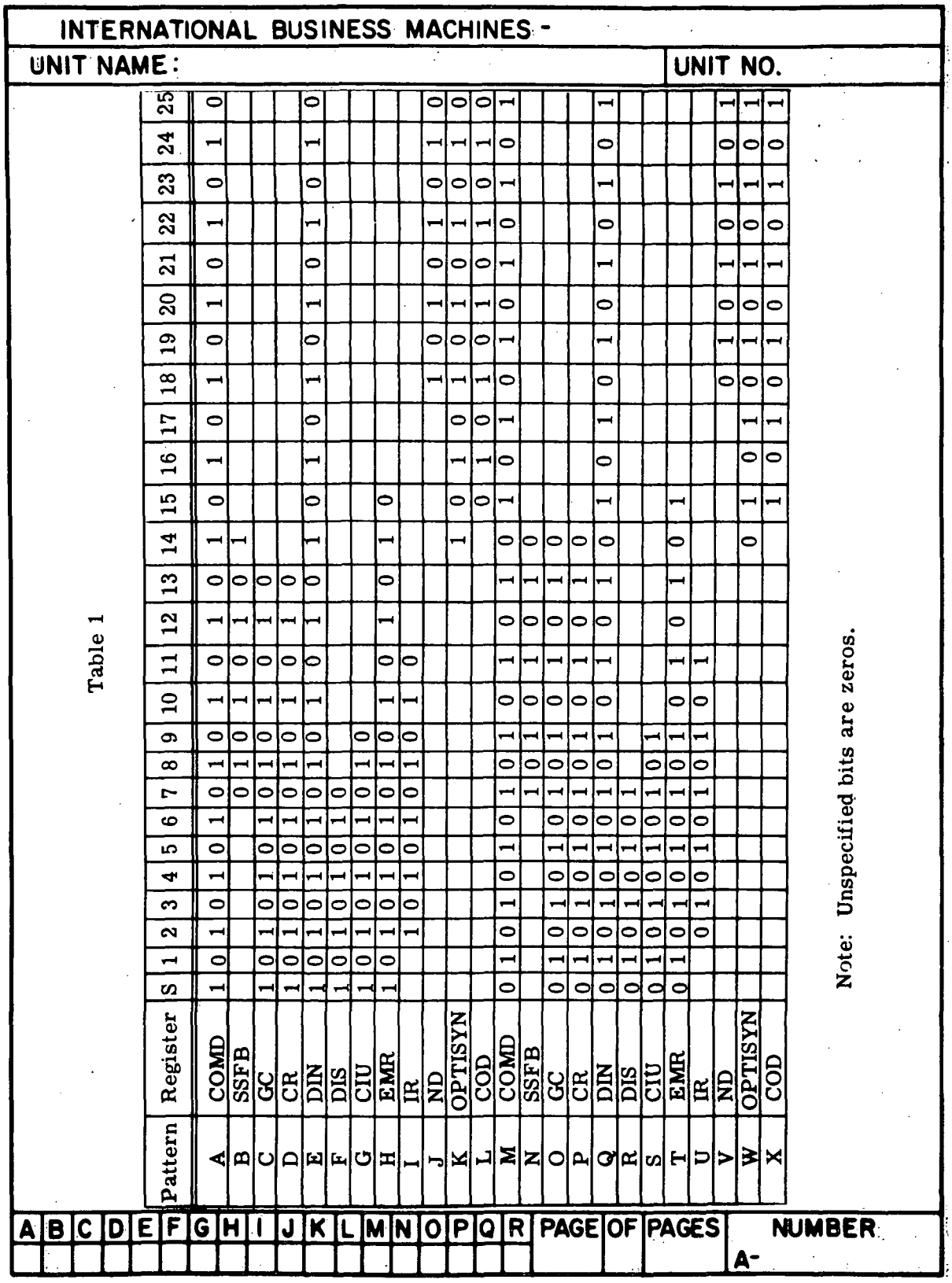

Figure 7-10. Output Registers and Input Multiplexer Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
11.0		COD Serializer		
EXP.		This procedure checks the operation of the COD serializer.		
11.1	PC	Press and release POWER SUPPLY ERROR.		
11.2	MT	With oscilloscope, observe signals at following points: TP69 (TE3A) TP70 (TE3B)	 0V level 0V level	 _____ _____
11.3	IM	Set OUTPUT REGISTERS slector switch to COD.		
11.4	IM	Set OUTPUT REGISTERS-COMD switches as follows: 15, 17, 19, 21, 23 and 25 to on all others to off		
11.5	IM	Press and release INSERT.		
11.6	IM	Observe following OUTPUT REGISTERS-REG lamps: 15, 17, 19, 21, 23 and 25 all others	 Lit Not lit	 _____ _____
EXP.		For all subsequent oscilloscope measurements, sync oscilloscope externally from TP6 (MT panel)		
11.7	PC	Set timing marker PHASE to A, BIT GATE to 1 and CLOCK to NONE.		
11.8	MT	With oscilloscope, observe signal at TP69 (TE3A).	Illustration A	_____

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Figure 7-11. COD Serializer Check (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: . UNIT NO.

Step	Panel	Operation	Normal Indication	Data
11.9	MT	With oscilloscope, observe signal at TP70 (TE3B).	Illustration A	_____
11.10	IM	Set OUTPUT REGISTERS-COMD switches as follows: 16, 18, 20, 22 and 24 to on all others to off		
11.11	IM	Press and release INSERT.		
11.12	IM	Observe following OUTPUT REGISTERS-REG lamps: 16, 18, 20, 22 and 24 all others	 Lit Not lit	 _____ _____
11.13	MT	With oscilloscope, observe signal at TP69 (TE3A).	Illustration B	_____
11.14	MT	With oscilloscope, observe signal at TP70 (TE3B).	Illustration B	_____
11.15	IM	Set OUTPUT REGISTERS-COMD switches as follows: 15 through 25 to on all others to off		
11.16	IM	Press and release INSERT.		
11.17	IM	Observe following OUTPUT REGISTERS-REG lamps: 15 through 25 all others	 Lit Not lit	 _____ _____
11.18	MT	With oscilloscope, observe signal at TP69 (TE3A).	Illustration C	_____
11.19	MT	With oscilloscope, observe signal at TP70 (TE3B)	Illustration C	_____

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Figure 7-11. COD Serializer Check (Sheet 2)

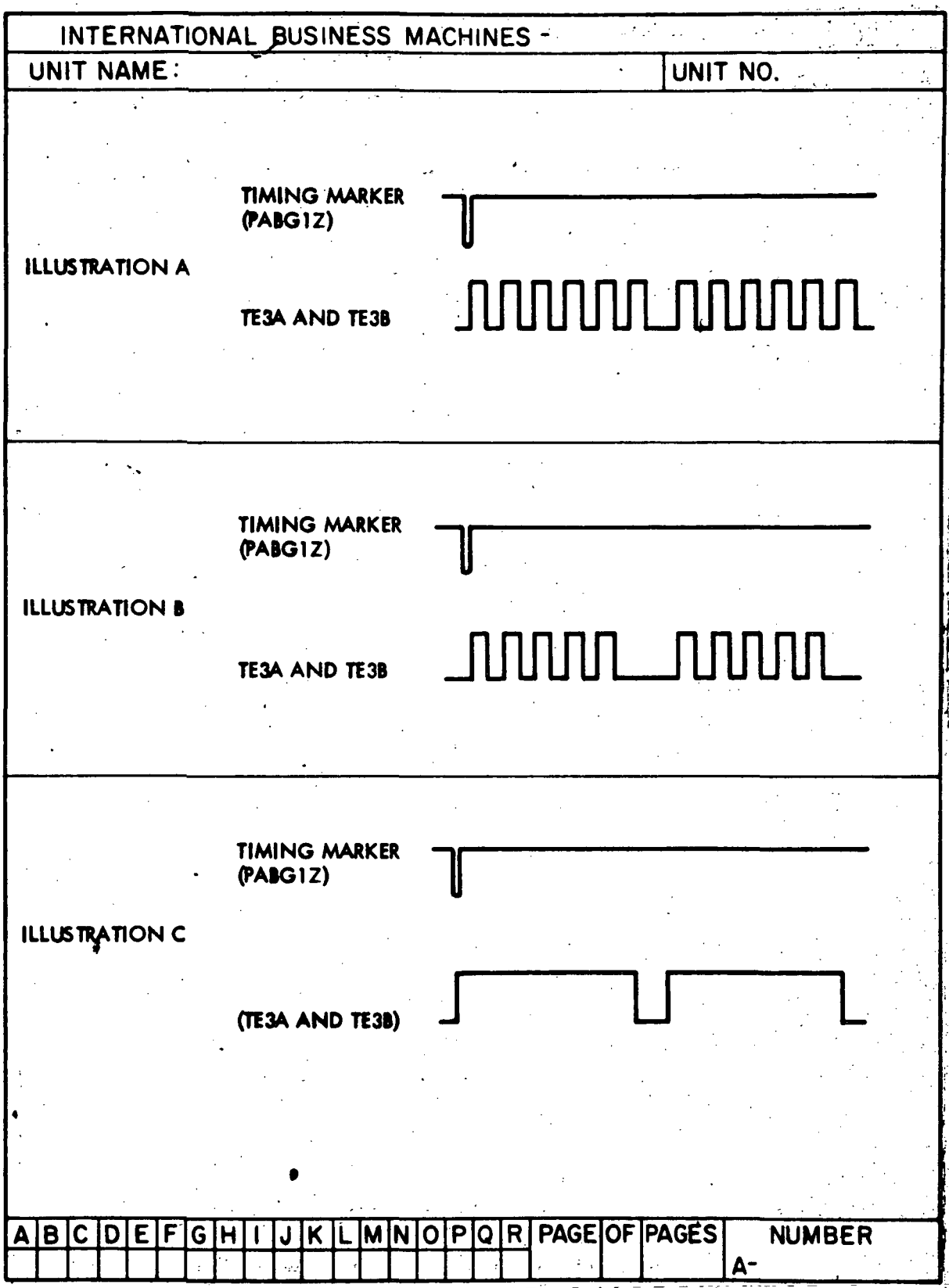

Figure 7-11. COD Serializer Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
12.0		Self-Check Feedback of LVDA Interface Using DIN REGISTER.		
EXP		This procedure checks the insertion of the following types of data into the input multiplexer: GCA, GCB, OC, NA SIM, DOR, SSR, TELA, TELB and CIU. The DIN register is used to feed data back to the interface. The DISCRETE OUTPUT REGISTER display lamps and the D/A MODE REGISTER display lamps are also checked.		
12 1	PC	Press and release POWER SUPPLY ERROR.		
12.2	IM	Set INPUT MULTIPLEXER selector switch to following positions: at each position, press and release ALTER and observe INPUT MULTIPLEXER display lamps:	Display Lamps	
		GCA	Not lit	———
		GCB	Not lit	———
		OC	Not lit	———
		NA SIM	Not lit	———
		DOR	Not lit	———
		SSR	Not lit	———
		TELA	Not lit	———
		TELB	Not lit	———
		CIU	Not lit	———
12.3	IM	Set INPUT MULTIPLEXER selector switch to OFF.		
12.4	IM	Set OUTPUT REGISTERS selector switch to DIN.		
12.5	IM	Set all OUTPUT REGISTERS-COMD switches to "1" (on).		

A | 1 | C | D | E | F | G | H | I | J | K | L | M | N | O | P | Q | R | PAGE | OF | PAGES | NUMBER A-

Figure 7-12. LVDA Interface Feedback Check (Sheet 1 of 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
12.6	IM	Press and release INSERT. (Disregard DISCRETE OUTPUT REGISTER and DA MODE REGISTER lamps that light)		
12.7	IM	Observe OUTPUT REGISTERS-REG lamps.	All lit	———
12.8	IM	Press and release ALTER.		
12.9	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	———
12.10	IM	Press and release OUTPUT REGISTERS-REG RESET.		
12.11	IM	Observe OUTPUT REGISTERS-REG lamps.	Not lit	———
12.12	IM	Set all OUTPUT REGISTERS-COMD switches to "0" (off). Note In the following steps, set and reset the specified bits in the DIN register according to Table I. Set INPUT MULTIPLEXER selector switch to specified positions and verify that the indicated display lamp is lit after pressing and releasing ALTER.		

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Figure 7-12. LVDA Interface Feedback Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
		EXAMPLE To perform Test 2 1. Set COMD-1 to on. 2. Set COMD-S to off. 3. Press and release INSERT. 4. Set INPUT MULTIPLEXER selector switch to following positions and press ALTER. Position — Lamp Lit GCA — 2 GCB — 3 OC — none NA SIM — 4 DOR — 5 SSR — 6 TELA — 7 TELB — 8 *CIU — 9 *Between TELB and SSFB		
12.13		Perform steps 1 through 26 of Table I	Refer to Table I.	———

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Figure 7-12. LVDA Interface Feedback Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

INPUT MULTIPLEXER selector

Test	Set	Reset	GCA	GCB	OC	NA SIM	DOR	SSR	TELA	TELB	CIU	*DOR	*MOD R
1	S	-	1	2		3	4	5	6	7	8	9	4
2	1	S	2	3		4	5	6	7	8	9	8	3
3	2	1	3	4		5	6	7	8	9	10	7	2
4	3	2	4	5		6	7	8	9	10	11	6	1
5	4	3	5	6		7	8	9	10	11	12	5	-
6	5	4	6	7		8	9	10	11	12	13	4	
7	6	5	7	8		9	10	11	12	13	14	3	
8	7	6	8	9		10	11	12	13	14		-	
9	8	7	9	10		11	12	13	14			-	
10	9	8	10	11		12		14	15			-	
11	10	9	11	12		13	14		16			1	
12	11	10	12	13		14			17				
13	12	11	13	14		15			18				
14	13	12	14			16			19				
15	14	13	15			17			20				
16	15	14	16			18			21				
17	16	15	17			19			22				
18	17	16	18			20			23				
19	18	17	19			21			24		S		
20	19	18	20			22			25		1		
21	20	19	21			23			S	1	2		
22	21	20	22			24		S	1	2	3		
23	22	21	23			25	S	1	2	3	4	13	
24	23	22	24		25	S	1	2	3	4	5	12	
25	24	23	25	S		1	2	3	4	5	6	11	6
26	25	24	S	1		2	3	4	5	6	7	10	5

INPUT MULTIPLEXER display lamps

*DISCRETE OUTPUT REGISTER
**D A MODE REGISTER

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Figure 7-12. LVDA Interface Feedback Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
13.0		Multiplexer Serializer and Serial DATAV Input to Multiplexer.		
EXP		This procedure checks the operation of the input multiplexer serializer.		
13.1	PC	Press and release POWER SUPPLY ERROR.		
13.2	IM	Set OUTPUT REGISTERS selector switch to DIN		
13.3	IM	Set INPUT MULTIPLEXER selector switch to DIN.		
13.4	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1 and A2 to on all others to off.		
13.5	IM	Set OUTPUT REGISTERS-COMD switches as follows: S and all even numbered switches to on all odd numbered switches to off.		
13.6	IM	Press and release INSERT.		
13.7	IM	Observe following OUTPUT REGISTERS-REG lamps: S and all even numbered lamps all odd numbered lamps	 Lit Not lit	 _____ _____
13.8	IM	Press and release ALTER.		
13.9	IM	Observe following INPUT MULTIPLEXER display lamps: S and all even numbered lamps all odd numbered lamps	 Lit Not lit	 _____ _____

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Figure 7-13. Multiplexer Serializer Check (Sheet 1 of 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
13.10	MT	Press and release PIO.		
13.11	IM	Observe following INPUT MULTIPLEXER display lamps:		
		S and all even numbered lamps	Not lit	_____
		all odd numbered lamps	Lit	_____
13.12	MT	Press and release PIO.		
13.13	IM	Observe following INPUT MULTIPLEXER display lamps:		
		S and all even numbered lamps	Lit	_____
		all odd numbered lamps	Not lit	_____
13.14	MT	Set ADDRESS REGISTER-COMMAND A8 to on.		
13.15	MT	Press and release PIO.		
13 16	IM	Observe following INPUT MULTIPLEXER display lamps:		
		S and all even numbered lamps	Lit	_____
		all odd numbered lamps	Not lit	_____
13.17	IM	Set all OUTPUT REGISTERS-COMD switches to on.		
13.18	IM	Press and release INSERT.		
13.19	IM	Observe OUTPUT REGISTERS-REG lamps.	All lit	_____
13.20	IM	Press and release ALTER.		
13 21	IM	Observe INPUT MULTIPLEXER display lamps.	All lit	_____
13.22	MT	Set ADDRESS REGISTER-COMMAND A8 to off.		

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Figure 7-13. Multiplexer Serializer Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
13.23	MT	Press and release REPEAT.		
13.24	MT	Observe REPEAT.	Lit	_____
13.25	MT	Press and hold PIO.		
13 26	MT	Observe following ADDRESS REGISTER-FEEDBACK lamps:		
		A1 and A2	Lit	_____
		all others	Not lit	_____
13.27	IM	Observe INPUT MULTIPLEXER display lamps.	Dimly lit	_____
13.28	MT	Release PIO.		
13 29	MT	Press and release REPEAT.		
13.30	MT	Observe following lamps:		
		REPEAT	Not lit	_____
		all ADDRESS REGISTER-FEEDBACK	Not lit	_____
13.31	IM	If INPUT MULTIPLEXER display lamps are not lit, press and release PIO.		
13.32	IM	Observe INPUT MULTIPLEXER display lamps.	All lit	_____
13.33	MT	Set ADDRESS REGISTER-COMMAND switches as follows:		
		A8, A2 and A1 to on		
		all others to off.		

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Figure 7-13. Multiplexer Serializer Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
13.34	MT	Press and release REPEAT.		
13.35	MT	Observe REPEAT.	Lit	———
13.36	MT	Press and release PIO.		
13.37	IM	Observe INPUT MULTIPLEXER display lamps.	All lit	———
13.38	MT	Observe following ADDRESS REGISTER-FEEDBACK lamps: A1, A2 and A8 all others	 Lit Not lit	 ——— ———
EXP.		The following steps check the CIO 005 reset of the input multiplexer.		
13.39	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A3 and A1 to on all others to off		
13.40	MT	Press and release REPEAT.		
13.41	MT	Observe REPEAT.	Not lit	———
13.42	MT	Press and release CIO.		
13.43	IM	Observe INPUT MULTIPLEXER display lamps.	None lit	———

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Figure 7-13. Multiplexer Serializer Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
14.0		Load of EM Register From LDATAV Line.		
EXP.		The following procedure checks the LDATAV serial-to-parallel converter and the EM register.		
14.1	PC	Press and release POWER SUPPLY ERROR.		
14.2	MT	If REPEAT is lit, press and release REPEAT.		
14.3	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A6, A8 and A9 to off all others to "1" on		
14.4	IM	Set OUTPUT REGISTERS selector switch to DIN.		
14.5	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 2, 4, 6, 8 and 10 to on all others to off.		
14.6	IM	Press and release INSERT.		
14.7	IM	Observe following OUTPUT REGISTERS-REG lamps: S, 2, 4, 6, 8 and 10 all others	 Lit Not lit	 _____ _____
14.8	IM	Set INPUT MULTIPLEXER selector switch to DIN.		
14.9	IM	Press and release ALTER.		

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Figure 7-14. Load of EM Register from LDAT AV Line Check (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
14.10	IM	Observe following INPUT MULTIPLEXER display lamps:		
		S, 2, 4, 6, 8 and 10	Lit	_____
		all others	Not lit	_____
14.11	IM	Set OUTPUT REGISTERS selector switch to EMR.		
14.12	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____
14.13	MT	Press and release PIO.		
14.14	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 2, 4, 6, 8 and 10	Lit	_____
		all others	Not lit	_____
14.15	IM	Observe following INPUT MULTIPLEXER display lamps:		
		S, 2, 4, 6, 8 and 10	Not lit	_____
		all others	Lit	_____
14.16	MT	Press and release PIO.		
14.17	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		1, 3, 5, 7, 9 and 11	Lit	_____
		all others	Not lit	_____
14.18	IM	Observe following INPUT MULTIPLEXER display lamps:		
		S, 2, 4, 6, 8 and 10	Lit	_____
		all others	Not lit	_____

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Figure 7-14. Load of EM Register from LDAT AV Line Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
15.0 EXP.		Error Detection. This procedure checks the LVDAME disagreement detectors and indicators.		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 1 of 12)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.1	PC	Press and release POWER SUPPLY ERROR.		
15.2	MT	Set COMMAND-A1 through COMMAND-A9 to "ones".		
15.3	IM	Press and release ACTIVE-$1\bar{2}3$.		
15.4	IM	Observe following lamps:		
		$\bar{1}23$	Lit	_____
		$1\bar{2}3$	Not lit	_____
		$12\bar{3}$	Not lit	_____
15.5	IM	Press and release INACTIVE-0.		
15.5.1	IM	Observe INACTIVE-0.	Lit	_____
15.6	IM	Observe following lamps:		
		AI3-1	Lit	_____
		LDATAV-1	Lit	_____
		ADV-A	Lit	_____
		PBAVN-A	Lit	_____
		G5DVN-A	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15.7	MT	Press and release PIO.		
15.8	IM	Observe following lamps:		
		A1V-1 through A9V-1	Lit	_____
		PIODV-A	Lit	_____
15.9	IM	Press and release ACTIVE-$1\bar{2}3$.		
15.10	IM	Observe following lamps:		
		$\bar{1}23$	Not lit	_____
		$1\bar{2}3$	Lit	_____
		$12\bar{3}$	Not lit	_____

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.11	IM	Observe following lamps:		
		AI3V-2	Lit	_____
		LDATAV-2	Lit	_____
		ADV-B	Lit	_____
		PBAVN-B	Lit	_____
		G5DVN-B	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15.12	MT	Press and release PIO.		
15.13	IM	Observe following lamps:		
		A1V-2 through A9V-2	Lit	_____
		PIODV-B	Lit	_____
15.14	IM	Press and release ACTIVE-12$\bar{3}$.		
15.15	IM	Observe following lamps:		
		1$\bar{2}$3	Not lit	_____
		1$\bar{2}\bar{3}$	Not lit	_____
		12$\bar{3}$	Lit	_____
15.16	IM	Observe following lamps:		
		AI3V-3	Lit	_____
		LDATAV-3	Lit	_____
		ADV-C	Lit	_____
		PBAVN-C	Lit	_____
		G5DVN-C	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15.17	MT	Press and release PIO.		
15.18	IM	Observe following lamps:		
		A1V-3 through A9V-3	Lit	_____
		PIODV-C	Lit	_____
15.19	MT	Set COMMAND-A1 through COMMAND-A9 to "zeros".		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.20	IM	Press and release ACTIVE-$\bar{1}23$.		
15.21	IM	Observe following lamps:		
		$\bar{1}23$	Lit	———
		$1\bar{2}3$	Not lit	———
		$12\bar{3}$	Not lit	———
15.22	IM	Observe following lamps:		
		ADV-A	Lit	———
		PBAVN-A	Lit	———
		AI3-1	Lit	———
		LDATAV-1	Lit	———
		All other ERROR DETECTION	Not lit	———
15.23	MT	Press and release PIO.		
15.24	IM	Observe following lamps:		
		TRSV-1	Lit	———
		DATAV-1	Lit	———
		PIODV-A	Lit	———
15.25	IM	Press and release ACTIVE-$1\bar{2}3$.		
15.26	IM	Observe following lamps:		
		$\bar{1}23$	Not lit	———
		$1\bar{2}3$	Lit	———
		$12\bar{3}$	Not lit	———
15.27	IM	Observe following lamps:		
		ADV-B	Lit	———
		PBAVN-B	Lit	———
		G5DVN-B	Lit	———
		AI3-2	Lit	———
		LDATAV-2	Lit	———
		All other ERROR DETECTION	Not lit	———
15.28	MT	Press and release PIO.		
15.29	IM	Observe following lamps:		
		TRSV-2	Lit	———
		DATAV-2	Lit	———
		PIODV-B	Lit	———

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.30	IM	Press and release ACTIVE-123.		
15.31	IM	Observe following lamps:		
		$\overline{123}$	Not lit	———
		$1\overline{23}$	Not lit	———
		$12\overline{3}$	Lit	———
15.32	IM	Observe following lamps:		
		ADV-C	Lit	———
		PBAVN-C	Lit	———
		G5DVN-C	Lit	———
		AI3-3	Lit	———
		LDATAV-3	Lit	———
		All other ERROR DETECTION	Not lit	———
15.33	MT	Press and release PIO.		
15.34	IM	Observe following lamps:		
		TRSV-3	Lit	———
		DATAV-3	Lit	———
		PIODV-C	Lit	———
15.35	IM	Press and release INACTIVE-1.		
15.36	IM	Observe following lamps:		
		INACTIVE-0	Not lit	———
		INACTIVE-1	Lit	———
15.37	IM	Observe following lamps:		
		AI3V-3	Lit	———
		TRSV-3	Lit	———
		LDATAV-3	Lit	———
		DATAV-3	Lit	———
		PIODV-C	Lit	———
		A1V-3 through A9V-3	Lit	———
		ADV-C	Lit	———
		PBAVN-C	Lit	———
		G5DVN-C	Lit	———
		All other ERROR DETECTION	Not lit	———
15.38	IM	Press and release $\overline{123}$.		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.39	IM	Observe following lamps:		
		$\bar{1}23$	Lit	_____
		$1\bar{2}3$	Not lit	_____
		$12\bar{3}$	Not lit	_____
15.40	IM	Observe following lamps:		
		AI3V-1	Lit	_____
		TRSV-1	Lit	_____
		LDATAV-1	Lit	_____
		DATAV-1	Lit	_____
		PIODV-A	Lit	_____
		A1V-1 through A9V-1	Lit	_____
		ADV-A	Lit	_____
		PBAVN-A	Lit	_____
		G5DVN-A	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15 41	IM	Press and release $1\bar{2}3$.		
15.42	IM	Observe following lamps.		
		$\bar{1}23$	Not lit	_____
		$1\bar{2}3$	Lit	_____
		$12\bar{3}$	Not lit	_____
15.43	IM	Observe following lamps:		
		AI3V-2	Lit	_____
		TRSV-2	Lit	_____
		LDATAV-2	Lit	_____
		DATAV-2	Lit	_____
		PIODV-B	Lit	_____
		A1V-2 through A9V-2	Lit	_____
		ADV-B	Lit	_____
		PBAVN-B	Lit	_____
		G5DVN-B	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15.44	IM	Press and release TMR.		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.45	IM	Observe following lamps:		
		TMR	Lit	_____
		INACTIVE-1	Not lit	_____
		INACTIVE-0	Not lit	_____
		$\overline{1}23$	Not lit	_____
		$1\overline{2}3$	Not lit	_____
		$12\overline{3}$	Not lit	_____
		All ERROR DETECTION	Not lit	_____
15.46	MT	Set address 613 (110 001 011) into ADDRESS REGISTER-COMMAND switches.		
15.47	IM	Set OUTPUT REGISTERS selector switch to DIN.		
15.48	IM	Set COMD-13 to "1" and all other COMD switches to "0".		
15 49	IM	Press and release INSERT.		
15.50	IM	Observe following lamps:		
		REG-13	Lit	_____
		All other REG lamps	Not lit	_____
15.51	MT	Press and release CIO. Observe ERROR, CHANNEL and MODULE lamps.	All lit	_____
15.52	IM	Set OUTPUT REGISTERS selector switch to CIU.		
15.53	IM	Set COMD-3, 6, and 9 to "1"; set COMD-13 to "0".		
15.54	IM	Press and release INSERT.		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.55	IM	Observe following lamps:		
		REG-3	Lit	———
		REG-6	Lit	———
		REG-9	Lit	———
		All other REG lamps	Not lit	———
15.56	IM	Observe following lamps:		
		LINTCV-1	Lit	———
		HALTV-1	Lit	———
		INFOV-1	Lit	———
		PCINFV-A	Lit	———
		INTCV-1	Lit	———
		All other ERROR DETECTION	Not lit	———
15.56.1	DAI	With oscilloscope, observe signal at TP2H.	+6V level	———
15.57	IM	Set COMD-2, 5 and 8 to "1"; Set COMD-3, 6 and 9 to "0".		
15.58	IM	Press and release INSERT.		
15.59	IM	Observe following lamps:		
		REG-2	Lit	———
		REG-5	Lit	———
		REG-8	Lit	———
		All other REG lamps	Not lit	———
15.60	IM	Press and release ERROR DETECTION-RESET.		
15.61	IM	Observe following lamps:		
		LINTCV-2	Lit	———
		HALTV-2	Lit	———
		INFOV-2	Lit	———
		PCINFV-B	Lit	———
		INTCV-2	Lit	———
		All other ERROR DETECTION	Not lit	———
15.61.1	DAI	With oscilloscope, observe signal at TP2H.	0 V level	———
15.62	IM	Set COMD-1, 4 and 7 to "1"; Set COMD-2, 5 and 8 to "0".		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.63	IM	Press and release INSERT.		
15.64	IM	Observe following lamps:		
		REG-1	Lit	_____
		REG-4	Lit	_____
		REG-7	Lit	_____
		All other REG lamps	Not lit	_____
15.65	IM	Press and release ERROR DETECTION-RESET		
15.66	IM	Observe following lamps:		
		LINTCV-3	Lit	_____
		HALTV-3	Lit	_____
		INFOV-3	Lit	_____
		PCINFV-C	Lit	_____
		INTCV-3	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15.67	IM	Set COMD-2, 5 and 8 to "1".		
15.68	IM	Press and release INSERT		
15.69	IM	Observe following lamps:		
		REG-1	Lit	_____
		REG-2	Lit	_____
		REG-4	Lit	_____
		REG-5	Lit	_____
		REG-7	Lit	_____
		REG-8	Lit	_____
		All other REG lamps	Not lit	_____
15.70	IM	Press and release ERROR DETECTION-RESET.		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.71	IM	Observe following lamps:		
		INTCV (above OPERATING MODE SWITCH)	Lit	_____
		LINTCV-1	Lit	_____
		HALTV-1	Lit	_____
		INFOV-1	Lit	_____
		PCINFV-A	Lit	_____
		INTCV-1	Lit	_____
		All other ERROR DETECTION	Not lit	_____
15.71.1	PC	Observe HLT.	Lit	_____
15.72	IM	Set COMD-3, 6 and 9 to "1".		
15.73	IM	Press and release INSERT.		
15.74	IM	Observe following lamps:		
		REG-1 through REG-9	Lit	_____
		All other REG lamps	Not lit	_____
15.75	IM	Press and release ERROR DETECTION-RESET.		
15.76	IM	Observe ERROR DETECTION lamps.	None lit	_____
15.77	IM	Observe INTCV	Lit	_____
15.78	IM	Set COMD-2, 5 and 8 to "0".		
15.79	IM	Press and release INSERT.		
15.80	IM	Observe following lamps:		
		REG-1	Lit	_____
		REG-3	Lit	_____
		REG-4	Lit	_____
		REG-6	Lit	_____
		REG-7	Lit	_____
		REG-9	Lit	_____
		All other REG lamps	Not lit	_____

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 10)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.81	IM	Observe following lamps:		
		INTCV	Lit	———
		LINTCV-2	Lit	———
		HALTV-2	Lit	———
		INFOV-2	Lit	———
		PCINFV-B	Lit	———
		INTCV-2	Lit	———
		All other ERROR DETECTION	Not lit	———
15.81.1	PC	Observe HLT.	Lit	———
15.82	IM	Set COMD-1, 4 and 7 to "0"; Set COMD-2, 5 and 8 to "1".		
15.83	IM	Press and release INSERT.		
15.84	IM	Observe following lamps:		
		REG-2	Lit	———
		REG-3	Lit	———
		REG-5	Lit	———
		REG-6	Lit	———
		REG-8	Lit	———
		REG-9	Lit	———
		All other REG lamps	Not lit	———
15.85	IM	Press and release ERROR DETECTION-RESET.		
15.86	IM	Observe following lamps:		
		INTCV	Lit	———
		LINTCV-3	Lit	———
		HALTV-3	Lit	———
		INFOV-3	Lit	———
		PCINFV-C	Lit	———
		INTCV-3	Lit	———
		All other ERROR DETECTION	Not lit	———
15.86.1	PC	Observe HLT.	Lit	———
15.87	IM	Set COMD-2, 3, 5, 6, 8 and 9 to "0".		

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 11)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
15.88	PC	Press and release POWER SUPPLY ERROR.		
15.89	IM	Observe following lamps:		
		REG lamps	None lit	_____
		ERROR DETECTION lamps	None lit	_____
		INTCV	Not lit	_____
15.90	PC	Observe ERROR, CHANNEL and MODULE lamps.	Not lit	_____

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Figure 7-15. Error Detection and Computer Channel Control Check (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
16.0		Address Register Feedback.		
EXP		The following procedure checks the loading of the address register and the feedback of address bits to the interface.		
16.1	PC	Press and release POWER SUPPLY ERROR.		
16.2	MT	Set ADDRESS REGISTER-COMMAND SWITCHES A1 through A9 to off.		
16.3	MT	Press and release REPEAT.		
16.4	MT	Observe REPEAT.	Lit	———
16.5	MT	Press and release PIO.		
16.6	MT	Sequentially set ADDRESS REGISTER-COMMAND switches A1 through A9 to on and verify that corresponding COMMAND and FEEDBACK lamps light as each switch is pressed	Refer to Operation column.	———
16.7	MT	Press and release REPEAT.		
16.8	MT	Observe REPEAT.	Not lit	———
16.8.1	MT	Observe ADDRESS REGISTER-FEEDBACK lamps.	None lit	———
16.9	IM	Set OUTPUT REGISTERS selector switch to DIN.		
16.10	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1, A2, A8 and A9 to on all others to off		

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Figure 7-16. Address Register Feedback Check (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
16.11	IM	Set OUTPUT REGISTERS-COMD switches as follows: 20, 22 and 24 to "1" (on) all others to "0" (off)		
16.12	IM	Press and release INSERT.		
16.13	IM	Observe following OUTPUT REGISTERS-REG lamps: 20, 22 and 24 all others	 Lit Not lit	 ——— ———
16.14	MT	Press and release CIO.		
16.14.1	IM	Observe following ERROR DETECTION LAMPS: AI3V-1 LDATAV-1 ADV-A PBAVN-A G5DVN-A	 Lit Lit Lit Lit Lit	 ——— ——— ——— ——— ———
16.14.2	IM	Observe following lamps: ACTIVE-123 INACTIVE-0	 Lit Lit	 ——— ———
16.15	MT	Press and release PIO.		
16.16	IM	Observe following ERROR DETECTION lamps: PIODV-A A1V-1 A2V-1 A8V-1 A9V-1	 Lit Lit Lit Lit Lit	 ——— ——— ——— ——— ———
16.17	IM	Set OUTPUT REGISTERS-COMD switches as follows: 23 and 25 to on all others to off		

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Figure 7-16. Address Register Feedback Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
16.18	IM	Press and release INSERT.		
16.19	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		23 and 25	Lit	———
		all others	Not lit	———
16.20	MT	Press and release CIO.		
16.21	IM	Observe ERROR DETECTION lamps.	None lit	———
16.22	IM	Observe COMPUTER-CHANNEL-TMR.	Lit	———

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Figure 7-16. Address Register Feedback Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
17.0		Input Multiplexer Load From Address Register.		
EXP		This procedure checks the address register inputs to the input multiplexer.		
17.1	PC	Press and release POWER SUPPLY ERROR.		
17.2	IM	Set INPUT MULTIPLEXER selector switch to ADDREG.		
17.3	MT	Set all ADDRESS REGISTER-COMMAND switches to "0".		
17.4	IM	Press and release ALTER.		
17.5	IM	Observe INPUT MULTIPLEXER	Not lit	———
17.6	MT	Set COMMAND-A9 to "1".		
17.7	IM	Press and release ALTER.		
17.8	IM	Observe following lamps: INPUT MULTIPLEXER-17 All other INPUT MULTIPLEXER	 Lit Not lit	 ——— ———
17.9	MT	Set COMMAND-A8 to "1".		
17.10	IM	Press and release ALTER.		
17.11	IM	Observe following lamps: INPUT MULTIPLEXER 17 18 All other INPUT MULTIPLEXER	 Lit Lit Not lit	 ——— ———
17.12	MT	Set COMMAND-A7 to "1".		

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Figure 7-17. Input Multiplexer Load from Address Register Check (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
17.13	IM	Press and release ALTER.		
17.14	IM	Observe following lamps: INPUT MULTIPLEXER 17 through 19	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———
17.15	MT	Set COMMAND-A6 to "1".		
17.16	IM	Press and release ALTER.		
17.17	IM	Observe following lamps: INPUT MULTIPLEXER 17 through 20	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———
17.18	MT	Set COMMAND-A5 to "1".		
17.19	IM	Press and release ALTER.		
17.20	IM	Observe following lamps: INPUT MULTIPLEXER 17 through 21	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———
17.21	MT	Set COMMAND-A4 to "1".		
17.22	IM	Press and release ALTER.		
17.23	IM	Observe following lamps: INPUT MULTIPLEXER 17 through 22	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———
17.24	MT	Set COMMAND-A3 to "1".		
17.25	IM	Press and release ALTER.		
17.26	IM	Observe following lamps: INPUT MULTIPLEXER 17 through 23	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———

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Figure 7-17. Input Multiplexer Load from Address Register Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
17.27	MT	Set COMMAND-A2 to "1".		
17.28	IM	Press and release ALTER.		
17.29	IM	Observe following lamps:		
		INPUT MULTIPLEXER 17 through 24	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———
17.30	MT	Set COMMAND-A1 to "1".		
17.31	IM	Press and release ALTER.		
17.32	IM	Observe following lamps:		
		INPUT MULTIPLEXER 17 through 25	Lit	———
		All other INPUT MULTIPLEXER	Not lit	———

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Figure 7-17. Input Multiplexer Load from Address Register Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
18.0		TSYNC, GCSYNCX and ICSN.		
EXP.		This procedure checks the characteristics of the TSYNC, GCSYNCX and ICSN signals.		
18.1	PC	Press and release POWER SUPPLY ERROR.		
18.2	IM	Set all OUTPUT REGISTERS-COMD switches to "0" (off).		
18.3	IM	Set OUTPUT REGISTERS selector switch to CR.		
18.4	IM	Press and release INSERT.		
18.5	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	____
18.6	IM	Set OUTPUT REGISTERS selector switch to DIN.		
18.7	IM	Set OUTPUT REGISTERS-COMD switches as follows: S to "1" (on) all others to "0" (off)		
18.8	IM	Press and release INSERT.		
18.9	IM	Observe following OUTPUT REGISTER-REG lamps: S all others	 Lit Not lit	 ____ ____
18.10	MT	Press and release TEL SAMPLE.		
18.10.1	MT	Press and release RCA SAMPLE.		
18.11	MT	Press and release SAMPLE RESET.		

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Figure 7-18. TSYNC, GCSYNCX and ICSN Checks (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
18.12	DAI	With oscilloscope, observe signal at TP23A (TSYNC).	+6V 192 μs pulse every 4.2 ms.	____
18.13	MT	Press and release TEL SAMPLE.		
18.14	MT	Press and release TEL SAMPLE, and observe signal at TP23A (TSYNC) when TEL SAMPLE is pressed.	+6V 192 μs pulse each time switch is pressed.	____
18.15	DAI	With oscilloscope, observe signals at following points: TP12D (GCSYNCX) TP12E (ICSN)	 0V 0V	 ____ ____
18.16	IM	Set OUTPUT REGISTERS-COMD switches as follows: 1 to "1" (on) all others to "0" (off)		
18.17	IM	Press and release INSERT.		
18.18	IM	Observe following OUTPUT REGISTERS-REG lamps: 1 all others	 Lit Not lit	 ____ ____
18.19	MT	Press and release RCA 110 SAMPLE.		
18.20	MT	Press and release SAMPLE RESET.		
18.21	DAI	With oscilloscope, observe signals at following points: TP23A (TSYNC) TP12D (GCSYNCX)	 0V +28V 192 μs pulse every 4.2 ms.	 ____ ____

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Figure 7-18. TSYNC, GCSYNCX and ICSN Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
18.22	MT	Press and release RCA 110 SAMPLE and observe signal at TP12D (GCSYNCX) when RCA 110 SAMPLE is pressed.	+28V 192 μs pulse each time switch is pressed.	_____
18.23	IM	Set OUTPUT REGISTERS-COMD switches as follows: 3 to "1" (on) all others to "0" (off)		
18.24	IM	Press and release INSERT.		
18.25	IM	Observe following OUTPUT REGISTERS-REG lamps: 3 all others	 Lit Not lit	 _____ _____
18.26	MT	Press and release RCA 110 SAMPLE.		
18.27	DAI	With oscilloscope, observe signals at following points: TP12D (GCSYNCX) TP23A (TSYNC)	 +28V level 0V	 _____ _____
18.28	IM	Press and release OUTPUT REGISTERS-REG RESET.		
18.29	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____
18.30	MT	Press and release RCA 110 SAMPLE.		
18.31	DAI	With oscilloscope, observe signal at TP12D (GCSYNCX)	0V	_____
18.32	IM	Set OUTPUT REGISTERS-COMD switches as follows: 2 to "1" (on) all others to "0" (off)		

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Figure 7-18. TSYNC, GCSYNCX and ICSN Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
18.33	IM	Press and release INSERT.		
18.34	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		2	Lit	_____
		all others	Not lit	_____
18.35	MT	Press and release TEL SAMPLE.		
18.36	DAI	With oscilloscope, observe signals at following points:		
		TP23A (TSYNC)	+6V level	_____
		TP12D (GCSYNCX)	0V	_____
18.37	IM	Set all OUTPUT REGISTERS-COMD switches to "0" (off)		
18.38	IM	Press and release OUTPUT REGISTERS-REG RESET.		
18.39	IM	Observe OUTPUT REGISTERS-REG lamps	None lit	_____
18.40	MT	Press and release TEL SAMPLE.		
18.41	DAI	With oscilloscope, observe signal at TP23A (TSYNC).	0V	
18.42	IM	Set OUTPUT REGISTERS selector switch to GC.		
18.43	IM	Press and release INSERT.		
18.44	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____
18.45	DAI	With oscilloscope, observe signal at TP12E (ICSN)	+28V level	_____
18.46	IM	Set OUTPUT REGISTERS selector switch to CR.		

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Figure 7-18. TSYNC, GCSYNCX and ICSN Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
18.47	IM	Press and release INSERT.		
18.48	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	
18.49	DAI	With oscilloscope, observe signal at TP12E (ICSN).	0V level	

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Figure 7-18. TSYNC, GCSYNCX and ICSN Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
19.0		Enable Compare:		
EXP		The following procedure checks the set and reset conditions for ENABLE COMPARE.		
19.1	PC	Press and release POWER SUPPLY ERROR.		
19.2	MT	Press and release ENABLE COMPARE.		
19.3	IM	Observe ENABLE COMPARE.	Not lit	———
19.4	IM	Set OUTPUT REGISTERS selector switch to DIN.		
19.5	IM	Set COMD switches as follows: S to on All others to off		
19.6	IM	Press and release INSERT.		
19.6.1	IM	Observe following OUTPUT REGISTERS-REG lamps: S All others	 Lit Not lit	 ——— ———
19.7	MT	Press and release ENABLE COMPARE.		
19.8	MT	Observe ENABLE COMPARE.	Lit	———
19.9	IM	Press and release REG RESET.		
19.10	IM	Observe REG-S.	Not lit	———
19.11	MT	Press and release ENABLE COMPARE.		
19.12	MT	Observe ENABLE COMPARE.	Not lit	———

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Figure 7-19. Enable Compare Check (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
19.13	IM	Press and release INSERT.		
19.14	IM	Observe REG-S	Lit	———
19.15	MT	Press and release ENABLE COMPARE.		
19.16	MT	Observe ENABLE COMPARE.	Lit	———
19.17	PC	Press and release POWER SUPPLY ERROR.		
19.18	MT	Observe ENABLE COMPARE.	Not lit	———
19.19	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	———

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Figure 7-19. Enable Compare Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
20.0		CST, DST and HLT.		
EXP		This procedure checks the operation of CST, DST and HLT.		
EXP		The following steps ensure that ADAPT mode displays are disabled unless the LVDAME is in DST.		
20.1	IM	Set OPERATING MODE to MAN TEST.		
20.2	PC	Press and release POWER SUPPLY ERROR.		
20.3	MT	With oscilloscope, observe signals at the following points: TP71 (TP DST) TP72 (DST)	 0 V level 0 V level	 ——— ———
20.4	IM	Set OUTPUT REGISTERS selector switch to DIN.		
20.5	IM	Set all OUTPUT REGISTERS-COMD switches to "1" (on).		
20.6	IM	Press and release INSERT.		
20.7	IM	Observe OUTPUT REGISTERS - REG lamps.	Lit	———
20.8	IM	Set INPUT MULTIPLEXER selector switch to DIN.		
20.9	IM	Press and release ALTER.		
20.10	IM	Observe INPUT MULTIPLEXER display lamps.	Lit	———

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Figure 7-20. CST, DST and HLT Checks (Sheet 1 of 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
20.11	IM	Set all OUTPUT REGISTERS-COMD switches to "0" (off).		
20.12	IM	Set OPERATING MODE to ADAPT.		
20.13	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit except +6.	———
20.13.1	MT	Observe DATA COMPARE ERROR.	Lit	———
20.14	IM	Observe following lamps:		
		OUTPUT REGISTERS-REG lamps	Not lit	———
		INPUT MULTIPLEXER display lamps.	Not lit	———
20.15	IM	Press and release INSERT.		
20.16	IM	Press and release ALTER.		
20.17	MT	Press and release SET DA DST.		
20.18	PC	Observe DST.	Lit	———
20.19	IM	Observe following lamps:		
		OUTPUT REGISTERS-REG lamps	Lit	———
		INPUT MULTIPLEXER-display lamps.	Lit	———
20.20	IM	Press and release INSERT.		
20.21	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	———
20.21.1	PC	Observe ERROR +6.	Lit	
20.22	IM	Press and release ALTER.		
20.23	IM	Observe INPUT MULTIPLEXER display lamps.	Not lit	———
20.24	MT	With oscilloscope, observe signals at the following points:		
		TP71 (TP DST)	-6 V (±0.5) V	———
		TP72 (DST)	+6 V (±0.5) V	———

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Figure 7-20. CST, DST and HLT Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP		The following steps ensure that DST cannot be set in ASTEC mode.		
20.25	MT	Press and release RESET DA DST.		
20.26	PC	Observe DST.	Not lit	———
20.27	IM	Set OPERATING MODE to ASTEC.		
20.28	PC	Observe ERROR, CHANNEL and MODULE lamps.	Not lit	———
20.29	MT	Press and release SET DA DST.		
20.30	PC	Observe DST.	Not lit	———
20.31	IM	Set OPERATING MODE to ADAPT.		
20.32	MT	Press and release SET DA DST.		———
20.33	PC	Observe DST.	Lit	
20.34	PC	Observe ERROR, CHANNEL and MODULE lamps.	Lit	———
20.35	MT	Press and release RESET DA DST.		
20.36	PC	Observe DST.	Not lit	———
EXP		The following steps check the HLTX and HLT1 lamps and the HLTX and HLT1 signals to the interface.		
20.37	DAI	Using oscilloscope, observe signal at TP27D (HLT X).	0 V level	———
20.38	MT	Press and release SET DA HLT.		
20.39	PC	Observe HLTX	Lit	———

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Figure 7-20. CST, DST and HLT Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
20.40	MT	Using oscilloscope, observe signal at TP27D (HLT X).	+28 (±0.5) V	———
20.41	MT	Press and release RESET DA HLT.		
20.42	PC	Observe HLTX.	Not lit	———
20.43	PC	Press and release HLTX.		
20.44	PC	Observe HLTX.	Lit	———
20.45	DAI	With oscilloscope, observe signal at TP27G (HLT 1).	0 V level	———
20.46	PC	Press and release HLT1.		
20.47	PC	Observe HLT1.	Lit	———
20.48	DAI	With oscilloscope, observe signal at TP27G (HLT 1).	+28 (±0.5) V	———
20.49	PC	Press and release POWER SUPPLY ERROR.		
20.50	PC	Observe following lamps: HLTX HLT1	 Not lit Not lit	 ——— ———
20.51	IM	Set OPERATING MODE to MAN TEST.		
20.51.1	PC	Observe ERROR, CHANNEL and MODULE lamps.	None lit	———
EXP		The following steps check the HALTV interface lines, the HLT indicator and the HALTV disagreement error detector.		

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Figure 7-20. CST, DST and HLT Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
20.52	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on A7, A6, A5 and A3 to off		
20.53	IM	Set OUTPUT REGISTERS selector switches to DIN.		
20.54	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 to on all others to off		
20.55	IM	Press and release INSERT.		
20.56	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 all others	 Lit Not lit	 ——— ———
20.57	IM	Set COMD-13 to off.		
20.58	MT	Press CIO.		
20.59	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	———
20.60	IM	Set OUTPUT REGISTERS selector switch to CIU.		
20.61	IM	Set OUTPUT REGISTERS-COMD switches as follows: 1, 2 and 9 to on all others to off		
20.62	IM	Press and release INSERT.		

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Figure 7-20. CST, DST and HLT Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
20.63	IM	Observe following OUTPUT REGISTERS-REG lamps: 1, 2 and 3 all others (Disregard ERROR DETECTION lamps.)	 Lit Not lit	 ——— ———
20.64	PC	Observe HLT.	Lit	———
20.65	IM	Press and release ACTIVE-$\bar{1}$23. (Disregard ERROR DETECTION lamps.)		
20.66	IM	Observe ACTIVE-$\bar{1}$23.	Lit	———
20.67	IM	Press and release INACTIVE-0 if INACTIVE-0 lamp is not lit.		
20.68	IM	Observe INACTIVE-0.	Lit	
20.69	PC	Observe HLT.	Lit	———
20.70	IM	Press and release ACTIVE-1$\bar{2}$3.		
20.71	IM	Observe ACTIVE-1$\bar{2}$3.	Lit	———
20.72	PC	Observe HLT.	Lit	———
20.73	IM	Press and release ACTIVE-12$\bar{3}$.		
20.74	IM	Observe ACTIVE-12$\bar{3}$.	Lit	———
20.75	PC	Observe HLT.	lit	———
EXP.		The following steps ensure that the ASTEC mode inhibits the HLT signal and HLT display.		
20.76	IM	Set OPERATING MODE to ASTEC.		
20.76.1	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	———
20.77	PC	Observe HLT.	Not lit	———

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Figure 7-20. CST, DST and HLT Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
20.78	IM	Set OPERATING MODE to MAN TEST.		
20.79	PC	Observe HLT.	Lit	———
20.79.1	IM	Observe REG-1, 2 and 3.	All lit	———
20.80	IM	Set COMD-3 to off.		
20.81	IM	Press and release INSERT.		
20.82	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		1 and 2	Lit	———
		all others	Not lit	———
20.83	PC	Observe HLT.	Lit	———
20.84	IM	Set COMD-2 to off.		
20.85	IM	Press and release INSERT.		
20.86	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		1	Lit	———
		all others	Not lit	———
20.87	PC	Observe HLT.	Not lit	———

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Figure 7-20. CST, DST and HLT Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
21.0		Manual Test of CIO Codes.		
EXP.		This procedure ensures that the four CIO codes (603, 613, 623 and 633) and the correct data bit/s control the proper LVDAME functions.		
21.1	PC	Press and release POWER SUPPLY ERROR.		
21.2	IM	Set OUTPUT REGISTERS selector switch to DIN.		
21.3	MT	Set all ADDRESS REGISTER-COMMAND switches to off.		
21.4	IM	Set all OUTPUT REGISTERS-COMD switches to on.		
21.5	IM	Press and release INSERT.		
21.6	IM	Observe OUTPUT REGISTERS-REG lamps.	All lit	———
21.7		Observe LVDAME lamps. Note DISCRETE OUTPUT REGISTER lamp 2 is not connected and does not light.	Normal display except that DISCRETE OUTPUT REGISTER and DA MODE REGISTER lamps are lit.	
21.8		Perform tests 1 through 27 of Table I. (Refer to following explanation.)	Refer to Table I.	

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Figure 7-21. CIO Codes Manual Check (Sheet 1 of 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP.		For each test in Table I, proceed as follows: 1. Select CIO Code. a. Set ADDRESS REGISTER-COMMAND switches to octal value of CIO. (A9 is most significant bit.) 2. Load DIN REG. a. Set specified OUTPUT REGISTERS-COMD switches to on, all others to off. b. Press and release INSERT. 3. Press and Release CIO. 4. Observe specified lamps. Note Disregard ERROR DETECTION lamps that light during these tests.		
21.9	MT	Press and release DATA ADAPTER switch.		
21.10	MT	Observe DATA ADAPTER lamp.	Not lit	———
21.11	MT	Press and release LAB TEST EQUIP.		
21.12	MT	Observe LAB TEST EQUIP.	Not lit	———
21.13		Repeat tests 9 and 10 of Table I.	Refer to Table I.	
21.14	PC	Press and release POWER SUPPLY ERROR.		
21.15	MT	Observe DATA ADAPTER lamp.	Not lit	———
21.16	MT	Observe LAB TEST EQUIP.	Not lit	———

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Figure 7-21. CIO Codes Manual Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table I

Test	CIO	OUTPUT REGISTERS-COMD	Lamps Lit
1	603	21, 22 and 24	ACTIVE-$\bar{1}$23 and INACTIVE-1
2		20	ACTIVE-$\bar{1}$23 and INACTIVE-0
3		22 and 25	ACTIVE-1$\bar{2}$3 and INACTIVE-0
4		21	ACTIVE-1$\bar{2}$3 and INACTIVE-1
5		23 and 24	ACTIVE-12$\bar{3}$ and INACTIVE-1
6		20	ACTIVE-12$\bar{3}$ and INACTIVE-0
7		23 and 25	TMR
8		21	TMR
9		19	DATA ADAPTER
10		18	LAB TEST EQUIP
11	613	25	+16VDC
12	623	18	+28VDC
13	613	24	+8VDC (DISCRETE CONTROL)
14	623	17	+28VDC
15	613	23	+8VDC (TELEMETRY BIAS)
16	623	16	SIG GRD
17	613	22	-8VDC
18	623	16	SIG GRD
19	613	17	CHANNEL SELECT-COMD 1 and CTRL 1

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Figure 7-21. CIO Codes Manual Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I (cont.)

Test	CIO	OUTPUT REGISTERS-COMD	Lamps Lit
20	613	16	CHANNEL SELECT-COMD 2 and CTRL 2
21		15	CHANNEL SELECT-COMD 3 and CTRL 3
22		14	CHANNEL SELECT-TMR
23		21	POWER SUPPLY AND DISCRETE OUTPUT-COMD 1 and CTRL 1
24		20	POWER SUPPLY AND DISCRETE OUTPUT-COMD 2 and CTRL 2
25		19	POWER SUPPLY AND DISCRETE OUTPUT-COMD 3 and CTRL 3
26		18	POWER SUPPLY AND DISCRETE OUTPUT-COMD 4 and CTRL 4
27	623	19	*

*At this time none of the lamps listed in this table should be lit.

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Figure 7-21. CIO Codes Manual Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
22.0		Interrupts.		
EXP.		This procedure checks interrupts 1, 2, 3, 4, 6, 9 and 10.		
22.1	PC	Press and release POWER SUPPLY ERROR.		
22.2	MT	With oscilloscope, observe signal at TP7 (INTRPT 1 NOT).	-6(±0.5)V	_____
22.3	IM	Set OUTPUT REGISTERS selector switch to DIN.		
22.4	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 to on all others to off		
22.5	IM	Press and release INSERT.		
22.6	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 all others	 Lit Not lit	 _____ _____
22.7	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1, A2, A4, A8 and A9 to on all others to off.		
22.8	MT	Press and release CIO.		
22.9	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	_____
22.10	MT	With oscilloscope, observe signal at TP7 (INTRPT 1 NOT).	-6(±0.5)V	_____

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Figure 7-22. Interrupt Checks (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
22.11	IM	Set OUTPUT REGISTERS selector switch to CIU.		
22.12	IM	Set OUTPUT REGISTERS-COMD switches as follows: 7, 8, and 9 to on all others to off.		
22.13	IM	Press and release INSERT.		
22.13.1	IM	Press and release ERROR DETECTION-RESET.		
22.14	IM	Observe following lamps: INTCV LINTCV-1, 2 or 3 all other ERROR DETECTION lamps	 Lit May be lit Not lit	 ——— ——— ———
22.15	IM	Observe following OUTPUT REGISTER-REG lamps: 7, 8 and 9 all others	 Lit Not lit	 ——— ———
22.16	MT	With oscilloscope, observe signal at TP7 (INTERRUPT 1 NOT).	0 (±0.5) V	———
22.17	IM	Set OUTPUT REGISTERS-COMD switches as follows: 1 to "1" (on) all others to "0" (off)		
22.18	IM	Press and release INSERT.		
22.18.1	IM	Observe HALTV-3 and PCINFV-C.	Both lit	———
22.19	IM	Observe following OUTPUT REGISTERS-REG lamps: 1 all others	 Lit Not lit	 ——— ———
22.20	MT	With oscilloscope, observe signal at TP7 (INTRPT 1 NOT).	-6 (±0.5) V	———

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Figure 7-22. Interrupt Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
22.21	IM	Observe INTCV.	Not lit	———
22.22	IM	Press and release REG RESET.		
22.22.1	IM	Press and release ERROR DETECTION-RESET.		
22.22.2	IM	Observe ERROR DETECTION LAMPS.	None lit	———
22.23	IM	Set OUTPUT REGISTERS selector switch to ND.		

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Figure 7-22. Interrupt Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
22.24	MT	With oscilloscope, observe signals at the following points:		
		TP9 (INTRPT 3 NOT)	-6(±0.5)V	_____
		TP10 (INTRPT 4 NOT)	-6(±0.5)V	_____
22.25	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		24 and 25 to "1" (on)		
		all others to "0" (off)		
22.26	IM	Press and release INSERT.		
22.27	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		24 and 25	Lit	_____
		all others	Not lit	_____
22.28	MT	With oscilloscope, observe singals at the following points:		
		TP9 (INTRPT 3 NOT)	0(±0.5)V	_____
		TP10 (INTRPT 4 NOT)	0(±0.5)V	_____
22.29	MT	Set ADDRESS REGISTER-COMMAND switches as follows:		
		A2 to "1" (on)		
		all others to "0" (off)		
22.30	MT	Press and release CIO.		
22.31	MT	With oscilloscope, observe signals at the following points:		
		TP8, TP12, TP14, TP15 and TP16	-6(±0.5)V	_____
22.32		Perform Tests 1 through 12 of Table I.	Refer to Table I	Record data on Table I.

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Figure 7-22. Interrupt Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

Test	*ADDRESS REGISTER-COMMAND A9	A8	A7	A6	A5	A4	A3	A2	A1	Test Point	INTRPT	Data
1	X	X	X	X	X	X	X	0	1	TP12	6	
2	X	X	X	X	X	X	X	0	0	TP12	6	
3	X	X	0	0	1	1	1	1	0	TP8	2	
4	X	0	1	0	1	1	1	1	1	TP14	8	
5	X	1	0	0	1	0	0	1	1	TP15	9	
6	X	1	1	1	1	0	0	1	1	TP15	9	
7	X	1	1	1	0	1	0	1	1	TP15	9	
8	X	1	0	0	1	0	1	1	1	TP15	9	
9	X	1	0	1	0	0	0	1	1	TP16	10	
10	X	1	1	1	0	0	0	1	1	TP16	10	
11	X	1	0	0	1	1	0	1	1	TP16	10	
12	X	1	1	0	1	1	0	1	1	TP16	10	

*After setting ADDRESS REGISTER-COMMAND switches, press and release PIO and verify that 0(±0.5) V exists for approximately 68 μs at the specified test point.

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Figure 7-22. Interrupt Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
23.0		COD ENABLE and TE1H.		
EXP.		This procedure checks the COD ENABLE circuit and the INT 14 NOT interface signal.		
23.1		Insert TE1H ODEC card at 01B6A26.		
23.1.1	PC	Press and release POWER SUPPLY ERROR.		
23.2	MT	With oscilloscope, observe signals at following test points: Test Point / Signal TP65 / TE1A TP66 / TE1B TP20 / INT 14 NOT TP68 / TE2B	 +6V level +6V level -6V level 0 V level	 _____ _____ _____ _____
23.3	MT	Press and release COD ENABLE.		
23.4	MT	Observe COD ENABLE.	Lit	_____
23.5	MT	With oscilloscope, observe signals at following test points: TP65 (TE1A) TP66 (TE1B)	 0V level 0V level	 _____ _____
23.6	PC	Set timing marker PHASE to OFF, BIT GATE to OFF and CLOCK to Y.		
23.7	MT	Sync oscilloscope from TP6; use external trigger.		
23.8	MT	Connect oscilloscope probes as follows: Channel 1 to TP6 Channel 2 to TP67		

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Figure 7-23. COD Enable and TE1H Checks (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
23.9		Observe oscilloscope display.	Illustration A	_____
23.10	PC	Set CLOCK to W.		
23.11		Observe oscilloscope display.	Illustration B	_____
23.12	MT	Connect Channel 2 oscilloscope probe to TP68.		
23.13		Observe oscilloscope display	Illustration B	_____
23.14	PC	Set CLOCK to Y.		
23.15		Observe oscilloscope display.	Illustration A	_____
23.16	IM	Set OUTPUT REGISTERS-COMD switches as follows: 12 to on all others to off		
23.17	IM	Set OUTPUT REGISTERS selector switch to DIN.		
23.18	IM	Press and release INSERT.		
23.19	IM	Observe following OUTPUT REGISTERS-REG lamps. 12 all others	 Lit Not lit	 _____ _____
23.20	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on all others to off (613)		
23.21	MT	Press and release CIO.		
23.22	MT	With oscilloscope, observe signal at TP20 (INT 14 NOT).	0V level	_____

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Figure 7-23. COD Enable and TE1H Checks (Sheet 2)

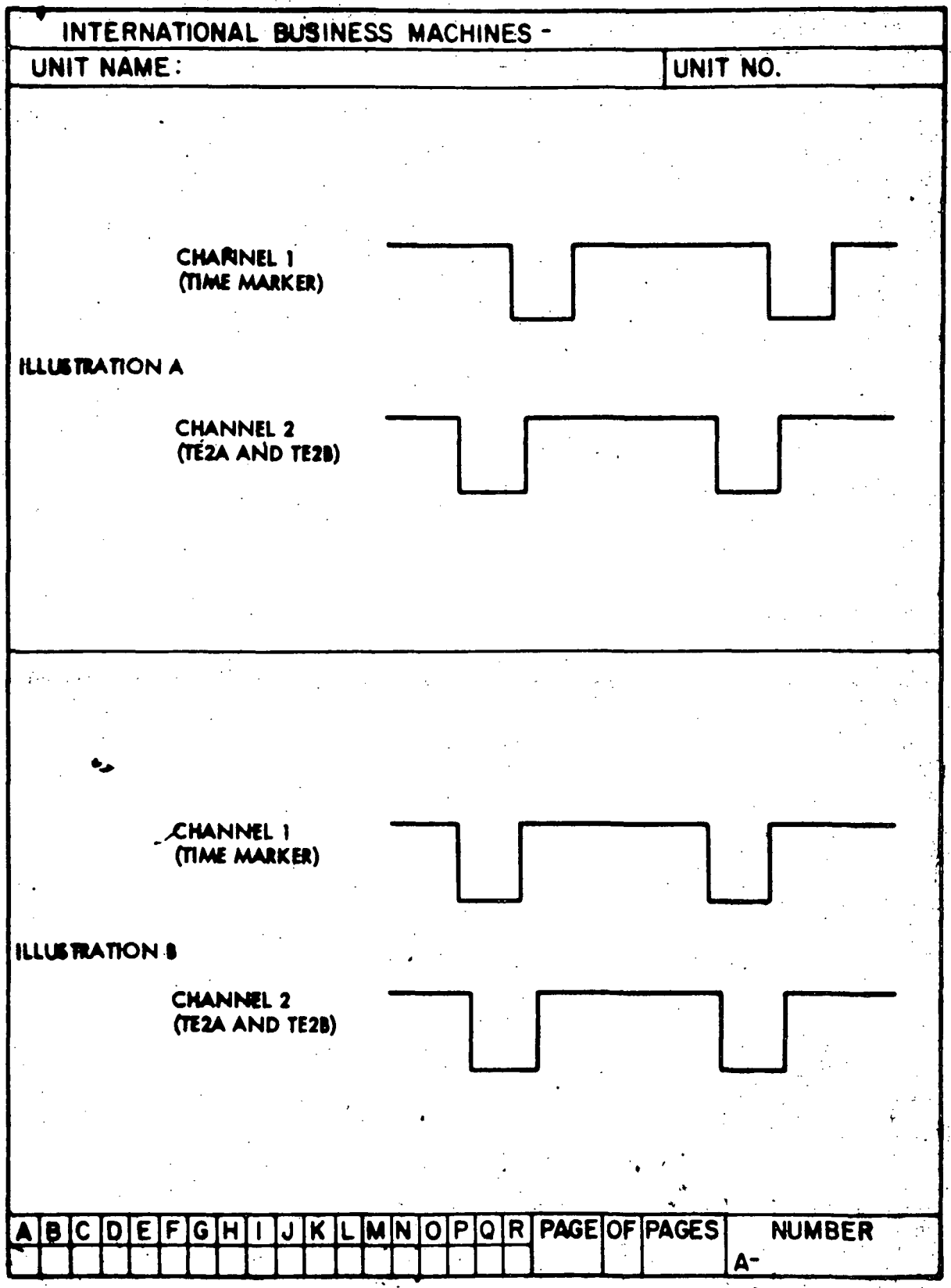

Figure 7-23. COD Enable and TE1H Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
23.23	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 to on all others to off		
23.24	IM	Press and release INSERT.		
23.25	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 all others	 Lit Not lit	 _____ _____
23.26	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A2 and A1 to on all others to off		
23.27	MT	Press and release CIO.		
23 28	MT	With oscilloscope, observe signal at TP20 (INT 14 NOT).	-6V level	_____
23.29	IM	Set OUTPUT REGISTERS-COMD switches as follows: 12 to on all others to off		
23.30	IM	Press and release INSERT.		
23.31	IM	Observe following OUTPUT REGISTERS-REG lamps: 12 all others	 Lit Not lit	 _____ _____
23.32	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on all others to off		

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Figure 7-23. COD Enable and TE1H Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
23.33	MT	Press and release CIO.		
23.34	MT	With oscilloscope, observe signal at TP20 (INT 14 NOT).	0V level	_____
23.35	PC	Press and release POWER SUPPLY ERROR.		
23.36	MT	With oscilloscope observe signal at TP20 (INT 14 NOT).	-6V level	_____

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Figure 7-23. COD Enable and TE1H Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
24.0		A/D Converter Manual Test.		
EXP.		This procedure checks the A/D multiplexer and the A/D converter.		
24.1	ADM	Set A/D Multiplexer TRIGGER selector switch to EXT.		
24.2	ADC	Set A/D Converter TRIGGER selector switch to EXT.		
24.3	ST	Set A/D CONVERTER-INTERNAL/EXTERNAL to INTERNAL.		
24.4	ST	Set A/D CONVERTER-POLARITY to up position		
24.5	PC	Set A/D CONVERTER MODE to AUTO.		
24.6	IM	Set INPUT MULTIPLEXER selector switch to ADCO.		
24.7	MT	Set ADDRESS REGISTER-COMMAND switches as follow: A3 to off A2 and A1 to on Note Leave A1, A2 and A3 as shown above for the remainder of this procedure. Note In the following step, after setting ADDRESS REGISTER-COMMAND switches as specified in Table I, press and release CIO (MT panel).		

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Figure 7-24. A/D Converter Manual Check (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
24.7.1		Perform tests 1 through 30 of Table I.	Refer to Table I.	Record data on Table I.
24.8	MT	Set ADDRESS REGISTER-COMMAND A4 through A9 to off.		
24.9	MT	Press and release CIO.		
24.10	ADM	Observe A/D Multiplexer Address Display lamps.	00_8	_____
24.11	PC	Set A/D CONVERTER MODE to MAN.		
24.12	MT	Press and release CIO.		
24.13	ADM	Observe A/D Multiplexer Address Display lamps.	00_8	_____
24.14	ADC	Set A/D CONVERTER MODE to SEQ.		
24.15	MT	Press and release CIO 47 times; each time CIO is pressed, observe Multiplexer Address Display lamps.	Binary count increases by 1 each time CIO is pressed. Final count is 57_8	_____
24.16	ST	Connect positive lead of Kintel 301R power supply to red A/D EXT INPUT jack; connect negative lead to black A/D EXT INPUT jack. Using Fluke Model 803 meter as a monitor, adjust power supply for an output of 100.00 volts.		
24.17	PC	Set A/D CONVERTER MODE to AUTO.		

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Figure 7-24. A/D Converter Manual Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table I

Test	A/D Converter Switch Position	ADDRESS REGISTER A9	A8	A7	A6	A5	A4	A/D Multiplexer Address Register 4	2	1	4	2	1	A/D Converter Display Register ±	1	4	2	1	4	2	1	4	2	1	4	2	1
1	00-30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	X	X	X	X	X	X
2	01-31	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0	1	0	X	X	X	X	X	X
3	02-32	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0	1	0	X	X	X	X	X	X
4	03-33	0	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	0	0	1	0	X	X	X	X	X	X
5	04-34	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	0	0	1	0	X	X	X	X	X	X
6	05-35	0	0	0	1	0	1	0	0	0	1	0	1	0	0	1	1	0	0	1	0	X	X	X	X	X	X
7	06-36	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1	1	0	0	1	0	X	X	X	X	X	X
8	07-37	0	0	0	1	1	1	0	0	0	1	1	1	0	0	1	1	0	0	1	0	X	X	X	X	X	X
9	10-40	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	1	X	X	X	X	X	X
10	11-41	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	1	0	0	1	0	X	X	X	X	X	X
11	13-	0	0	1	0	1	1	0	0	1	0	1	1	0	0	1	1	0	0	0	1	X	X	X	X	X	X
12	14-	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	0	1	1	1	X	X	X	X	X	X
13	15-	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	0	0	1	X	X	X	X	X	X
14	20-50	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	1	1	X	X	X	X	X
15	21-51	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	1	0	1	1	X	X	X	X	X
16	22-52	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0	1	0	1	1	X	X	X	X	X
17	27-57	0	1	0	1	1	1	0	1	0	1	1	1	0	0	0	1	0	1	0	1	1	X	X	X	X	X
18	06-36	0	1	1	1	1	0	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
19	07-37	0	1	1	1	1	1	0	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	X	X	X	X
20	10-40	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
21	11-41	1	0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	X	X	X	X
22	-42	1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
23	20-50	1	0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
24	21-51	1	0	1	0	0	1	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1	1	X	X	X	X
25	22-52	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
26	-53	1	0	1	0	1	1	1	0	1	0	1	1	1	0	0	0	0	1	1	1	1	1	X	X	X	X
27	-54	1	0	1	1	0	0	1	0	1	1	0	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
28	-55	1	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1	1	X	X	X	X
29	-56	1	0	1	1	1	0	1	0	1	1	1	0	1	0	0	0	0	1	1	1	1	1	X	X	X	X
30	27-57	1	0	1	1	1	1	1	0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	X	X	X	X

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Figure 7-24. A/D Converter Manual Check (Sheet 3)

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UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
24.18	ST	Set A/D CONVERTER-INTERNAL EXTERNAL to EXTERNAL.		
24.19	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9 A8 A7 A6 A5 A4 on off on on on on		
24.20	MT	Press and release CIO.		
		Observe A/D Converter Display Register.	$+17777_8$	
		Observe A/D Multiplexer Address Display Register.	57_8	
24.21	IM	Press and release ALTER.		
24.22	IM	Observe following INPUT MULTIPLEXER display lamps: 10 through 22 All others	 Lit Not lit	 ——— ———
24.23	ST	Set INTERNAL/OFF/EXTERNAL to OFF.		
24.24		Disconnect KINTEL meter from LVDAME.		
24.25	ST	Set POLARITY to OFF.		
24.26	PC	Press and release FULL SEQ.		
24.27	PC	Observe following: FULL SEQ.	 Lit	 ———
24.28		Perform steps 1 through 13 of Table II.	Refer to Table II.	Record data on Table II.

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Figure 7-24. A/D Converter Manual Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES -	
UNIT NAME:	UNIT NO.

Table II

Test	ADDRESS REGISTER A9	A8	A7	A6	A5	A4	A/D Multiplexer Address Register 4	2	1	4	2	1	A/D Converter Display Register +	1	4	2	1	4	2	1	4	2	1
1	0	1	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	1	X	X	X	X
2	0	1	1	0	0	1	0	1	1	0	0	1	1	0	0	0	0	0	1	1	1	1	X	X	X	X
3	0	1	1	0	1	0	0	1	1	0	1	0	1	0	0	0	0	0	1	1	1	1	X	X	X	X
4	0	1	1	0	1	1	0	1	1	0	1	1	1	0	0	0	0	0	1	1	1	1	X	X	X	X
5	0	1	1	1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	1	1	1	X	X	X	X
6	0	1	1	1	0	1	0	1	1	1	0	1	1	0	0	0	0	0	1	1	1	1	X	X	X	X
7	1	0	0	0	1	1	1	0	0	0	1	1	X	0	0	0	0	0	0	0	0	0	X	X	X	X
8	1	0	0	1	0	1	1	0	0	1	0	1	1	0	1	0	0	0	1	0	1	X	X	X	X	X

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Figure 7-24. A/D Converter Manual Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
25.0		Temperature Indicators.		
EXP.		The following procedure checks the operation of the temperature sensing and indicating circuits.		
25.1	PC	Press and release POWER SUPPLY ERROR.		
25.2	MT	Observe following lamps:		
		COMPUTER-NORMAL	Lit	_____
		COMPUTER-HIGH	Not lit	_____
		COMPUTER-ARRAY	Not lit	_____
		COMPUTER-PAGE	Not lit	_____
		DATA ADAPTER-NORMAL	Lit	_____
		DATA ADAPTER-HIGH	Not lit	_____
		DATA ADAPTER-1	Not lit	_____
		DATA ADAPTER-2	Not lit	_____
25.3	ST	Set TEMP TEST to ARRAY-1		
25.4	PC	Observe HLTX.	Lit	_____
25.5	MT	Observe following lamps:		
		COMPUTER-NORMAL	Not lit	_____
		COMPUTER-HIGH	Lit	_____
		COMPUTER-ARRAY	Lit	_____
		COMPUTER-PAGE	Not lit	_____
		DATA ADAPTER-NORMAL	Not lit	_____
		DATA ADAPTER-HIGH	Lit	_____
		DATA ADAPTER-1	Lit	_____
		DATA ADAPTER-2	Not lit	_____
25.6	ST	Set TEMP TEST to OFF.		
25.7	PC	Observe HLTX	Not lit	_____
25.8	MT	Press and release COMPUTER-ARRAY/PAGE.		

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Figure 7-25. Temperature Indicators Check (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
25.9	MT	Observe following lamps:		
		COMPUTER-HIGH	Not lit	_____
		COMPUTER-ARRAY	Not lit	_____
		COMPUTER-NORMAL	Lit	_____
25.10	MT	Press and release DATA ADAPTER-1/2		
25.11	MT	Observe following lamps:		
		DATA ADAPTER-HIGH	Not lit	_____
		DATA ADAPTER-1	Not lit	_____
		DATA ADAPTER-NORMAL	Lit	_____
25.12	ST	Set TEMP TEST to PAGE-2		
25.13	PC	Observe HLTX	Lit	_____
25.14	MT	Observe following lamps:		
		COMPUTER-NORMAL	Not lit	_____
		COMPUTER-HIGH	Lit	_____
		COMPUTER-ARRAY	Not lit	_____
		COMPUTER-PAGE	Lit	_____
		DATA ADAPTER-NORMAL	Not lit	_____
		DATA ADAPTER-HIGH	Lit	_____
		DATA ADAPTER-1	Not lit	_____
		DATA ADAPTER-2	Lit	_____
25.15	ST	Set TEMP TEST to OFF		
25.16	PC	Observe HLTX	Not lit	_____
25.17	MT	Press and release COMPUTER-ARRAY/PAGE		
25.18	MT	Observe following lamps:		
		COMPUTER-HIGH	Not lit	_____
		COMPUTER-PAGE	Not lit	_____
		COMPUTER-NORMAL	Lit	_____

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Figure 7-25. Temperature Indicators Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
25.19	MT	Press and release DATA ADAPTER 1/2.		
25.20	MT	Observe following lamps:		
		DATA ADAPTER-HIGH	Not lit	———
		DATA ADAPTER-2	Not lit	———
		DATA ADAPTER-NORMAL	Lit	———
25.21	ST	Set TEMP TEST to ARRAY-1.		
25.22	PC	Observe HLTX.	Lit	———
25.23	ST	Set TEMP TEST to PAGE-2.		———
25.24	PC	Observe HLTX.	Lit	———
25.25	ST	Set TEMP TEST to OFF.		
25.26	PC	Observe HLTX.	Not lit	———
25.27	MT	Observe TEMPERATURE lamps:	All lit	———
25.28	PC	Press and release POWER SUPPLY ERROR.		
25.29	MT	Observe following lamps:		
		COMPUTER-NORMAL	Lit	———
		DATA ADAPTER-NORMAL	Lit	———
		All other TEMPERATURE lamps	Not lit	———

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Figure 7-25. Temperature Indicators Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
26.0		Interrupt Compare Error.		
EXP		The following procedure checks the operation of the interrupt compare logic and indicator. During this procedure, ignore all lighted ERROR DETECTION lamps.		
26.1	PC	Press and release POWER SUPPLY ERROR.		
26.2	IM	Set OUTPUT REGISTERS selector switch to DIN.		
26.3	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 to on all others to off		
26.4	IM	Press and release INSERT.		
26.5	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 all others	 Lit Not lit	 ——— ———
26.6	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on all others to off (613)		
26.7	MT	Press and release CIO.		
26.8	PC	Observe ERROR, CHANNEL and MODULE lamps.	All lit	———
26.9	IM	Set OUTPUT REGISTERS selector switch to CIU.		

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Figure 7-26. Interrupt Compare Error Check (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
26.10	IM	Set OUTPUT REGISTERS-COMD switches as follows: 4 through 9 to on all others to off		
26.11	IM	Press and release INSERT. (Ignore lighted ERROR DETECTION lamps.)		
26.12	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		4 through 9	Lit	———
		all others	Not lit	———
26.13	MT	Observe INTER COMPARE ERROR.	Not lit	———
26.14	IM	Set OUTPUT REGISTERS-COMD switches as follows: 6 through 9 to on all others to off		
26.15	IM	Press and release INSERT.		
26.16	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		6 through 9	Lit	———
		all others	Not lit	———
26.17	MT	Observe INTER COMPARE ERROR.	Lit	———
26.18	IM	Set OUTPUT REGISTERS-COMD switches as follows: 4 through 9 to on all others to off		
26.19	IM	Press and release INSERT.		

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Figure 7-26. Interrupt Compare Error Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
26.20	IM	Observe following OUTPUT REGISTERS-REG lamps: 4 through 9 all others	 Lit Not lit	 ——— ———
26.21	MT	Press and release INTER COMPARE ERROR.		
26.22	MT	Observe INTER COMPARE ERROR.	Not lit	———
26.23	IM	Set OUTPUT REGISTERS-COMD switches as follows: 4, 5, 6 and 9 to on all others to off		
26.24	IM	Press and release INSERT.		
26.25	IM	Observe following OUTPUT REGISTERS-REG lamps: 4, 5, 6 and 9 all others	 Lit Not lit	 ——— ———
26.26	MT	Observe INTER COMPARE ERROR.	Lit	———
26.27	IM	Set OUTPUT REGISTERS-COMD switches as follows: 4 through 9 to on all others to off		
26.28	IM	Press and release INSERT.		
26.29	IM	Observe following OUTPUT REGISTERS-REG lamps: 4 through 9 all others	 Lit Not lit	 ——— ———

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Figure 7-26. Interrupt Compare Error Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
26.30	MT	Press and release INTER COMPARE ERROR.		
26.31	MT	Observe INTER COMPARE ERROR.	Not lit	———
26.32	IM	Set OUTPUT REGISTERS-COMD switches as follows: 4, 5, 6 and 9 to on all others to off		
26.33	IM	Press and release INSERT.		
26.34	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		4, 5, 6 and 9	Lit	———
		all others	Not lit	———
26.35	MT	Observe INTER COMPARE ERROR.	Lit	———
26.36	IM	Set OUTPUT REGISTERS selector switch to DIN.		
26.37	IM	Set OUTPUT REGISTERS-COMD switches as follows: 15 to on all others to off		
26.38	IM	Press and release INSERT.		
26.39	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		15	Lit	———
		all others	Not lit	———
26.40	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A2 and A1 to on all others to off (623)		

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Figure 7-26. Interrupt Compare Error Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
26.41	MT	Press and release CIO.		
26.42	PC	Observe ERROR, CHANNEL and MODULE lamps.	None lit	———
26.43	PC	Press and release POWER SUPPLY ERROR.		
26.44	MT	Observe INTER COMPARE ERROR.	Not lit	———

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Figure 7-26. Interrupt Compare Error Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.0		Resolver Simulator.		
EXP		This procedure checks the operation of the resolver simulator.		
EXP		The following steps check the outputs of the tapped transformer.		
27.1	PC	Press and release POWER SUPPLY ERROR.		
27.2	ST	Set EXT FREQ/OFF/INT 24VAC to EXT FREQ.		
27.3	IM	Set OUTPUT REGISTERS selector switch to DIN.		
27.4	IM	Set all OUTPUT REGISTERS-COMD switches to off.		
27.5	IM	Press and release INSERT.		
27.6	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	———
27.7	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1, A2 and A3 to on all others to off (007)		
27.8	MT	Press and release CIO.		
27.9	ST	Connect external frequency source (adjusted to 1000 cps and 26 V RMS) to EXT FREQ INPUT jacks.		

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Figure 7-27. Resolver Simulator Check (Sheet 1 of 24)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.10	ST	Measure (with AC Fluke meter) the voltage between SIN and REF, and COS and REF jacks as the RESOLVER SIMULATION selector switch is rotated to positions listed in Table I.	Refer to Table I	Record data on Table I.
EXP		The following steps check the path selection circuits.		
27.11	IM	Set OUTPUT REGISTERS-COMD switches as follows: 2 through 25 to on S and 1 to off		
27.12	IM	Press and release INSERT.		
27.13	IM	Observe following OUTPUT REGISTERS-REG lamps: 2 through 25 S and 1	 Lit Not lit	 ——— ———
27.14	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1 through A7 to on A8 and A9 to off (177)		
27.15	MT	Press and release CIO twice.		
27.16	IM	Set OUTPUT REGISTERS-COMD switches as follows: 8 to on all others to off		
27.17	IM	Press and release INSERT.		

Figure 7-27. Resolver Simulator Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Table I

RESOLVER SIMULATION Switch Position	*Voltage (VAC) SIN to REF DATA	Voltage (VAC) COS to REF DATA
FG1	4.240 ____	2.650 ____
FG2	4.095 ____	2.870 ____
FG3	2.650 ____	4.240 ____
FG4	2.870 ____	4.095 ____
CG1	3.045 ____	3.965 ____
CG2	3.215 ____	3.830 ____
CG3	3.965 ____	3.045 ____
CG4	3.830 ____	3.215 ____
9	4.570 ____	2.035 ____
10	1.545 ____	4.755 ____
11	4.395 ____	2.385 ____
12	2.035 ____	4.570 ____
13	2.385 ____	4.395 ____
14	4.755 ____	1.545 ____
15	3.345 ____	3.715 ____
16	3.715 ____	3.345 ____
17	3.475 ____	3.595 ____
18	3.595 ____	3.475 ____

*Tolerance on each voltage is ±5%.

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Figure 7-27. Resolver Simulator Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.18	IM	Observe following OUTPUT REGISTERS-REG lamps: 8 all others	 Lit Not lit	 ——— ———
27.19	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1, A2 and A3 to on all others to off		
27.20	MT	Press and release CIO.		
27.21	ST	Set RESOLVER SIMULATION selector switch to 18.		
27.22	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———
27.23	IM	Set OUTPUT REGISTERS-COMD switches as follows: 9 to on all others to off		
27.24	IM	Press and release INSERT.		
27.25	IM	Observe following OUTPUT REGISTERS-REG lamps: 9 all others	 Lit Not lit	 ——— ———
27.26	MT	Press and release CIO.		
27.27	ST	Set RESOLVER SIMULATION selector switch to 16.		

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Figure 7-27. Resolver Simulator Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.28	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———
27.29	IM	Set OUTPUT REGISTERS-COMD switches as follows: 10 to on all others to off		
27.30	IM	Press and release INSERT.		
27.31	IM	Observe following OUTPUT REGISTERS-REG lamps: 10 all others	 Lit Not lit	 ——— ———
27.32	MT	Press and release CIO		
27.33	ST	Set RESOLVER SIMULATION selector switch to CG4.		
27.34	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———
27.35	IM	Set OUTPUT REGISTERS-COMD switches as follows: 11 to on all others to off		
27.36	IM	Press and release INSERT.		
27.37	IM	Observe following OUTPUT REGISTERS-REG lamps: 11 all others	 Lit Not lit	 ——— ———

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Figure 7-27. Resolver Simulator Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.38	MT	Press and release CIO.		
27.39	ST	Set RESOLVER SIMULATION selector switch to CG3.		
27.40	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———
27.41	IM	Set OUTPUT REGISTERS-COMD switches as follows: 12 to on all others to off		
27.42	IM	Press and release INSERT.		
27.43	IM	Observe following OUTPUT REGISTERS-REG lamps: 12 all others	 Lit Not lit	 ——— ———
27.44	MT	Press and release CIO.		
27.45	ST	Set RESOLVER SIMULATION selector switch to FG2.		
27.46	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———
27.47	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 to on all others to off		
27.48	IM	Press and release INSERT.		

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Figure 7-27. Resolver Simulator Check (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.49	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 all others	 Lit Not lit	 ——— ———
27.50	MT	Press and release CIO.		
27.51	ST	Set RESOLVER SIMULATION selector switch to FG1.		
27.52	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———
27.53	IM	Set OUTPUT REGISTERS-COMD switches as follows: 14 to on all others to off		
27.54	IM	Press and release INSERT.		
27.55	IM	Observe following OUTPUT REGISTERS-REG lamps: 14 all others	 Lit Not lit	 ——— ———
27.56	MT	Press and release CIO		
27.57	ST	Set RESOLVER SIMULATION selector switch to 11.		
27.58	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	———

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Figure 7-27. Resolver Simulator Check (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.59	IM	Set OUTPUT REGISTERS-COMD switches as follows: 15 to on all others to off		
27.60	IM	Press and release INSERT.		
27.61	IM	Observe following OUTPUT REGISTERS-REG lamps: 15 all others	 Lit Not lit	 _____ _____
27.62	MT	Press and release CIO.		
27.63	ST	Set RESOLVER SIMULATION selector switch to 9.		
27.64	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	_____
27.65	IM	Set OUTPUT REGISTERS-COMD switches as follows: 16 to on all others to off		
27.66	IM	Press and release INSERT.		
27.67	IM	Observe following OUTPUT REGISTERS-REG lamps: 16 all others	 Lit Not lit	 _____ _____
27.68	MT	Press and release CIO.		
27.69	ST	Set RESOLVER SIMULATION selector switch to 14.		

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Figure 7-27. Resolver Simulator Check (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.70	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks	5 (±0.5) VAC	_____
27.71	IM	Set OUTPUT REGISTERS-COMD switches as follows: 17 to on all others to off		
27.72	IM	Press and release INSERT		
27.73	IM	Observe following OUTPUT REGISTERS-REG lamps: 17 all others	 Lit Not lit	 _____ _____
27.74	MT	Press and release CIO		
27.75	ST	Set RESOLVER SIMULATION selector switch to 17.		
27.76	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	_____
27.77	IM	Set OUTPUT REGISTERS-COMD switches as follows: 18 to on all others to off		
27.78	IM	Press and release INSERT.		
27.79	IM	Observe following OUTPUT REGISTERS-REG lamps: 18 all others	 Lit Not lit	 _____ _____
27.80	MT	Press and release CIO		

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Figure 7-27. Resolver Simulator Check (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.81	ST	Set RESOLVER SIMULATION selector switch to 15		
27.82	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks	5 (±0.5) VAC	_____
27.83	IM	Set OUTPUT REGISTERS-COMD switches as follows: 19 to on all others to off		
27.84	IM	Press and release INSERT		
27.85	IM	Observe following OUTPUT REGISTERS-REG lamps: 19 all others	 Lit Not lit	 _____ _____
27.86	MT	Press and release CIO.		
27.87	ST	Set RESOLVER SIMULATION selector switch to CG2.		
27.88	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	_____
27.89	IM	Set OUTPUT REGISTERS-COMD switches as follows: 20 to on all others to off		
27.90	IM	Press and release INSERT		
27.91	IM	Observe following OUTPUT REGISTERS-REG lamps: 20 all others	 Lit Not lit	 _____ _____

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Figure 7-27. Resolver Simulator Check (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.92	MT	Press and release CIO.		
27.93	ST	Set RESOLVER SIMULATION selector switch to CG1.		
27.94	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	_____
27.95	IM	Set OUTPUT REGISTERS-COMD switches as follows: 21 to on all others to off		
27.96	IM	Press and release INSERT.		
27.97	IM	Observe following OUTPUT REGISTERS-REG lamps: 21 all others	 Lit Not lit	 _____ _____
27.98	MT	Press and release CIO.		
27.99	ST	Set RESOLVER SIMULATION selector switch to FG4.		
27.100	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0.5) VAC	_____
27.101	IM	Set OUTPUT REGISTERS-COMD switches as follows: 22 to on all others to off		
27.102	IM	Press and release INSERT		

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Figure 7-27. Resolver Simulator Check (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.103	IM	Observe following OUTPUT REGISTERS-REG lamps: 22 all others	 Lit Not lit	 _____ _____
27.104	MT	Press and release CIO		
27.105	ST	Set RESOLVER SIMULATION selector switch to FG3.		
27.106	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks	5 (±0.5) VAC	_____
27.107	IM	Set OUTPUT REGISTERS-COMD switches as follows: 23 to on all others to off		
27.108	IM	Press and release INSERT.		
27.109	IM	Observe following OUTPUT REGISTERS-REG lamps: 23 all others	 Lit Not lit	 _____ _____
27.110	MT	Press and release CIO.		
27.111	ST	Set RESOLVER SIMULATION selector switch to 13.		
27.112	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks	5 (±0.5) VAC	_____
27.113	IM	Set OUTPUT REGISTERS-COMD switches as follows: 24 to on all others to off		

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Figure 7-27. Resolver Simulator Check (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.114	IM	Press and release INSERT.		
27.115	IM	Observe following OUTPUT REGISTERS-REG lamps: 24 all others	 Lit Not lit	 _____ _____
27.116	MT	Press and release CIO.		
27.117	ST	Set RESOLVER SIMULATION selector switch to 12		
27.118	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks	5 (±0 5) VAC	_____
27.119	IM	Set OUTPUT REGISTERS-COMD switches as follows: 25 to on all others to off		
27.120	IM	Press and release INSERT.		
27.121	IM	Observe following OUTPUT REGISTERS-REG lamps: 25 all others	 Lit Not lit	 _____ _____
27.122	MT	Press and release CIO.		
27.123	ST	Set RESOLVER SIMULATION selector switch to 10.		
27.124	ST	Measure voltage between SIN and REF jacks and between COS and REF jacks.	5 (±0 5) VAC	_____

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Figure 7-27. Resolver Simulator Check (Sheet 13)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP		The following steps check the sin and cos magnitude registers. Tolerance on all voltage measurements is ±10%.		
27.125	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1, 2 and 14 to on all others to off		
27.126	IM	Press and release INSERT.		
27.127	IM	Observe following OUTPUT REGISTERS-REG lamps: S, 1, 2 and 14 all others	 Lit Not lit	 ———— ————
27.128	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1 through A7 to on A8 and A9 to off		
27.129	MT	Press and release CIO.		
27.130	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 2.5 VAC 2.5 VAC	 ———— ————
27.131	MT	Press and release CIO.		
27.132	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 2.5 VAC 2.5 VAC	 ———— ————
27.133	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1, 3 and 15 to on all others to off		

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Figure 7-27. Resolver Simulator Check (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.134	IM	Press and release INSERT.		
27.135	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 3 and 15	Lit	_____
		all others	Not lit	_____
27.136	MT	Press and release CIO.		
27.137	ST	Measure voltage between the following test jacks:		
		SIN and REF	1.23 VAC	_____
		COS and REF	1.23 VAC	_____
27.138	MT	Press and release CIO.		
27.139	ST	Measure voltage between the following test jacks:		
		SIN and REF	1.23 VAC	_____
		COS and REF	1.23 VAC	_____
27.140	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		S, 1, 4 and 16 to on		
		all others to off		
27.141	IM	Press and release INSERT.		
27.142	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 4 and 16	Lit	_____
		all others	Not lit	_____
27.143	MT	Press and release CIO.		
27.144	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.61 VAC	_____
		COS and REF	0.61 VAC	_____
27.145	MT	Press and release CIO.		

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Figure 7-27. Resolver Simulator Check (Sheet 15)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.146	ST	Measure voltage between the following test jacks:		
		SIN and REF	0 61 VAC	_____
		COS and REF	0 61 VAC	_____
27.147	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		S. 1, 5 and 17 to on		
		all others to off		
27.148	IM	Press and release INSERT.		
27.149	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S. 1, 5 and 17	Lit	_____
		all others	Not lit	_____
27.150	MT	Press and release CIO.		
27.151	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.3 VAC	_____
		COS and REF	0.3 VAC	_____
27.152	MT	Press and release CIO		
27.153	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.3 VAC	_____
		COS and REF	0.3 VAC	_____
27.154	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		S. 1, 6 and 18 to on		
		all others to off		
27.155	IM	Press and release INSERT.		

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Figure 7-27. Resolver Simulator Check (Sheet 16)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.156	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 6 and 18	Lit	_____
		all others	Not lit	_____
27.157	MT	Press and release CIO.		
27.158	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.15 VAC	_____
		COS and REF	0.15 VAC	_____
27.159	MT	Press and release CIO.		
27.160	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.15 VAC	_____
		COS and REF	0 15 VAC	_____
27.161	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		S, 1, 7 and 19 to on		
		all others to off		
27.162	IM	Press and release INSERT.		
27.163	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 7 and 19	Lit	_____
		all others	Not lit	_____
27.164	MT	Press and release CIO.		
27.165	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.075 VAC	_____
		COS and REF	0.075 VAC	_____
27.166	MT	Press and release CIO.		

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Figure 7-27. Resolver Simulator Check (Sheet 17)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.167	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 0.075 VAC 0.075 VAC	 _____ _____
27.168	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1, 8 and 20 to on all others to off		
27.169	IM	Press and release INSERT.		
27.170	IM	Observe following OUTPUT REGISTERS-REG lamps: S, 1, 8 and 20 all others	 Lit Not lit	 _____ _____
27 171	MT	Press and release CIO.		
27 172	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 0 037 VAC 0.037 VAC	 _____ _____
27.173	MT	Press and release CIO.		
27 174	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 0.037 VAC 0 037 VAC	 _____ _____
27 175	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1, 9 and 21 to on all others to off		
27.176	IM	Press and release INSERT.		

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Figure 7-27. Resolver Simulator Check (Sheet 18)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.177	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 9 and 21	Lit	_____
		all others	Not lit	_____
27.178	MT	Press and release CIO.		
27.179	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.018 VAC	_____
		COS and REF	0.018 VAC	_____
27.180	MT	Press and release CIO		
27.181	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.018 VAC	_____
		COS and REF	0.018 VAC	_____
27.182	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		S, 1, 10 and 22 to on		
		all others to off		
27.183	IM	Press and release INSERT		
27.184	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 10 and 22	Lit	_____
		all others	Not lit	_____
27.185	MT	Press and release CIO.		
27.186	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.0084 VAC	_____
		COS and REF	0.0084 VAC	_____
27.187	MT	Press and release CIO.		

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Figure 7-27. Resolver Simulator Check (Sheet 19)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.188	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 0 0084 VAC 0.0084 VAC	 _____ _____
27.189	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1, 11 and 23 to on all others to off		
27 190	IM	Press and release INSERT.		
27.191	IM	Observe following OUTPUT REGISTERS-REG lamps: S, 1, 11 and 23 all others	 Lit Not lit	 _____ _____
27.192	MT	Press and release CIO		
27.193	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 0.0046 VAC 0.0046 VAC	 _____ _____
27.194	MT	Press and release CIO		
27.195	ST	Measure voltage between the following test jacks: SIN and REF COS and REF	 0.0046 VAC 0.0046 VAC	 _____ _____
27.196	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1, 12 and 24 to on all others to off		
27.197	IM	Press and release INSERT.		

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Figure 7-27. Resolver Simulator Check (Sheet 20)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.198	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S, 1, 12 and 24	Lit	_____
		all others	Not lit	_____
27.199	MT	Press and release CIO.		
27.200	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.0023 VAC	_____
		COS and REF	0.0023 VAC	_____
27.201	MT	Press and release CIO.		
27 202	ST	Measure voltage between the following test jacks:		
		SIN and REF	0.0023 VAC	_____
		COS and REF	0.0023 VAC	_____

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Figure 7-27. Resolver Simulator Check (Sheet 21)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP.		The following steps check the quadrant selection circuits.		
27.203	IM	Set all OUTPUT REGISTERS-COMD switches to on.		
27.204	IM	Press and release INSERT.		
27.205	IM	Observe OUTPUT REGISTERS-REG	All lit	_____
27.206	MT	Press and release CIO.		
27.207	ST	Measure ac voltage between SIN and COS jacks.	Less than 20 mv	_____
27.208	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A2 and A1 to on all others to off (623)		
27.209	IM	Set OUTPUT REGISTERS-COMD switches as follows: 20 and 21 to on all others to off		
27.210	IM	Press and release INSERT.		
27.211	IM	Observe following OUTPUT REGISTERS-REG lamps: 20 and 21 all others	 Lit Not lit	 _____ _____
27.212	MT	Press and release CIO.		
27.213	ST	Measure ac voltage between SIN and COS jacks.	Approx. 10 VAC	

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Figure 7-27. Resolver Simulator Check (Sheet 22)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.214	IM	Set OUTPUT REGISTERS-COMD switches as follows: 22 and 23 to on all others to off		
27.215	IM	Press and release INSERT.		
27.216	IM	Observe following OUTPUT REGISTERS-REG lamps: 22 and 23 all others	 Lit Not lit	 _____ _____
27.217	MT	Press and release CIO.		
27.218	ST	Measure ac voltage between SIN and COS jacks.	Less than 20 mv	_____
27.219	IM	Set all OUTPUT REGISTERS-COMD switches to on		
27.220	IM	Press and release INSERT		
27.221	IM	Observe OUTPUT REGISTERS-REG lamps.	All lit	_____
27.222	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1 through A7 to on A8 and A9 to off		
27.223	MT	Press and release CIO		
27.224	ST	Measure ac voltage between SIN and COS jacks	Less than 20 mv	_____
27.225	IM	Set OUTPUT REGISTERS COMD switches as follows: 20 and 21 to on all others to off		
27.226	IM	Press and release INSERT.		

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Figure 7-27. Resolver Simulator Check (Sheet 23)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: • UNIT NO.

Step	Panel	Operation	Normal Indication	Data
27.227	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		. 20 and 21	Lit	————
		all others	Not lit	————
27.228	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A2 and A1 to on all others to off (623)		
27.229	MT	Press and release CIO.		
27.230	ST	Measure ac voltage between SIN and COS jacks.	Approx. 10 VAC	
27.231	IM	Set OUTPUT REGISTERS-COMD switches as follows: 22 and 23 to on all others to off		
27.232	IM	Press and release INSERT.		
27.233	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		22 and 23	Lit	————
		all others	Not lit	————
27.234	MT	Press and release CIO.		
27.235	ST	Measure ac voltage between SIN and COS jacks.	Less than 20 mv	
27.236	ST	Set EXT FREQ/OFF/INT 24 VAC to OFF.		
27.237		Disconnect all external test equipment from the LVDAME.		

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Figure 7-27. Resolver Simulator Check (Sheet 24)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.0		Interrupt 15 and Power Sequencing Telemetry Tests.		
EXP		This procedure checks the generation of INT 15 NOT and the operation of the DATA ADAPTER TELEMETRY indicators.		
28.1	PC	Press and release POWER SUPPLY ERROR.		
28.2	PC	Press and release FULL SEQ.		
28.3	PC	Observe following lamps FULL SEQ POWER UP	 Lit Lit	 ——— ———
28.4	IM	Set OUTPUT REGISTERS selector switch to DIN.		
28.5	IM	Set OUTPUT REGISTERS-COMD switches as follows: 21 to on all others to off		
28.6	IM	Press and release INSERT.		
28.7	IM	Observe following OUTPUT REGISTERS-REG lamps: 21 all others	 Lit Not lit	 ——— ———
28.8	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on all others to off (613)		
28.9	MT	Press and release CIO.		

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 1 of 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.10	PC	Observe following POWER SUPPLY AND DISCRETE OUTPUT lamps: COMD-1 and CTRL 1	 Both lit	 ———
28.11	MT	Press and release CIO while observing signal at TP21 (INT 15 NOT). (Trigger INT +)	Illustration A	———
28.12	PC	Press and release POWER SUPPLY AND DISCRETE OUTPUT-RESET.		
28.13	PC	Observe POWER SUPPLY AND DISCRETE OUTPUT lamps.	None lit	———
28.14	IM	Set OUTPUT REGISTERS-COMD switches as follows: 20 to on all others to off		
28.15	IM	Press and release INSERT.		
28.16	IM	Observe following OUTPUT REGISTERS-REG lamps: 20 all others	 Lit Not lit	 ——— ———
28.17	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A4, A2 and A1 to on all others to off.		
28.18	MT	Press and release CIO.		
28.19	PC	Observe following lamps: FULL SEQ INITIAL SEQ HLTX	 Not lit Lit Lit	 ——— ——— ———

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.20	MT	Press and release CIO while observing signal at TP21.	Illustration A	_____
28.21	IM	Set OUTPUT REGISTERS-COMD switches as follows: 21 to on all others to off		
28.22	IM	Press and release INSERT.		
28.23	IM	Observe following OUTPUT REGISTERS-REG lamps: 21 all others	 Lit Not lit	 _____ _____
28.24	MT	Press and release CIO.		
28.25	PC	Observe following lamps: FULL SEQ INITIAL SEQ HLTX	 Lit Not lit Not lit	 _____ _____ _____
28.26	MT	Press and release CIO while observing signal at TP21.	Illustration A	_____
EXP.		The following steps ensure that a coolant flow failure will sequence power off. Ignore all unspecified lamps.		
28.27	ST	Set Self-Check switch to 1.		
28.28	PC	Observe following lamps: SEQ OFF FULL SEQ HLTX	 Lit Not lit Lit	 _____ _____ _____
28.29	ST	Set Self-Check switch to OFF.		
28.30	PC	Observe HLTX.	Not lit	_____

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
EXP		The following steps ensure that an LVDA or Computer temperature error will sequence power off. Ignore all unspecified lamps.		
28.31	PC	Press and release FULL SEQ.		
28.32	PC	Observe following lamps:		
		FULL SEQ	Lit	———
		SEQ OFF	Not lit	———
28.33	ST	Set TEMP TEST to ARRAY-1.		
28.34	PC	Observe following lamps:		
		SEQ OFF	Lit	———
		FULL SEQ	Not lit	———
		HLTX	Lit	———
28.35	ST	Set TEMP TEST to OFF.		
28.36	PC	Observe HLTX.		
28.37	PC	Press and release INITIAL SEQ.		
28.38	PC	Observe following lamps:		
		INITIAL SEQ	Lit	———
		SEQ OFF	Not lit	———
		HLTX	Lit	———
28.39	ST	Set TEMP-TEST to PAGE-2.		
28.40	PC	Observe following lamps:		
		SEQ OFF	Lit	———
		INITIAL SEQ	Not lit	———
28.41	ST	Set TEMP TEST to OFF.		

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.42	PC	Observe HLTX.	Not lit	———
28.43	MT	Press and release ARRAY/PAGE; press and release 1/2.		
28.44	MT	Observe TEMPERATURE lamps.	Two NORMAL lamps lit.	———
28.45	IM	Set OUTPUT REGISTERS-COMD switches as follows: 11 to on all others to off		
28.46	IM	Press and release INSERT.		
28.47	IM	Observe following OUTPUT REGISTERS-REG lamps: 11 all others	 Lit Not lit	 ——— ———
28.48	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A4, A2 and A1 to on all others to off (613)		
28.49	MT	Press and release CIO.		
28.50	MT	Observe DATA ADAPTER TELEMETRY lamps.	One is lit.	———
28.51	IM	Set OUTPUT REGISTERS-COMD switches as follows: 14, 16, 18, 20, 22 and 24 to on all others to off		
28.52	IM	Press and release INSERT.		

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.53	IM	Observe following OUTPUT REGISTERS-REG lamps: 14, 16, 18, 20, 22 and 24 all others	 Lit Not lit	 ——— ———
28.54	MT	Press and release FULL SEQ.		
28.55	MT	Observe DATA ADAPTER TELEMETRY lamps.	None lit	———
28.56	PC	Observe following lamps: FULL SEQ SEQ OFF	 Lit Not lit	 ——— ———
28.57	IM	Set OUTPUT REGISTERS-COMD switches as shown in Test 1, Table I. All unspecified bits are "0's" (off).		
28.58	IM	Press and release INSERT.		
28.59	PC	Verify that SEQ OFF is lit and FULL SEQ is not lit.		
28.60	MT	Observe DATA ADAPTER TELEMETRY lamps.	Refer to Table I.	Record data on Table I.
28.61	IM	Set OUTPUT REGISTERS-COMD switches as follows: 14, 16, 18, 20, 22 and 24 to on all others to off.		
28.62	MT	Press and release DATA ADAPTER TELEMETRY-RESET.		
28.62.1	MT	Observe DATA ADAPTER TELEMETRY lamp specified in Table I.	Lit	Record data on Table I.

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.63	IM	Press and release INSERT.		
28.64	MT	Press and release DATA ADAPTER TELEMETRY-RESET.		
28.64.1	MT	Observe DATA ADAPTER TELEMETRY lamps.	None lit	
28.65	PC	Press and release FULL SEQ.		
28.66		Repeat steps 28.57 through 28.65 for Tests 2 through 12 of Table I.		
28.67	IM	Set OUTPUT REGISTERS-COMD switches as follows: 11 to on all others to off		
28.68	IM	Press and release INSERT.		
28.69	IM	Observe following OUTPUT REGISTERS-REG lamps: 11 all others	 Lit Not lit	 ——— ———
28.70	PC	Observe following lamps: SEQ OFF FULL SEQ	 Lit Not lit	 ——— ———
28.71	MT	Observe DATA ADAPTER TELEMETRY lamps.	One is lit	———
28.72	MT	Press and release DATA ADAPTER TELEMETRY-RESET.		
28.73	MT	Observe DATA ADAPTER TELEMETRY lamps.	Lamp lit in step 28.71 still lit.	———

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
28.74	PC	Press and release FULL SEQ.		
28.75	PC	Observe following lamps:		
		FULL SEQ	Not lit	———
		SEQ OFF	Lit	———
		FULL ERROR	Lit	———
28.76	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A9, A8, A5, A2 and A1 to on all others to off (623)		
28.77	MT	Press and release CIO.		
28.78	MT	Press and release DATA ADAPTER TELEMETRY-RESET.		
28.79	MT	Observe DATA ADAPTER TELEMETRY lamps.	None lit	———
28.80	PC	Press and release FULL SEQ.		
28.81	PC	Observe following lamps:		
		FULL SEQ	Lit	———
		SEQ OFF	Not lit	———
		FULL ERROR	Not lit	———
EXP.		The following steps check the EPDN logic.		
28.82	ST	Set Self Test switch to 11.		
28.83	PC	Observe following lamps		
		FULL SEQ	Not lit	———
		INITIAL SEQ	Lit	———
		HLTX	Lit	———
28.84	ST	Set Self Test switch to OFF.		

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

Test	OUTPUT REGISTERS-COMD switches 14	15	16	17	18	19	20	21	22	23	24	25	DATA ADAPTER TELEMETRY- Lamp Lit	Data
1	1	1	1	0	1	0	1	0	1	0	1	0	+20VDC	
2	0	0	1	0	1	0	1	0	1	0	1	0	+20VDC	
3	1	0	1	1	1	0	1	0	1	0	1	0	+12VDC	
4	1	0	0	0	1	0	1	0	1	0	1	0	+12VDC	
5	1	0	1	0	1	1	1	0	1	0	1	0	+6VDC left	
6	1	0	1	0	0	0	1	0	1	0	1	0	+6VDC left	
7	1	0	1	0	1	0	1	1	1	0	1	0	+6VDC right	
8	1	0	1	0	1	0	0	0	1	0	1	0	+6VDC right	
9	1	0	1	0	1	0	1	0	1	1	1	0	-3VDC	
10	1	0	1	0	1	0	1	0	0	0	1	0	-3VDC	
11	1	0	1	0	1	0	1	0	1	0	1	1	-20VDC	
12	1	0	1	0	1	0	1	0	1	0	0	0	-20VDC	

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Figure 7-28. Interrupt 15 and Power Sequencing Telemetry Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.0		Optisyn Simulator.		
EXP.		This procedure checks the operation of the optisyn simulator.		
29.1	IM	Set OUTPUT REGISTERS-selector switch to OPT.		
29.1.1	IM	Set all OUTPUT REGISTERS-COMD switches to off.		
29.1.2	IM	Press and release INSERT.		
29.1.3	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____

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Figure 7-29. Optisyn Simulator Check (Sheet 1 of 26)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.2	PC	Press and release POWER SUPPLY ERROR.		
29.2 1	MT	Press and release ACCEL PLUS OR MINUS.		
29.3	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.4	IM	Set INPUT MULTIPLEXER selector switch to DIN.		
29.5	IM	Set OUTPUT REGISTERS-COMD switches as follows: 13 through 25 to on all others to off		
29.6	IM	Press and release INSERT.		
29.7	IM	Observe following OUTPUT REGISTERS-REG lamps: 13 through 25 all others	 Lit Not lit	 _____ _____
29.8	IM	Press and release INPUT MULTIPLEXER-ALTER		
29.9	IM	Observe following INPUT MULTIPLEXER display lamps: 13 through 25 all others	 Lit Not lit	 _____ _____

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Figure 7-29. Optisyn Simulator Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.10	MT	Press and release ACCEL DL1.		
29.11	IM	Set COMD-23 to off.		
29.12	IM	Press and release INSERT.		
29.13	IM	Observe REG 23	Not lit	_____
29.14	MT	Press and release ACCEL INHIBIT SUB.		
29.15	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.16	IM	Observe REG-14 through 17.	Lamps light and go out in following sequence: 14 15 16 17 0 0 0 0 0 1 0 1 1 1 1 1 1 0 1 0 sequence repeats.	_____
29.17	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.18	IM	Set COMD-23 to on.		
29.19	IM	Press and release INSERT.		
29.20	IM	Observe REG-23.	Lit	_____
29.21	MT	Press and release ACCEL PLUS OR MINUS.		

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Figure 7-29. Optisyn Simulator Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.22	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.23	IM	Observe REG-14 through 17.	Lamps light and go out in following sequence: 14 15 16 17 0 0 0 0 1 0 1 0 1 1 1 1 0 1 0 1 sequence repeats.	_____
29.24	MT	Wait for a time that no OUTPUT REGISTERS-REG lamps are lit. then press and release ACCELL INHIBIT SUB.		
29.25	IM	Observe REG-14 through 17.	None lit	_____
29.26	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.27	IM	Set OUTPUT REGISTERS-COMD switches as follows: 23, 24 and 25 to on all others to off		
29.28	IM	Press and release INSERT.		
29.29	IM	Observe following OUTPUT REGISTERS-REG lamps: 23, 24 and 25 all others	 Lit Not lit	 _____ _____

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Figure 7-29. Optisyn Simulator Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.30	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.31	IM	Observe following INPUT MULTIPLEXER display lamps: 23, 24 and 25 all others	 Lit Not lit	 _____ _____
29.32	MT	Press and release ACCEL DL1.		
29.33	IM	Set REG-23 to off.		
29.34	IM	Press and release INSERT		
29.35	IM	Observe REG-23.	Not lit	_____
29.36	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.37	IM	Observe OUTPUT REGISTERS-REG lamps	None lit	_____
29.38	MT	Press and release SET DA DST.		
29.39	PC	Observe DST.	Lit	_____
29.40	MT	Press and release ACCEL INHIBIT SUB.		
29.41	MT	Press and release ADVANCE six times.		
29.42	IM	Observe REG-14 through 17.	None lit	_____
29.43	MT	Press and release ADVANCE.		

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Figure 7-29. Optisyn Simulator Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.44	IM	Ovserve following OUTPUT REGISTERS-REG lamps:		
		14 and 16	Lit	_____
		15 and 17	Not lit	_____
		all others	Not lit	_____
29.45	MT	Press and release ADVANCE six times.		
29.46	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		14 and 16	Lit	_____
		15 and 17	Not lit	_____
29.47	MT	Press and release ADVANCE.		
29.48	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		14 through 17	All lit	_____
29.49	MT	Press and release ADVANCE six times.		
29.50	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		14 through 17	All lit	_____
29.51	MT	Press and release ADVANCE.		
29.52	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		15 and 17	Lit	_____
		14 and 16	Not lit	_____
29.53	MT	Press and release ADVANCE six times.		

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Figure 7-29. Optisyn Simulator Check (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.53	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		15 and 17	Lit	_____
		14 and 16	Not lit	_____
29.55	MT	Press and release ADVANCE.		
29.56	IM	Observe REG-14 through 17.	None lit	_____
29.57	MT	Press and release RESET DA DST.		
29.58	PC	Observe DST.	Not lit	_____
29.59	PC	Repeat steps 29.1 through 29.1.3.		
29.60	MT	Press and release ACCEL PLUS OR MINUS.		
29.61	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.62	IM	Set OUTPUT REGISTERS-COMD switches as follows:		
		S and 1 through 12 to on		
		all others to off		
29.63	IM	Press and release INSERT.		
29.64	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		S and 1 through 12	Lit	_____
		all others	Not lit	_____
29.65	IM	Press and release INPUT MULTIPLEXER-ALTER.		

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Figure 7-29. Optisyn Simulator Check (Sheet 7)

INTERNATIONAL BUSINESS MACHINES–				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
29.66	IM	Observe following INPUT MULTIPLEXER display lamps: S and 1 through 12 all others	 Lit Not lit	 _____ _____
29.67	MT	Press and release ACCEL DL2.		
29.68	IM	Press and release COMD-23 and COMD-25.		
29.69	IM	Press and release INSERT.		
29.70	IM	Observe REG-23 and REG-25	Both lit	_____
29.71	MT	Press and release ACCEL INHIBIT SUB.		
29.72	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.73	IM	Observe REG-18 through 21.	Lamps light and go out in following sequence: 18 19 20 21 0 0 0 0 0 1 0 1 1 1 1 1 1 0 1 0 sequence repeats.	_____
29.74	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.75	IM	Set COMD-24 to on.		

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Figure 7-29. Optisyn Simulator Check (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.76	IM	Press and release INSERT.		
29.77	IM	Observe REG-24.	Lit	_____
29.78	MT	Press and release ACCEL PLUS OR MINUS.		
29.79	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.80	IM	Observe REG-18 through 21.	Lamps light and go out in following sequence: 18 19 20 21 0 0 0 0 1 0 1 0 1 1 1 1 0 1 0 1 sequence repeats.	_____
29.81	MT	Wait for a time that no OUTPUT REGISTERS-REG lamps are lit, then press and release ACCEL INHIBIT SUB.		
29.82	IM	Observe REG 18 through 21.	None lit	_____
29.83	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.84	IM	Set OUTPUT REGISTERS-COMD switches as follows: 10, 11, 12, 23, 24 and 25 to on all others to off		

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Figure 7-29. Optisyn Simulator Check (Sheet 9)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.85	IM	Press and release INSERT.		
29.86	IM	Observe following OUTPUT REGISTERS-REG lamps: 10, 11; 12, 23, 24 and 25 all others	 Lit Not lit	 _____ _____
29.87	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.88	IM	Observe following INPUT MULTIPLEXER display lamps: 10, 11, 12, 23, 24 and 25 all others	 Lit Not lit	 _____ _____
29.89	MT	Press and release ACCEL DL2.		
29.90	IM	Set COMD-24 to off.		
29.91	IM	Press and release INSERT.		
29.92	IM	Observe REG-24.	Not lit	_____
29.93	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.94	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____
29.95	MT	Press and release SET DA DST.		
29.96	PC	Observe DST.	Lit	_____
29.97	MT	Press and release ACCEL INHIBIT SUB.		
29.98	MT	Press and release ADVANCE six times.		

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Figure 7-29. Optisyn Simulator Check (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.99	IM	Observe REG 18 through 21.	None lit	_____
29.100	MT	Press and release ADVANCE.		
29.101	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		18 and 20	Lit	_____
		19 and 21	Not lit	_____
		all others	Not lit	_____
29.102	MT	Press and release ADVANCE six times.		
29.103	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		18 and 20	Lit	_____
		19 and 21	Not lit	_____
29.104	MT	Press and release ADVANCE.		
29.105	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		18 through 21	All lit	_____
29.106	MT	Press and release ADVANCE six times.		
29.107	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		18 through 21	All lit	_____
29.108	MT	Press and release ADVANCE.		
29.109	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		19 and 21	Lit	_____
		18 and 20	Not lit	_____

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Figure 7-29. Optisyn Simulator Check (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.110	MT	Press and release ADVANCE six times.		
29.111	IM	Observe following OUTPUT REGISTERS-REG lamps: 19 and 21 18 and 20	 Lit Not lit	 _____ _____
29.112	MT	Press and release ADVANCE.		
29.113	IM	Observe REG-18 through 21.	None lit	_____
29.114	MT	Press and release RESET DA DST.		
29.115	PC	Observe DST.	Not lit	_____
29.116	PC	Repeat steps 29.1 through 29.1.3.		
29.117	MT	Press and release ACCEL PLUS OR MINUS.		
29.118	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.119	IM	Set OUTPUT REGISTERS-COMD switches as follows: S, 1 through 12, 23 and 24 to on all others to off		
29.120	IM	Press and release INSERT.		
29.121	IM	Observe following OUTPUT REGISTERS-REG lamps: S through 12, 23 and 24 all others	 Lit Not lit	 _____ _____

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Figure 7-29. Optisyn Simulator Check (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.122	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.123	IM	Observe following INPUT MULTIPLEXER display lamps: S through 12, 23 and 24 all others	 Lit Not lit	 _____ _____
29.124	MT	Press and release ACCEL DL3.		
29.125	MT	Press and release ACCEL INHIBIT SUB.		
29.126	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.127	IM	Observe REG-22 through 25.	Lamps light and go out in following sequence: 22 23 24 25 0 0 0 0 0 1 0 1 1 1 1 1 1 0 1 0 sequence repeats.	_____
29.128	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.129	IM	Set COMP-25 to on.		
29.130	IM	Press and release INSERT.		
29.131	IM	Observe REG-25.	Lit	_____

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Figure 7-29. Optisyn Simulator Check (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.132	MT	Press and release ACCEL PLUS OR MINUS.		
29.133	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.134	IM	Observe REG-22 through 25.	Lamps light and go out in following sequence: 22 23 24 25 0 0 0 0 1 0 1 0 1 1 1 1 0 1 0 1 sequence repeats.	_____
29.135	MT	Wait for a time that no OUTPUT REGISTERS-REG lamps are lit, then press and release ACCEL INHIBIT SUB.		
29.136	IM	Observe REG-22 through REG-25.	None lit	_____
29.137	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.138	IM	Set OUTPUT REGISTERS-COMD switches as follows: 10, 11, 12, 23, 24 and 25 to on all others to off		
29.139	IM	Press and release INSERT.		
29.140	IM	Observe following OUTPUT REGISTERS-REG lamps: 10, 11, 12, 23, 24 and 25 all others	Lit Not lit	_____ _____

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Figure 7-29. Optisyn Simulator Check (Sheet 14)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.141	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.142	IM	Observe following INPUT MULTIPLEXER display lamps: 10, 11, 12, 23, 24 and 25 all others	 Lit Not lit	 _____ _____
29.143	MT	Press and release ACCEL DL3.		
29.144	IM	Set COMD-25 to off.		
29.145	IM	Press and release INSERT.		
29.146	IM	Observe REG-25.	Not lit	_____
29.147	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.148	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____
29.149	MT	Press and release SET DA DST.		
29.150	PC	Observe DST.	Lit	_____
29.151	MT	Press and release ACCEL INHIBIT SUB.		
29.152	MT	Press and release ADVANCE six times.		
29.153	IM	Observe REG-22 through 25.	None lit	_____
29.154	MT	Press and release ADVANCE.		

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Figure 7-29. Optisyn Simulator Check (Sheet 15)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.155	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		22 and 24	Lit	_____
		23 and 25	Not lit	_____
		all others	Not lit	_____
29.156	MT	Press and release ADVANCE six times.		
29.157	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		22 and 24	Lit	_____
		23 and 25	Not lit	_____
29.158	MT	Press and release ADVANCE.		
29.159	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		22 through 25	All lit	_____
29.160	MT	Press and release ADVANCE six times.		
29.161	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		22 through 25	Lit	_____
29.162	MT	Press and release ADVANCE.		
29.163	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		23 and 25	Lit	_____
		22 and 24	Not lit	_____
29.164	MT	Press and release ADVANCE six times.		

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Figure 7-29. Optisyn Simulator Check (Sheet 16)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.165	IM	Observe following OUTPUT REGISTERS-REG lamps: 23 and 25 22 and 24	 Lit Not lit	 _____ _____
29.166	MT	Press and release ADVANCE.		
29.167	IM	Observe REG-22 through 25.	None lit	_____
29.168	MT	Press and release RESET DA DST.		
29.169	PC	Observe DST.	Not lit	_____
29.170	PC	Repeat steps 29.1 through 29.1.3.		
29.171	MT	Press and release ACCEL PLUS OR MINUS.		
29.172	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.173	IM	Set all OUTPUT REGISTERS-COMD switches to on.		
29.174	IM	Press and release INSERT.		
29.175	IM	Observe OUTPUT REGISTERS-REG lamps.	All lit	_____
29.176	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.177	IM	Observe INPUT MULTIPLEXER display lamps.	All lit	_____
29.178	MT	Press and release ACCEL DL1		

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Figure 7-29. Optisyn Simulator Check (Sheet 17)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.179	MT	Press and release ACCEL DL2.		
29.180	MT	Press and release ACCEL DL3.		
29.181	IM	Set COMD-23, 24 and 25 to off.		
29.182	IM	Press and release INSERT.		
29.183	IM	Observe following OUTPUT REGISTERS-REG lamps: 23, 24 and 25	Not lit	____
29.184	MT	Press and release ACCEL INHIBIT SUB.		
29.185	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.186	IM	Observe REG-14 through 25.	Lamps light and go out as shown in Table I.	____
29.187	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.188	IM	Set COMD-23, 24 and 25 to on.		
29.189	IM	Press and release INSERT.		
29.190	IM	Observe following OUTPUT REGISTERS-REG lamps: 23, 24 and 25	Lit	____
29.191	MT	Press and release ACCEL PLUS OR MINUS.		

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Figure 7-29. Optisyn Simulator Check (Sheet 18)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.192	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.193	IM	Observe REG-14 through 25.	Lamps light and go out as shown in Table II.	_____
29.194	MT	Wait for a time that no OUTPUT REGISTERS-REG lamps are lit. then press and release ACCEL INHIBIT SUB.		
29.195	IM	Observe REG-14 through 25.	None lit	_____
29.196	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.197	IM	Set OUTPUT REGISTERS-COMD switches as follows: 10, 11, 12, 23, 24 and 25 to on all others to off		
29.198	IM	Press and release INSERT.		
29.199	IM	Observe following OUTPUT REGISTERS-REG lamps: 10, 11, 12, 23, 24 and 25 all others	 Lit Not lit	 _____ _____
29.200	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.201	IM	Observe following INPUT MULTIPLEXER display lamps: 10, 11, 12, 23, 24 and 25 all others	 Lit Not lit	 _____ _____

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Figure 7-29. Optisyn Simulator Check (Sheet 19)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.202	MT	Press and release SET DA DST.		
29.203	PC	Observe DST.	Lit	_____
29.204	MT	Press and release ACCEL DL1.		
29.205	MT	Press and release ACCEL DL2.		
29.206	MT	Press and release ACCEL DL3.		
29.207	MT	Press and release RESET DA DST.		
29.208	PC	Observe DST.	Not lit	_____
29.209	IM	Set COMD-23, 24 and 25 to off.		
29.210	IM	Press and release INSERT.		
29.211	IM	Observe following OUTPUT REGISTERS-REG lamps: 23, 24 and 25	Not lit	_____
29.212	MT	Press and release ACCEL INHIBIT SUB.		
29.213	IM	Set COMD-23, 24 and 25 to on.		
29.214	IM	Press and release INSERT.		
29.215	IM	Observe following OUTPUT REGISTERS-REG lamps: 23, 24 and 25	Lit	_____
29.216	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.217	IM	Observe REG-14 through 25.	Each very dimly lit.	_____

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Figure 7-29. Optisyn Simulator Check (Sheet 20)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.218	MT	Press and release ACCEL INHIBIT SUB.		
29.219	IM	Observe following OUTPUT REGISTERS-REG lamps: 14, 16, 18, 20, 22 and 24	All lit or none lit	_____
29.220	IM	Observe following OUTPUT REGISTERS-REG lamps: 15, 17, 19, 21, 23 and 25	All lit or none lit	_____
29.221	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.222	IM	Set COMD-23, 24 and 25 to off.		
29.223	IM	Press and release INSERT		
29.224	IM	Observe following OUTPUT REGISTERS-REG lamps: 23, 24 and 25	Not lit	_____
29.225	MT	Press and release ACCEL INHIBIT SUB		
29.226	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.227	IM	Observe REG-14 through 25.	Each very dimly lit.	_____
29.228	MT	Press and release SET DA DST		
29.229	PC	Observe DST.	Lit	_____

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Figure 7-29. Optisyn Simulator Check (Sheet 21)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.230	IM	Observe following OUTPUT REGISTERS-REG lamps: 14, 16, 18, 20, 22 and 24	All lit or none lit.	_____
29.231	IM	Observe following OUTPUT REGISTERS-REG lamps: 15, 17, 19, 21, 23 and 25	All lit or none lit	_____
29.232	MT	Press and release RESET DA DST.		
29.233	PC	Observe DST.	Not lit	_____
29.234	PC	Repeat steps 29.1 through 29.1.3.		
29.235	MT	Press and release ACCEL PLUS OR MINUS.		
29.236	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.237	IM	Set OUTPUT REGISTERS-COMD switches as follows: 9 and 22 to on all others to off		
29.238	IM	Press and release INSERT.		
29.239	IM	Observe following OUTPUT REGISTERS-REG lamps: 9 and 22 all others	Lit Not lit	_____ _____
29.240	IM	Press and release INPUT MULTIPLEXER-ALTER.		

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Figure 7-29. Optisyn Simulator Check (Sheet 22)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.241	IM	Observe following INPUT MULTIPLEXER display lamps: 9 and 22 all others	 Lit Not lit	 _____ _____
29.242	MT	Press and release ACCEL DL1.		
29.243	MT	Press and release ACCEL DL2.		
29.244	MT	Press and release ACCEL DL3.		
29.245	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.246	IM	Set OUTPUT REGISTERS-COMD switches as follows: 16, 17, 20, 21, 24 and 25 to on all others to off		
29.247	IM	Press and release INSERT.		
29.248	IM	Observe following OUTPUT REGISTERS-REG lamps: 16, 17, 20, 21, 24 and 25 all others	 Lit Not lit	 _____ _____
29.249	MT	Press and release SET DA DST.		
29.250	PC	Observe DST.	Lit	_____
29.251	MT	Press and release ACCEL INHIBIT SUB.		
29.252	IM	Observe OUTPUT REGISTERS-REG lamps.	None lit	_____
29.253	PC	Press and release POWER SUPPLY ERROR.		

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Figure 7-29. Optisyn Simulator Check (Sheet 23)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.254	MT	Press and release ACCEL PLUS OR MINUS.		
29.255	IM	Set OUTPUT REGISTERS selector switch to DIN.		
29.256	IM	Set OUTPUT REGISTERS-COMD switches as follows: 9 and 22 to on all others to off		
29.257	IM	Press and release INSERT.		
29.258	IM	Observe following OUTPUT REGISTERS-REG lamps: 9 and 22	Lit	_____
29.259	IM	Press and release INPUT MULTIPLEXER-ALTER.		
29.260	IM	Observe following INPUT MULTIPLEXER display lamps: 9 and 22 all others	Lit Not lit	_____ _____
29.262	MT	Press and release ACCEL DL1.		
29.262	MT	Press and release ACCEL DL2.		
29.263	MT	Press and release ACCEL DL3.		
29.264	IM	Set OUTPUT REGISTERS selector switch to OPTISYN.		
29.265	IM	Set OUTPUT REGISTERS-COMD switches as follows: 14, 15, 18, 19, 22 and 23 to on all others to off.		

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Figure 7-29. Optisyn Simulator Check (Sheet 24)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
29.266	IM	Press and release INSERT.		
29.267	IM	Observe following OUTPUT REGISTERS-REG lamps:		
		14, 15, 18, 19, 22 and 23	Lit	_____
		all others	Not lit	_____
29.268	MT	Press and release SET DA DST.		
29.269	PC	Observe DST.	Lit	_____
29.270	MT	Press and release ACCEL INHIBIT SUB.		
29.271	IM	Observe OUTPUT REGISTERS-REG lamps.	All lit	_____

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Figure 7-29. Optisyn Simulator Check (Sheet 25)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

	14	15	16	17	18	19	20	21	22	23	24	25
1.	0	0	0	0	0	0	0	0	0	0	0	0
2.	0	1	0	1	0	1	0	1	0	1	0	1
3.	1	1	1	1	1	1	1	1	1	1	1	1
4.	1	0	1	0	1	0	1	0	1	0	1	0

5. (sequence repeats)

Table II

	14	15	16	17	18	19	20	21	22	23	24	25
1.	0	0	0	0	0	0	0	0	0	0	0	0
2.	1	0	1	0	1	0	1	0	1	0	1	0
3.	1	1	1	1	1	1	1	1	1	1	1	1
4.	0	1	0	1	0	1	0	1	0	1	0	1

5. (sequence repeats)

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Figure 7-29. Optisyn Simulator Check (Sheet 26)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.0		DC Adjustments.		
EXP.		This procedure contains the adjustments necessary to ensure correct voltage from each of the ETS power supplies. Voltages are monitored at LVDAME PC panel test points, and adjustments are made at the power supply and/or the PC panel remote programming potentiometers.		
1.1	ETS	Rotate CURRENT ADJUST on PS1 (+28I supply) fully clockwise.		
1.2	ETS	Rotate CURRENT ADJUST and CURRENT VERNIER on PS2 (-26.5V supply) fully clockwise.		
1.3	ETS	Rotate CURRENT ADJUST and CURRENT VERNIER on PS3 (+28DA supply) fully clockwise.		
1.4	ETS	Rotate CURRENT ADJUST on PS4 (+6I supply) fully clockwise.		
1.5	ETS	Rotate CURRENT ADJUST on PS5 (-3V supply) fully clockwise.		
1.6	PC	Press and release POWER ON		
1.7	PC	Observe following lamps: POWER ON POWER OFF DC OFF	 Lit Not lit Lit	 _____ _____ _____
1.8	PC	Press and release DC ON.		
1.9	PC	Observe following lamps: DC ON DC OFF	 Lit Not lit	 _____ _____

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Figure 7-30. DC Adjustments (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
1.10	PC	Measure voltages at test points listed in Table I. If any voltages are out of tolerance, rotate control specified in Table I until voltage is within tolerance.	Refer to Table I.	
1.11	PC	Press and release DISCRETE CONTROL- +8VDC.		
1.12	PC	Observe following DISCRETE CONTROL lamps: +8VDC +28VDC	 Lit Not lit	 _____ _____
1.13	PC	Measure voltage at +28I test points. If voltage is not +8.0(±0.08) V, adjust 02A6 R2 (located at back of PC panel).		
1.14	PC	Press and release DISCRETE CONTROL +16VDC.		
1.15	PC	Observe following DISCRETE CONTROL lamps: +16VDC +8VDC	 Lit Not lit	 _____ _____
1.16	PC	Measure voltage at +28I test points. If voltage is not +16.0 (±0.160) V, adjust 02A6 R1 (located at back of PC panel).		

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Figure 7-30. DC Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: | UNIT NO.

Table I

Test Point (PC Panel)	Voltage and Tolerance	Adjustment
-26.5	-26.5(±.265) V	-26.5VDC control (PC Panel)
+28DA	+28.0 (±.280) V	D A +28VDC control (PC Panel)
+6I	+6.0 (±.060) V	+6VDC control (PC Panel)
-3	-3.0 (±.030) V	-3VDC control (PC Panel)
+28I	+28.0 (.280) V	+28I control (PC Panel)
+12	+12.0 (±120) V	VOLTAGE ADJUST (02A1 PS1)
-12A	-12.0 (±120) V	VOLTAGE ADJUST (02A8 PS1)
-12B	-12.0 (±120) V	VOLTAGE ADJUST (02A1 PS2)
-12C	-12.0 (±120) V	VOLTAGE ADJUST (02A8 PS2)
-6	-6.0 (±.060) V	VOLTAGE ADJUST (02A7 PS1)
-36	-36.0 (±.360) V	VOLTAGE ADJUST (02A7 PS2)

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Figure 7-30. DC Adjustments (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: UNIT NO.

Step	Panel	Operation	Normal Indication	Data
2.0		Data Adapter Control.		
EXP		This procedure contains all the single-shot adjustments for the LVDA control section of the LVDAME.		
2.1	IM	Set OPERATING MODE to MAN TEST.		
2.2	ST	Set MANUAL D A POWER CONTROL to FREE RUN.		
2.3	PC	Verify that INITIAL SEQ. FULL ERROR, FULL SEQ and SEQ OFF sequentially light and go out.		
2.4		Open gate 02B3 and observe signals at each test point listed in tests 1 through 26 of Table I. If a pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width settings in Data column of Table I. Note All up levels are 0 V and all down levels are -6 V. Pulse widths are measured at the 50% points and all pulses are negative.	Refer to Operation column.	Record data on Table I.
2.5		Connect jumper between 02B3 E24H and 02B3 E24J.		
2.6		Perform test 27 of Table I.	Refer to Operation column, step 2.4.	

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Figure 7-31. Data Adapter Control Adjustments (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES -

UNIT NAME: | UNIT NO.

Table I

Test	Gate 02B3 Test Point	* Signal Name	ALD Ref. Page	Pulse Width	Data
1	D11B	SS 1	05.12.21.1	120 (±6)MS	
2	C24B	SS 2	05.12.21.1	125 (±6)MS	
3	D23B	SS 3	05.12.21.1	320 (±15)MS	
4	F07B	SCPSO	05.12.13.1	1.0 (±0.1)MS	
5	A15B	Half Intl Seq	05.12.13.1	10 (±2) us	
6	B13B	Half Fl.ll Seq	05.12.13.1	10 (±2)us	
7	A19B	HLTA Sel 1	05.12.16.1	3.0 (±0.2)MS	
8	D19B	MEM REL	05.12.16.1	6.0 (±1)MS	
9	C18B	MEM REL NOT	05.12.15.1	3.0 (±0.2)MS	
10	C22B	Test INH Set	05.12.20.1	10 (±2)us	
11	B26B	Sel 2	05.12.18.1	3.0 (±0.2)MS	
12	E25B	50 MS Delay	05.12.18.1	52.5 (±2.5)MS	
13	C20B	Rel Con	05.12.18.1	3.0 (±0.2)MS	
14	D21B	MEM CON	05.12.17.1	16.5 (±1.5)MS	
15	B20B	MEM Short Set	05.12.17.1	3.0 (±0.2)MS	
16	A26B	ERR Reset 2	05.12.18.1	11 (±1)MS	
17	D26B	END Seq Up	05.12.18.1	10 (±2)us	
18	C12B	HLT B Sel 1	05.12.16.1	3.0 (±0.2)MS	
19	A17B	SC POWER OFF	05.12.15.1	9.0 (±1)MS	

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Figure 7-31. Data Adapter Control Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: | UNIT NO.

Table 1 (cont)

Test	Gate 02B3 Test Point	* Signal Name	ALD Ref. Page	Pulse Width	Data
20	B18B	Turn PW OFF	05.12.15.1	10 (±2)us	
21	A23B	End Seq DM Delay	05.12.24.1	100 (±10)MS	
22	B23B	End Seq Dn	05.12.24.1	10 (±2)us	
23	E04B	Initial Test Reset	05.12.09.1	3.0 (±0.2)us	
24	F13B	Test Reset	05.12.09.1	11 (±1)MS	
25	F14B	Test Set	05.12.09.1	11 (±1)MS	
26	F15B	Test Set sample	05.12.34.1	10 (±2)us	
27	F16B	Intrpt 15	05.12.34.1	10 (±2)us	

* All names listed under SIGNAL NAME will not be listed in the ALDs. Names were given to every single-shot to help define its function.

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Figure 7-31. Data Adapter Control Adjustments (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
2.7		Remove jumper inserted in step 2.5.		
2.8		Close gate 02B3.		
2.9		Set MANUAL D A POWER CONTROL to NORMAL.		
2.10		Press POWER SUPPLY ERROR.		
2.11		Open gate 02B2.		
2.12		Alternately press CHANNEL SELECT COMD and TMR while observing signals at each point listed in Table II. If a pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width settings in Data column of Table II.	Refer to Operation column.	Record data on Table II.
2.13		Close gate 02B2.		

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Figure 7-31. Data Adapter Control Adjustments (Sheet 4)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: UNIT NO.

Table 2

Test	Gate 02B3 Test Point	* Signal Name	ALD Ref. Page	Pulse Width	Data
1	E15B	Leading Edge HALTV INH	05.02.03.1	5.0 (±1)us	
2	E15B	Trailing Edge HALTV INH	05.02.03.1	5.0 (±1)us	
3	B11B	Initiate CK	05.12.28.1	10 (±2)us	
4	A12B	ON Delay 1	05.12.28.1	140 (+5, -2)MS	
5	A14B	Reset Delay 1 Latch	05.12.28.1	10 (±2)us	
6	B13B	ON Delay 2	05.12.28.1	180 (+5, -2)MS	
7	B15B	Set Delay 2 latch	05.12.28.1	10 (±2)us	
8	A10B	ON Delay 3	05.12.30.1	1.0 (±0.2)MS	
9	A16B	Set Delay 3 latch	05.12.30.1	10 (±2)us	
10	B09B	ON Delay 4	05.12.30.1	170 (±5)MS	
11	B17B	Reset Delay 4 latch	05.12.30.1	10 (±2)us	
12	A11B	ON Delay 5	05.12.31.1	157 (±5)MS	
13	A17B	Set Delay 5 latch	05.12.31.1	10 (±2)us	
14	D25B	OFF SEQ Delay 1	05.12.33.1	3.0 (±0.5)us	
15	B19B	Set OFF Delay latch	05.12.33.1	10 (±2)us	
16	B23B	OFF SEQ Delay 2	05.12.33.1	285 (±5)MS	
17	B20B	Reset OFF Delay latch	05.12.33.1	10 (±2)us	
18	D25B	OFF SEQ Delay 3	05.12.33.1	188 (±5)MS	
19	A21B	DAPS Not Sample	05.12.33.1	11 (±1)us	
20	A24B	OFF SEQ Delay 4	05.12.33.1	6.5 (±1.5)MS	
21	A20B	Mem 20 Sample	05.12.33.1	10 (±2)us	
22	E18B	6S INH	05.22.03.1	100 (±10)MS	

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Figure 7-31. Data Adapter Control Adjustments (Sheet 5)

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
3.0		Output Registers Insert Single-Shot Adjustment.		
EXP.		This procedure describes the adjustment of the output registers insert single-shot.		
3.1		Open gate 01A6.		
3.2		Connect oscilloscope probe to 01A6 F14B. (Use INTERNAL - trigger.)		
3.3		Press OUTPUT REGISTERS-INSERT switch while observing oscilloscope display. (Repeat if necessary) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 5(±1)MS pulse each time INSERT is pressed.	_____
3.4		Connect oscilloscope probe to 01A6 F13B. (Use INTERNAL - trigger.)		
3.5		Press OUTPUT REGISTERS-INSERT switch while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 5(±1)MS pulse each time INSERT is pressed.	_____
3.6		Close gate 01A6.		

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Figure 7-32. Output Register Insert Single-Shot Adjustment

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
4.0		TSYNC and GCSYNCX Single-Shot Adjustment.		
EXP.		This procedure describes the TSYNC and GCSYNCX single-shot adjustment.		
4.1		Open gate 01A6.		
4.2		Connect oscilloscope probe to 01A6 F06B. (Use INTERNAL - trigger.)		
4.3	MT	Press SAMPLE RESET switch while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 4.0 (±0.1)MS pulse each time SAMPLE RESET is pressed.	_____
4.4		Connect oscilloscope probe to 01A6 F07B. (Use INTERNAL - trigger.)		
4.5	MT	Press SAMPLE RESET switch while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 192 (±10)μs pulse each time SAMPLE RESET is pressed.	_____
4.6	IM	Set OUTPUT REGISTERS selector switch to DIN.		
4.7	IM	Set OUTPUT REGISTERS-COMD switches as follows: S to on all others to off		

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Figure 7-33. TSYNC and GCSYNCX Adjustments (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
4.8	IM	Press INSERT.		
4.9	IM	Observe following OUTPUT REGISTERS-REG lamps: S all others	 Lit Not lit	 _____ _____
4.10		Connect oscilloscope probe to 01A6 F08. (Use INTERNAL - trigger.)		
4.11	MT	Press TEL SAMPLE while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 500 (±25) μs pulse each time TEL SAMPLE is pressed.	_____
4.12		Close gate 01A6.		

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Figure 7-33. TSYNC and GCSYNCX Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES–				
UNIT NAME:			UNIT NO.	
Step	Panel	Operation	Normal Indication	Data
5.0		Input Multiplexer Alter Single-Shot Adjustment.		
EXP.		This procedure describes the adjustment of the input multiplexer alter single-shot.		
5.1		Open gate 01A8.		
5.2		Connect oscilloscope probe to 01A8 F17B. (Use INTERNAL - trigger.)		
5.3	IM	Press INPUT MULTIPLEXER-ALTER while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 5 (±1)μs pulse each time ALTER is pressed.	_____
5.4		Connect oscilloscope probe to 01A8 F14B. (Use INTERNAL - trigger.)		
5.5	IM	Press INPUT MULTIPLEXER-ALTER while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 5 (±1) μs pulse each time ALTER is pressed.	_____
5.6		Close gate 01A8.		

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Figure 7-34. Input Multiplexer Alter Single-Shot Adjustment

INTERNATIONAL BUSINESS MACHINES—				
UNIT NAME:				UNIT NO.
Step	Panel	Operation	Normal Indication	Data
6.0		A/D Multiplexer Trigger Adjustment.		
EXP.		This procedure describes the adjustment of the A/D Multiplexer trigger.		
6.1	MT	Set ADDRESS REGISTER-COMMAND switches as follows: A1 and A2 to on all others to off		
6.2	MT	Set REPEAT to on.		
6.3		Open gate 01B6.		
6.4		Connect oscilloscope probe to 01B6 A16A. (Use INTERNAL - trigger.)		
6.5	MT	Press and hold CIO.		
6.6		Observe oscilloscope display. If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-12 V 5 (±1)MS pulses.	_____
6.7	MT	Release CIO.		
6.8		Close gate 01B6.		

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Figure 7-35. A/D Multiplexer Trigger Adjustment

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
7.0		Resolver Simulater Adjustment.		
EXP.		This procedure describes the adjustment of the resolver simulator single-shots.		
7.1		Set ADDRESS REGISTER-COMMAND switches as follows: A1, A2, A3 and A4 to on all others to off		
7.2		Open gate 01B7.		
7.3		Connect oscilloscope probe to 01B7 D09B. (Use INTERNAL - trigger.)		
7.4	MT	Press CIO while observing oscilloscope display. (Repeat if necessary.) If pulse width is not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V, 25 (±3)MS pulse each time CIO is pressed.	_____
7.5		Connect oscilloscope probe to 01B7 D10B. (Use INTERNAL - trigger.)		
7.6	MT	Press CIO while observing oscilloscope display. (Repeat is necessary.) If pulse widths are not within tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	Two -6 V, 1.5(±0.5)MS pulses each time CIO is pressed.	_____

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Figure 7-36. Resolver Simulator Adjustments (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: | UNIT NO.

Step	Panel	Operation	Normal Indication	Data
7.7	•	Connect oscilloscope probe to 01B7 D11B. (Use INTERNAL - trigger.)		
7.8	MT	Press CIO while observing oscilloscope display. (Repeat if necessary. If pulse width is not width tolerance, adjust single-shot on card for nominal pulse width. Record final pulse width in Data column.	-6 V 1.5 (±0.5)MS each time CIO is pressed.	_____
7.9		Close gate 01B7.		

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Figure 7-36. Resolver Simulator Adjustments (Sheet 2)

SECTION VIII

TROUBLE ISOLATION

8-1. SCOPE.

8-2. This section describes the basic operations involved in isolating trouble in the LVDAME. (General trouble isolating procedures keyed to the calibration procedures will be supplied in revisions to this basic manual.)

8-3. BASIC TROUBLE SHOOTING PROCEDURE.

8-4. ANALYSIS.

8-5. When an LVDAME malfunction is discovered, the pertinent calibration procedures in Section VII should be performed to localize the malfunction to a particular functional unit of the LVDAME.

8-6. When the malfunctioning unit has been determined, analyze its circuits with the aid of the Second Level Logic and Electrical Schematic Diagrams in Section X and the circuit descriptions in Section II. Reference is made from the Second Level Logic Diagrams to the Automated Logic Diagrams (ALD's) by the "LN" numbers of the ALD sheets. The ALD's show the point-to-point wiring of the gate assemblies; circuit points for testing signal levels can be determined from these diagrams. Reference is also made between the ALD's and the Electrical Schematic Diagrams by "LN" numbers.

NOTE

Descriptions of the format and contents of these types of diagrams are given in Section X. The format of the "LN" numbers is also explained in Section X.

8-7. PROBING GATE ASSEMBLIES.

8-8. Signal levels of the gate assembly circuits can be observed by probing the pins of the SMS card receptacles. (The logic blocks on the ALD's specify the pins used for logic signals and the locations of the cards (and receptacles) in the gate assemblies.)

CAUTION

To prevent damage to the equipment, take care to locate the correct pins while probing a gate assembly.

8-9. Figure 8-1 shows the SMS card receptacle pin arrangement on the wiring side of a gate assembly; the gate assembly is shown in its extended or open position.

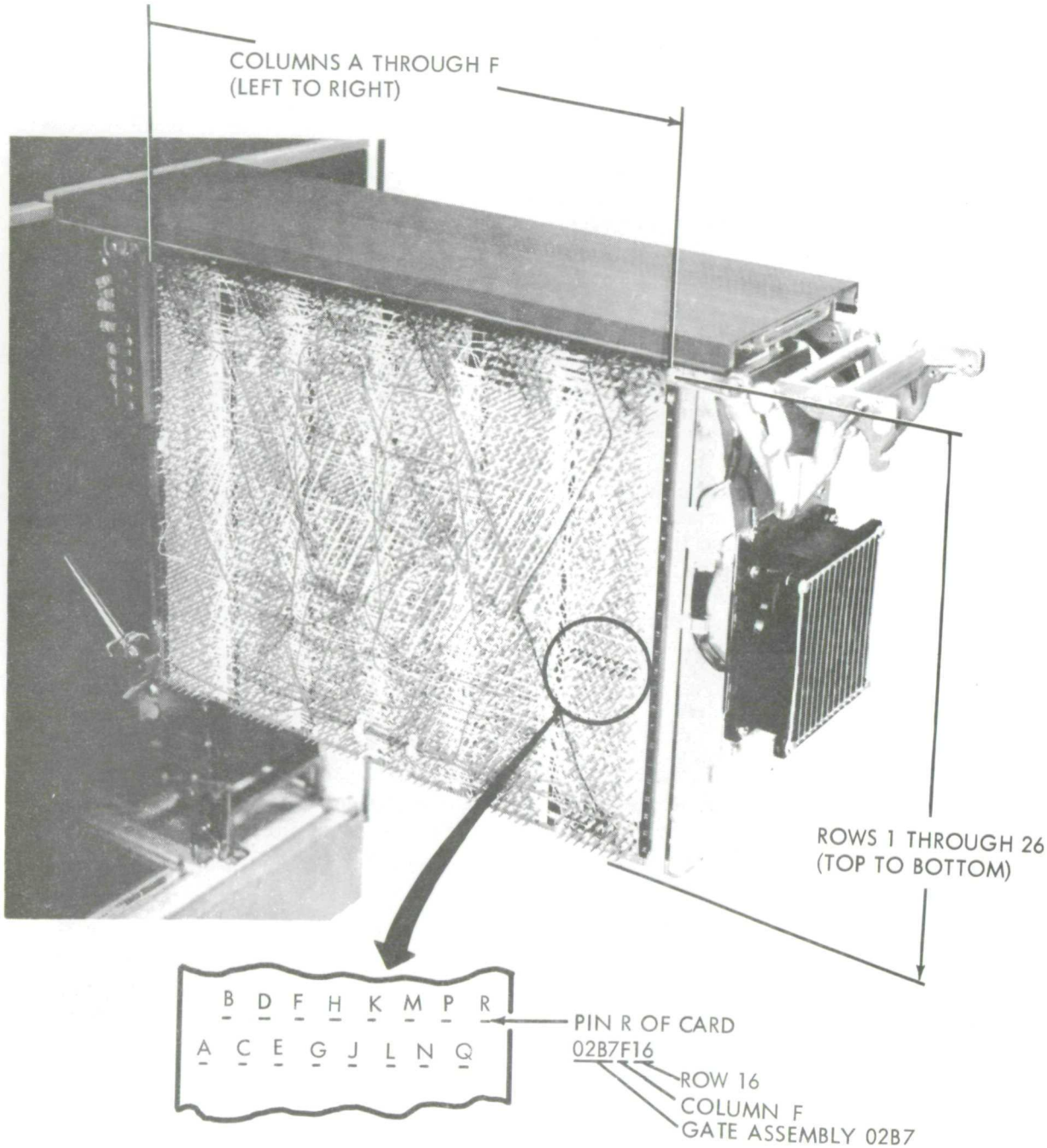


Figure 8-1. SMS Card Location and Pin Arrangement in Gate Assemblies

8-10. TROUBLE SHOOTING SMS CARDS.

8-11. Except for the special printed circuit board assemblies (figure 9-4), SMS cards are considered nonreparable and should be replaced by a new card when a failure occurs. If a special printed circuit board assembly (card) is determined to be faulty, the card should be checked to determine the faulty component. To check the card circuits:

a. Turn off LVDAME power.

b. Pull the card from its receptacle (use SMS Card Puller, IBM part number 6072429, shown on figure 4-4, part A).

c. Insert Card Extender (IBM part number 6072431, shown on figure 4-4, part C) into the card receptacle.

d. Insert the card into the Card Extender, and apply power to the LVDAME.

With the aid of the special card schematic diagrams (figures 10-58 through 10-79) the defective card component can be determined; the card should then be repaired as described in Section IX.

SECTION IX

REPAIR

9-1. SCOPE.

9-2. This section contains the (1) lists of replaceable LVDAME assemblies and parts and (2) discussions of recommended methods for replacement and repair of these assemblies and parts. The applications of many of the special tools listed and illustrated in Section IV are described in these discussions.

9-3. This section also contains a list of recommended materials for repainting the LVDAME exterior surfaces and a description of recommended methods for repainting these surfaces.

9-4. REPLACEABLE ASSEMBLIES AND PARTS.

9-5. Figure 9-1 lists the major LVDAME assemblies that contain replaceable parts.

NOTE

The vendor codes used on figures in this section are taken from the Federal Supply Code for Manufacturers, Cataloging Handbook H4-1. Figure 9-17 serves as a cross-reference for vendors and their codes.

9-6. GATE ASSEMBLIES.

9-7. Each gate assembly (listed in figure 9-1) contains a replaceable fan assembly (IBM part number 480991, vendor code 88360) which circulates cooling air over the logic circuits in the gate assembly. A fan assembly is mounted at the bottom of each gate assembly in the lower half of the LVDAME and at the top of each gate assembly in the upper half of the LVDAME.

9-8. The SMS cards and edge connectors for each gate assembly are specified on the Circuit Card Location Charts and Edge Connector Lists. The part numbers and "LN" numbers of these charts and lists are shown in figures 9-2 and 9-3. Refer to Section X for the discussion of these charts and lists and the explanation of the "LN" numbers.

9-9. PRINTED CIRCUIT BOARD (SMS CARD) ASSEMBLIES. The special SMS cards listed in figure 9-4 are repairable assemblies. All electrical components and spacers (pads) for transistor mountings on these special cards are replaceable parts. The part numbers and the locations of the parts on the special SMS cards are shown on the Printed Circuit Board Assembly drawings (figures 10-58 and 10-79).

NOTE

All other single SMS cards in the LVDAME are considered nonrepairable and should be replaced by a new card when a failure occurs.

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
01A1	Interface Monitoring Panel Assembly	Refer to figure 9-5	03640
01A2	Manual Test Panel Assembly	Refer to figure 9-6	03640
01A3	Data Adapter Interface Panel Assembly	Refer to figure 9-7	03640
01A4	Self Test Panel Assembly	Refer to figure 9-8	03640
01A6	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01A7	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01A8	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B1	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B2	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B3	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B4	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B5	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B6	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B7	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
01B8	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
02A1	Power Supply Assembly	Refer to figure 9-10	03640
02A2	A/D Converter	VR13-AB/NE	11359
02A3	Multiplexer	VMX40B/VMX8DB	11359
02A6	Power Control Panel Assembly	Refer to figure 9-11	03640
02A7	Power Supply Assembly	Refer to figure 9-12	03640
02A8	Power Supply Assembly	Refer to figure 9-13	03640
02B1	Power Supply Assembly	Refer to figure 9-14	03640
02B2	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
02B3	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640

Figure 9-1. Replaceable LVDAME Assemblies (Sheet 1 of 2)

Reference Designation	Nomenclature	Manufactuere's Part Number	Vendor Code
02B4	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
02B5	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
02B6	Relay Chassis Assembly	Refer to figure 9-15	03640
02B7	Gate Assembly	Refer to figures 9-2, 9-3, and 9-4	03640
02B8	AC Power Box Assembly	Refer to figure 9-16	03640

Figure 9-1. Replaceable LVDAME Assemblies (Sheet 2)

Gate Assembly	IBM Part Number	"LN" Number	Number of Sheets
01A6	6942709	01.01.01.0	2
01A7	6942809	01.01.02.0	3
01A8	6942909	01.01.03.0	3
01B1	6940209	01.01.11.0	3
01B2	6940309	01.01.12.0	2
01B3	6940409	01.01.13.0	3
01B4	6940509	01.01.14.0	3
01B5	6940609	01.01.15.0	2
01B6	6940709	01.01.16.0	3
01B7	6940809	01.01.17.0	3
01B8	6940909	01.01.18.0	3
02B2	6941309	02.01.11.0	2
02B3	6941409	02.01.12.0	2
02B4	6941509	02.01.13.0	2
02B5	6941609	02.01.14.0	3
02B7	6941809	02.01.15.0	3

Figure 9-2. List of LVDAME Circuit Card Location Charts

Gate Assembly	IBM Part Number	"LN" Number	Number of Sheets
01A6	6942710	01.02.01.0	5
01A7	6942810	01.02.02.0	4
01A8	6942910	01.02.03.0	4
01B1	6940210	01.02.11.0	3
01B2	6940310	01.02.12.0	3
01B3	6940410	01.02.13.0	3
01B6	6940510	01.02.14.0	2
01B7	6940610	01.02.15.0	3
01B8	6940710	01.02.16.0	4
02B2	6940810	01.02.17.0	3
02B3	6940910	01.02.18.0	5
02B4	6941310	02.02.11.0	4
02B5	6941410	02.02.12.0	3
02B4	6941510	02.02.13.0	5
02B5	6941610	02.02.14.0	2
02B7	6941810	02.02.15.0	2

Figure 9-3. List of LVDAME Edge Connector Lists

Vendor Code	Part Number	Nomenclature	Assembly Drawing
03640	6901030	Relay Card	10-58
03640	6901330	AN1 Translator	10-59
03640	6901342	NA2 Translator	10-60
03640	6901349	3.6 K Resistor	10-61
03640	6901352	2.048 MC Oscillator	10-62
03640	6901356	CD1	10-63
03640	6901358	SC3	10-64
03640	6942024	ODL1	10-65
03640	6942026	OTO6	10-66
03640	6942028	OT28	10-67
03640	6942030	OTO2	10-68
03640	6942032	OTO3	10-69
03640	6942033	OTO4	10-70

Figure 9-4. Repairable Printed Circuit Board (SMS Card) Assemblies (Sheet 1 of 2)

Vendor Code	Part Number	Nomenclature	Assembly Drawing
03640	6942036	OVD1	10-71
03640	6942037	OCD2	10-72
03640	6942038	ORD1	10-73
03640	6942040	OTO5	10-74
03640	6942042	OSS1	10-75
03640	6942044	OMCR	10-76
03640	6942045	OSTT	10-77
03640	6942047	OTDL	10-78
03640	6942049	OTSD	10-79

Figure 9-4. Repairable Printed Circuit Board (SMS Card) Assemblies (Sheet 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
DS1 thru DS88	Lamp	6078990	03640
S1 thru S26	Switch (Light Module 6080637)	6078529	03640
S27	Switch (Light Module 6079732)	6078534	03640
S28	Rotary Switch	6081131	03640
S29, S30	Switch (Light Module 6079732)	6078534	03640
S31	Rotary Switch	6081131	03640
S32, S33	Switch (Light Module 6079732)	6078534	03640
S34	Switch (Light Module 6079731)	6078534	03640
S35, S36	Switch (Light Module 6079732)	6078534	03640
S37	Switch (Light Module 6079733)	6078534	03640
S38 thru S40	Switch (Light Module 6079732)	6078534	03640
S41	Rotary Switch	6035436	03640
S42	Switch (Light Module 6079730)	6078529	03640
XDS29 thru XDS41	Light Module	6081044	03640
XDS44 thru XDS65	Light Module	6078416	03640
XDS66 thru XDS69	Light Module	6079732	03640
XDS70	Light Module	6078416	03640
XDS71 thru XDS88	Light Module	6081044	03640
Note: Use switch housing part number 6078442 and screen 6078943 for all switches except S28, S31, and S41. Refer to figure 10-51 when replacing parts.			

Figure 9-5. Interface Monitoring Panel (01A1) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
DS1 thru DS53	Lamp	6078990	03640
S1 thru S8	Switch (Light Module 6079720)	6078529	03640
S9 thru S16	Switch (Light Module 6079732)	6078534	03640
S17	Switch (Light Module 6079732)	6078529	03640
S18 thru S27	Switch (Light Module 6079732)	6078534	03640
S29	Switch (Light Module 6079727)	6078534	03640
S30	Switch (Light Module 6079718)	6078534	03640
S31	Switch (Light Module 6079732)	6078534	03640
S32 thru S36	Switch (Light Module 6079730)	6078534	03640
S37, S38	Switch (Light Module 6079718)	6078534	03640
S39	Switch (Light Module 6079730)	6078529	03640
XDS31	Light Module	6079718	03640
XDS32 and XDS33	Light Module	6078415	03640
XDS34	Light Module	6079718	03640
XDS35	Light Module	6078415	03640
XDS37	Light Module	6079732	03640
XDS38	Light Module	6079718	03640
XDS39	Light Module	6079720	03640
XDS40 thru XDS42	Light Module	6079718	03640
XDS43	Light Module	6079720	03640
XDS49 and XDS52	Light Module	6081058	03640
TP1 thru TP75	Test Point	6015339	03640
TP76 thru TP80	Test Point	6015537	03640

Notes: Use switch housing part number 6078442 and screen 6078943 for all switches. Refer to figure 10-52 when replacing parts

Figure 9-6. Manual Test Panel (01A2) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
TP1-A thru TP6-G	Test point	6015339	03640
TP6-H	Test point	6015537	03640
TP7-A thru TP12-G	Test point	6015339	03640
TP12-H	Test point	6015537	03640
TP13-A thru TP15-G	Test point	6015339	03640
TP15-H	Test point	6015537	03640
TP16-A thru TP17-G	Test point	6015339	03640
TP17-H	Test point	6015537	03640
TP18-A thru TP23-G	Test point	6015339	03640
TP23-H	Test point	6015537	03640
TP24-A thru TP27-G	Test point	6015339	03640
TP27-H	Test point	6015537	03640
TP28-A thru TP33-G	Test point	6015339	03640
TP33-H	Test point	6015537	03640
TP34-A thru TP36-G	Test point	6015339	03640
TP36-H	Test point	6015537	03640
TP37-A thru TP39-G	Test point	6015339	03640
TP39-H	Test point	6015537	03640
TP40-A thru TP41-G	Test point	6015339	03640
TP41-H	Test point	6015537	03640
TP42-A thru TP328-H	Test point	6015339	03640
Note: Refer to figure 10-53 when replacing parts			

Figure 9-7. Data Adapter Interface Panel (01A3) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
S1	Rotary Switch	6081375	03640
S2	Rotary Switch	6035431	03640
S3, S4	Rotary Switch	6035435	03640
S5 thru S8	Toggle Switch	6034112	03640
TP1 thru TP5	Test Point	6015339	03640
TP6	Test Point	6015537	03640
TP7	Test Point	6015339	03640
NA	Terminal Lug	6013350	03640
NA	Knob (for S1 thru S4)	6072801	03640
Note: Refer to figure 10-54 when replacing parts.			

Figure 9-8. Self Test Panel (01A4) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
C1 thru C16	Capacitor	6081445	03640
R1	Resistor	6081162	03640
R2	Resistor	6081438	03640
R3	Resistor	6081441	03640
R4	Resistor	6081163	03640
R5, R6	Resistor	6081442	03640
R7	Resistor	6081164	03640
R8	Resistor	6081439	03640
R9	Resistor	6081440	03640
R10	Resistor	6081443	03640
TB1R1 thru TB1R10	Resistor	6011557	03640
Note: Refer to figure 10-55 when replacing parts.			

Figure 9-9. Resistor-Capacitor Assembly (01A10) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
B1	Fan Assembly	480991	88360
NA	Printed Circuit Board Assembly	370576	88360
NA	Printed Circuit Board Assembly	370610	88360
NA	Lug Terminal	6034213	03640

Figure 9-10. Power Supply Assembly (02A1) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
DS1 thru DS42	Lamp	6078990	03640
R1, R2	Resistor	6081062	03640
R3	Resistor	6081061	03640
R4	Resistor	6081064	03640
R5	Resistor	6078360	03640
R6	Resistor	6081063	03640
R7	Resistor	6078360	03640
R8	Resistor	6081068	03640
R9	Resistor	6081065	03640
R10	Resistor	6081067	03640
R11	Resistor	6081066	03640
S1	Switch (Light Module 6080638)	6078534	03640
S2	Switch (Light Module 6078415)	6078534	03640
S3	Switch (Light Module 6079733)	6078534	03640
S4 thru S7	Switch (Light Module 6079732)	6078534	03640
S8 thru S10	Switch (Light Module 6080638)	6078534	03640
S11	Switch (Light Module 6079732)	6078534	03640
S12 thru S14	Switch (Light Module 6079726)	6078534	03640
S15 thru S19	Switch (Light Module 6079732)	6078534	03640
S20 thru S23	Switch (Light Module 6079720)	6078534	03640
S24	Rotary Switch	6035436	03640
S25 thru S27	Switch (Light Module 6079732)	6078534	03640
S28	Rotary Switch	6035431	03640
S29	Switch (Light Module 6079732)	6078534	03640
S30	Switch (Light Module 6079733)	6078534	03640
S31	Switch (Light Module 6079730)	6078529	03640
S32 thru S34	Rotary Switch	6035437	03640
S35	Switch	482219	88360
TB1CR1	Diode	6018033	03640
TB1R1 thru TB1R13	Resistor	6011557	03640
TB1R14 thru TB1R23	Resistor	6078566	03640
TB1R24 thru TB1R28	Resistor	6011557	03640

Figure 9-11. Power Control Panel (02A6) Replaceable Parts (Sheet 1 of 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
TP1	Test Point	6015537	03640
TP2	Test Point	6015339	03640
TP3	Test Point	6015537	03640
TP4	Test Point	6015339	03640
TP5	Test Point	6015537	03640
TP6	Test Point	6015339	03640
TP7	Test Point	6015537	03640
TP8	Test Point	6015339	03640
TP9	Test Point	6015537	03640
TP10	Test Point	6015339	03640
TP11	Test Point	601537	03640
TP12	Test Point	6015339	03640
TP13	Test Point	601537	03640
TP14	Test Point	6015339	03640
TP15	Test Point	601537	03640
TP16	Test Point	6015339	03640
TP17	Test Point	601537	03640
TP18 thru TP20	Test Point	6015339	03640
TP21	Test Point	601537	03640
TP22 thru TP24	Test Point	6015339	03640
TP25	Test Point	601537	03640
TP26 thru TP28	Test Point	6015339	03640
XDS8	Light Module	6079718	03640
XDS16 thru XDS19	Light Module	6079281	03640
XDS20 thru XDS24	Light Module	6079730	03640
XDS26	Light Module	6079731	03640
XDS40 and XDS41	Light Module	6078419	03640
NA	Knob for S24, S28, S32, S33 and S34	6072801	03640

Notes: Use switch housing part number 6078442 and screen 6078943 for all switches except S24, S28, and S32 thru S35. Refer to figure 10-56 when replacing parts.

Figure 9-11. Power Control Panel (02A6) Replaceable Parts (Sheet 2 of 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
B1	Fan Assembly	480991	88360
NA	Printed Circuit Board Assembly	370575	88360
NA	Printed Circuit Board Assembly	370576	88360
NA	Printed Circuit Board Assembly	370609	88360
NA	Printed Circuit Board Assembly	370612	88360
NA	Lug Terminal	6029426	03640

Figure 9-12. Power Supply Assembly (02A7) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
B1	Fan Assembly	480991	88360
NA	Printed Circuit Board Assembly	370576	88360
NA	Printed Circuit Board Assembly	370610	88360
NA	Lug Terminal	6034213	03640

Figure 9-13. Power Supply Assembly (02A8) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
NA	Lug Terminal	6029799	03640
NA	Lug Terminal	6033229	03640
NA	Lug Terminal	6034213	03640

Figure 9-14. Power Supply Assembly (02B1) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
K1 thru K9	Relay	6081176	03640
K10	Relay	6081173	03640
K11	Relay	6078430	03640
K12	Relay	6081173	03640
K13 thru K18	Relay	6078148	03640
K19 thru K23	Relay	6081174	03640
TB1CR1 thru TB1CR11	Diode	6018033	03640
TB1R1	Resistor	6081665	03640
TB1R2	Resistor	6081666	03640
TB1R3	Resistor	6081665	03640
TB1R4	Resistor	6081666	03640
TB1R5	Resistor	6081665	03640
TB1R6	Resistor	6081666	03640
TB1R7	Resistor	6081667	03640
TB1R8	Resistor	6081668	03640
TB1R9	Resistor	6081669	03640
TB1R10	Resistor	6081670	03640
TB1R11	Resistor	6081671	03640
TB2R1	Resistor	6081675	03640
TB2R2	Resistor	6082076	03640
TB2R3	Resistor	6082075	03640
TB2R4 thru TB2R6	Resistor	6081672	03640
TB2R7	Resistor	6081673	03640
XK1 thru XK9	Socket	6081364	03640
XK10 thru XK12	Socket	6013283	03640
XK13 thru XK23	Socket	6078153	03640

Figure 9-15. Relay Chassis Assembly (02B6) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CB1, CB2	Circuit Breaker	6081051	03640
CB3	Circuit Breaker	6079224	03640
CB4	Circuit Breaker	6081052	03640
FL1 thru FL4	Filter	6070743	03640
J3, J4	Outlet	6070428	03640
J33	Receptacle	6072145	03640
J44, J45	Outlet	6070428	03640
K1	Contactor	6081054	03640
K2	Contactor	6081055	03640
K3	Relay	6081099	03640
R1 thru R4	Resistor	6081045	03640
TB6CR1, TB6CR2	Diode	6018033	03640
TB6R1 thru TB6R4	Resistor	6041432	03640
NA	Lug Terminal	6029799	03640
NA	Lug Terminal	6033228	03640
Note: Refer to figure 10-57 when replacing parts.			

Figure 9-16. AC Power Box (03B8) Replaceable Parts

Vendor Code	Name	Address
03640	International Business Machines Corp.	Owego, N. Y.
11359	Adage, Inc.	Cambridge, Mass.
88360	International Business Machines Corp.	Endicott, N. Y.

Figure 9-17. Vendor Code Cross-Reference.

9-10. REPAIR TECHNIQUES.

9-11. The following paragraphs discuss repair techniques applicable to the LVDAME.

9-12. PUSHBUTTON SWITCH ASSEMBLIES.

9-13. As shown on figure 9-18, a pushbutton switch assembly consists of four basic parts: switch housing, switch, light module, and screen. All of these parts and the lamp bulbs within the light modules are replaceable parts, as indicated on figures 9-5, 9-6, and 9-11.

CAUTION

LVDAME power should be off (POWER OFF lamp is lit) before dismantling any switch assemblies on the LVDAME.

9-14. The screen of any LVDAME pushbutton switch can be removed from the switch housing by inserting the arms of the Switch Assembly Extractor (IBM part number 6900020) into the spaces between the sides of the screen and the switch housing until the arms of the extractor engage the openings in the frame which supports the screen; the screen (and its frame) can then be pulled out of the switch housing. When the screen has been removed, the light module can be removed in the same manner. The switch can be removed from its housing by using the Switch Assembly Wrench (IBM part number 6900017) to loosen the nut which holds the switch to its housing.

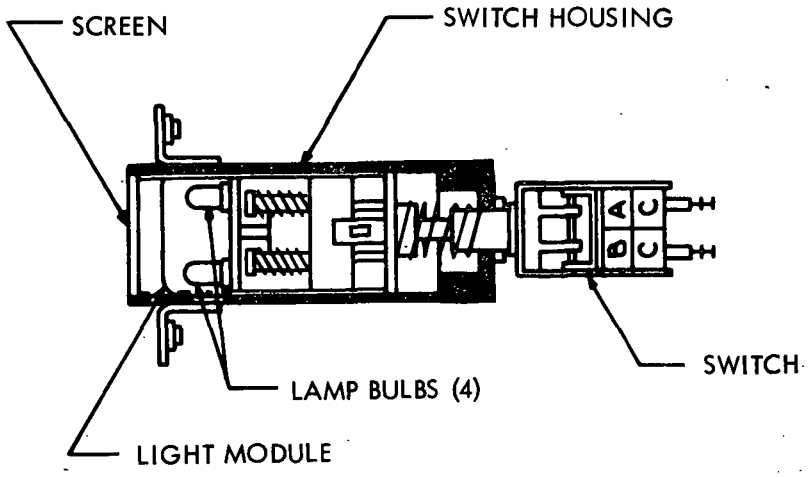


Figure 9-18. Pushbutton Switch Assembly

9-15. WRAPPED CONNECTIONS.

9-16. The wire wrapped connection is a precision pressure junction. A special wrapping tool wraps the stripped end of a wire tightly around the stationary terminal on a gate assembly. The resulting connection is a highly reliable permanent connection because of the high local residual stresses produced in the wire and terminal. Figure 9-19 illustrates a typical wrapped connection. The following paragraphs discuss the processes for using manual tools to wrap and unwrap connections. Recommended tools for wrapped connections are listed on figure 9-20.

CAUTION

Only nylon-jacketed or semi-rigid PVC (polyvinyl chloride-insulated) wire should be used for re-wiring back panels. Teflon-insulated wire, used in panels produced by automation, is unsuitable for re-wiring in the field due to the difficulty in stripping without damaging the conductor.

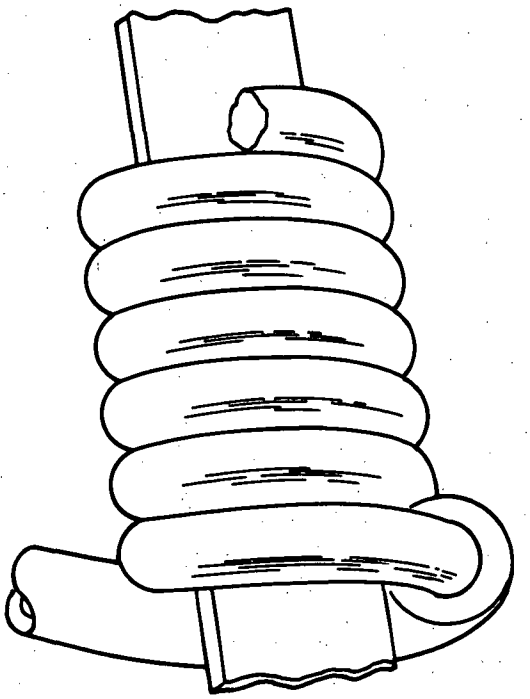


Figure 9-19. Wrapped Connection

Tool	Vendor/Part Number	Description
Hand Unwrap Tool	IBM 6072437	See figure 4-4, part J
Hand Wire Wrap Tool	IBM 6072438	See figure 4-4, part G
Wrapping Bit (No. 20)	Keller A-18633	See figure 4-4, part H
Wrapping Bit (No. 22)	Keller A-18632	
Wrapping Bit (No. 24)	Keller A-26232	
Wrapping Bit (No. 26)	Keller A-27611	
Sleeve (No. 20)	Keller A-18285	See figure 4-4, part I
Sleeve (No. 22, 24)	Keller A-18840	
Sleeve (No. 26)	Keller A-17611-2	

Figure 9-20. Recommended Wrapping Tools

9-17. WRAPPING. The following procedure indicates the necessary steps in making a wrapped connection.

a. Select the bit and sleeve for the wire size to be used.

Wire Size AWG	Wrapping Bit	Sleeve
26	Keller, A-27611	Keller, A-17611-2
24	Keller, A-26232	Keller, A-18840
22	Keller, A-18632	Keller, A-18840
20	Keller, A-18633	Keller, A-18285

b. Install bit and sleeve in the nose assembly of the wrapping tool (figure 9-21):

Figure 9-21. Wrapping Tool Assembly

1. Loosen the collet nut on the nose assembly.

2. Insert the wrapping bit into the collet. Rotate the bit while applying slight pressure against the end until it seats itself. (To remove the bit, reverse this process.)

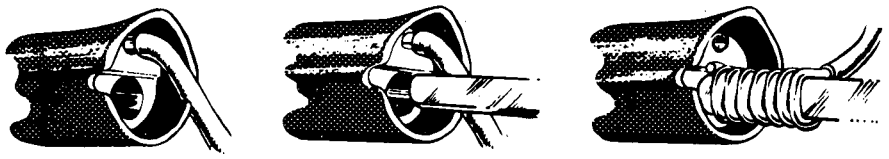
3. Place the sleeve over the bit and into the collet. Rotate until sleeve is seated and positioned. Apply slight pressure to the end of the sleeve and tighten collet nut.

c. Strip 1-3/8 to 1-1/2 inch of insulation from the end of the wire to be wrapped. This will result in about six wraps around the terminal. The completed terminal must have at least five turns of bare wire.

CAUTION

Do not nick or scrape the wire. A nicked wire is subject to breaks that are difficult to detect. Areas where plating is removed will oxidize, causing an unreliable connection.

d. Insert the stripped wire into the small hole of the wrapping bit (figure 9-22, part A) taking care to insert the wire up to the insulation. Do not bend the bare end of the wire, it may be difficult to slide into the bit. If the wire is not inserted in the wrapping bit up to the insulation, a "shiner" (bare wire between insulation and terminal) may result. There should be 1/4 turn to 3/4 turn of insulation at the beginning of each wrap, except for coaxial cable. Coaxial cable insulation should not be wrapped, but it must end no more than 1/16 inch from the terminal.



A B C

Figure 9-22. Wrapping Procedure

e. Hold the wire with the fingers and bend the insulated portion of the lead into the retaining notch in the sleeve (figure 9-22, part B). Use the right or left notch as determined by the direction of the approach (or exit) of the lead. Place the wrapping bit on the terminal. Be sure the terminal is inserted into the bit as far as it will go. Hold the tool in line with the terminal.

f. Hold the tool on the terminal and squeeze the trigger to wrap the wire on the terminal. The tool will automatically recede as the wire coils on the terminal. Release trigger and remove tool from terminal. The wrapped connection is complete (figure 9-22, part C).

NOTE

If too much pressure is used to push the tool on the terminal, a turn of wire will wrap over a previous turn. If too little pressure is exerted, the adjacent wraps of wire may not touch each other. Maximum separation between individual turns on the terminal must not exceed 0.005 inch, excluding the first and last wrap (figure 9-23).

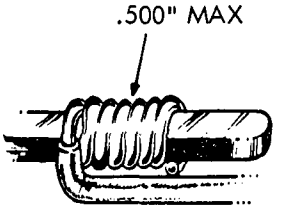


Figure 9-23. Wrap Spacing

9-18. UNWRAPPING. Wires can be removed from a terminal by using the hand unwrap tool illustrated on figure 9-24. This tool can unwrap both right and left-hand wraps.

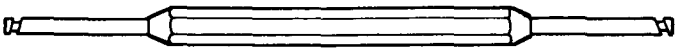


Figure 9-24. Unwrap Tool

9-19. Unwrapping is accomplished by catching the tail of the wire with the unwrap point and turn the tool in a direction opposite to that of the wrap. In some cases, it may be necessary to lift the wire tail away from the pin before the wire can be unwrapped. Apply only enough pressure to loosen turns.

CAUTION

An unwrapped wire must never be rewrapped. A new wire must be used as a replacement.

Never slide a termination on a pin because this rounds the sharp corner of the pin and makes subsequent connections unreliable. As you unwrap a wire, see that the first coil does not break off and drop into the panel. This breakage is often caused by the lip of the tool not engaging the tail of the wire. Terminals may be wrapped ten times before replacement is necessary.

9-20. WRAPPED CONNECTION QUALITY. Because the connection is destroyed if a wrap is disturbed in any manner, it is difficult to determine if a good quality junction has been made. The most common factors causing poor quality wraps are:

1. lncorrect wrapping bit for the wire size in use.

2. Worn or damaged wrapping bit.

3. Dirty wrapping bit.

9-21. A defective wrapped connection may be either too tight or too loose. If the wrap is made too tight, the wire is deformed to such an extent that it becomes brittle. The wire may then break under vibration and handling. A loose wrap will not have sufficient pressure to bond the wire to the terminal.

9-22. SMS back panel wires are frequently routed around, but not attached to, an intermediate terminal. If a wire is pulled too tight or excessive pressure is exerted at the point of contact with the intermediate terminal, insulation damage may result, allowing the wire to short to the terminal. This short may be intermittent. When wiring back panels, do not pull wires tightly around intermediate terminals, or allow a wire to rub along a terminal pin.

9-23. CRIMPED CONNECTIONS.

9-24. A crimped connection is a union of two electrical conductors formed by pressure. A crimped connection is usually made with a terminal that has a barrel or trough to accept a short length of wire. The wire is inserted in the terminal, which is then formed to compress and restrict the wire inside the terminal barrel as indicated on figure 9-25. If the correct pressure is applied during the forming process, a homogeneous mass will result in the crimped area.

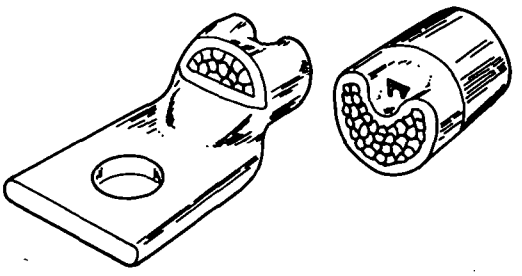


Figure 9-25. Crimped Connection, Cross Section

9-25. The critical factor in making a crimped connection is the extent to which the terminal and conductor are formed. Pressure produced in the process must be high enough to cause a bond between the terminal and conductor materials, yet low enough to prevent embrittlement of the formed parts.

9-26. RECOMMENDED CRIMPING TOOLS. Recommended crimping tools and their intended applications are listed in figure 9-26.

9-27. AMP tool 59501 is a ratchet crimping tool to be used with 22-24 AWG solid or stranded wire only. The die-set is not replaceable, and no adjustments are provided on the tool.

Crimping Tool	Application	Description
AMP 59501	Used to crimp AWG 22-24 solid or stranded wire.	See figure 4-4, part Q
Berg HT-3-20	Used to crimp AWG 20 solid or stranded wire to a slip-on terminal.	See figure 4-4, part R
Berg HT-3-22	Used to crimp AWG 22 solid or stranded wire to a slip-on terminal.	
Berg HT-3-24	Used to crimp AWG 24 solid or stranded wire to a slip-on terminal.	
Bendix 11-7295 (Kit)	Used to crimp size 12, 16, and 20 type connector contacts.	See figure 4-4, part K

Figure 9-26. Recommended Crimping Tools

9-28. Terminals used with the AMP ratchet tool have a two-section crimping barrel as illustrated in figure 9-27. The tool crimps one section on the conductor and the other section on the insulation. Make certain to insert terminals into the die so that the larger die opening crimps the insulation.

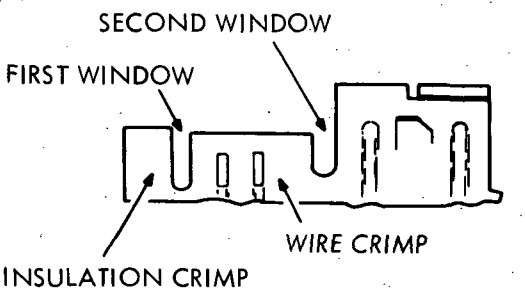


Figure 9-27. Slip-on Connector Terminal

9-29. CRIMPED CONNECTION QUALITY. The quality of a crimped connection depends largely on the correct combination of wire, terminal, and tool for each application. The following procedure is recommended for determining the quality of crimped connections:

a. Visually inspect all completed connections for the following:

CAUTION

Do not use a connection that does not meet these criteria.

1. Stripped portion of the wire centrally located under the crimp.
2. No deformation of the terminal outside of the crimp area.
3. No fractures of the terminal or wire.

b. Test completed connections having no visual defects as follows:

1. Grip the wire between the thumb and forefinger of one hand and the terminal between the thumb and forefinger of the other hand.

2. Pull the wire, exerting only enough pressure to make the wire taut. Check for any movement of the wire within the terminal barrel.

NOTE

Wire movement in the terminal barrel can often be heard, but not seen. Such a connection is called a clicker and must not be used.

3. Bend the wire about 30 from center and repeat step 2. Bend the wire in the opposite direction about 30 from center and repeat step 2.

9-30. SOLDERED CONNECTIONS.

9-31. The soldering process involves six steps: selection of materials, preparing the soldering iron and tip, preparing the work, heating the work, applying the flux and solder, and cooling.

9-32. SELECTION OF MATERIALS. Recommended soldering tools are listed in figure 9-28.

CAUTION

Do not use acid-core solder.

Tool	Vendor Part No.	Description
Soldering Handle	Hexacon P25	See figure 4-4, part E
Soldering Tip	Hexacon HT248D	See figure 4-4, part F

Figure 9-28. Recommended Soldering Tools

9-33. Rosin cored wire solder (conforming to Federal Specification QQ-S-571) is similar to a piece of spaghetti; the hollow center is filled with flux that flows over the work when heated to a moderate temperature (about 300° F). This temperature is below the melting point of the solder (about 360° F). The flux becomes active upon further heating, but prolonged exposure to heat causes it to decompose.

9-34. PREPARING THE SOLDERING IRON AND TIP. The soldering iron is used only to transmit heat to the work. Before using the iron, heat it to operating temperature and tin it: wipe the tip with a clean cloth or canvas; then apply flux and solder, giving the tip a clean, shiny coat of solder. Tinning is done to insure good heat transfer and to keep the connection area free of contamination. Subsequent accumulation of flux residue and solder dross can be removed in the same manner.

9-35. PREPARING THE WORK. The work must be clean. No grease, wax, paint, dust or other foreign material should be present on the surfaces to be soldered. These surfaces should be pretinned. Pretinning is the application of a thin layer of solder over the surfaces of the metals to be joined, using the same process as for tinning the soldering iron tip.

9-36. Use extreme care when stripping insulation from wire. The stripping tools should be adjusted so that no metal is removed from the wire during the stripping operation. Cutting the strands in stranded wire reduces the cross-sectional area, which decreases current carrying capacity and presents a mechanically weak spot; a nick in solid wire has much the same effect.

9-37. Unless otherwise specified, insulation should be stripped so that not more than 1/8 inch nor less than 1/16 inch of wire will be exposed between the soldered terminal and the insulation (figure 9-29). Leads of an axial lead component should not be formed closer than 1/16 inch from the component body (figure 9-30).

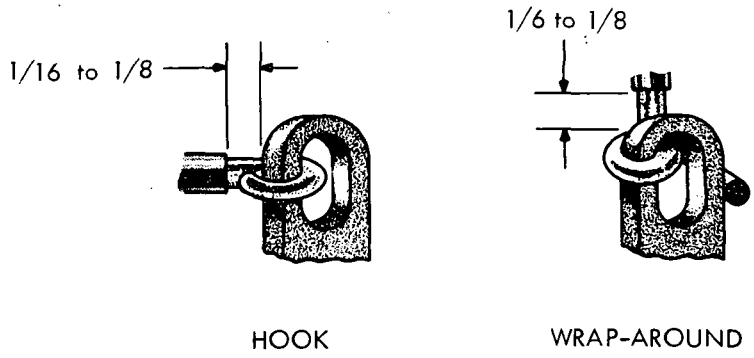


Figure 9-29. Terminal Connections

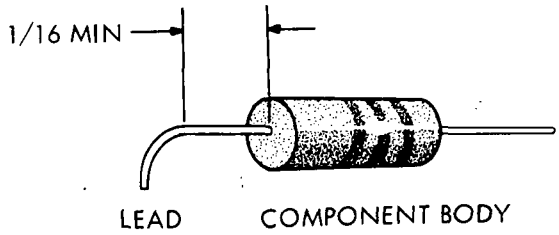


Figure 9-30. Axial Lead Connection

9-38. HEATING THE WORK. The joint must be thoroughly heated before applying solder. Efficient heat transfer from the iron to the work depends on the cleanliness of the surfaces and the size of the contact area. A small amount of clean solder on the iron tip will insure effective heat transfer.

9-39. Poor solder connections are often the result of insufficient heat. Protect components, but remember that a destroyed component is less expensive than a cold soldered joint that causes intermittent failures.

9-40. APPLYING THE FLUX AND SOLDER. The solder should be applied to the work, not to the iron. If the surfaces are clean and are at the correct temperature, flux and solder will flow freely over the surfaces and wet the metal. This wetting action is the basic solder bond. After the solder solidifies, it will remain adhered to the surface and will provide electrical continuity.

9-41. The proper amount of solder is important. The solder bond occurs on the metal surfaces and excessive solder does not improve the joint but can introduce undesirable side effects. Use enough solder to cover the parts to be joined, but leave the outlines visible.

9-42. COOLING. Once the solder has been applied, withdraw the soldering iron and allow the joint to cool. Solidification of solder is not instantaneous, and any movement during this time may cause a solder bond of unacceptable quality. Keep the parts perfectly still until the solder is frozen.

9-43. VISUAL INSPECTION. A good soldered connection is bright and smooth. The solder feathers out to a thin edge from the main body of solder in the joint. It also approximately outlines the wire and terminal. Figure 9-31 illustrates good soldered connections.

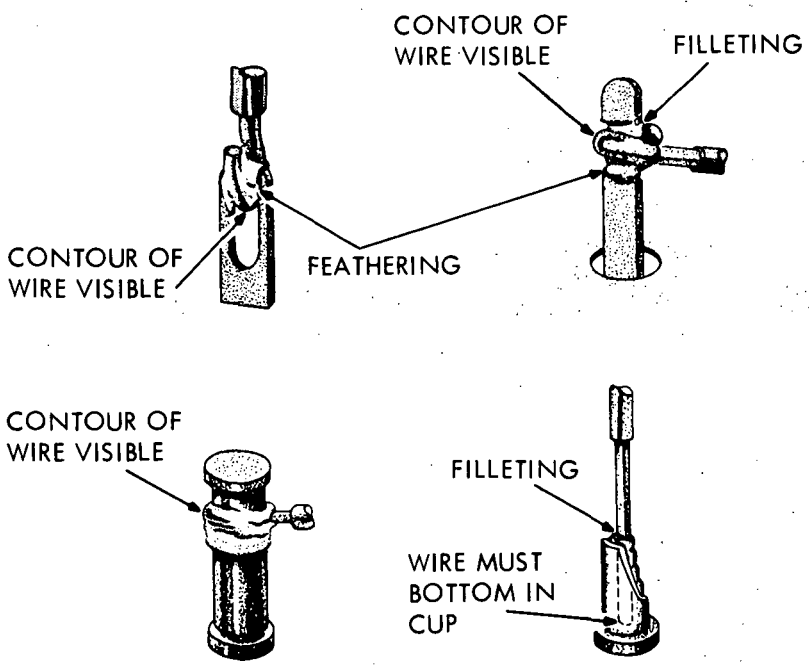


Figure 9-31. Good Soldered Connections

9-44. Figure 9-32 illustrates defective soldered connections.

9-45. The Cold Soldered Joint (figure 9-32, part A) has a dull, granular appearance. It is caused by insufficient heating, or movement of the work during cooling.

9-46. The Rosin Joint (figure 9-32, part B) has a rosin inclusion. Rosin joints can be due to insufficient heat to permit the rosin to be displaced by the solder, or insufficient heat to permit adequate melting of the flux.

9-47. The Excessively Soldered Joint (figure 9-32, part C) hides the outline of the joint components with an excessive amount of solder.

9-48. The Fractured Soldered Joint (figure 9-32, part D) is one in which small cracks are present. This condition can be due to stress applied before the solder is completely solidified.

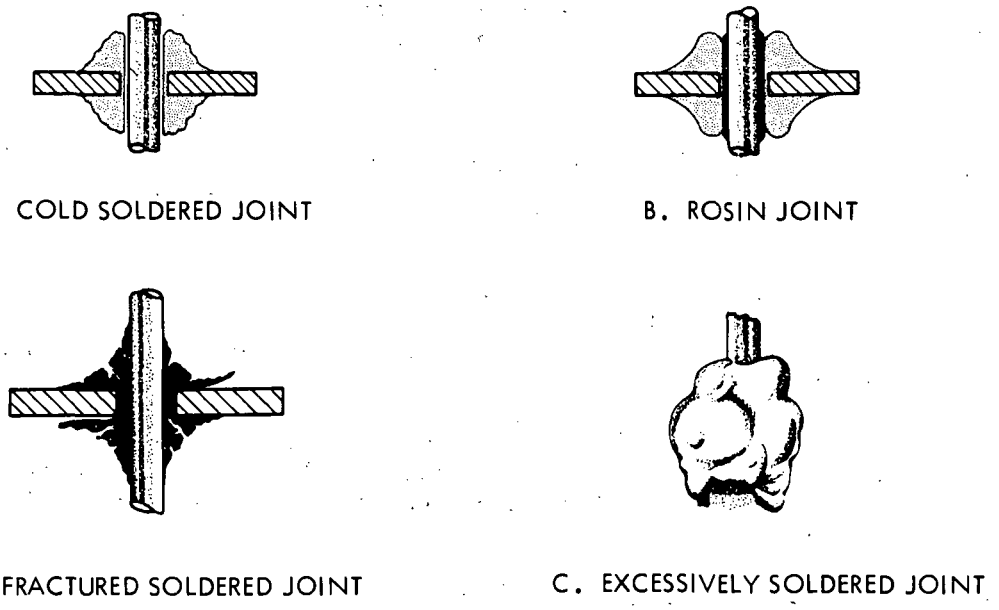


Figure 9-32. Defective Soldered Connections

9-49. SMS CARD REPLACEMENT.

9-50. The SMS card puller (IBM 6072429) facilitates insertion or removal of SMS cards from their sockets. Use of this tool reduces the probability of dropping cards and other handling damage. This tool is illustrated on figure 4-4, part A.

9-51. In operation, the card puller fits over the edges of an SMS card. When the tool is properly positioned, a tooth on the spring-loaded latch seats in a hole in the card. The card is released by depressing the latch.

CAUTION

Before removing an SMS card, insert IBM punched cards or similar material between the card to be removed and adjacent SMS cards. Damage to SMS cards or components may be eliminated in this manner.

Oil or moisture from the fingers can critically decrease the insulation resistance of the land pattern side of the card. Cards should be carefully handled by the edges only.

9-52. When an SMS card is removed from its socket, the card contacts should be cleaned and lubricated before the card is reinstalled if either of the following conditions exists:

1. The card contacts are visibly contaminated.

2. The card contacts have been handled. If there is any doubt about the contamination of the contacts, clean and relubricate them.

9-53. The following cleaning and lubricating procedure insures low contact resistance and reduces wear of the gold-plated contact surfaces. The procedure may be performed any number of times without affecting contact reliability. To clean and lubricate the contacts:

a. Apply lubricant (IBM part number 6072430) either directly to the contacts or indirectly with a saturated, clean, lint-free cloth or tissue.

b. Wipe the contacts toward the component section of the card with a cloth or tissue moistened with the lubricant.

CAUTION

Do not allow the lubricant to contact the clear plastic coating on the component portion of the card. The solvents in the lubricant can dissolve the plastic coating, which will act as an insulator if rubbed on the contacts.

c. Rub the contacts with a clean, dry piece of cloth of tissue until there is no visible trace of the lubricant. The cloth or tissue will darken if further cleaning is necessary. Repeat the procedure from step a if further cleaning is needed.

9-54. SMS CARD REPAIR.

9-55. Repair of printed circuit cards primarily consists of soldering and unsoldering operations. The specific jobs involved are:

1. Removal of defective components.

2. Installation of replacement components.

3. Joining broken printed conductors.

9-56. Care must be taken to avoid damage to the card assembly during the repair process. The card assembly is easily damaged in two ways:

1. Heat damage to the card or to components on the card.

2. Physical damage.

9-57. The card is made of an insulating material that will withstand a dipsolder temperature of about 515° F for 30 seconds. This compares with a minimum solder melting temperature of 360° F and an average soldering iron temperature of 750° F. This means that the soldering iron must contact the card for only a short interval of time. Excessive heat may damage a card in two ways by:

1. Destroying the bond between the insulated board and a printed conductor, resulting in a raised conductor;

2. Scorching or burning the board.

9-58. Excessive heat may also damage components on the card. Semiconductors are especially sensitive to heat. Use of the soldering tools recommended under SOLDERED CONNECTIONS will help avoid heat damage.

9-59. Physical damage in the form of a raised conductor is easily inflicted if stress is applied in a direction that tends to separate the conductor from the board (figure 9-33).

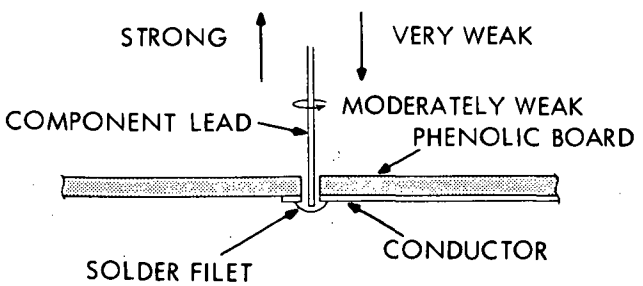


Figure 9-33. Stress Applied to Component Leads

9-60. COMPONENT REMOVAL. When the leads of the defective component must be saved, use the following procedure to remove the component:

a. Straighten the component leads that are bent over on the wiring side of the board. Figure 9-34 illustrates a method of using the soldering iron tip as a wedge to prevent pulling the land away from the board. A pair of long-nose pliers may be used on the component side of the card to prevent downward movement of the lead.

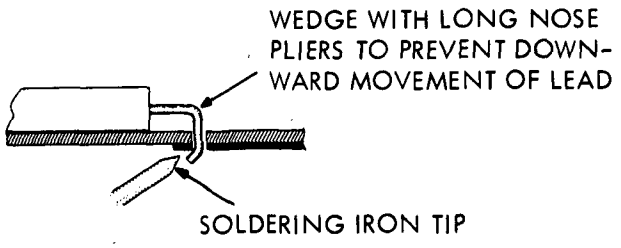


Figure 9-34. Component Removal

b. Heat the component leads and pull them through the holes from the component side of the board.

9-61. If the leads of the defective component may be destroyed, use the following removal procedure:

a. Cut the leads of the defective component as close as possible to the board on the component side of the card. Do not damage the board or adjacent components.

b. Hold the card in your hand and use a clean, tinned soldering iron to heat the solder connection between the remaining portion of the leads and the conductor pattern.

c. When the solder starts to flow, rap the hand holding the card on the work surface.

d. Repeat steps b and c if the solder and piece of lead do not leave the hole.

9-62. COMPONENT INSTALLATION. Use the following procedure for installing components on SMS cards.

a. Insert component leads through the holes in the board. Cut the leads so that about 1/16 inch remains to bend over on the conductor pattern. Bend the leads parallel to the component body and toward each other. Axial lead components, such as resistors, are mounted flush against the surface of the board.

CAUTION

Do not bend leads close to components (see SOLDERED CONNECTIONS for technique). The leads on tantalum capacitors are particularly subject to damage.

b. Solder the component leads to the conductor pattern. Avoid excessive heat and solder, particularly with transistors and diodes. It is not desirable to fill the hole in the board with solder.

c. Wash the general area of repair using a typewriter cleaning brush and IBM cleaning fluid (IBM part number 450608). Dry the affected area by wiping with a clean piece of cloth or tissue.

9-63. PRINTED CONDUCTOR REPAIR. Two printed conductor defects may be found: broken conductor, or delaminated conductor (raised land).

9-64. To repair a broken conductor, solder a 24 AWG solid wire jumper across the break. The wire should overlap the printed conductor at least 1/16 inch on each end. If the break is long, and the possibility of a short exists, use insulated wire stripped on each end.

9-65. To repair a delaminated conductor, cut both ends of the loose section at a point where the bond is not broken. After the loose section is removed, repair the conductor using the same method used for a broken conductor.

9-66. EXTERIOR SURFACE COATINGS.

9-67. Figure 9-35 lists the solvents, reducers, primers and paints needed to refurbish LVDAME coatings that become chipped, discolored, or otherwise defective.

9-68. REPAINTING TECHNIQUES.

9-69. The following paragraphs indicate the recommended consistencies for the paints and other fluids needed to repair the exterior coatings of the LVDAME. A fine brush should be used to retouch defective panel markings and any small scratches on the LVDAME For repainting areas greater than 1 in. square, the paint should be applied by spraying.

9-70. SOLVENT. The surface to be repainted should be thoroughly cleaned by wiping it with the solvent indicated in figure 9-35. The surface should then be allowed to dry for at least 30 minutes.

9-71. PRIMERS. If the coating has been marred so that the metal surface is exposed, a primer coating should be applied before the paint is applied. The primer need not be diluted for brush application; however, for spray application the primer should be diluted with one part reducer to two parts primer. The primer coating should be air dried for at least three minutes before paint is applied.

Surface	Solvent	Reducer*	Primer*	Paint (Vinyl)*	Notes*
Frame Covers	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903.	Charcoal-John L. Armitage Co., P-318.	Deep Charcoal-John L. Armitage Co., U-211.	Use texturing agent, John L. Armitage Co., M-411.
Feature Strips (Between A and B Modules)	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903.	Charcoal-John L. Armitage Co., P-318.	Deep Charcoal-John L. Armitage Co., U-211.	
Control Panels: Background	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903 or M-130.	Blue-Gray-John L. Armitage Co., P-350.	Light Gray-John L. Armitage Co., U-662S.	
Functional Areas	None	None	None	Dark Gray-John L. Armitage Co., M-1085. **	
Markings	None	None	None	White-John L. Armitage Co., M-1027. **	Use on Dark Gray functional areas.
Markings	None	None	None	Black-John L. Armitage Co., M-1035. **	Used on Light Gray areas.
A/D Converter and Multiplexer: Background	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903 or M-130.	White-John L. Armitage Co., P-320.	Light-Gray-John L. Armitage Co., U-662S.	

*Equivalent materials may be used.
**Vinyl inks, originally applied by silk screen processes.

Figure 9-35. Recommended Repainting Materials (Sheet 1 of 2)

Surface	Solvent	Reducer*	Primer*	Paint (Vinyl)*	Notes*
Functional Areas	Xylene conforming to Federal Specification TT-X-916	John L. Armitage Co., A-903 or M-130	Charcoal-John L. Armitage Co., P-318.	Dark Gray-John L. Armitage Co., U-663S.	
Markings	None	None	None	White-Irvin, Jewell, and Vison Co., 4795	Used as filler for engraving.
Markings	None	None	None	Black-Interchemical Corp., 3989-1	
Name Plate	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903 or M-130.	Yellow-John L. Armitage Co., P-321.	Yellow-John L. Armitage Co., U-396S.	
Name Plate	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903 or M-130.	Blue-John L. Armitage Co., P-300.	Sky Blue-John L. Armitage Co., U-333.	
Name Plate	None	None	None	White-John L. Armitage Co., M-1027.	Used as a filler for engraving.

*Equivalent materials may be used.

Figure 9-35. Recommended Repainting Materials (Sheet 2)

9-72. PAINTS. The paints need not be diluted for brush application; however, for spray application the paint should be diluted with one part reducer to four parts paint. Four or more sprayed coats should be applied, allowing a minimum time of one minute between the application of each coat. For a non-textured finish, these applications are the finish coat; however, for a textured finish these applications are only the first finish coat.

NOTE

The number of paint coats required to adequately repair the defective surface depends on the depth of the defect and the thickness of the original coatings.

9-73. If the final surface is to be textured, a second finish coat of paint should be applied after the first finish coat has been air dried. The paint for this second finish coat need not be diluted for brush application; however, for spray application the paint should be diluted with one part reducer to eight parts paint. Five or more sprayed coats should be applied, allowing a minimum time of one minute between the application of each coat. (See not in preceding paragraph.)

9-74. TEXTURING AGENT. The texturing agent should not be diluted before being sprayed as a fine mist coat over the second finish coat.

SECTION X

DIAGRAMS

10-1. SCOPE.

10-2. This section contains three types of Engineering drawings required for maintenance of the LVDAME (Electrical Schematic Diagrams, Second Level Logic Diagrams, and Assembly Drawings) as follows:

Figure 10-4. Power Distribution Electrical Schematic Diagram (LN 00.03.02.0 through LN 00.03.06.0)

Figure 10-5. Computer Dummy Loads Electrical Schematic Diagram (LN 00.03.07.0)

Figure 10-6. Connector 9420 J32 Electrical Schematic Diagram (LN 00.03.08.0)

Figure 10-7. Interface Monitoring Panel (01A1) Electrical Schematic Diagram (LN 04.00.01.0 through LN 04.00.05.0)

Figure 10-8. Manual Test Panel (01A2) Electrical Schematic Diagram (LN 04.00.06.0 through LN 04.00.10.0)

Figure 10-9. Power Control Panel (02A6) Electrical Schematic Diagram (LN 04.00.11.0 through LN 04.00.15.0)

Figure 10-10. Multiplexer - A/D Converter Interface Electrical Schematic Diagram (LN 04.00.18.0 and LN 04.00.19.0)

Figure 10-11. Ratiotran and Tapped Transformer Electrical Schematic Diagram (LN 04.00.20.0)

Figure 10-12. A Cable Interface (Connector 9420 J23) Electrical Schematic Diagram (LN 04.00.21.0)

Figure 10-13. B Cable Interface (Connector 9420 J22) Electrical Schematic Diagram (LN 04.00.22.0)

Figure 10-14. C Cable Interface (Connector 9420 J27) Electrical Schematic Diagram (LN 04.00.23.0)

Figure 10-15. D Cable Interface (Connector 9420 J26) Electrical Schematic Diagram (LN 04.00.24.0)

Figure 10-16. E Cable Interface (Connector 9420 J25) Electrical Schematic Diagram (LN 04.00.25.0)

Figure 10-17. BC Cable Interface (Connector 9420 J24) Electrical Schematic Diagram (LN 04.00.26.0)

Figure 10-68. OTO2 Printed Circuit Board Assembly (6942030)

Figure 10-69. OTO3 Printed Circuit Board Assembly (6942032)

Figure 10-70. OTO4 Printed Circuit Board Assembly (6942033)

Figure 10-71. OVD1 Printed Circuit Board Assembly (6942036)

Figure 10-72. OCD2 Printed Circuit Board Assembly (6942037)

Figure 10-73. ORD1 Printed Circuit Board Assembly (6942038)

Figure 10-74. OTO5 Printed Circuit Board Assembly (6942040)

Figure 10-75. OSS1 Printed Circuit Board Assembly (6942042)

Figure 10-76. OMCR Printed Circuit Board Assembly (6942044)

Figure 10-77. OSTT Printed Circuit Board Assembly (6942045)

Figure 10-78. OTD1 Printed Circuit Board Assembly (6942047)

Figure 10-79. OTSD Printed Circuit Board Assembly (6942049)

10-3. Automated Logic Diagrams (ALD's), Circuit Card Location Charts, and Edge Connector Lists are not included in this manual; they are supplied in a set of four volumes entitled SATURN V LTE-LVDA Manual Exerciser Automated Logic Diagrams. However, the ALD page format and the contents of the Circuit Card Location Charts and Edge Connector Lists are explained in this section.

10-4. DRAWING REFERENCES.

10-5. References are made between and within the Electrical Schematic Diagrams, ALD's, Circuit Card Location Charts, and Edge Connector Lists by an "LN" seven-digit number (xx. xx. xx. x) assigned to each page (or sheet). The LN number indicates the type of drawing as follows:

Electrical Schematic Diagrams – LN 00. 03. xx. x or LN 04. 00. xx. x

ALD's – LN 05. xx. xx. x

The digit positions indicated here by x's specify the page number sequence.

10-6. Figure 10-1 lists the LVDAME ALD's by logic page (LN) number and page part number. The page part number is used for ordering a specific page or series of pages.

10-7. SECOND LEVEL LOGIC DIAGRAMS.

10-8. Second level logic diagrams are so called because they do not contain the degree of detail found on the automated or "first level" logic diagrams. Second level logic diagrams do not contain such details as pin connection designations, voltage levels, SMS card types, or location of SMS cards in the gate assemblies; all these details are included on the automated logic diagrams.

Logic Page Number	Page Part Number
05.01.01.1	6940550
05.01.02.1	6940551
05.01.03.1	6940552
05.01.04.1	6940553
05.01.05.1	6940554
05.01.06.1	6940555
05.01.07.1	6940556
05.01.08.1	6940557
05.01.09.1	6940558
05.01.10.1	6940559
05.01.11.1	6940560
05.01.12.1	6940561
05.01.13.1	6940562
05.01.14.1	6940563
05.01.15.1	6940564
05.01.16.1	6940565
05.01.17.1	6940566
05.01.18.1	6940567
05.01.19.1	6940568
05.01.20.1	6940569
05.01.21.1	6940450
05.01.22.1	6940451
05.01.23.1	6940452
05.01.24.1	6940453
05.01.25.1	6940454
05.01.26.1	6940455
05.01.27.1	6940456
05.01.28.1	6940457
05.01.29.1	6940458
05.01.30.1	6940459
05.01.31.1	6940460
05.01.32.1	6940561
05.01.33.1	6940462
05.01.34.1	6940463
05.01.35.1	6940464
05.01.36.1	6940465
05.01.37.1	6940466
05.01.38.1	6940467
05.01.39.1	6940468
05.01.40.1	6940469
05.01.41.1	6940470
05.01.42.1	6940471
05.01.43.1	6940472
05.01.44.1	6940473
05.01.45.1	6940474
05.01.46.1	6940475
05.01.47.1	6940476

Logic Page Number	Page Part Number
05.01.48.1	6940477
05.02.01.1	6941350
05.02.02.1	6941351
05.02.03.1	6941352
05.02.04.1	6941364
05.03.01.1	6942750
05.03.02.1	6942751
05.03.03.1	6942752
05.03.04.1	6942753
05.03.05.1	6942754
05.03.06.1	6942755
05.03.07.1	6942756
05.03.08.1	6942757
05.03.09.1	6942758
05.03.10.1	6942759
05.03.11.1	6942760
05.03.12.1	6942761
05.03.13.1	6942762
05.03.14.1	6942763
05.03.15.1	6942764
05.03.16.1	6942765
05.03.17.1	6942766
05.03.18.1	6942767
05.03.19.1	6942768
05.03.20.1	6942769
05.03.21.1	6942770
05.03.22.1	6942771
05.04.01.1	6941650
05.04.02.1	6941651
05.04.03.1	6941652
05.04.04.1	6941653
05.04.05.1	6941654
05.04.06.1	6941655
05.04.07.1	6941656
05.04.08.1	6941657
05.04.09.1	6941658
05.04.10.1	6941659
05.04.11.1	6941660
05.04.12.1	6941661
05.04.13.1	6941662
05.04.14.1	6941663
05.04.15.1	6941664
05.04.16.1	6941665
05.04.17.1	6941666
05.04.18.1	6941667
05.04.19.1	6941668
05.04.20.1	6941669

Logic Page Number	Page Part Number
05.04.21.1	6941670
05.04.22.1	6941671
05.04.23.1	6941672
05.04.24.1	6941673
05.04.25.1	6941674
05.04.26.1	6941675
05.05.01.1	6940750
05.05.02.1	6940751
05.05.03.1	6940752
05.05.04.1	6940753
05.05.05.1	6940754
05.05.06.1	6940755
05.05.07.1	6940776
05.05.08.1	6940777
05.06.01.1	6940756
05.06.02.1	6940757
05.06.03.1	6940778
05.06.04.1	6940779
05.07.01.1	6940850
05.07.02.1	6940851
05.07.03.1	6940852
05.07.04.1	6940853
05.07.05.1	6940854
05.07.05.2	6940855
05.07.06.1	6940856
05.07.07.1	6940857
05.07.08.1	6940858
05.07.09.1	6940859
05.07.10.1	6940860
05.07.11.1	6940861
05.07.12.1	6940862
05.07.13.1	6940863
05.07.14.1	6940864
05.07.15.1	6940865
05.07.16.1	6940866
05.07.17.1	6940867
05.07.18.1	6940868
05.07.19.1	6940869
05.07.20.1	6940870
05.07.21.1	6940871
05.07.22.1	6940872
05.07.23.1	6940873
05.07.24.1	6940874
05.07.25.1	6940875
05.07.26.1	6940876
05.07.27.1	6940877
05.07.28.1	6940878

Figure 10-1. LVDAME Automated Logic Diagram Part Numbers (Sheet 1 of 3)

Logic Page Number	Page Part Number
05.07.29.1	6940879
05.07.30.1	6940880
05.07.31.1	6940881
05.07.32.1	6940882
05.08.01.1	6940350
05.08.02.1	6940351
05.08.03.1	6940352
05.08.04.1	6940353
05.08.05.1	6940354
05.08.06.1	6940355
05.08.07.1	6940356
05.08.08.1	6940357
05.08.09.1	6940358
05.08.10.1	6940359
05.08.11.1	6940360
05.08.12.1	6940361
05.08.13.1	6940362
05.08.14.1	6940363
05.08.15.1	6940364
05.08.16.1	6940365
05.08.17.1	6940366
05.08.18.1	6940367
05.08.19.1	6940368
05.08.20.1	6940369
05.08.21.1	6940370
05.08.22.1	6940371
05.08.23.1	6940372
05.08.24.1	6940373
05.08.25.1	6940374
05.08.26.1	6940375
05.08.27.1	6940376
05.08.28.1	6940377
05.08.29.1	6940378
05.08.30.1	6940379
05.08.31.1	6940380
05.08.32.1	6940381
05.08.34.1	6940384
05.08.34.2	6940386
05.08.35.1	6940665
05.08.36.1	6940666
05.08.37.1	6940667
05.08.38.1	6940668
05.08.39.1	6940669
05.08.40.1	6940670
05.08.41.1	6940671
05.08.42.1	6940672
05.08.43.1	6940673

Logic Page Number	Page Part Number
05.08.44.1	6940674
05.08.45.1	6940675
05.08.46.1	6940676
05.08.47.1	6940677
05.08.48.1	6940678
05.08.49.1	6940679
05.08.49.2	6940570
05.08.50.1	6940571
05.08.51.1	6940572
05.08.52.1	6940573
05.08.53.1	6940574
05.08.54.1	6940575
05.08.55.1	6940576
05.08.56.1	6940577
05.09.01.1	6940950
05.09.02.1	6940951
05.09.03.1	6940952
05.09.04.1	6940953
05.09.05.1	6940954
05.09.06.1	6940955
05.09.07.1	6940956
05.09.08.1	6940957
05.09.09.1	6940958
05.09.10.1	6940959
05.09.11.1	6940960
05.09.12.1	6940961
05.09.13.1	6940962
05.09.14.1	6940963
05.09.15.1	6940964
05.09.16.1	6940965
05.09.17.1	6940966
05.09.18.1	6940967
05.09.19.1	6940968
05.09.20.1	6940969
05.09.21.1	6940970
05.09.22.1	6940971
05.09.23.1	6940972
05.09.24.1	6940973
05.09.25.1	6940974
05.09.26.1	6940975
05.09.27.1	6940976
05.09.28.1	6940977
05.09.29.1	6940978
05.09.30.1	6940979
05.09.31.1	6940980
05.09.32.1	6940981
05.09.33.1	6940650

Logic Page Number	Page Part Number
05.09.34.1	6940982
05.09.35.1	6940651
05.09.36.1	6940652
05.09.37.1	6940653
05.09.38.1	6940654
05.09.39.1	6940655
05.09.40.1	6940656
05.10.01.1	6942850
05.10.02.1	6942851
05.10.03.1	6942852
05.10.04.1	6942853
05.10.05.1	6942854
05.10.06.1	6942855
05.10.07.1	6942856
05.10.08.1	6942857
05.10.09.1	6942858
05.10.10.1	6942859
05.10.11.1	6942860
05.10.12.1	6942861
05.10.13.1	6942862
05.10.14.1	6942863
05.10.15.1	6942864
05.10.16.1	6942865
05.10.17.1	6942866
05.10.18.1	6942867
05.10.19.1	6942868
05.10.20.1	6942869
05.10.21.1	6942870
05.10.22.1	6942871
05.10.23.1	6942950
05.10.24.1	6942951
05.10.25.1	6942952
05.10.26.1	6942953
05.10.27.1	6942954
05.10.28.1	6942955
05.10.29.1	6942956
05.10.30.1	6942957
05.10.31.1	6942958
05.10.32.1	6942959
05.10.33.1	6942960
05.10.34.1	6942961
05.10.35.1	6942962
05.10.36.1	6942963
05.10.37.1	6942964
05.10.38.1	6942965
05.10.39.1	6942966
15.10.40.1	6942967

Figure 10-1. LVDAME Automated Logic Diagram Part Numbers (Sheet 2)

Logic Page Number	Page Part Number
05. 10. 41. 1	6942968
05. 10. 42. 1	6942969
05. 10. 43. 1	6942970
05. 10. 44. 1	6942971
05. 10. 45. 1	6942972
05. 10. 46. 1	6942973
05. 10. 47. 1	6942872
05. 10. 48. 1	6942873
05. 10. 49. 1	6942974
05. 10. 50. 1	6942975
05. 10. 51. 1	6942874
05. 11. 01. 1	6941850
05. 11. 02. 1	6941851
05. 11. 03. 1	6941852
05. 11. 04. 1	6941853
05. 11. 05. 1	6941854
05. 11. 06. 1	6941855
05. 11. 07. 1	6941856
05. 11. 08. 1	6941857
05. 11. 09. 1	6941858
05. 11. 10. 1	6941859
05. 11. 11. 1	6941860
05. 11. 12. 1	6941861
05. 11. 13. 1	6941862
05. 11. 14. 1	6941863
05. 11. 15. 1	6941864
05. 11. 16. 1	6941865
05. 11. 17. 1	6941866
05. 11. 18. 1	6941867
05. 12. 01. 1	6941450
05. 12. 02. 1	6941451
05. 12. 03. 1	6941452
05. 12. 04. 1	6941453
05. 12. 05. 1	6941454
05. 12. 06. 1	6941455
05. 12. 07. 1	6941456
05. 12. 08. 1	6941457
05. 12. 09. 1	6941458
05. 12. 10. 1	6941459
05. 12. 11. 1	6941460
05. 12. 12. 1	6941461
05. 12. 13. 1	6941462
05. 12. 14. 1	6941463
05. 12. 15. 1	6941464
05. 12. 16. 1	6941465
05. 12. 17. 1	6941466

Logic Page Number	Page Part Number
05. 12. 18. 1	6941467
05. 12. 19. 1	6941468
05. 12. 20. 1	6941469
05. 12. 21. 1	6941470
05. 12. 22. 1	6941471
05. 12. 23. 1	6941472
05. 12. 24. 1	6941473
05. 12. 25. 1	6941474
05. 12. 26. 1	6941475
05. 12. 27. 1	6941476
05. 12. 28. 1	6941356
05. 12. 29. 1	6941357
05. 12. 30. 1	6941358
05. 12. 31. 1	6941359
05. 12. 32. 1	6941360
05. 12. 33. 1	6941361
05. 12. 34. 1	6941457
05. 12. 35. 1	6940256
05. 12. 36. 1	6940257
05. 12. 38. 1	6940258
05. 12. 39. 1	6940259
05. 13. 01. 1	6940251
05. 13. 02. 1	6940252
05. 13. 03. 1	6940253
05. 13. 04. 1	6940254
05. 13. 05. 1	6940260
05. 14. 01. 1	6940662
05. 14. 02. 1	6940663
05. 14. 03. 1	6940664
05. 15. 01. 1	6941550
05. 15. 02. 1	6941551
05. 15. 03. 1	6941552
05. 15. 04. 1	6941553
05. 15. 05. 1	6941554
05. 15. 06. 1	6941555
05. 15. 07. 1	6941556
05. 15. 08. 1	6941557
05. 15. 09. 1	6941558
05. 15. 10. 1	6941559
05. 15. 11. 1	6941560
05. 15. 12. 1	6941561
05. 15. 13. 1	6941562
05. 15. 14. 1	6941563
05. 15. 15. 1	6941564
05. 15. 16. 1	6941565
05. 16. 17. 1	6941566

Logic Page Number	Page Part Number
05. 15. 18. 1	6941567
05. 15. 19. 1	6941568
05. 15. 20. 1	6941569
05. 15. 21. 1	6941570
05. 15. 22. 1	6941571
05. 15. 23. 1	6941572
05. 15. 24. 1	6941573
05. 15. 25. 1	6941574
05. 15. 26. 1	6941575
05. 15. 27. 1	6941576
05. 15. 28. 1	6941577
05. 15. 29. 1	6941578
05. 15. 30. 1	6941579
05. 16. 01. 1	6940775
05. 17. 01. 1	6940758
05. 17. 02. 1	6940759
05. 17. 03. 1	6940760
05. 17. 04. 1	6940761
05. 17. 05. 1	6940762
05. 17. 06. 1	6940763
05. 17. 07. 1	6940764
05. 17. 08. 1	6940765
05. 17. 09. 1	6940766
05. 17. 10. 1	6940767
05. 17. 11. 1	6940768
05. 17. 12. 1	6940769
05. 17. 13. 1	6940770
05. 17. 14. 1	6940771
05. 17. 15. 1	6940772
05. 17. 16. 1	6940773
05. 17. 17. 1	6940774
05. 18. 01. 1	6942772
05. 18. 02. 1	6942773
05. 19. 01. 1	6940657
05. 19. 02. 1	6940658
05. 19. 03. 1	6940659
05. 19. 04. 1	6940660
05. 19. 05. 1	6940661
05. 19. 06. 1	6940680
05. 20. 01. 1	6941355
05. 21. 01. 1	6940250
05. 22. 01. 1	6941353
05. 22. 02. 1	6941354
05. 22. 03. 1	6941362
05. 23. 01. 1	6941363
05. 23. 02. 1	6941364

Figure 10-1. LVDAME Automated Logic Diagram Part Numbers (Sheet 3)

10-9. The second level logic diagrams (figure 10-50) are provided to aid in the logical analysis of the LVDAME. These diagrams are arranged by LVDAME functions. Included with these diagrams is the chart of logic symbol definitions (figure 10-50, sheets 1 and 2) which define the logic symbols used in these diagrams. A block diagram (figure 10-50, sheet 3) showing the relationship of the LVDAME functions is also included.

NOTE

The Logic Symbols listing (located at the end of this Volume) also defines each second level logic symbol and the corresponding ALD symbol.

10-10. In the lower left corner of each second level logic diagram except sheets 1, 2, and 3 is a table which lists (by LN number) the ALD pages that are represented on the diagram.

10-11. In the upper left corner of each second level diagram except sheets 1, 2, and 3 are tables that list (by sheet number) the origins of the input signals to the sheet and the destinations of the outputs from the sheet; however, common timing signals and signals whose origin or destination is on the Electrical Schematic Diagrams are not listed in these tables.

10-12. AUTOMATED LOGIC DIAGRAMS (ALD's).

10-13. PAGE LAYOUT. Each ALD page contains page identification, edge information, logic blocks, connecting lines, and an area for comments. Figure 10-2 shows a typical logic page. Each page has a possible logic format of five blocks wide and nine blocks long, so logic blocks can occupy any of 45 possible positions.

10-14. PAGE IDENTIFICATION. As shown on figure 10-2, the following information appears at the top of each logic diagram page:

a. Page part number (1), used for ordering a specific page or series of pages.

b. Title (2), a description of the logic contained on the page.

c. Equipment name or code number (3).

d. Logic page (LN) number (4), a seven-digit number (05. xx. xx. x) assigned to the page. (Refer to paragraph 10-5 for the explanation of the seven digits in the LN number.)

10-15. SIGNAL LINES. All lines entering or leaving a logic page are labeled to correspond to the labeling on the logic page to which they interconnect. Lines enter on the left side of the page and leave on the right side of the page. If a line leaves a page and goes to several locations on another page, the line is usually distributed on the destination page and not the origin page. If a line leaves a page and goes to several other pages, it is shown as a branched line on the origin page.

10-16. EDGE INFORMATION. Data shown at the extreme left and extreme right of each page are called edge information. Edge information includes names of input and

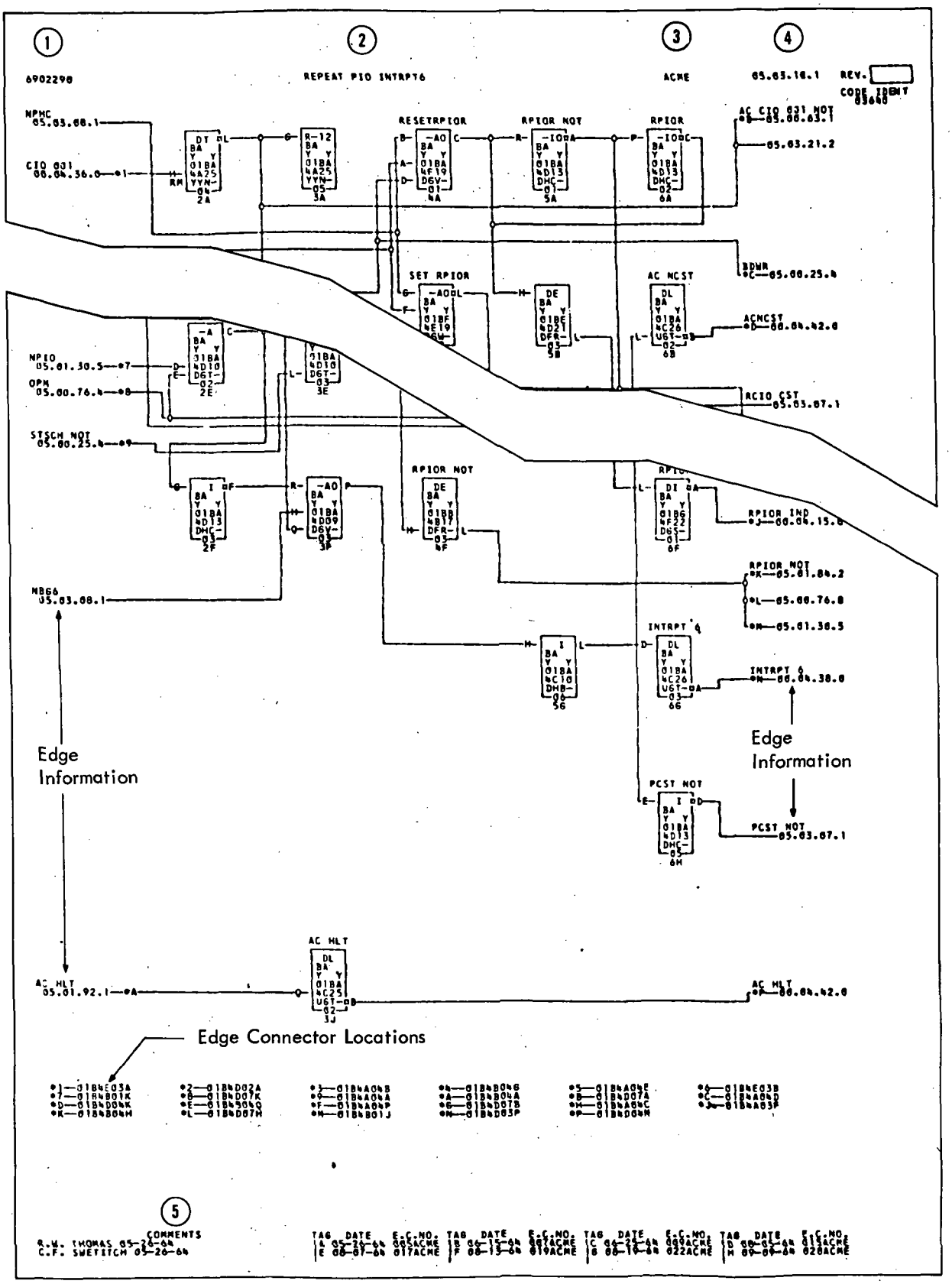


Figure 10-2. Typical Logic Page

output signals, and numbers of the logic pages on which these signals also appear. The first line (and second line, if necessary) contains the signal name. The last line lists the number of the logic page on which the signal appears again. The logic page number is directly opposite the signal line.

10-17. EDGE CONNECTORS. When a signal or service wire enters or leaves a gate assembly, it may be routed through an edge connector. An edge connector is a modified SMS card whose contacts lead to an inter-chassis cable instead of to a printed circuit. An edge connector plugs into an SMS card receptacle exactly like a standard SMS card. An edge connector is so called because it is usually plugged into a receptacle near one edge of a gate assembly.

10-18. On ALD pages, a signal line connected to an edge connector is indicated by an asterisk or lozenger and a number or letter combination (for example, *2, *C, ⌑ 1, ⌑F, 1 ⌑, etc.) located on the entry or exit line. This notation refers to an entry in the table of edge connector locations and pin letters near the bottom of the ALD page.

10-19. Edge connector locations and pin letters are given in the standard SMS card location code. (See figure 10-2.) For example, *1--01A8A25A indicates that the signal line designated *1 (in the upper left corner of figure 10-2) is routed through the edge connector in frame 01, gate assembly A8, column A, position 25, via pin A of this edge connector.

10-20. LOGIC BLOCKS. The logic blocks represent the SMS card circuits. A basic logic function is usually represented by a single block, but some functions may require more than one block. In the case of multiple circuits on one SMS card, each circuit is represented by a separate logic block. The standard format of the logic block is shown on figure 10-3; salient features are as follows:

a. Timing. The timings of special circuits, such as single shots, oscillators, and delays, are printed above the logic blocks.

b. Functional Symbol. This symbol consists of a sign (when used) and letter(s) that indicate the type of circuit.

c. Machine Feature Index. This code indicates the configuration of the equipment. BA indicates the basic configuration.

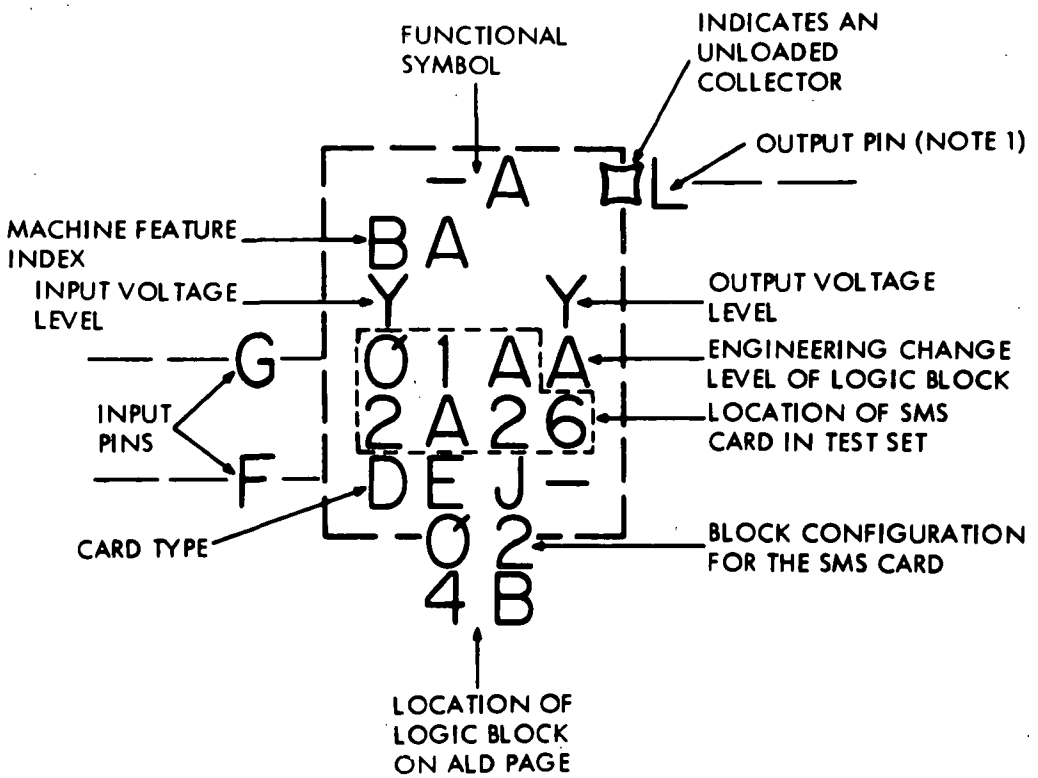
d. Voltage Levels. These two code letters indicate the nominal levels of input and output voltage. The Y symbol indicates "0" = 0 vdc and "1" = -6 vdc.

e. Card Location. The location of an SMS card in the gate assemblies is indicated by a seven-character code; for example, 02B3F22 indicates that a card is located in frame 02, gate assembly B3, column F, position 22.

f. Card Type. The type of SMS card is indicated by a four-character alphanumeric code.

g. Block Configuration Code. Most SMS cards contain more than one circuit. The circuit used for a particular logic function is indicated by the two-digit block configuration code.

h. Logic Block Location. Each ALD page is composed on a grid containing seven columns (designated 1 through 7, left to right) and nine rows A through H and J, top to



NOTES:

1. IF THE OUTPUT PIN IS SHOWN IN THE TOP HALF OF THE LOGIC BLOCK, THE OUTPUT IS OUT OF PHASE WITH THE INPUT(S). IF THE OUTPUT PIN IS SHOWN IN THE BOTTOM HALF OF THE LOGIC BLOCK, THE OUTPUT IS IN PHASE WITH THE INPUT(S).

2. ADJACENT PIN LETTERS (ON EITHER SIDE OF THE BLOCK) INDICATE THAT THESE PINS ARE JUMPERED TOGETHER.

Figure 10-3. Typical Logic Block

bottom). A logic block may occupy any of the 45 locations in columns 2 through 6 (columns 1 and 7 are reserved for edge information); each location is designated by a two-character code designating the column and row.

10-21. COMMENTS. An area (5 on figure 10-2) at the bottom of each ALD page is reserved for comments. These comments usually indicate the designer(s) and the dates and numbers of the revisions that have been made to this ALD page.

10-22. CIRCUIT CARD LOCATION CHARTS.

10-23. The circuit card location charts (included with the ALD's) designate the SMS card (by type and IBM part number) used in each card location on the gate assemblies. These charts also indicate the total number of block configurations for that card and the ALD page(s) on which a logic block representing a circuit on that card is shown; each page entry indicates one logic block printed on that page.

10-24. EDGE CONNECTOR LISTS.

10-25. The edge connector lists (included with the ALD's) list the edge connectors for each SMS gate assembly, the signal present on each edge connector pin, and the ALD page (by LN number) on which the edge connector pin and signal are shown.

10-26. ASSEMBLY DRAWINGS.

10-27. The assembly drawings are provided to aid in the location of replaceable parts. Only the assembly drawings that are required for part replacement are included in this section.

NOTE

Many assembly drawings contain notes referring to IBM specifications; these notes are for manufacturing purposes only and should be disregarded for maintenance purposes.

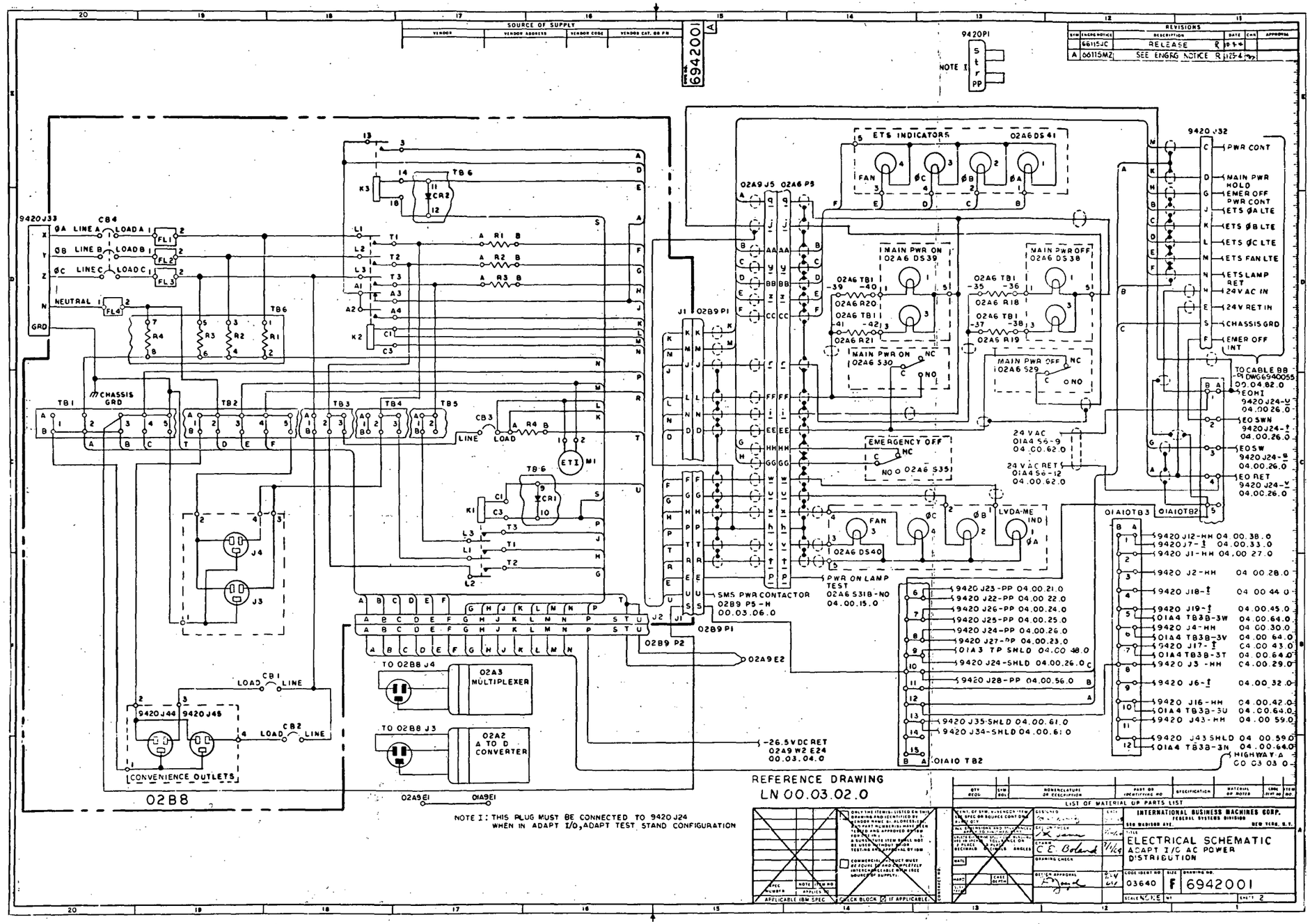


Figure 10-4. Power Distribution Electrical Schematic Diagram (LN 00. 03. 02. 0 through LN 00. 03. 06. 0) (Sheet 1 of 5)

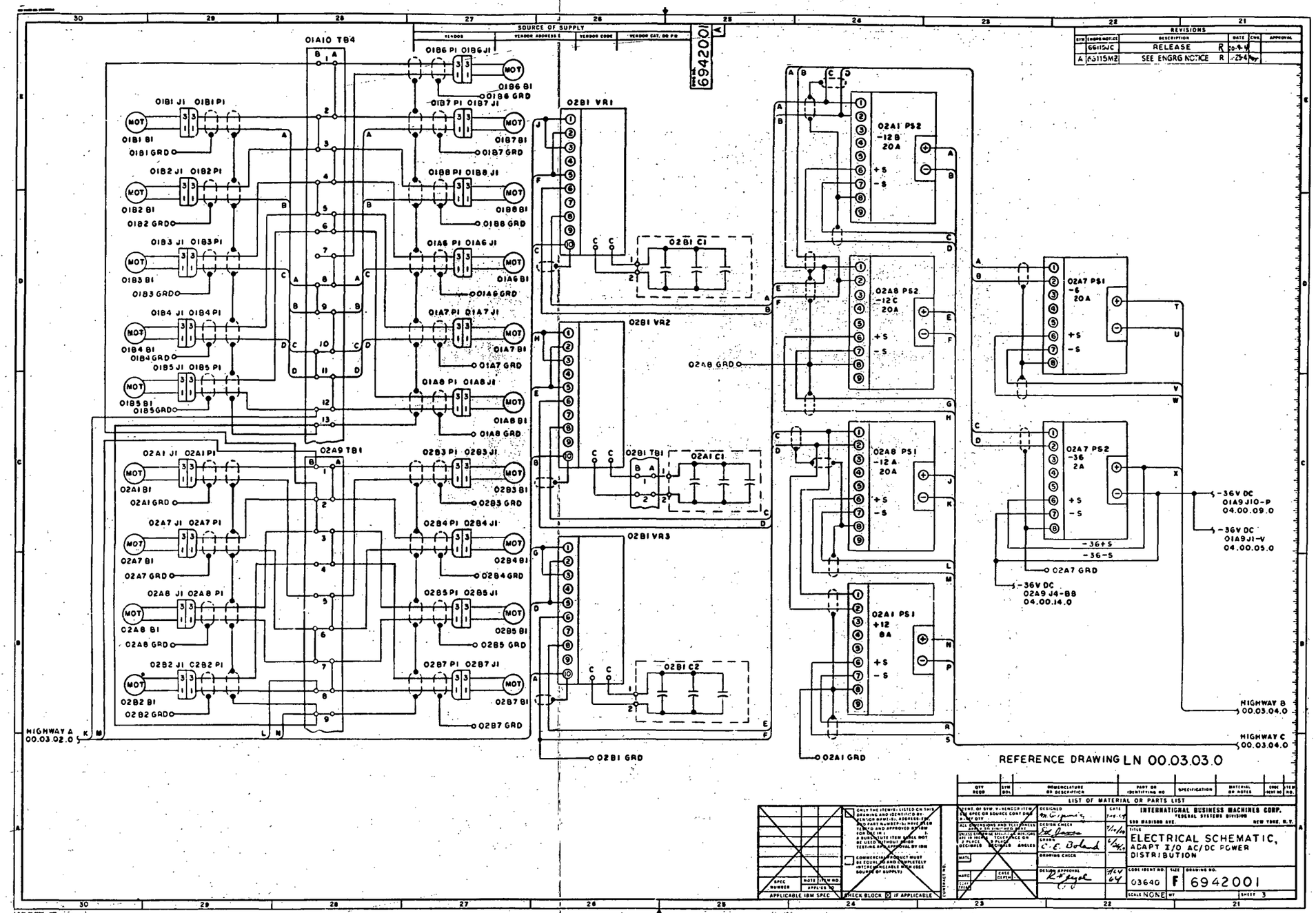


Figure 10-4. Power Distribution Electrical Schematic Diagram (LN 00.03.02.0 through LN 00.03.06.0) (Sheet 2)

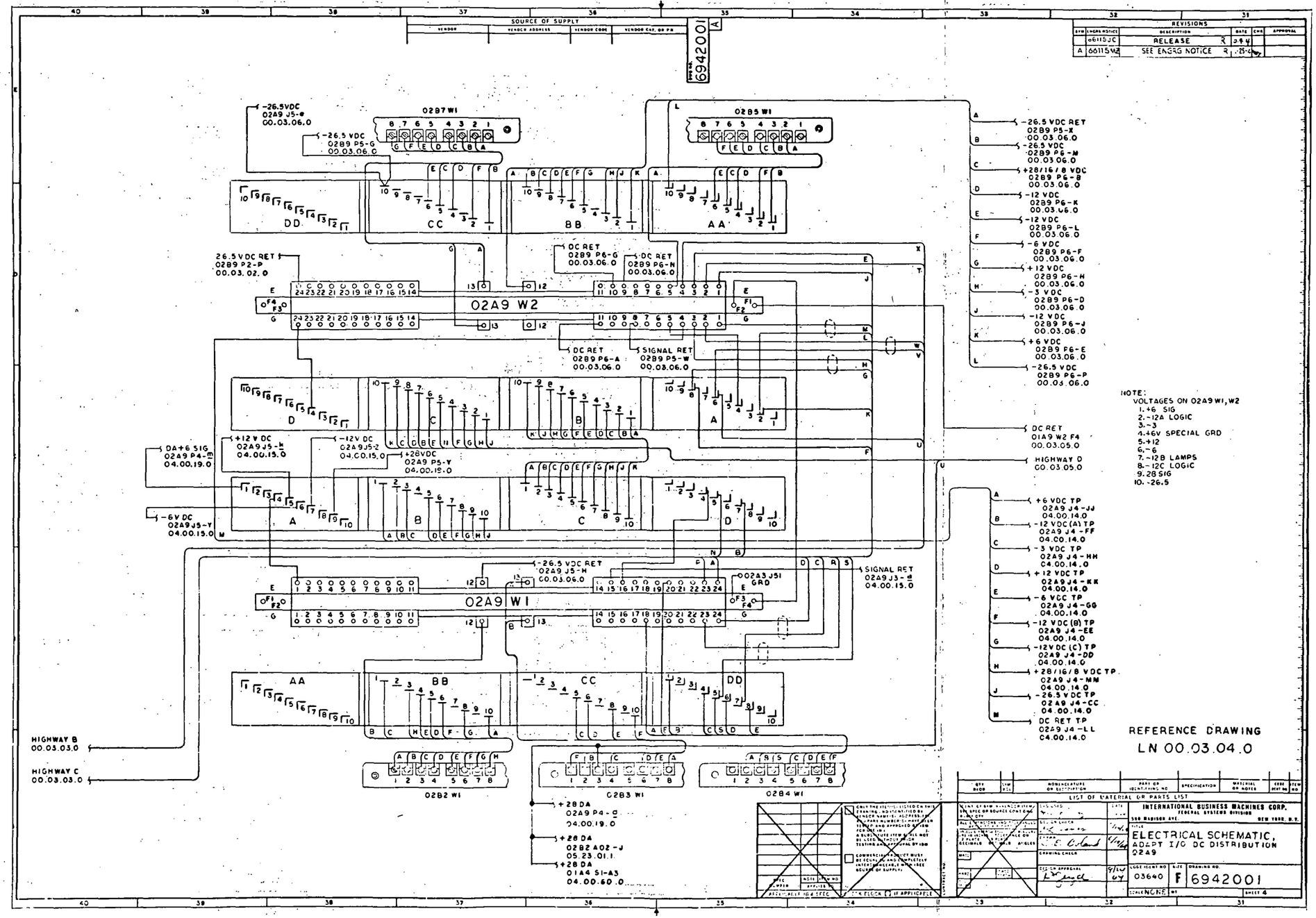


Figure 10-4. Power Distribution Electrical Schematic Diagram (LN 00.03.02.0 through LN 00.03.06.0) (Sheet 3)

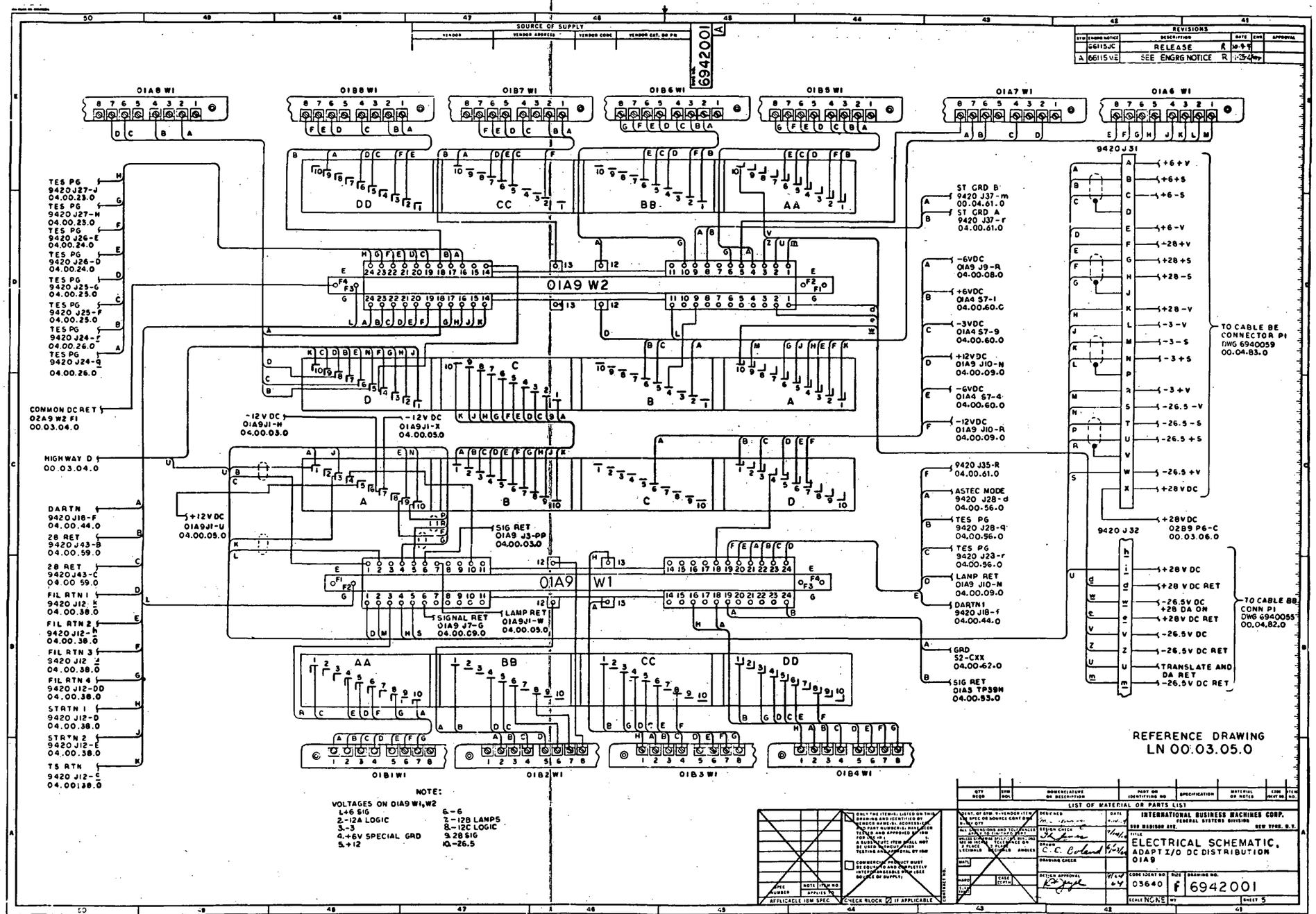


Figure 10-4. Power Distribution Electrical Schematic Diagram (LN 00.03.02.0 through LN 00.03.06.0) (Sheet 4)

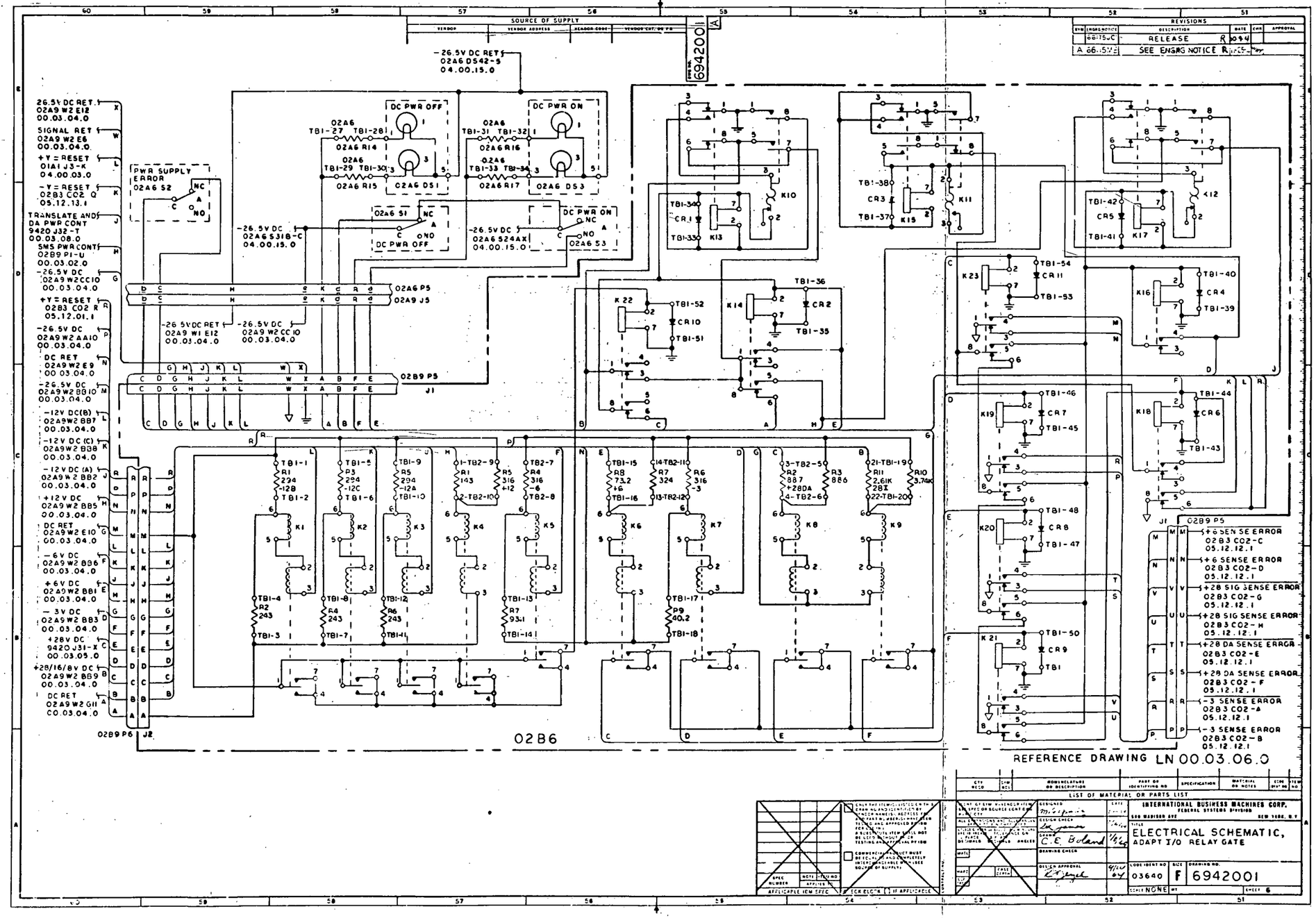


Figure 10-4. Power Distribution Electrical Schematic Diagram (LN 00. 03. 02. 0 through LN 00. 03. 06. 0) (Sheet 5)

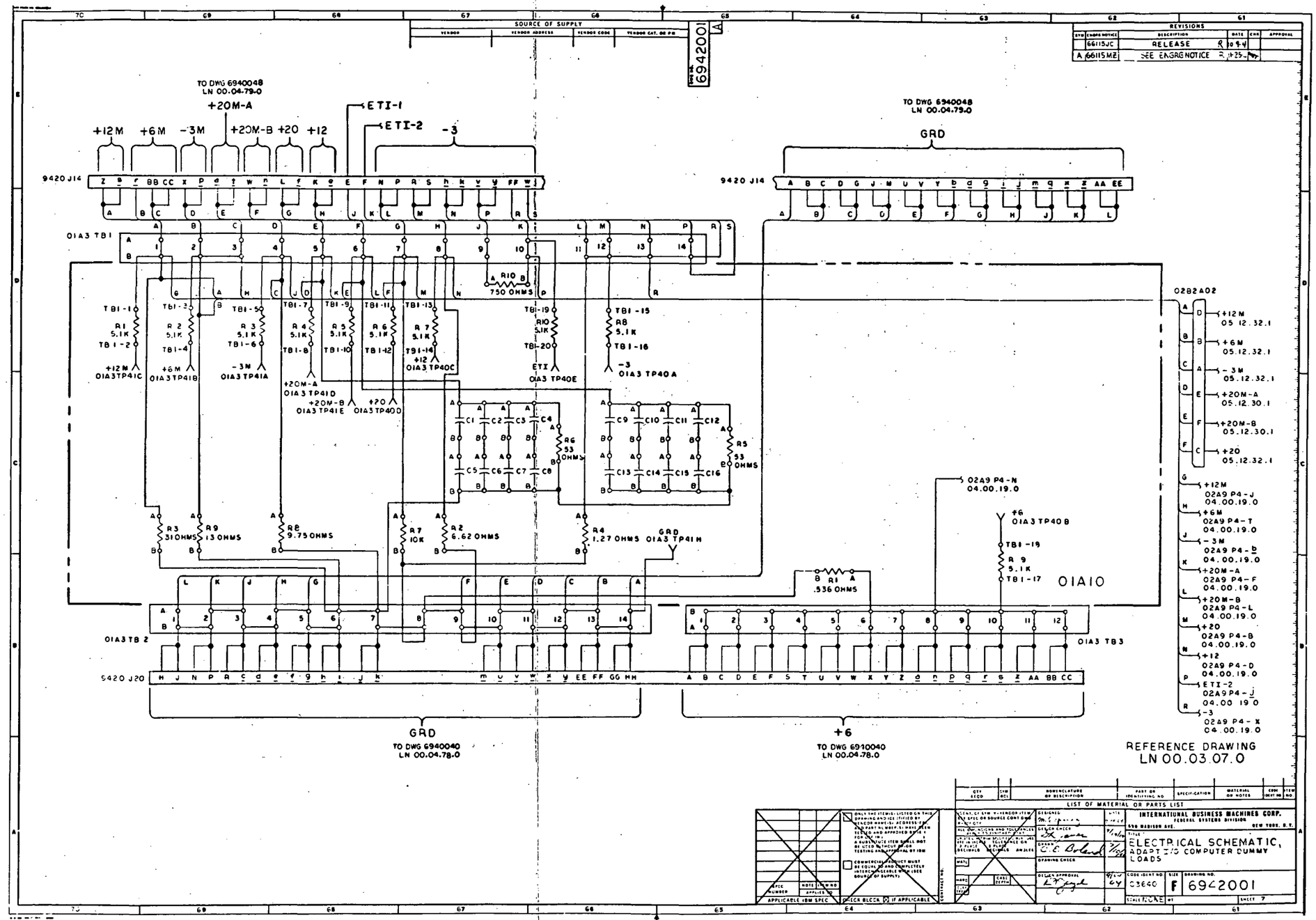


Figure 10-5. Computer Dummy Loads Electrical Schematic Diagram (LN 00.03.07.0)

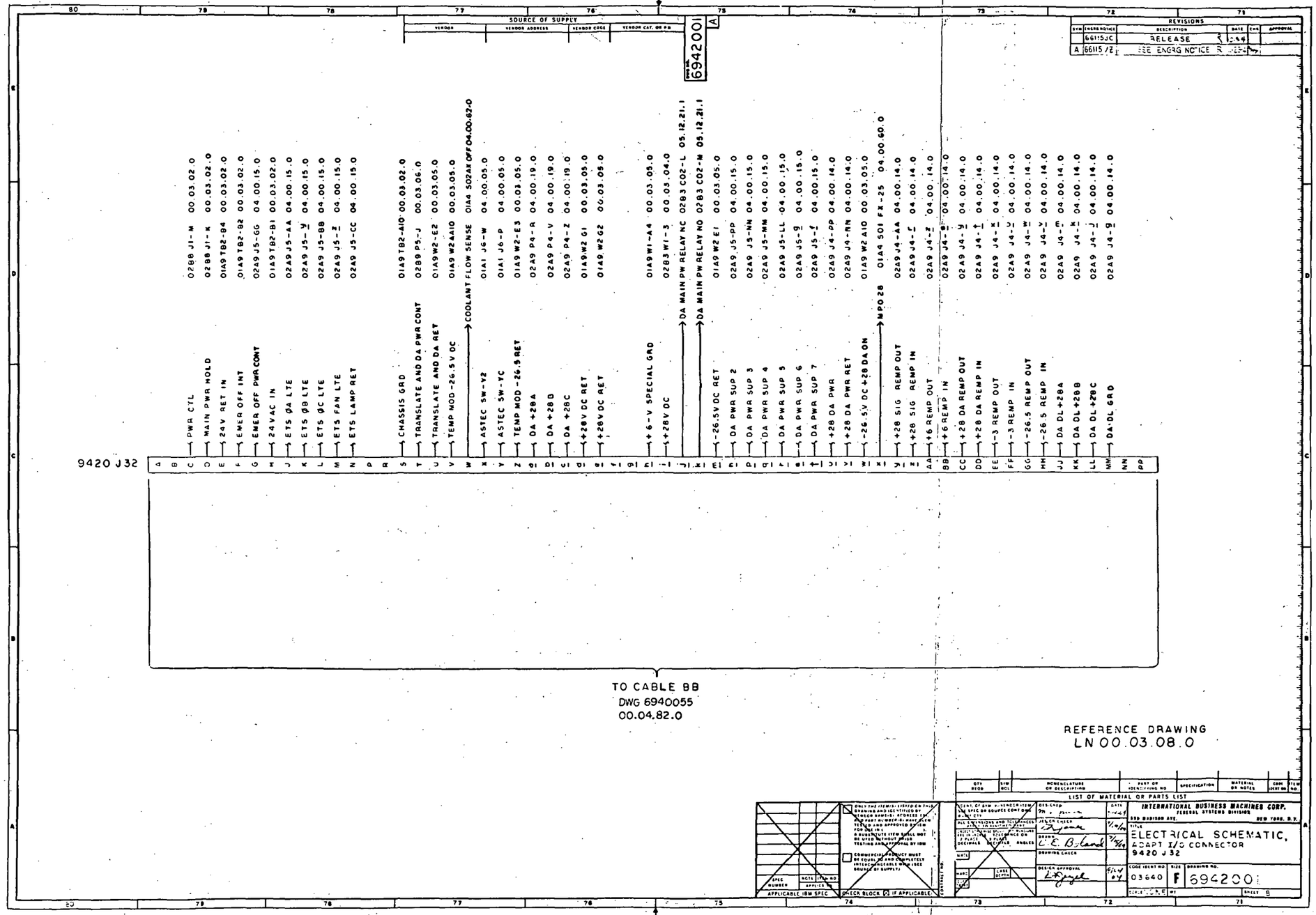


Figure 10-6. Connector 9420 J32 Electrical Schematic Diagram (LN 00.03.08.0)

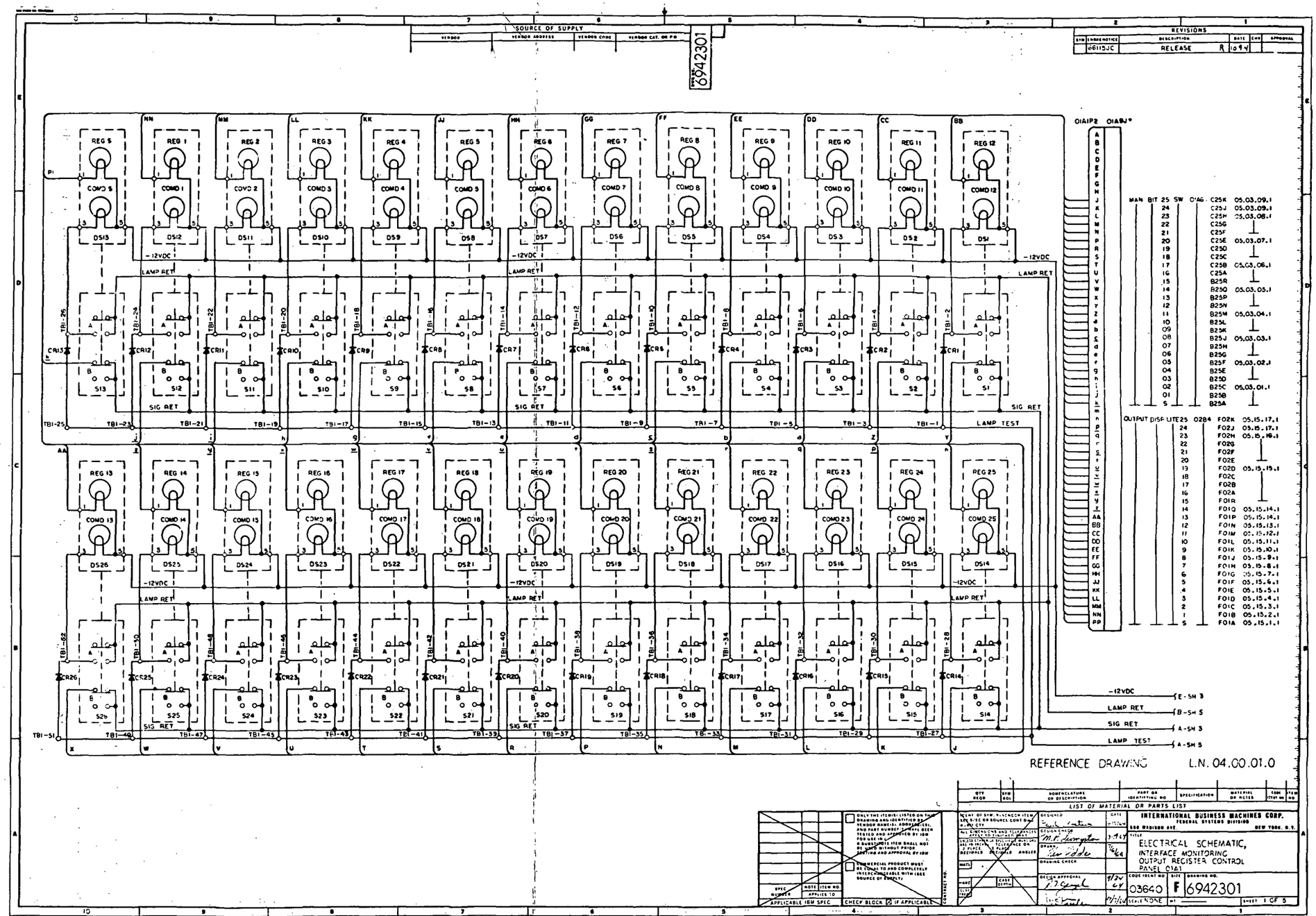


Figure 10-7. Interface Monitoring Panel (01A1) Electrical Schematic Diagram (LN 04.00.01.0 through LN 04.00.05.0) (Sheet 1 of 5)

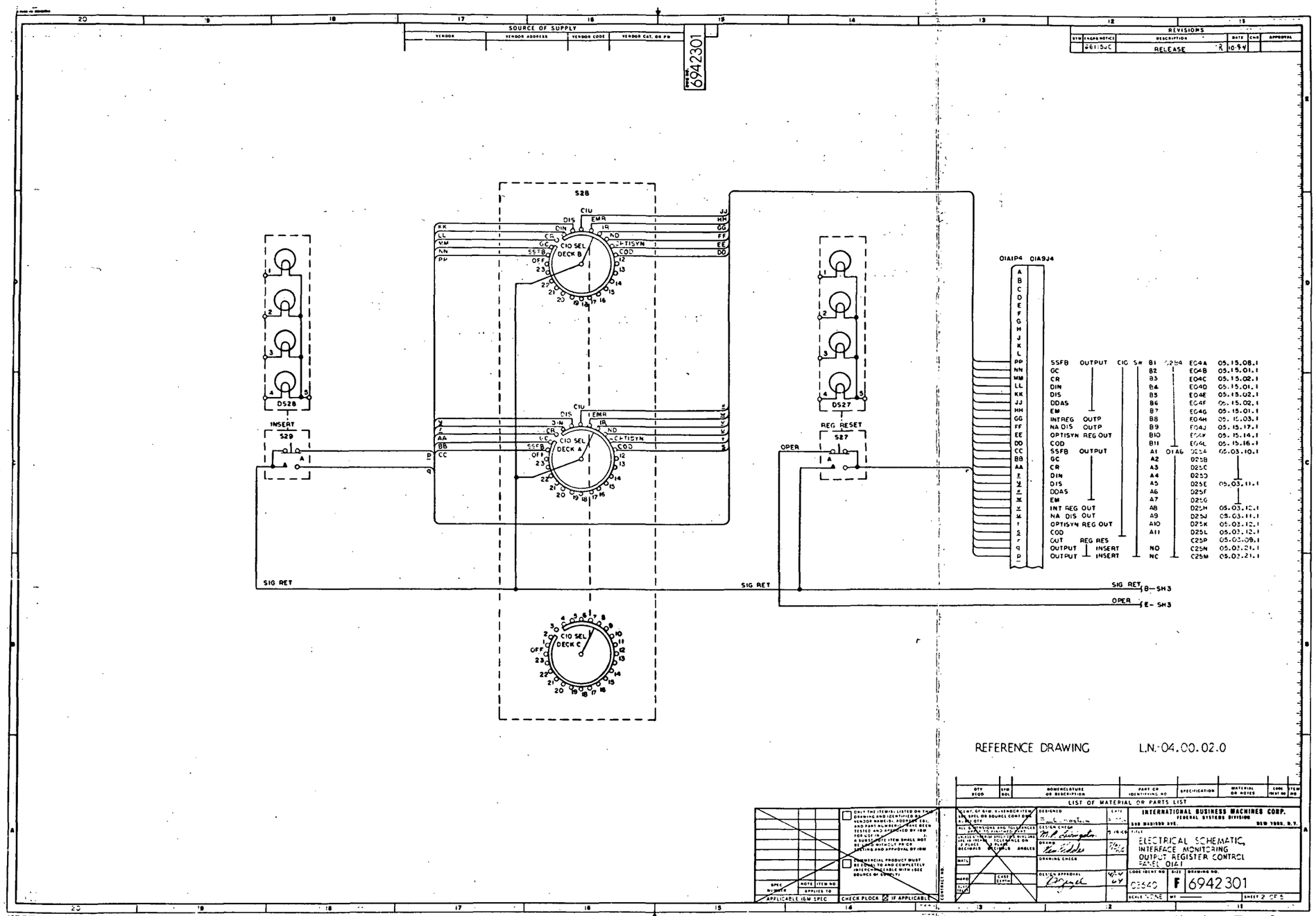


Figure 10-7. Interface Monitoring Panel (01A1) Electrical Schematic Diagram (LN 04.00.01.0 through LN 04.00.05.0) (Sheet 2)

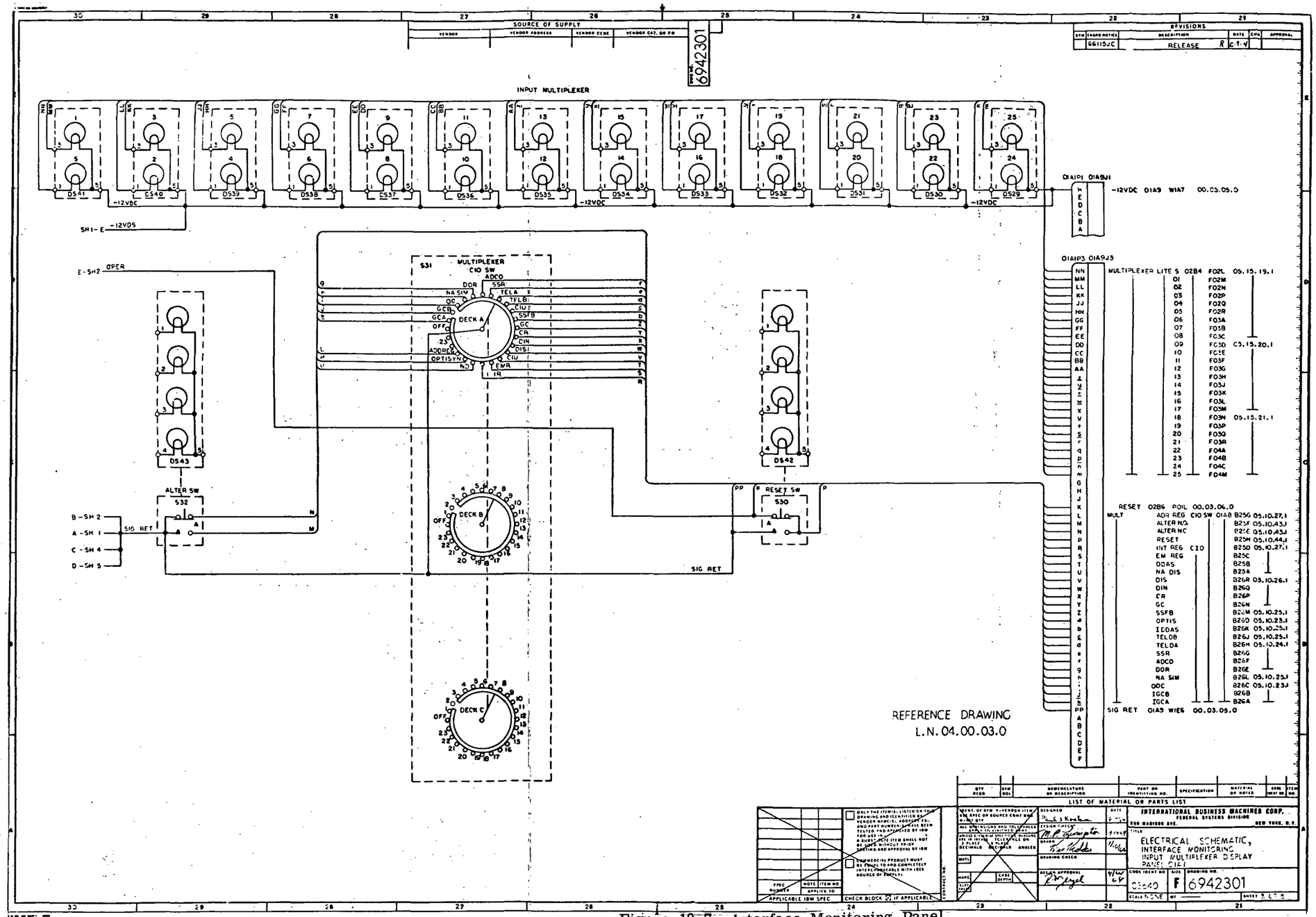


Figure 10-7. Interface Monitoring Panel (01A1) Electrical Schematic Diagram (LN 04.00.01.0 through LN 04.00.05.0) (Sheet 3)

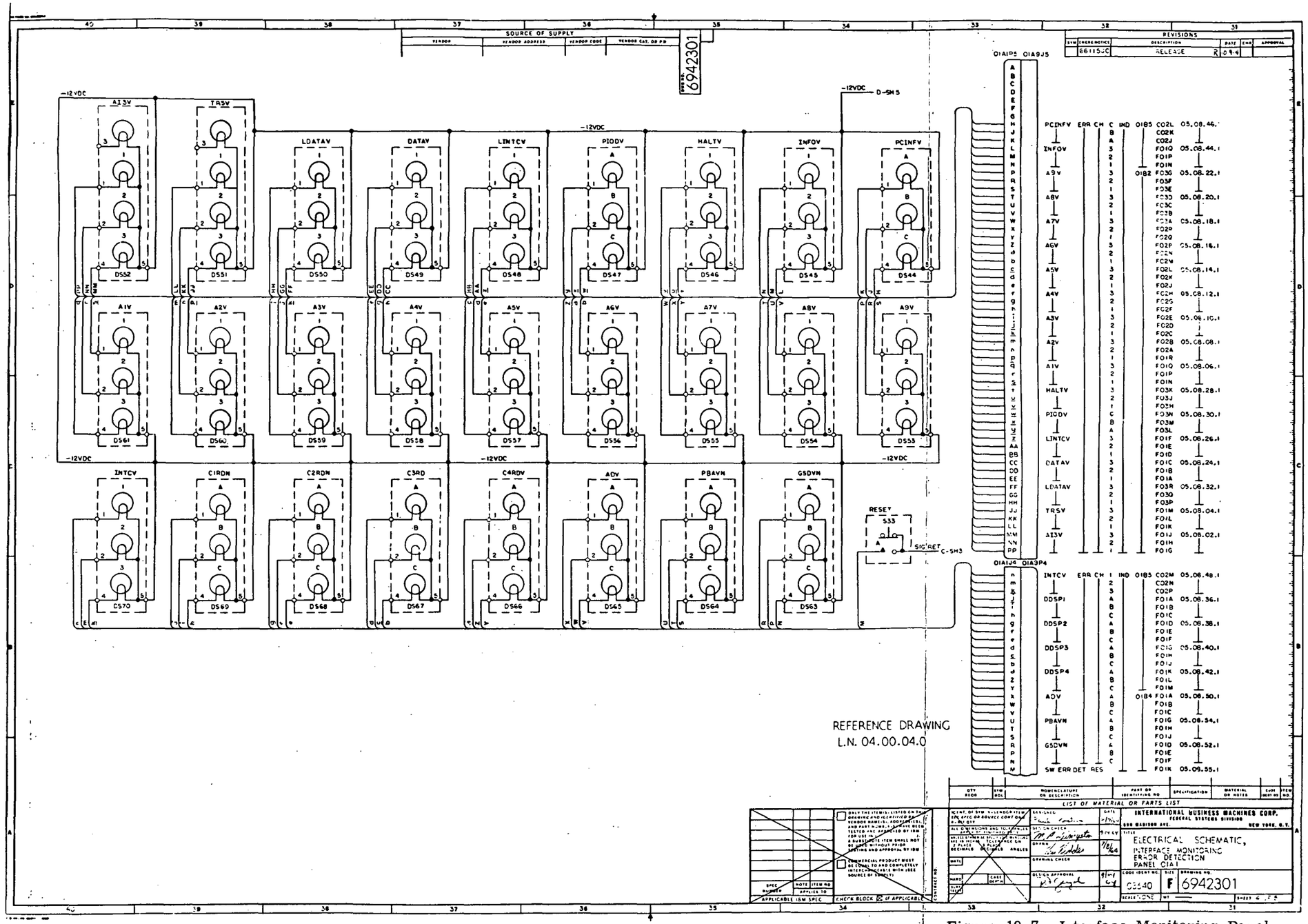


Figure 10-7. Interface Monitoring Panel (01A1) Electrical Schematic Diagram (LN 04.00.01.0 through LN 04.00.05.0) (Sheet 4)

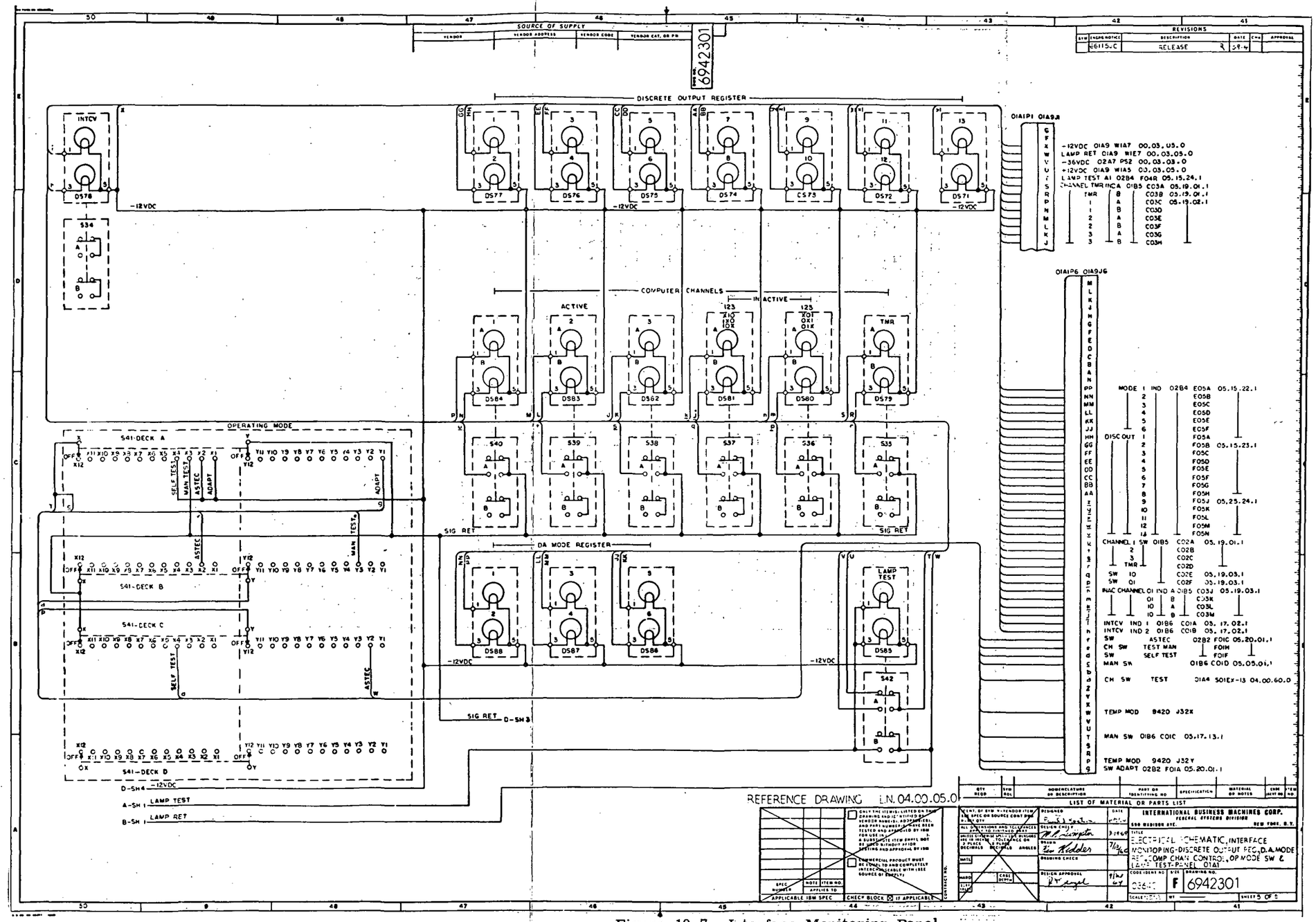


Figure 10-7. Interface Monitoring Panel (01A1) Electrical Schematic Diagram (LN 04.00.01.0 through LN 04.00.05.0) (Sheet 5)

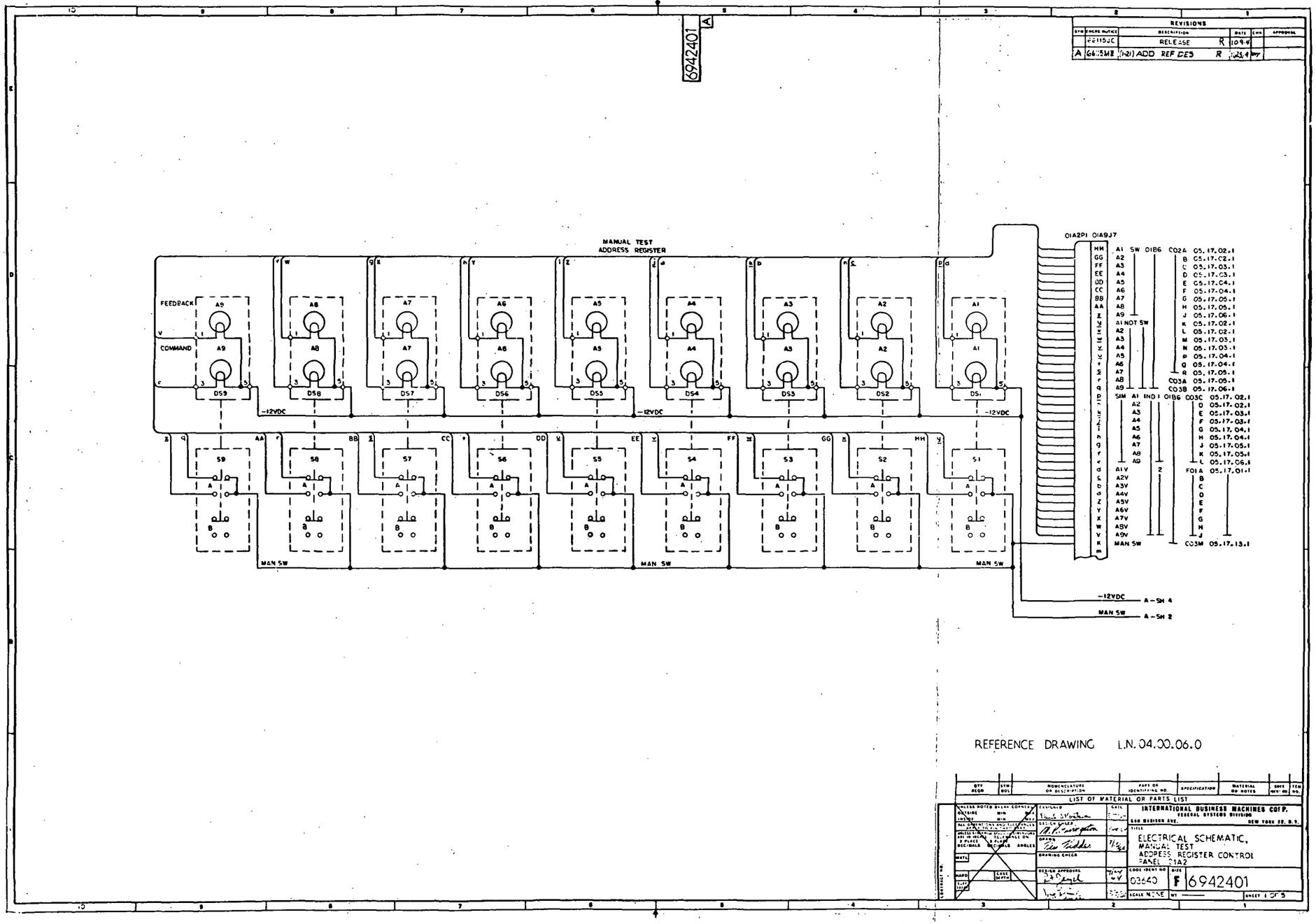


Figure 10-8. Manual Test Panel (01A2) Electrical Schematic Diagram (LN 04.00.06.0 through LN 04.00.10.0) (Sheet 1 of 5)

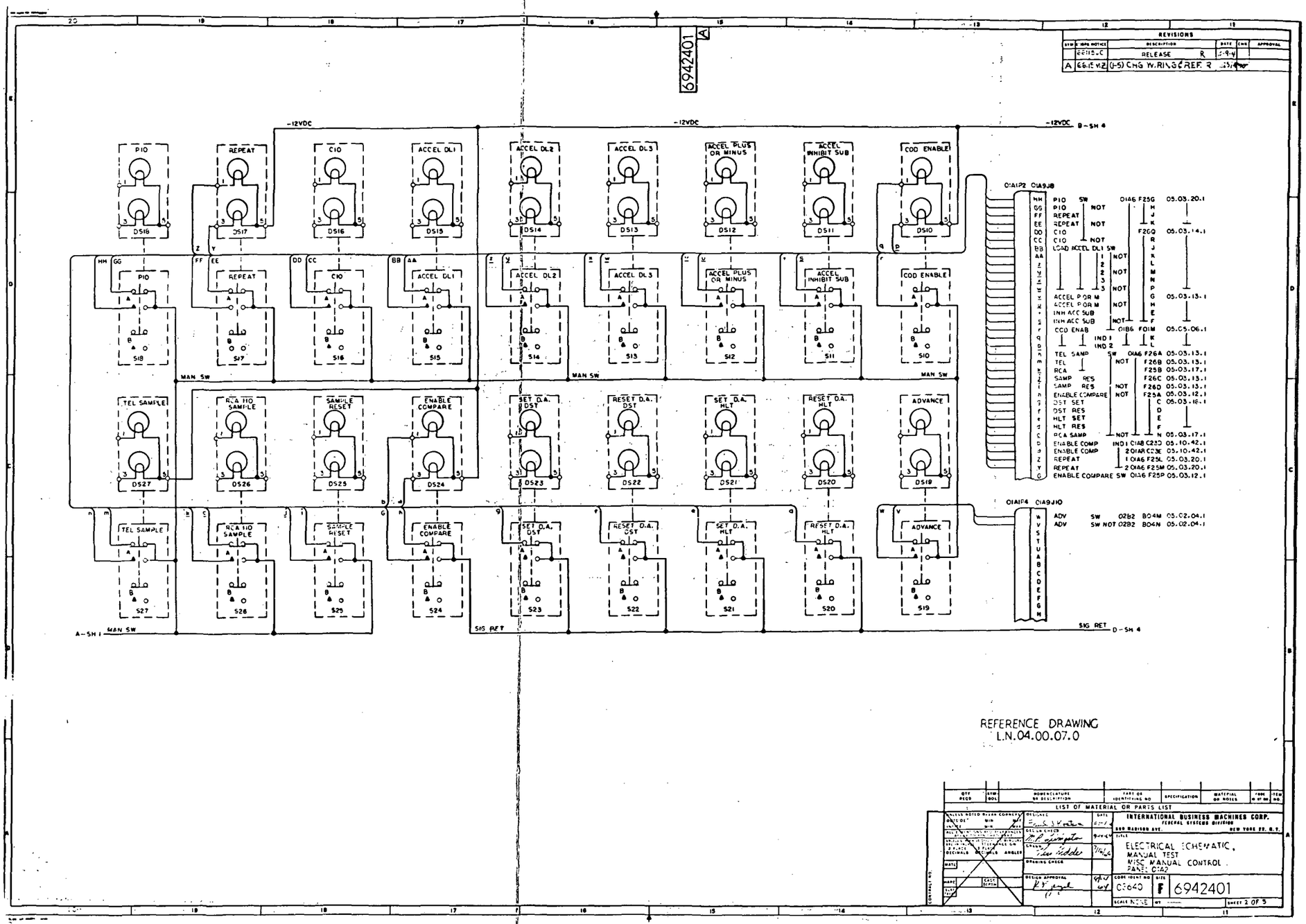


Figure 10-8. Manual Test Panel (01A2) Electrical Schematic Diagram (LN 04.00.06.0 through LN 04.00.10.0) (Sheet 2)

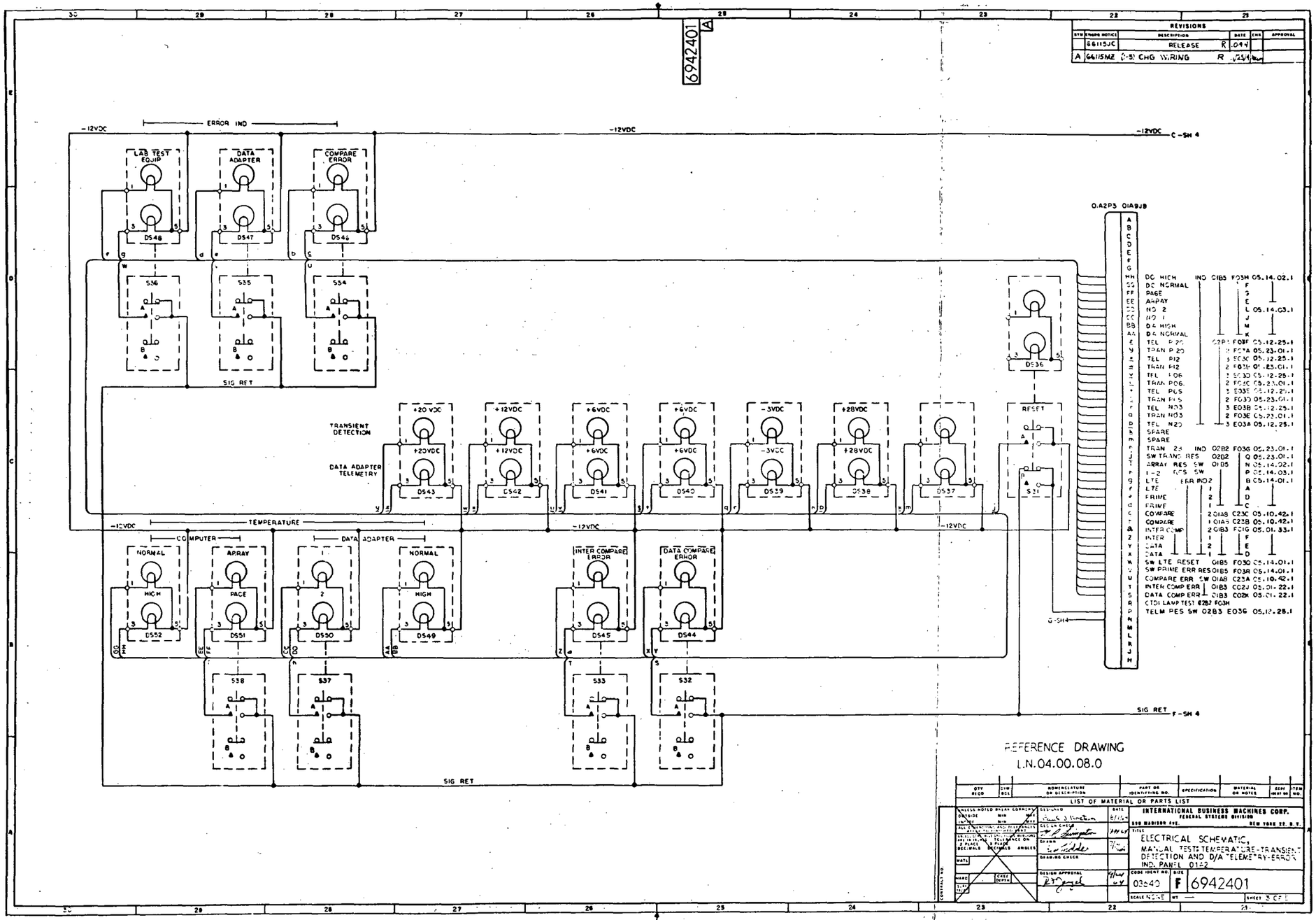


Figure 10-8. Manual Test Panel (01A2) Electrical Schematic Diagram (LN 04.00.06.0 through LN 04.00.10.0) (Sheet 3)

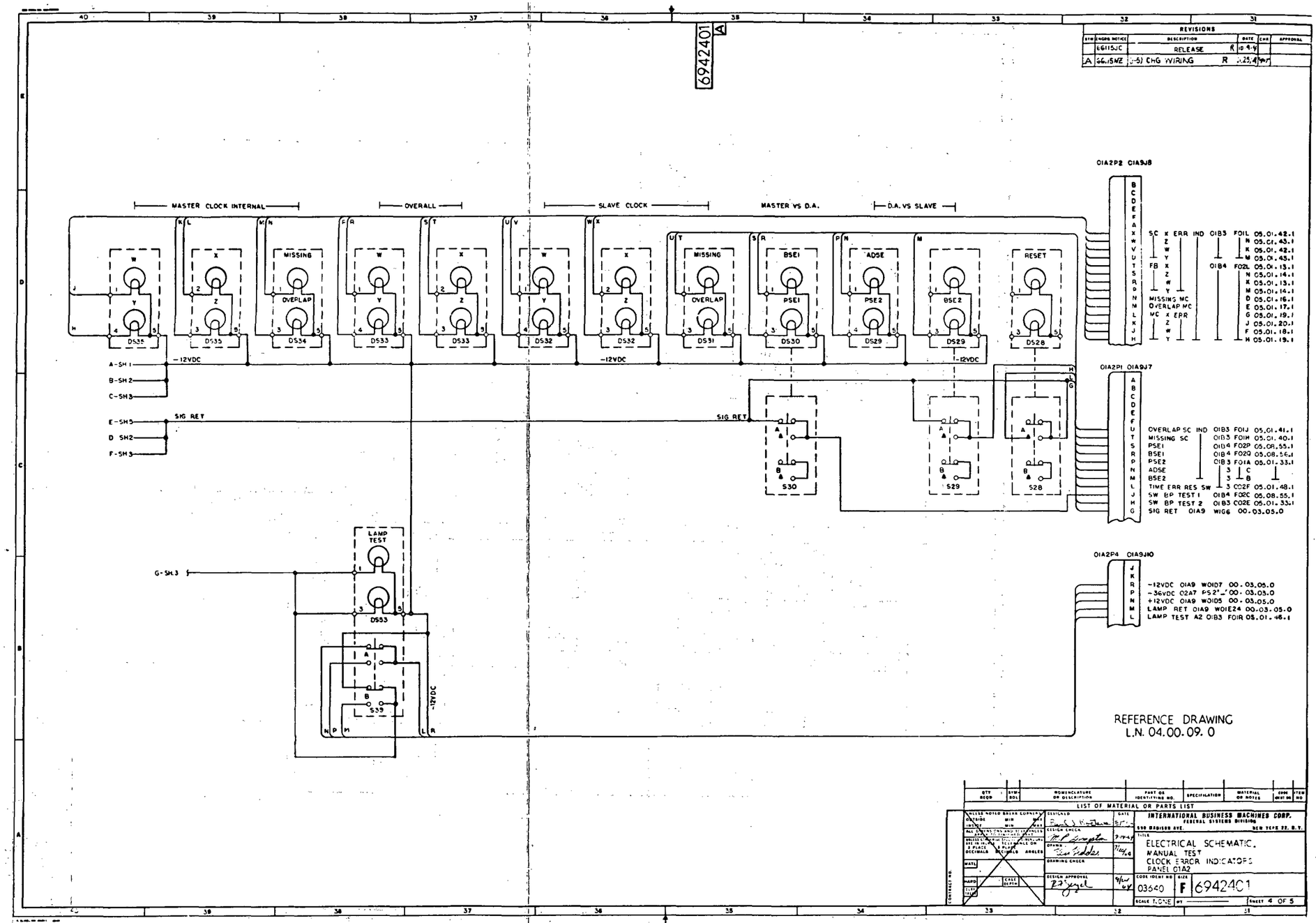


Figure 10-8. Manual Test Panel (01A2) Electrical Schematic Diagram (LN 04.00.06.0 through LN 04.00.10.0) (Sheet 4)

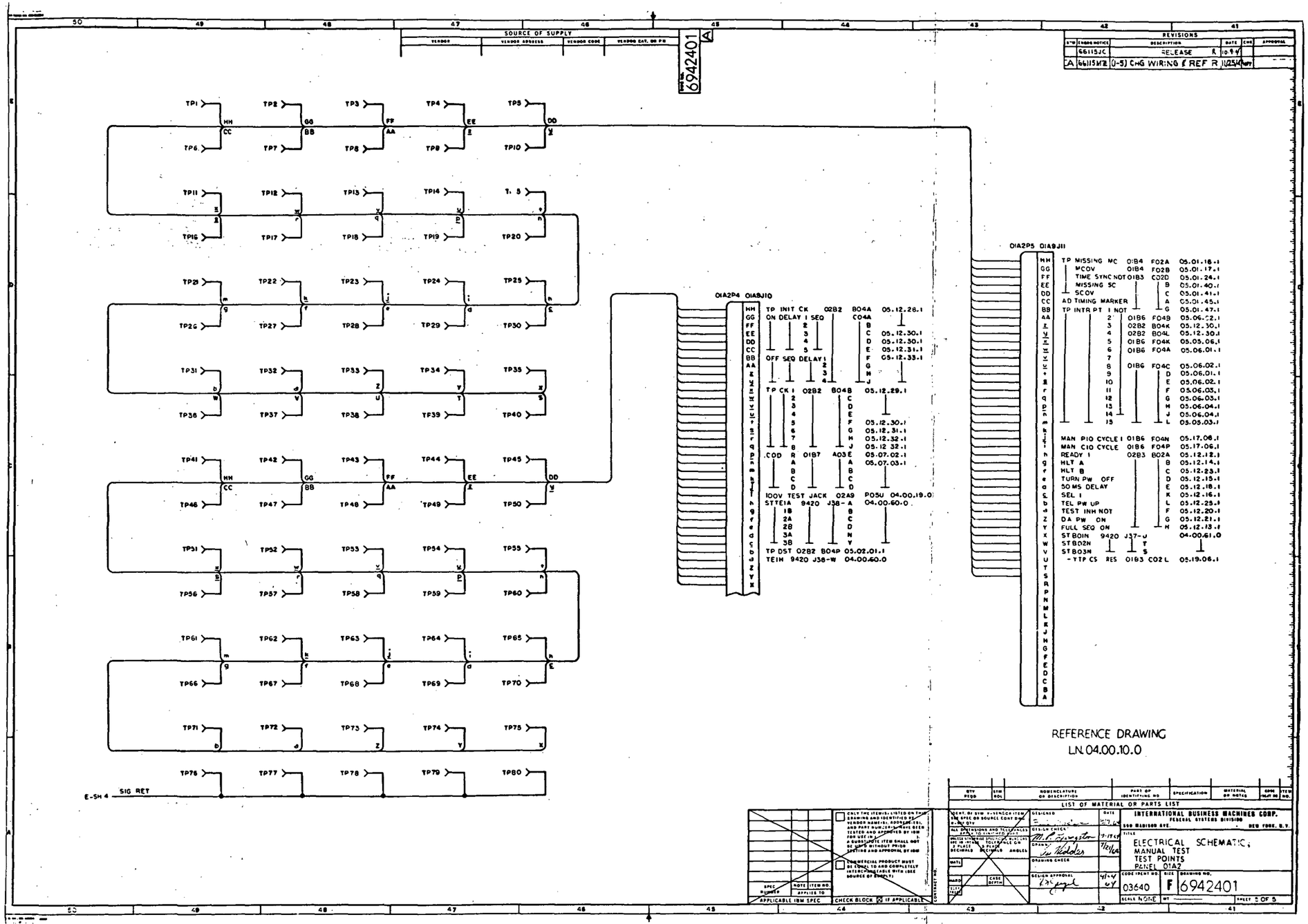


Figure 10-8. Manual Test Panel (01A2) Electrical Schematic Diagram (LN 04.00.06.0 through LN 04.00.10.0) (Sheet 5)

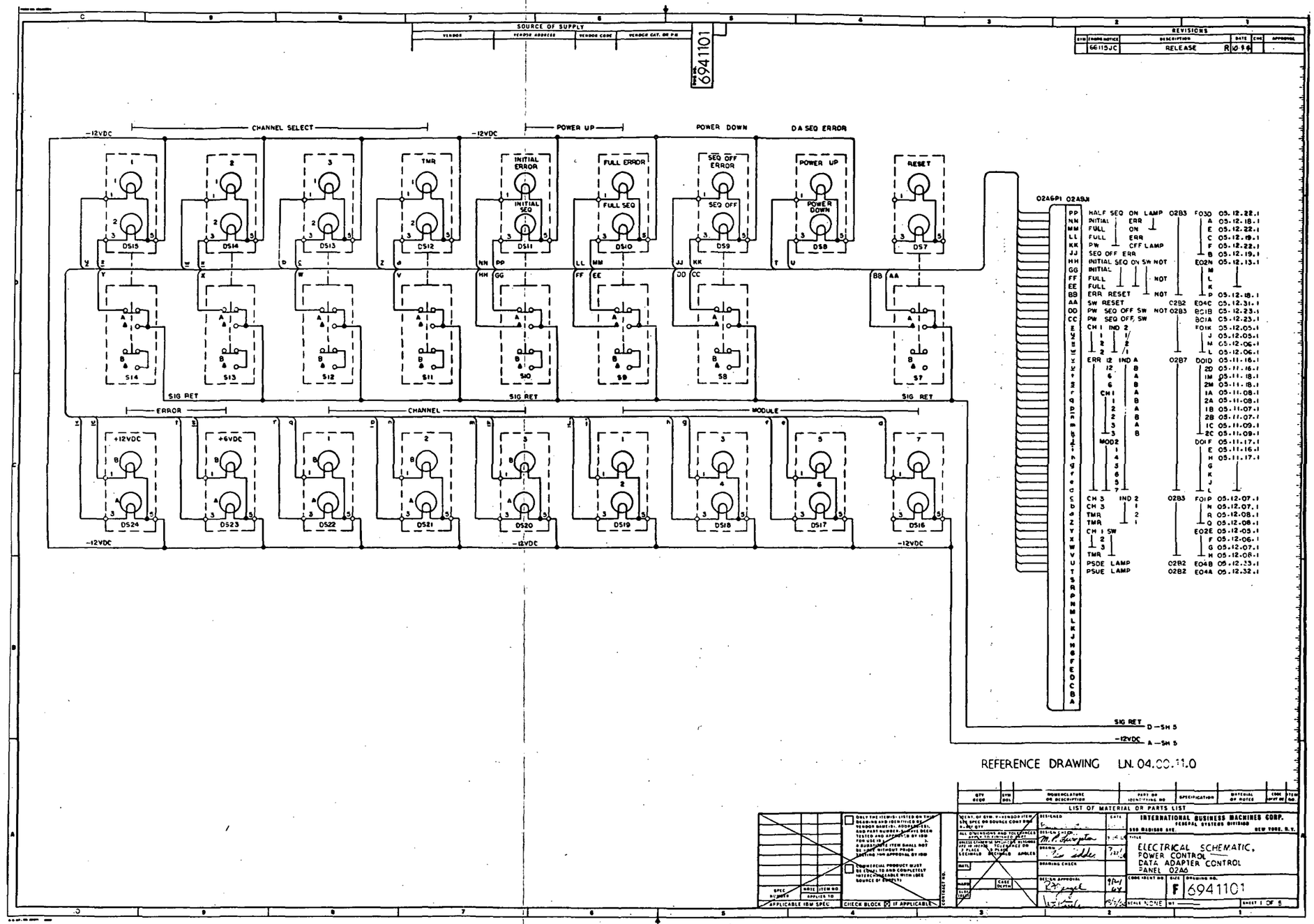


Figure 10-9. Power Control Panel (02A6) Electrical Schematic Diagram (LN 04.00.11.0 through LN 04.00.15.0) (Sheet 1 of 5)

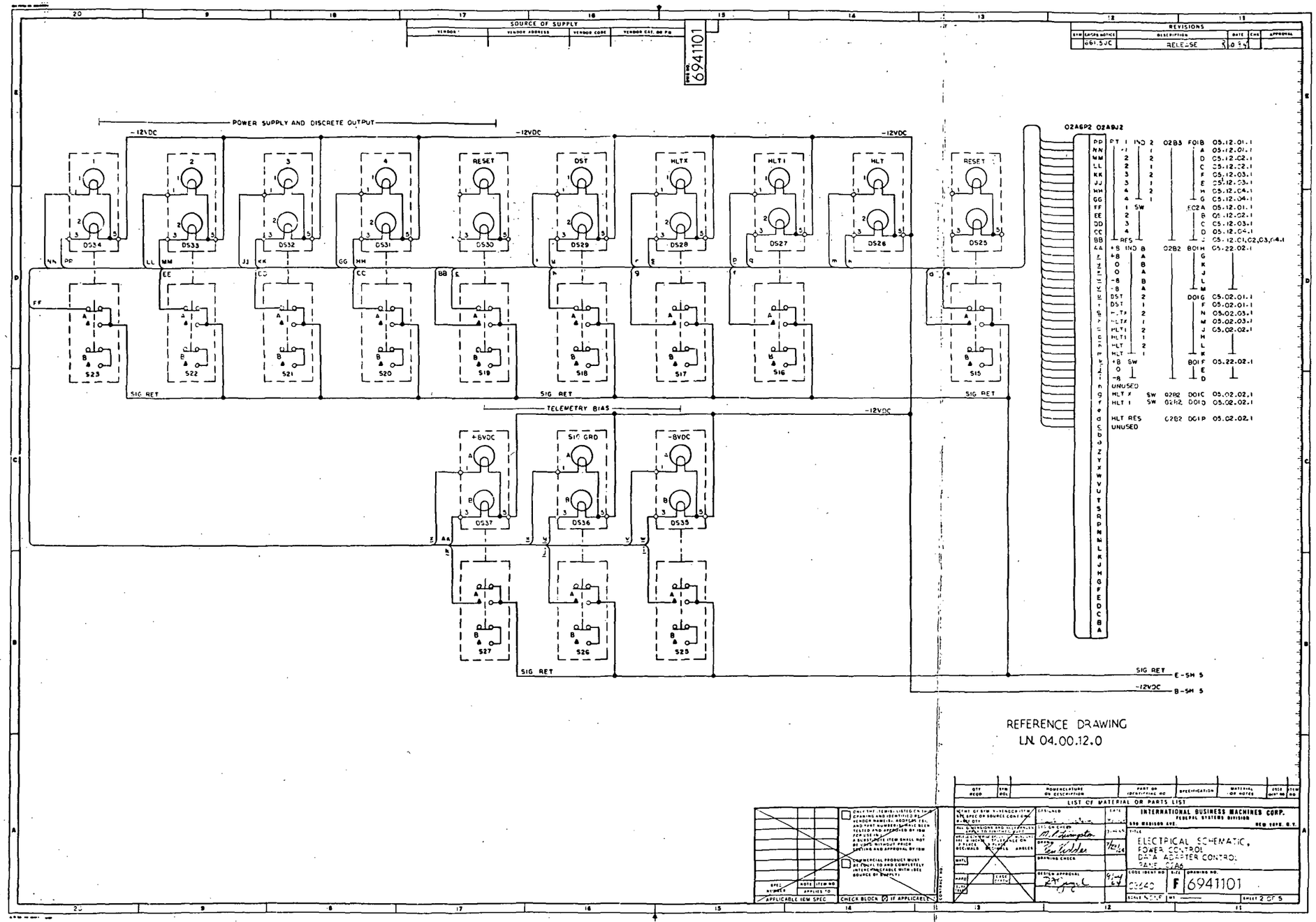


Figure 10-9. Power Control Panel (02A6) Electrical Schematic Diagram (LN 04.00.11.0 through LN 04.00.15.0) (Sheet 2)

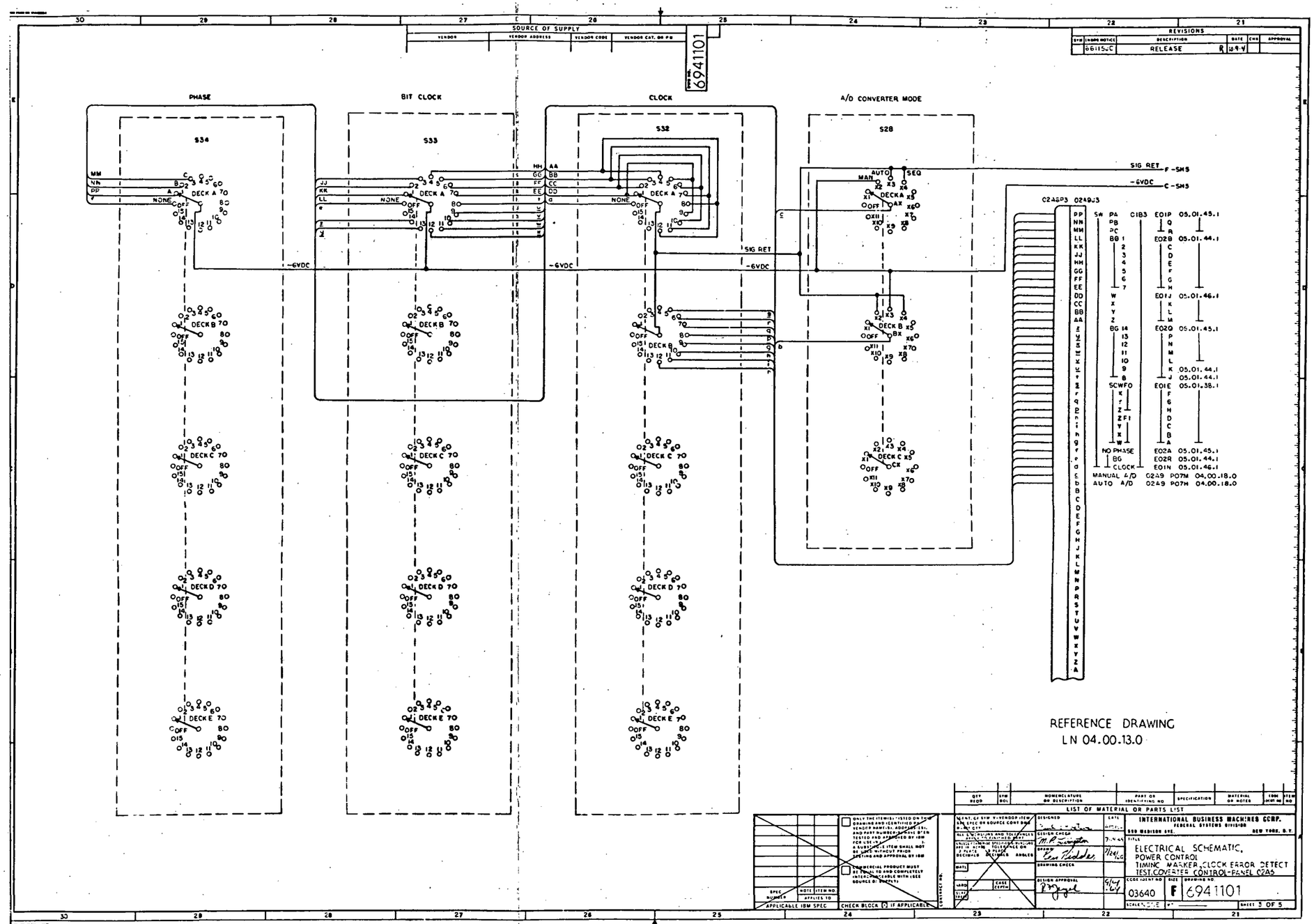


Figure 10-9. Power Control Panel (02A6) Electrical Schematic Diagram (LN 04.00.11.0 through LN 04.00.15.0) (Sheet 3)

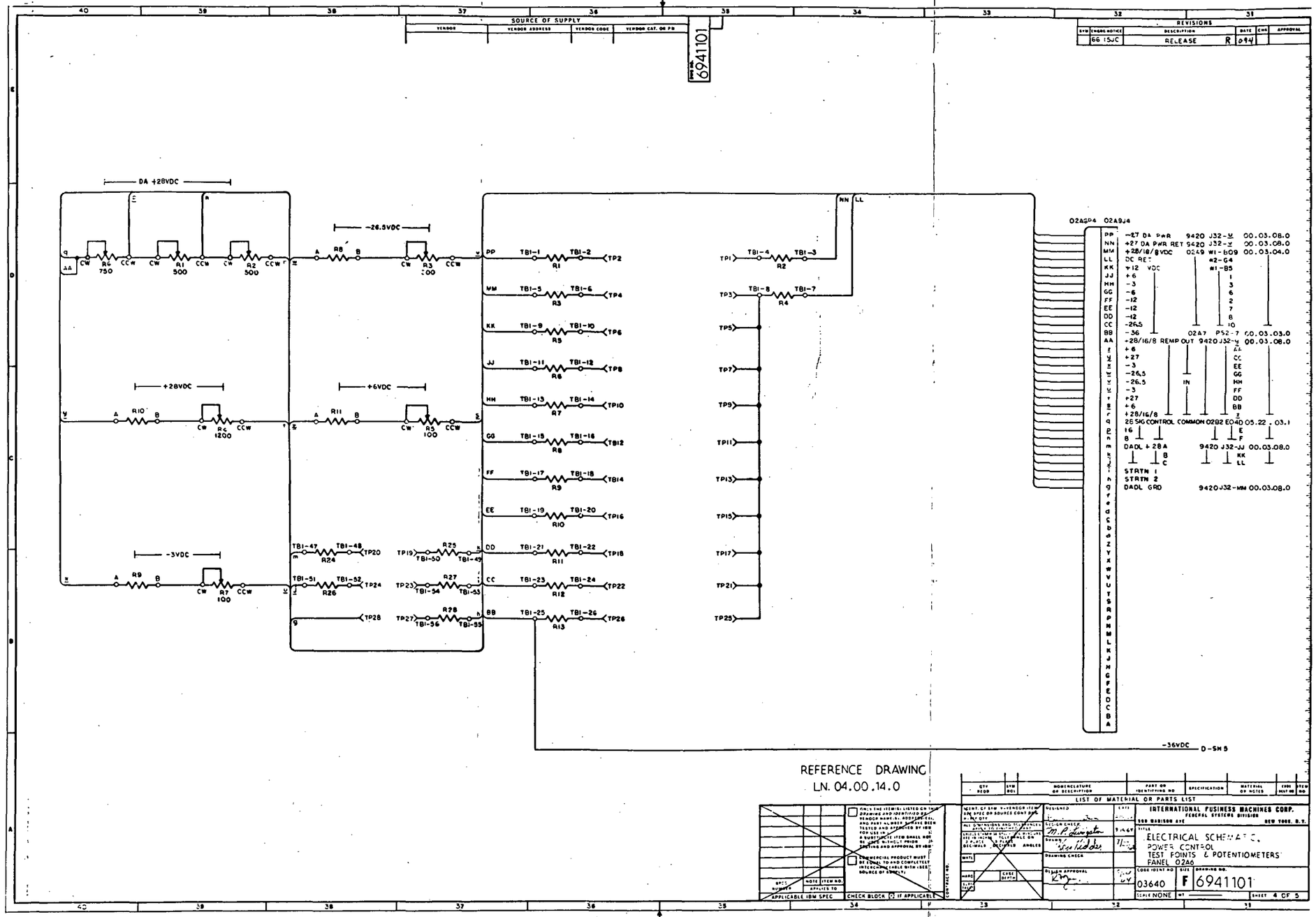


Figure 10-9. Power Control Panel (02A6) Electrical Schematic Diagram (LN 04.00.11.0 through LN 04.00.15.0) (Sheet 4)

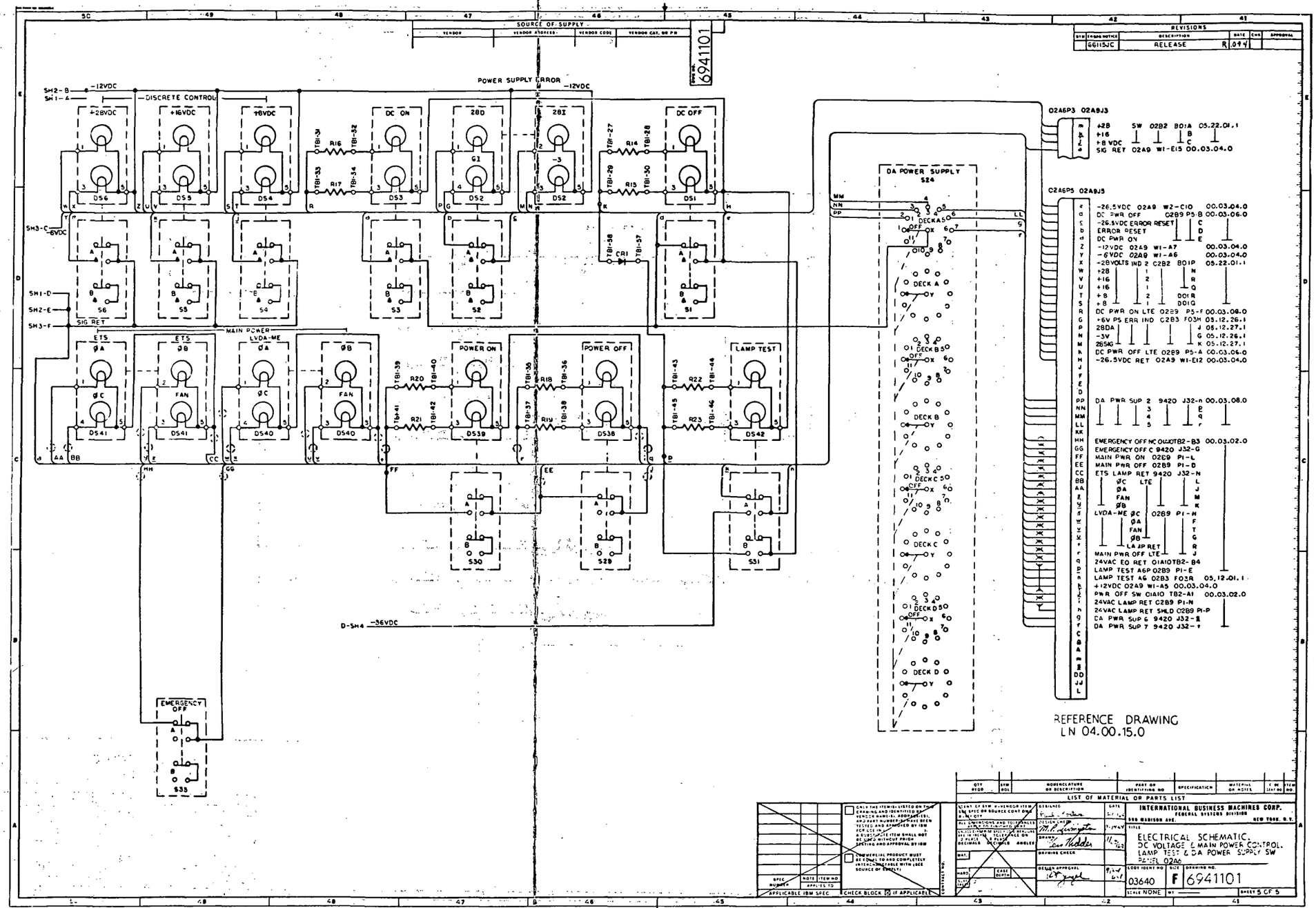


Figure 10-9. Power Control Panel (02A6) Electrical Schematic Diagram (LN 04.00.11.0 through LN 04.00.15.0) (Sheet 5)

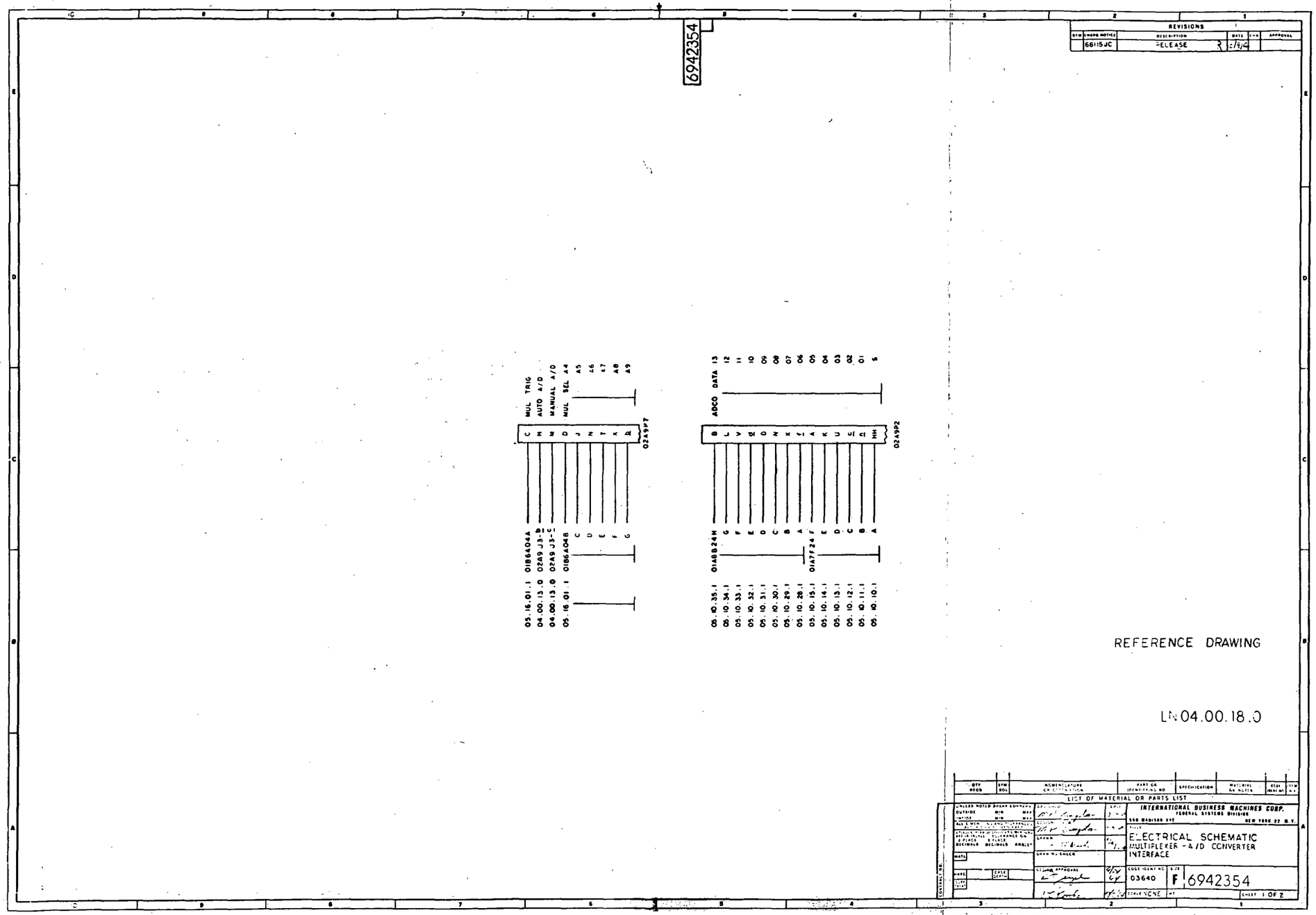


Figure 10-10. Multiplexer - A/D Converter Interface Electrical Schematic Diagram (LN 04. 00. 18. 0 through LN 04. 00. 19. 0) (Sheet 1 of 2)

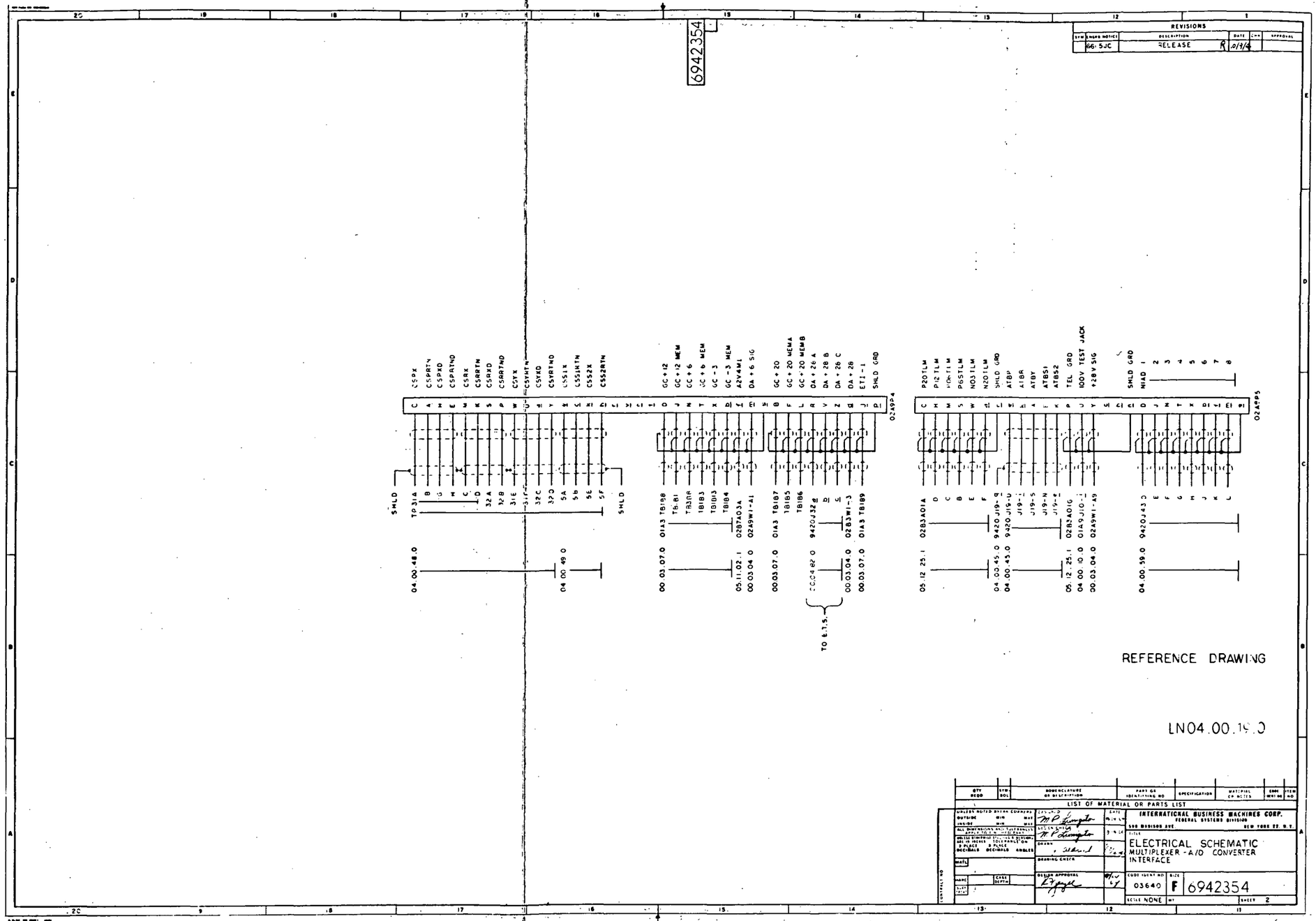


Figure 10-10. Multiplexer - A/D Converter Interface Electrical Schematic Diagram (LN 04. 00. 18. 0 through LN 04. 00. 19. 0) (Sheet 2)

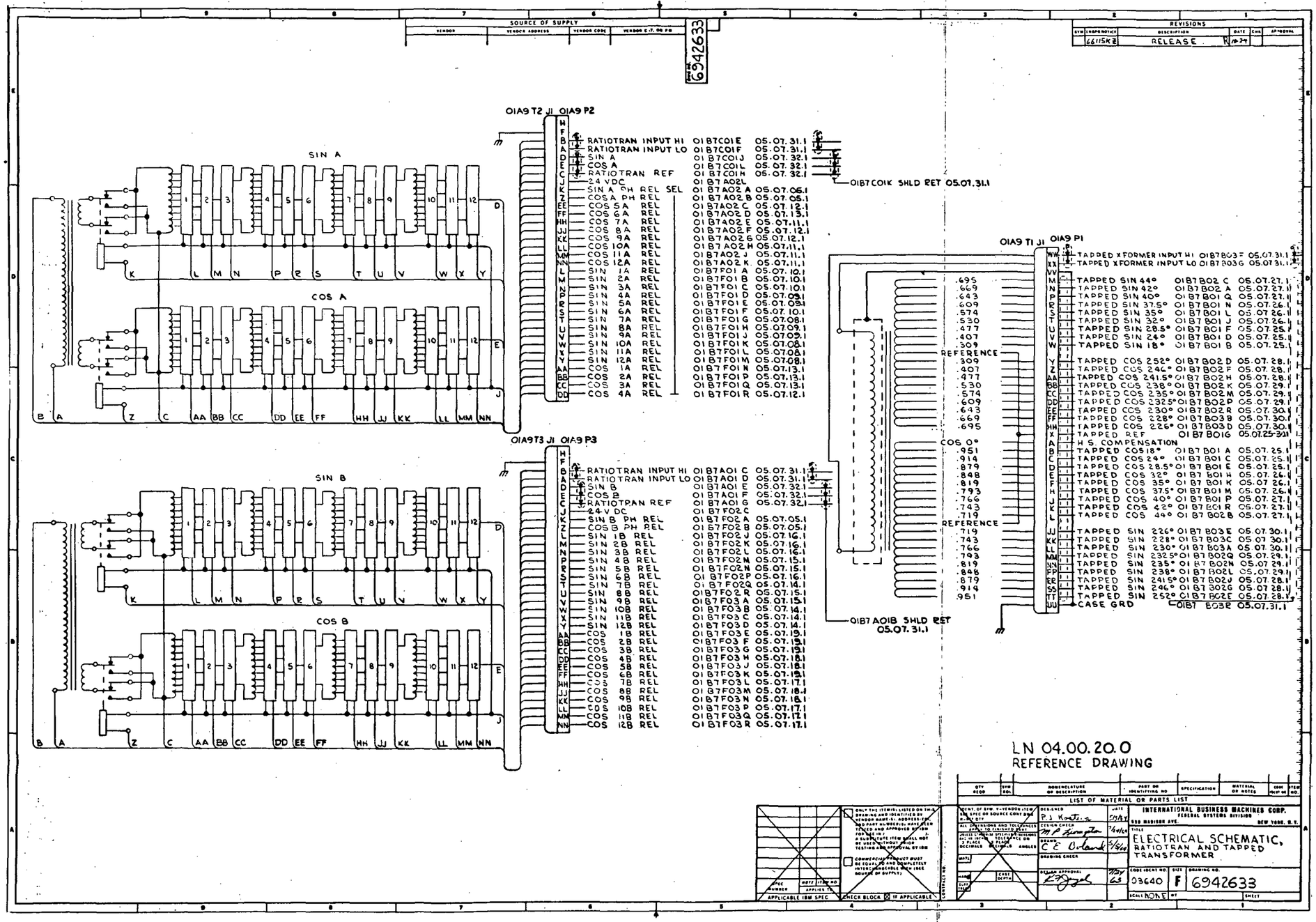


Figure 10-11. Ratiotran and Tapped Transformer Electrical Schematic Diagram (LN 04. 00. 20. 0)

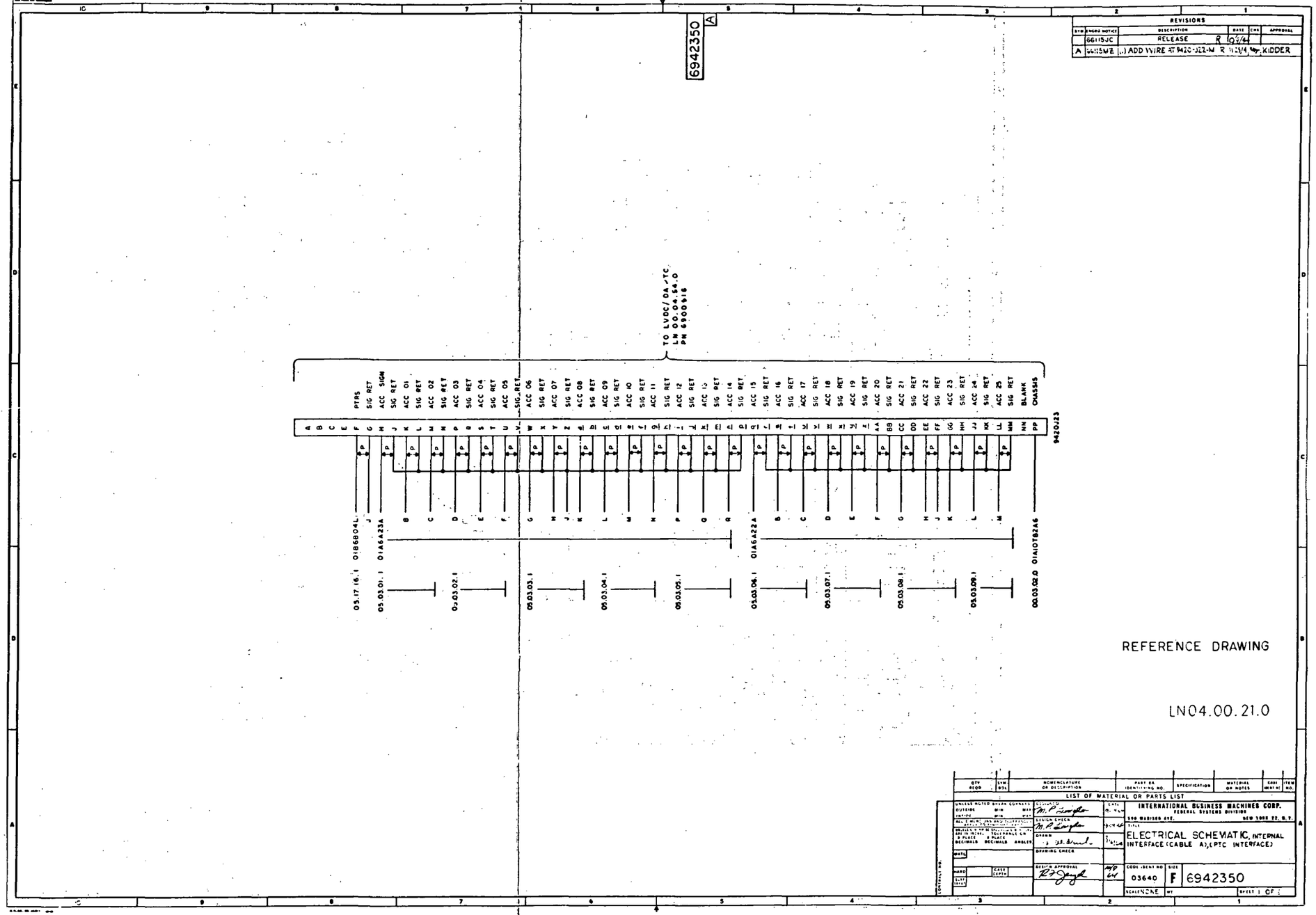


Figure 10-12. A Cable Interface (Connector 9420 J23) Electrical Schematic Diagram LN 04.00.21.0)

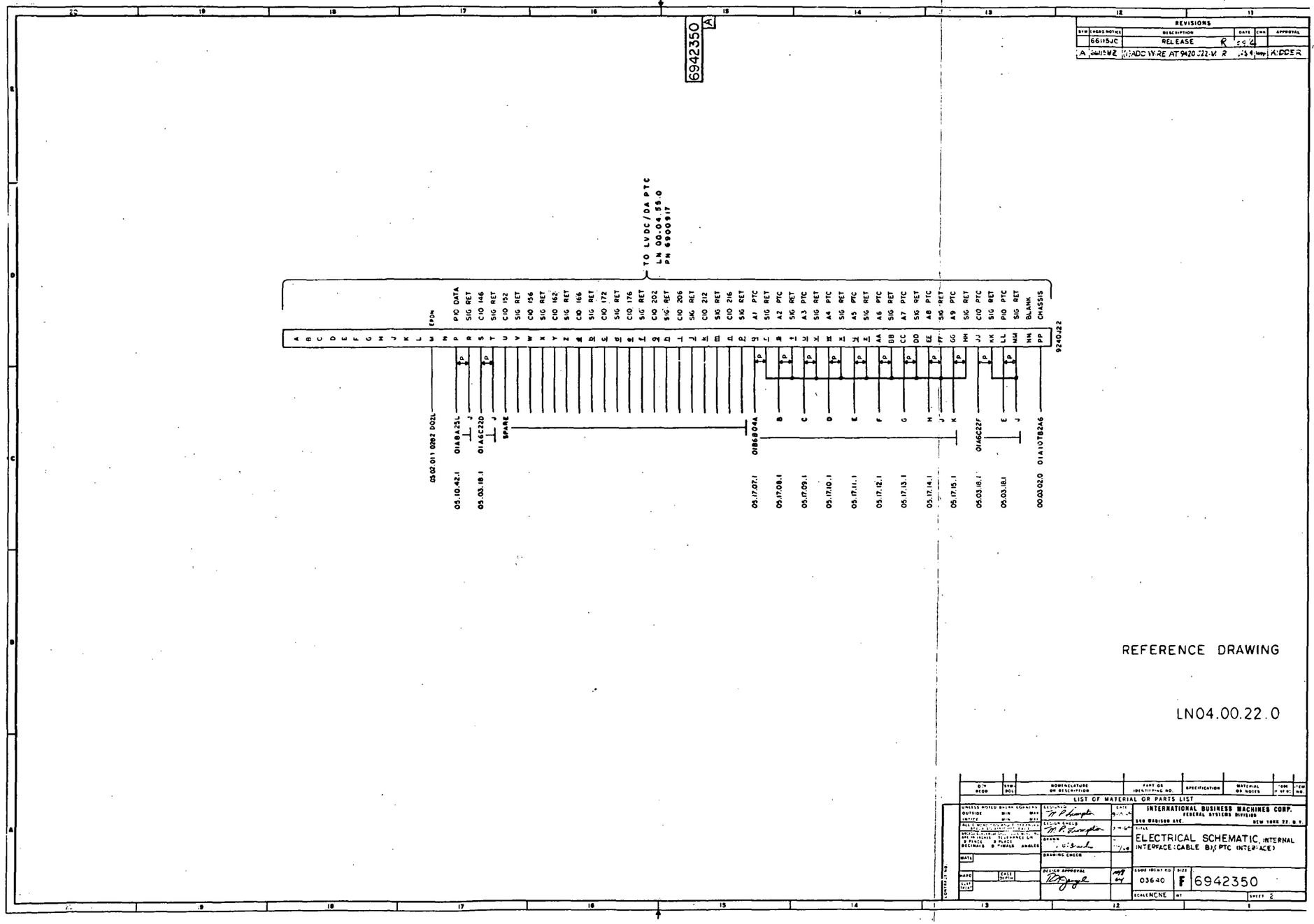


Figure 10-13. B Cable Interface (Connector 9420 J22) Electrical Schematic Diagram (LN 04.00.22.0)

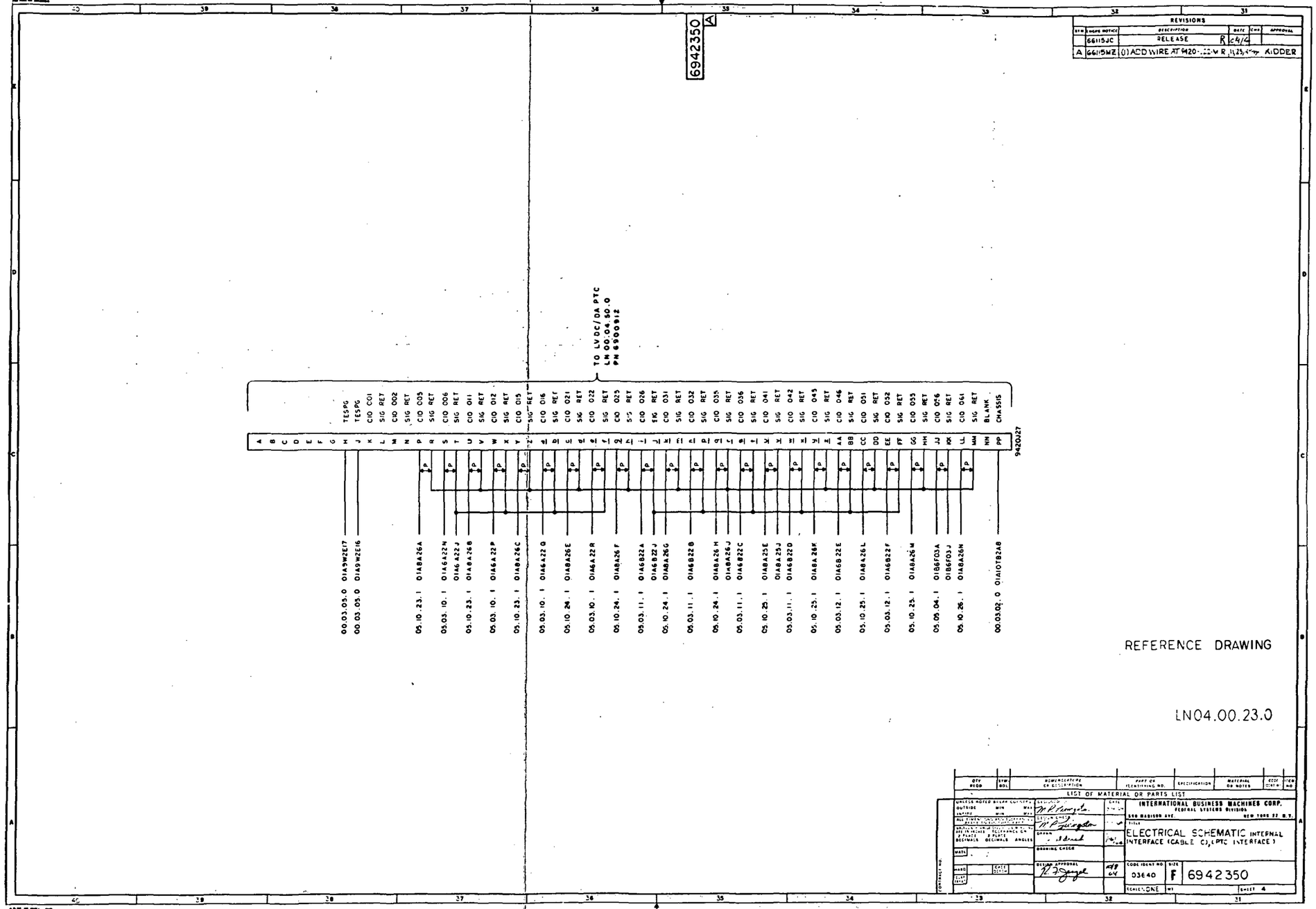


Figure 10-14. C Cable Interface (Connector 9420 J27) Electrical Schematic Diagram (LN 04. 00. 23. 0)

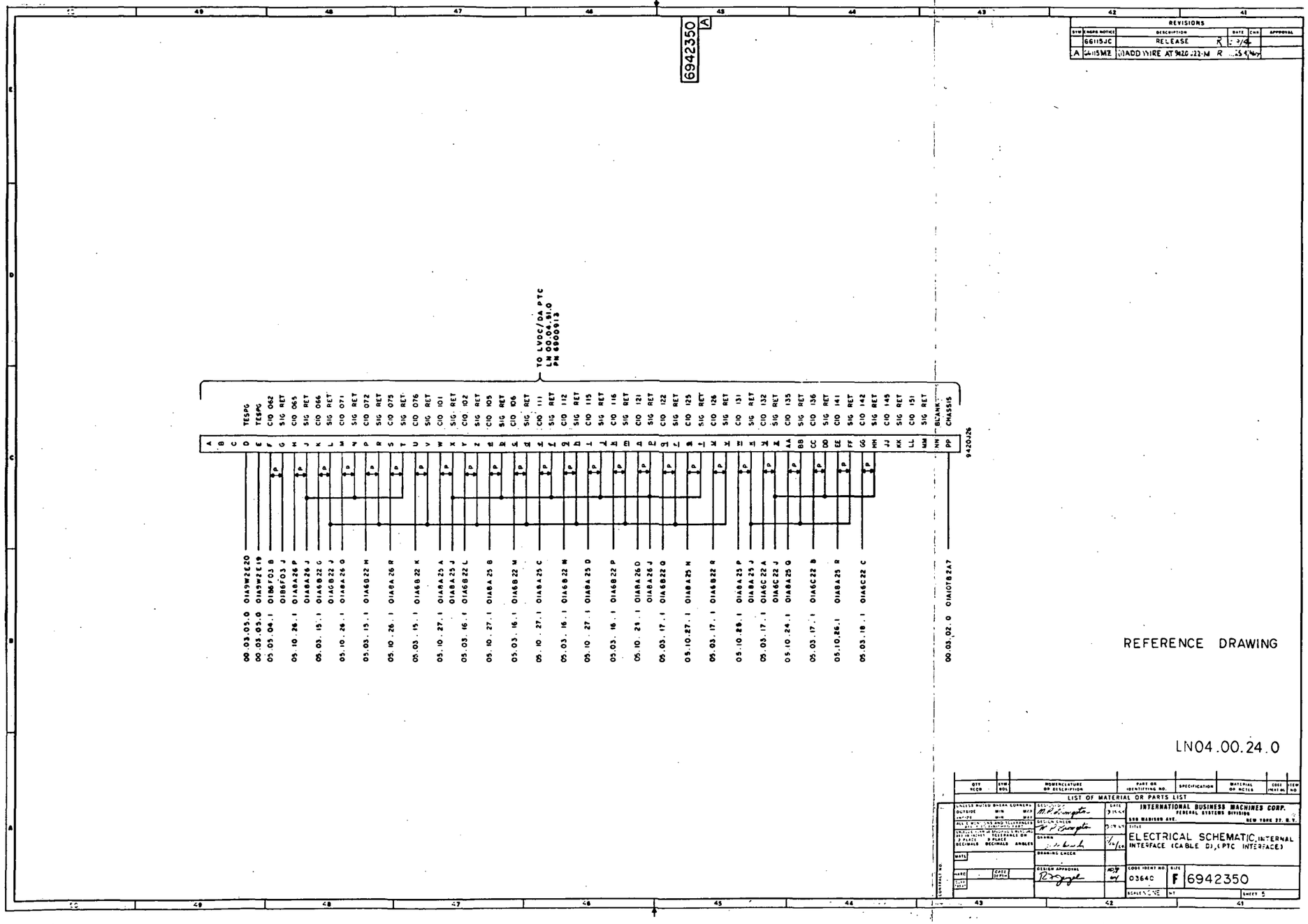


Figure 10-15. D Cable Interface (Connector 9420 J26) Electrical Schematic Diagram (LN 04. 00. 24. 0)

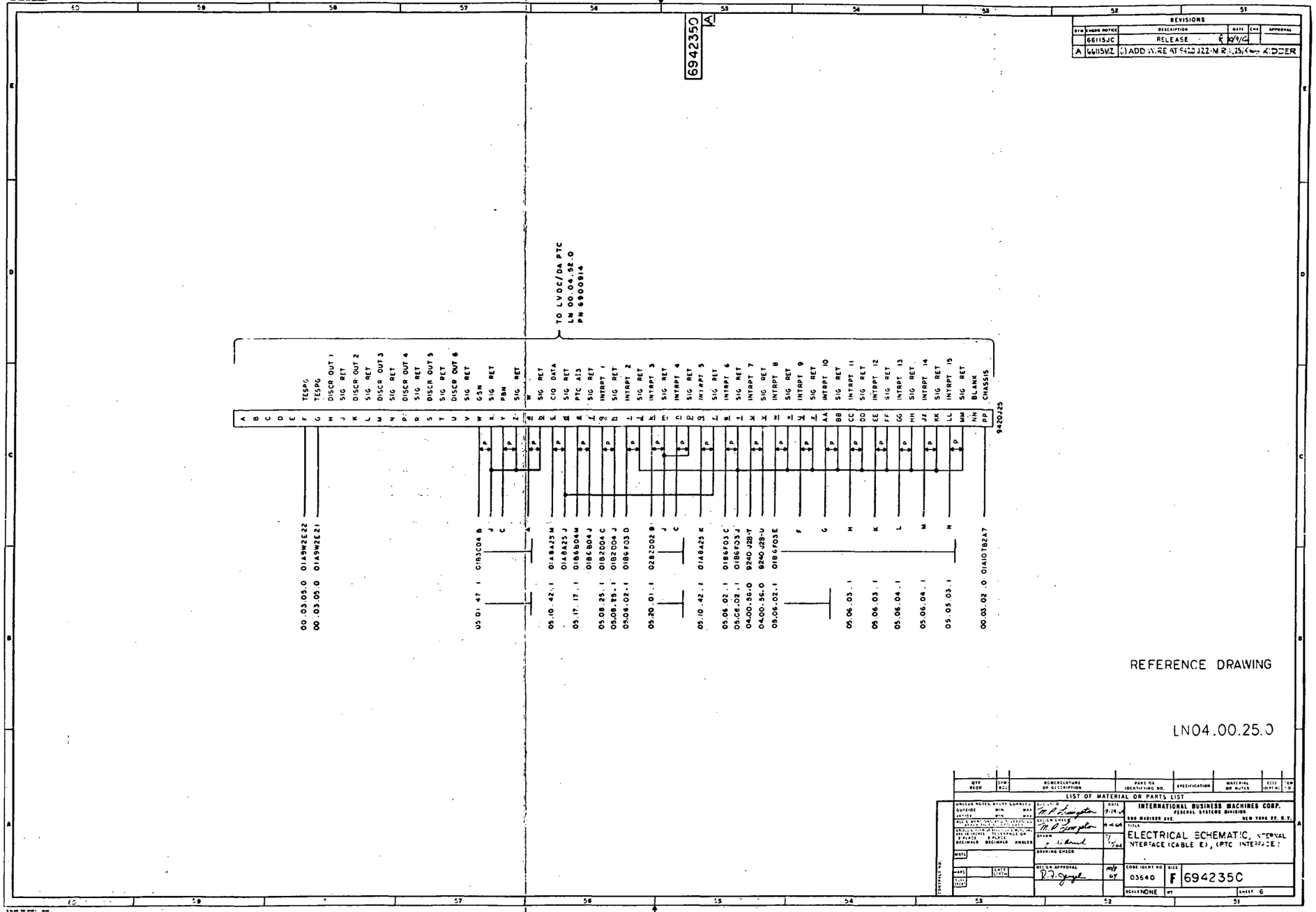


Figure 10-16. E Cable Interface (Connector 9420 J25) Electrical Schematic Diagram (LN 04. 00. 25. 0)

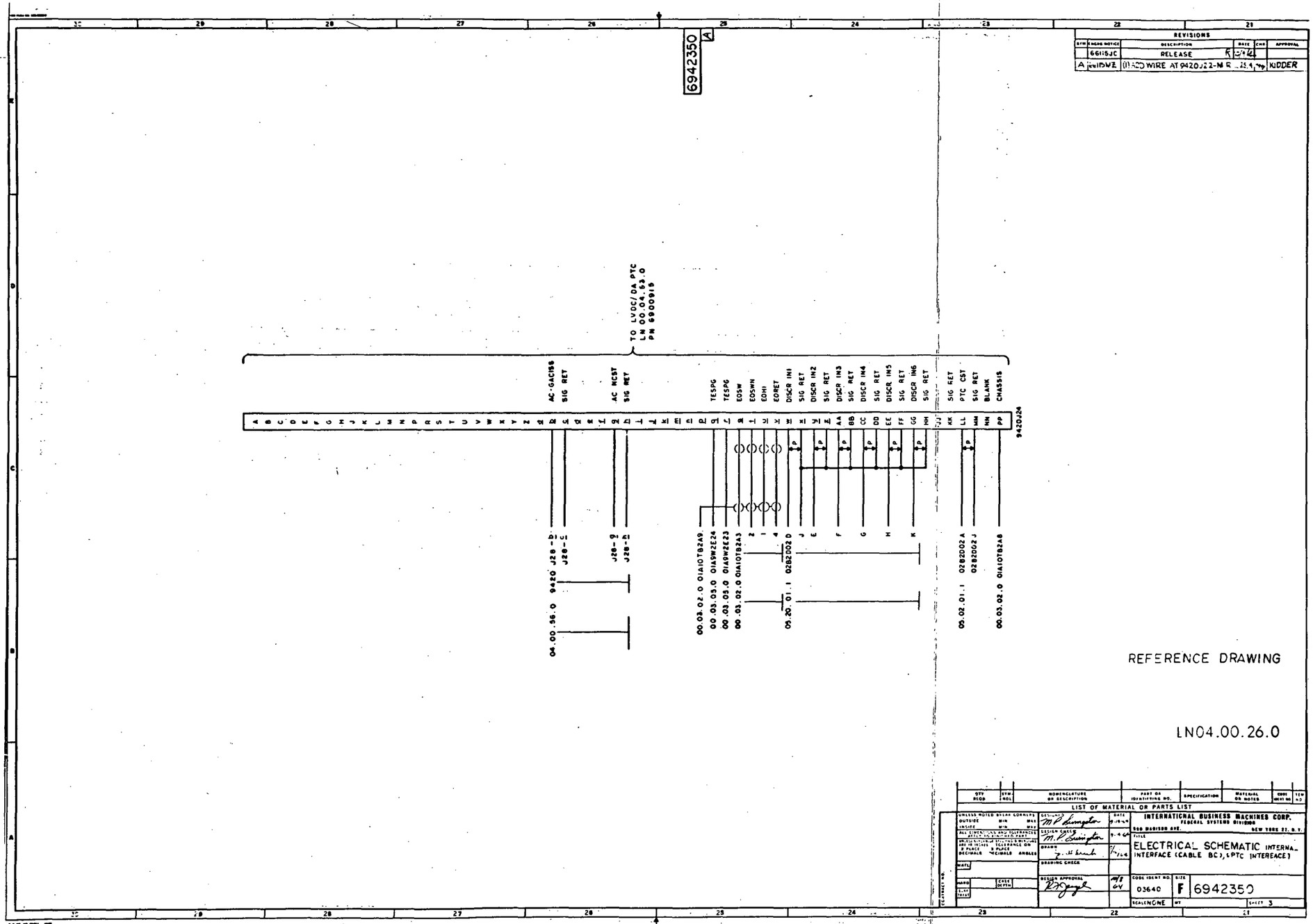


Figure 10-17. BC Cable Interface (Connector 9420 J24) Electrical Schematic Diagram (LN 04.00.26.0)

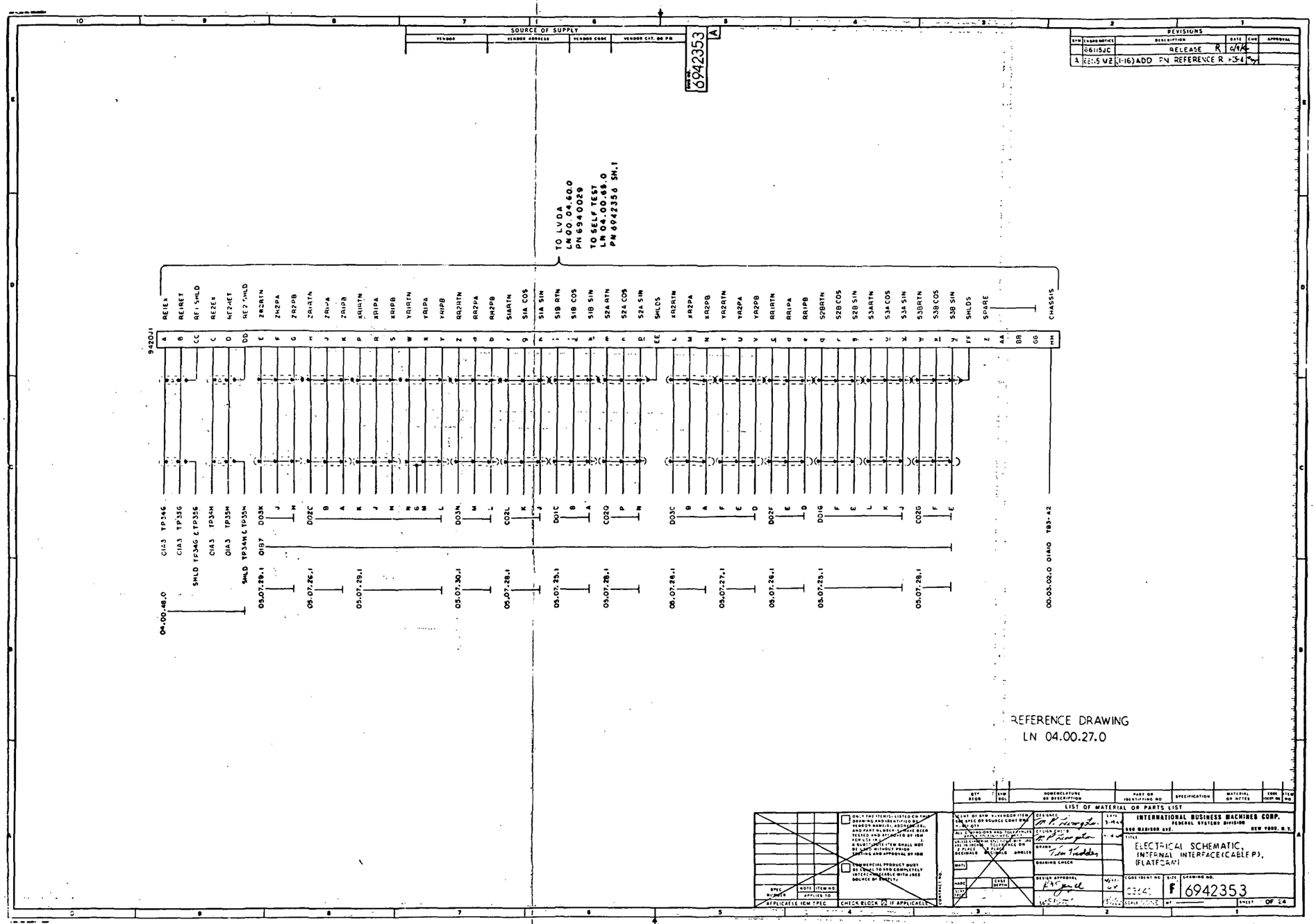


Figure 10-18. P Cable Interface (Connector 9420 J1) Electrical Schematic Diagram (LN 04.00.27.0)

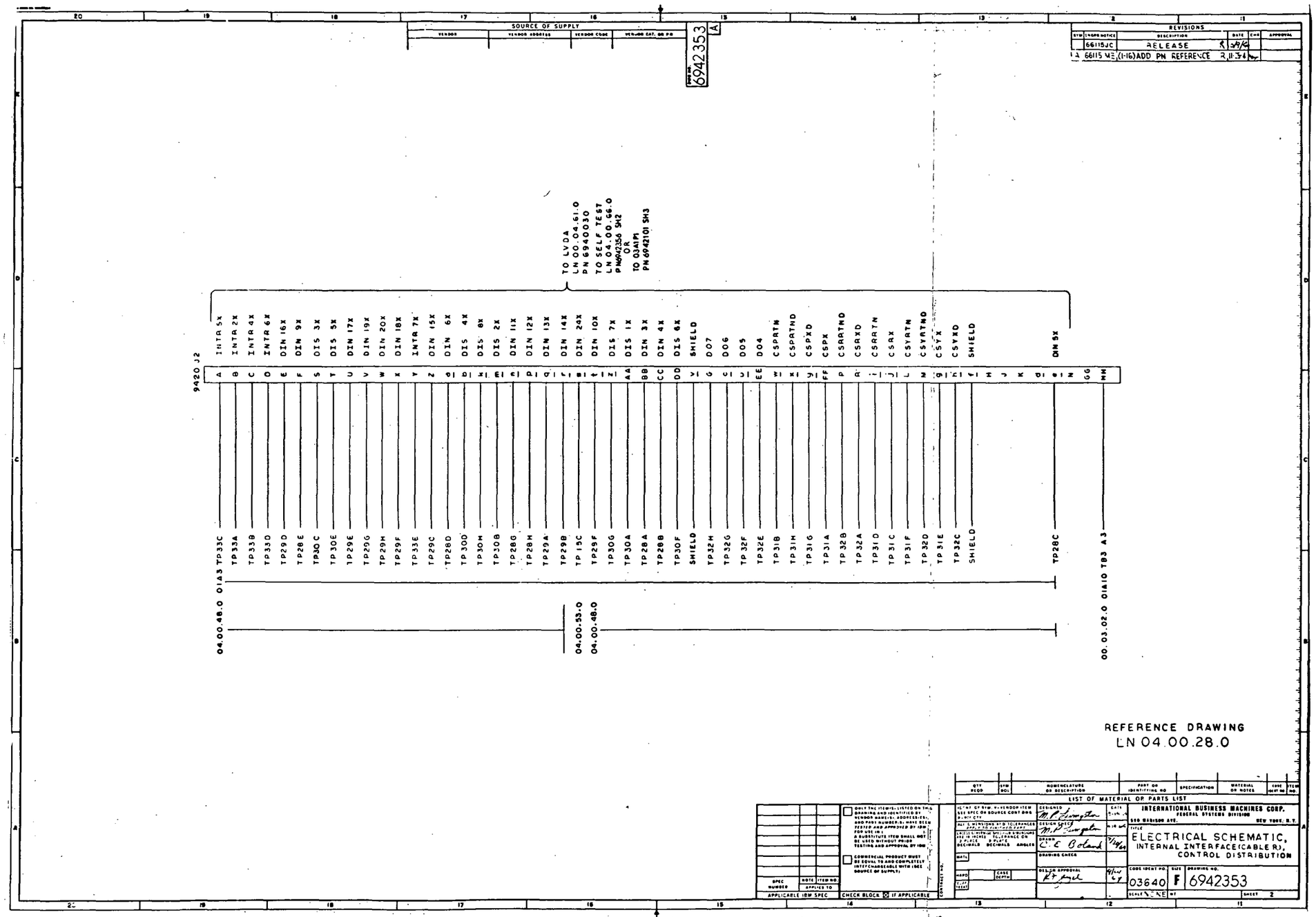


Figure 10-19. R Cable Interface (Connector 9420 J2) Electrical Schematic Diagram (LN 04.00.28.0)

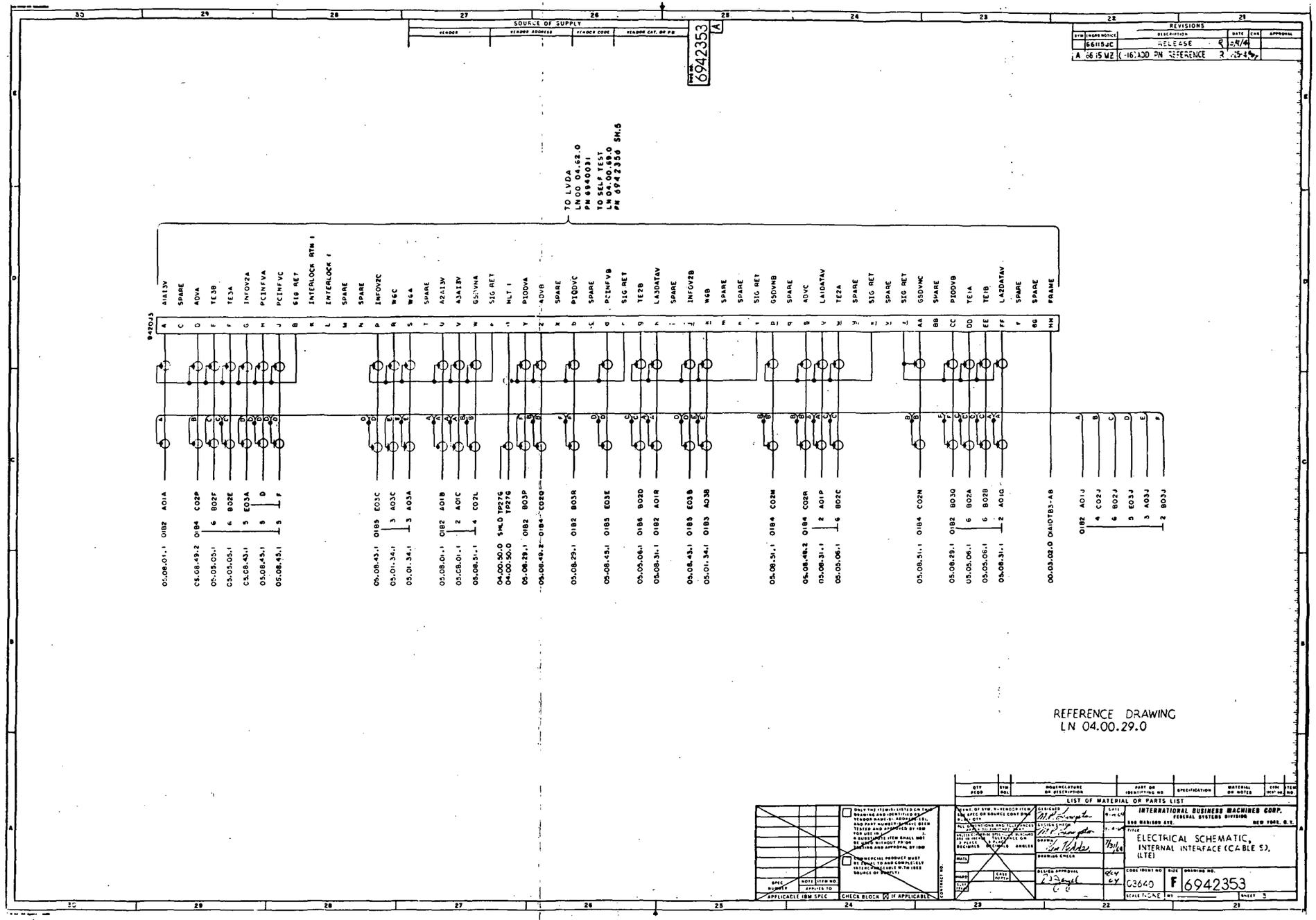


Figure 10-20. S Cable Interface (Connector 9420 J3) Electrical Schematic Diagram (LN 04.00.29.0)

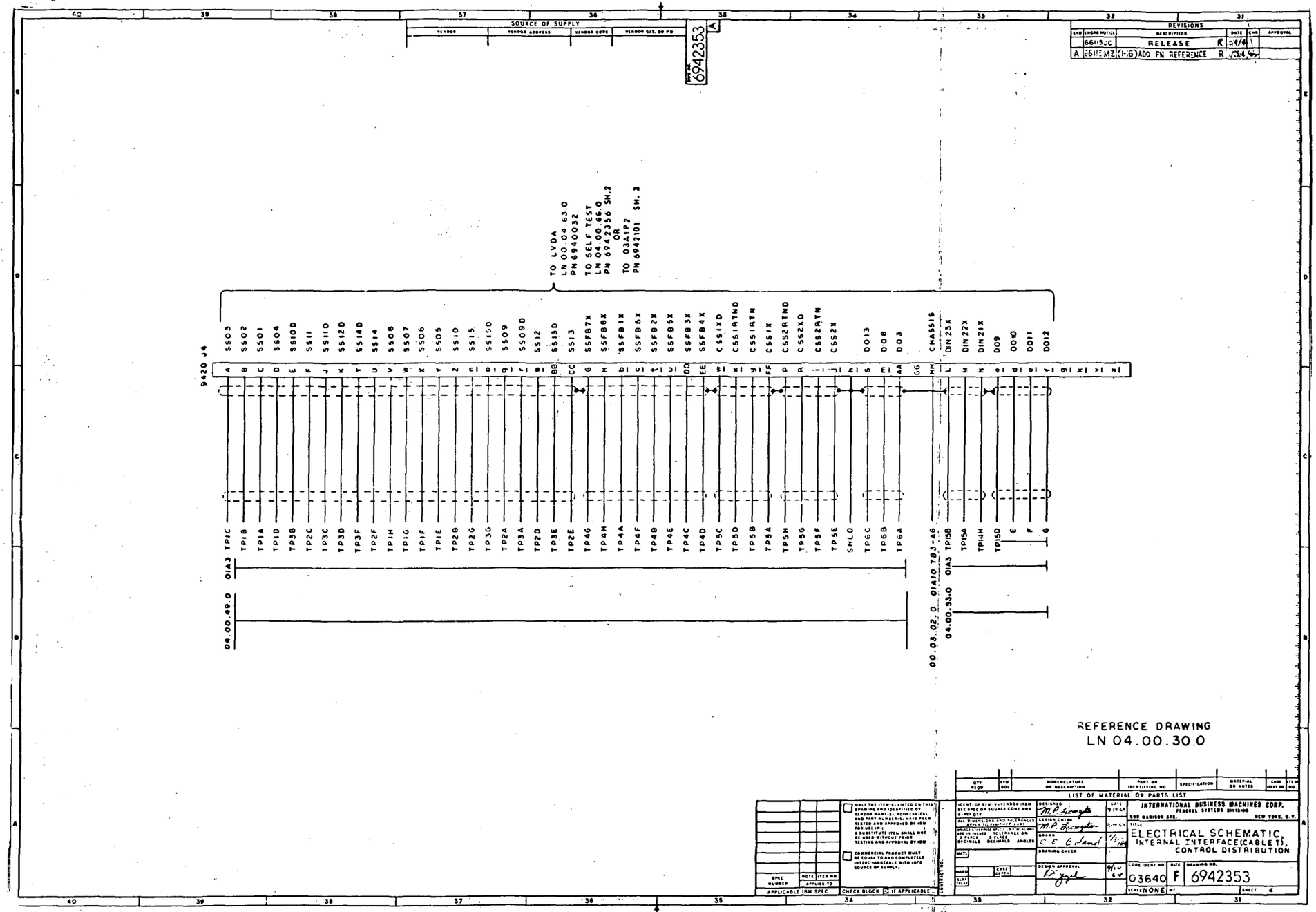


Figure 10-21. T Cable Interface (Connector 9420 J4) Electrical Schematic Diagram (LN 04. 00. 30. 0)

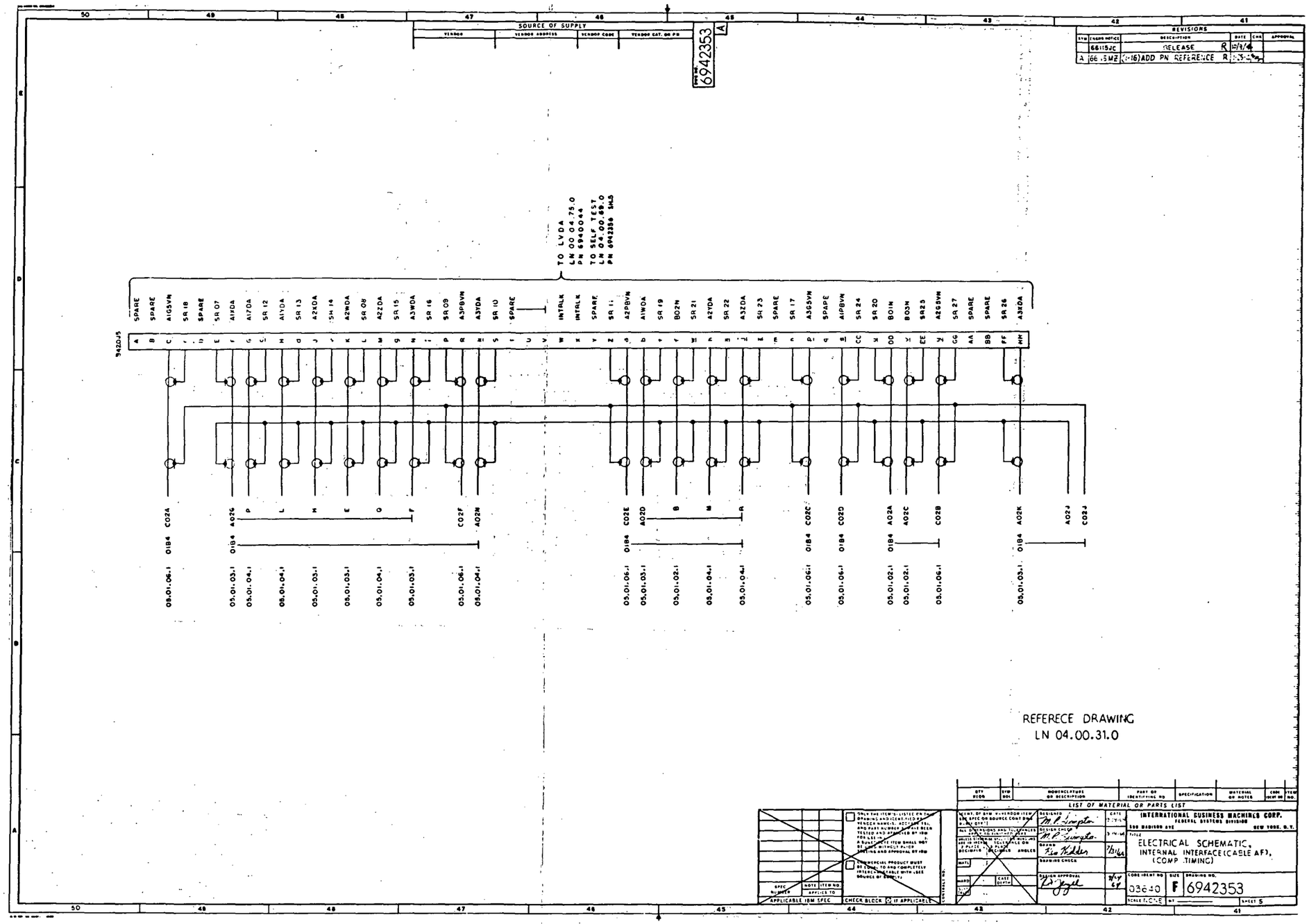


Figure 10-22. AF Cable Interface (Connector 9420 J5) Electrical Schematic Diagram (LN 04. 00. 31. 0)

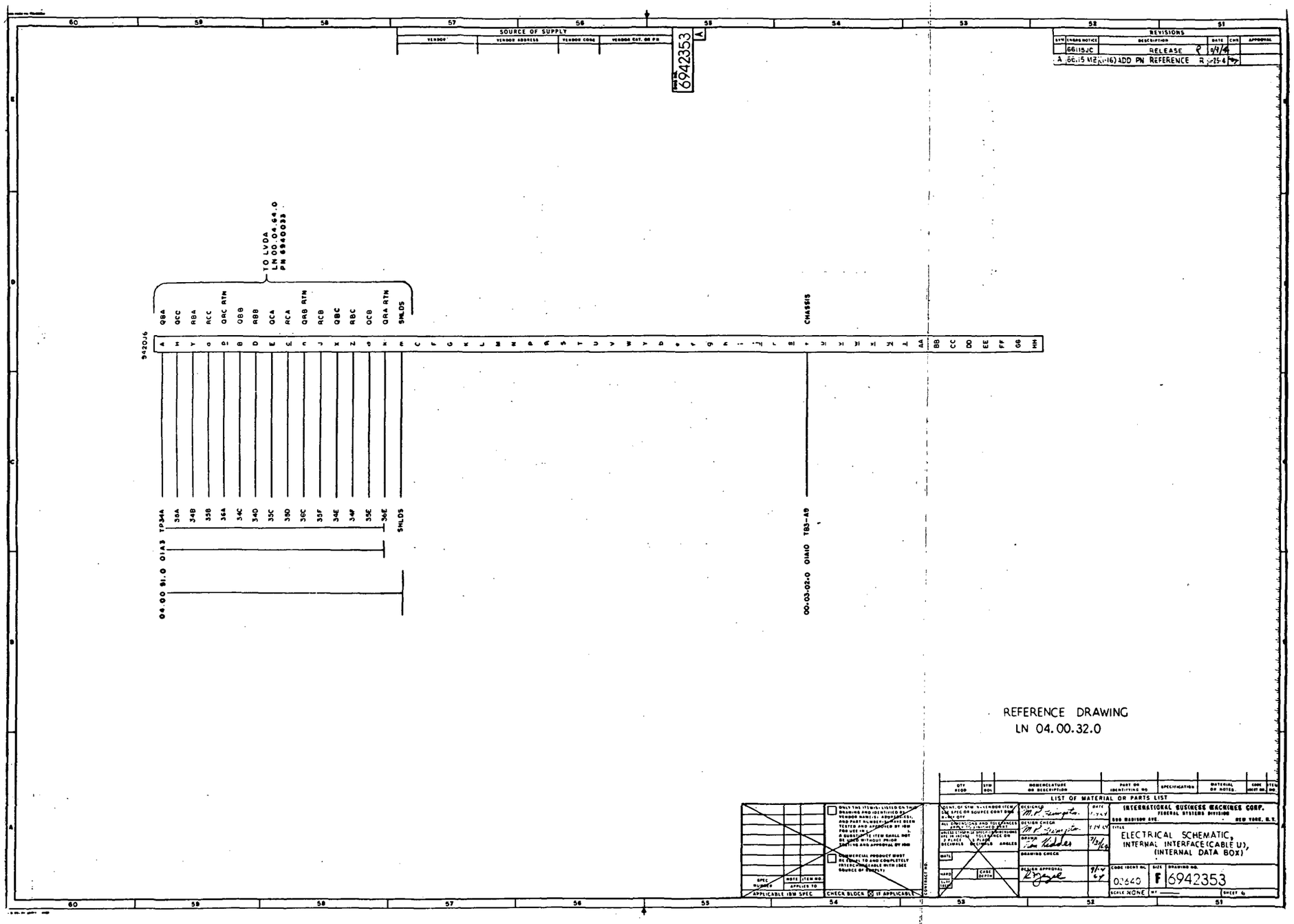


Figure 10-23. U Cable Interface (Connector 9420 J6) Electrical Schematic Diagram (LN 04.00.32.0)

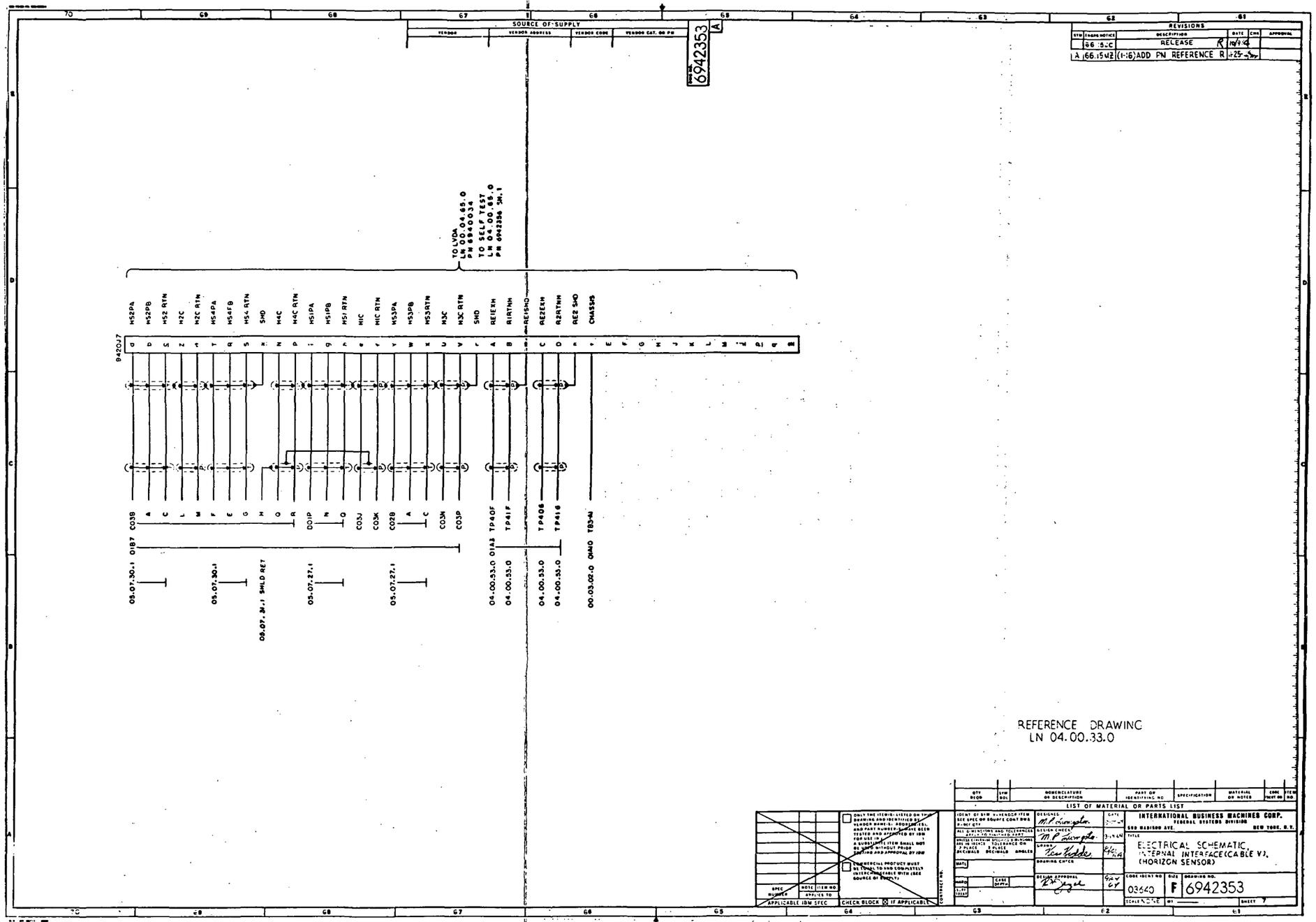


Figure 10-24. V Cable Interface (Connector 9420 J7) Electrical Schematic Diagram (LN 04. 00. 33. 0)

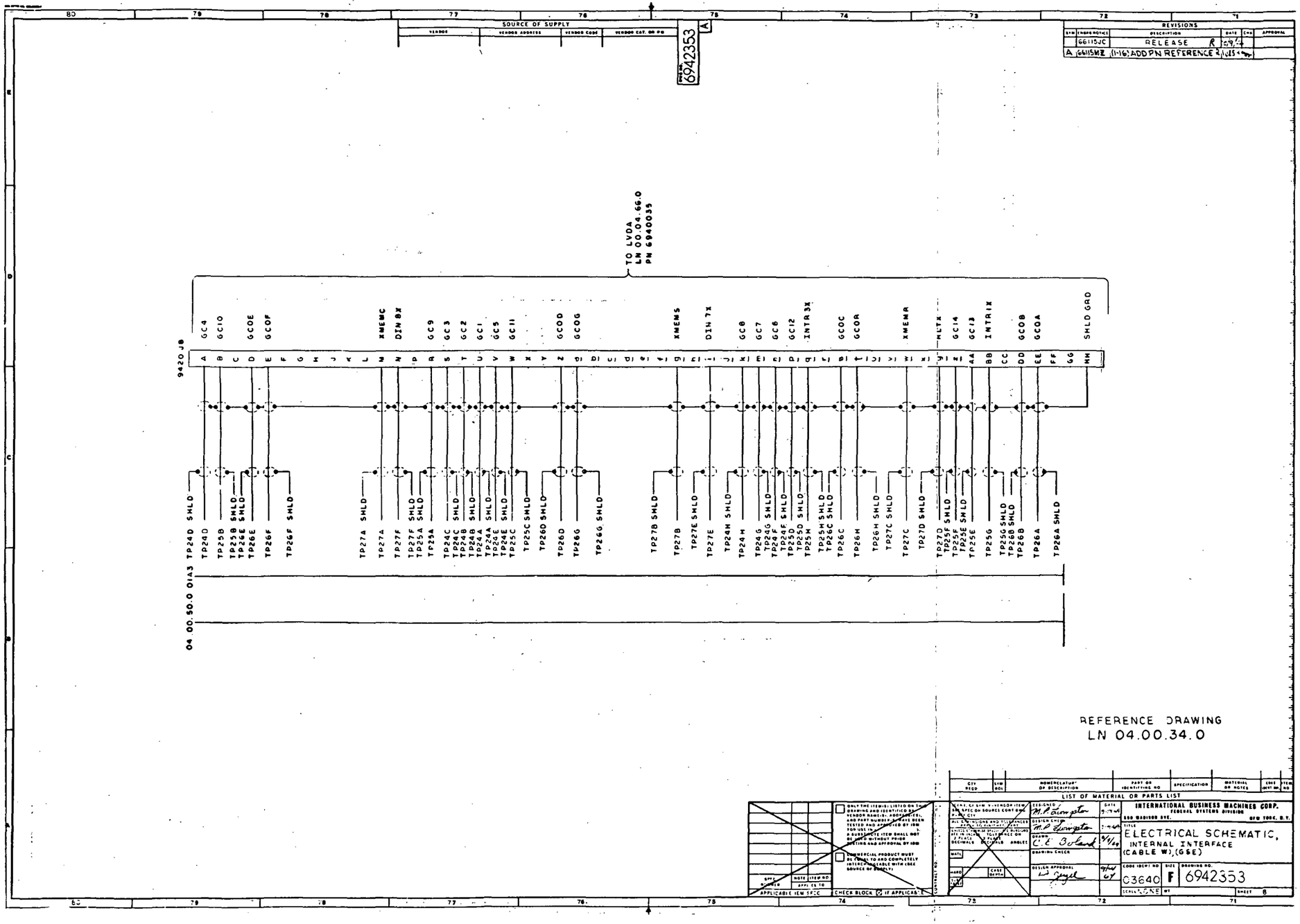


Figure 10-25. W Cable Interface (Connector 9420 J8) Electrical Schematic Diagram (LN 04.00.34.0)

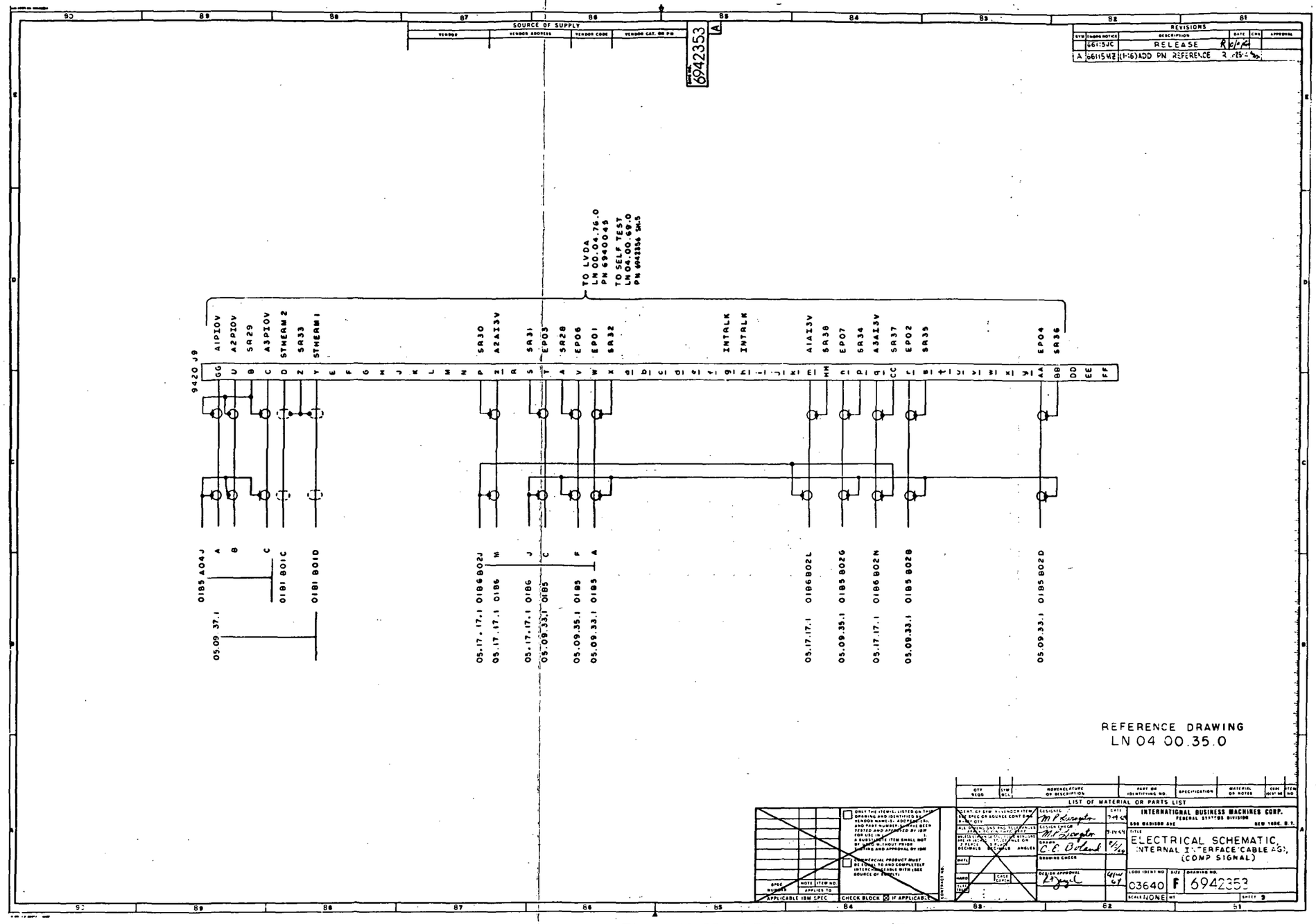


Figure 10-26. AG Cable Interface (Connector 9420 J9) Electrical Schematic Diagram (LN 04.00.35.0)

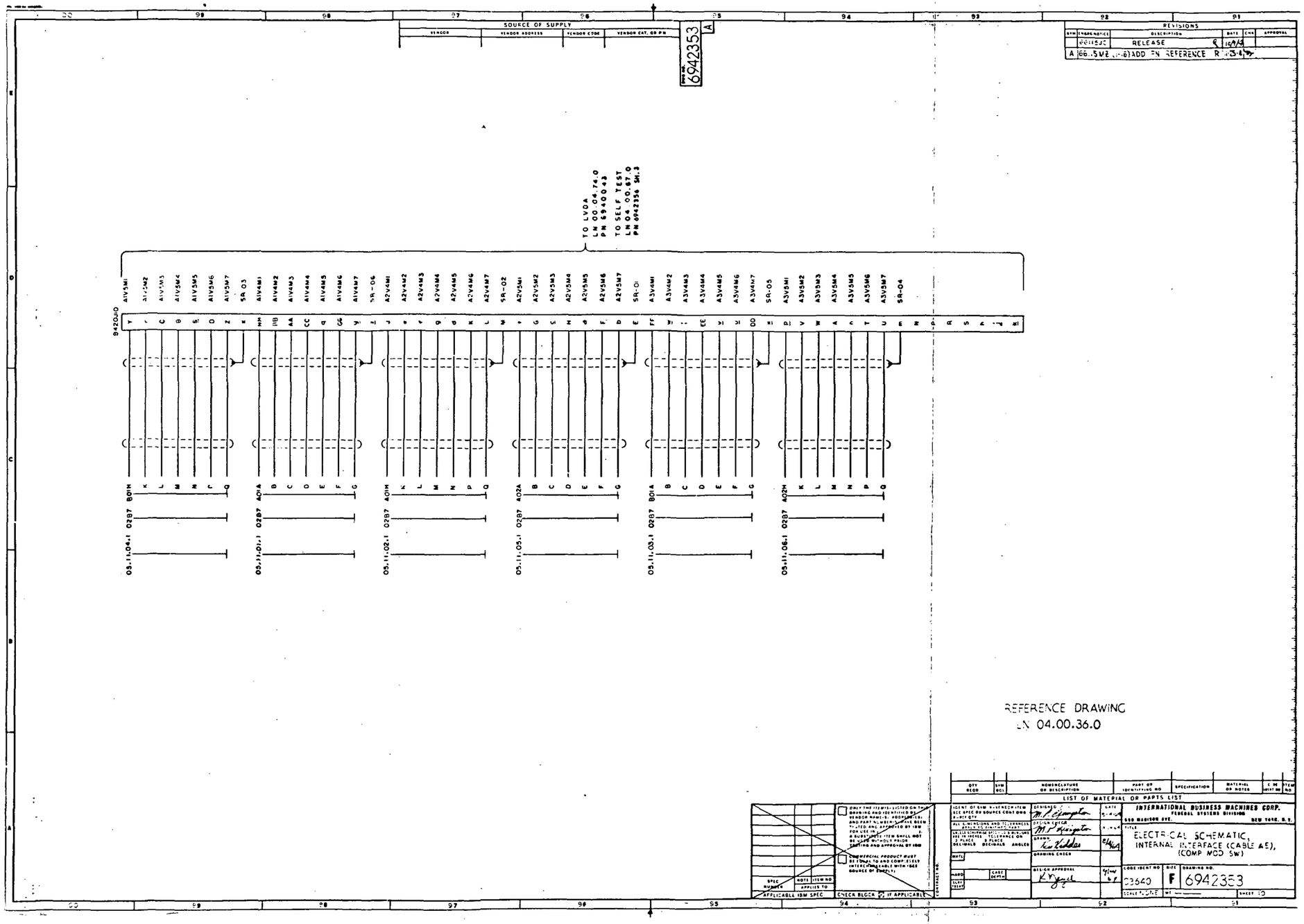


Figure 10-27. AE Cable Interface (Connector 9420 J10) Electrical Schematic Diagram (LN 04.00.36.0)

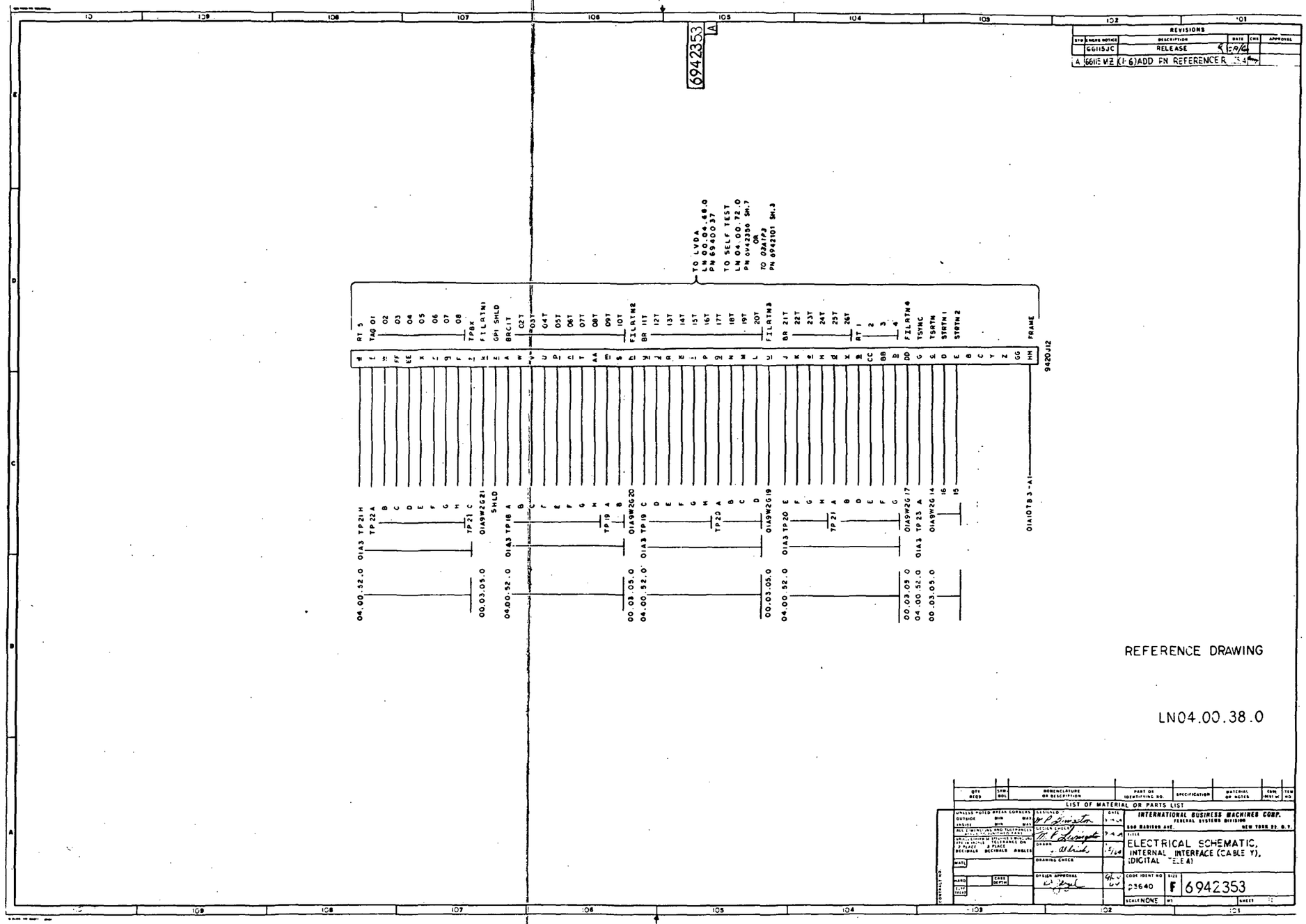


Figure 10-28. Y Cable Interface (Connector 9420 J12) Electrical Schematic Diagram (LN 04. 00. 38. 0)

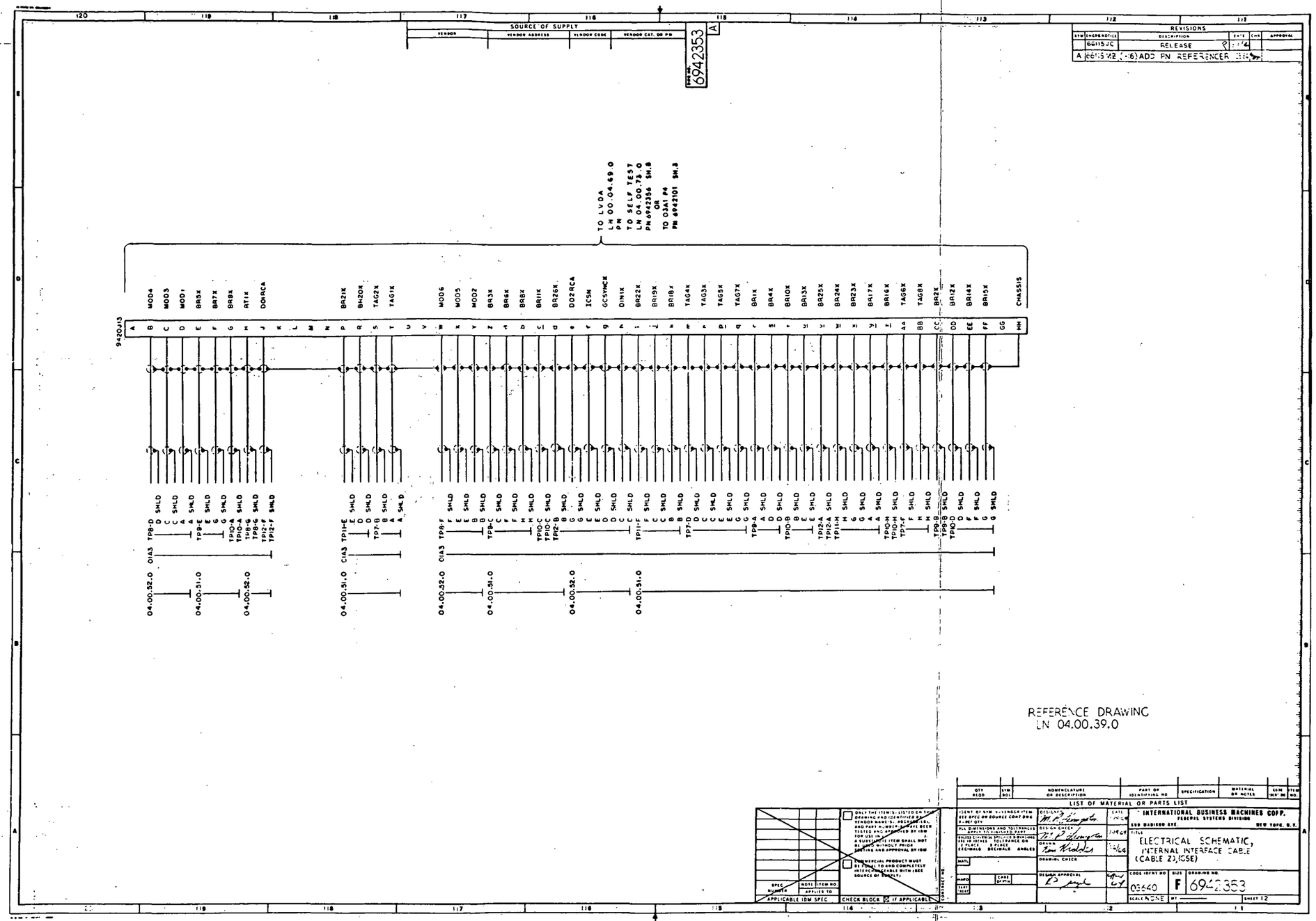


Figure 10-29. Z Cable Interface (Connector 9420 J13) Electrical Schematic Diagram (LN 04.00.39.0)

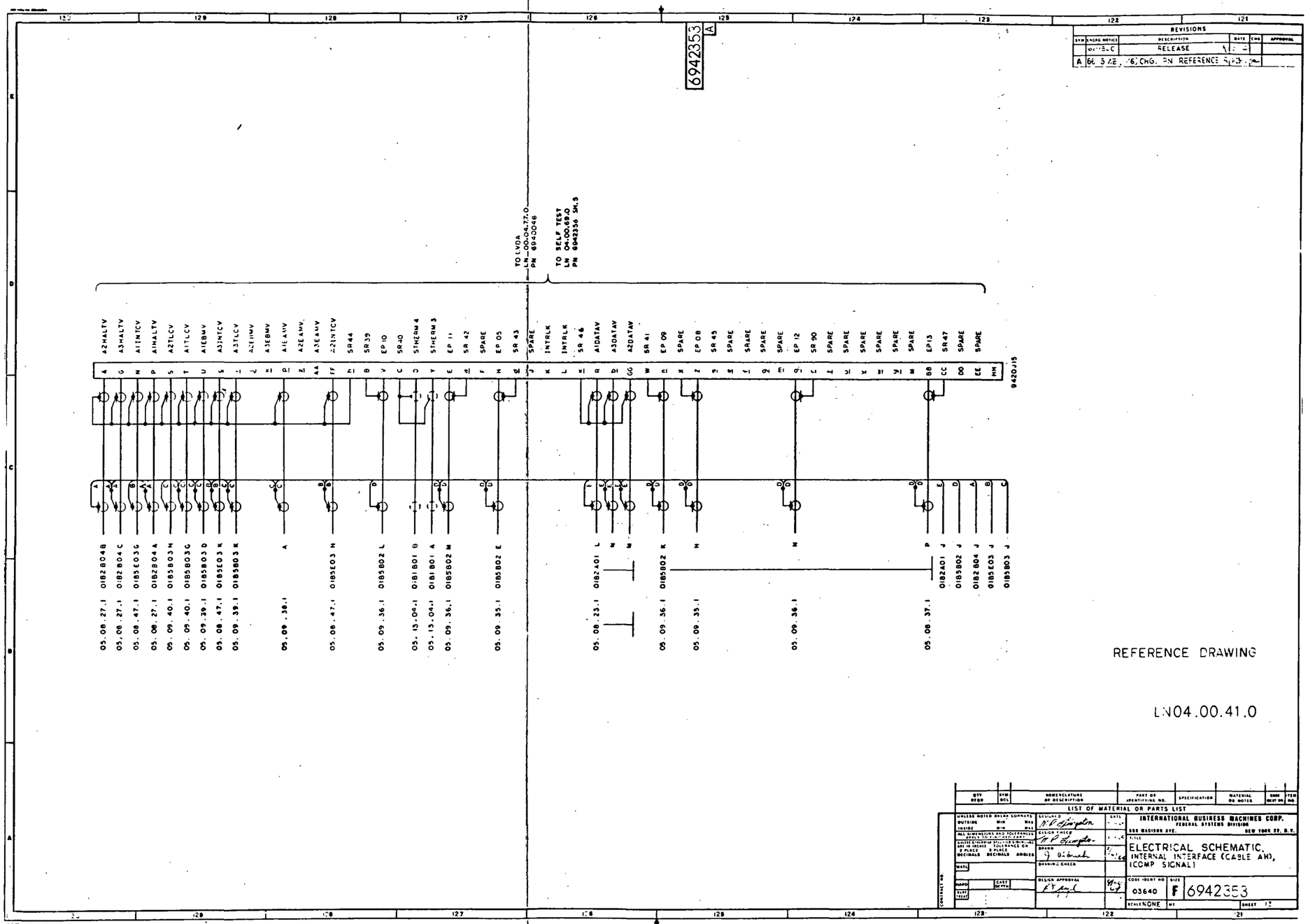


Figure 10-30. AH Cable Interface (Connector 9420 J15) Electrical Schematic Diagram (LN 04.00.41.0)

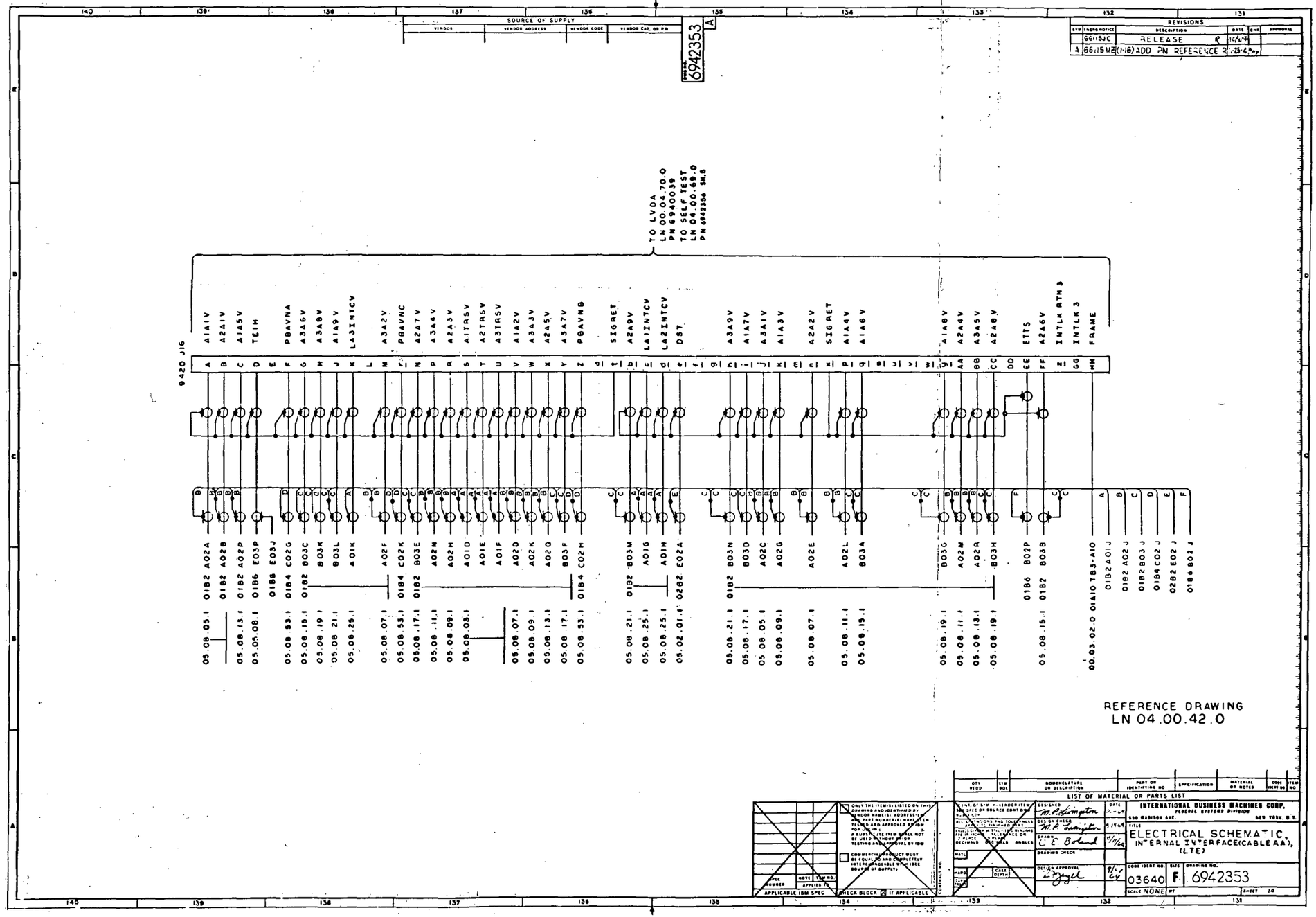


Figure 10-31. AA Cable Interface (Connector 9420 J16) Electrical Schematic Diagram (LN 04.00.42.0)

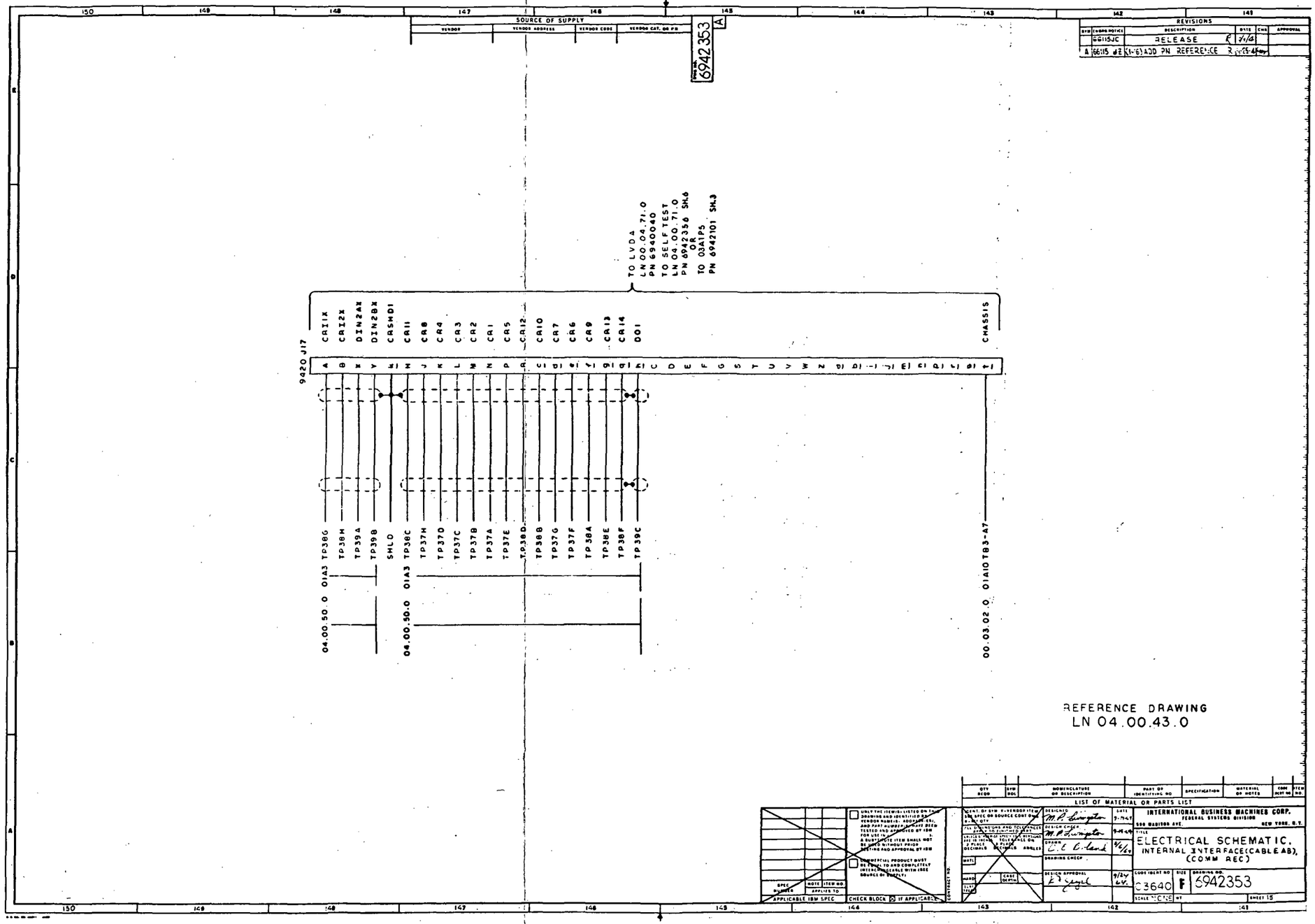


Figure 10-32. AB Cable Interface (Connector 9420 J17) Electrical Schematic Diagram (LN 04.00.43.0)

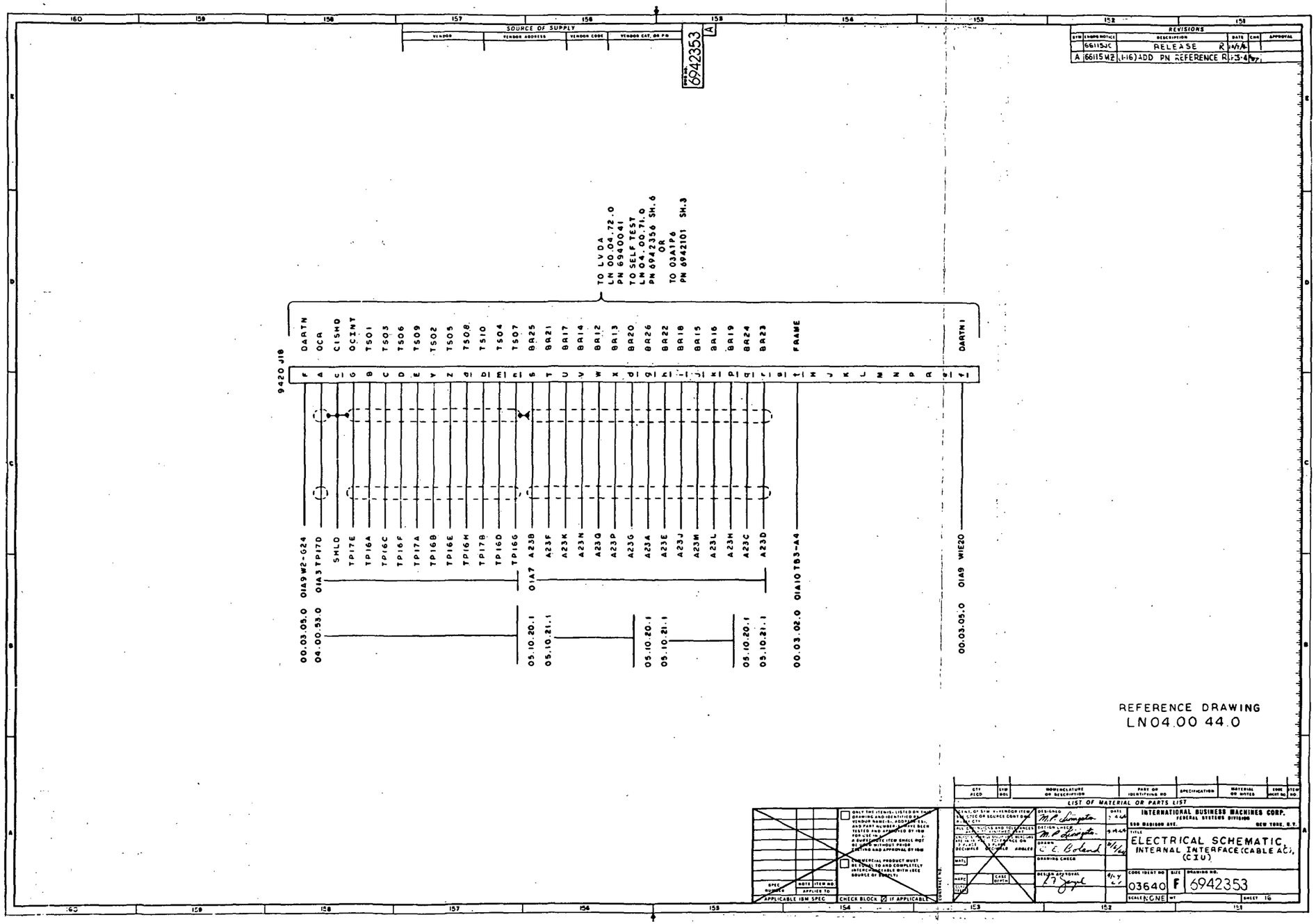


Figure 10-33. AC Cable Interface (Connector 9420 J18) Electrical Schematic Diagram (LN 04.00.44.0)

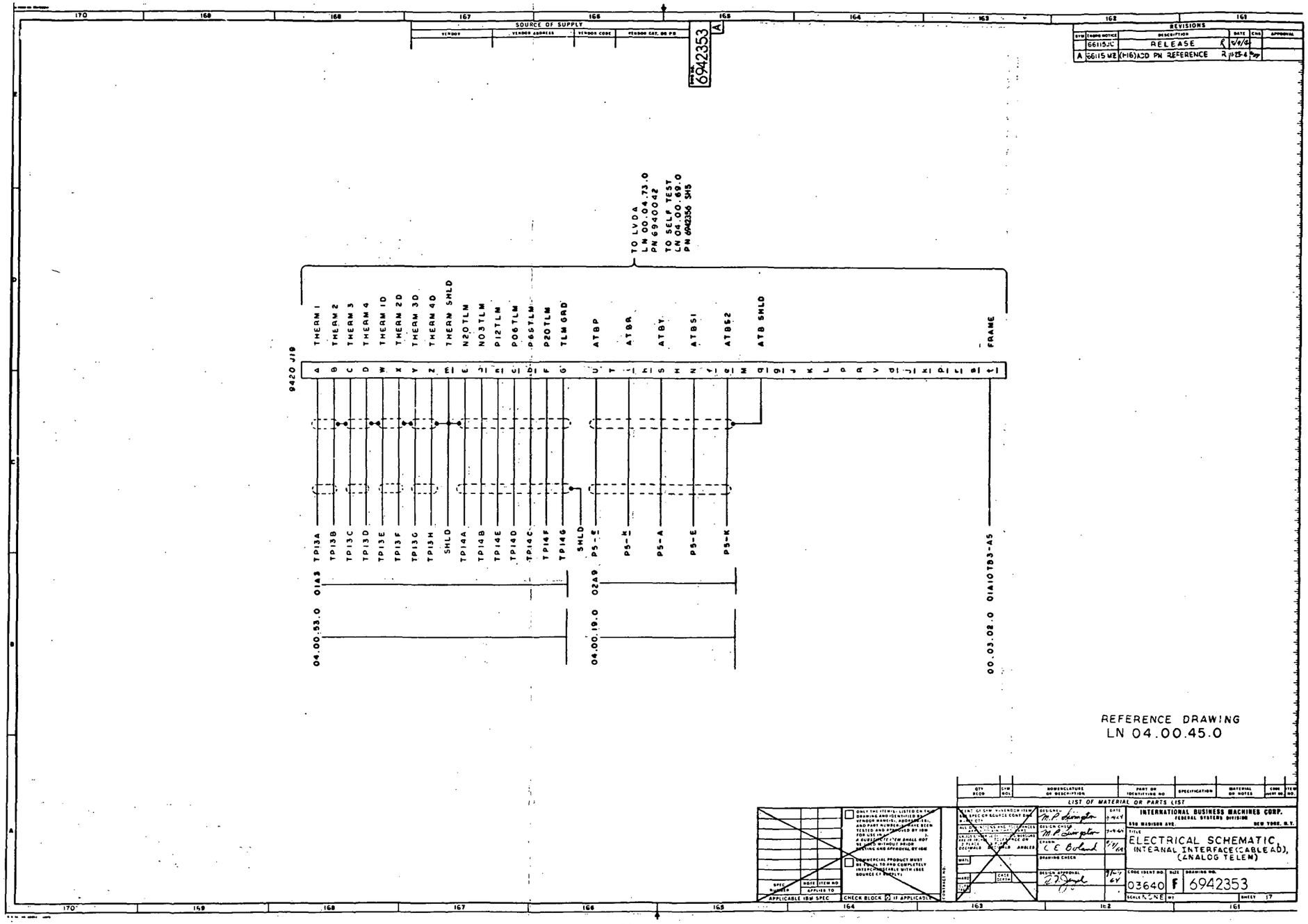


Figure 10-34. AD Cable Interface (Connector 9420 J19) Electrical Schematic Diagram (LN 04.00.45.0)

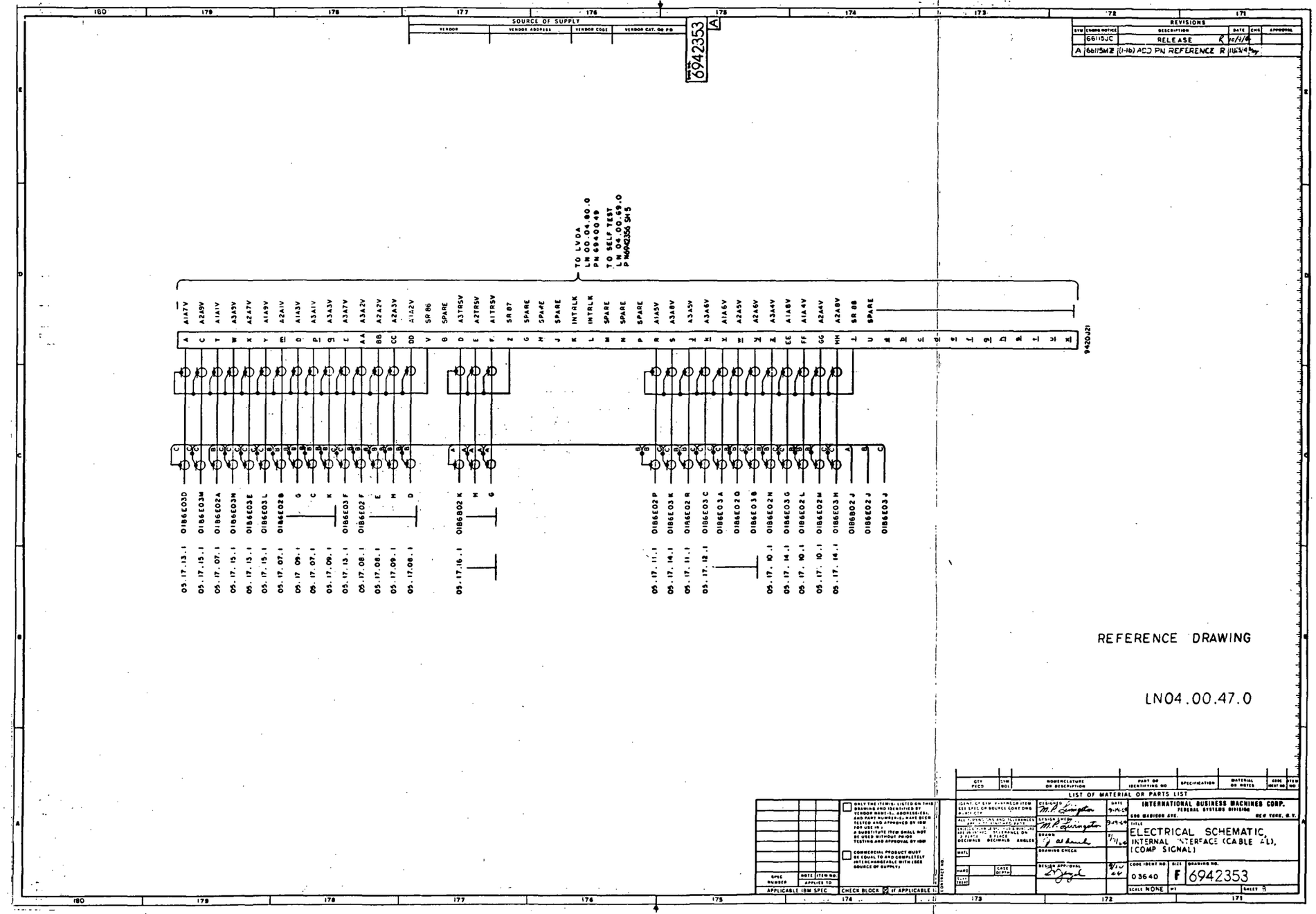


Figure 10-35. AL Cable Interface (Connector 9420 J21) Electrical Schematic Diagram (LN 04. 00. 47. 0)

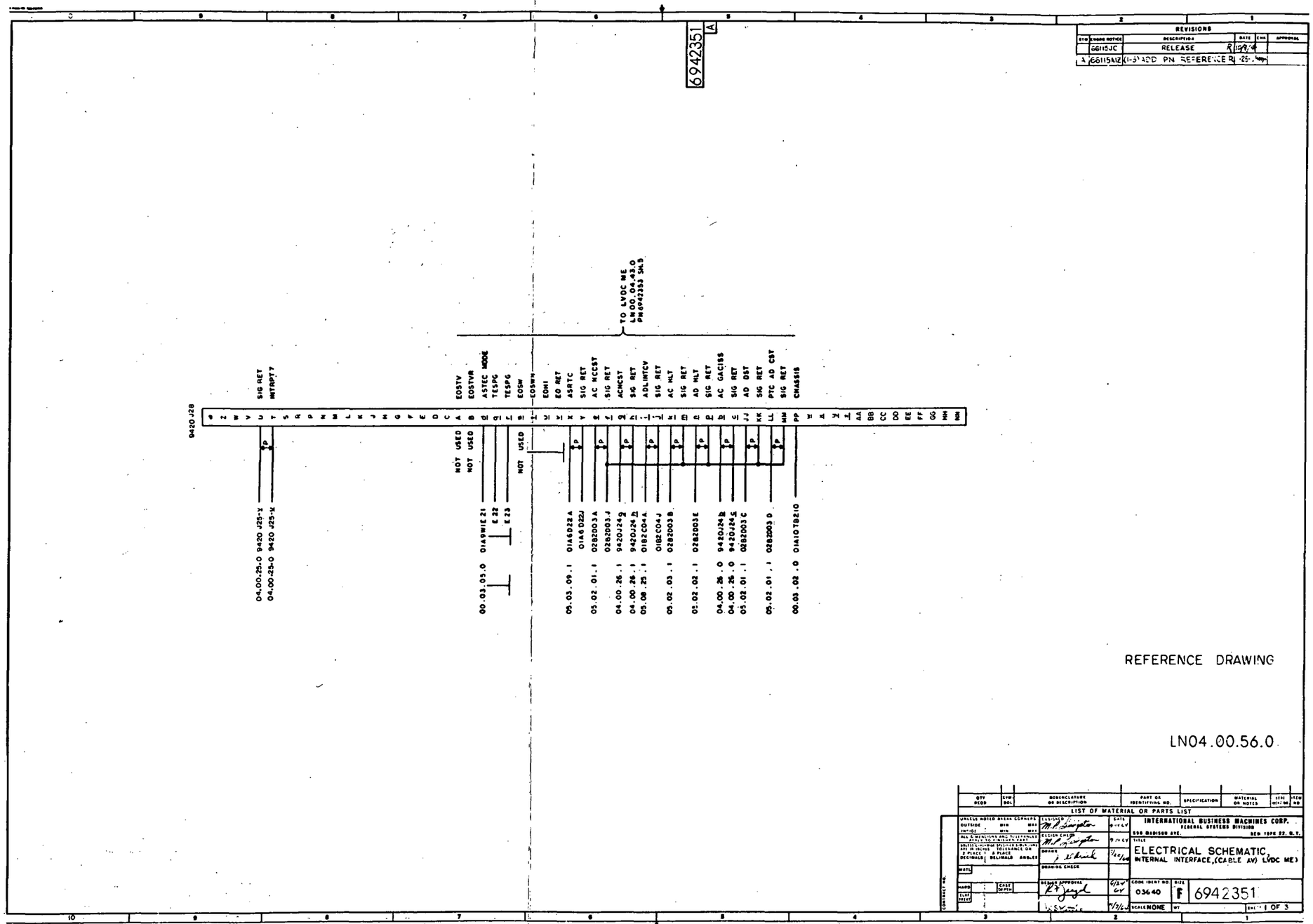


Figure 10-36. AV Cable Interface (Connector 9420 J28) Electrical Schematic Diagram (LN 04.00.56.0)

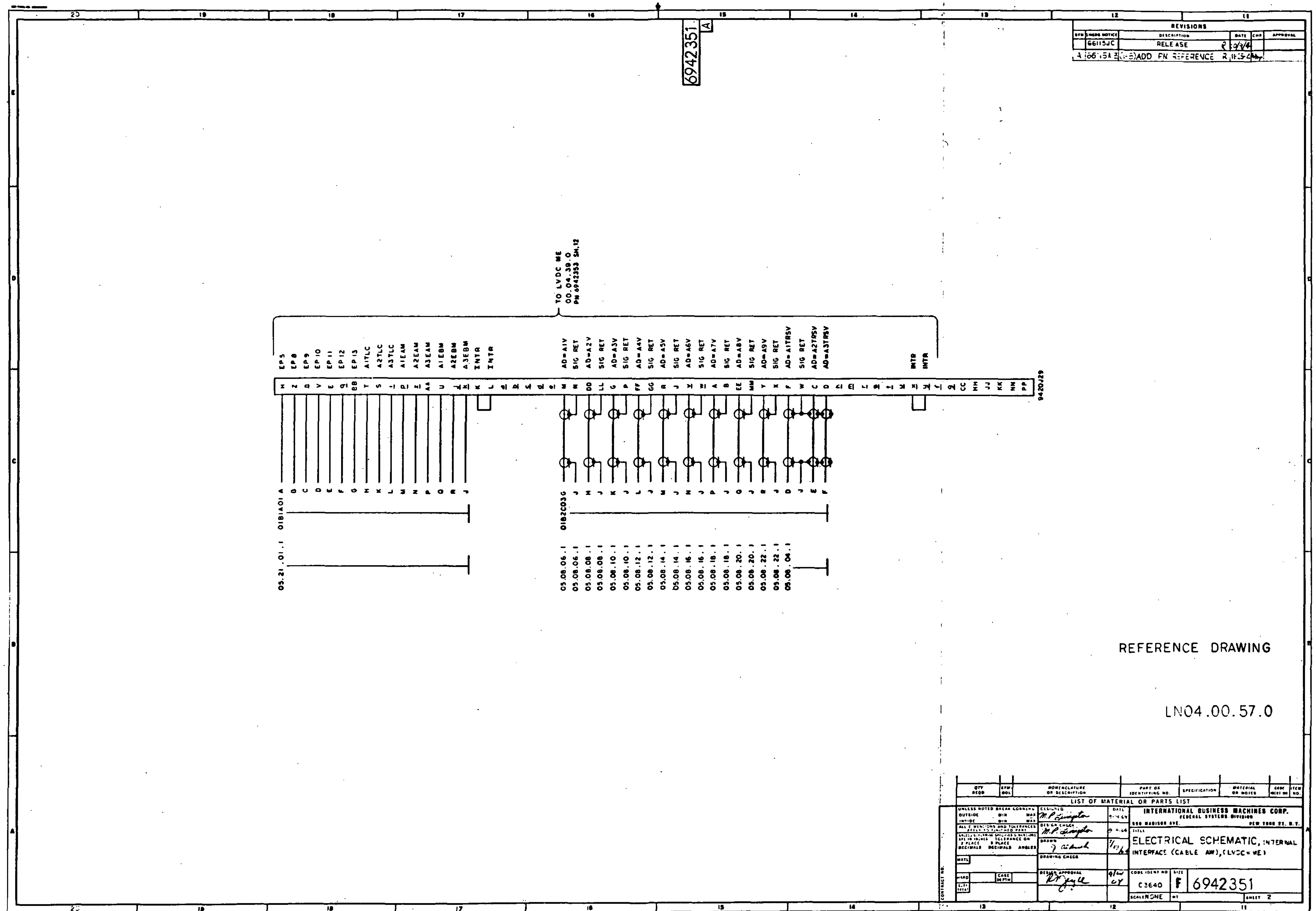


Figure 10-37. AW Cable Interface (Connector 9420 J29) Electrical Schematic Diagram (LN 04. 00. 57. 0)

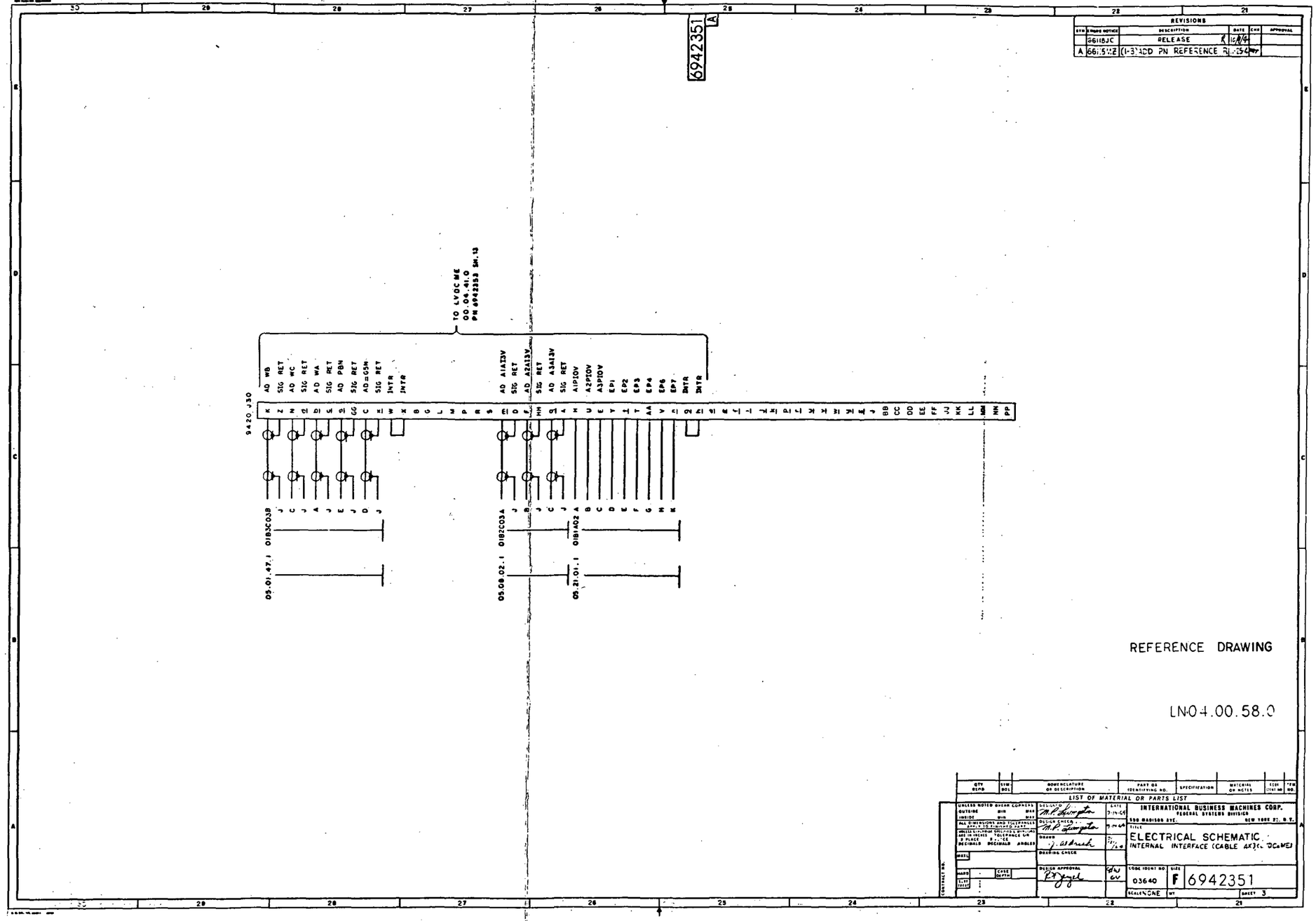


Figure 10-38. AX Cable Interface (Connector 9420 J30) Electrical Schematic Diagram (LN 04.00.58.0)

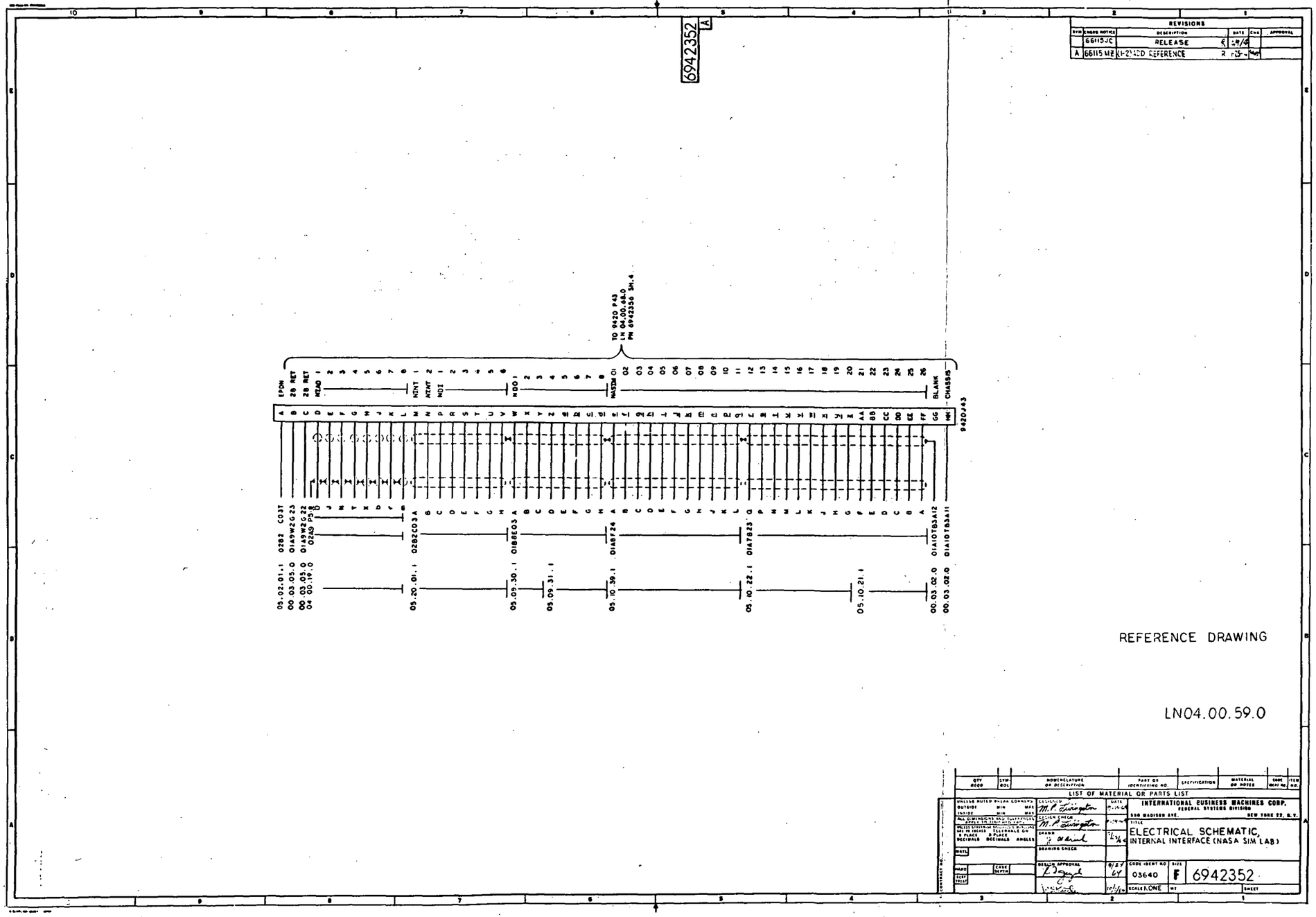


Figure 10-39. NASA SIM LAB Cable Interface (Connector 9420 J43) Electrical Schematic Diagram (LN 04. 00. 59. 0)

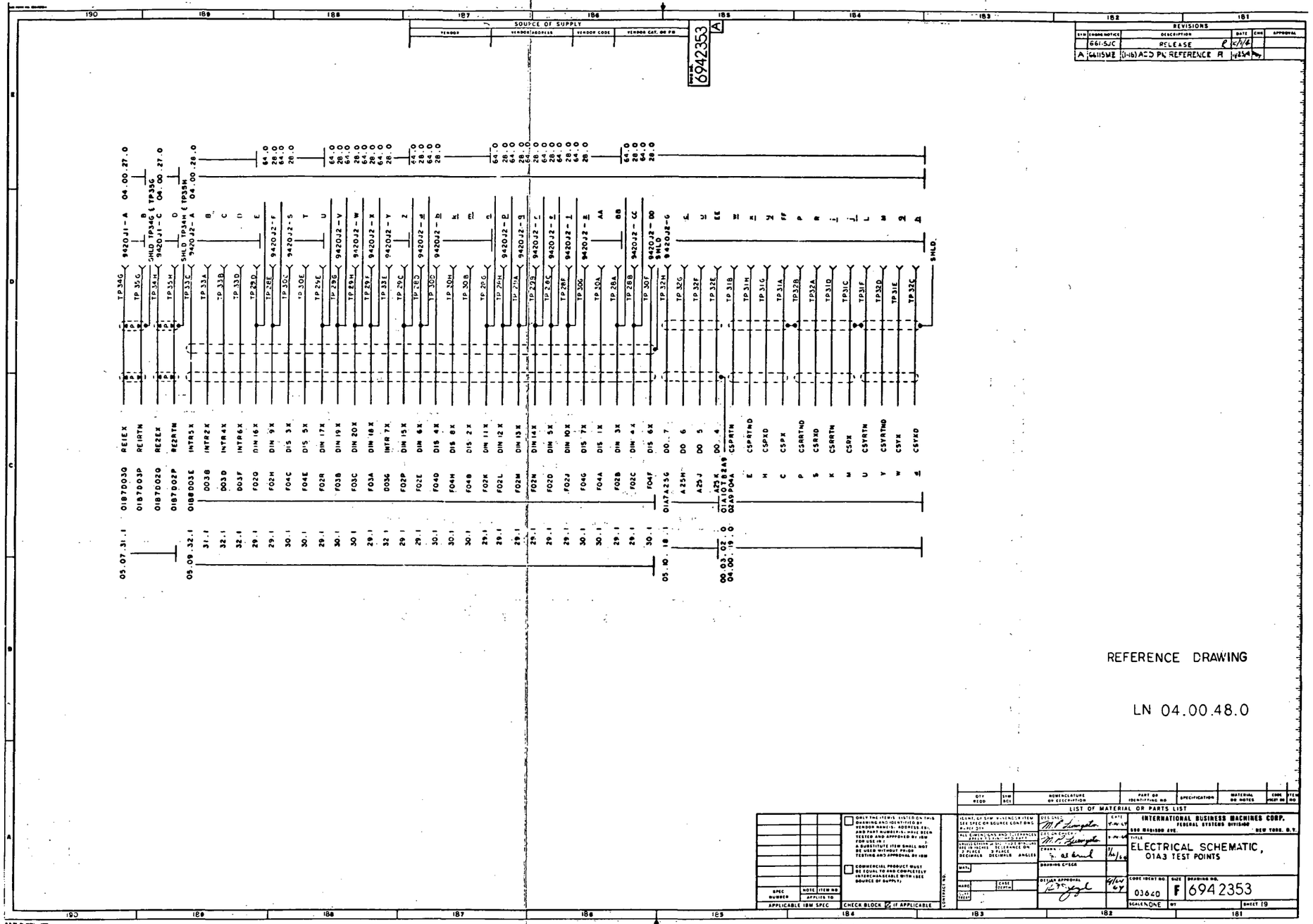


Figure 10-40. Panel 01A3 Test Points Electrical Schematic Diagram (LN 04.00.48.0 through LN 04.00.53.0) (Sheet 1 of 6)

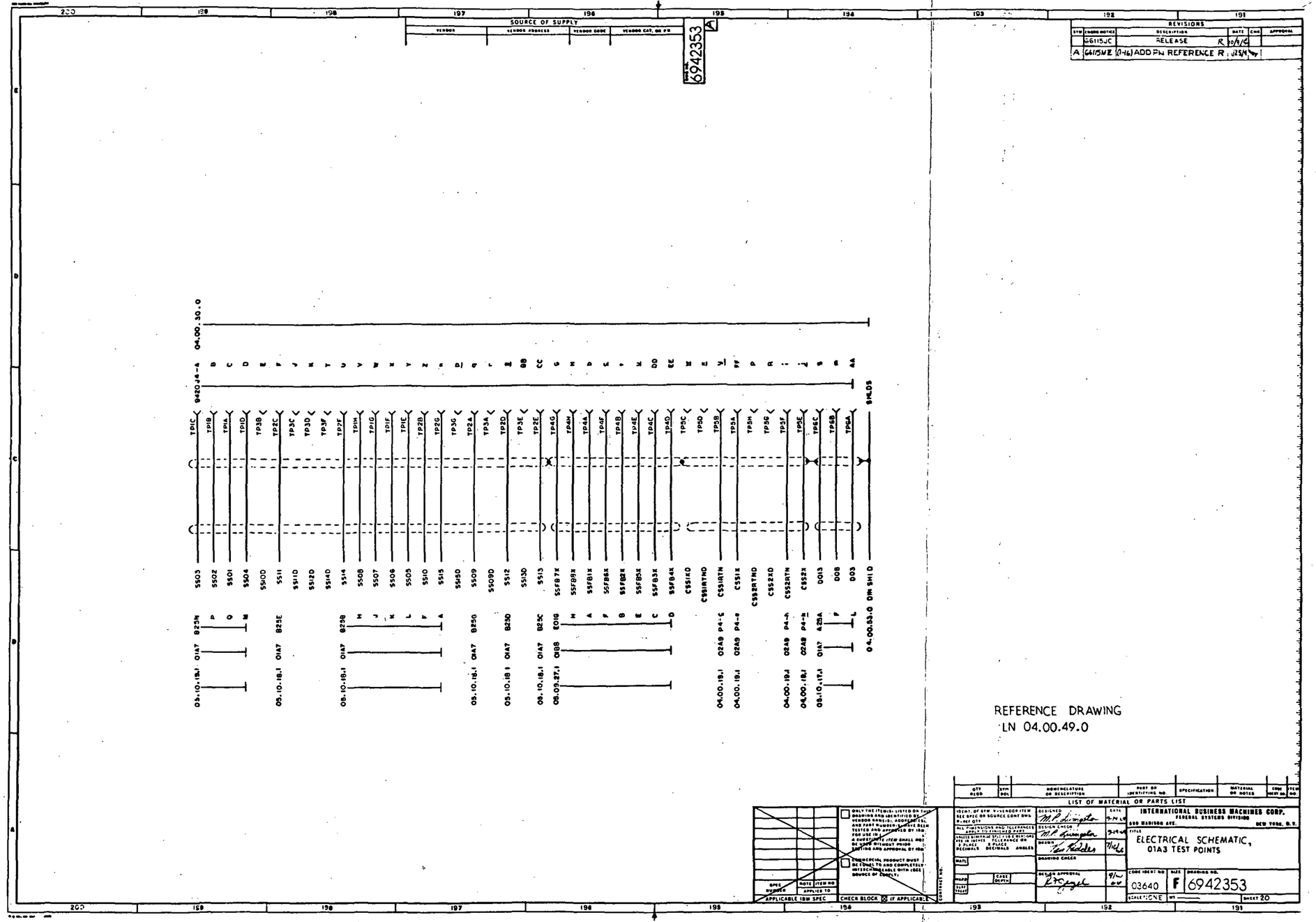


Figure 10-40. Panel 01A3 Test Points Electrical Schematic Diagram (LN 04.00.48.0 through LN 04.00.53.0) (Sheet 2)

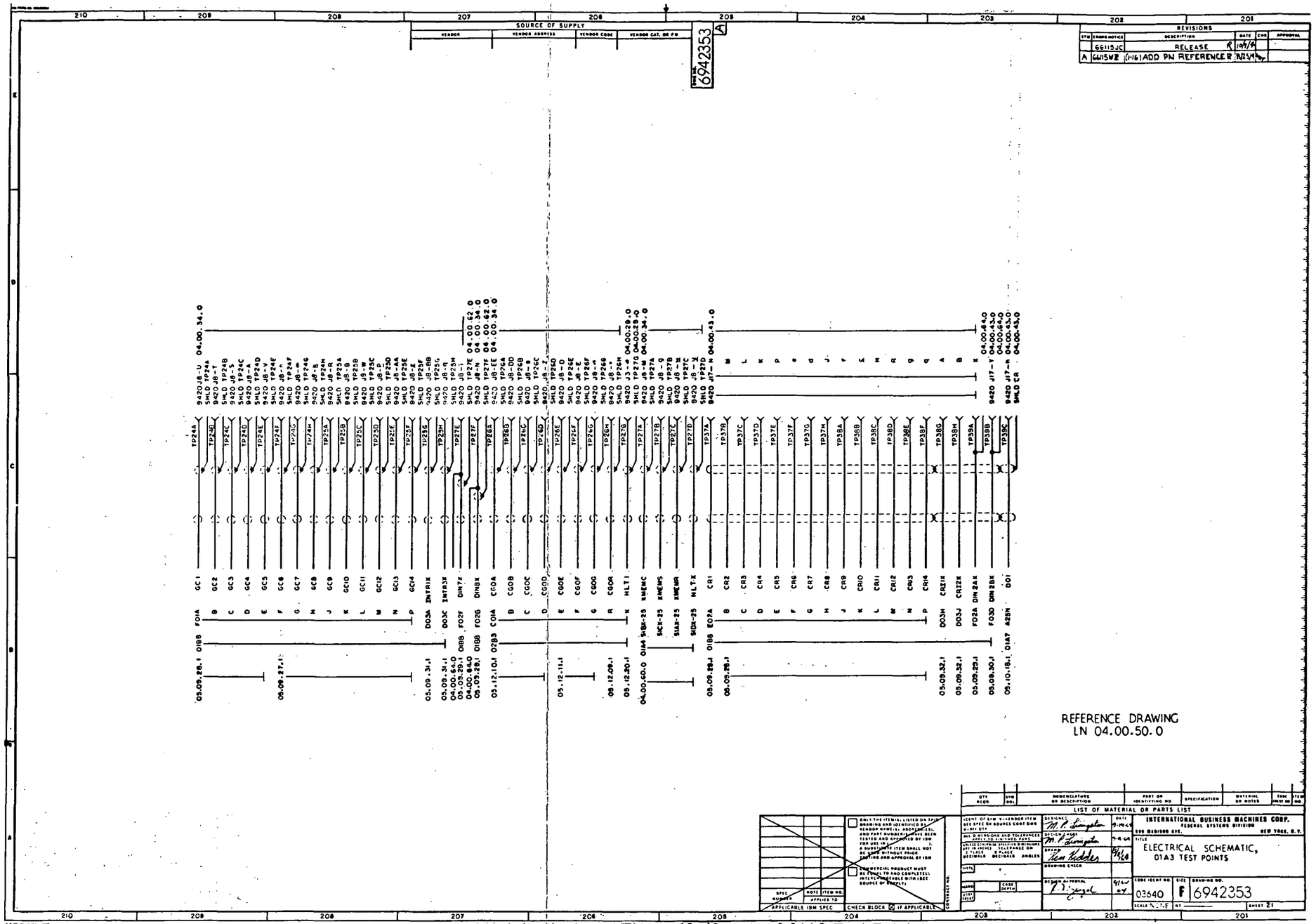


Figure 10-40. Panel 01A3 Test Points Electrical Schematic Diagram (LN 04.00.48.0 through LN 04.00.53.0) (Sheet 3)

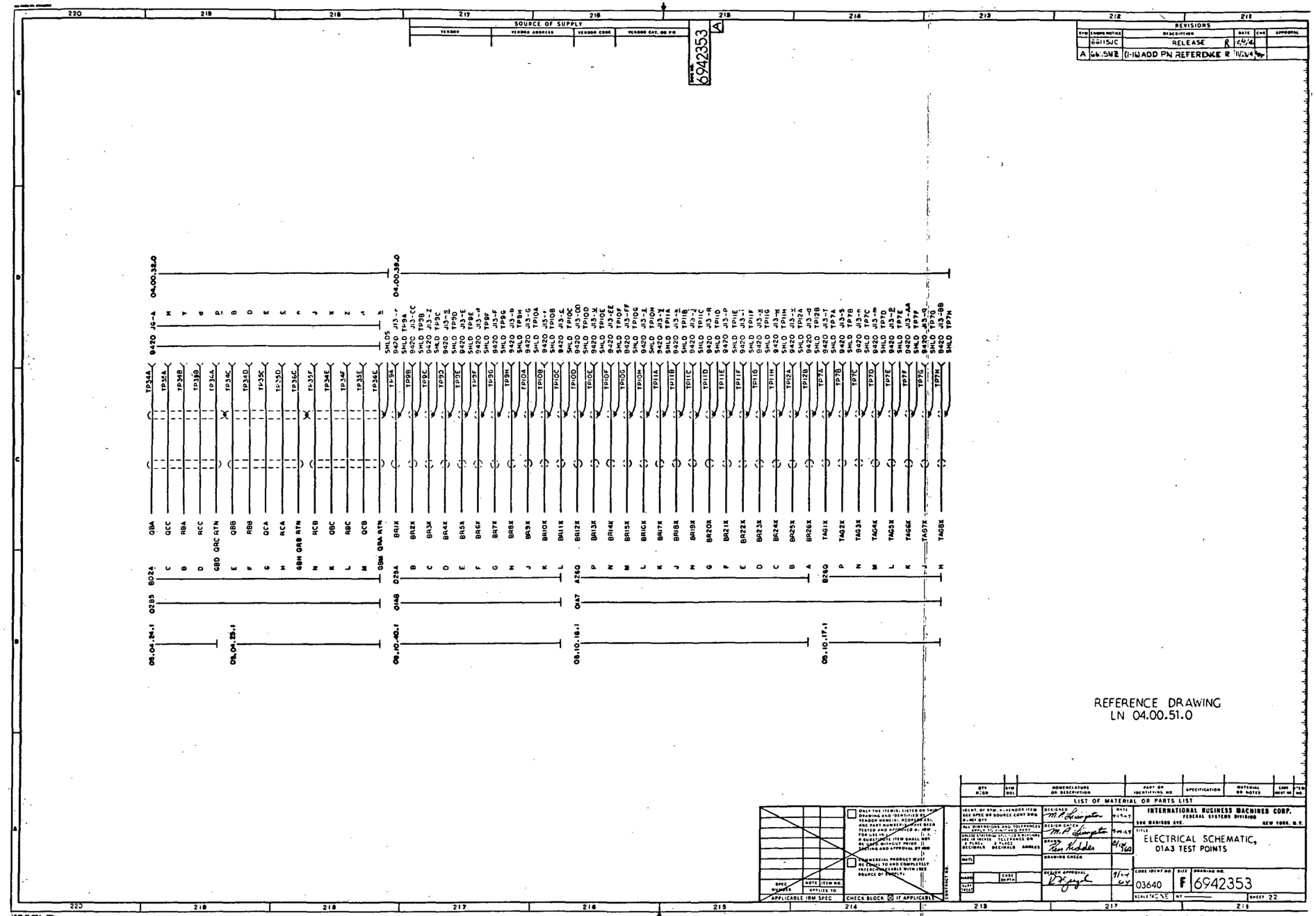


Figure 10-40. Panel 01A3 Test Points Electrical Schematic Diagram (LN 04.00.48.0 through LN 04.00.53.0) (Sheet 4)

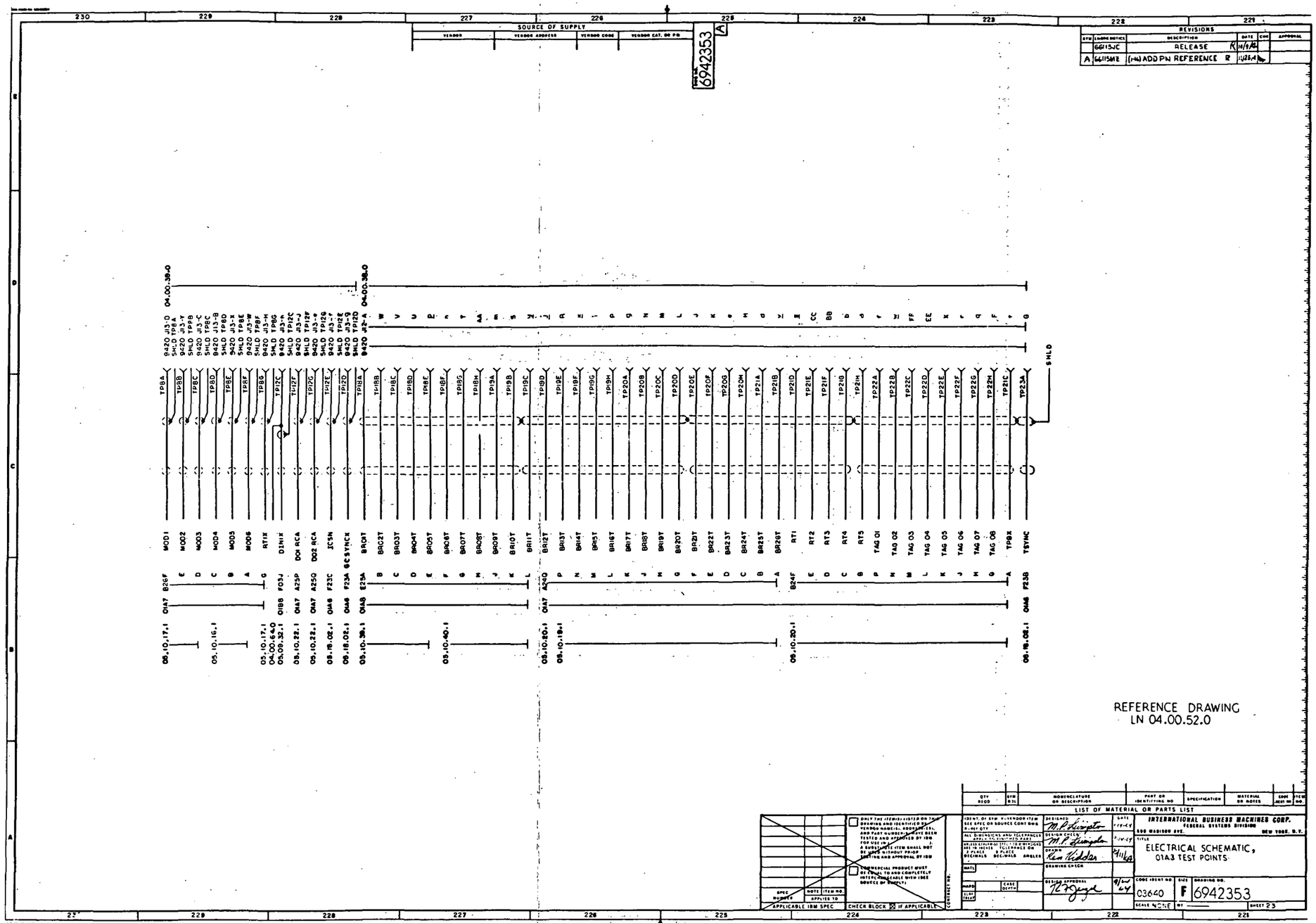


Figure 10-40. Panel 01A3 Test Points Electrical Schematic Diagram (LN 04.00.48.0 through LN 04.00.53.0) (Sheet 5)

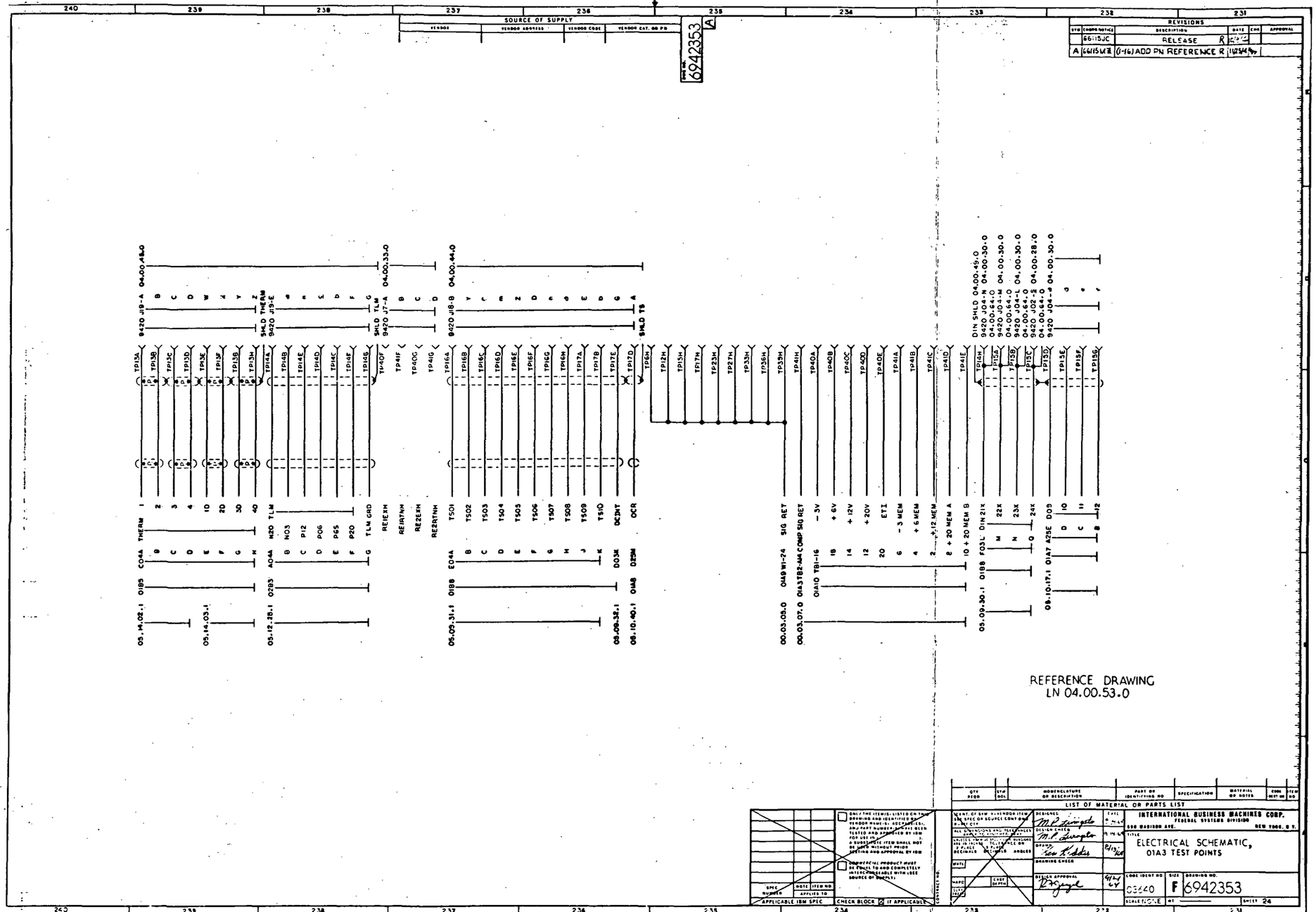


Figure 10-40. Panel 01A3 Test Points Electrical Schematic Diagram (LN 04.00.48.0 through LN 04.00.53.0) (Sheet 6)

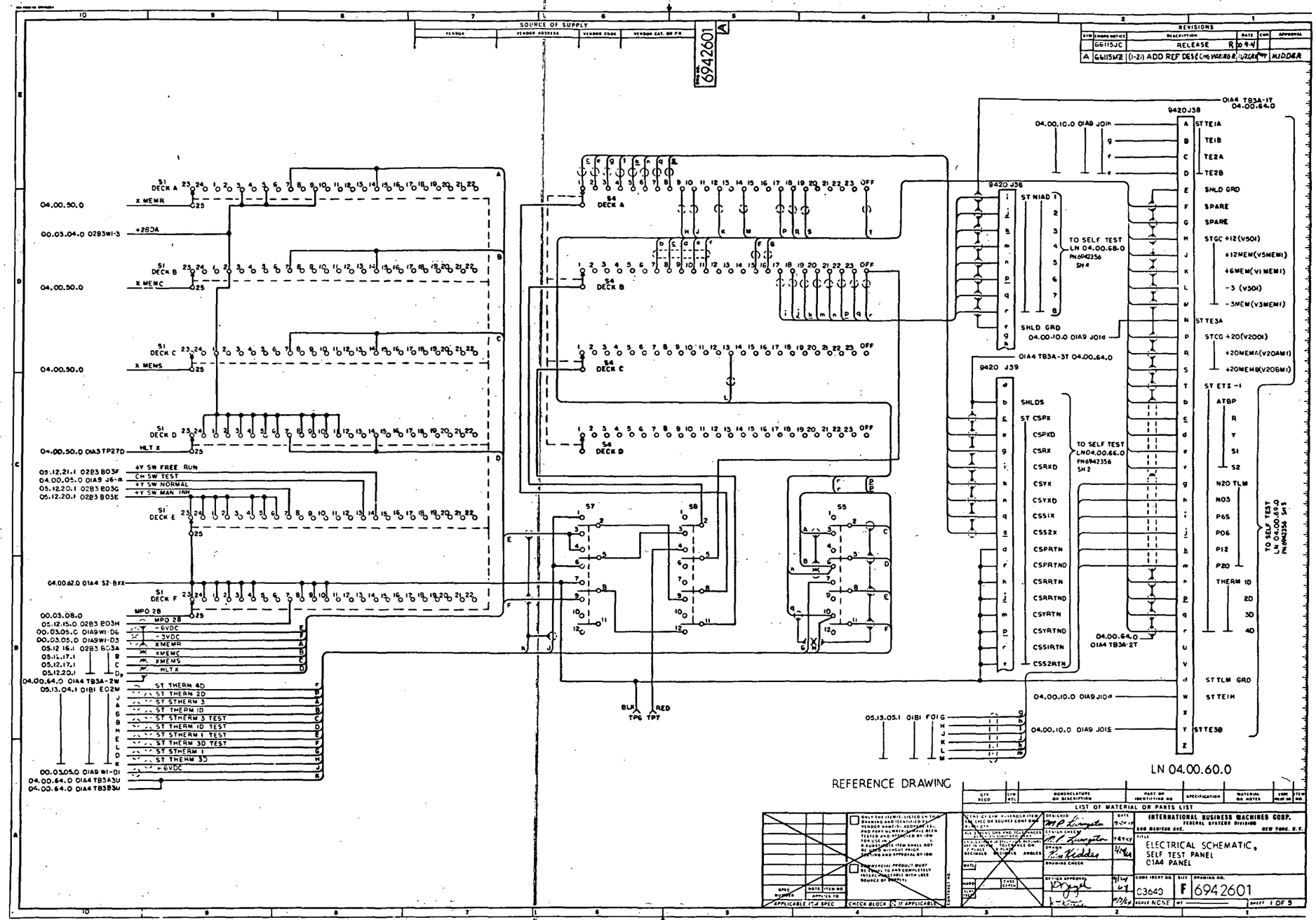


Figure 10-41. Self-Test Panel (01A4) Electrical Schematic Diagram (LN 04.00.60.0 through LN 04.00.64.0) (Sheet 1 of 5)

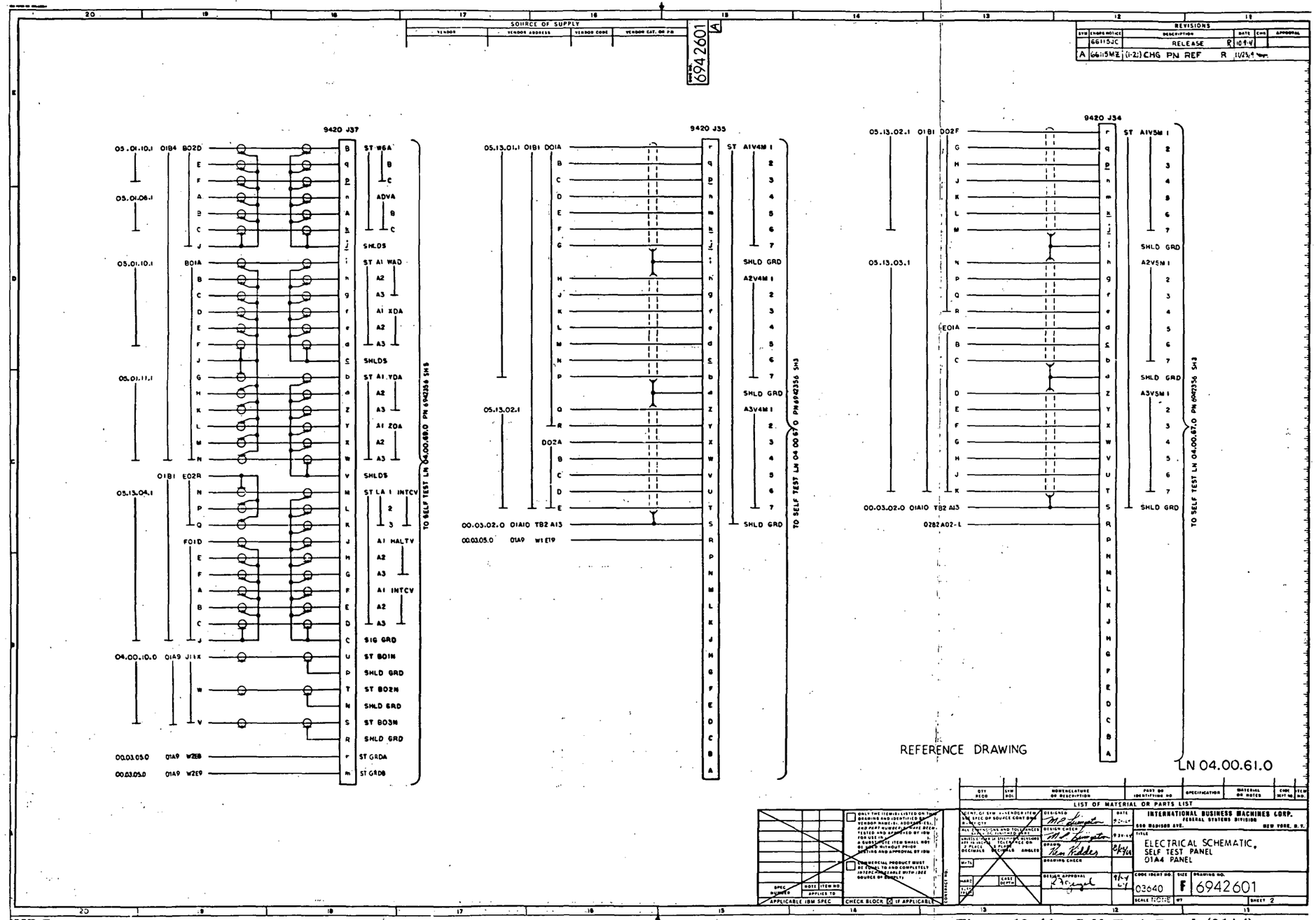


Figure 10-41. Self-Test Panel (01A4) Electrical Schematic Diagram (LN 04.00.60.0 through LN 04.00.64.0) (Sheet 2)

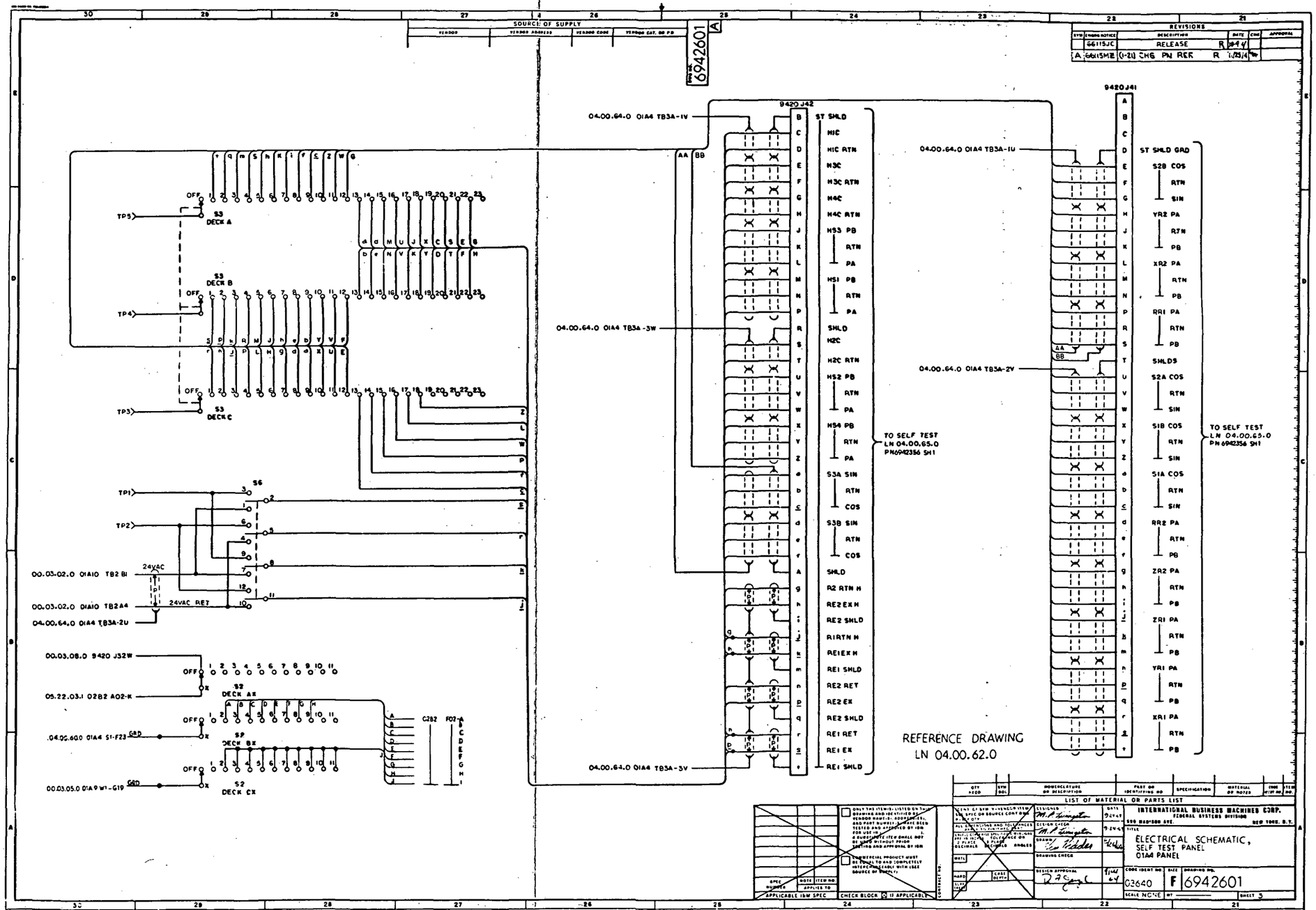


Figure 10-41. Self-Test Panel (01A4) *Electrical Schematic Diagram* (LN 04.00.60.0 through LN 04.00.64.0) (Sheet 3)

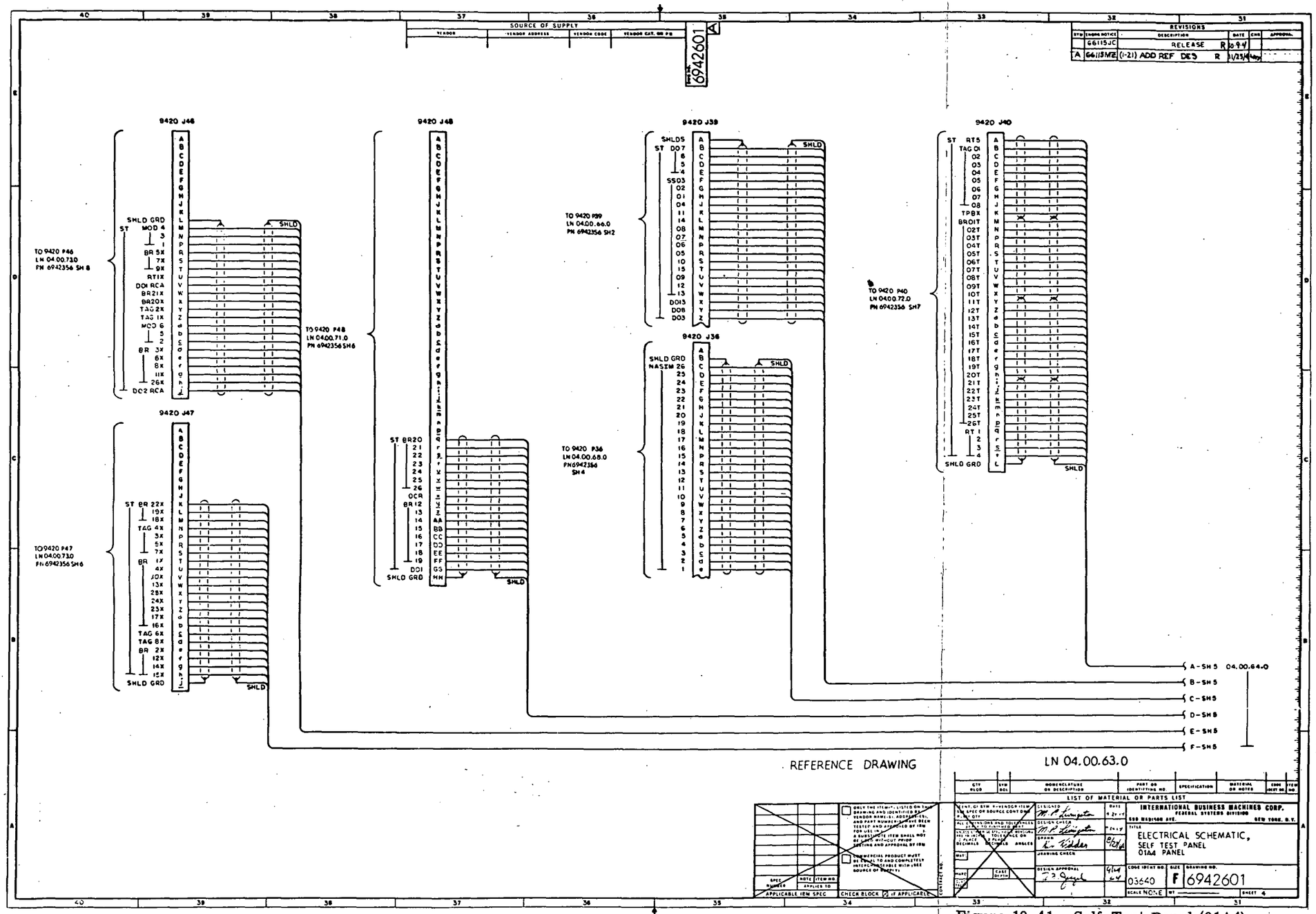


Figure 10-41. Self-Test Panel (01A4) Electrical Schematic Diagram (LN 04. 00. 60. 0 through LN 04. 00. 64. 0) (Sheet 4)

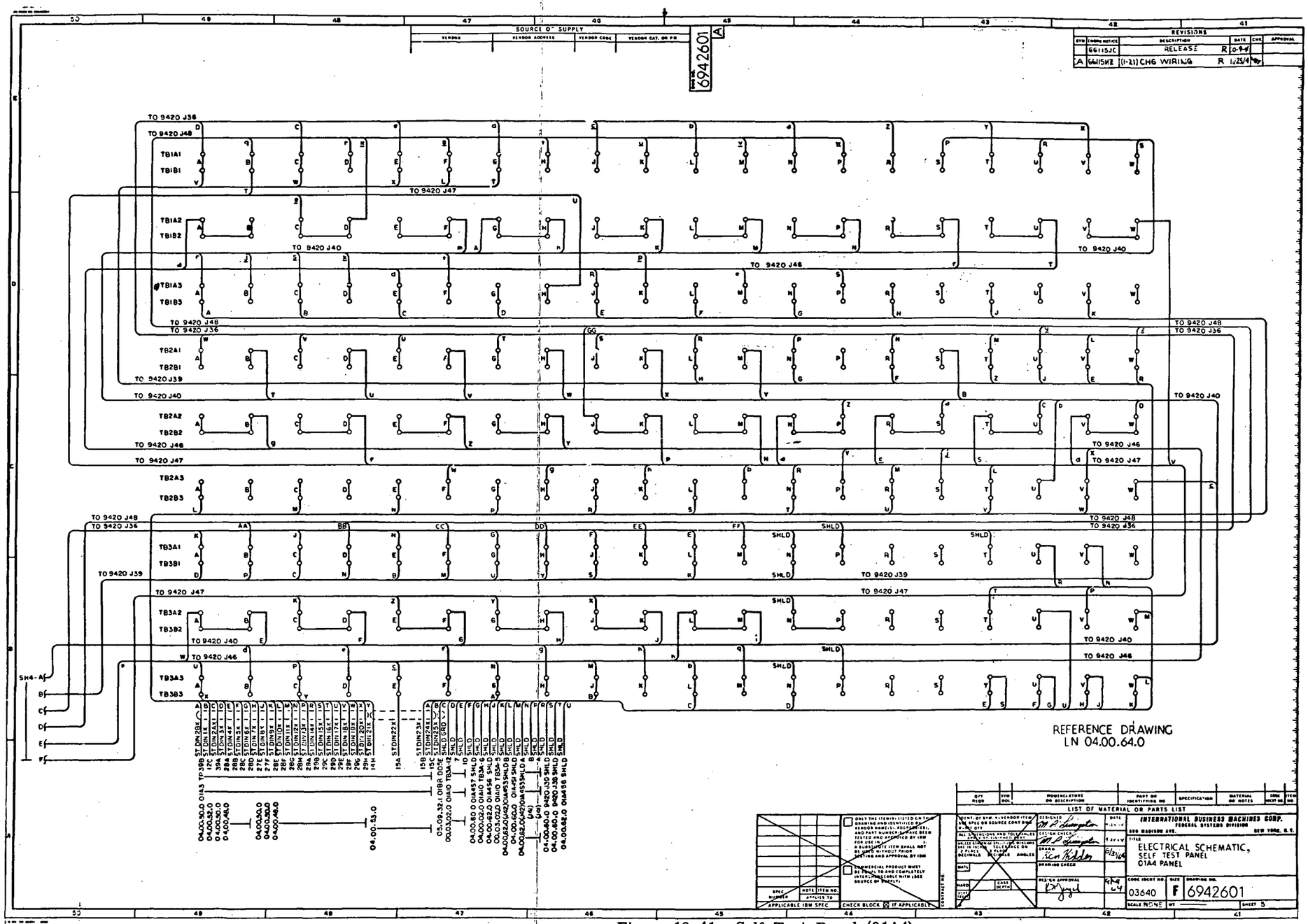


Figure 10-41. Self-Test Panel (01A4) Electrical Schematic Diagram (LN 04.00.60.0 through LN 04.00.64.0) (Sheet 5)

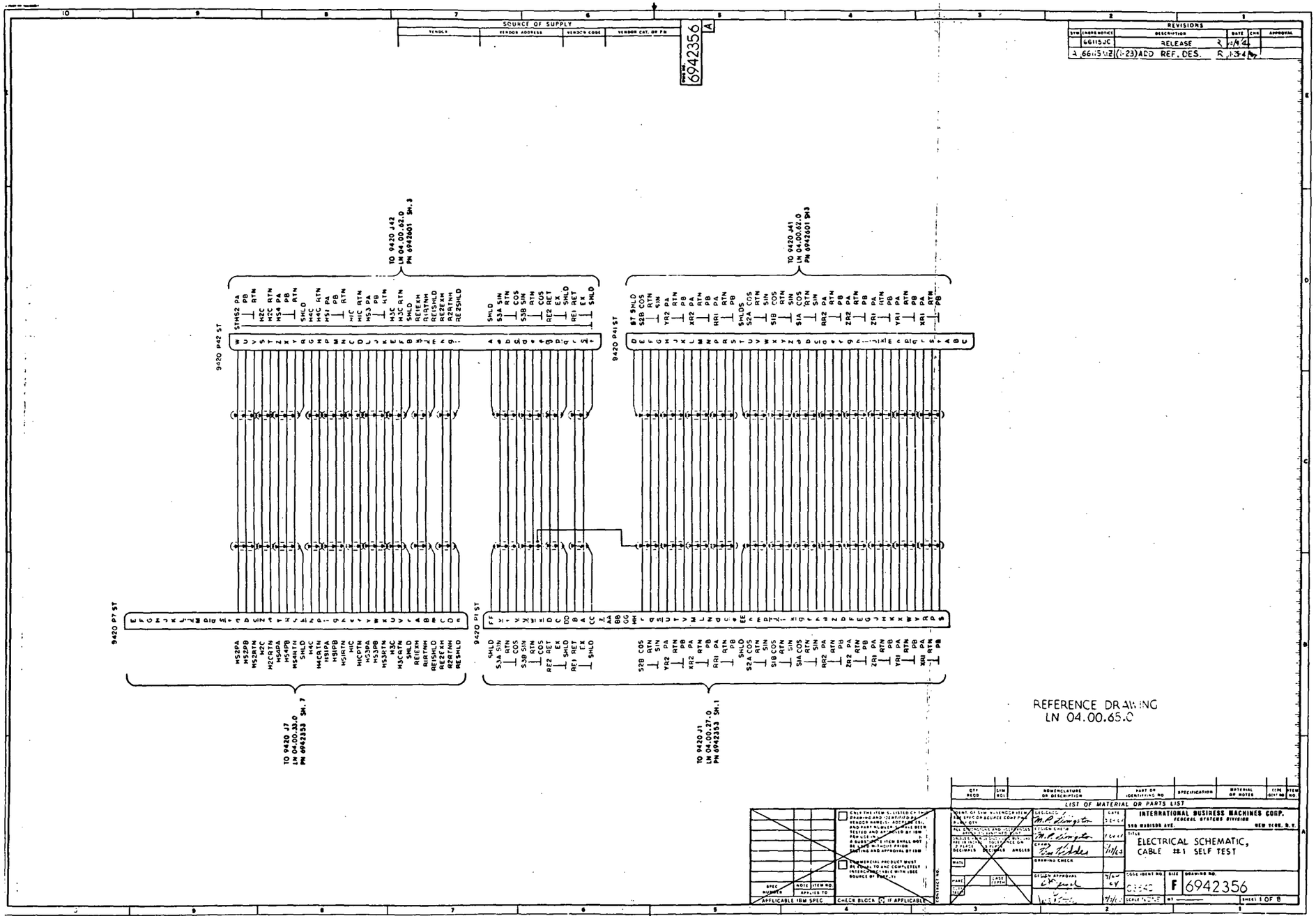


Figure 10-42. Self-Test Cable No. 1 Electrical Schematic Diagram (LN 04. 00. 65. 0)

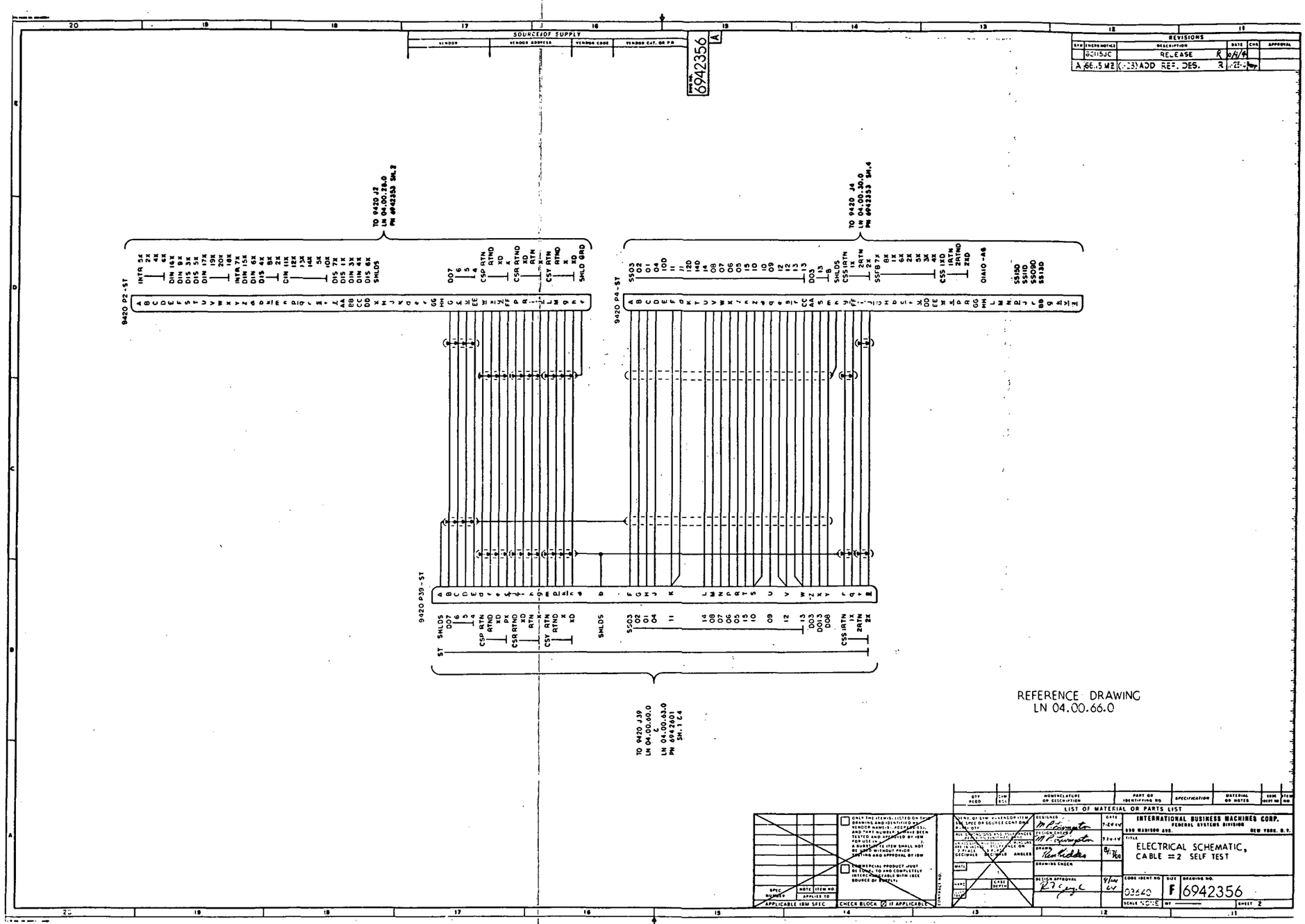


Figure 10-43. Self-Test Cable No. 2 Electrical Schematic Diagram (LN 04. 00. 66. 0)

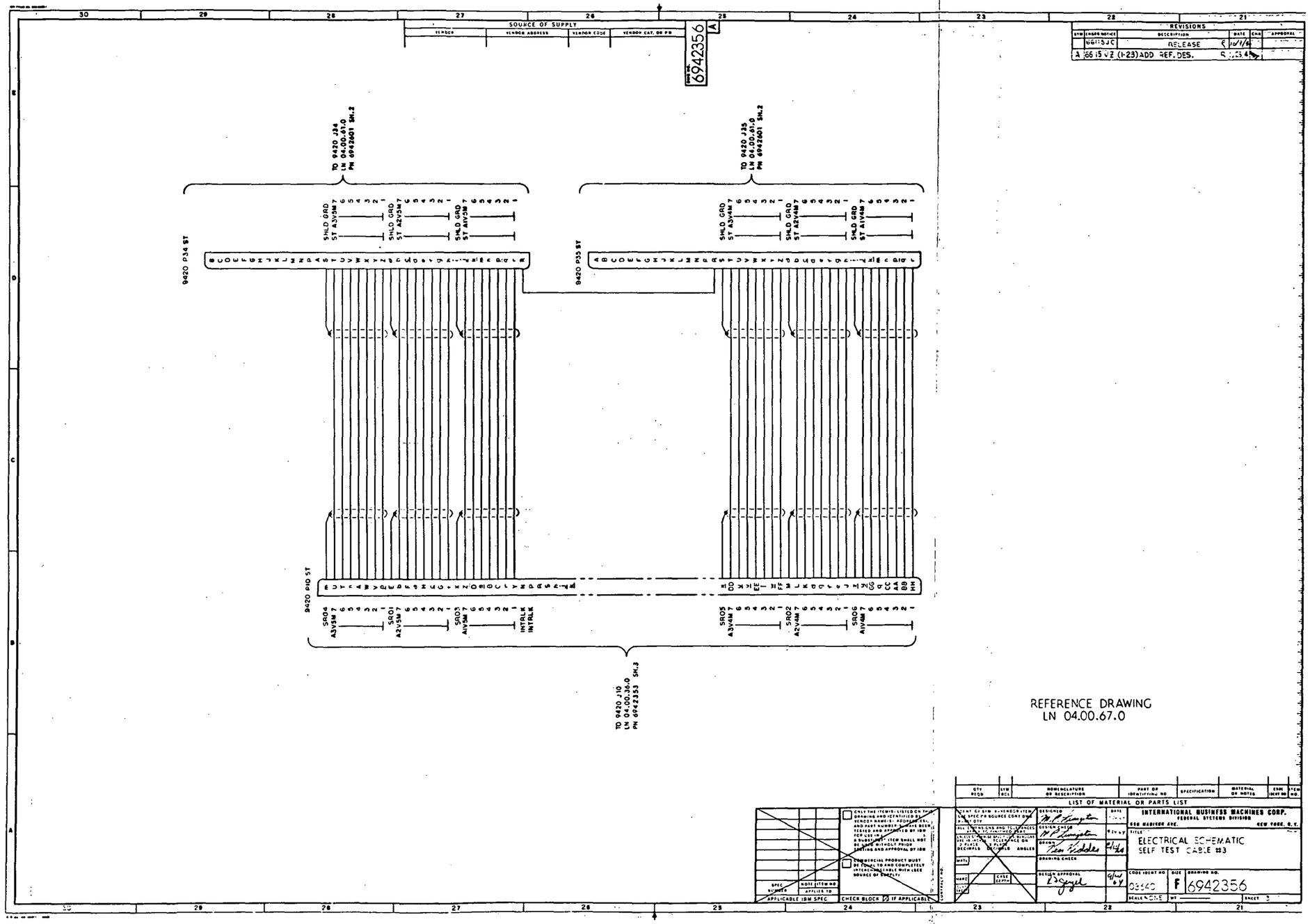


Figure 10-44. Self-Test Cable No. 3 Electrical Schematic Diagram (LN 04. 00. 67. 0)

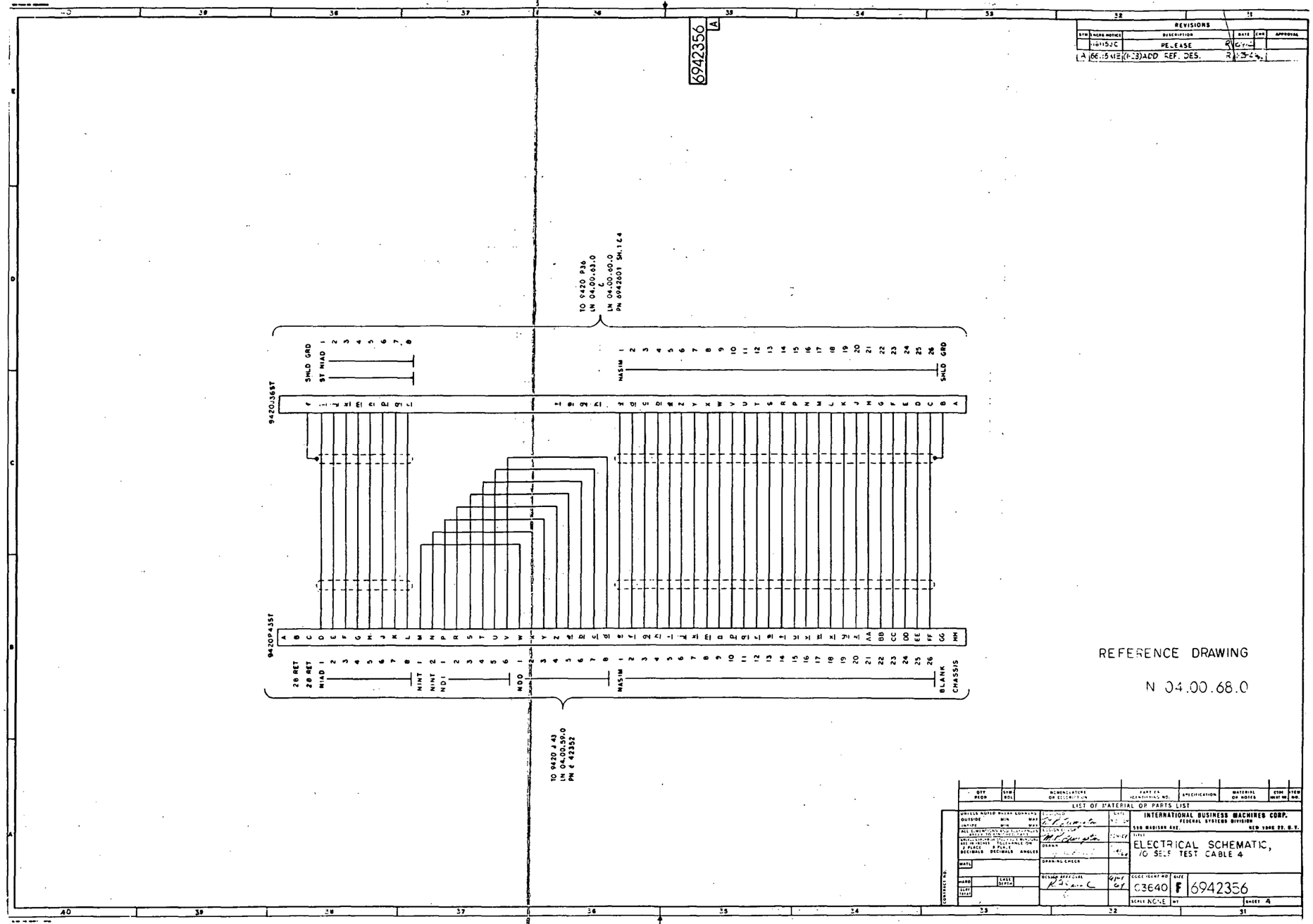


Figure 10-45. Self-Test Cable No. 4
Electrical Schematic Diagram
(LN 04. 00. 68. 0)

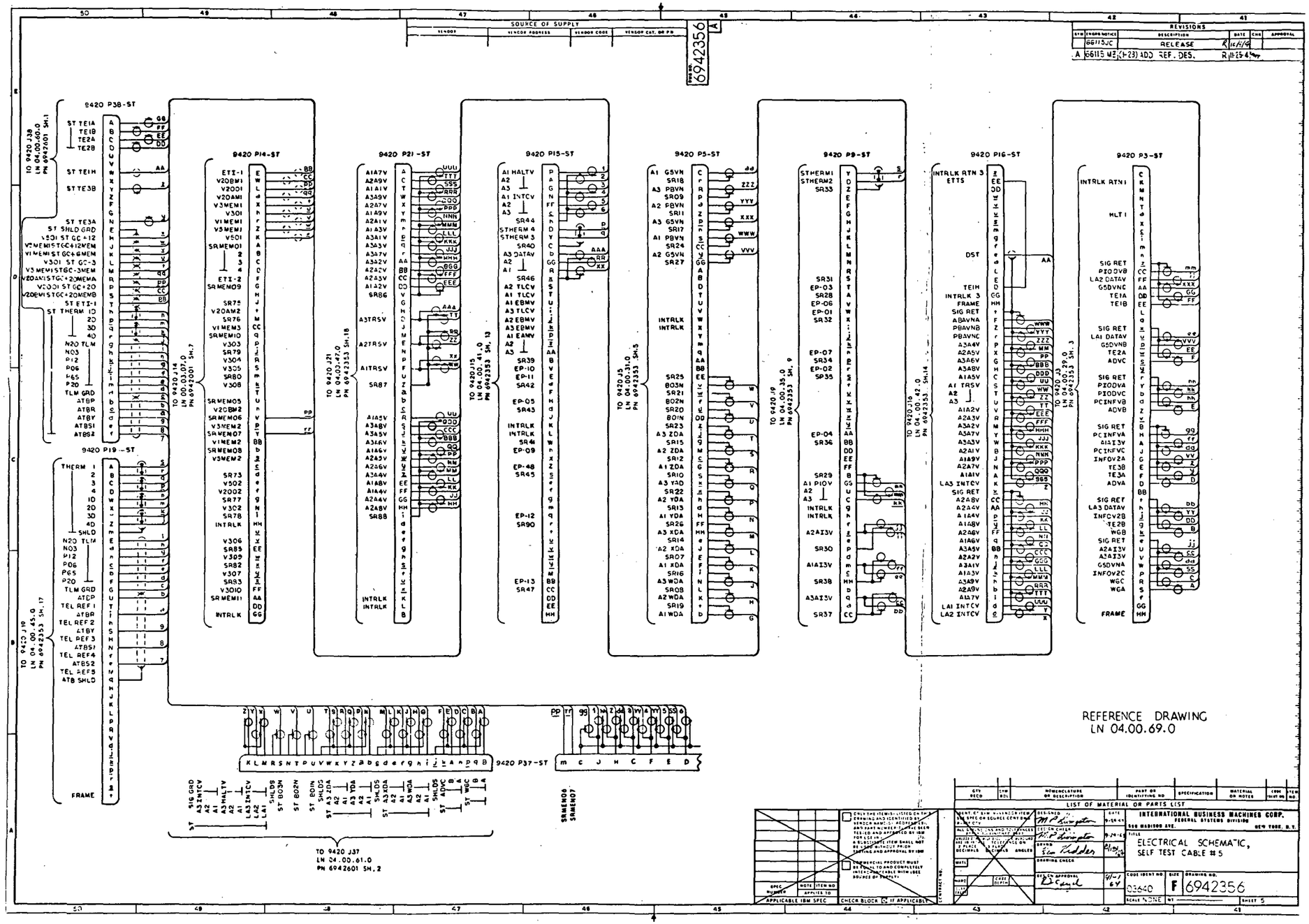


Figure 10-46. Self-Test Cable No. 5 Electrical Schematic Diagram (LN 04. 00. 69. 0)

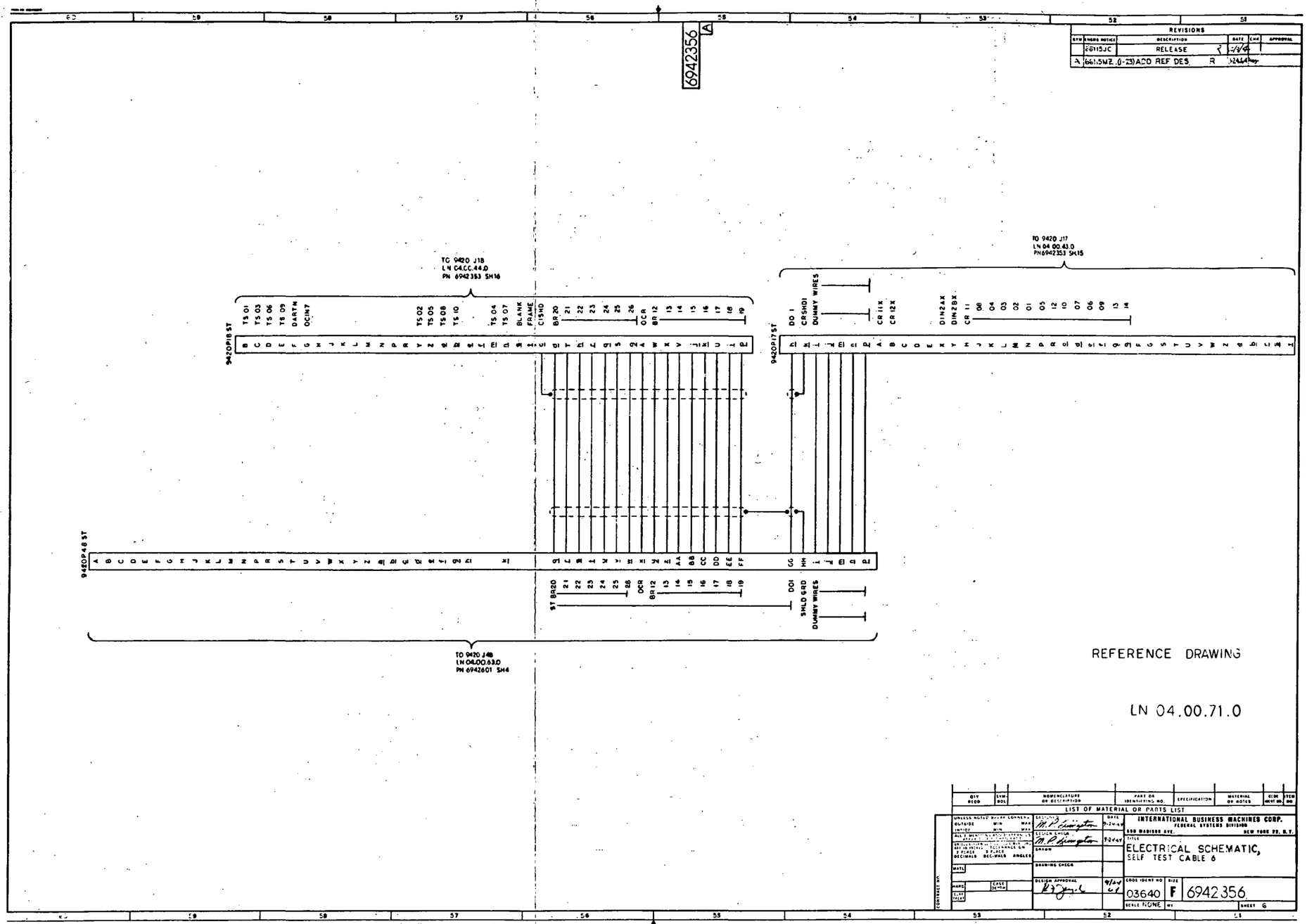


Figure 10-47. Self-Test Cable No. 6 Electrical Schematic Diagram (LN 04. 00. 71. 0)

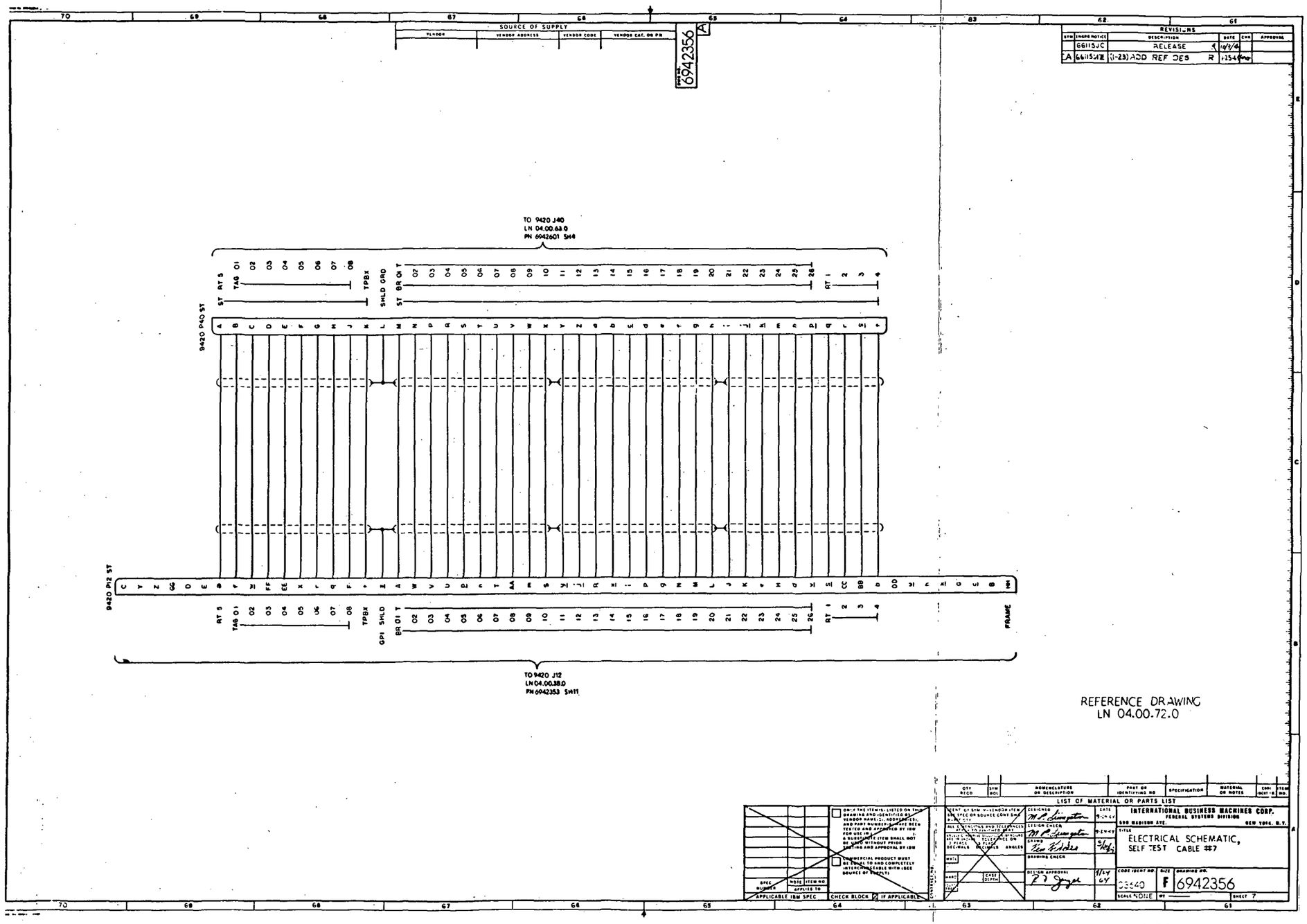


Figure 10-48. Self-Test Cable No. 7 Electrical Schematic Diagram (LN 04. 00. 72. 0)

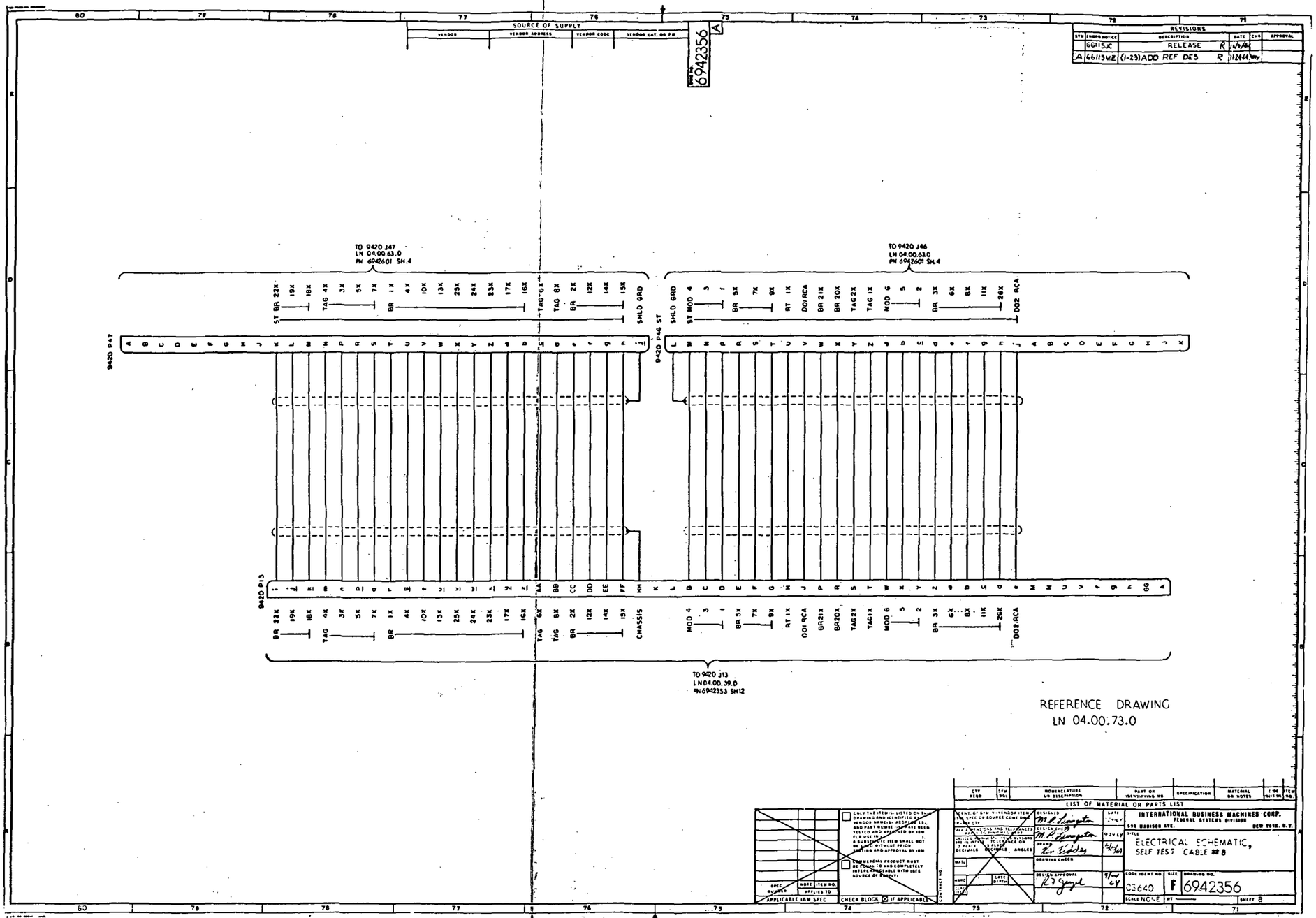


Figure 10-49. Self-Test Cable No. 8
Electrical Schematic Diagram
(LN 04. 00. 73. 0)

6942020

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

SYMBOL INDEX

1. AND
2. AND-Invert
3. AND-OR-Invert
4. Transient Detector
5. Delay
6. Driver Terminator
7. Inverter
8. Inverter-OR
9. Latch 1
10. Latch 2
11. Latch 3
12. Latch 4
13. Latch 5
14. Latch 6
15. Lamp Driver
16. Line Driver
17. Oscillator
18. OR-Invert
19. Power Driver
20. Relay Driver
21. Relay
22. Resistor
23. Resistor
24. Selected Interrupt
25. Single Slot
26. Translator
27. Translator Inverter
28. Tratch
29. Trigger
30. Temperature Sensor
31. Voltage Divider

SYMBOL DEFINITIONS

NOTE

A logic "one" is a -6VDC (or -12VDC) level and a logic "zero" is a 0VDC level unless otherwise noted.

INDEX NO.	SYMBOL	NAME	DESCRIPTION
1.	A (MULTIPLE INPUT)	AND	When all inputs are "1", the output is a "1". If any input is a "0", the output is a "0".
2.	A (MULTIPLE INPUT)	AND-INVERT	When all inputs are "1", the output is a "0". If any input is a "0", the output is a "1".
3.	AO	AND-OR-IN-VERT	Inputs - outputs are the same as an And-Invert. The output transistor allows the outputs of several And-Or-Inverts to be connected (OR'd) together. A "0" output of any AO of an "OR'd" group of AO's will force a "0" output from the group.
4.	1 2 3 4 DET	TRANSIENT DETECTOR	Produces a "1" output when a transient is detected at either input 1 or input 4 while input 2 is a "0". A "0" at input 3 forces a "0" output.
5.	X USEC DLY	DELAY	The Delay circuit delays the input signal for the nominal duration shown above the symbol.
6.	DT	DRIVER TERMI-NATOR	Signal shaper and low impedance matching device.
7.	I	INVERTER	A "1" input will result in a "0" output and vice-versa.
8.	IO	INVERTER-OR	Input - output same as Inverter. The output transistor allows the outputs of several Inverter-Ors to be connected (OR'd) together; a "0" output of any IO of an "OR'd" group of IO's will force a "0" output from the group.
9.	"0" SET, L1, SET OUTPUT, RESET OUTPUT, "0" RESET	LATCH 1	"0" SET — IO — SET OUTPUT; "0" RESET — IO — RESET OUTPUT. The set and reset outputs are complementary. A "0" at the "0" set input will cause the set output to become a "1" and the reset output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed. Similarly, a "0" at the "0" reset input will cause the reset output to become a "1" and the set output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed.

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
10.	"0" SET, "1" SET, L2, SET OUTPUT, "1" RESET, RESET OUTPUT, "0" RESET	LATCH 2	"0" SET, "1" SET — A — OR — SET OUTPUT; "1" RESET — A — OR — RESET OUTPUT; "0" RESET. Same as Latch 1. A "1" at the "1" set input will cause the set output to become a "1" and the reset output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed. Similarly, a "1" at the "1" reset input will cause the reset output to become a "1" and the set output to become a "0"; the outputs will remain in this condition even after the input conditioning level is removed.
11.	"0" SET, L3, SET OUTPUT, RESET OUTPUT, "0" RESET	LATCH 3	"0" SET — A — SET OUTPUT; "0" RESET — I — RESET OUTPUT. See Latch 1.
12.	"0" SET, L4, SET OUTPUT, RESET OUTPUT, "0" RESET	LATCH 4	"0" SET — A — SET OUTPUT; "0" RESET — A — RESET OUTPUT. See Latch 1.
13.	"0" SET, "1" SET, L5, SET OUTPUT, RESET OUTPUT, "0" RESET	LATCH 5	"1" SET — OR — SET OUTPUT; "0" SET — A — RESET OUTPUT; "0" RESET — A. See Latch 1 and Latch 2
14.	"1" SET, L6, SET OUTPUT, RESET OUTPUT, "0" RESET	LATCH 6	"1" SET — OR — SET OUTPUT; I — RESET OUTPUT; A. "0" RESET. See Latch 1 and Latch 2

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
15.	LD	LAMP DRIVER	A "1" input causes the Lamp Driver to turn on its associated indicator lamp; a "0" input causes the Lamp Driver to turn off its associated indicator lamp.
16.	LINE DR	LINE DRIVER	Signal driver and low impedance matching device.
17.	2.048 MC OSC	OSCILLATOR	Generates a square wave signal (0VDC to -6VDC) at a 2.048 MC frequency.
18.	OR	OR-INVERT	When all inputs are "0", the output is a "1". If any input is a "1", the output is a "0". The outputs of several Or-Inverts can be OR'd together.
19.	PD	POWER DRIVER	Signal shaper and driver — a "1" input causes a "1" output; a "0" input causes a "0" output.
20.	RELAY DR	RELAY DRIVER	Input: "1" = 0VDC; "0" = -26.5VDC
21.	RLY	RELAY	RELAY COIL, NORMALLY OPEN, NORMALLY CLOSED, RELAY COIL, ARMATURE
22.	R	RESISTOR	
23.	R	RESISTOR	
24.	SI	SELECTED INTERRUPT	A selection network. Outputs are dependent on card type used.

REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE MFRS NO	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX. ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED MINIMUM BREAK ON SHARP EDGES AT PLACE DECIMALS FOR DECIMALS ANGLES. MATL. HARD SOFT. CASE DEPTH. CONTRACT NO.

DESIGNED — DATE

INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION
850 MADISON AVE., NEW YORK 22, N.Y.

DESIGN CHECK W. K. Hurley 9-11-68
DRAWN IBM
DRAWING CHECK
DESIGN APPROVAL M. P. Livingston 9-11-68

LOGIC DIAGRAM, LAUNCH VEHICLE DATA ADAPTER MANUAL EXERCIZER (LVDA-ME)-SYMBOL DEFINITIONS

CODE IDENT NO. | SIZE F | 6942020

SCALE | WT | SHEET 1 OF 75

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 1 of 78)

6942020

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
25.	X USEC SS	SINGLE SHOT	Any or all three inputs may be connected. An unconnected input (indicated by the absence of an input) is effectively a "1" input. All inputs must equal "1" to trigger the single shot. The negative going transition of the last input to become a "1" triggers the single shot. The duration of the negative square wave output is shown above the symbol.
26.	TSLT	TRANSLATOR	Input: +6VDC ("1"), 0VDC ("0") Output: -6VDC ("1"), 0VDC ("0")
27.	TSLI	TRANSLATOR INVERTER	Input: +6VDC ("1"), 0VDC ("0") Output: 0VDC ("0"), -6VDC ("1")
28.	"0" "0" "1" TCH "1" "1" "1"	TRATCH	A "0" input forces the corresponding output to a "0" and the other two outputs to "1's".
29.	A, B, "1" SET, SET OUTPUT, T, "1" RESET, RESET OUTPUT, C, D	TRIGGER	The set output becomes a "1" when input A is a "0" and input B goes from a "1" to a "0". The reset output becomes a "1" when input D is a "0" and input C goes from a "1" to "0". (The omission of "1" set and "1" reset inputs indicates that that these lines are grounded.)
30.	TS	TEMPERATURE SENSOR	Replaces thermistor in the LVDA during self check.
31.	VD	VOLTAGE DIVIDER	+12V, +8V, -8V, -12V

NOTES:

1. Abbreviations are:
   - MS millisecond
   - USEC microsecond
   - NSEC nanosecond
   - MC megacycles
2. The numbers listed in tabular INPUTS and OUTPUT columns are sheet number locations of signal origin and destinations.
3. All logic blocks are defined on sheets 1 and 2.

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPR'VAL

REFERENCE DRAWING

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX, INSIDE MIN MAX. ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±

DESIGNED — DATE

DESIGN CHECK W. K. Hurley 8-11-66

DRAWN IBM

DRAWING CHECK

MATL

HARD / SOFT TREAT — CASE DEPTH

DESIGN APPROVAL M. P. Farrington 8-11-66

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: SYMBOL DEFINITIONS

CODE IDENT NO. F — SIZE — 6942020

SCALE — WT — SHEET 2

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 2)

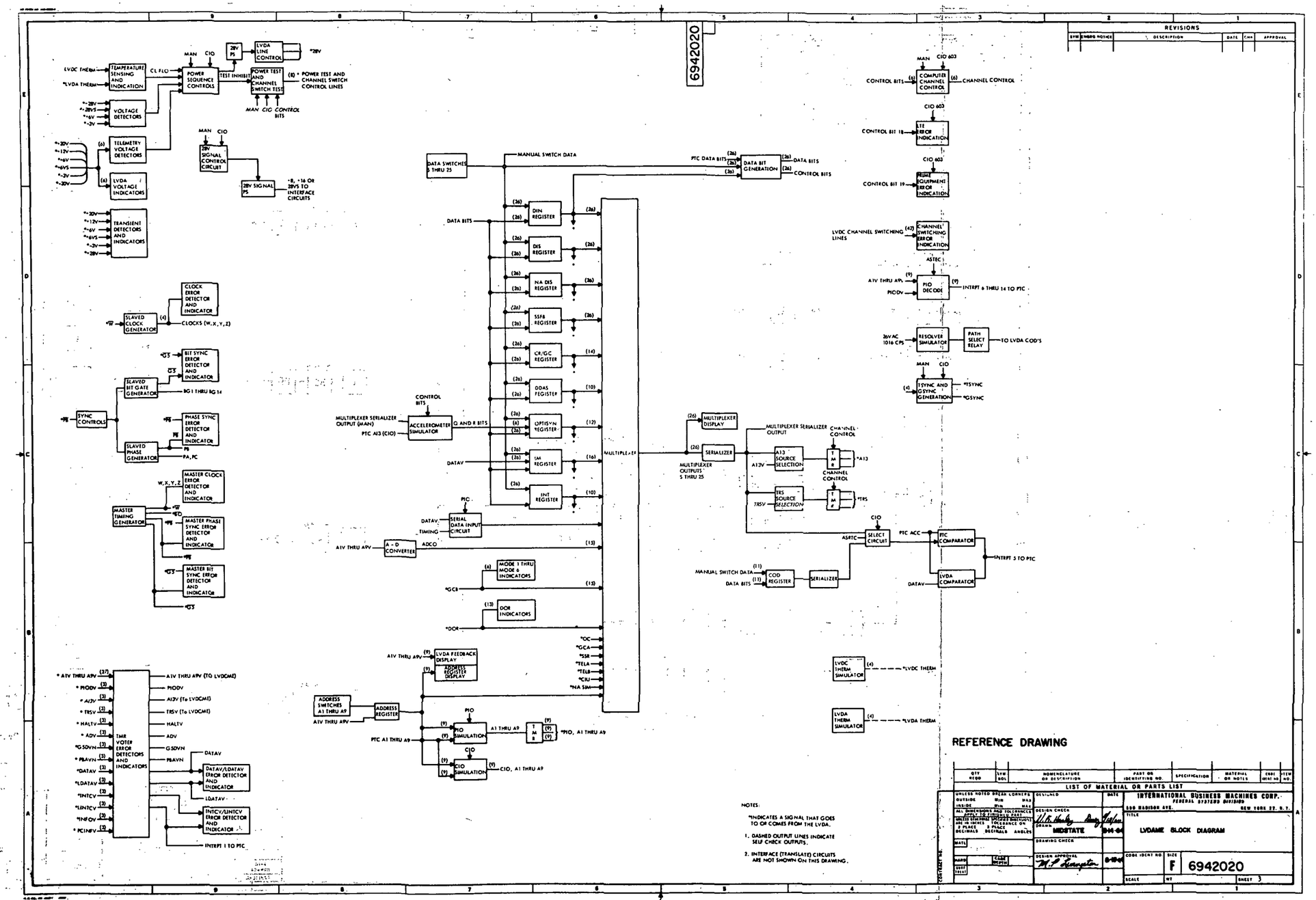


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 3)

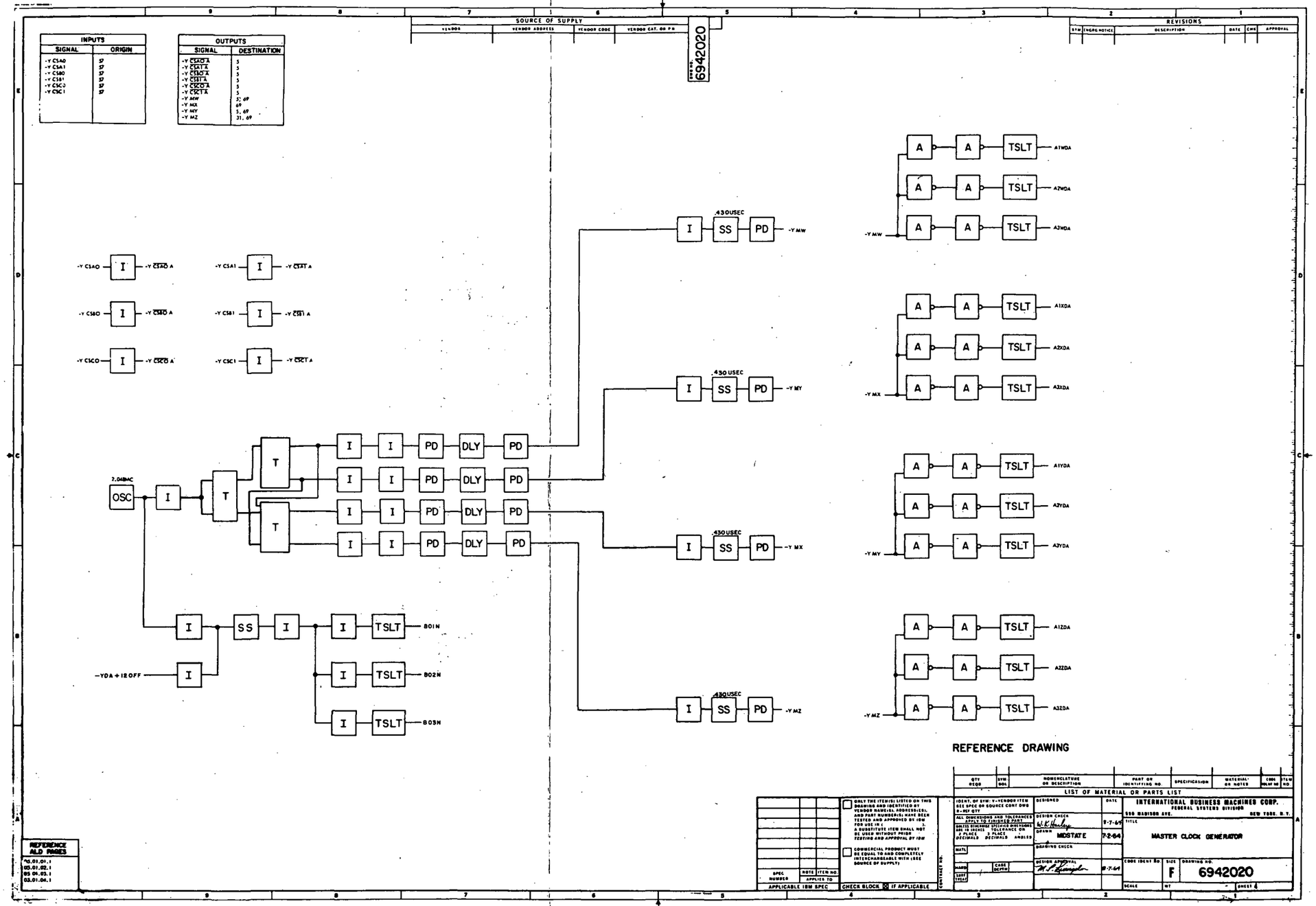
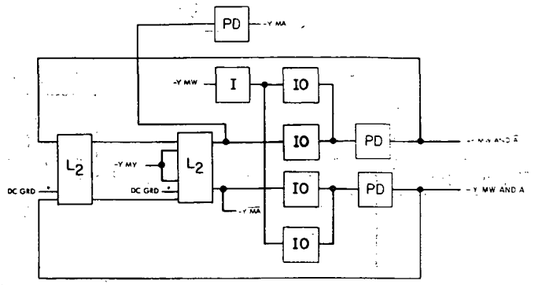
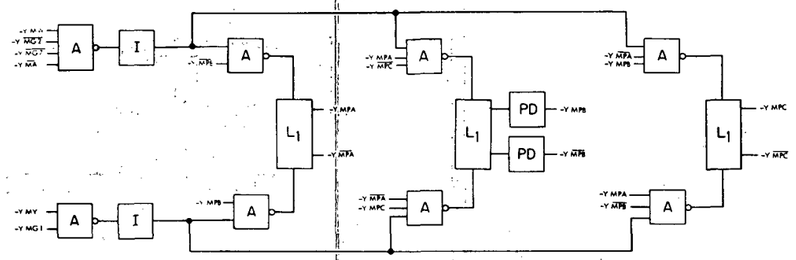


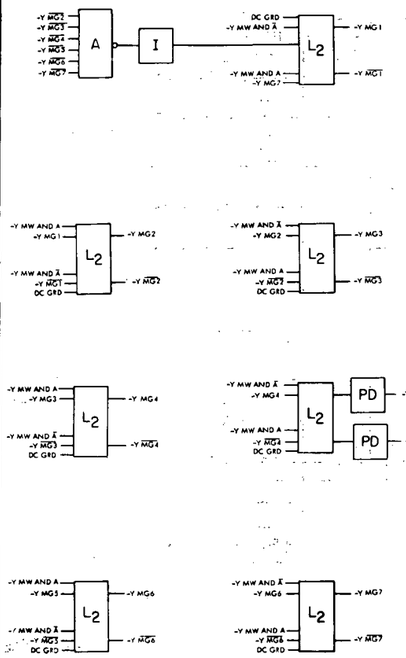
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 4)

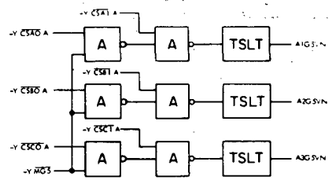
INPUTS	
SIGNAL	ORIGIN
-Y $\overline{CSAD}$ A	4
-Y $\overline{CSAT}$ A	4
-Y $\overline{CSBD}$ A	4
-Y $\overline{CSBT}$ A	4
-Y $\overline{CSCD}$ A	4
-Y $\overline{CSCT}$ A	4
-Y MW	4
-Y MY	4

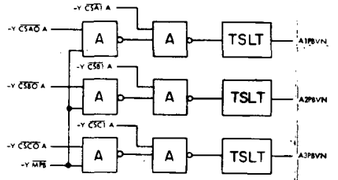
OUTPUTS	
SIGNAL	DESTINATION
-Y $\overline{MG5}$	31
-Y $\overline{MG5}$	31
-Y $\overline{MP8}$	31
-Y $\overline{MP8}$	31

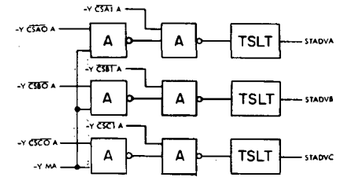












REFERENCE ALD PAGES
05.01.05.1
05.01.06.1
05.01.07.1
05.01.08.1
05.01.09.1

REFERENCE DRAWING

SPEC NUMBER	NOTE ITEM NO APPLIES TO
APPLICABLE IBM SPEC	

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S), HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN (A) SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY).

CHECK BLOCK ☒ IF APPLICABLE

QTY REQD	SYM NO.	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO	SPECIFICATION	MATERIAL OR NOTE	USE ON NEXT ASSY	ITEM NO

LIST OF MATERIAL OR PARTS LIST

IDENT. OF SYM. V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG B-NOT QTY

ALL DIMENSIONS AND TOLERANCES APPLY AFTER PLATING AND FINISHING

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± .01 3 PLACE DECIMALS ± .005 ANGLES ± 1°

MATL

HARD

SURF TREAT

CONTRACT NO.

	DATE
DESIGNED	
DESIGN CHECK	9-7-64
DRAWN MIDSTATE	7-2-64
DRAWING CHECK	
DESIGN APPROVAL	9-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
580 MADISON AVE. NEW YORK, N.Y.

TITLE
MASTER BIT COUNTER AND MASTER PHASE COUNTER

CODE IDENT NO | SIZE F | DRAWING NO 6942020

SCALE | WT | SHEET 5

SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT OR P.N.

DRAWING 6942020

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 5)

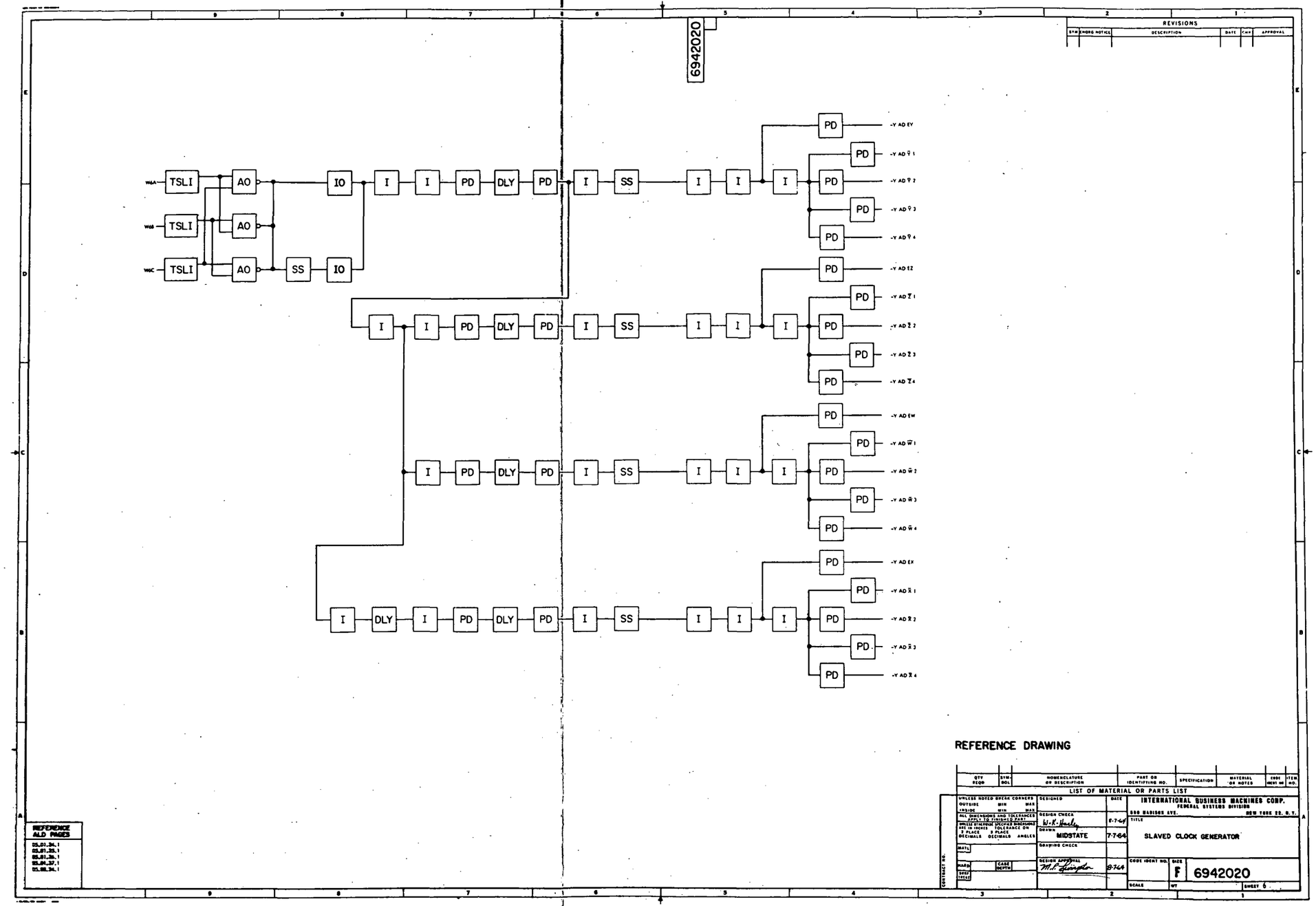


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 6)

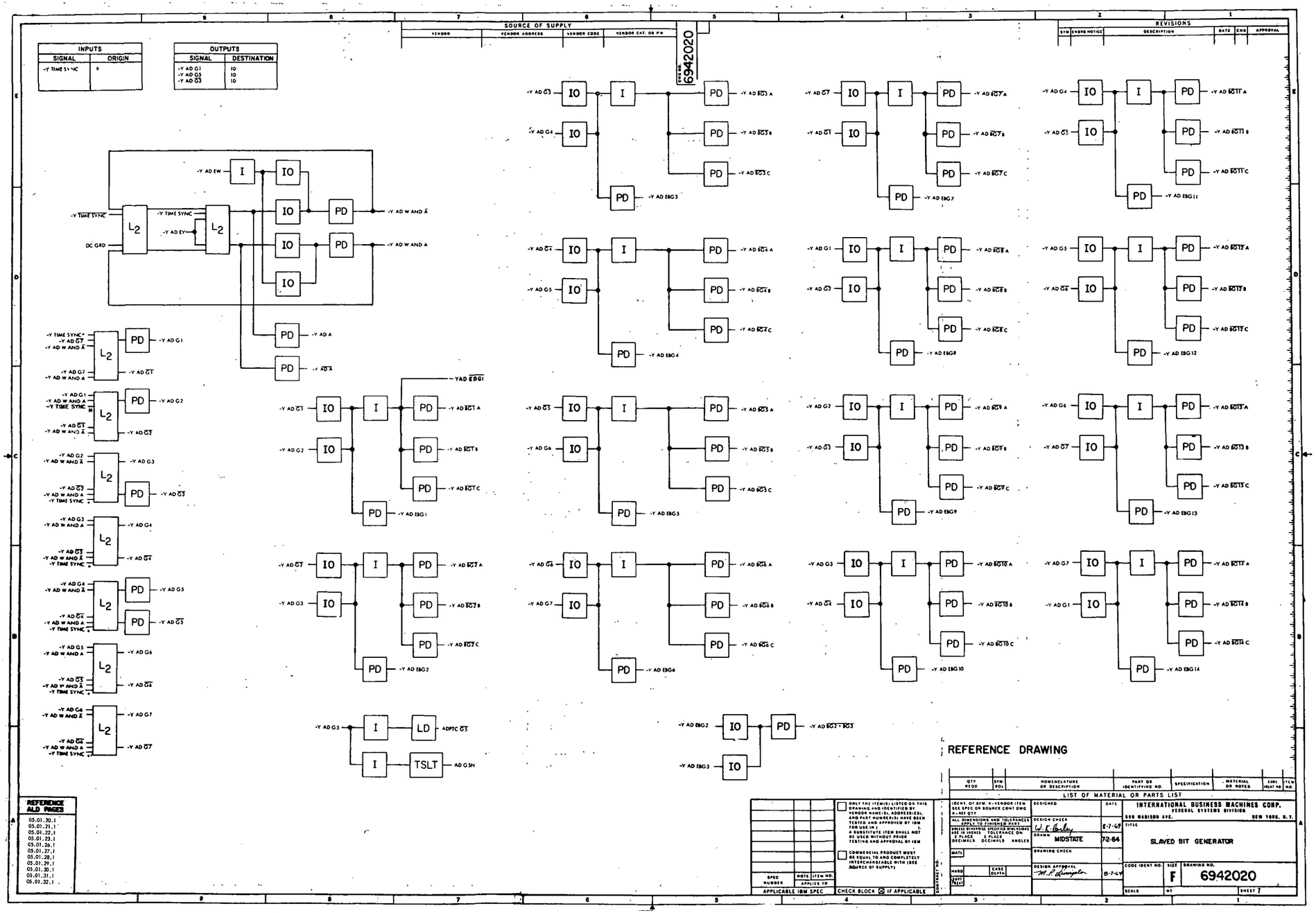


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 7)

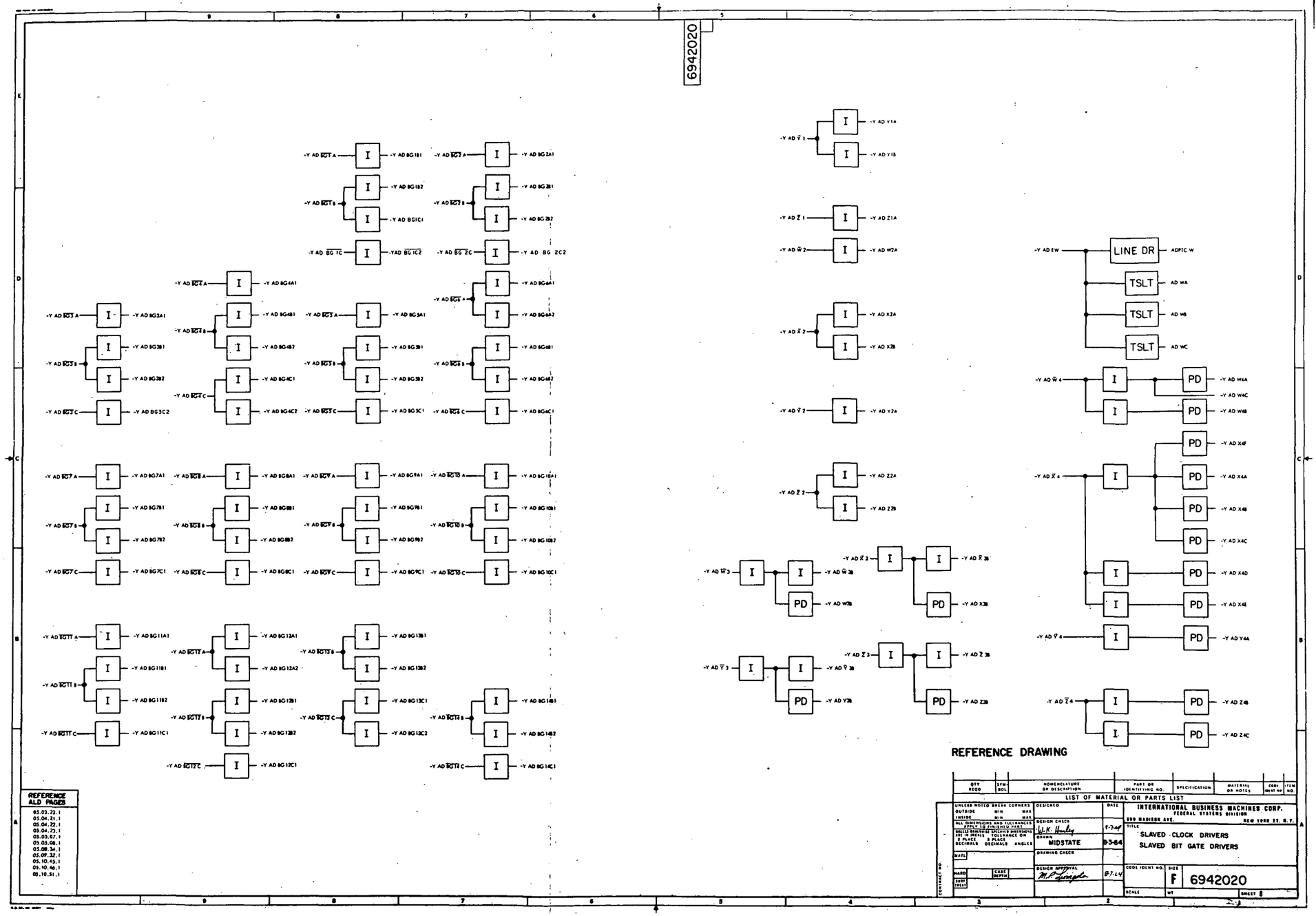


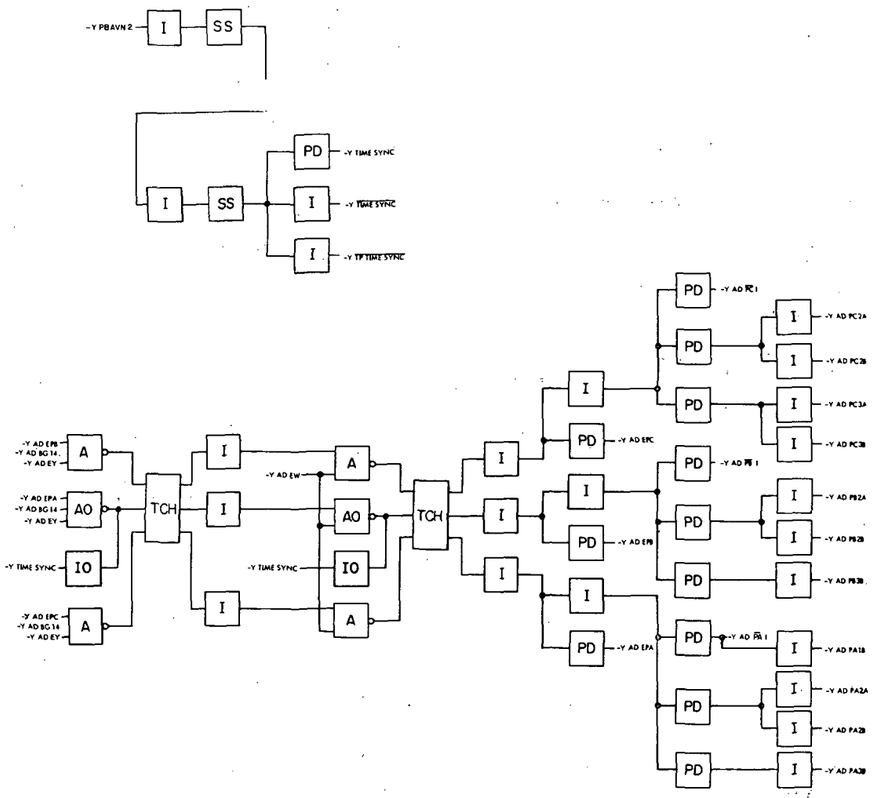
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 8)

INPUTS	
SIGNAL	ORIGIN
-Y PBAVN 2	20

OUTPUTS	
SIGNAL	DESTINATION
-Y TIME SYNC	7

6942020

REVISIONS				
SYM	NCRC NOTICE	DESCRIPTION	DATE	CHK APPROVAL



REFERENCE ALD PAGES
05.01.24.1
05.01.25.1
05.03.22.1
05.04.22.1
05.10.43.1
05.10.51.1

REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE .MIN .MAX INSIDE .MIN .MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON: 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
FINISH CASE DEPTH
DEPT ISSUE

		DATE
DESIGNED		
DESIGN CHECK	W. E. Hurley	7-7-64
DRAWN	MIDSTATE	8-3-64
DRAWING CHECK		
DESIGN APPROVAL	W. A. Livingston	8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
SLAVED PHASE GENERATOR AND DRIVERS

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 9

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 9)

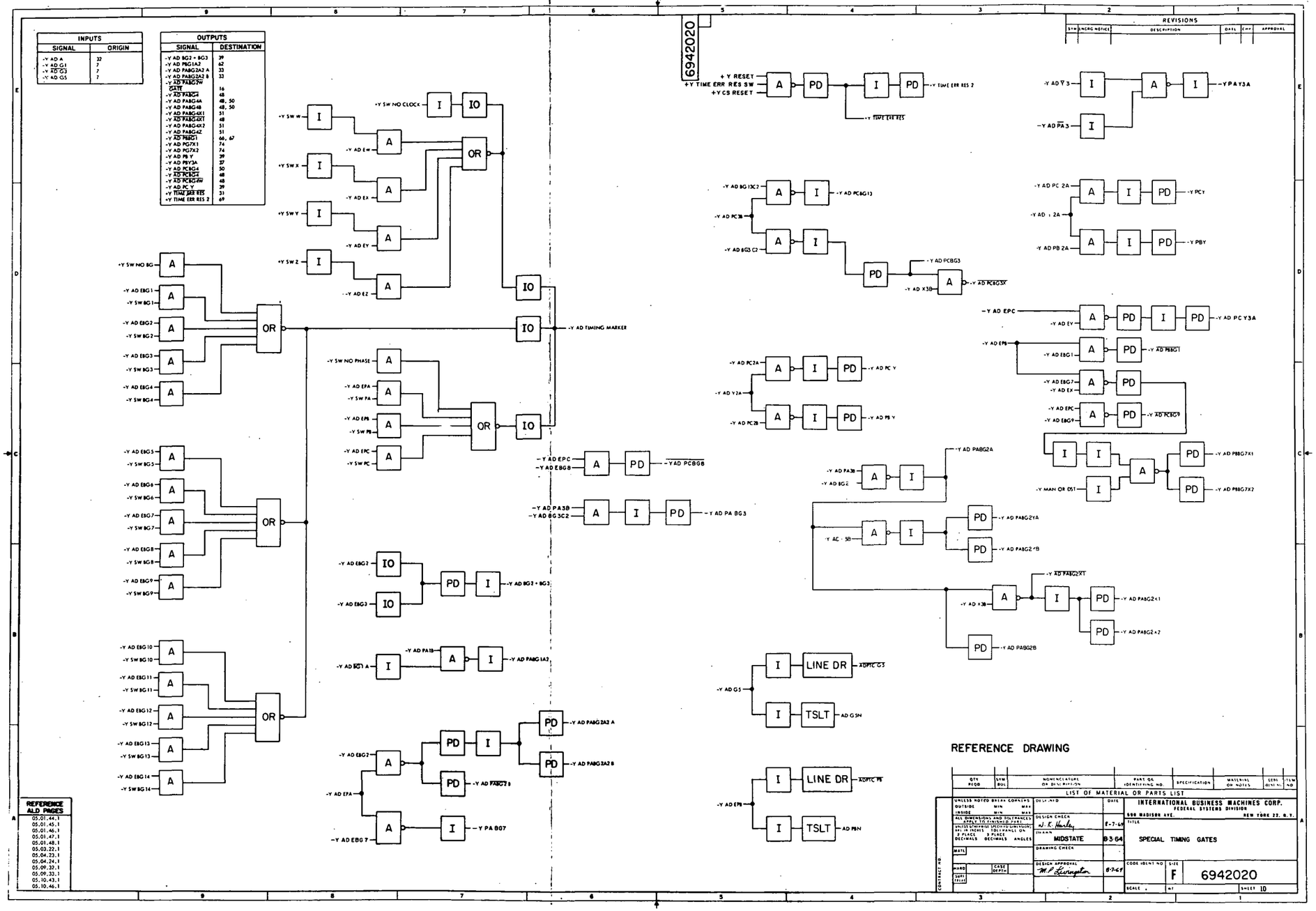


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 10)

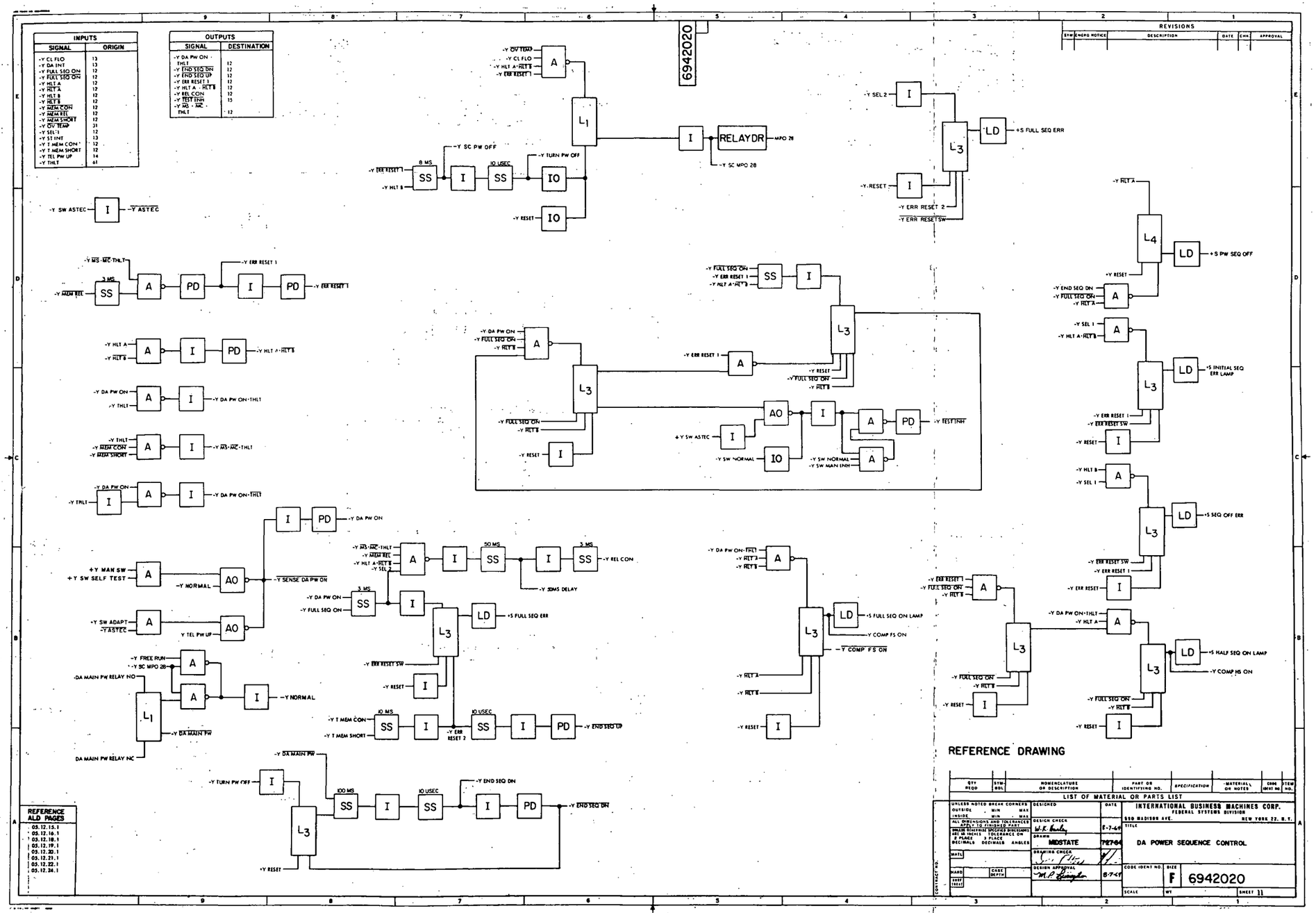


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 11)

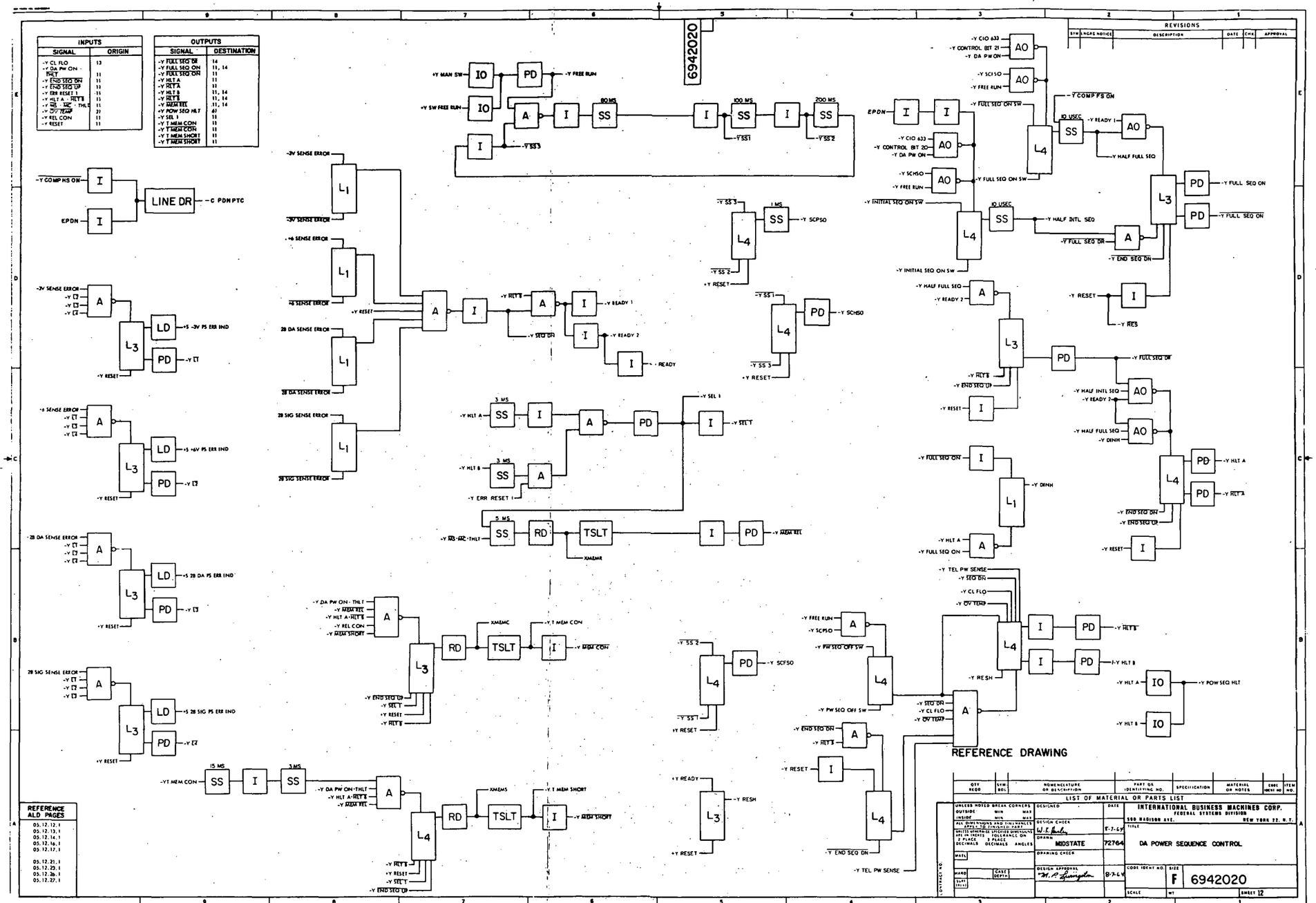


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 12)

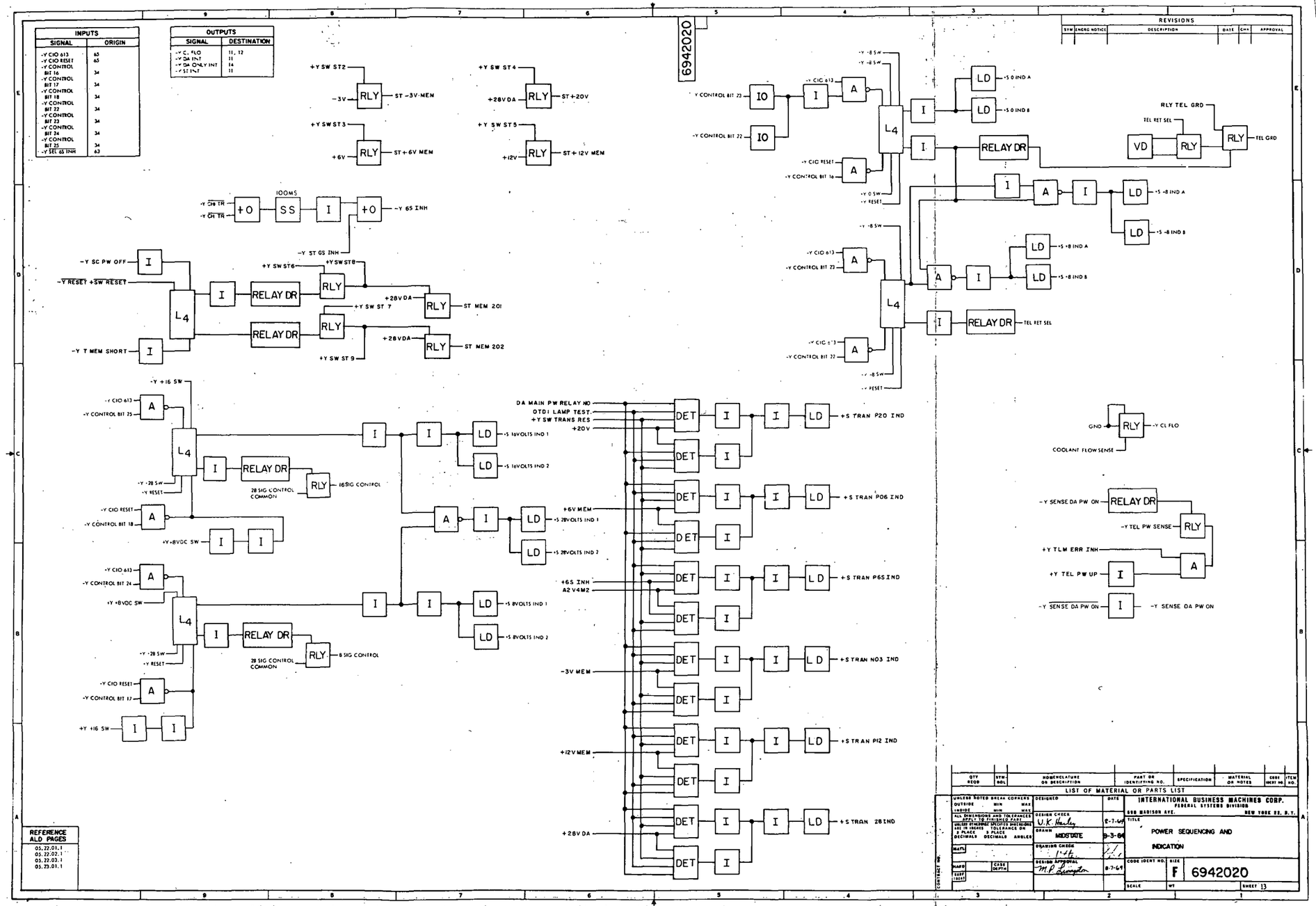


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 13)

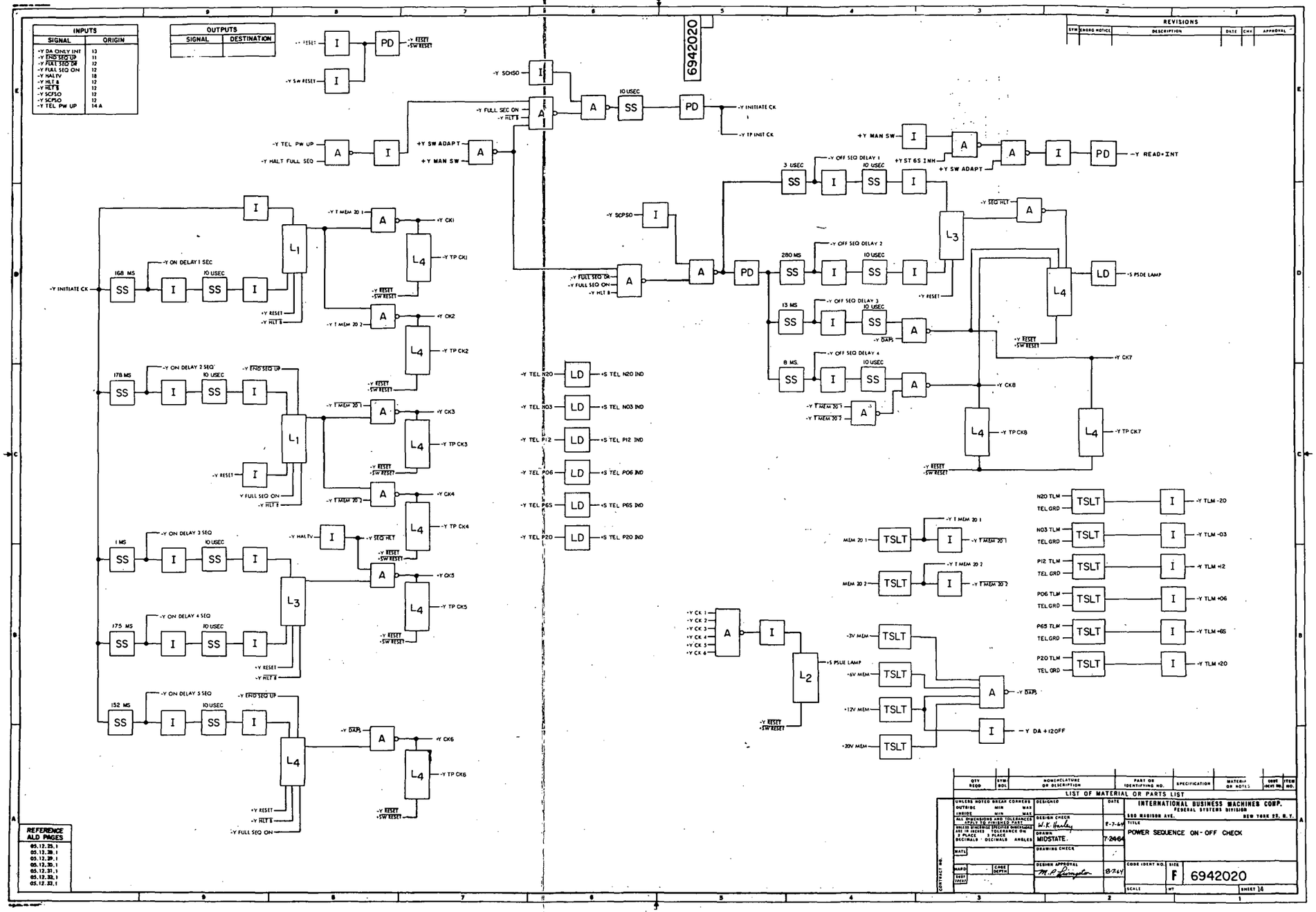


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 14)

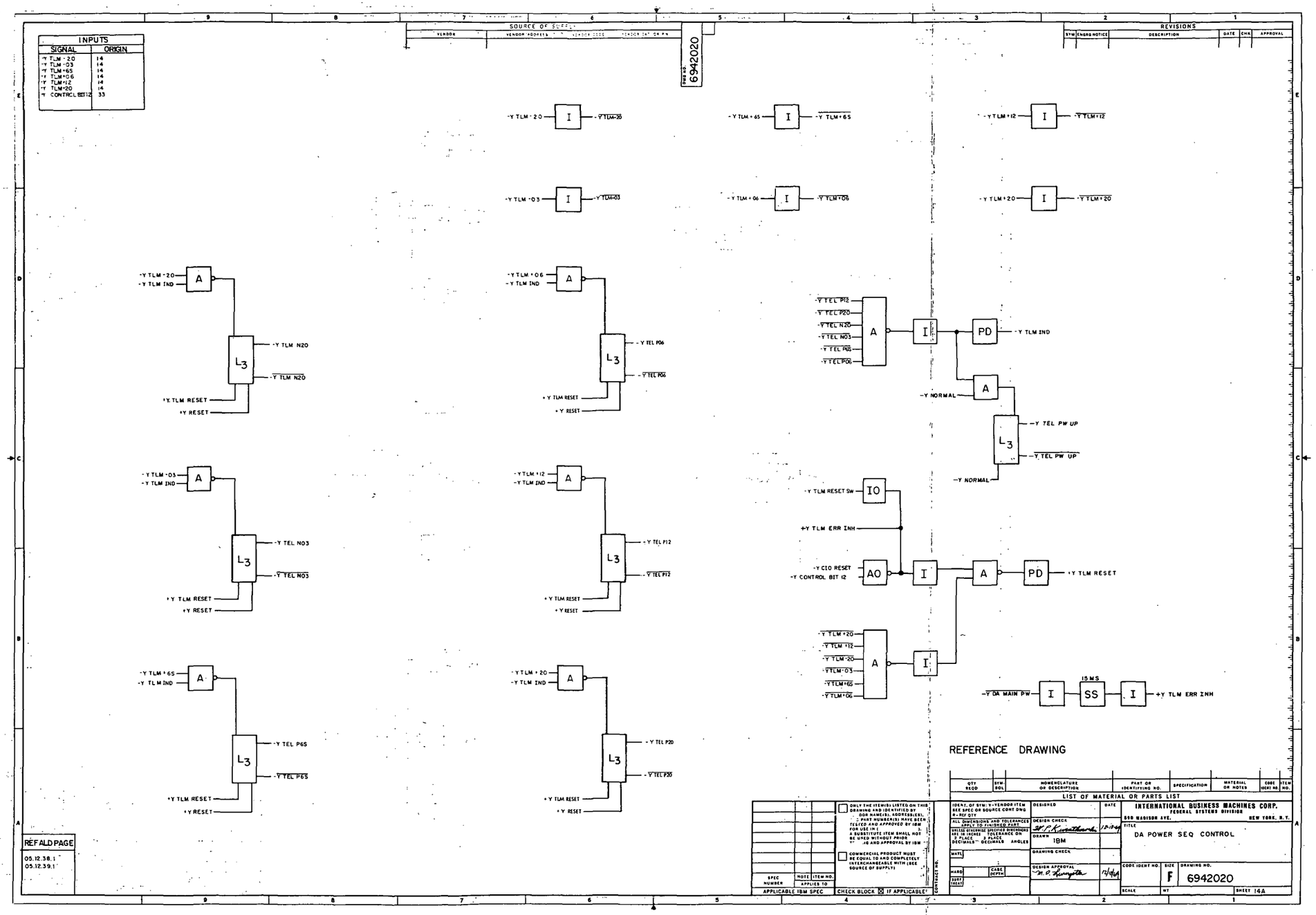


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 15)

SIGNAL	DESIGN
-Y CIO 613	65
-Y CONTROL BIT 11	33
-Y DIN 01	38
-Y DIN 2A	38
-Y DIN 2B	38
-Y DIN 03	38
-Y DIN 04	38
-Y DIN 05	38
-Y DIN 06	38
-Y DIN 07	38
-Y DIN 08	38
-Y DIN 09	38
-Y DIN 10	38

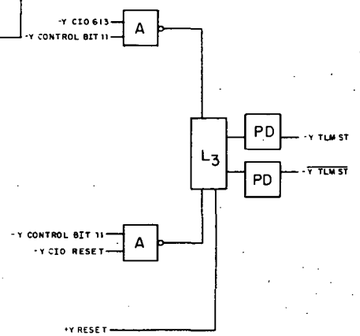
SOURCE OF SUPPLY

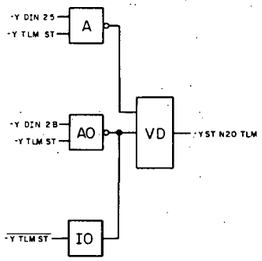
VENDOR ADDRESS	VENDOR ITEM	VENDOR PART NUMBER

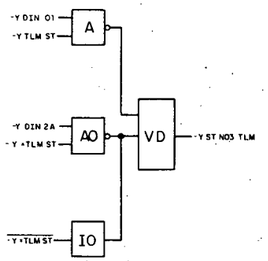
6942020

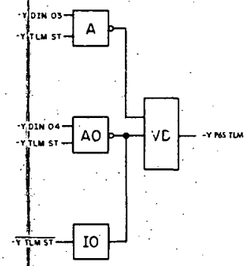
REVISIONS

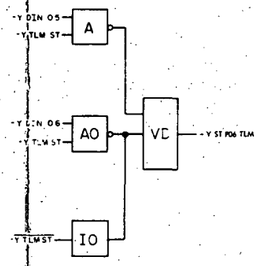
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

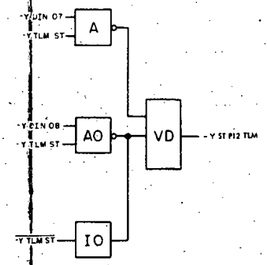


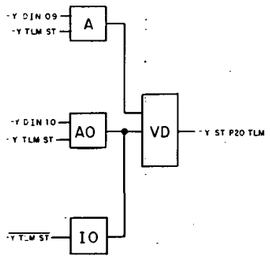












REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE SHEET NO.	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG R-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± .01 3 PLACE DECIMALS ± .005 ANGLES ±

MATL

HARD SURF TREAT CASE DEPTH

ONLY THE ITEMS LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN [ ]. A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

SYM | NOTE REMARKS | APPLIES TO

APPLICABLE IBM SPEC

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

DESIGNED | DATE

DESIGN CHECK

DRAWN IBM

DRAWING CHECK

DESIGN APPROVAL M D Livingston 12-6-68

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE
DA POWER SEQ CONTROL

CODE IDENT NO. | SIZE F | DRAWING NO. 6942020

SCALE | WT | SHEET 148

REFALD PAGE
05.13.05.1

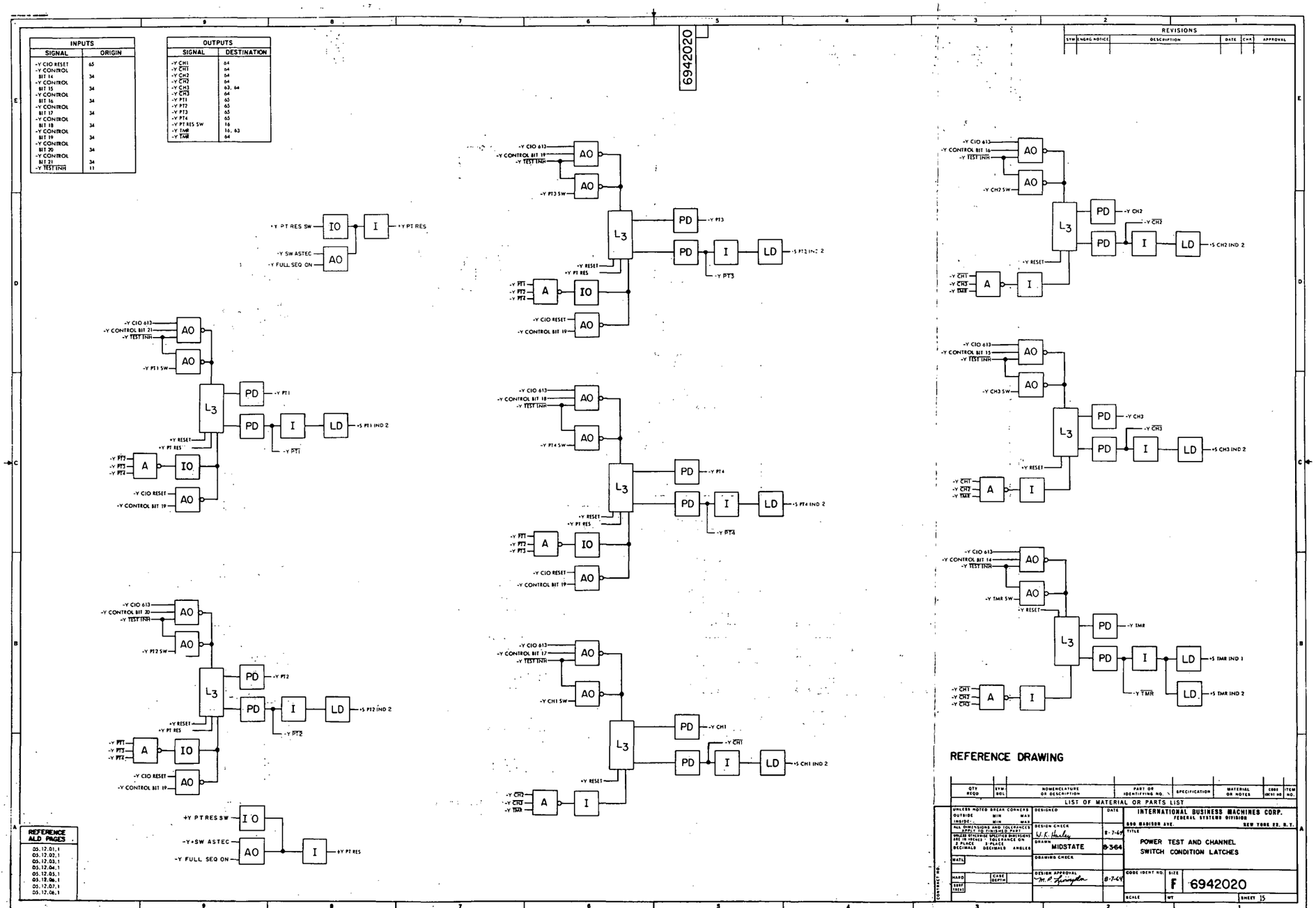
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 16)

INPUTS	
SIGNAL	ORIGIN
-Y CIO RESET	65
-Y CONTROL BIT 14	34
-Y CONTROL BIT 15	34
-Y CONTROL BIT 16	34
-Y CONTROL BIT 17	34
-Y CONTROL BIT 18	34
-Y CONTROL BIT 19	34
-Y CONTROL BIT 20	34
-Y CONTROL BIT 21	34
-Y TEST INH	11

OUTPUTS	
SIGNAL	DESTINATION
-Y CH1	64
-Y CH1	64
-Y CH2	64
-Y CH2	64
-Y CH3	63, 64
-Y CH3	64
-Y PT1	65
-Y PT2	65
-Y PT3	65
-Y PT4	65
-Y PT RES SW	16
-Y TMR	16, 63
-Y TMR	64

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL



REFERENCE ALD PAGES
05.12.01.1
05.12.02.1
05.12.03.1
05.12.04.1
05.12.05.1
05.12.06.1
05.12.07.1
05.12.08.1

REFERENCE DRAWING

QTY REQD	SYM SEL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES · TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
HARD CASE DEPTH
HEAT TREAT

DESIGNED — DATE
DESIGN CHECK — W.K. Hurley — 8-7-64
DRAWN — MIDSTATE — 8364
DRAWING CHECK
DESIGN APPROVAL — M.P. Livingston — 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
POWER TEST AND CHANNEL SWITCH CONDITION LATCHES

CONTRACT NO.
CODE IDENT NO. 6942020 — SIZE F
SCALE — WT — SHEET 15

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 17)

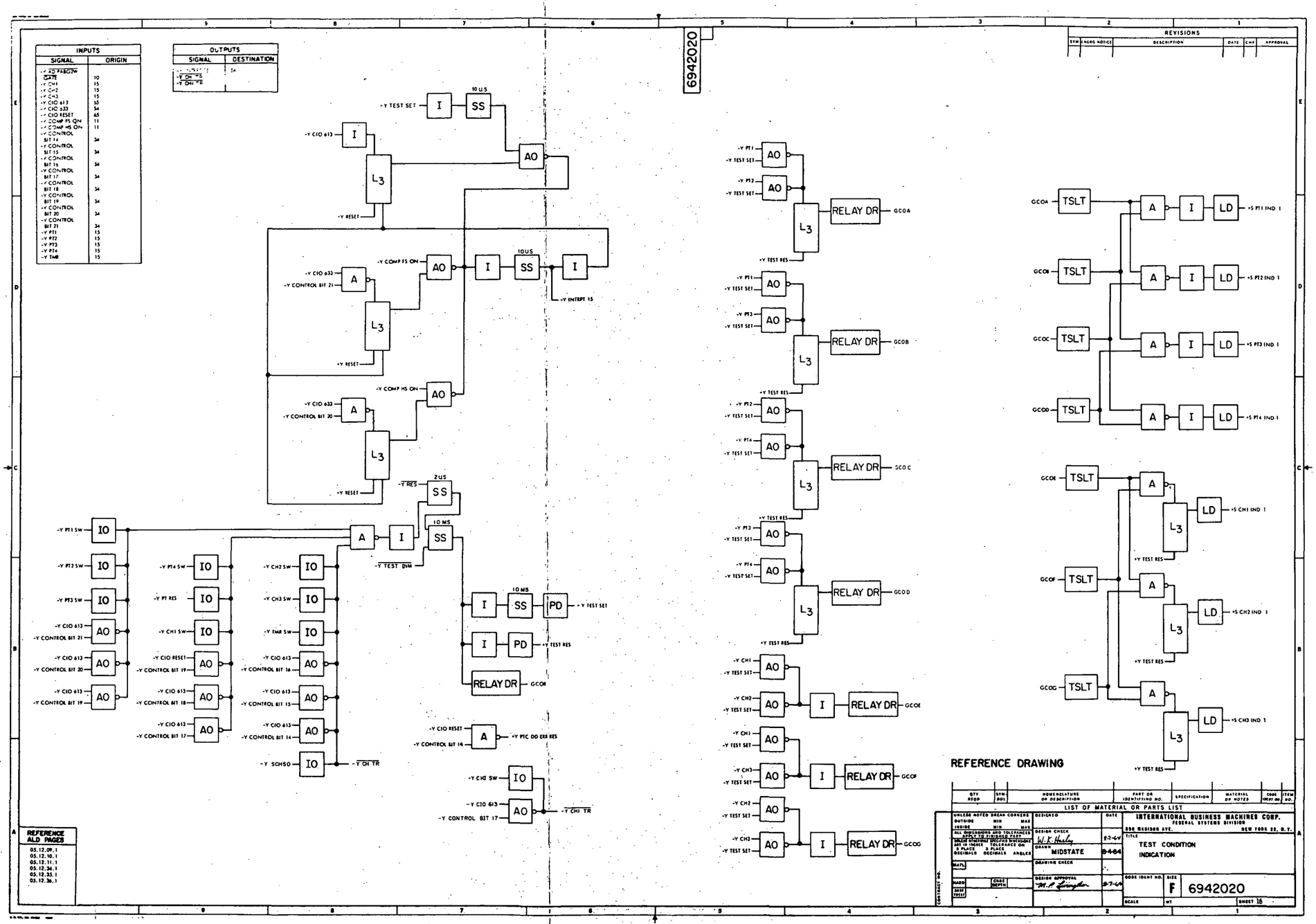


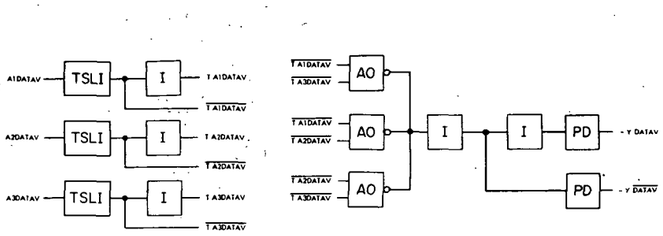
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 18)

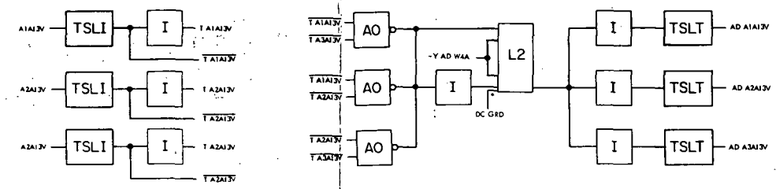
INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RES 3A	31

OUTPUTS	
SIGNAL	DESTINATION
-Y DATAV -Y DATAV	21, 29 29

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHG	APPROVAL





REFERENCE ALD PAGES

05.08.01.1
05.08.02.1
05.08.33.1
05.08.36.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED — DATE
DESIGN CHECK W.J. K Hurley — 6-7-64
DRAWN MIDSTATE — 6-30-64
DRAWING CHECK — 7-1-64
DESIGN APPROVAL M. P. Livingston — 8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
ERROR DETECTOR AND VOTER
DATAV-A13V

CODE IDENT NO. | SIZE F | 6942020

SCALE | WT | SHEET 17

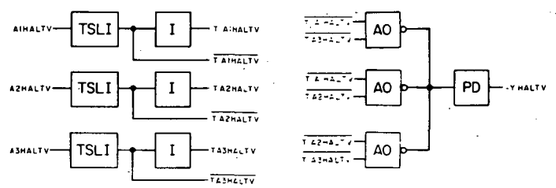
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 19)

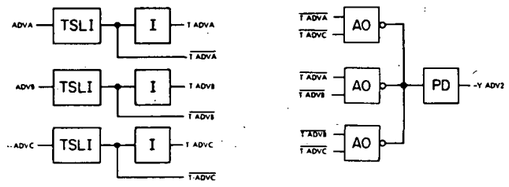
INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RES 1	31
-Y DD ERR RES 48	31
-Y HALTV TEST ON	61
-Y HALTV TEST OFF	61

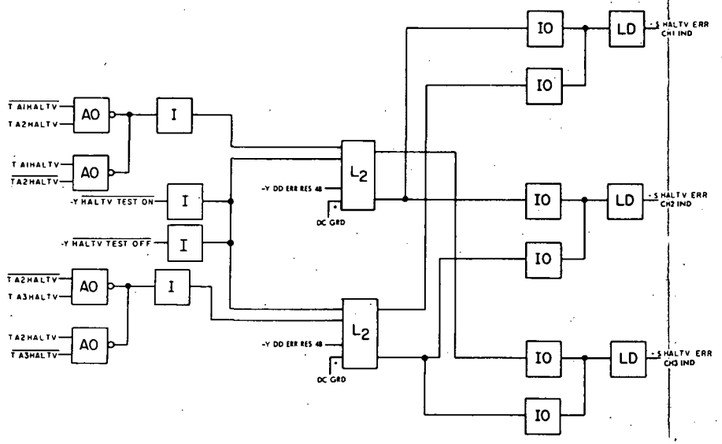
OUTPUTS	
SIGNAL	DESTINATION
-Y ADV ERR CHA	31
-Y ADV ERR CHB	31
-Y AD V2	32
-Y HALTV	31

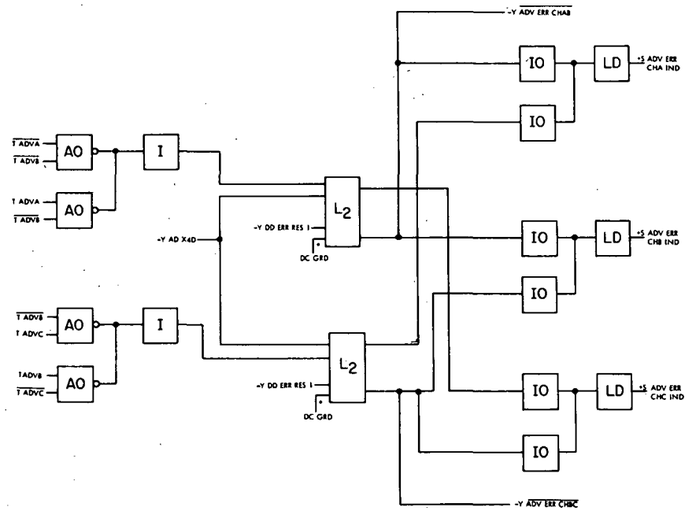
6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL









REFERENCE ALD PAGES

05.00.27.1
05.30.76.1
05.30.49.2
05.30.X.1

REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED MACHINING TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD / SOFT — CASE DEPTH

	NAME	DATE
DESIGNED		
DESIGN CHECK	W. K. Hurley	8-7-64
DRAWN	MIDSTATE	8-30-64
DRAWING CHECK		
DESIGN APPROVAL	M. P. Langdon	9-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
ERROR DETECTOR AND VOTER
HALTV – ADV

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 18

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 20)

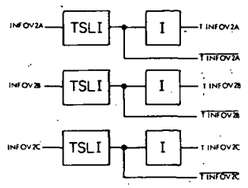
INPUTS	
SIGNAL	ORIGIN
-Y DO ERR RESET 2B	2'

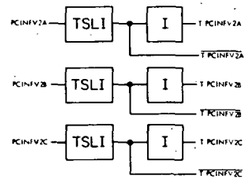
OUTPUTS	
SIGNAL	DESTINATION

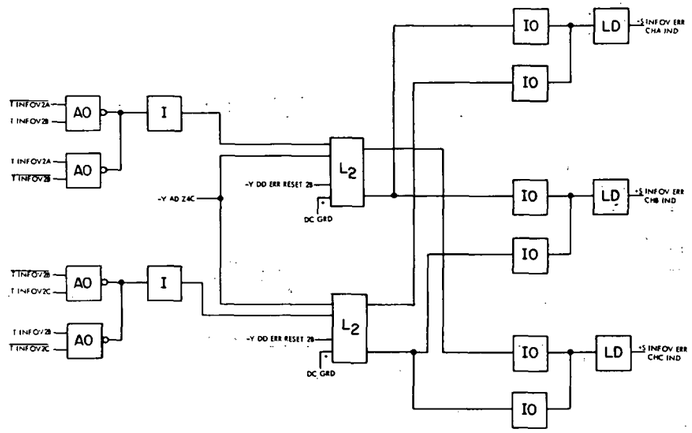
6942020

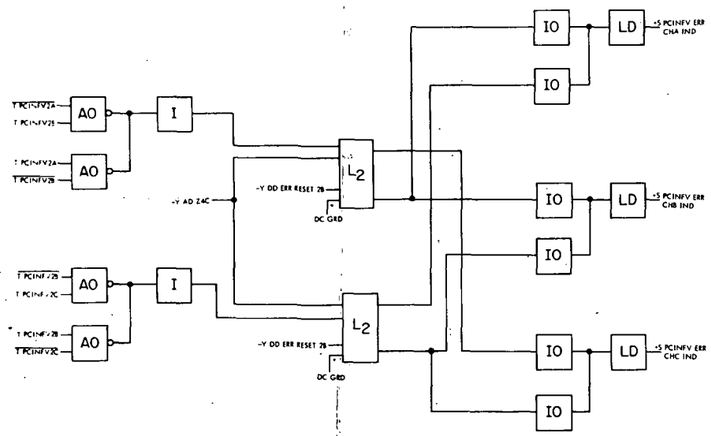
REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL









REFERENCE ALD PAGES
05.06.43.1
05.06.44.1
05.06.45.1
05.06.46.1

REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CAGE (MFG) NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX	DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 590 MADISON AVE. NEW YORK 22, N.Y.
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART	DESIGN CHECK W.K. Hurley	8-7-64	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES / TOLERANCE ON 2 PLACE DECIMALS / 3 PLACE DECIMALS / ANGLES	DRAWN MIDSTATE	53064	TITLE ERROR DETECTOR INFOV - PCINFV
MATL	DRAWING CHECK		
HARD / CASE DEPTH	DESIGN APPROVAL M.J. Livingston	8-7-64	CUDE IDENT NO. / SIZE F / 6942020
SHRT STEEL			SCALE / WT / SHEET 19

CONTRACT NO

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 21)

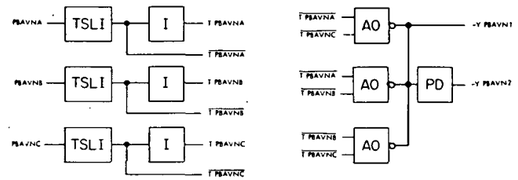
INPUTS	
SIGNAL	ORIGIN
-Y DO ERR RES 1	::

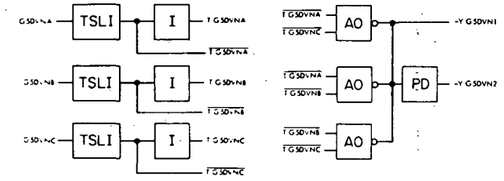
OUTPUTS	
SIGNAL	DESTINATION
-Y G5D-VN ERR CHA	31
-Y G5D-VN ERR CHB	31
-Y G5D-VN ERR CHC	31
-Y G5D-VN1	31
-Y G5D-VN2	32
-Y PBA-VN ERR CHA	31
-Y PBA-VN ERR CHB	31
-Y PBA-VN ERR CHC	31
-Y PBA-VN1	31
-Y PBA-VN2	9, 32

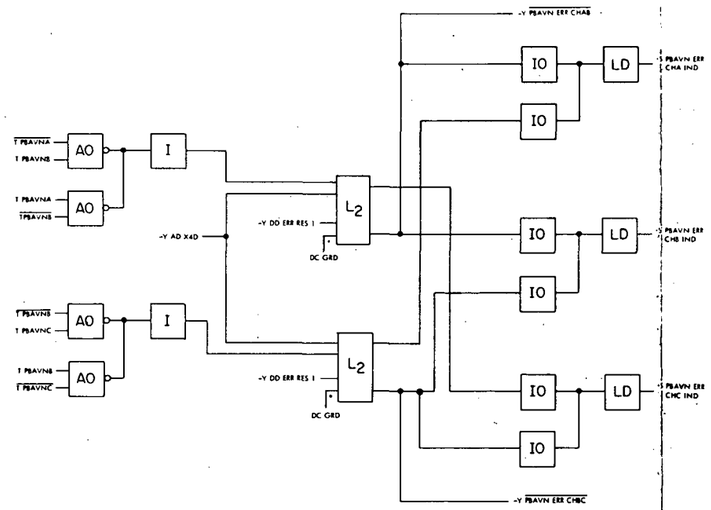
6942020

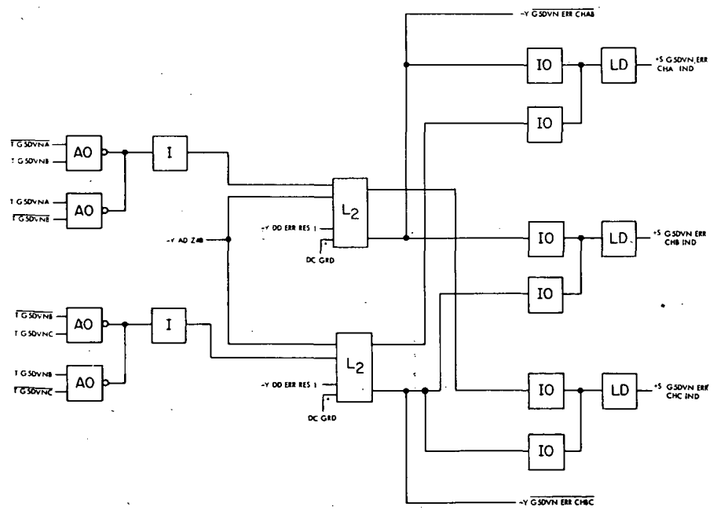
REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL









REFERENCE ALD PAGES
05.08.51.1
05.08.52.1
05.08.53.1
05.08.54.1

REFERENCE DRAWING

QTY REQD	SYM NO.	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK EDGES OUTSIDE MIN MAX INSIDE MIN MAX ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PARTS UNLESS OTHERWISE SPECIFIED DIMENSIONS AT PLATED OR FINISHED SURFACES APPLY AFTER PLATING DECIMALS FRACTIONS ANGLES MATL HARD CASE DEPTH SURF TREAT	DESIGNED	DATE
	DESIGN CHECK W. K. Hanley	8-7-69
	DRAWN MIDSTATE	6/30/69
	DRAWING CHECK	
	DESIGN APPROVAL M. P. Livingston	8-7-69

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N. Y.

TITLE
ERROR DETECTOR AND VOTER
PBAVN - G5DVN

CODE IDENT NO	SIZE	
	F	6942020
SCALE	WT	SHEET 20

CONTRACT NO

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 22)

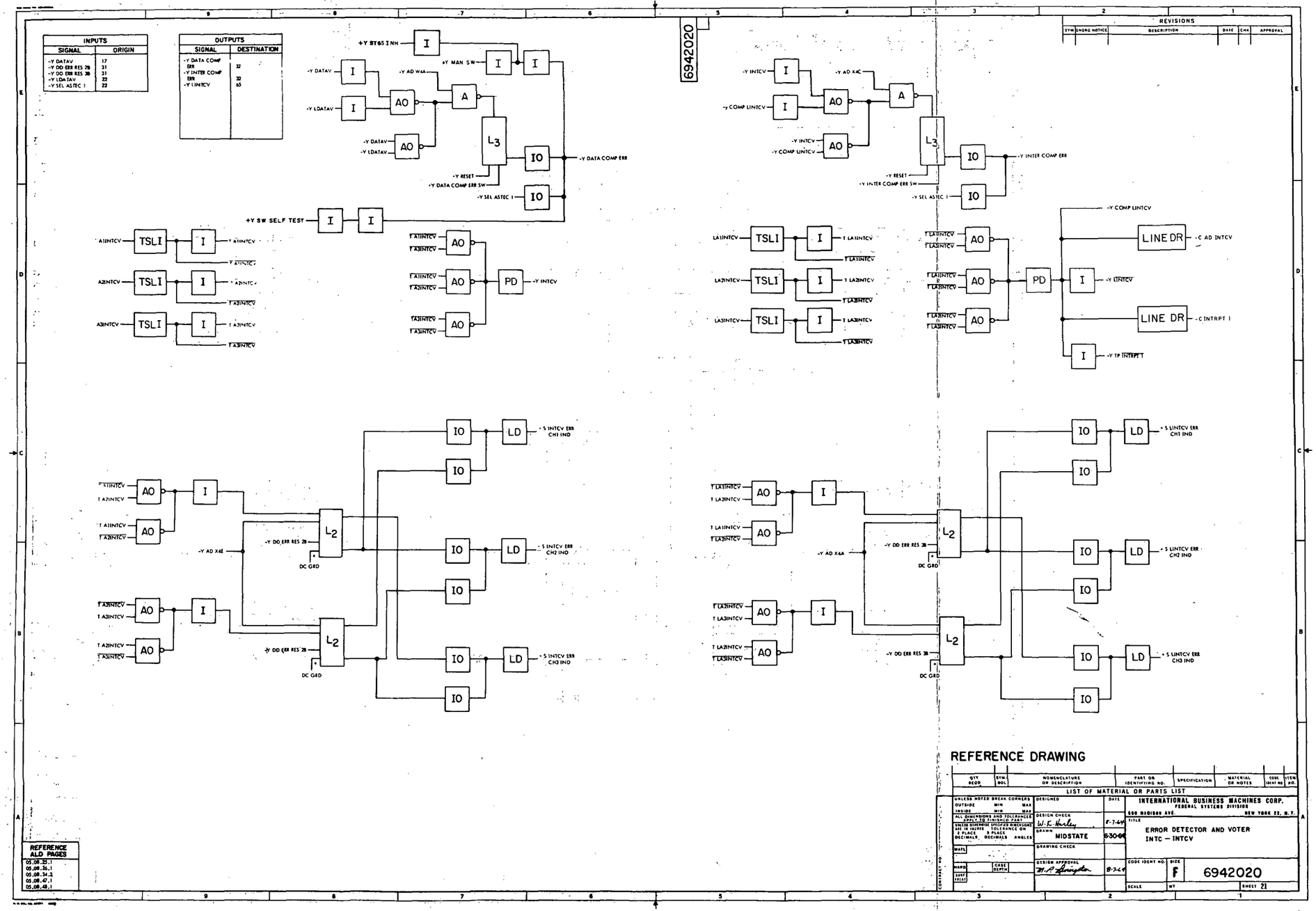


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 23)

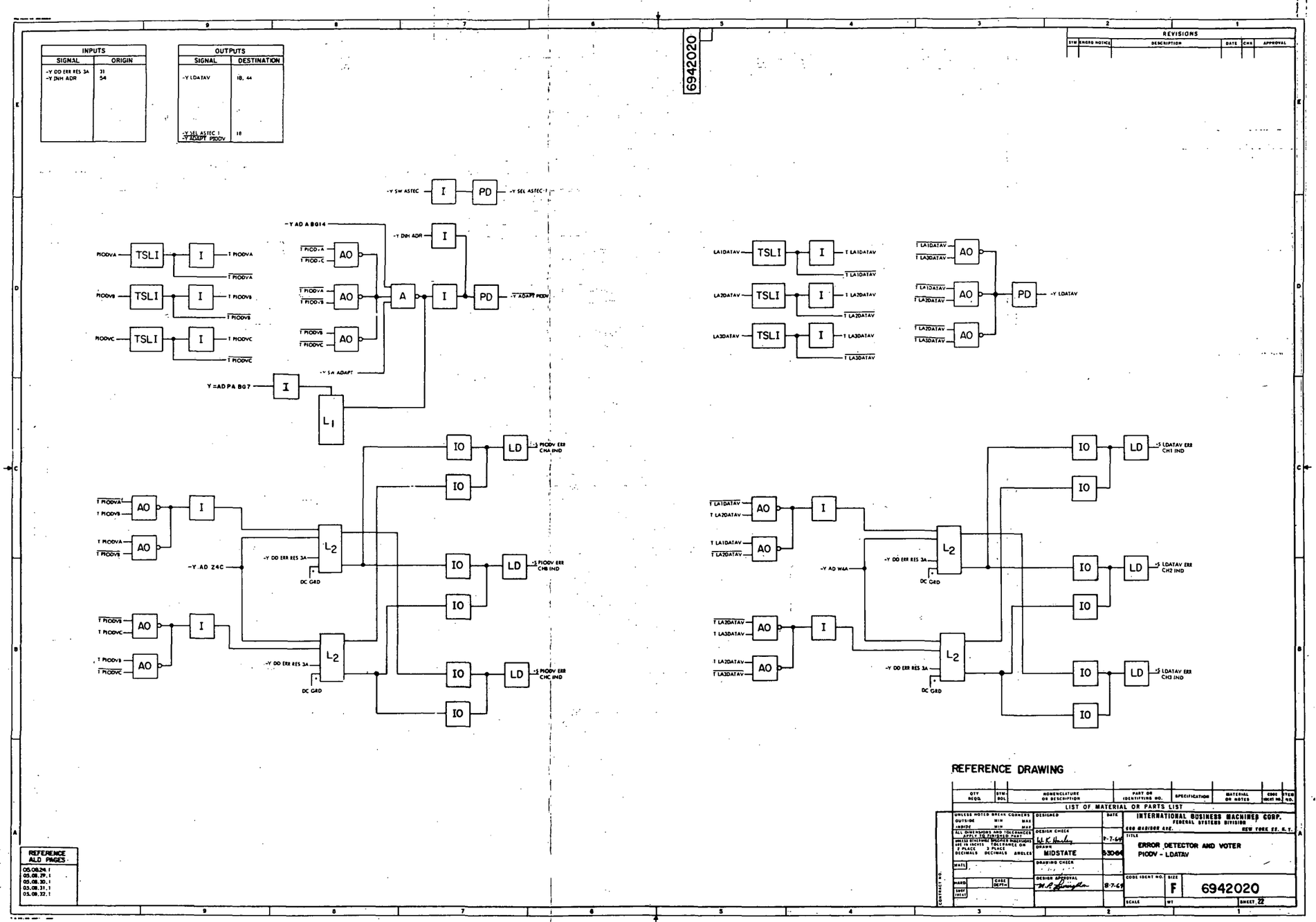


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 24)

INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RESET 2A	31

OUTPUTS	
SIGNAL	DESTINATION

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

DDSP1A — TSLI — I — T DDSP1A / T DDSP1A

DDSP1B — TSLI — I — T DDSP1B / T DDSP1B

DDSP1C — TSLI — I — T DDSP1C / T DDSP1C

DDSP2 A — TSLI — I — T DDSP2 A / T DDSP2 A

DDSP2 B — TSLI — I — T DDSP2 B / T DDSP2 B

DDSP2 C — TSLI — I — T DDSP2 C / T DDSP2 C

T DDSP1A, T DDSP1B — AO — I
T DDSP1A, T DDSP1B — AO — I
-Y AD Z4C
-Y DD ERR RESET 2A → L_2 → DC GRD

T DDSP1B, T DDSP1C — AO — I
T DDSP1B, T DDSP1C — AO — I
-Y DD ERR RESET 2A → L_2 → DC GRD

IO → LD → -S DDSP1 ERR CHA IND
IO
IO → LD → -S DDSP1 ERR CHB IND
IO
IO → LD → -S DDSP1 ERR CHC IND
IO

T DDSP2 A, T DDSP2 B — AO — I
T DDSP2 A, T DDSP2 B — AO — I
-Y AD Z4C
-Y DD ERR RESET 2A → L_2 → DC GRD

T DDSP2 B, T DDSP2 C — AO — I
T DDSP2 B, T DDSP2 C — AO — I
-Y DD ERR RESET 2A → L_2 → DC GRD

IO → LD → -S DDSP2 ERR CHA IND
IO
IO → LD → -S DDSP2 ERR CHB IND
IO
IO → LD → -S DDSP2 ERR CHC IND
IO

REFERENCE ALD PAGES
05.08.35.1
05.08.36.1
05.08.37.1
05.08.38.1

REFERENCE DRAWING

QTY REQD.	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (MAT NO)	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
HAND TEST
CASE DEPTH
CONTRACT NO

	DESIGNED	DATE
	DESIGN CHECK	
	W. K. Hanby	8-7-64
	DRAWN MIDSTATE	8-30-64
	DRAWING CHECK	
	DESIGN APPROVAL M. P. Enright	8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
ERROR DETECTOR
DDSP1 – DDSP2

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 23

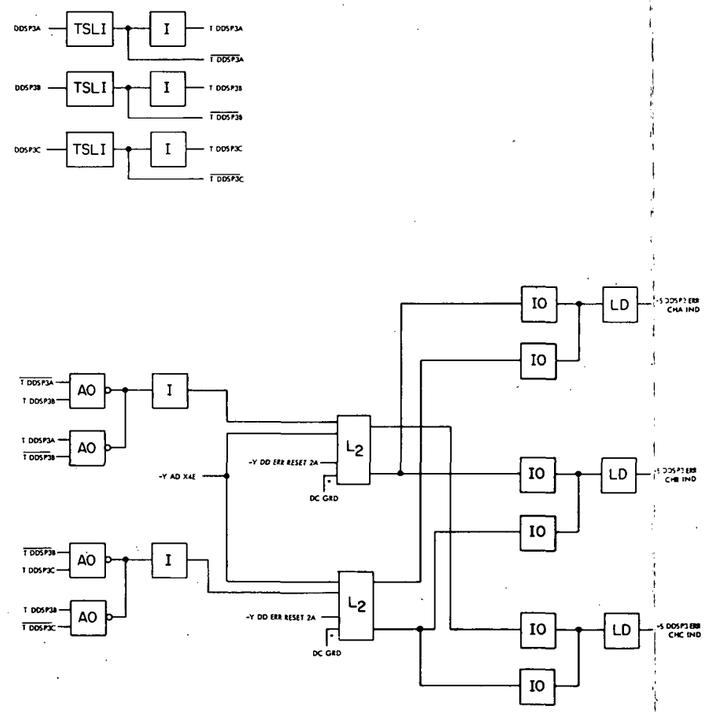
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 25)

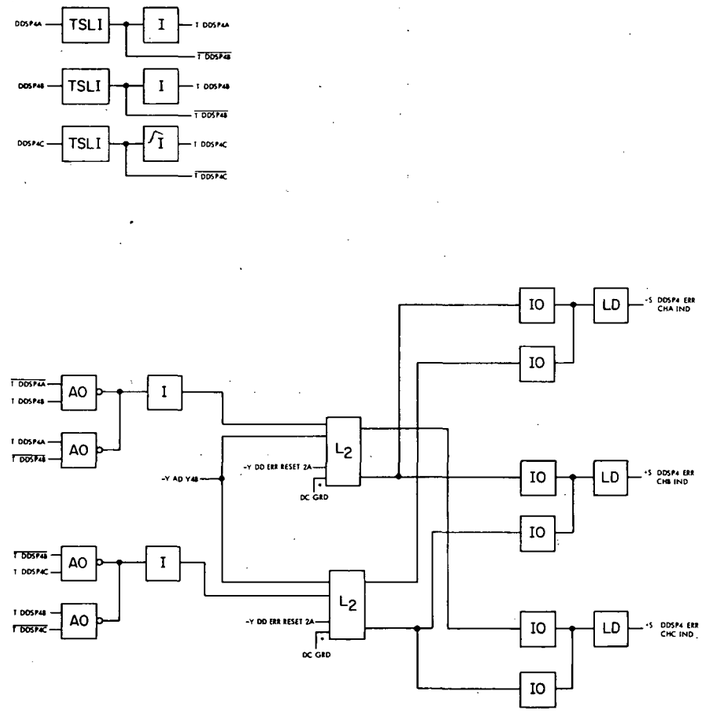
6942020

INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RESET 2A	31

OUTPUTS	
SIGNAL	DESTINATION

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL





REFERENCE ALD PAGES

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (MFGR NO.)	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX ALL DIMENSIONS AND TOLERANCES APPLY AFTER PLATING UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES MATL HARD SOFT CASE DEPTH

DESIGNED DATE
DESIGN CHECK 8-7-64
W.K. Hurley
DRAWN MIDSTATE 53064
DRAWING CHECK
DESIGN APPROVAL M.P. Smyth 8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
ERROR DETECTOR
DDSP3 - DDSP4

CODE IDENT NO. SIZE F 6942020
SCALE WT SHEET 26

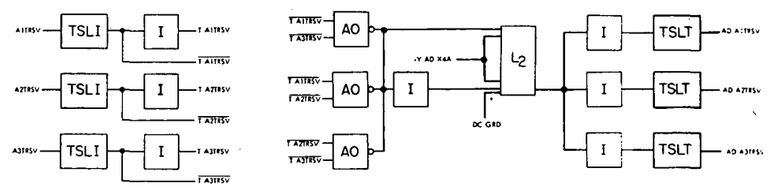
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 26)

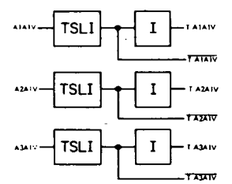
INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RES 3B	31

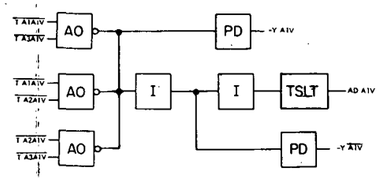
OUTPUTS	
SIGNAL	DESTINATION
-Y AIV	30,35
-Y $\overline{\text{AIV}}$	30,35

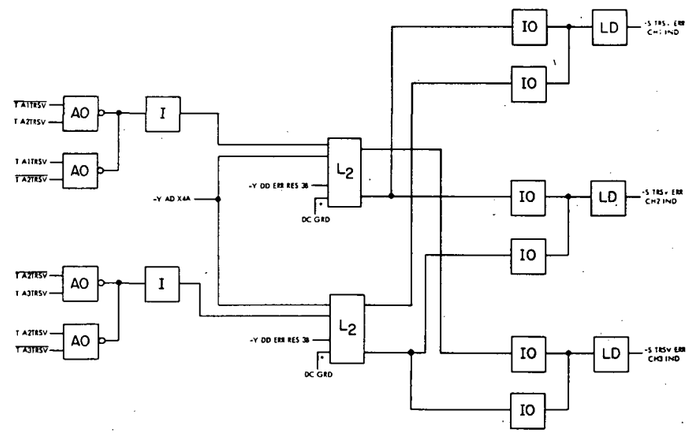
6942020

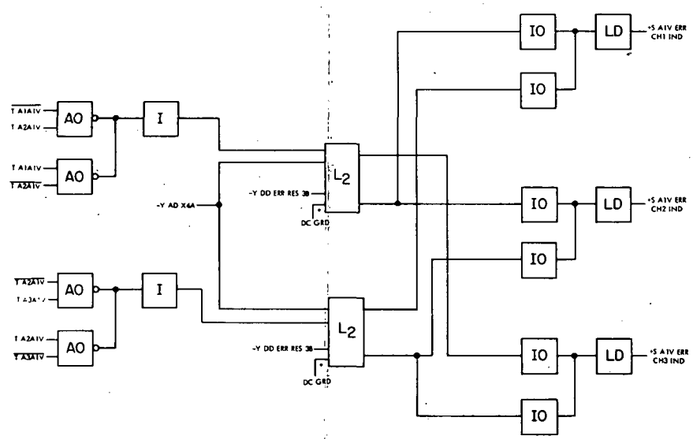
REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL











REFERENCE ALD PAGES
05.08.03.1
05.08.04.1
05.08.05.1
05.08.06.1

REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CAGE (HEAT NO)	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
BOARD / LAST ITEM USED — CAGE DEPTH

DESIGNED — DATE
DESIGN CHECK — U. K. Hanley — 8-7-64
DRAWN — MIDSTATE — 8-30-64
DRAWING CHECK
DESIGN APPROVAL — M. P. Livingston — 8-7-64

CONTRACT NO

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
ERROR DETECTOR AND VOTER
TROSV - AIV

CODE IDENT NO. — SIZE F — 6942020
SCALE — WT — SHEET 25

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 27)

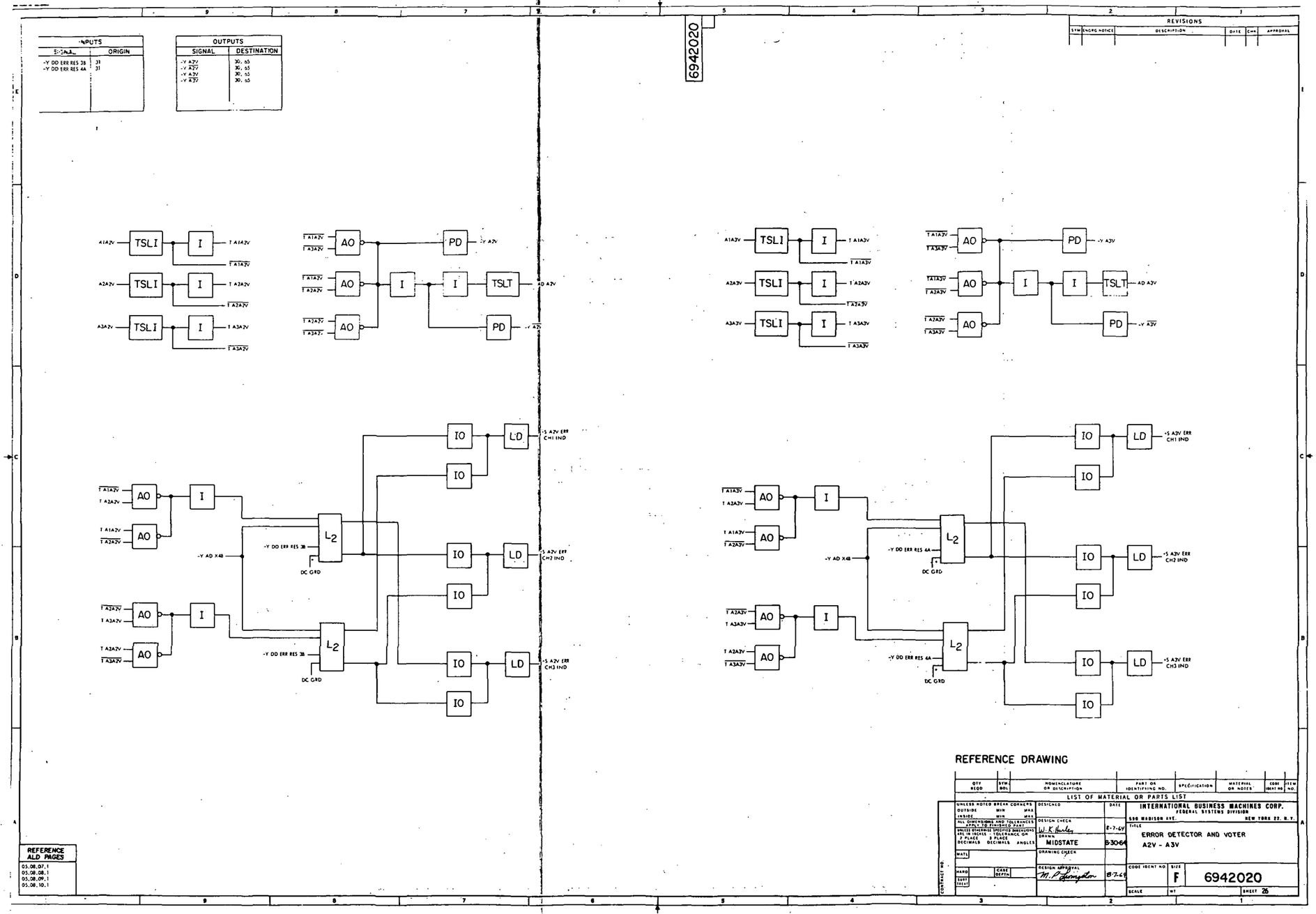


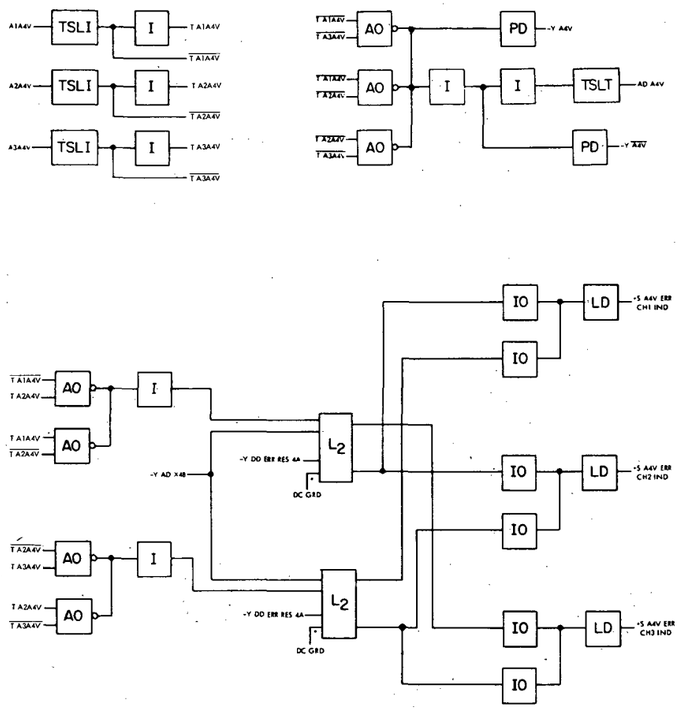
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 28)

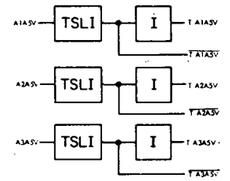
INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RES 4A	31

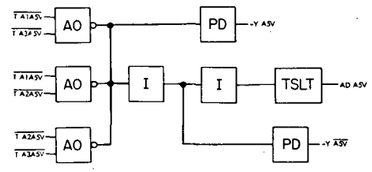
OUTPUTS	
SIGNAL	DESTINATION
-Y A4V	30, 65
-Y A4V	30, 65
-Y A5V	30, 65
-Y A5V	30, 65

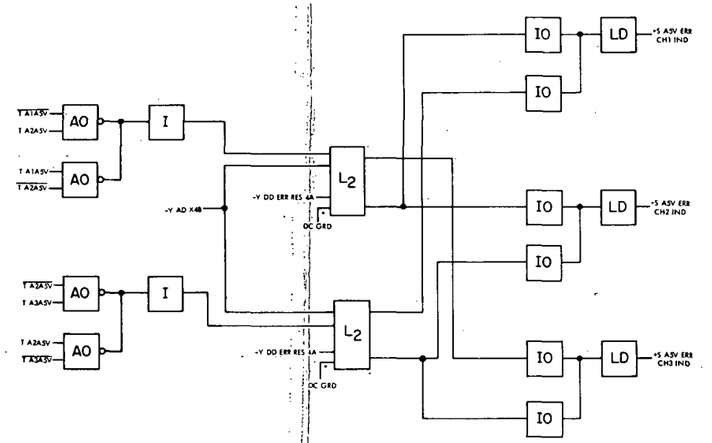
6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL









REFERENCE AID PAGES
05.08.11.1
05.08.12.1
05.08.13.1
05.08.14.1

REFERENCE DRAWING

QTY REQD	SYM SEL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PARTS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES 1 PLACE DECIMALS ± TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
TEST SPEC

	DESIGNED	DATE
DESIGN CHECK	W. K. Hawley	8-7-64
DRAWN	MIDSTATE	63066
DRAWING CHECK		
DESIGN APPROVAL	M. P. Livingston	8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N. Y.

TITLE
ERROR DETECTOR AND VOTER
A4V–A5V

CONTRACT NO.
CODE IDENT NO. 63066
SIZE F
6942020
SCALE WT
SHEET 27

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 29)

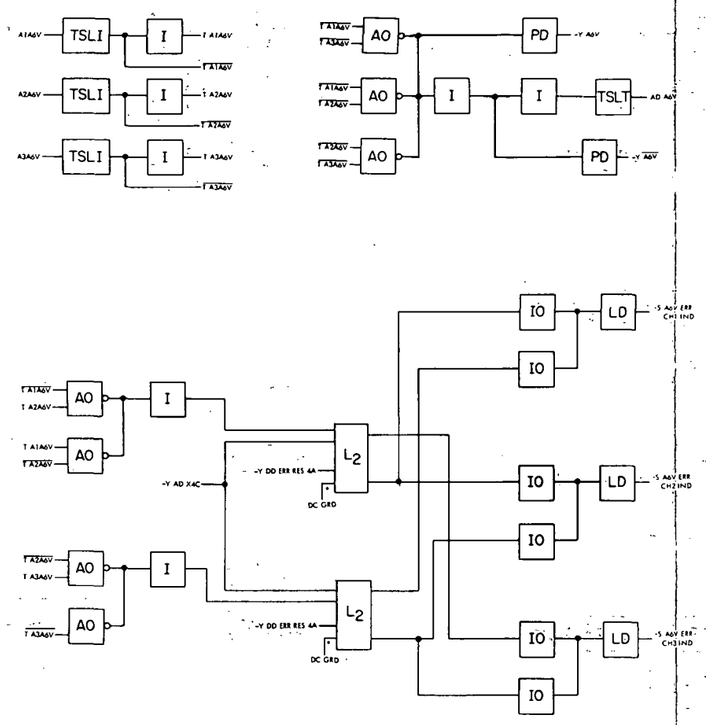
INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RES 4A	31
-Y DD ERR RES 4B	31

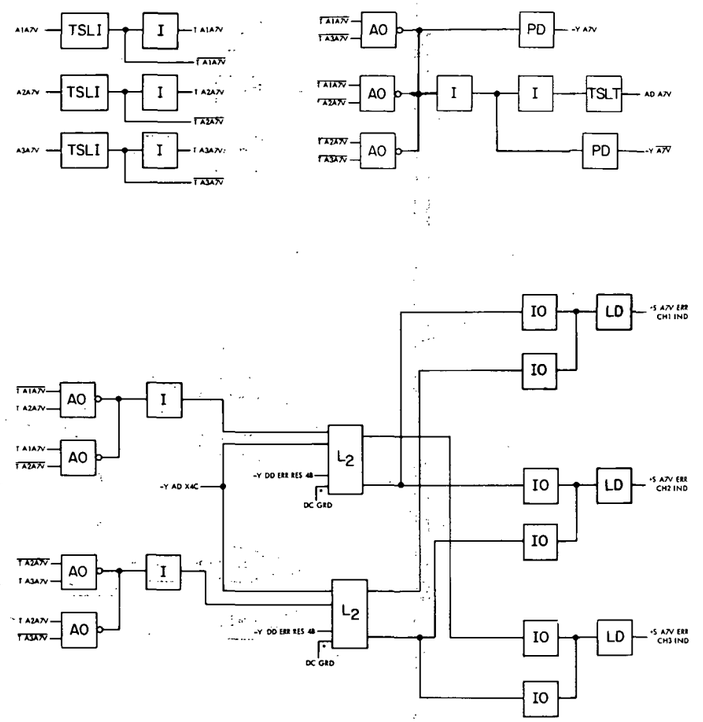
OUTPUTS	
SIGNAL	DESTINATION
-Y A6V	30, 65
-Y A6V	30, 65
-Y A7V	30, 65
-Y A7V	30, 65

6942020

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL





REFERENCE ALD PAGES

05.08.15.1
05.08.16.1
05.08.17.1
05.08.18.1

REFERENCE DRAWING

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN - MAX INSIDE MIN - MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES

DESIGNED		DATE
DESIGN CHECK	W. K. Hawley	8-7-64
DRAWN	MIDSTATE	8-3-64
DRAWING CHECK		/ /
DESIGN APPROVAL	M. P. Livingston	8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: ERROR DETECTOR AND VOTER A6V - A7V

CODE IDENT NO. F SIZE 6942020

SCALE WT SHEET 28

CONTRACT NO.

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 30)

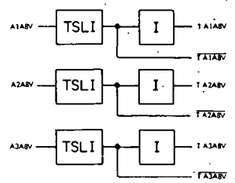
INPUTS	
SIGNAL	ORIGIN
-Y DD ERR RES 48	31

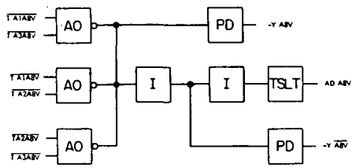
OUTPUTS	
SIGNAL	DESTINATION
-Y A1V -Y $\overline{A1V}$ -Y A2V -Y $\overline{A2V}$	30, 65 30, 65 30, 65 30, 65

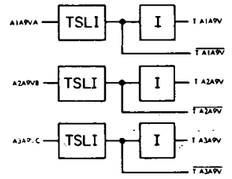
6942020

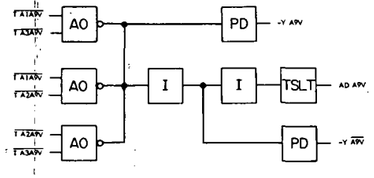
REVISIONS

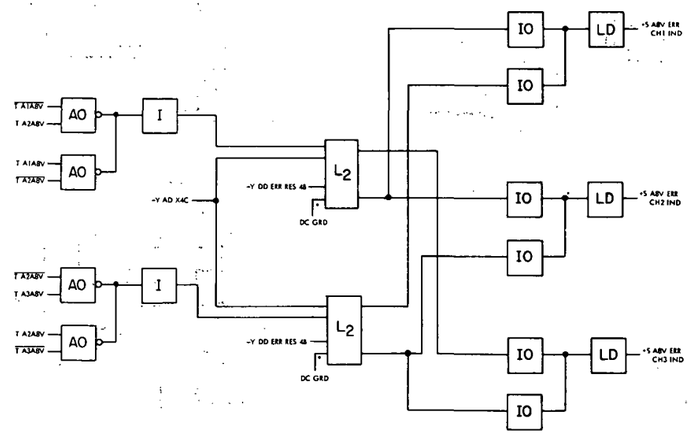
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

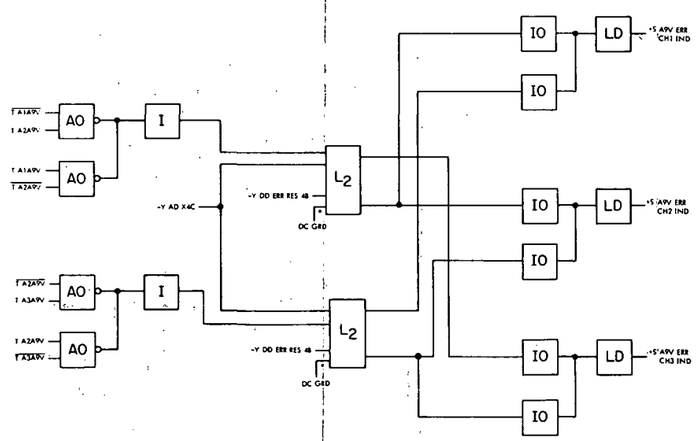












REFERENCE ALD PAGES
05.08.19.1
05.08.20.1
05.08.21.1
05.08.22.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES 2 PLACE DECIMALS ± TOLERANCE ON 3 PLACE DECIMALS ANGLES MAT'L HARD SHEET CASE DEPTH CONTRACT NO.	DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 590 MADISON AVE. NEW YORK 22, N.Y.
	DESIGN CHECK W. K. Hanlon	8-7-64	
	DRAWN MIDSTATE	9-30-64	TITLE ERROR DETECTOR AND VOTER A8V - A9V
	DRAWING CHECK		
	DESIGN APPROVAL M. A. Livingston	8-7-64	CODE IDENT NO. F 6942020
	SCALE	WT	SHEET 29

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 31)

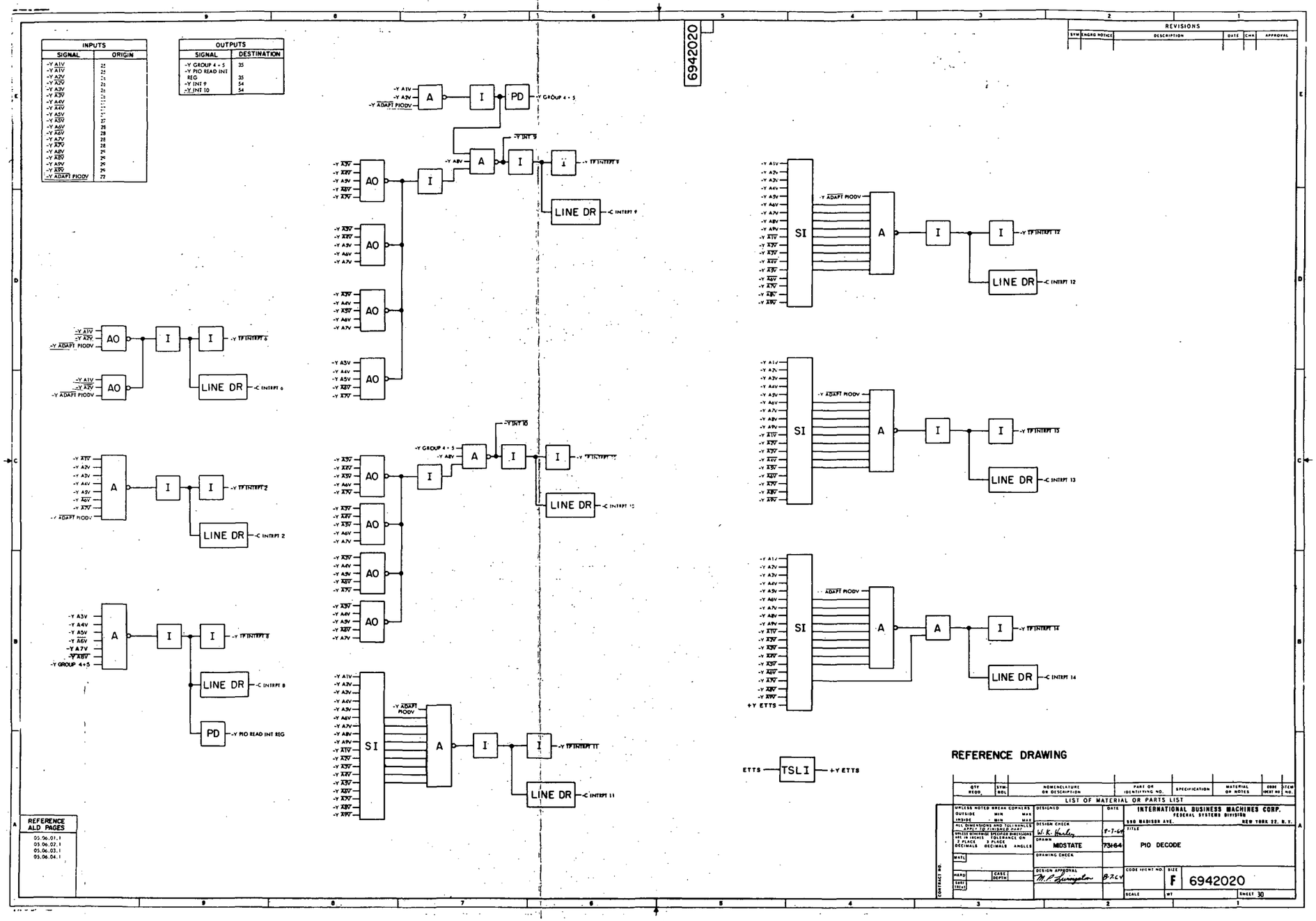
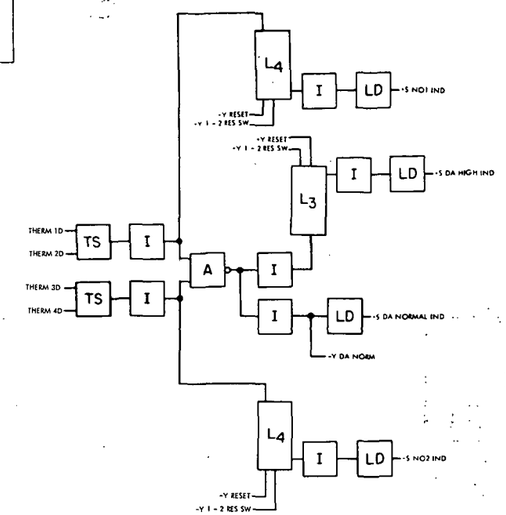


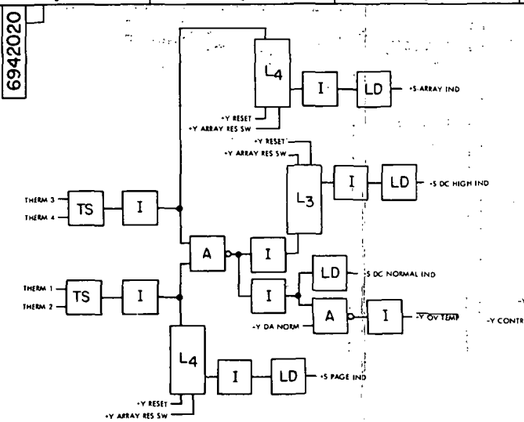
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 32)

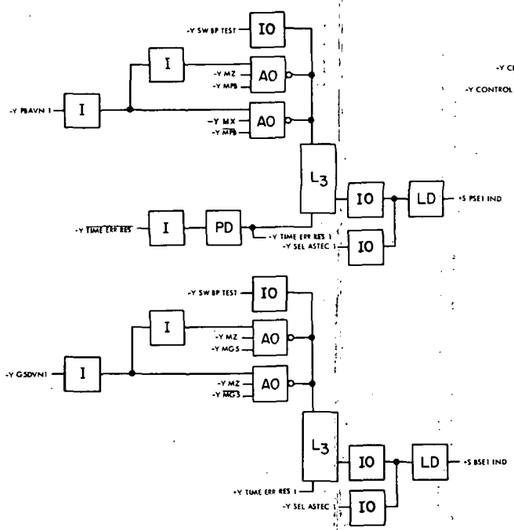
INPUTS	
SIGNAL	ORIGIN
-Y ADV ERR CHAB	18
-Y ADV ERR CHBC	18
-Y CIO 603	57
-Y CONTROL BIT 18	34
-Y CONTROL BIT 19	34
-Y GSDVN ERR CHAB	20
-Y GSDVN ERR	
-Y MGS	5
-Y MGS	5
-Y MPB	5
-Y MPB	5
-Y M2	4
-Y PBAVN 1	20
-Y PBAVN ERR CHAB	20
-Y PBAVN ERR CHBC	20
-Y SEL ASTEC 1	22
+Y TIME ERR RES	10

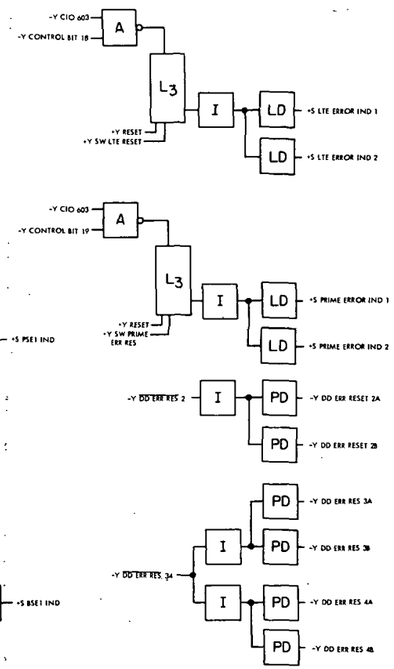
OUTPUTS	
SIGNAL	DESTINATION
-Y DD ERR RES 1	18, 20
-Y DD ERR RES 2A	23, 24
-Y DD ERR RES 2B	19, 21
-Y DD ERR RES 3A	17, 22
-Y DD ERR RES 3B	21, 26, 25
-Y DD ERR RES 4A	28, 27, 26
-Y DD ERR RES 4B	18, 28, 29
-Y OV TEMP	12
+Y TIME ERR RES 1	70, 69

REFERENCE ALD PAGES
05.08.34.1
05.08.49.1
05.08.33.1
05.08.36.1
05.14.01.1
05.14.02.1
05.14.03.1









REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF FINISH

DESIGNED — DATE
DESIGN CHECK — W. K. Hanley — 8-7-64
DRAWN — WEDSTATE — 8-4-64
DRAWING CHECK
DESIGN APPROVAL — M. P. Livingston — 8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
DD ERROR INDICATION AND ERROR RESET

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 31

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

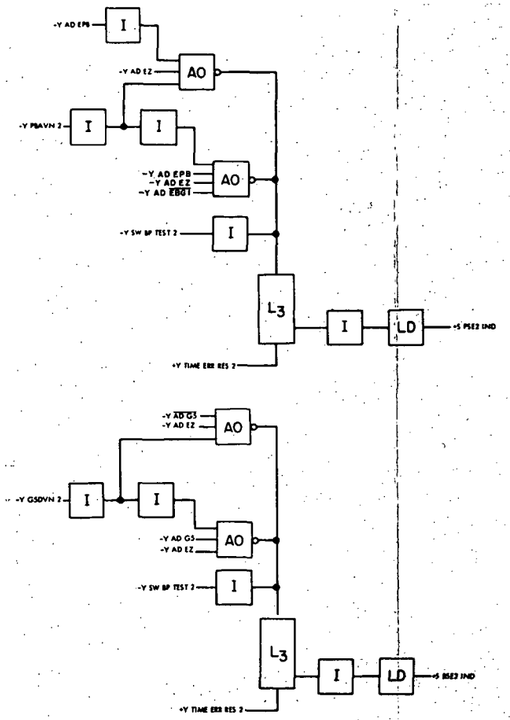
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 33)

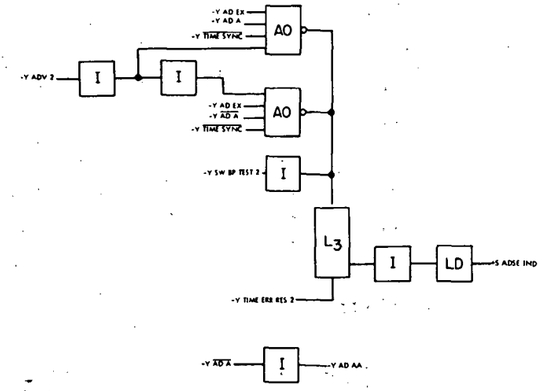
INPUTS	
SIGNAL	ORIGIN
-Y ADV 2	18
-Y GSDVN 2	20
-Y PBAVN 2	20
-Y DATA COMP ERR	21
-Y INTER COMP ERR	21
-Y TIME SYNC	9
-Y AD A	7

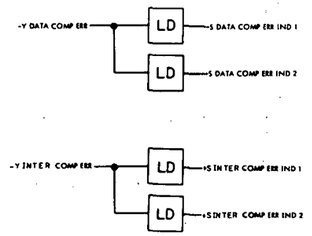
OUTPUTS	
SIGNAL	DESTINATION
-Y AD AA	56

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL







REFERENCE DRAWING

QTY REQD	SYM DES	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
TEST

DESIGNED		DATE
DESIGN CHECK	W. C. Hurley	9-7-64
DRAWN	MIDSTATE	9-7-64
DRAWING CHECK		
DESIGN APPROVAL	M. P. Langlois	9-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
ERROR INDICATIONS

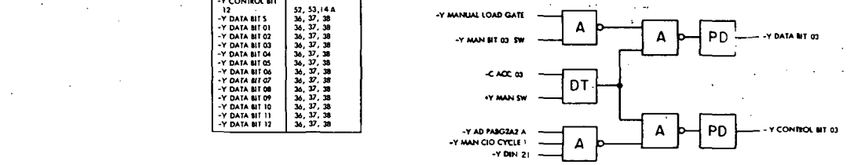
CONTRACT NO.
CODE IDENT NO. SIZE F 6942020
SCALE WT SHEET 32

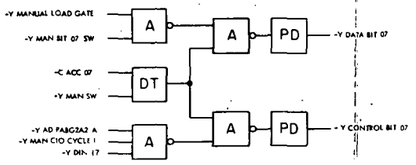
REFERENCE ALD PAGES
05.01.33.1

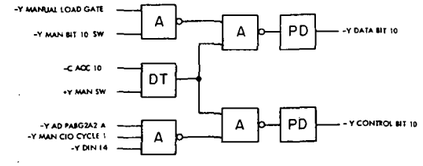
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 34)

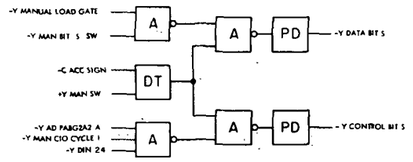
INPUTS	
SIGNAL	ORIGIN
-Y AD PABG2A2 A	10
-Y DIN 12	38
-Y DIN 13	38
-Y DIN 14	38
-Y DIN 15	38
-Y DIN 16	38
-Y DIN 17	38
-Y DIN 18	38
-Y DIN 19	38
-Y DIN 20	38
-Y DIN 21	38
-Y DIN 22	38
-Y DIN 23	38
-Y DIN 24	38
-Y MAN CIO CYCLE 1	60
-Y MAN CIO CYCLE 2	60
-Y MANUAL LOAD GATE	60

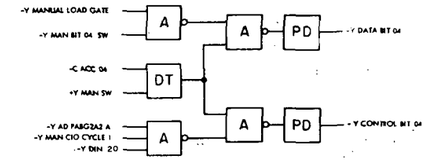
OUTPUTS	
SIGNAL	DESTINATION
-Y CONTROL BIT 5	39, 53, 62
-Y CONTROL BIT 01	53, 62
-Y CONTROL BIT 02	52, 53, 62
-Y CONTROL BIT 03	52, 53, 62
-Y CONTROL BIT 04	52, 53
-Y CONTROL BIT 05	52, 53
-Y CONTROL BIT 06	52, 53
-Y CONTROL BIT 07	52, 53, 56
-Y CONTROL BIT 08	52, 53
-Y CONTROL BIT 09	52, 53
-Y CONTROL BIT 10	52, 53
-Y CONTROL BIT 11	52, 53, 14 B
-Y CONTROL BIT 12	52, 53, 14 A
-Y DATA BIT 5	36, 37, 38
-Y DATA BIT 01	36, 37, 38
-Y DATA BIT 02	36, 37, 38
-Y DATA BIT 03	36, 37, 38
-Y DATA BIT 04	36, 37, 38
-Y DATA BIT 05	36, 37, 38
-Y DATA BIT 06	36, 37, 38
-Y DATA BIT 07	36, 37, 38
-Y DATA BIT 08	36, 37, 38
-Y DATA BIT 09	36, 37, 38
-Y DATA BIT 10	36, 37, 38
-Y DATA BIT 11	36, 37, 38
-Y DATA BIT 12	36, 37, 38

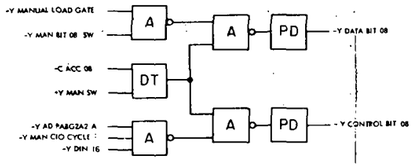


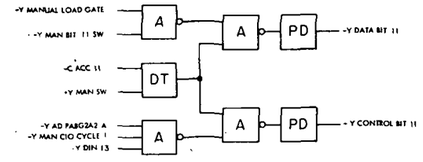


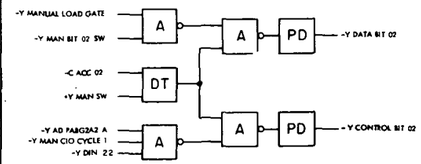


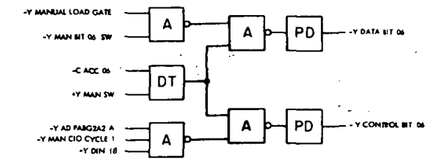












REFERENCE ALD PAGES
05.03.01.1
05.03.02.1
05.03.03.1
05.03.04.1
05.03.05.1

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES ARE APPLIED AFTER PLATING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD SOFT
CASE DEPTH
CONTRACT NO.

DESIGNED — DATE
DESIGN CHECK — 7-7-64
DRAWN — IBM — 7/15/64
DRAWING CHECK
DESIGN APPROVAL — 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: DATA BIT GENERATOR

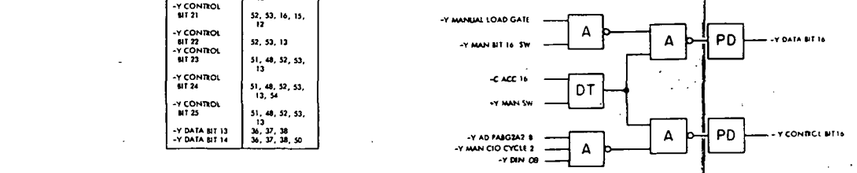
CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 33

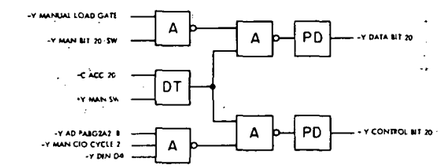
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 35)

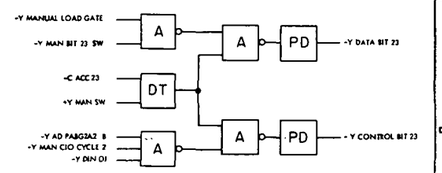
INPUTS	
SIGNAL	ORIGIN
-Y AD PABG2A2 A	10
-Y AD PABG2A2 B	10
-Y DIN 01	38
-Y DIN 02	38
-Y DIN 03	38
-Y DIN 04	38
-Y DIN 05	38
-Y DIN 06	38
-Y DIN 07	38
-Y DIN 08	38
-Y DIN 09	38
-Y DIN 10	38
-Y DIN 11	38
-Y DIN 2A	38
-Y DIN 2B	38
-Y DIN 25	38
-Y MAN CIO CYCLE 2	60
-Y MANUAL LOAD GATE	60

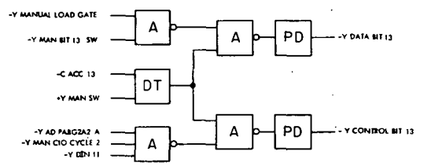
OUTPUTS	
SIGNAL	DESTINATION
-Y CONTROL BIT 13	52, 53, 64
-Y CONTROL BIT 14	52, 53, 15, 16
-Y CONTROL BIT 15	52, 53, 15, 16
-Y CONTROL BIT 16	52, 53, 15, 16, 13
-Y CONTROL BIT 17	52, 53, 15, 16, 13
-Y CONTROL BIT 18	52, 53, 15, 16, 13, 31
-Y CONTROL BIT 19	52, 53, 15, 16, 31
-Y CONTROL BIT 20	52, 53, 16, 15, 12
-Y CONTROL BIT 21	52, 53, 16, 15, 12
-Y CONTROL BIT 22	52, 53, 13
-Y CONTROL BIT 23	51, 48, 52, 53, 13
-Y CONTROL BIT 24	51, 48, 52, 53, 13, 54
-Y CONTROL BIT 25	51, 48, 52, 53, 13
-Y DATA BIT 13	36, 37, 38
-Y DATA BIT 14	36, 37, 38, 50

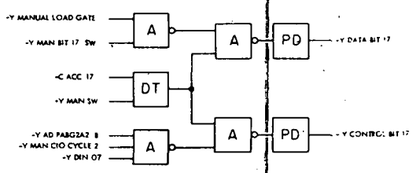
OUTPUTS	
SIGNAL	DESTINATION
-Y DATA BIT 15	50, 54, 37, 38
-Y DATA BIT 16	38, 50, 54
-Y DATA BIT 17	38, 50, 54
-Y DATA BIT 18	38, 50, 54
-Y DATA BIT 19	38, 50, 54
-Y DATA BIT 20	38, 50, 54
-Y DATA BIT 21	38, 50, 54
-Y DATA BIT 22	38, 50, 54
-Y DATA BIT 23	38, 50, 54
-Y DATA BIT 24	38, 50, 54
-Y DATA BIT 25	38, 50, 54

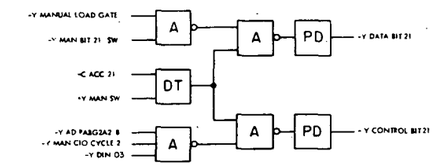


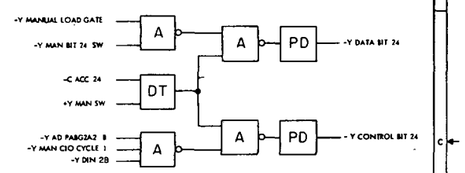


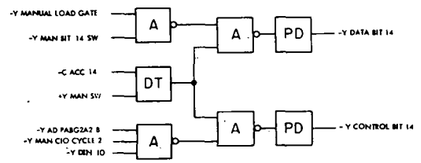


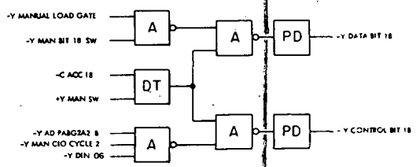


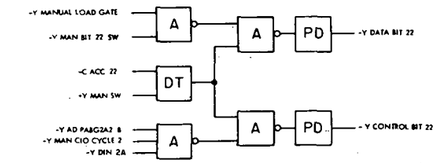


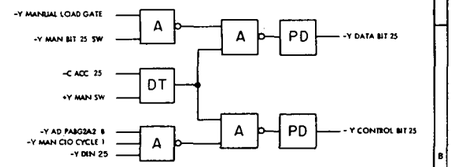


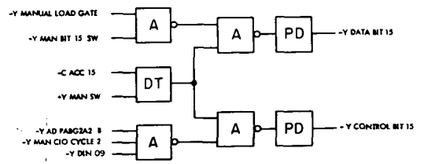


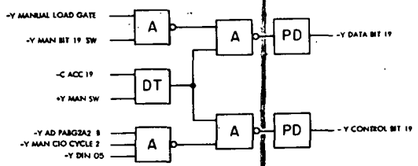












REFERENCE ALD PAGES
05.03.05.1
05.03.06.1
05.03.07.1
05.03.08.1
05.03.09.1

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE DRAWING

QTY REQD.	SYM NOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (PART NO)	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX	DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 590 MADISON AVE. NEW YORK 22, N.Y.
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE: ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES	DESIGN CHECK W.K. Hanley	7-7-64	
MATL	DRAWN IBM	7-15-64	TITLE DATA BIT GENERATOR
HARD CASE DEPTH	DRAWING CHECK		
HEAT TREAT	DESIGN APPROVAL M.A. Frangos	8-7-64	CODE IDENT NO. SIZE F 6942020
			SCALE WT SHEET 36

CONTRACT NO.

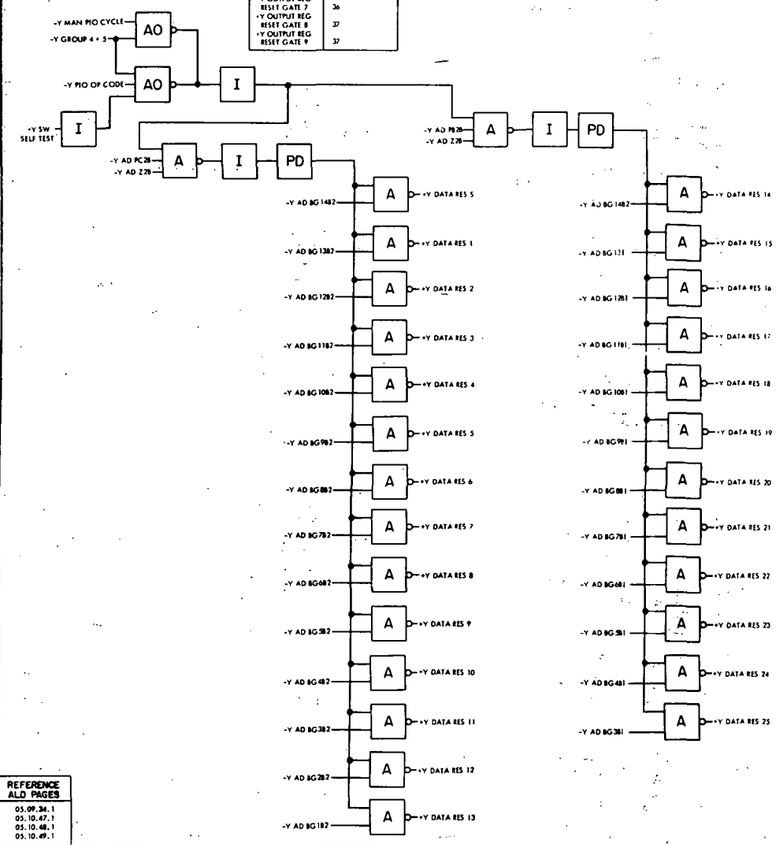
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 36)

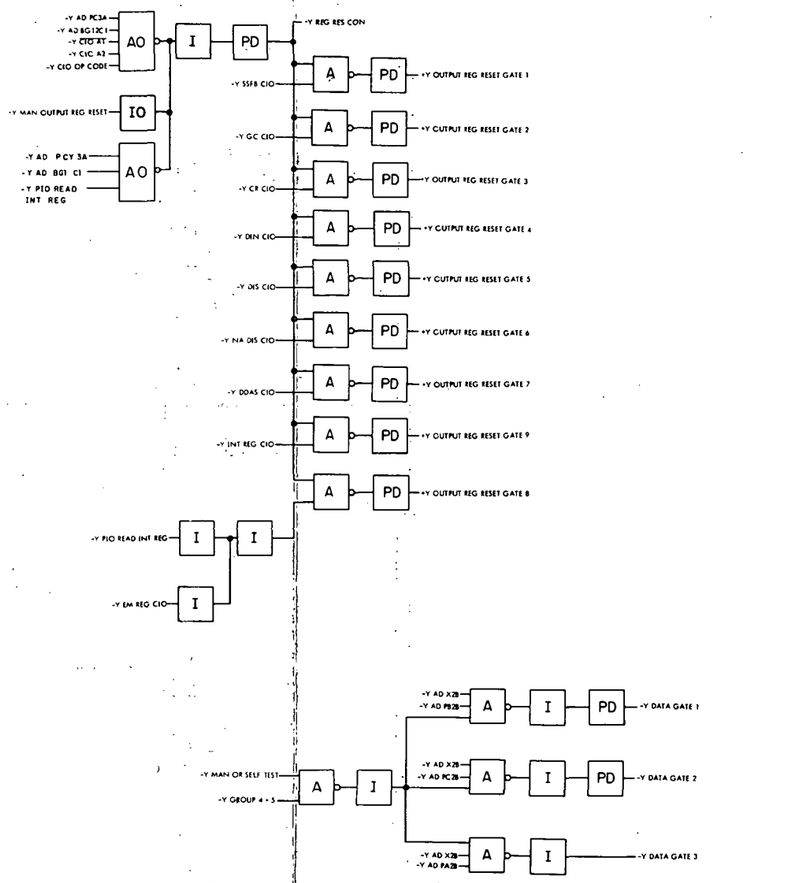
INPUTS	
SIGNAL	ORIGIN
-Y CIO A1	67
-Y CIO A2	67
-Y CIO OP CODE	60
-Y EM REG CIO	60
-Y GROUP 4 + 5	30
-Y MAN OR SELF TEST	39
-Y MAN OUTPUT REG RESET	60
-Y MAN PIO CYCLE	60
-Y PIO OP CODE	60
-Y PIO READ INT REG	30

OUTPUTS	
SIGNAL	DESTINATION
-Y DATA GATE 1	43, 44
-Y DATA GATE 2	40, 41, 42
-Y DATA GATE 3	40
+Y DATA RES 5	40
+Y DATA RES 1	40
+Y DATA RES 2	40
+Y DATA RES 3	40
+Y DATA RES 4	40
+Y DATA RES 5	41
+Y DATA RES 6	41
+Y DATA RES 7	41
+Y DATA RES 8	41
+Y DATA RES 9	41
+Y DATA RES 10	42
+Y DATA RES 11	42
+Y DATA RES 12	42
+Y DATA RES 13	42
+Y DATA RES 14	42
+Y DATA RES 15	43
+Y DATA RES 16	43
+Y DATA RES 17	43
+Y DATA RES 18	43
+Y DATA RES 19	43
+Y DATA RES 20	44
+Y DATA RES 21	44
+Y DATA RES 22	44
+Y DATA RES 23	44
+Y DATA RES 24	44
+Y DATA RES 25	44
+Y OUTPUT REG RESET GATE 1	36
+Y OUTPUT REG RESET GATE 2	36
+Y OUTPUT REG RESET GATE 3	36
+Y OUTPUT REG RESET GATE 4	38
+Y OUTPUT REG RESET GATE 5	38
+Y OUTPUT REG RESET GATE 6	36
+Y OUTPUT REG RESET GATE 7	36
+Y OUTPUT REG RESET GATE 8	37
+Y OUTPUT REG RESET GATE 9	37

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL





REFERENCE ALO PAGES
05.09.34.1
05.10.47.1
05.10.48.1
05.10.49.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (RNT NO)	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS DIFFERENT SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED		DATE
DESIGN CHECK	W. K. Hurley	8-7-64
DRAWN	MIDSTATE	8-3-64
DRAWING CHECK		
DESIGN APPROVAL	M. F. Langdon	8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N. Y.

TITLE: DATA RESETS, DATA GATES, AND OUTPUT REG RESETS

CODE IDENT NO | SIZE F | 6942020
SCALE | WT | SHEET 35

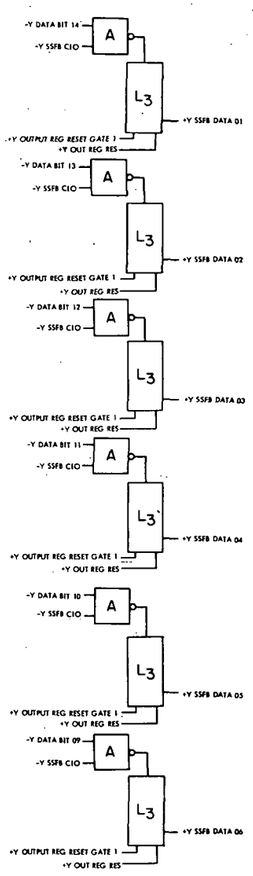
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 37)

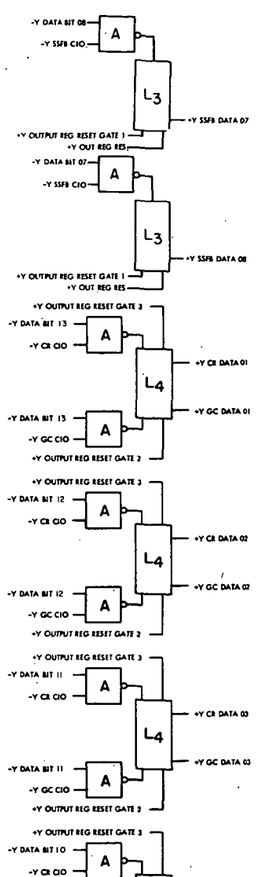
INPUTS	
SIGNAL	ORIGIN
-Y CR CIO	60
-Y DATA BIT 5	33
-Y DATA BIT 01 thru 14	33
-Y DDAS CIO	60
+Y OUTPUT REG RESET GATE 1	35
+Y OUTPUT REG RESET GATE 3	35
+Y OUTPUT REG RESET GATE 7	35
-Y SSFB CIO	60
-Y NA DIS CIO	60

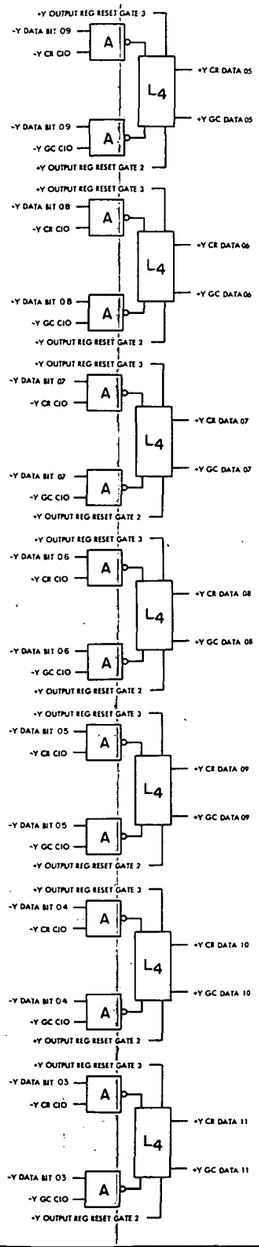
OUTPUTS	
SIGNAL	DESTINATION
-Y CR DATA 01 thru 14	72
+Y DDAS DATA 01 thru 10	72
-Y GC DATA 01 thru 14	72
+Y NA DIS DATA 01 thru 08	72
-Y SSFB DATA 01 thru 08	72

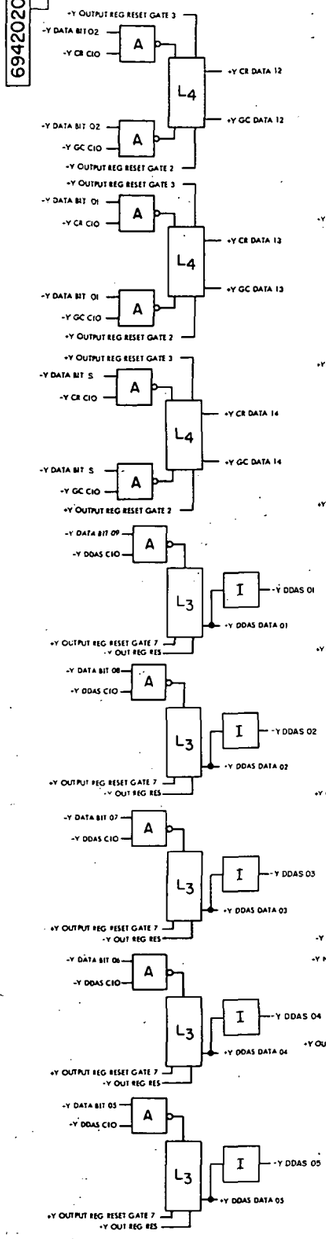
REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

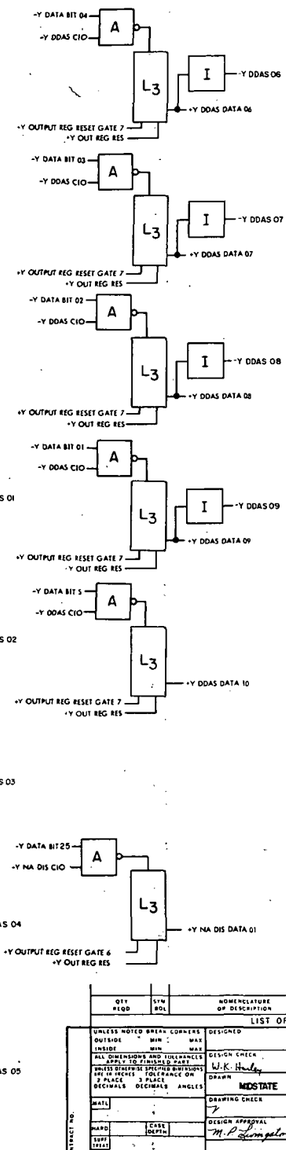
6942020

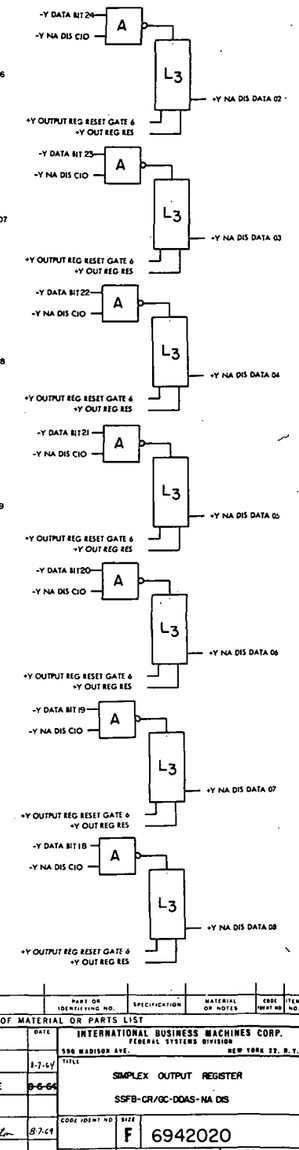












REFERENCE ALD PAGES
05.09.01.1
05.09.02.1
05.09.03.1
05.09.04.1
05.09.05.1
05.09.06.1
05.09.15.1
05.09.16.1
05.09.17.1
05.09.18.1
05.09.19.1

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX ALL DIMENSIONS AND TOLERANCES ARE IN INCHES. TOLERANCE ON UNITED STATES SPECIFICATIONS 2 PLACE DECIMALS ± .01 3 PLACES DECIMALS ± .005 ANGLES ± 1°

MATL

HARD COAT DEPTH

SURF TREAT

CONTRACT NO.

DESIGNED — DATE

DESIGN CHECK — W.K. Hurley — 8-7-64

DRAWN — MIDSTATE — 8-6-64

DRAWING CHECK — J.

DESIGN APPROVAL — M.P. Lampe — 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
SIMPLEX OUTPUT REGISTER
SSFB-CR/GC-DDAS-NA DIS

CODE IDENT NO — SIZE F — 6942020

SCALE — WT — SHEET 38

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 38)

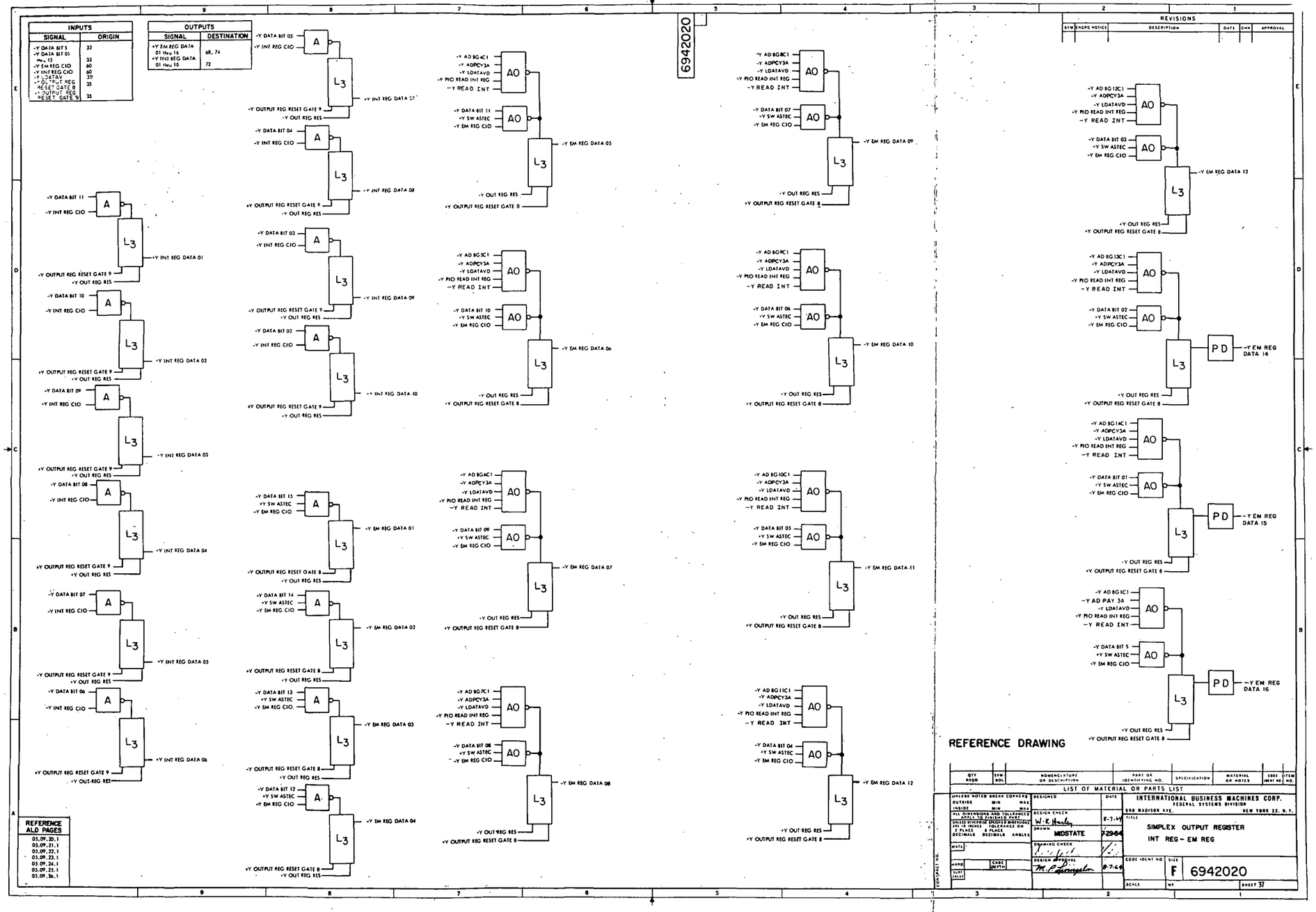


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 39)

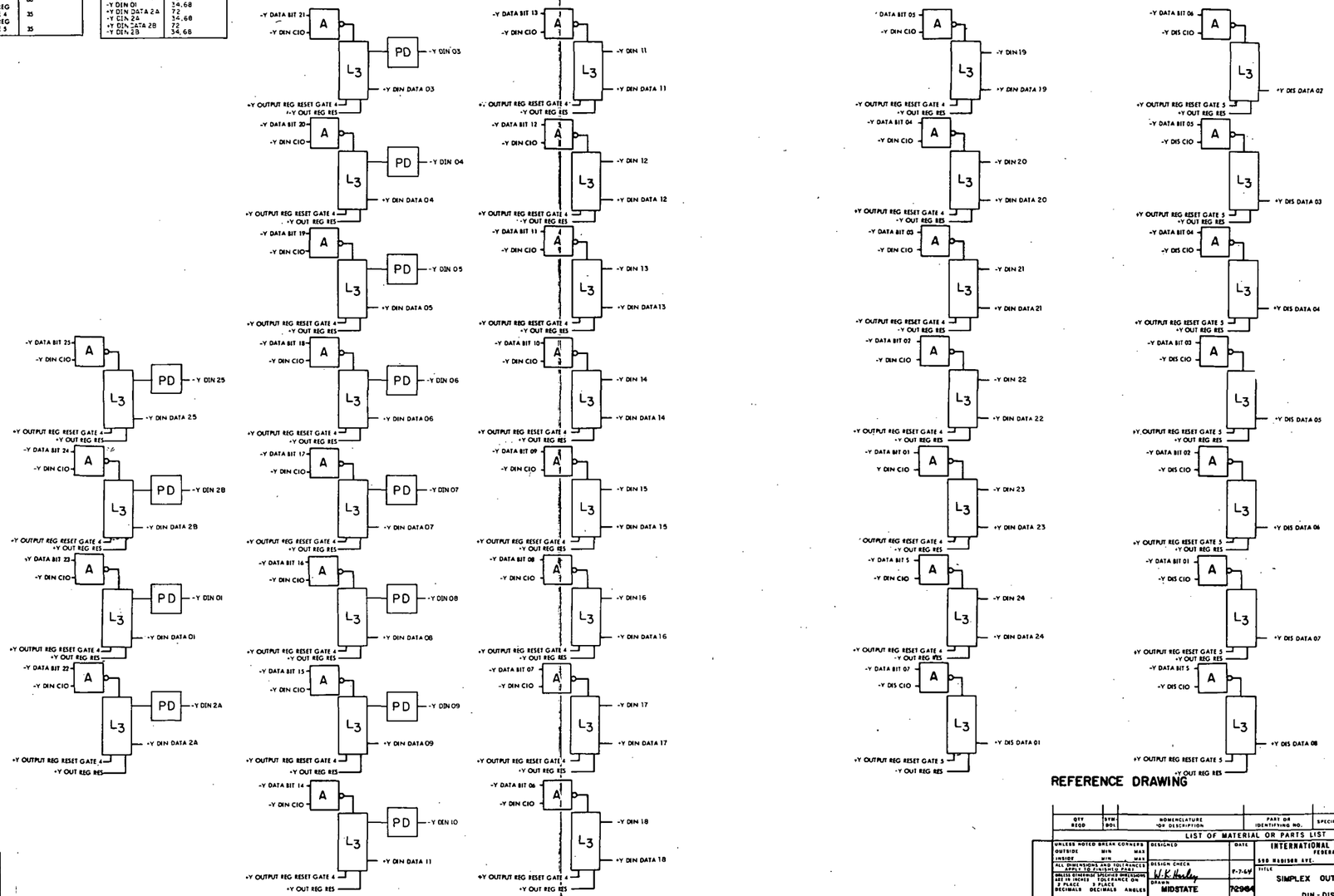
INPUTS	
SIGNAL	ORIGIN
-Y DATA BIT 5	33
-Y DATA BIT 01 thru 12	33
-Y DATA BIT 13 thru 25	34
-Y DIN CIO	60
-Y DIS CIO	60
+Y OUTPUT REG RESET GATE 4	35
+Y OUTPUT REG RESET GATE 5	35

OUTPUTS	
SIGNAL	DESTINATION
+Y DIN DATA 03 thru 25	72
-Y DIN 03 thru 12	34, 68
+Y DIN 3 thru 26	33, 68
+Y DIS DATA 01 thru 08	72
+Y DIN DATA 01	72
-Y DIN 01	34,68
+Y DIN DATA 2A	72
-Y DIN 2A	34,68
+Y DIN DATA 2B	72
-Y DIN 2B	34,68

6942020

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL



REFERENCE ALD PAGES
05.09.06.1
05.09.07.1
05.09.08.1
05.09.09.1
05.09.10.1
05.09.11.1
05.09.12.1
05.09.13.1
05.09.14.1

REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	SHEET NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
HARD
SHRT TRTMT
CASE DEPTH

DESIGNED — DATE
DESIGN CHECK W.K. Hurley — 7-7-69
DRAWING CHECK MIDSTATE 72984
DRAWING CHECK
DESIGN APPROVAL M.P. Hampton — 8-7-69

CONTRACT NO

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
SIMPLEX OUTPUT REGISTER
DIN - DIS

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 38

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 40)

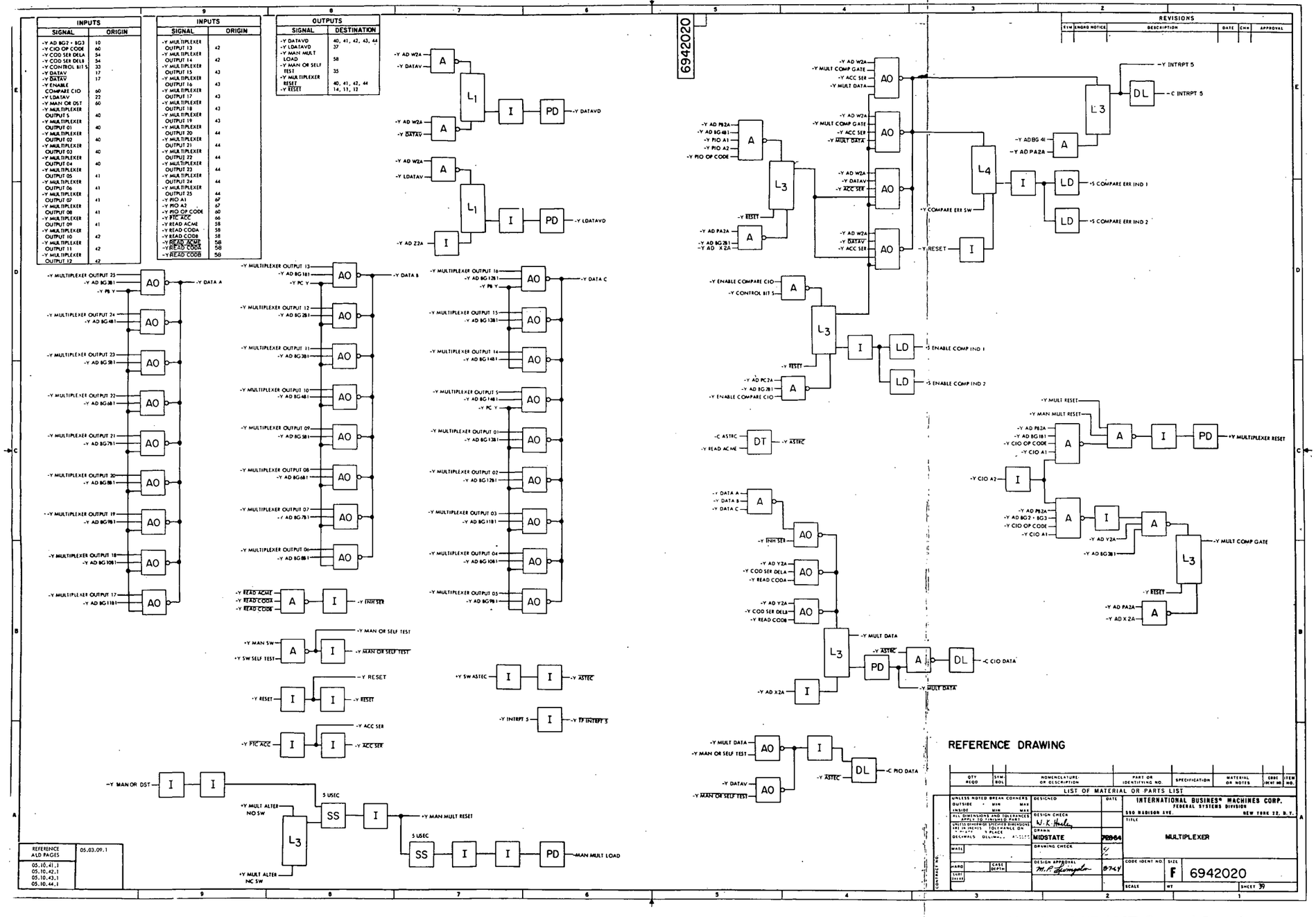


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 41)

INPUTS	
SIGNAL	ORIGIN
-Y ADCO INPUT CIO	58
-Y CR DATA 10 OUT	73
-Y CR DATA 11 OUT	73
-Y CR DATA 12 OUT	73
-Y CR DATA 13 OUT	73
-Y CR DATA 14 OUT	73
-Y CR INPUT CIO	58
-Y DATA GATE 2	35
-Y DATA GATE 3	35
-Y DATA RES 5	35
-Y DATA RES 1	35
-Y DATA RES 2	35
-Y DATA RES 3	35
-Y DATA RES 4	35
-Y DATAVD	39
-Y DDAS DATA 06 thru 10 OUT	73
-Y DDAS IN DATA 22 thru 26	71

INPUTS	
SIGNAL	ORIGIN
-Y DDAS INPUT CIO	58
-Y DIN DATA 20 thru 24 OUT	73
-Y DIN INPUT CIO	58
-Y DIS DATA 04 thru 08 OUT	73
-Y DIS INPUT CIO	58
-Y DOR IN DATA 09 thru 13	71
-Y DOR INPUT CIO	58
-Y EM REG DATA 12 thru 16 OUT	73
-Y EM REG INPUT CIO	58
-Y GC A IN DATA 22 thru 26	71
-Y GC DATA 10 thru 14 OUT	73
-Y GC INPUT CIO	58
-Y GC MODR IN DATA 2 thru 6	71
-Y IDDAS INPUT CIO	58

INPUTS	
SIGNAL	ORIGIN
-Y IGCA INPUT CIO	58
-Y IGCB INPUT CIO	58
-Y INT REG DATA 08 OUT	73
-Y INT REG DATA 09 OUT	73
-Y INT REG DATA 10 OUT	73
+Y MULTIPLEXER RESET	39
-Y NA SIM IN DATA 22 thru 26	71
-Y NA SIN INPUT CIO	58
-Y SSR IN DATA 11 thru 15	71
-Y SSR INPUT CIO	58
-Y TEL DA IN DATA 22 thru 26	71
-Y TEL DA INPUT CIO	58
-Y TEL DB INPUT CIO	58
-Y TEL RTR IN DATA 5	71

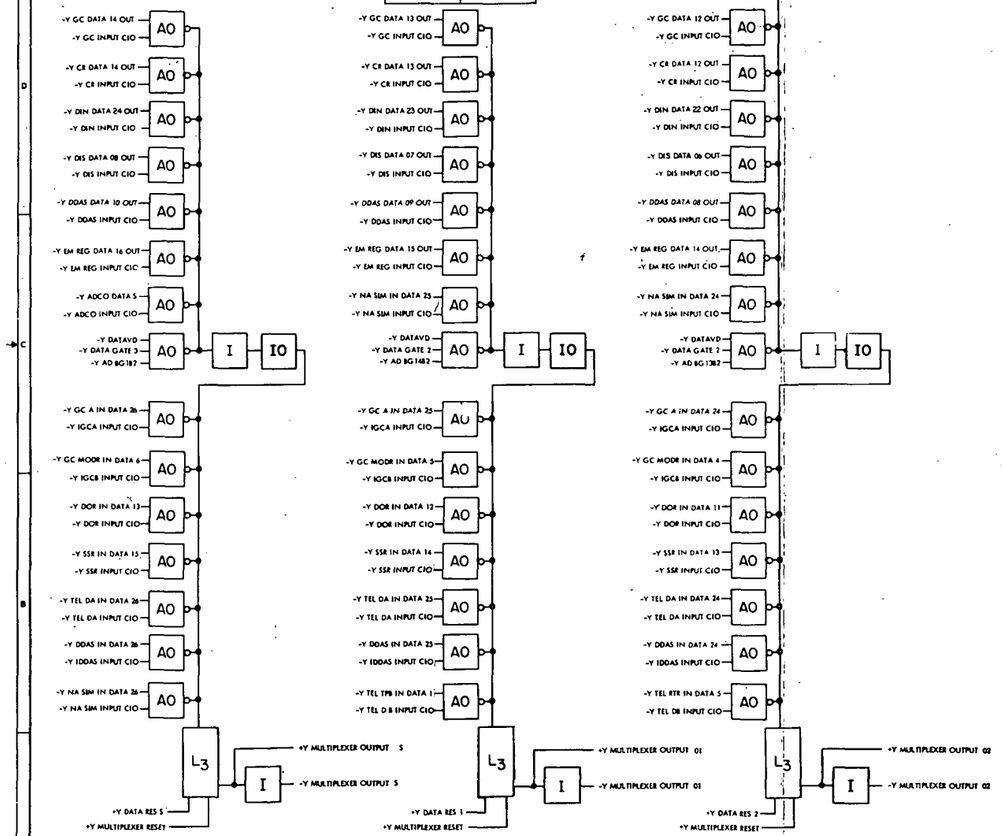
INPUTS	
SIGNAL	ORIGIN
-Y TEL RTR IN DATA 4	71
-Y TEL RTR IN DATA 5	71
-Y TEL TPB IN DATA 1	71

OUTPUTS	
SIGNAL	DESTINATION
-Y MULTIPLEXER OUTPUT 5	39
+Y MULTIPLEXER OUTPUT 01	39
-Y MULTIPLEXER OUTPUT 02	39
-Y MULTIPLEXER OUTPUT 03	39
-Y MULTIPLEXER OUTPUT 04	39
+Y MULTIPLEXER OUTPUT 5	45
-Y MULTIPLEXER OUTPUT 01	45
+Y MULTIPLEXER OUTPUT 02	45
+Y MULTIPLEXER OUTPUT 03	45
+Y MULTIPLEXER OUTPUT 04	45

6942020

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL



REFERENCE ALD PAGES
05.10.01.1
05.10.02.1
05.10.03.1
05.10.04.1
05.10.05.1
05.10.50.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTE	TOOL	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX	DESIGNED	DATE
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART	DESIGN CHECK W.K. Healy	7-1-69
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE NO. 2 PLACE DECIMALS ± .03 3 PLACE DECIMALS ± .010 ANGLES ± 1°	MIDSTATE 72864	
MATL	DRAWING CHECK	
HARD CASE DEPTH	DESIGN APPROVAL M.P. Schmeckpeper	8-7-69
SURF ROUGH		

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE., NEW YORK 22, N.Y.

TITLE: MULTIPLEXER OUTPUTS

CONTRACT NO.

SYSTEM IDENT NO	SIZE	
	F	6942020

SCALE NONE SHEET 80

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 42)

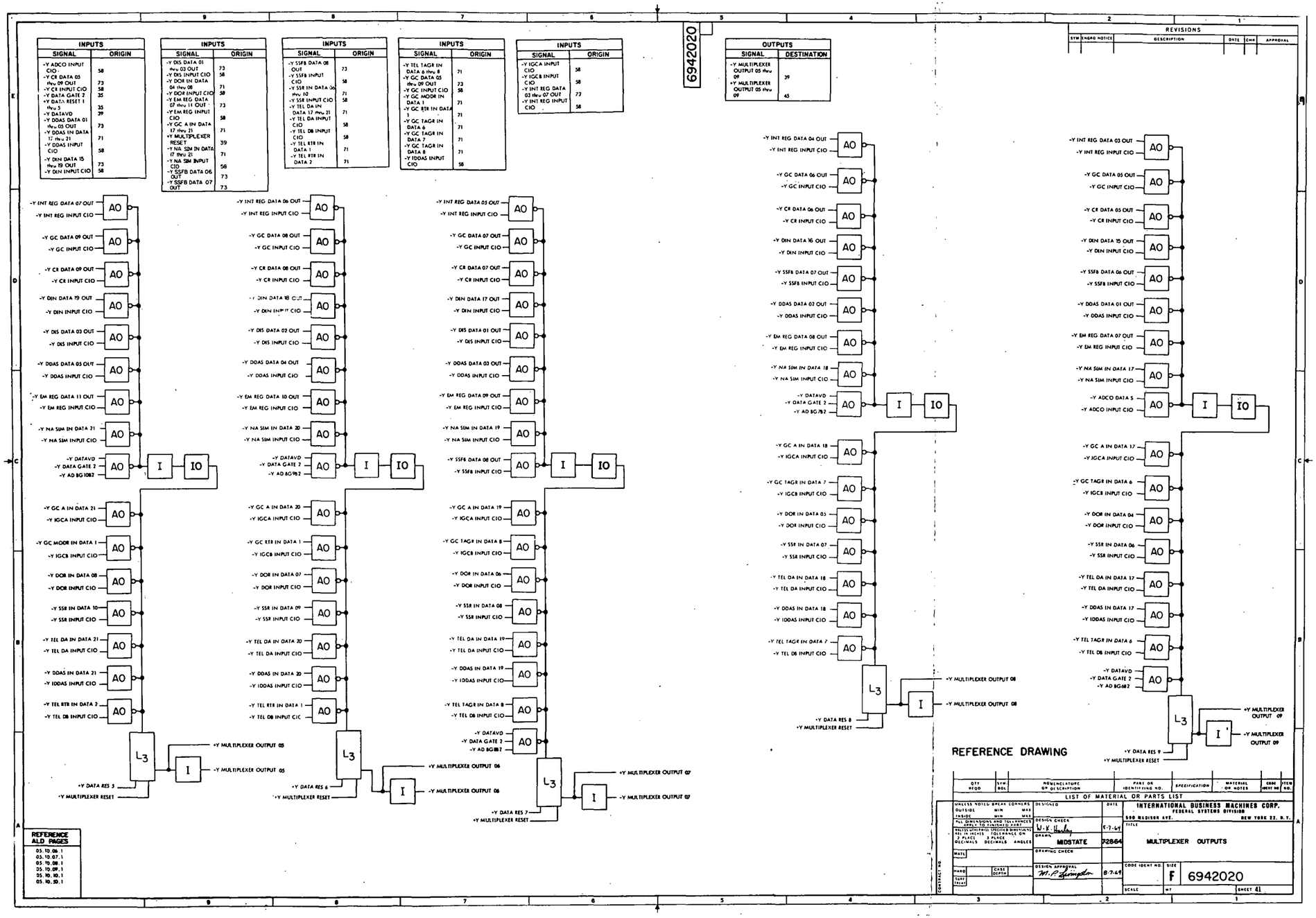


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 43)

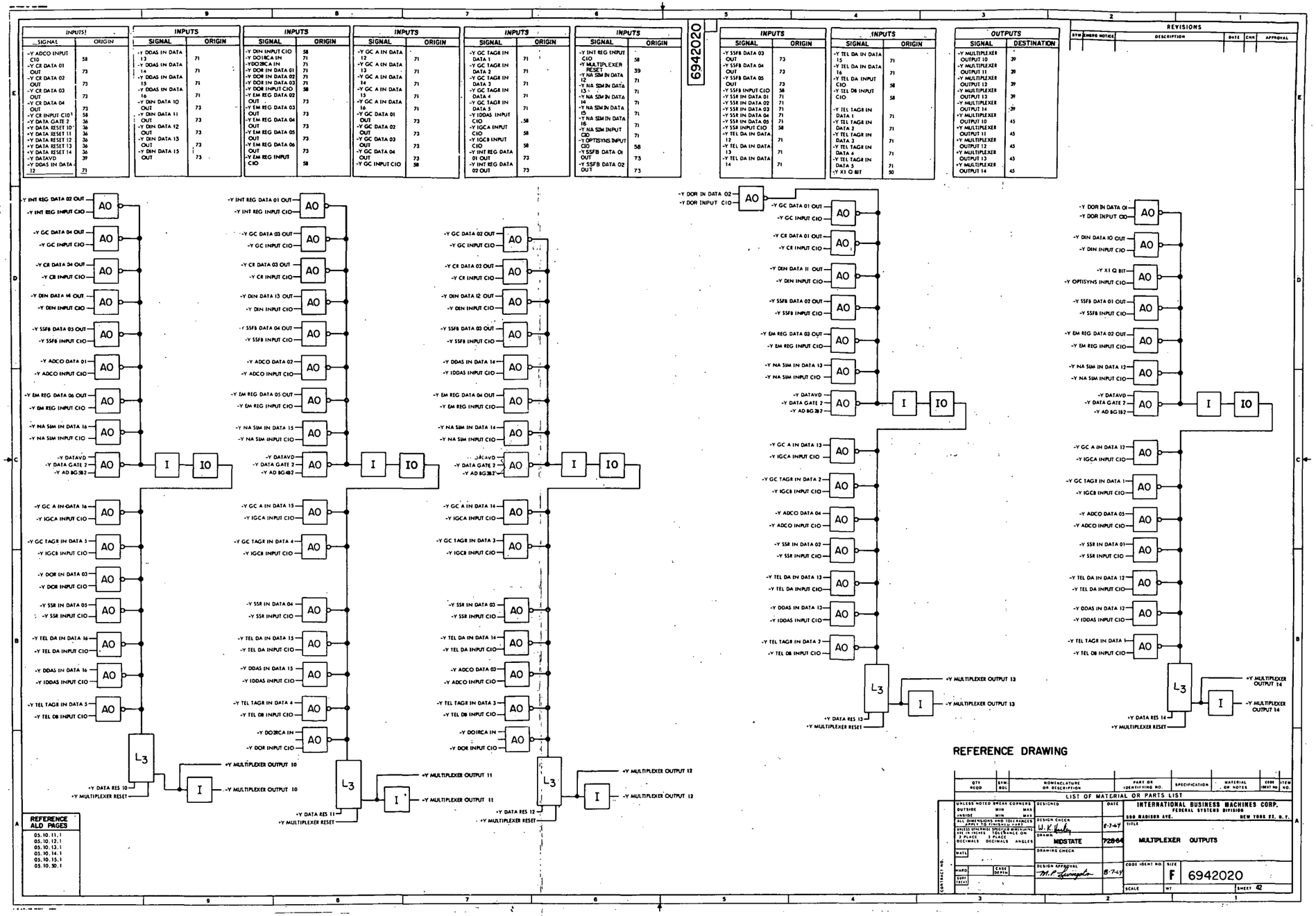


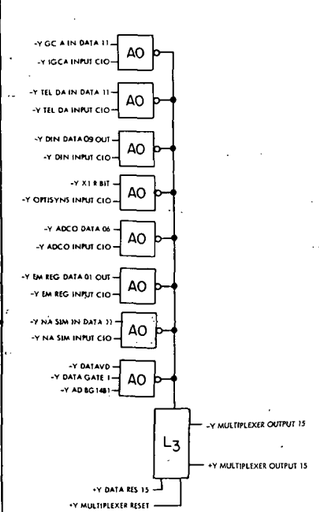
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 44)

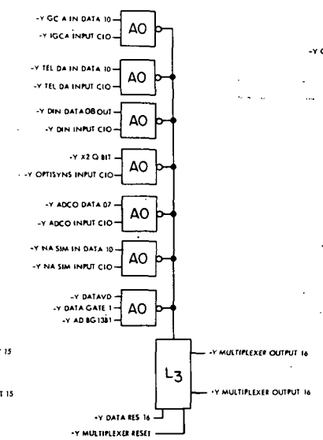
6942020

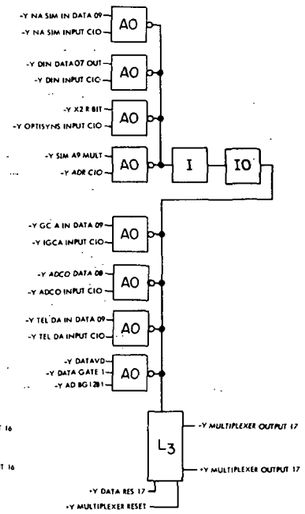
INPUTS	
SIGNAL	ORIGIN
-Y ADCO INPUT CIO	58
-Y ADR CIO	58
-Y DATA GATE 1	35
-Y DATA RESET 15	35
-Y DATA RESET 16	35
-Y DATA RESET 17	35
-Y DATA RESET 18	35
-Y DATA RESET 19	35
-Y DATAVD	39
-Y DIN DATA 05 OUT	73
-Y DIN DATA 06 OUT	73
-Y DIN DATA 07 OUT	73
-Y DIN DATA 08 OUT	73
-Y DIN DATA 09 OUT	73
-Y DIN INPUT CIO	58
-Y EM REG DATA 01 OUT	73
-Y EM REG INPUT CIO	58
-Y GC A IN DATA 07	71
-Y GC A IN DATA 08	71
-Y GC A IN DATA 09	71
-Y GC A IN DATA 10	71
-Y GC A IN DATA 11	71
-Y IGCA INPUT CIO	58
-Y OPTISYNS INPUT CIO	58
-Y NA DIS DATA 07 OUT	73
-Y NA DIS DATA 08 OUT	73
-Y NA DIS INPUT CIO	58
-Y MULTIPLEXER RESET	39

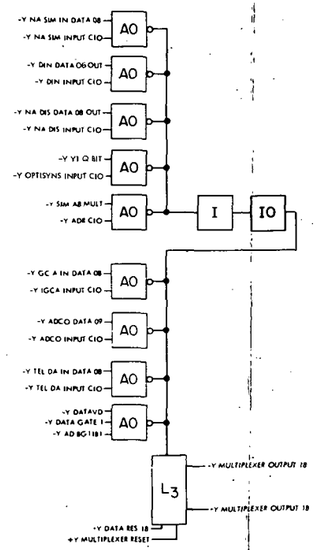
INPUTS	
SIGNAL	ORIGIN
-Y NA SIM IN DATA 07	71
-Y NA SIM IN DATA 08	71
-Y NA SIM IN DATA 09	71
-Y NA SIM IN DATA 10	71
-Y NA SIM IN DATA 11	71
-Y NA SIM INPUT CIO	58
-Y SIM A7 MULT	65
-Y SIM A8 MULT	65
-Y SIM A9 MULT	65
-Y TEL DA IN DATA 07	71
-Y TEL DA IN DATA 08	71
-Y TEL DA IN DATA 09	71
-YTEL DA IN DATA 10	71
-Y TEL DA IN DATA 11	71
-Y TEL DA INPUT CIO	58
-Y X1 R BIT	50
-Y X2 Q BIT	50
-Y X2 R BIT	50
-Y Y1 Q BIT	50
-Y Y1 R BIT	50

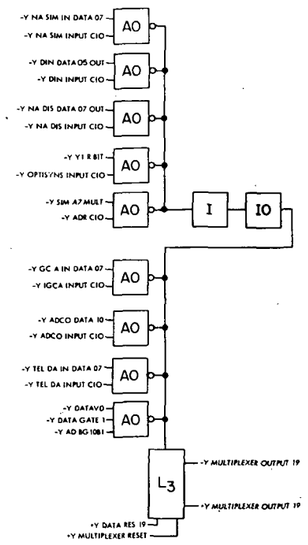
OUTPUTS	
SIGNAL	DESTINATION
-Y MULTIPLEXER OUTPUT 15	39
-Y MULTIPLEXER OUTPUT 16	39
-Y MULTIPLEXER OUTPUT 17	39
-Y MULTIPLEXER OUTPUT 18	39
-Y MULTIPLEXER OUTPUT 19	39
+Y MULTIPLEXER OUTPUT 15	45
+Y MULTIPLEXER OUTPUT 16	45
+Y MULTIPLEXER OUTPUT 17	45
+Y MULTIPLEXER OUTPUT 18	45
+Y MULTIPLEXER OUTPUT 19	45











REFERENCE ALD PAGES
05.10.28.1
05.10.29.1
05.10.30.1
05.10.31.1
05.10.32.1

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE DRAWING

LIST OF MATERIAL OR PARTS LIST

DESIGNED	
DESIGN CHECK	W. K. Hanley 8-7-64
DRAWN	MIDSTATE 7-28-64
DRAWING CHECK	
DESIGN APPROVAL	M. L. Livingston 8-24-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: MULTIPLEXER OUTPUTS

CODE IDENT NO. | SIZE: F | 6942020

SCALE | WT | SHEET 45

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 45)

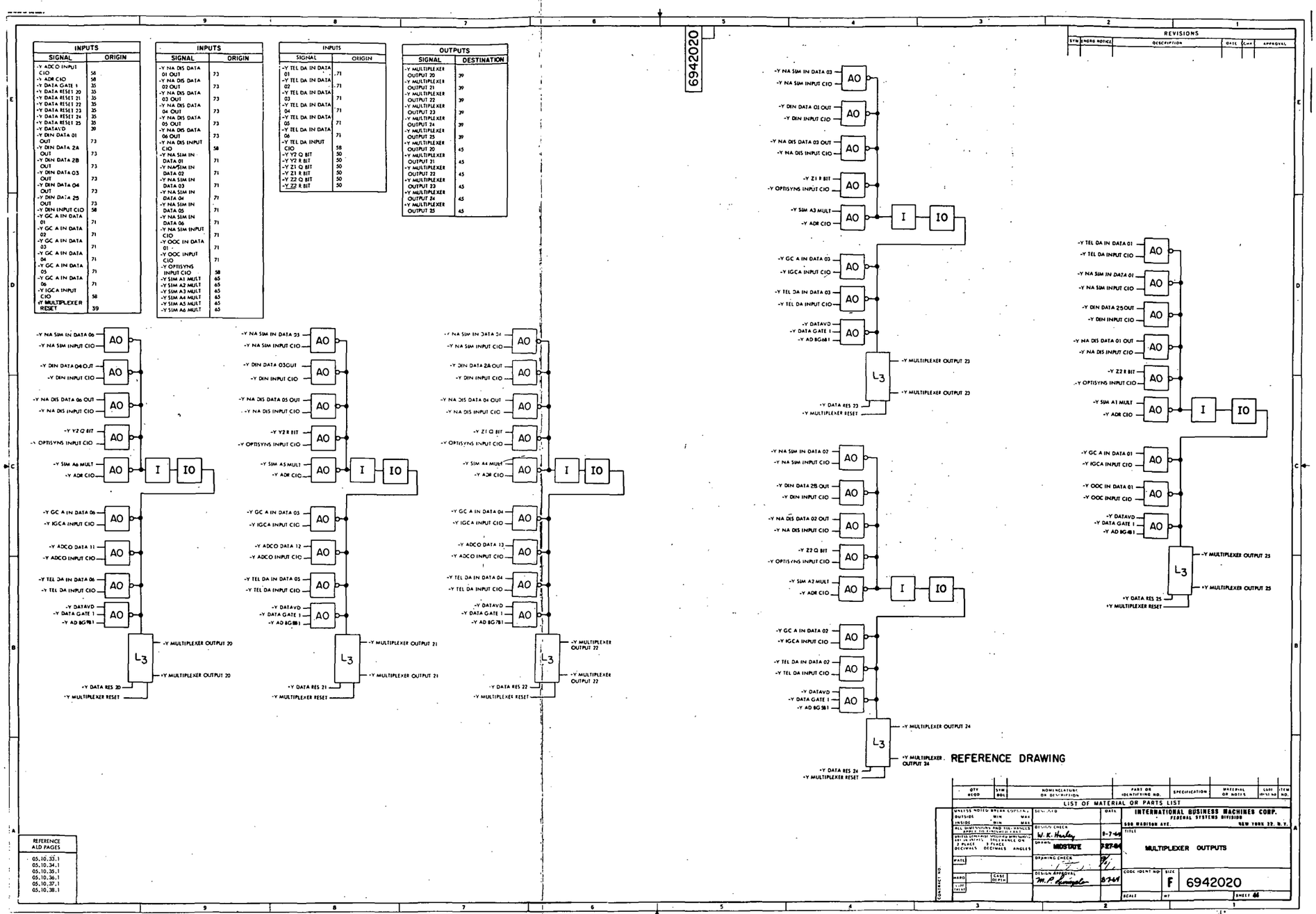
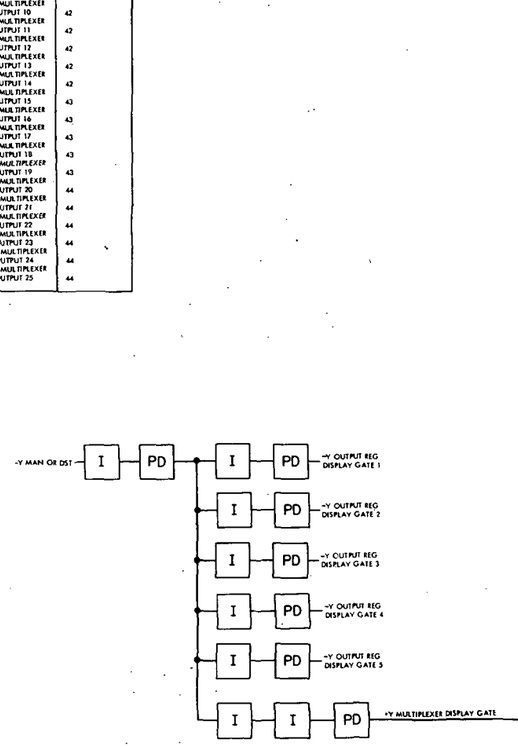


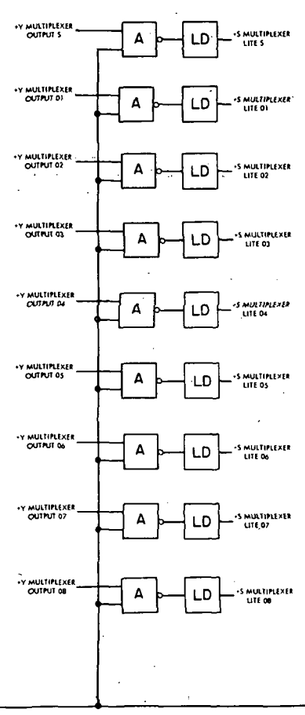
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 46)

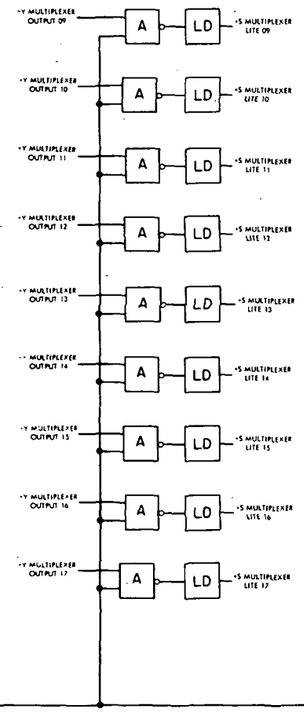
INPUTS	
SIGNAL	ORIGIN
-Y MAIN OR DST	60
-Y MULTIPLEXER OUTPUT 5	40
-Y MULTIPLEXER OUTPUT 01	40
-Y MULTIPLEXER OUTPUT 02	40
-Y MULTIPLEXER OUTPUT 03	40
-Y MULTIPLEXER OUTPUT 04	40
-Y MULTIPLEXER OUTPUT 05	41
-Y MULTIPLEXER OUTPUT 06	41
-Y MULTIPLEXER OUTPUT 07	41
-Y MULTIPLEXER OUTPUT 08	41
-Y MULTIPLEXER OUTPUT 09	41
-Y MULTIPLEXER OUTPUT 10	42
-Y MULTIPLEXER OUTPUT 11	42
-Y MULTIPLEXER OUTPUT 12	42
-Y MULTIPLEXER OUTPUT 13	42
-Y MULTIPLEXER OUTPUT 14	42
-Y MULTIPLEXER OUTPUT 15	43
-Y MULTIPLEXER OUTPUT 16	43
-Y MULTIPLEXER OUTPUT 17	43
-Y MULTIPLEXER OUTPUT 18	43
-Y MULTIPLEXER OUTPUT 19	43
-Y MULTIPLEXER OUTPUT 20	44
-Y MULTIPLEXER OUTPUT 21	44
-Y MULTIPLEXER OUTPUT 22	44
-Y MULTIPLEXER OUTPUT 23	44
-Y MULTIPLEXER OUTPUT 24	44
-Y MULTIPLEXER OUTPUT 25	44

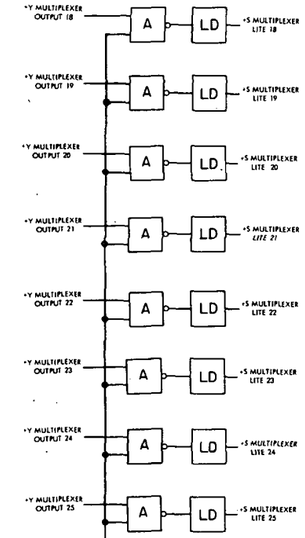
OUTPUTS	
SIGNAL	DESTINATION
-Y OUTPUT REG DISPLAY GATE 1	46
-Y OUTPUT REG DISPLAY GATE 2	46
-Y OUTPUT REG DISPLAY GATE 3	47
-Y OUTPUT REG DISPLAY GATE 4	47
-Y OUTPUT REG DISPLAY GATE 5	47

6942020









REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE ALD PAGES
05.15.18.1
05.15.19.1
05.15.20.1
05.15.21.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CAGE (NCAGE) NO	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD / SURF TREAT — CASE DEPTH

DESIGNED — DATE
DESIGN CHECK U.E. Hanley — 8-7-67
DRAWN MIDSTATE 72364
DRAWING CHECK
DESIGN APPROVAL M.P. Livingston — 8-7-67

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
MANUAL CONTROLS AND IO
MULTIPLEXER DISPLAY

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 45

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 47)

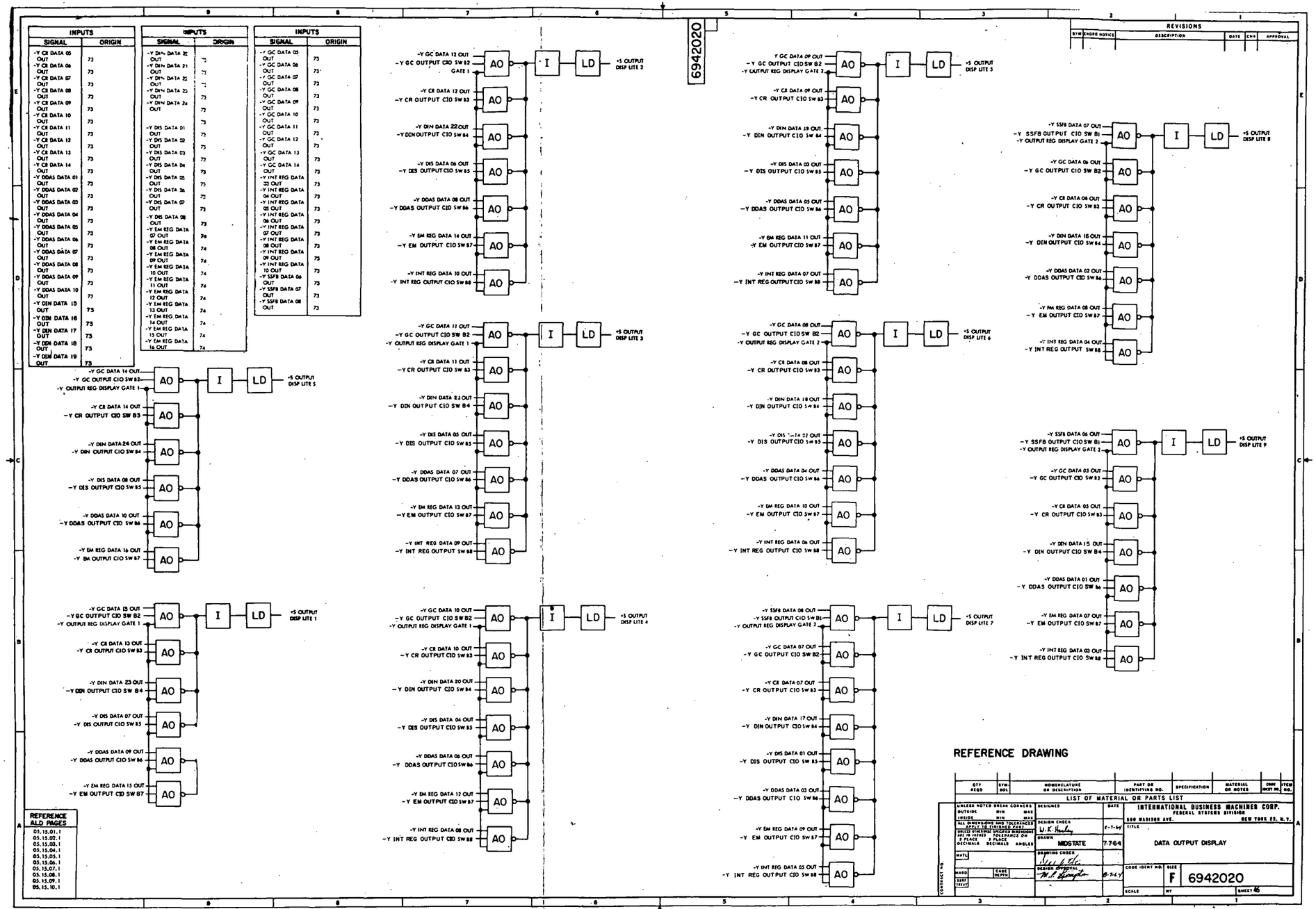


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 48)

INPUTS	
SIGNAL	ORIGIN
-Y COD DATA 01 thru 15	54
-Y CR DATA 01 thru 04 OUT	73
-Y DIN DATA 03 thru 15 OUT	72
-Y GC DATA 01 thru 04 OUT	73
-Y EM REG DATA 01 thru 06 OUT	74
-Y INT REG DATA 01 OUT	73
-Y INT REG DATA 02 OUT	73
-Y NA DIS DATA 01 thru 08 OUT	73
-Y SSFB DATA 01 thru 05 OUT	73
-Y X1 Q BIT	50
-Y X1 R BIT	50
-Y X2 Q BIT	50
-Y X2 R BIT	50
-Y V1 Q BIT	50
-Y Y1 R BIT	50
-Y Y2 Q BIT	50
-Y Y2 R BIT	50
-Y Z1 Q BIT	50
-Y Z1 R BIT	50
-Y Z2 Q BIT	50
-Y Z2 R BIT	50
+Y OUTPUT REG DISPLAY GATE 3	45
+Y OUTPUT REG DISPLAY GATE 4	45
+Y OUTPUT REG DISPLAY GATE 5	45
-Y DIN DATA 01	72
-Y DIN DATA 2A	72
-Y DIN DATA 2B	72

REFERENCE ALD PAGES
05.15.11.1
05.15.12.1
05.15.13.1
05.15.14.1
05.15.15.1
05.15.16.1
05.15.17.1

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REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK APPROVAL

REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	TCD REQ

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE .01 MAX INSIDE .01 MIN MAX	DESIGNED	DATE	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 590 MADISON AVE. NEW YORK 22, N. Y.
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART	W. K. Hanley	8-7-64	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE .02 DECIMALS 3 PLACE .005 DECIMALS ANGLES	DRAWN IBM	7/14/64	TITLE DATA OUTPUT DISPLAY
MATL	DRAWING CHECK		
HARD CASE DEPTH	DESIGN APPROVAL M. P. Livingston	8-7-64	CODE IDENT NO. F SIZE 6942020
SURF TREAT			SCALE WT SHEET 47

CONTRACT NO.

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 49)

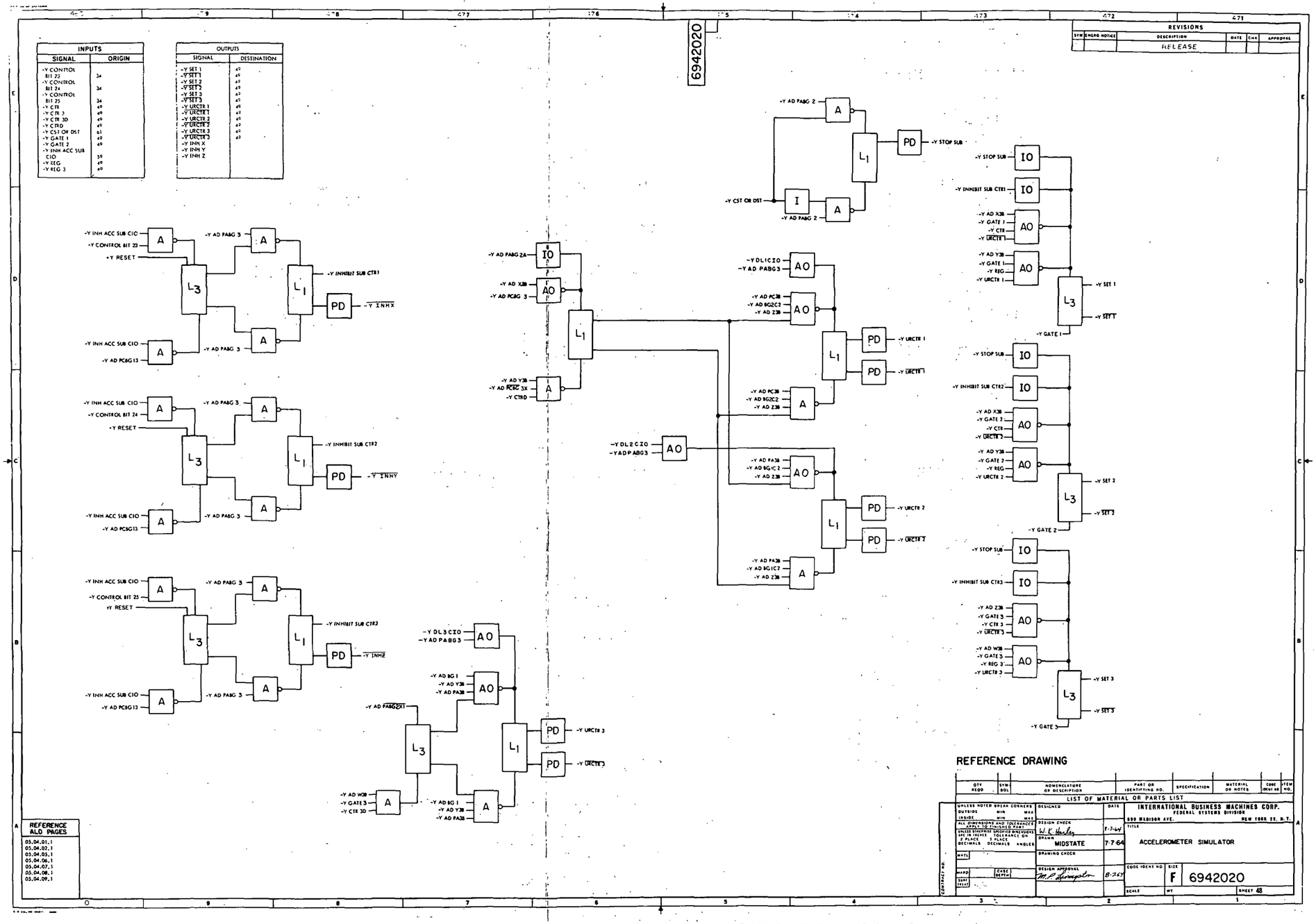

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 50)

INPUTS	
SIGNAL	ORIGIN
-Y LOAD ACCEL DL 1 CIO	59
-Y LOAD ACCEL DL 2 CIO	59
-Y LOAD ACCEL DL 3 CIO	59
-Y MULT DATA	39
-Y PIC ACC	66
-Y SET1	49
-Y SET1	49
-Y SET2	49
-Y SET2	49
-Y SET3	49
-Y SET3	49
-Y URCTR1	49
-Y URCTR1	49
-Y URCTR2	49
-Y URCTR2	49
-Y URCTR3	49
-Y URCTR3	49

OUTPUTS	
SIGNAL	DESTINATION
-Y CTR	48
-Y CTR3	48
-Y CTR 3D	48
-Y CTRD	48
-Y GATE 1	48
-Y GATE 2	48
-Y REG	48
-Y REG3	48

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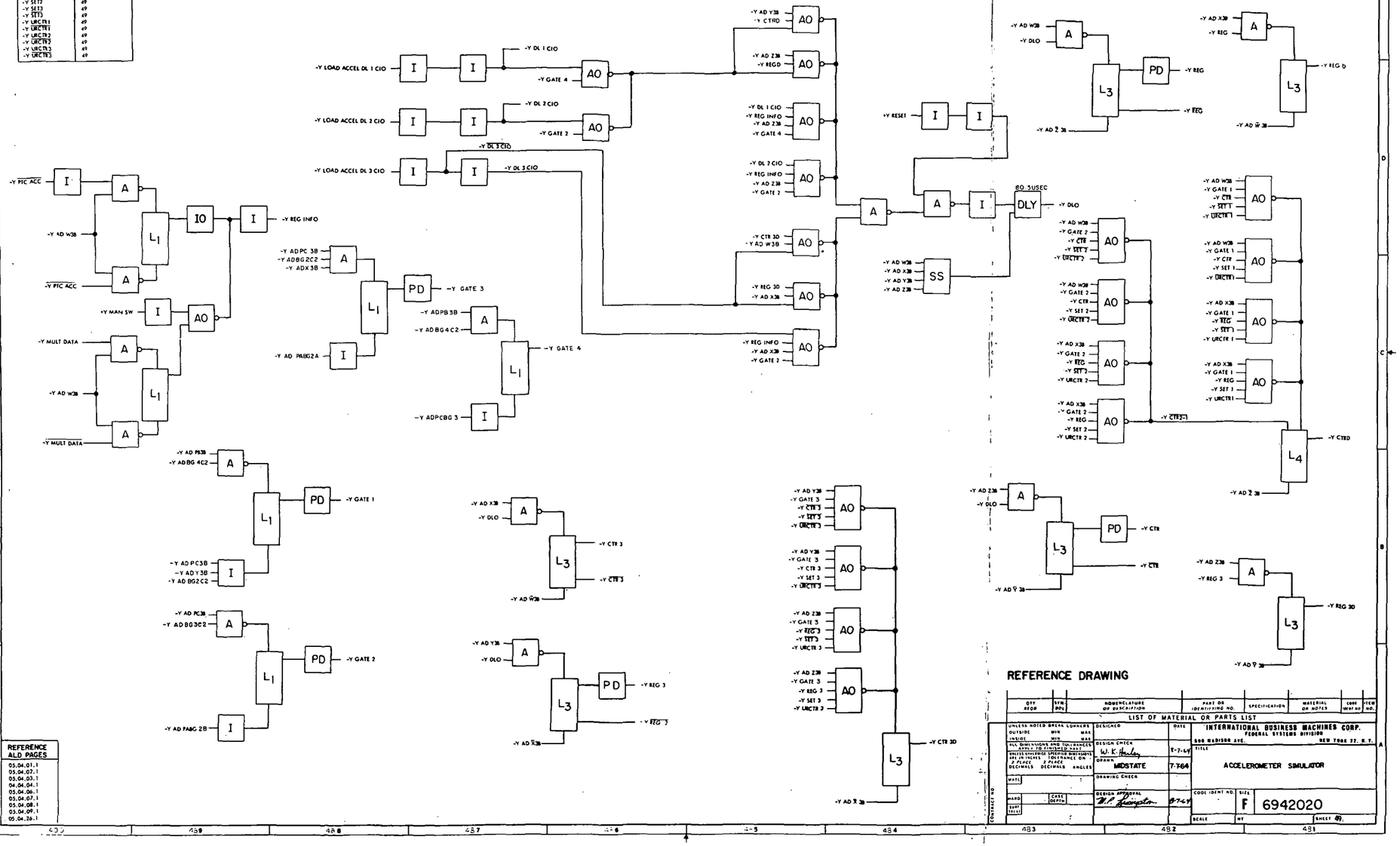
REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
		RELEASE			



REFERENCE ALD PAGES
05.04.01.1
05.04.07.1
05.04.03.1
04.04.04.1
05.04.06.1
05.04.07.1
05.04.08.1
05.04.09.1
05.04.26.1

REFERENCE DRAWING

QTY REQD	SYM. SOL.	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY BEFORE PLATING
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
HARD
SURF FINISH
CASE DEPTH
CONTRACT NO

DESIGNED — DATE
DESIGN CHECK — W. E. Hurley — 8-7-64
DRAWN — MIDSTATE — 7-7-64
DRAWING CHECK
DESIGN APPROVAL — M. P. Crompton — 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: ACCELEROMETER SIMULATOR

CODE IDENT NO. | SIZE F | 6942020

SCALE | WT | SHEET 69

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 51)

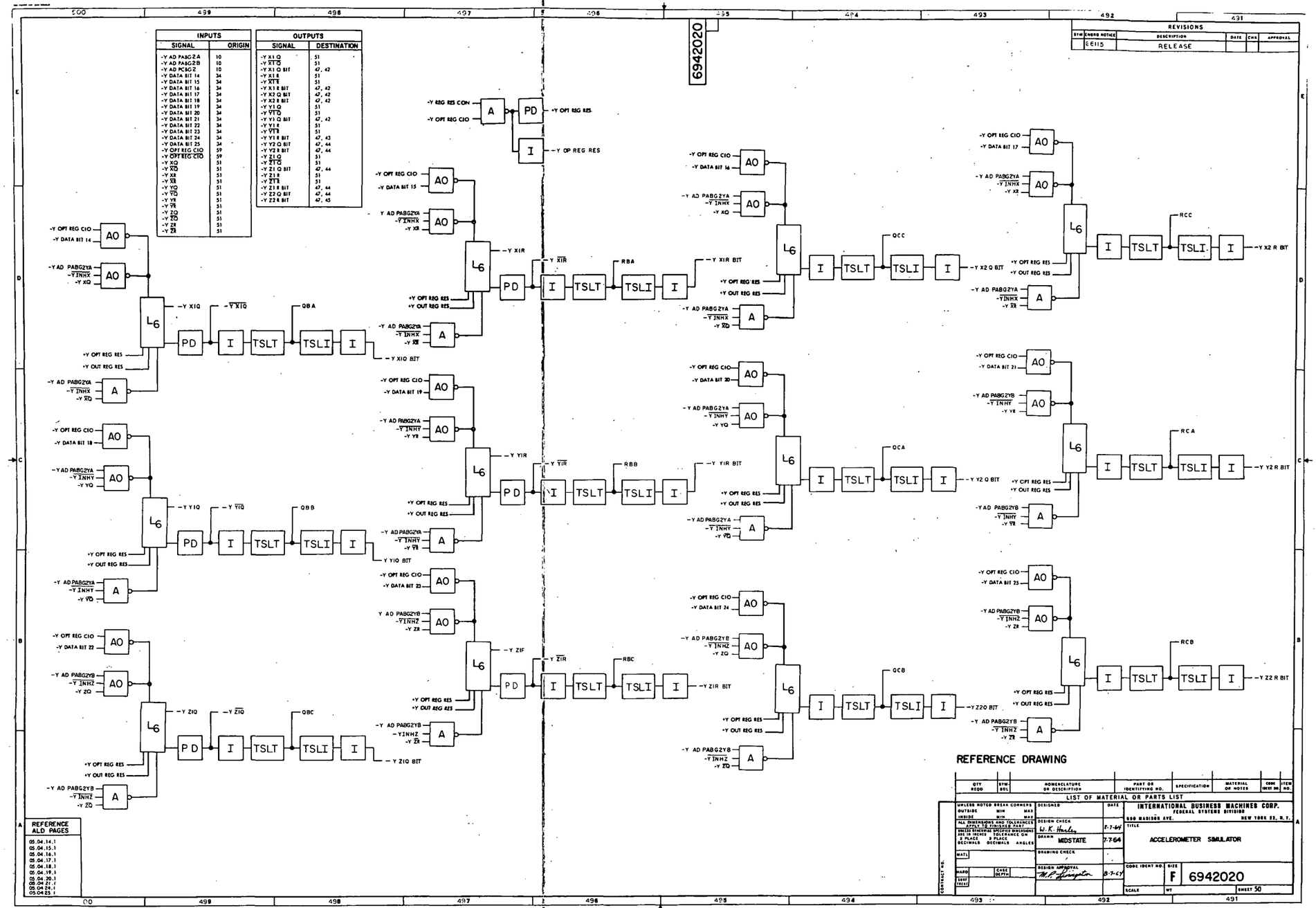


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 52)

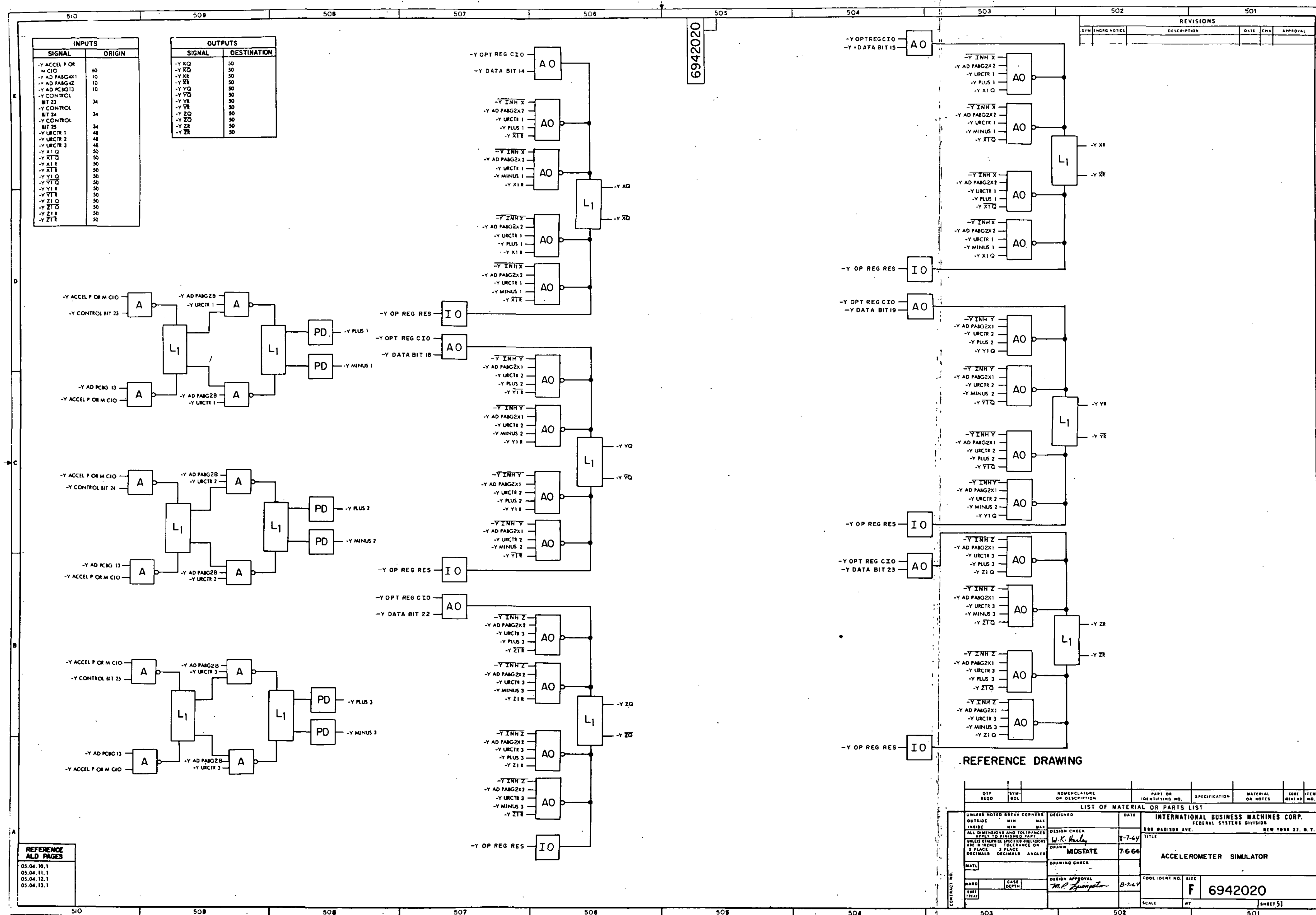


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 53)

INPUTS	
SIGNAL	ORIGIN
-Y BCOS RESET	56
-Y BCOS SET	56
-Y COD RESET A	56
-Y COD RESET B	56
-Y COD SELECT A	56
-Y COD SELECT B	56

OUTPUTS	
SIGNAL	DESTINATION
COD REL 1	56
COD REL 2	56
COD REL 3	56
COD REL 4	56
COD REL 5	56
COD REL 6	56
COD REL 7	56
COD REL 8	56
COD REL 9	56
COD REL 10	56
COD REL 11	56
COD REL 12	56
COD REL 13	56
COD REL 14	56
COD REL 15	56
COD REL 16	56
COD REL 17	56
COD REL 18	56

REFERENCE ALD PAGES
05.07.17.1
05.07.18.1
05.07.19.1
05.07.20.1
06.07.21.1
05.07.22.1
05.07.23.1
05.07.24.1

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REVISIONS

SYM	ENGR NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF FINISH

	DESIGNED	DATE
DESIGN CHECK	W.K. Hadley	7-7-64
DRAWN	MIDSTATE	7-23-64
DRAWING CHECK		
DESIGN APPROVAL	M.F. Livingston	8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
RESOLVER SIMULATORS

CODE IDENT NO. F SIZE 6942020

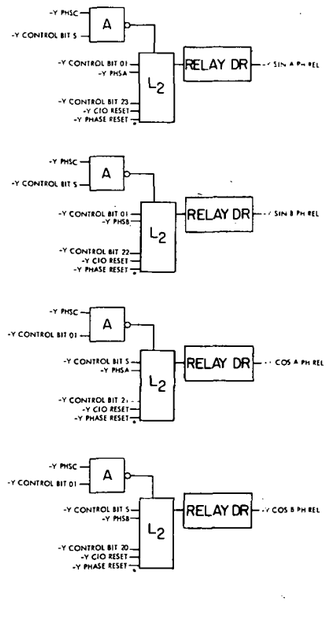
SCALE WT SHEET 52

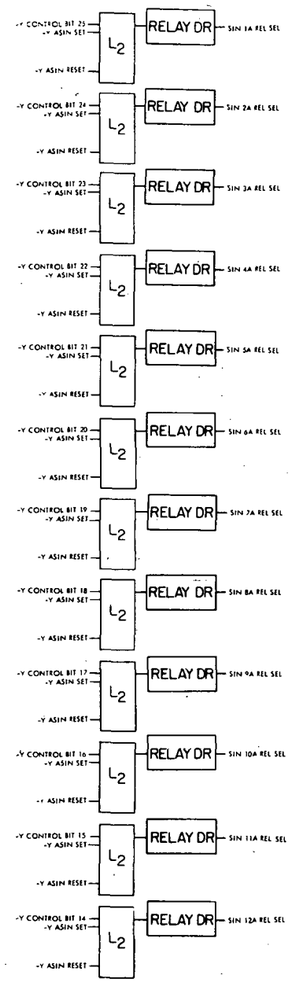
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 54)

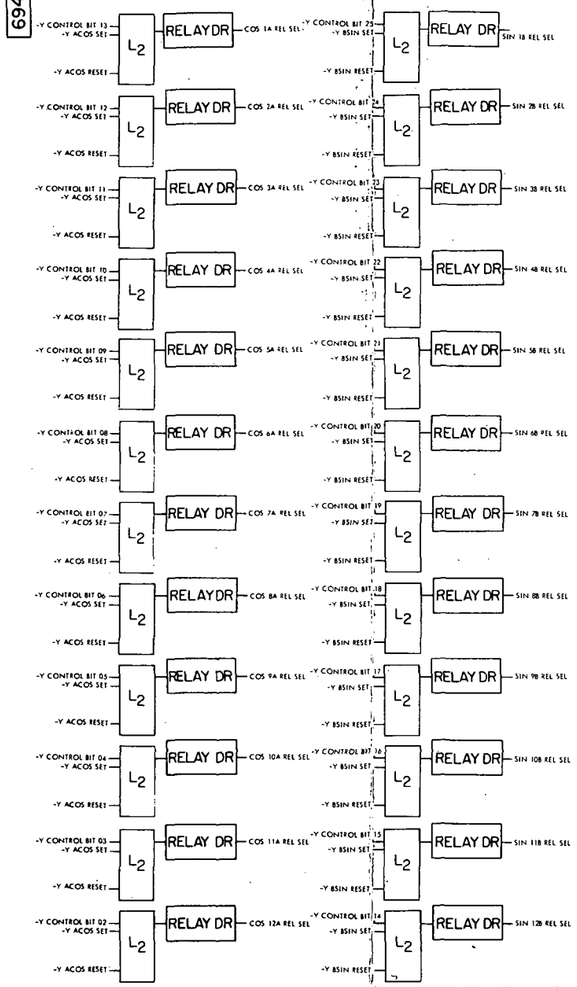
INPUTS	
SIGNAL	ORIGIN
-Y CONTROL BIT 15	34
-Y CONTROL BIT 16	34
-Y CONTROL BIT 17	34
-Y CONTROL BIT 18	34
-Y CONTROL BIT 19	34
-Y CONTROL BIT 20	34
-Y CONTROL BIT 21	34
-Y CONTROL BIT 22	34
-Y CONTROL BIT 23	34
-Y CONTROL BIT 24	34
-Y CONTROL BIT 25	34
-Y PHASE RESET	56
-Y PHSA	56
-Y PHSB	56
-Y PHSC	56

OUTPUTS	
SIGNAL	DESTINATION
-Y COS A PH REL	53
-Y COS B PH REL	53
-Y SIN A PH REL	53
-Y SIN B PH REL	53

INPUTS	
SIGNAL	ORIGIN
-Y ACOS RESET	56
-Y ACOS SET	56
-Y ASIN RESET	56
-Y ASIN SET	56
-Y BSIN RESET	56
-Y BSIN SET	56
-Y CIO RESET	65
-Y CONTROL BIT 5	33
-Y CONTROL BIT 01	33
-Y CONTROL BIT 02	33
-Y CONTROL BIT 03	33
-Y CONTROL BIT 04	33
-Y CONTROL BIT 05	33
-Y CONTROL BIT 06	33
-Y CONTROL BIT 07	33
-Y CONTROL BIT 08	33
-Y CONTROL BIT 09	33
-Y CONTROL BIT 10	33
-Y CONTROL BIT 11	33
-Y CONTROL BIT 12	33
-Y CONTROL BIT 13	34
-Y CONTROL BIT 14	34







REFERENCE ALD PAGES
05.07.05.1
05.07.06.1
05.07.07.1
05.07.08.1
05.07.09.1
05.07.10.1
05.07.11.1
05.07.12.1
05.07.13.1
05.07.14.1
05.07.15.1
05.07.16.1

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES ARE IN INCHES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED DATE
DESIGN CHECK W.K. Hanks 8-7-64
DRAWN MIDSTATE 72364
DRAWING CHECK
DESIGN APPROVAL M.P. Livingston 8-7-64

CONTRACT NO

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
RESOLVER SIMULATORS

CODE IDENT NO | SIZE F | 6942020
SCALE | WT | SHEET 53

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 55)

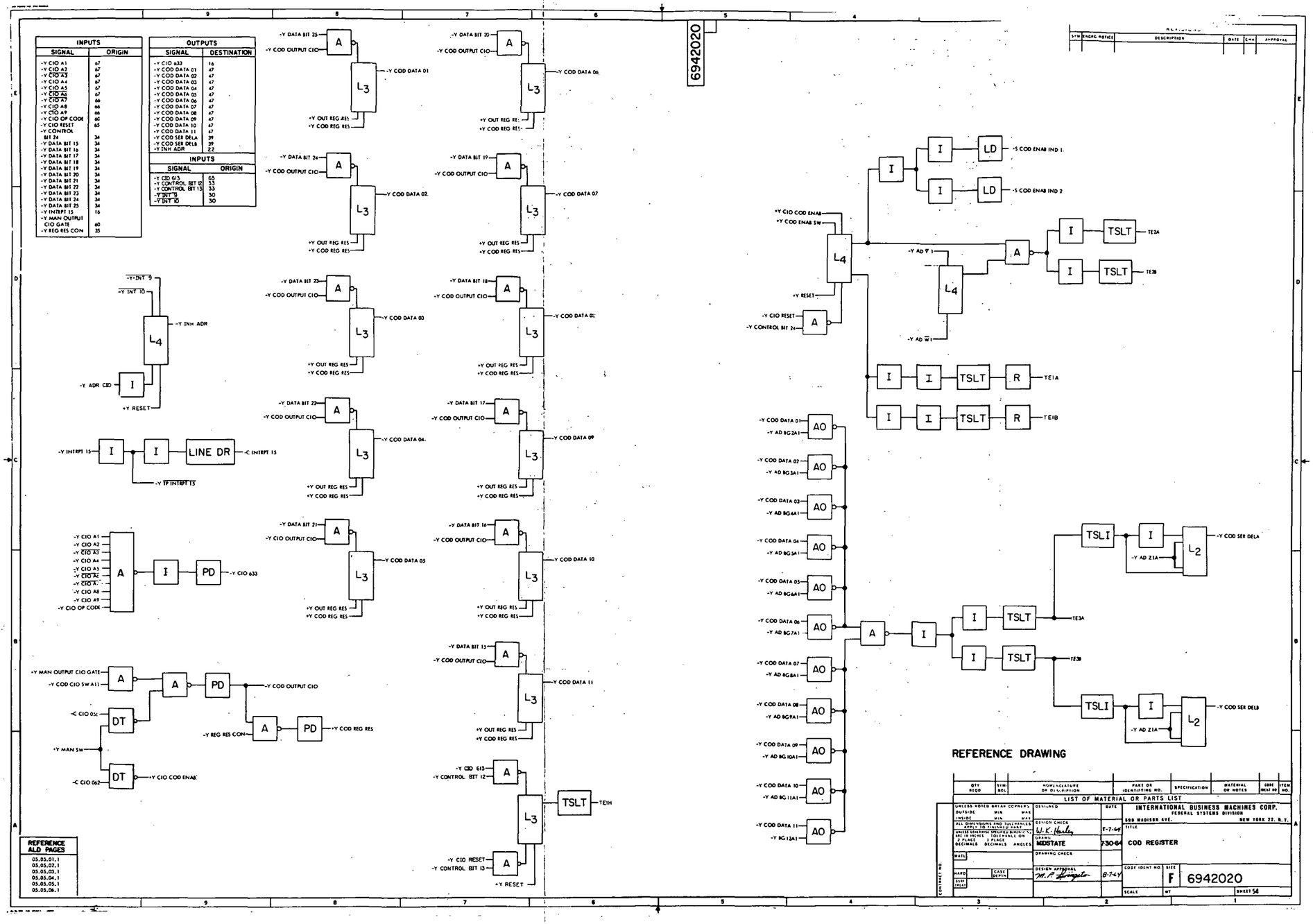
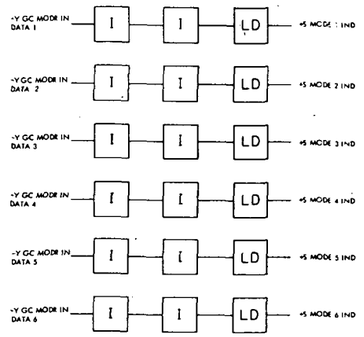
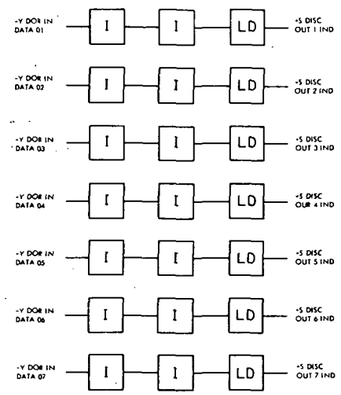


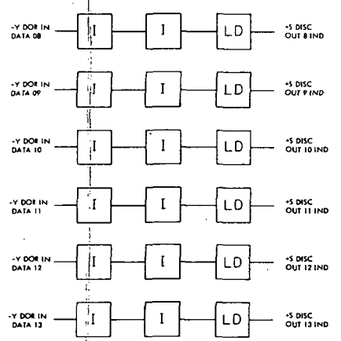
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 56)

6942020

INPUTS	
SIGNAL	ORIGIN
-Y DOR IN DATA 01	71
-Y DOR IN DATA 02	71
-Y DOR IN DATA 03	71
-Y DOR IN DATA 04	71
-Y DOR IN DATA 05	71
-Y DOR IN DATA 06	71
-Y DOR IN DATA 07	71
-Y DOR IN DATA 08	71
-Y DOR IN DATA 09	71
-Y DOR IN DATA 10	71
-Y DOR IN DATA 11	71
-Y DOR IN DATA 12	71
-Y DOR IN DATA 13	71
-Y GC MODR IN DATA 1	71
-Y GC MODR IN DATA 2	71
-Y GC MODR IN DATA 3	71
-Y GC MODR IN DATA 4	71
-Y GC MODR IN DATA 5	71
-Y GC MODR IN DATA 6	71







REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE ALD PAGES
05.15.22.1
05.15.23.1
05.15.24.1

REFERENCE DRAWING

QTY REQD	SYM. SCL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS DIRECTLY TOLERANCED DIMENSIONS ARE TO BE WITHIN
2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±

		DATE
DESIGNED		
DESIGN CHECK	W. K. Hurley	8-7-64
DRAWN	IBM	8-5-64
DRAWING CHECK		
DESIGN APPROVAL	M. Livingston	8-7-64

CONTRACT NO.
HARD / SOFT TREAT / CASE DEPTH

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N. Y.

TITLE
MODE AND DISCRETE OUTPUT DISPLAY

CODE IDENT NO. | SIZE F | 6942020
SCALE | WT | SHEET 55

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 57)

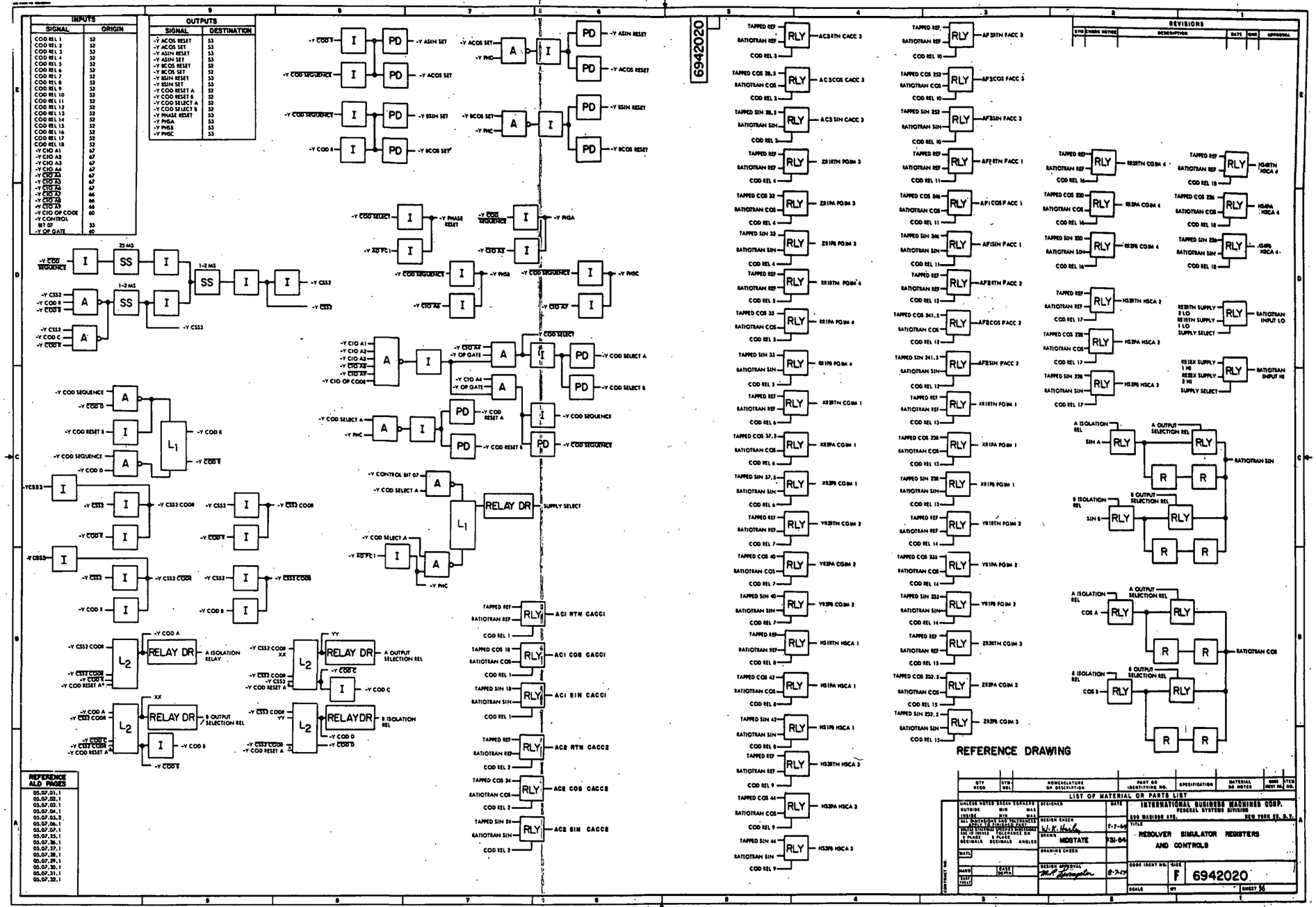


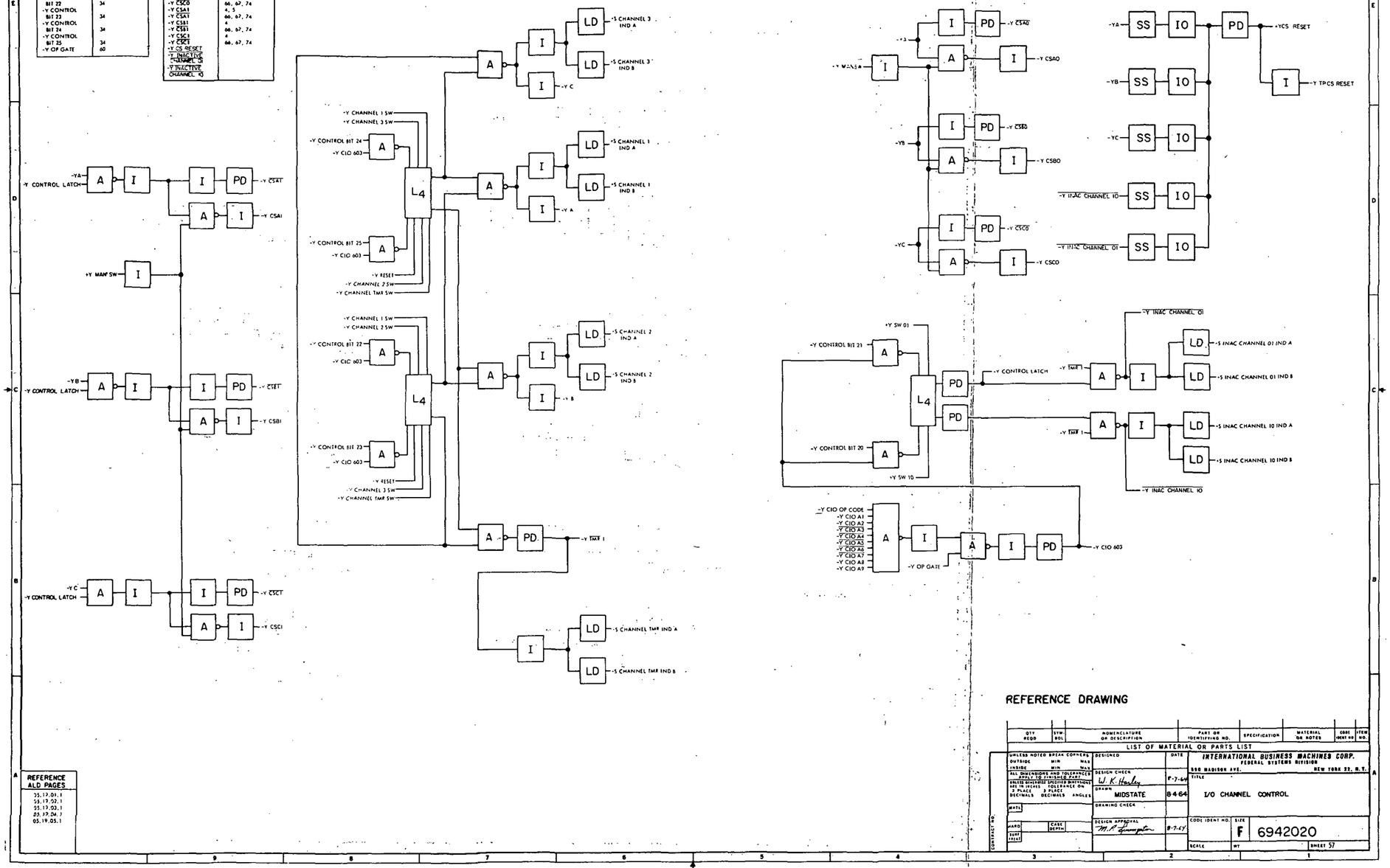
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 58)

6942020

INPUTS	
SIGNAL	ORIGIN
-Y CONTROL BIT 20	34
-Y CONTROL BIT 21	34
-Y CONTROL BIT 22	34
-Y CONTROL BIT 23	34
-Y CONTROL BIT 24	34
-Y CONTROL BIT 25	34
-Y OP GATE	60

OUTPUTS	
SIGNAL	DESTINATION
-Y CSA0	4
-Y CSA0	66, 67, 74
-Y CSB0	4
-Y CSB0	66, 67, 74
-Y CSC0	4
-Y CSC0	66, 67, 74
-Y CSA1	4, 5
-Y CSA1	66, 67, 74
-Y CSB1	4
-Y CSB1	66, 67, 74
-Y CSC1	4
-Y CSC1	66, 67, 74
-Y CS RESET	
-Y INJECTIVE CHANNEL 01	
-Y INJECTIVE CHANNEL 10	

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL



REFERENCE ALD PAGES
55.19.01.1
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05.19.05.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	COST IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS & EDGES .005 MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART AFTER PLATING, COATING, PAINTING, ETC.
2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±30'

DESIGNED		DATE
DESIGN CHECK	W. K. Hurley	9-7-64
DRAWN	MIDSTATE 8464	
DRAWING CHECK		
DESIGN APPROVAL	M. F. Livingston	9-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: I/O CHANNEL CONTROL

CODE IDENT NO. | SIZE F | 6942020

SCALE | WT | SHEET 57

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 59)

INPUTS	
SIGNAL	ORIGIN
-Y MAN MULT LOAD	39

OUTPUTS	
SIGNAL	DESTINATION
-Y ADCO INPUT CIO	40, 42, 43, 44
-Y ADR INPUT CIO	43, 44
-Y CR INPUT CIO	40, 41, 42
-Y DDAS INPUT CIO	40, 41
-Y DIN INPUT CIO	40, 41, 42, 43, 44
-Y DIS INPUT CIO	40, 41
-Y DOR INPUT CIO	40, 41, 42
-Y EM REG INPUT CIO	40, 41, 42, 43
-Y GC INPUT CIO	40, 41, 42
-Y IDDAS INPUT CIO	40, 41, 42
-Y IGCA INPUT CIO	40, 41, 42, 43, 44
-Y IGCB INPUT CIO	40, 41, 42
-Y INT REG INPUT CIO	41, 42
-Y NA DIS INPUT CIO	

OUTPUTS	
SIGNAL	DESTINATION
-Y NA SIM INPUT CIO	43, 44
-Y OOC INPUT CIO	40, 41, 42, 43, 44
-Y OPTISYNS INPUT CIO	44
-Y SSFB INPUT CIO	42, 43, 44
-Y SSR INPUT CIO	41, 42
	40, 41, 42

OUTPUTS	
SIGNAL	DESTINATION
-Y TEL DA INPUT CIO	40, 41, 42, 43, 44
-Y TEL DB INPUT CIO	40, 41, 42
-Y READ ACME	39
-Y READ ACME	39
-Y READ CODA	39
-Y READ CODA	39
-Y READ CODB	39
-Y READ CODB	39

6942020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

-C CIO 003 → DT; +Y MAN SW → DT; -Y MULT IGCA CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y IGCA INPUT CIO

-C CIO 011 → DT; +Y MAN SW → DT; -Y MULT IGCB CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y IGCB INPUT CIO

-C CIO 013 → DT; +Y MAN SW → DT; -Y MULT OOC CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y OOC INPUT CIO

-C CIO 021 → DT; +Y MAN SW → DT; -Y MULT DOR CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y DOR INPUT CIO

-C CIO 025 → DT; +Y MAN SW → DT; -Y MULT ADCO CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y ADCO INPUT CIO

-C CIO 031 → DT; +Y MAN SW → DT; -Y MULT SSR CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y SSR INPUT CIO

-C CIO 035 → DT; +Y MAN SW → DT; -Y MULT TEL DA CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y TEL DA INPUT CIO

-C CIO 041 → DT; +Y MAN SW → DT; -Y MULT TEL DB CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y TEL DB INPUT CIO

-C CIO 045 → DT; +Y MAN SW → DT; -Y MULT IDDAS CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y IDDAS INPUT CIO

-C CIO 051 → DT; +Y MAN SW → DT; -Y MULT NA SIM CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y NA SIM INPUT CIO

-C CIO 055 → DT; +Y MAN SW → DT; -Y MULT SSFB CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y SSFB INPUT CIO

-C CIO 061 → DT; +Y MAN SW → DT; -Y MULT GC CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y GC INPUT CIO

-C CIO 065 → DT; +Y MAN SW → DT; -Y MULT CR CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y CR INPUT CIO

-C CIO 071 → DT; +Y MAN SW → DT; -Y MULT DIN CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y DIN INPUT CIO

-C CIO 075 → DT; +Y MAN SW → DT; -Y MULT DIS CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y DIS INPUT CIO

-C CIO 101 → DT; +Y MAN SW → DT; -Y MULT NA DIS CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y NA DIS INPUT CIO

-C CIO 105 → DT; +Y MAN SW → DT; -Y MULT DDAS CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y DDAS INPUT CIO

-C CIO 111 → DT; +Y MAN SW → DT; -Y MULT EM REG CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y EM REG INPUT CIO

-C CIO 115 → DT; +Y MAN SW → DT; -Y MULT INT REG CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y INT REG INPUT CIO

-C CIO 121 → DT; +Y MAN SW → DT; -Y MULT OPTIS CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y OPTISYNS INPUT CIO

-C CIO 125 → DT; +Y MAN SW → DT; -Y MULT ADR REG CIO SW → A; -Y MAN MULT LOAD → A; DT, A → PD → -Y ADR CIO

-C CIO 131 → DT; +Y MAN SW → DT; DT → I → -Y READ CODA; I → -Y READ CODA

-C CIO 135 → DT; +Y MAN SW → DT; DT → I → -Y READ ACME; I → -Y READ ACME

-C CIO 141 → DT; +Y MAN SW → DT; DT → I → -Y READ CODB; I → -Y READ CODB

REFERENCE ALD PAGES
05.10.23.1
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05.10.27.1

REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	COST (MFG'G)	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS AT PLATED SURFACES TOLERANCE ON DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED — DATE
DESIGN CHECK — U.K. Hurley — 8-7-64
DRAWN — MIDSTATE — 7-27-64
DRAWING CHECK — K.F. — 8-7-64
DESIGN APPROVAL — M. Pennington — 8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
500 MADISON AVE. NEW YORK 22, N.Y.

TITLE: INPUT CIO CODES

CODE IDENT NO. 6942020 SIZE F
SCALE WT SHEET 58

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 60)

INPUTS	
SIGNAL	ORIGIN
-Y ACCEL P OR M SEL	60
-Y INH ACC SUB SEL	60
-Y LOAD ACCEL DL 1 SEL	60
-Y LOAD ACCEL DL 2 SEL	60
-Y LOAD ACCEL DL 3 SEL	60
-Y MAN CIO CYCLE 1	60
-Y MAN CIO CYCLE 2	60
-Y MAN CIO CYCLE 3	60
-Y MAN OUTPUT CIO GATE	60
-Y PIO SEL	60
-Y SAMP RES SEL	60
-Y TEL SAMP SEL	60
-Y RCA SAMP SEL	60

OUTPUTS	
SIGNAL	DESTINATION
-Y ACCEL PR OR M CIO	51
-Y CIO OP CODE	54, 35, 56, 66, 67, 39
-Y CR CIO	36, 35, 62
-Y DIN CIO	38, 35
-Y DIS CIO	38, 35
-Y DDAS CIO	36, 35
-Y DST RES CIO	61
-Y DST SET CIO	61
-Y EM REG CIO	37, 35
-Y ENABLE COMPARE CIO	39
-Y GC CIO	36, 35, 62
-Y HLT RES CIO	61
-Y HLT SET CIO	61
-Y INT REG CIO	37, 35
-Y INH ACC SUB CIO	48
-Y LOAD ACCEL DL 1 CIO	59
-Y LOAD ACCEL DL 2 CIO	59
-Y LOAD ACCEL DL 3 CIO	59
-Y NA DIS CIO	35
-Y OPT REG CIO	50
-Y PIO OP CODE	35, 39
-Y RCA SAMP CIO	62
-Y SAMP RES CIO	62
-Y SSFB CIO	36, 35
-Y TEL SAMP CIO	62
-Y ENABLE COMPARE SEL	
-Y ENABLE COMPARE SEL	60

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05.03.10.1
05.03.11.1
05.03.12.1
05.03.15.1
05.03.16.1
05.03.17.1
05.03.18.1

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (MAT'L)	F/M NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX	DESIGNED	DATE
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES	DESIGN CHECK W.K. Hanley	8-7-69
MATL	DRAWN IBM	7/14/69
HARD CASE DEPTH	DRAWING CHECK	
SURF TREAT	DESIGN APPROVAL M.F. Livingston	8-7-69

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N. Y.

TITLE: CIO-PIO CONTROLS

CONTRACT NO.

CODE IDENT NO. | SIZE F | 6942020

SCALE | WT | SHEET 59

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 61)

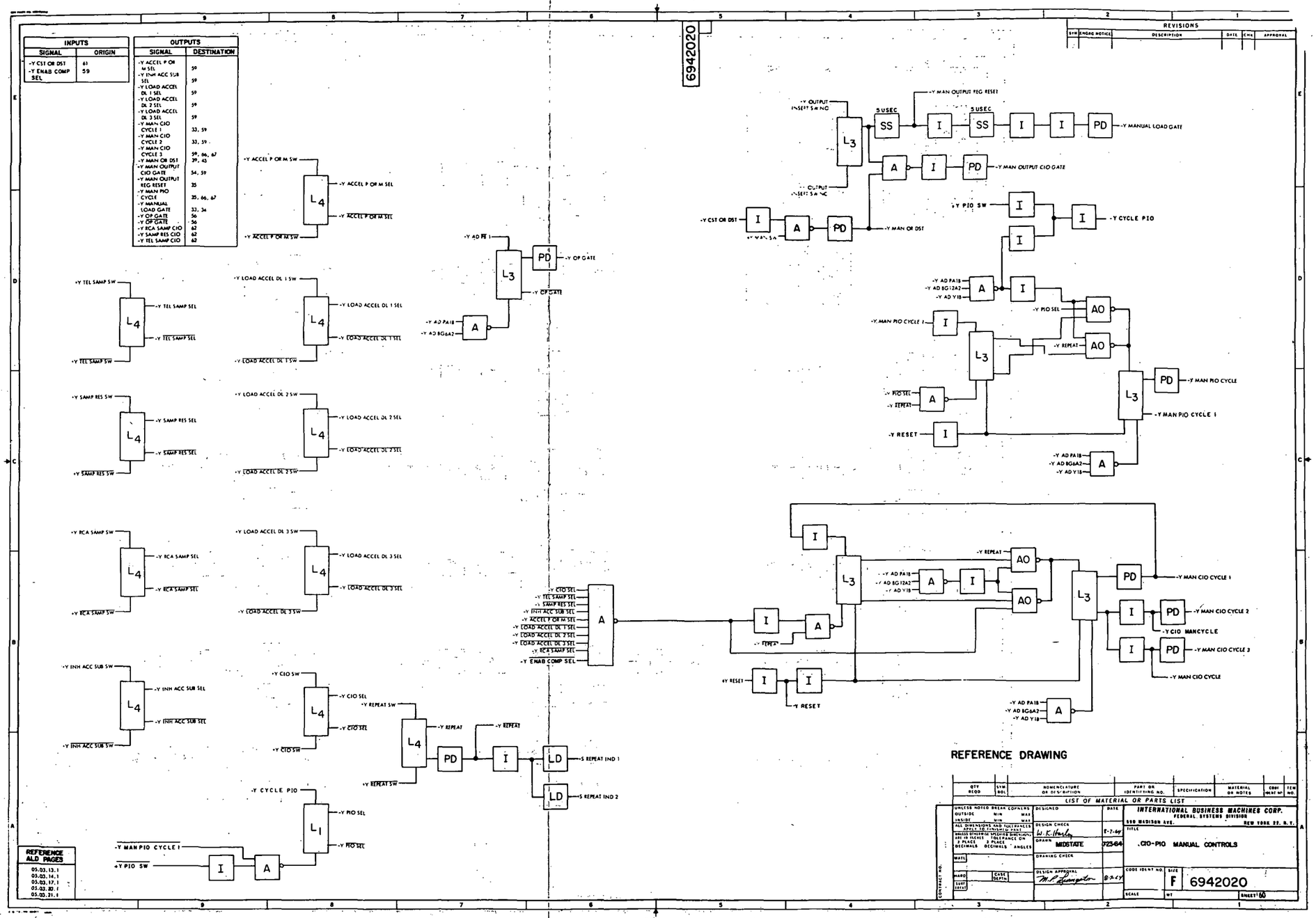


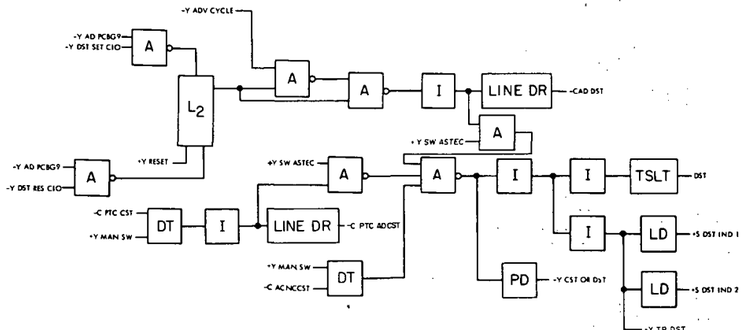
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 62)

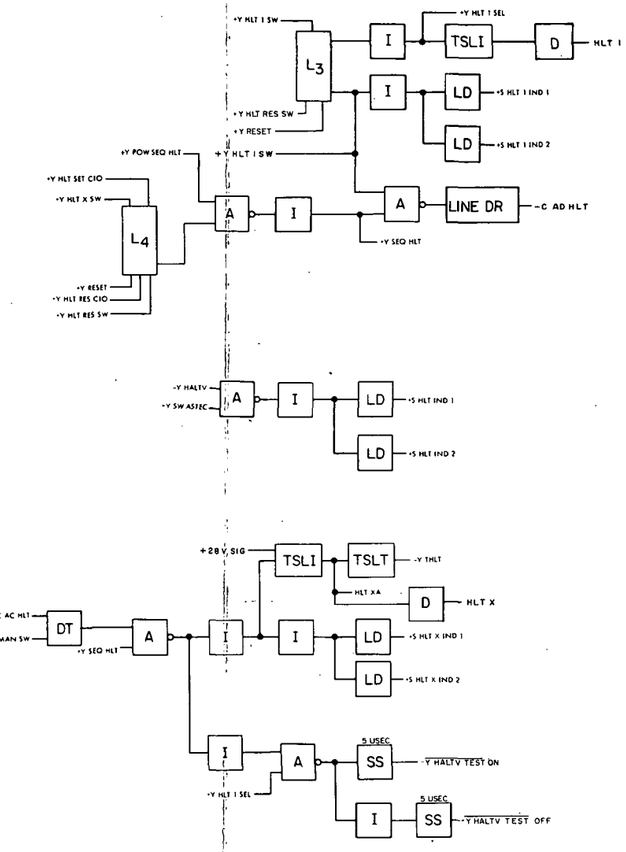
INPUTS	
SIGNAL	ORIGIN
-Y AD PCBG9	10
-Y DST RES CIO	60
-Y DST SET CIO	60
-Y HALTV	18
+Y HLT RES CIO	60
+Y HLT SET CIO	60
-Y POW SEQ HLT	12

OUTPUTS	
SIGNAL	DESTINATION
-Y CST OR DST	60, 48
-Y HALTV TEST	18
-Y TMLT	11
-Y HALTV TEST ON	18
Y HALTV TEST OFF	18

6942020

REVISIONS					
LTR	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL





REFERENCE ALD PAGES
05.01.48.1
05.02.01.1
05.02.02.1
05.02.03.1
05.02.04.1
05.12.20.1

REFERENCE DRAWING

QTY REQD	SYM SHL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ANGLES
MATL
HARD / SOFT (HEAT) CASE DEPTH
CONTRACT NO.

DESIGNED — DATE
DESIGN CHECK — W. E. Hartley — 8-7-64
DRAWN — MIDSTATE — 7-27-64
DRAWING CHECK — 8-7-64
DESIGN APPROVAL — M. P. Symplon — 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: CST, DST, HLT

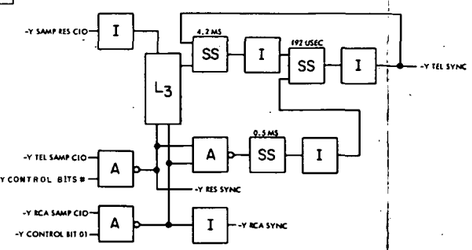
CODE IDENT NO. F — SIZE — 6942020
SCALE — WT — SHEET 61

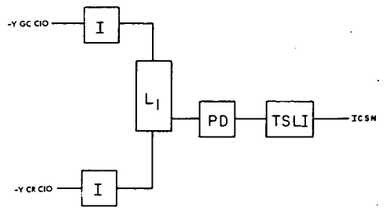
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 63)

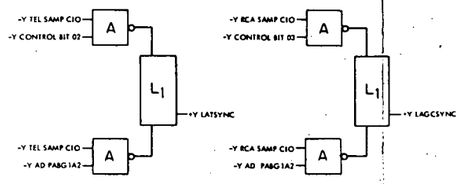
INPUTS	
SIGNAL	ORIGIN
-Y AD PABG1A2	10
-Y CONTROL BIT 5	33
-Y CONTROL BIT 01	33
-Y CONTROL BIT 02	33
-Y CONTROL BIT 03	33
-Y RCA SAMP CIO	60
-Y SAMP RES CIO	60
-Y TEL SAMP CIO	60
-Y CR CIO	59
-Y GC CIO	59

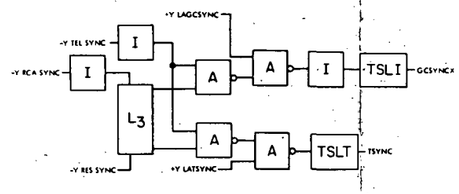
OUTPUTS	
SIGNAL	DESTINATION

6942020









REFERENCE ALD PAGES
05.18.01.1
05.18.02.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD
STRESS RELIEF
CASE DEPTH

DESIGNED
DATE
DESIGN CHECK
DRAWN W. K. Hurley 8-7-64
DRAWING CHECK MIDSTATE 7306
DESIGN APPROVAL M. P. Lincoln 8-24-64

CONTRACT NO

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
TSYNC-GCSYNC-RCA SAMP-TEL SAMP

CODE IDENT NO F 6942020

SCALE WT SHEET 62

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 64)

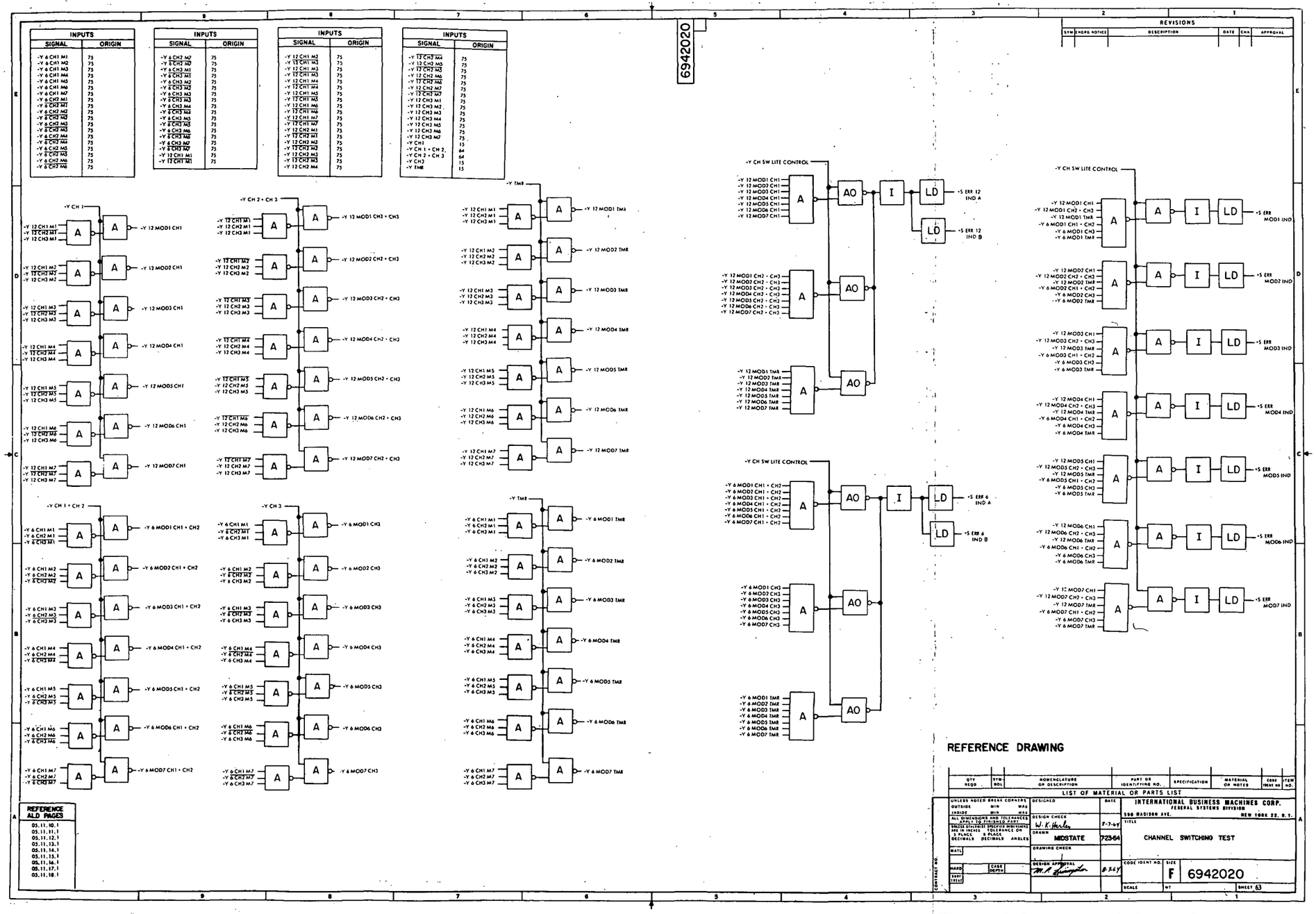


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 65)

INPUTS	
SIGNAL	ORIGIN
-Y 6 CH1 M1	75
-Y 6 CH1 M2	75
-Y 6 CH1 M3	75
-Y 6 CH1 M4	75
-Y 6 CH1 M5	75
-Y 6 CH1 M6	75
-Y 6 CH1 M7	75
-Y 6 CH2 M1	75
-Y 6 CH2 M2	75
-Y 6 CH2 M3	75
-Y 6 CH2 M4	75
-Y 6 CH2 M5	75
-Y 6 CH2 M6	75
-Y 6 CH2 M7	75
-Y 6 CH3 M1	75
-Y 6 CH3 M2	75
-Y 6 CH3 M3	75
-Y 6 CH3 M4	75
-Y 6 CH3 M5	75
-Y 6 CH3 M6	75
-Y 6 CH3 M7	75
-Y 12 CH1 M1	75
-Y 12 CH1 M2	75

INPUTS	
SIGNAL	ORIGIN
-Y 12 CH1 M3	75
-Y 12 CH1 M4	75
-Y 12 CH1 M5	75
-Y 12 CH1 M6	75
-Y 12 CH1 M7	75
-Y 12 CH1 M1	75
-Y 12 CH1 M2	75
-Y 12 CH1 M3	75
-Y 12 CH1 M4	75
-Y 12 CH1 M5	75
-Y 12 CH1 M6	75
-Y 12 CH1 M7	75
-Y 12 CH2 M1	75
-Y 12 CH2 M2	75
-Y 12 CH2 M3	75
-Y 12 CH2 M4	75
-Y 12 CH2 M5	75
-Y 12 CH2 M6	75
-Y 12 CH2 M7	75
-Y 12 CH3 M1	75
-Y 12 CH3 M2	75
-Y 12 CH3 M3	75
-Y 12 CH3 M4	75
-Y 12 CH3 M5	75
-Y 12 CH3 M6	75
-Y 12 CH3 M7	75
-Y CH 1	15
-Y CH 2	15
-Y CH 3	15
-Y CH 1	15

INPUTS	
SIGNAL	ORIGIN
-Y CH 3	15
-Y CIO 613	65
-Y CIO RESET	65
-Y CONTROL BIT 13	34
-Y CONTROL BIT 15	34
-Y TMR	15

OUTPUTS	
SIGNAL	DESTINATION
-Y CH2 + CH3	62
-Y CH1 + CH2	63

6942020

REVISIONS

SYS	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

-Y CIO 613, -Y CONTROL BIT 13 → A; -Y RESET, -Y CIO RESET, -Y CONTROL BIT 15 → A; → L3 → A → PD → -Y CH SW LITE CONTROL; PD → I → PD → -Y TMR ENABLE; -Y SW ADAPT, +Y CH SW TEST MAN

-Y CH 1, -Y CH 2, -Y CH 3, -Y TMR → A → -Y ALL CH ERR ENABLE

-Y 12 CH1 M1 … M7, -Y CH 1, -Y TMR → A → AO; -Y CH SW LITE CONTROL → AO; I → A → I → LD → -S ERR CH 1 IND A; LD → -S ERR CH 1 IND B

-Y 6 CH1 M1 … M7, -Y ALL CH ERR ENABLE → A → AO

-Y 12 CH1 M1 … M7, -Y 13 CH1 M0 → A → AO; -Y CH 2, -Y CH 3 → A → PD → -Y CH 2 + CH 3

-Y 12 CH2 M1 … M7, -Y CH 2, -Y CH 3, -Y TMR → A → AO; -Y CH SW LITE CONTROL → AO; I → A → I → LD → -S ERR CH 2 IND A; LD → -S ERR CH 2 IND B

-Y 6 CH2 M1 … M7, -Y CH 1, -Y CH 2, -Y TMR → A → AO

-Y 12 CH2 M1 … M7, -Y CH 1 → A → AO

-Y 6 CH2 M1 … M7, -Y CH 3 → A → A

-Y 12 CH3 M1 … M7, -Y ALL CH ERR ENABLE → A → AO; -Y CH SW LITE CONTROL → AO; I → A → I → LD → -S ERR CH 3 IND A; LD → -S ERR CH 3 IND B

-Y 6 CH3 M1 … M7, -Y CH 3, -Y TMR → A → AO

-Y 6 CH3 M1 … M7, -Y CH 1, -Y CH 2 → A → PD → -Y CH 1 + CH 2

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05.11.07.1
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05.11.09.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE MFGR NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX; INSIDE MIN MAX; ALL DIMENSIONS AND TOLERANCES ARE IN INCHES; UNLESS OTHERWISE NOTED TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES

MATL

HARD TEST TABLE CASE DEPTH

DESIGNED — DATE

DESIGN CHECK W. K. Hanley 8-7-64

DRAWN IBM 7/16/64

DRAWING CHECK

DESIGN APPROVAL M. P. Livingston 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE., NEW YORK 22, N.Y.

TITLE: CHANNEL SWITCHING TEST

CONTRACT NO.

CODE IDENT NO. | SIZE F | 6942020

SCALE — WT — SHEET 64

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 66)

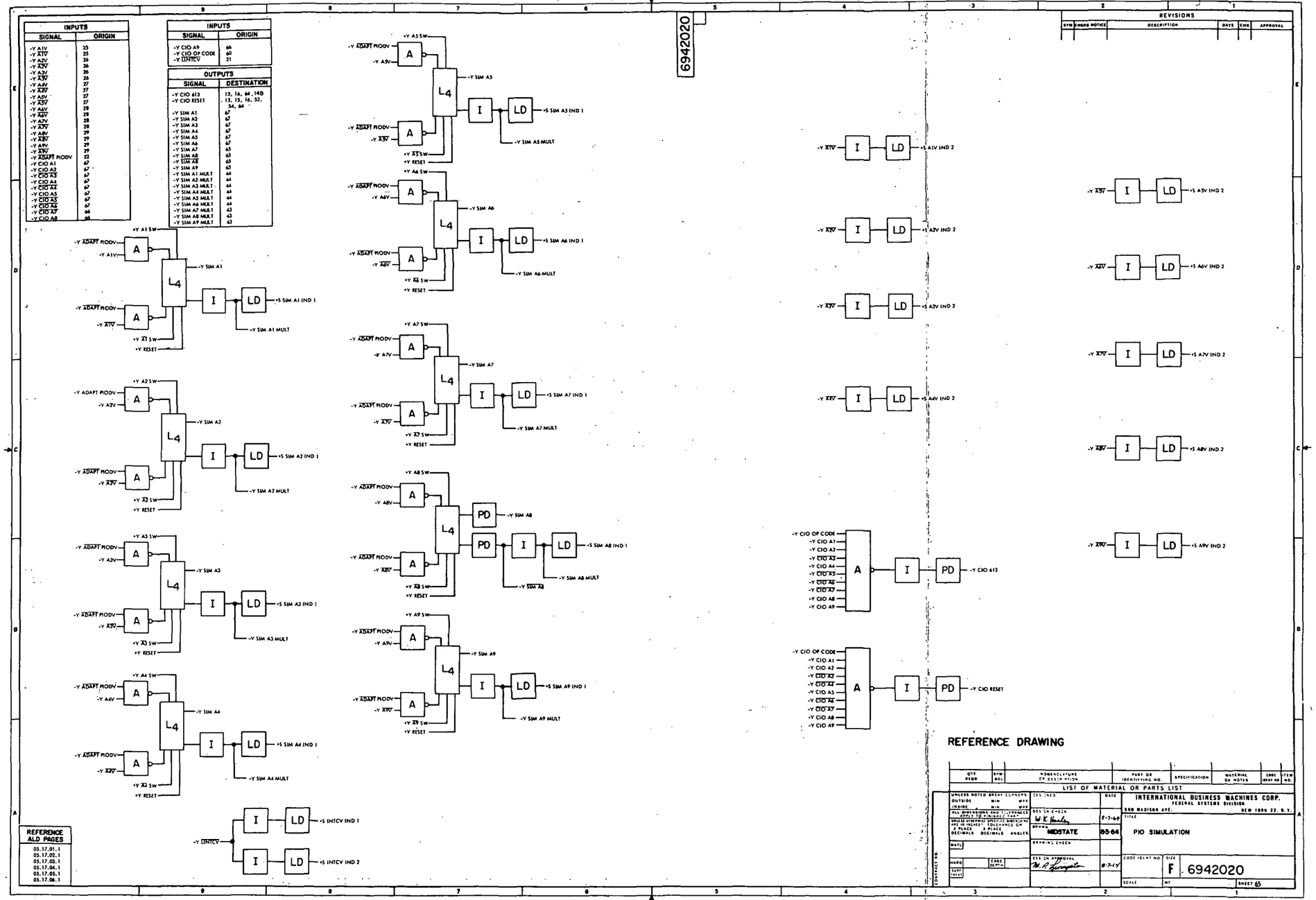
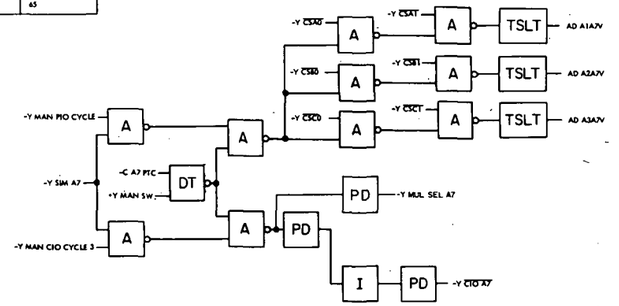
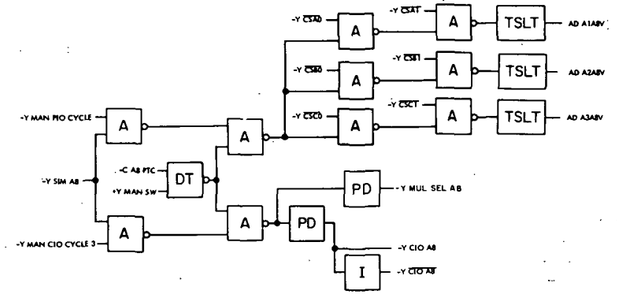


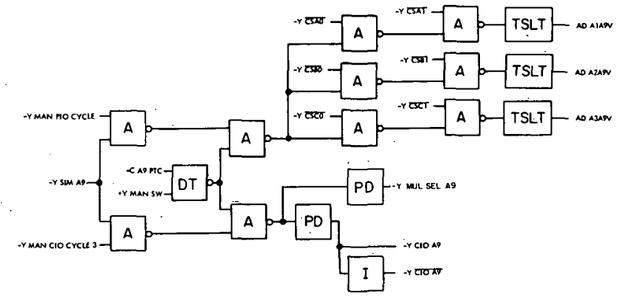
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 67)

INPUTS	
SIGNAL	ORIGIN
-Y AD AA	72
-Y CSA0	57
-Y CSA1	57
-Y CSB0	57
-Y CSB1	57
-Y CSC0	57
-Y CSC1	57
-Y MAN PIO CYCLE	60
-Y MAN CIO CYCLE 3	60
-Y MULT DATA	39
-Y MULT DATA	39
-Y SIM A7	65
-Y SIM A8	65
-Y SIM A8	65
-Y SIM A9	65

OUTPUTS	
SIGNAL	DESTINATION
-Y CIO A7	54
-Y CIO A7	56
-Y CIO A8	54
-Y CIO A8	56
-Y CIO A9	54
-Y CIO A9	56
-Y PTC ACC	39, 49







REFERENCE ALD PAGES
05.16.01.1
05.17.13.1
05.17.14.1
05.17.15.1
05.17.16.1
05.17.17.1

6942020

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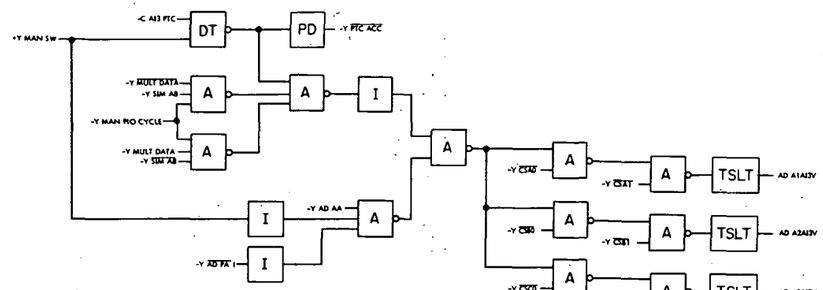
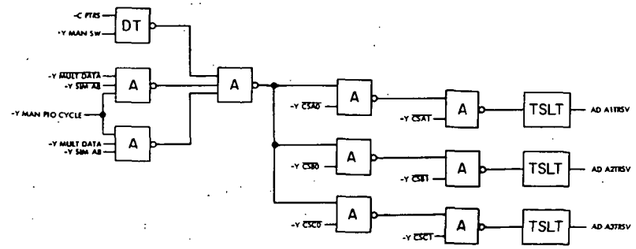
SYM	PUBLG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL





REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE .010 MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED SURFACES ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±1°
MATL
HARD
HEAT TREAT
CASE DEPTH

DESIGNED — DATE
DESIGN CHECK — W. K. Hawley — 7-7-64
DRAWN — MIDSTATE — 7-3-64
DRAWING CHECK
DESIGN APPROVAL — M. P. Knight — 8-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
500 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PIO SIMULATION

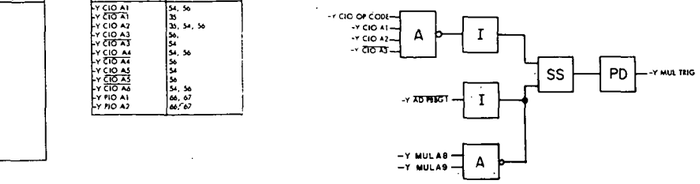
CODE IDENT NO. F — SIZE — 6942020
SCALE — WT — SHEET 66

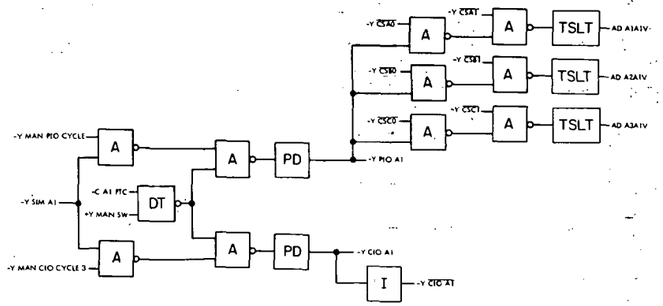
CONTRACT NO.

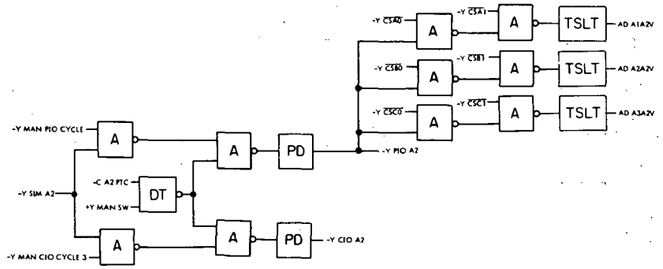
Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 68)

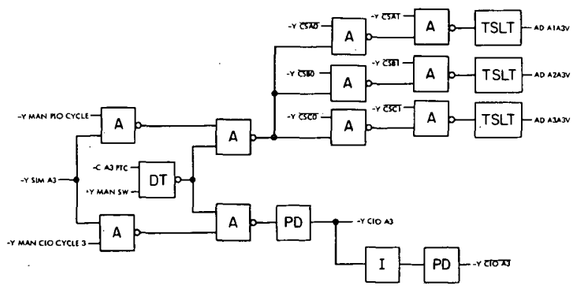
INPUTS	
SIGNAL	ORIGIN
-Y AD PBSG1	10
-Y CIO OP CODE	60
-Y CSA0	57
-Y CSA1	57
-Y CSB0	57
-Y CSB1	57
-Y CSC0	57
-Y CSC1	57
-Y MAN CIO CYCLE 3	60
-Y MAN PIO CYCLE	60
-Y SIM A1	65
-Y SIM A2	65
-Y SIM A3	65
-Y SIM A4	65
-Y SIM A5	65
-Y SIM A6	65

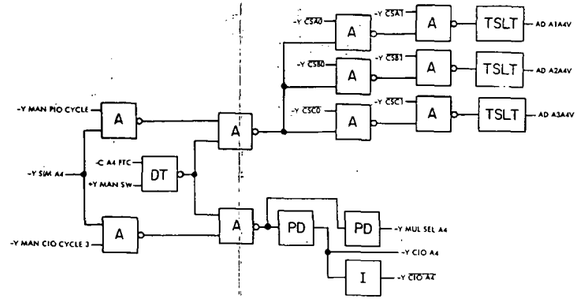
OUTPUTS	
SIGNAL	DESTINATION
-Y CIO A1	54, 56
-Y CIO A1	35
-Y CIO A2	35, 54, 56
-Y CIO A3	56
-Y CIO A3	54
-Y CIO A4	54, 56
-Y CIO A4	56
-Y CIO A5	54
-Y CIO A5	56
-Y CIO A6	54, 56
-Y PIO A1	66, 67
-Y PIO A2	66, 67

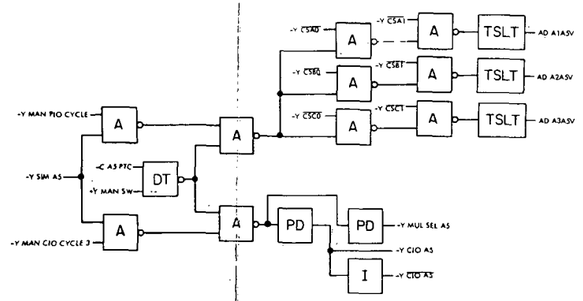


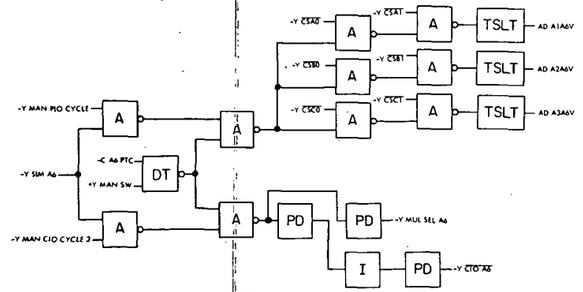












REFERENCE ALD PAGES
05.16.01.1
05.17.07.1
05.17.08.1
05.17.09.1
05.17.10.1
05.17.11.1
05.17.12.1

REFERENCE DRAWING

REVISIONS				
SYM	ENGRG NOTICE	DESCRIPTION	DATE	APP'D

6942020

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CORG SHEET NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS SHARP. OUTSIDE MIN MAX INSIDE MIN MAX. ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ±.03, 3 PLACE DECIMALS ±.010, ANGLES ±1°. MATL. HARD. CASE DEPTH. SOFT. TREAT.

DESIGNED — DATE
DESIGN CHECK W.K. Hurley 8-7-64
DRAWN MIDSTATE 7-31-64
DRAWING CHECK
DESIGN APPROVAL M.J. Thompson 8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PIO SIMULATION

CODE IDENT NO. F — SIZE — 6942020

SCALE — WT — SHEET 67

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 69)

INPUTS	
SIGNAL	ORIGIN
-Y DIN 01	38
-Y DIN 02	38
-Y DIN 03	38
-Y DIN 04	38
-Y DIN 05	38
-Y DIN 06	38
-Y DIN 07	38
-Y DIN 08	38
-Y DIN 09	38
-Y DIN 10	38
-Y DIN 11	38
-Y DIN 12	38
-Y DIN 13	38
-Y DIN 14	38
-Y DIN 15	38
-Y DIN 16	38
-Y DIN 17	38
-Y DIN 18	38
-Y DIN 19	38
-Y DIN 20	38
-Y DIN 21	38
-Y DIN 22	38
-Y DIN 23	38
-Y DIN 24	38
-Y DIN 25	38
-Y DIS 01	38
-Y DIS 02	38
-Y DIS 03	38
-Y EM REG DATA 01	37
-Y EM REG DATA 02	37
-Y EM REG DATA 03	37
-Y EM REG DATA 04	37

INPUTS	
SIGNAL	ORIGIN
-Y EM REG DATA 05	37
-Y EM REG DATA 06	37
-Y EM REG DATA 07	37
-Y EM REG DATA 08	37
-Y EM REG DATA 09	37
-Y EM REG DATA 10	37
-Y EM REG DATA 11	37
-Y EM REG DATA 12	37
-Y EM REG DATA 13	37
-Y EM REG DATA 14	37
-Y EM REG DATA 15	37
-Y EM REG DATA 16	37

6942020

REVISIONS

SYM	ENGR NOTICE	DESCRIPTION	DATE	CHK	APPROVAL

-Y DIN 2B → TSLT → ST A1V4M1
-Y DIN 01 → TSLT → ST A1V4M2
-Y DIN 2A → TSLT → ST A1V4M3
-Y DIN 03 → TSLT → ST A1V4M4
-Y DIN 04 → TSLT → ST A1V4M5
-Y DIN 05 → TSLT → ST A1V4M6
-Y DIN 06 → TSLT → ST A1V4M7
-Y DIN 07 → TSLT → ST A2V4M1
-Y DIN 08 → TSLT → ST A2V4M2
-Y DIN 09 → TSLT → ST A2V4M3
-Y DIN 10 → TSLT → ST A2V4M4
-Y DIN 11 → TSLT → ST A2V4M5
-Y DIN 12 → TSLT → ST A2V4M6

-Y DIN 13 → TSLT → ST A2V4M7
-Y DIN 14 → TSLT → ST A3V4M1
-Y DIN 15 → TSLT → ST A3V4M2
-Y DIN 16 → TSLT → ST A3V4M3
-Y DIN 17 → TSLT → ST A3V4M4
-Y DIN 18 → TSLT → ST A3V4M5
-Y DIN 19 → TSLT → ST A3V4M6
-Y DIN 20 → TSLT → ST A3V4M7
-Y DIN 21 → TSLT → ST A1V5M1
-Y DIN 22 → TSLT → ST A1V5M2
-Y DIN 23 → TSLT → ST A1V5M3
-Y DIN 24 → TSLT → ST A1V5M4
-Y DIN 25 → TSLT → ST A1V5M5

-Y EM REG DATA 01 → TSLT → ST A1V5M6
-Y EM REG DATA 02 → TSLT → ST A1V5M7
-Y EM REG DATA 03 → TSLT → ST A2V5M1
-Y EM REG DATA 04 → TSLT → ST A2V5M2
-Y EM REG DATA 05 → TSLT → ST A2V5M3
-Y EM REG DATA 06 → TSLT → ST A2V5M4
-Y EM REG DATA 07 → TSLT → ST A2V5M5
-Y EM REG DATA 08 → TSLT → ST A2V5M6
-Y EM REG DATA 09 → TSLT → ST A2V5M7
-Y EM REG DATA 10 → TSLT → ST A3V5M1
-Y EM REG DATA 11 → TSLT → ST A3V5M2
-Y EM REG DATA 12 → TSLT → ST A3V5M
-Y EM REG DATA 13 → TSLT → ST A3V5M4
-Y EM REG DATA 14 → TSLT → ST A3V5M5
-Y EM REG DATA 15 → TSLT → ST A3V5M6
-Y EM REG DATA 16 → TSLT → ST A3V5M7

-Y DDAS 01 → TSLT → ST LA1 INTCV
-Y DDAS 02 → TSLT → ST LA2 INTCV
-Y DDAS 03 → TSLT → ST LA3 INTCV
-Y TMR ENABLE → I

-Y TMR ENABLE → I → TSLT → ST A1 INTCV
-Y DDAS 04 → I → TSLT → ST A2 INTCV
-Y DDAS 05 → I → TSLT → ST A3 INTCV
-Y DDAS 06 → I → TSLT → ST A1 HALTV
-Y DDAS 07 → I → TSLT → ST A2 HALTV
-Y DDAS 08 → I → TSLT → ST A3 HALTV
-Y DDAS 09 → I

STHERM 3 → R
ST STHERM 3 → R
STHERM 4 → R
ST STHERM 3 TEST → R

STHERM 1 → R
ST STHERM 1 → R
STHERM 2 → R
ST STHERM 1 TEST → R

ST STHERN 1D → R
ST STHERN 2D → R
ST STHERM 1D TEST → R

ST STHERM 3D → R
ST STHERM 4D → R
ST STHERM 3D TEST → R

EP5 → R
EP8 → R
EP9 → R
EP10 → R
EP11 → R
EP12 → R
EP13 → R
A1 TLC → R
A2 TLC → R

A3 TLC → R
A1 EAM → R
A2 EAM → R
A3 EAM → R
A1 EBM → R
A2 EBM → R
A3 EBM → R
A1 PIOV → R
A2PIOV → R

A3 PIOV → R
EP1 → R
EP2 → R
EP3 → R
EP4 → R
EP6 → R
EP7 → R

REFERENCE ALD PAGES
05.13.01.1
05.13.02.1
05.13.03.1
05.13.04.1
05.29.01.1

REFERENCE DRAWING

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST.

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED — DATE
DESIGN CHECK W. K. Hurley 8-7-64
DRAWN MIDSTATE 73064
DRAWING CHECK
DESIGN APPROVAL M. A. Livingston 8-7-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
500 MADISON AVE. NEW YORK 22, N.Y.

TITLE: SELF CHECK

CODE IDENT NO. | SIZE F | 6942020

SCALE | WT | SHEET 68

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 70)

INPUTS	
SIGNAL	ORIGIN
-Y MW	4
-Y MX	4
-Y MY	4
-Y MZ	4
+Y OVERLAP MC LATCH	70
-Y OVERLAP SC LATCH	70

OUTPUTS	
SIGNAL	DESTINATION
-Y MISSING MC	70
-Y MISSING SC	70
-Y MISSING MC LATCH	70
-Y MISSING SC LATCH	70
-Y SCMC A	70
-Y SCMC $\bar{A}$	70
-Y SCMC B	70
-Y SCMC $\bar{B}$	70
-Y SCSC A	70
-Y SCSC $\bar{A}$	70
-Y SCSC B	70
-Y SCSC $\bar{B}$	70
-Y SCWF1 A	70
-Y SCWF1 B	70
-Y SCXF1 A	70
-Y SCXF1 B	70
-Y SCYF1 A	70
-Y SCYF1 B	70
-Y SCZFMA	70
-Y SCZF1 B	70

SOURCE OF SUPPLY: VENDOR | VENDOR ADDRESS | VENDOR CODE | VENDOR CAT. OR P.N.

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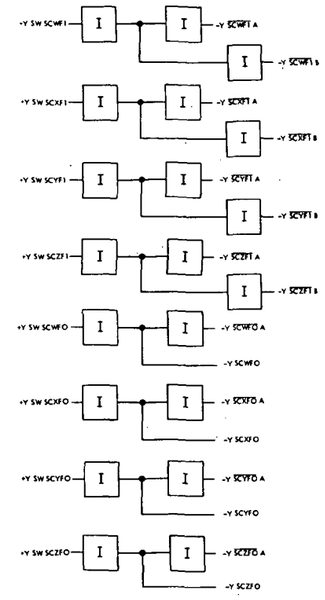
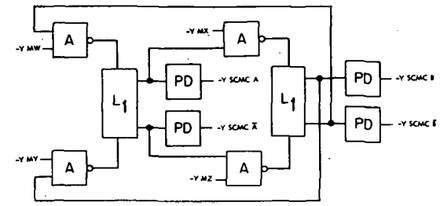
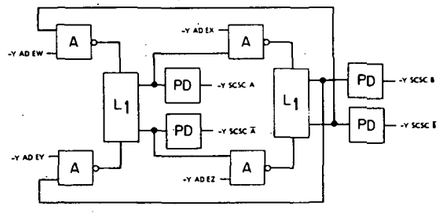
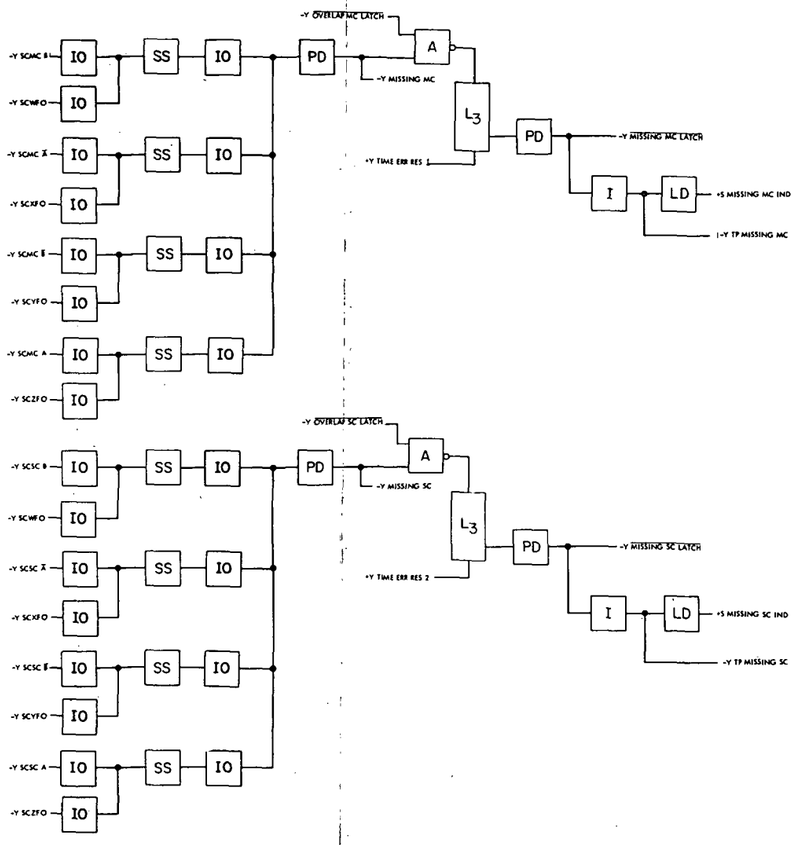
REVISIONS: SYM | ENGRG NOTICE | DESCRIPTION | DATE | CHK | APPROVAL









REFERENCE ALD PAGES
05.01.15.1
05.01.16.1
05.01.38.1
05.01.39.1
05.01.40.1

REFERENCE DRAWING

QTY REQD	SYM DES	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE INDEX NO.	ITEM NO.

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COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

SPEC NUMBER | NOTE | ITEM NO. APPLIES TO — APPLICABLE IBM SPEC — CHECK BLOCK ☒ IF APPLICABLE

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG N-NO QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED DIMENSIONS AT LEFT APPLY TO SOURCE ON THIS DRAWING

	DECIMALS	DECIMALS	ANGLES
MATL			
HARD		CASE DEPTH	
TEST (YEAR)			

		DATE
DESIGNED		
DESIGN CHECK	W. K. Hurley	9-7-64
DRAWN	MIDSTATE	7/1/64
DRAWING CHECK		
DESIGN APPROVAL	W. A. Livingston	9-7-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: CLOCK SELF CHECK

CODE IDENT NO. | SIZE: F | DRAWING NO.: 6942020

SCALE | WT | SHEET 69

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 71)

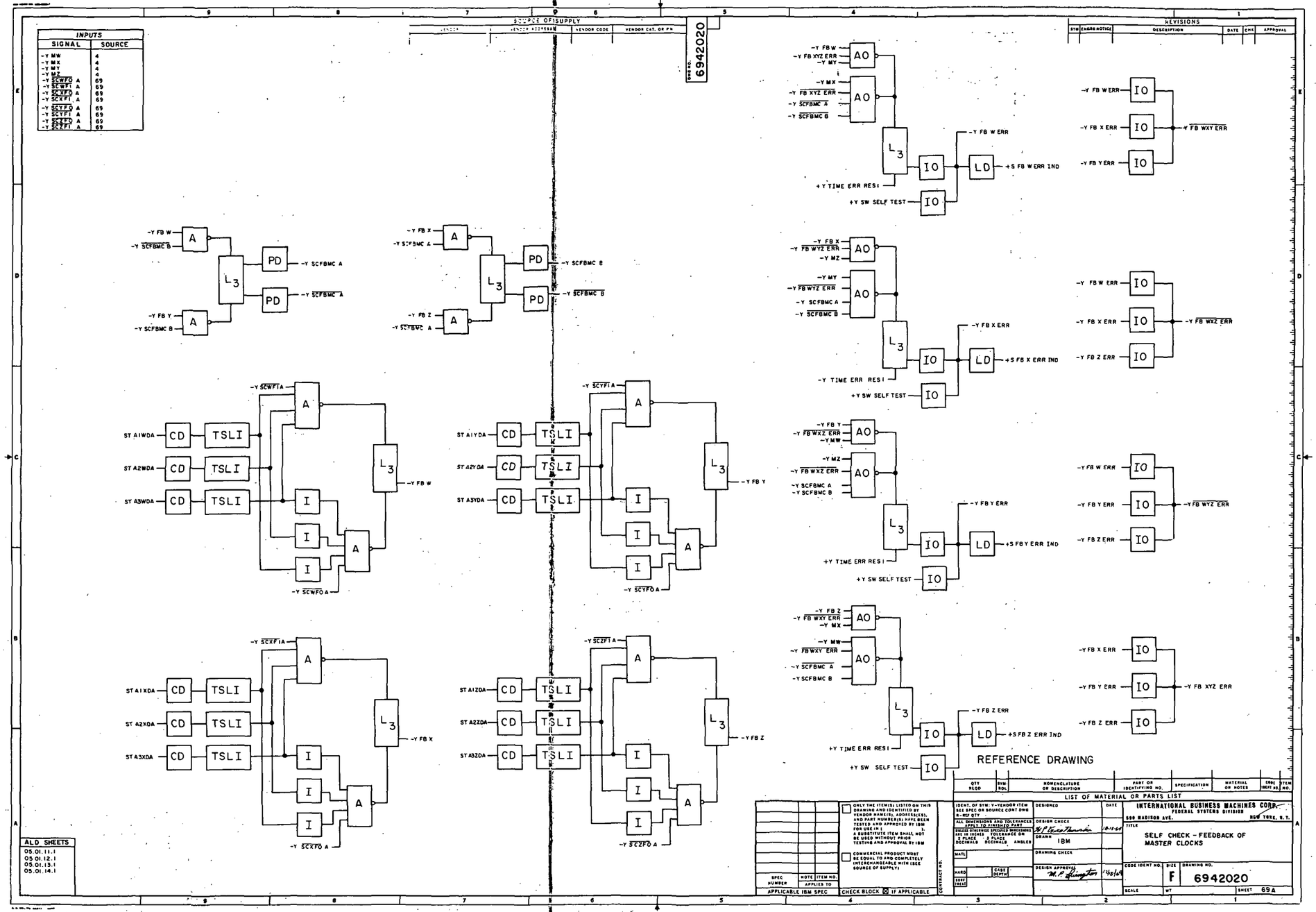

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 72)

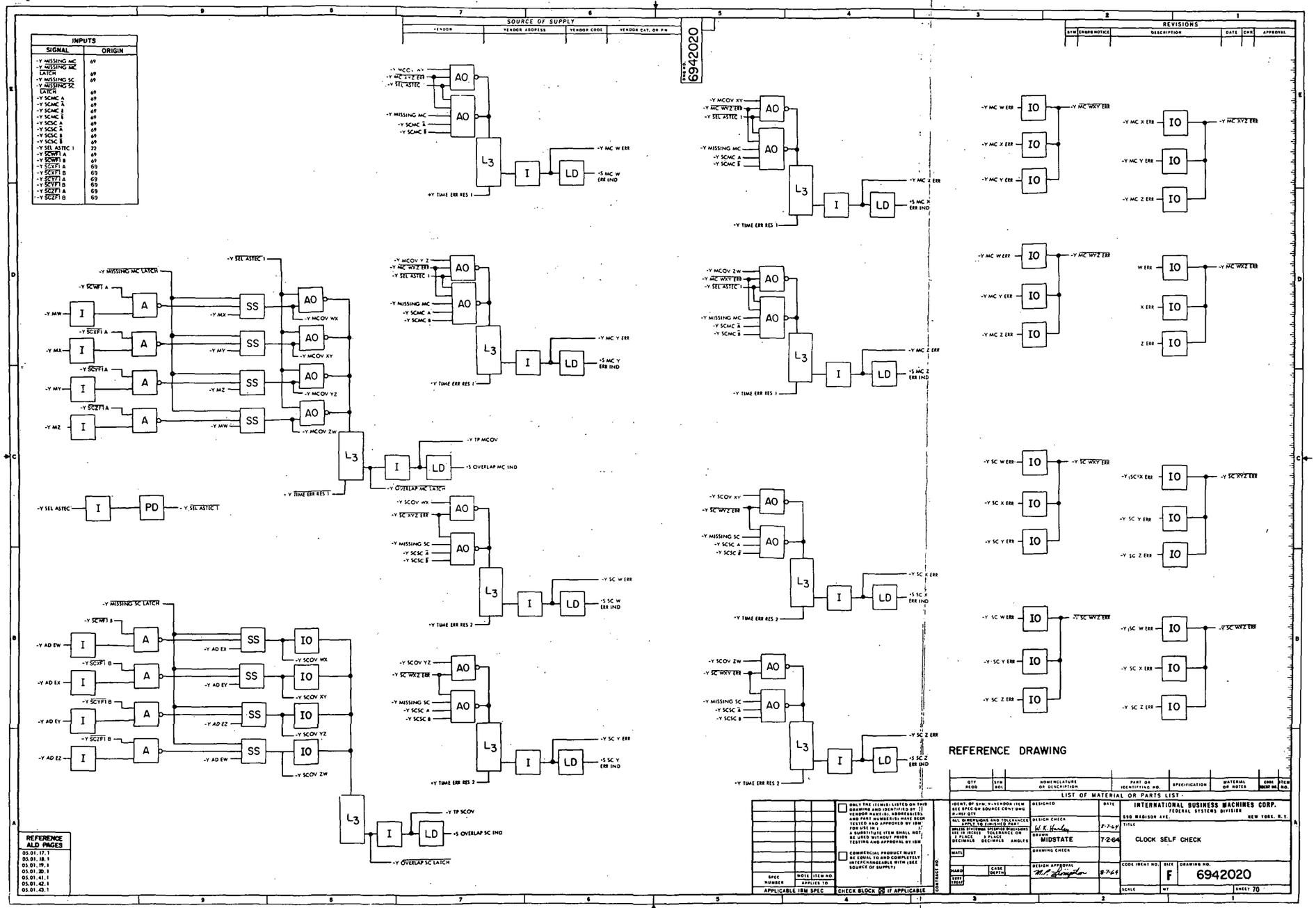

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 73)

OUTPUTS	
SIGNAL	DESTINATION
-Y DDAS IN DATA 12	42
-Y DDAS IN DATA 13	42
-Y DDAS IN DATA 14	42
-Y DDAS IN DATA 15	42
-Y DDAS IN DATA 16	42
-Y DDAS IN DATA 17	41
-Y DDAS IN DATA 18	41
-Y DDAS IN DATA 19	41
-Y DDAS IN DATA 20	41
-Y DDAS IN DATA 21	41
-Y DDAS IN DATA 22	40
-Y DDAS IN DATA 23	40
-Y DDAS IN DATA 24	40
-Y DDAS IN DATA 25	40
-Y DDAS IN DATA 26	40
-Y DOR IN DATA 01	42, 55
-Y DOR IN DATA 02	42, 55
-Y DOR IN DATA 03	42, 55
-Y DOR IN DATA 04	41, 55
-Y DOR IN DATA 05	41, 55
-Y DOR IN DATA 06	41, 55
-Y DOR IN DATA 07	41, 55
-Y DOR IN DATA 08	41, 55
-Y DOR IN DATA 09	40, 55
-Y DOR IN DATA 10	40, 55
-Y DOR IN DATA 11	40, 55
-Y DOR IN DATA 12	40, 55
-Y DOR IN DATA 13	40, 55
-Y D01RCA IN	42
-Y D02RCA IN	42
-Y GC A IN DATA 01	44
-Y GC A IN DATA 02	44
-Y GC A IN DATA 03	44
-Y GC A IN DATA 04	44
-Y GC A IN DATA 05	44
-Y GC A IN DATA 06	44
-Y GC A IN DATA 07	43
-Y GC A IN DATA 08	43
-Y GC A IN DATA 09	43
-Y GC A IN DATA 10	43
-Y GC A IN DATA 11	43
-Y GC A IN DATA 12	42
-Y GC A IN DATA 13	42
-Y GC A IN DATA 14	42
-Y GC A IN DATA 15	42
-Y GC A IN DATA 16	42
-Y GC A IN DATA 17	41
-Y GC A IN DATA 18	41
-Y GC A IN DATA 19	41
-Y GC A IN DATA 20	41
-Y GC A IN DATA 21	41
-Y GC A IN DATA 22	40
-Y GC A IN DATA 24	40
-Y GC A IN DATA 25	40
-Y GC A IN DATA 26	40
-Y GC MODR IN DATA 1	41, 55
-Y GC MODR IN DATA 2	40, 55
-Y GC MODR IN DATA 3	40, 55
-Y GC MODR IN DATA 4	40, 55

OUTPUTS	
SIGNAL	DESTINATION
-Y GC MODR IN DATA 5	40, 55
-Y GC MODR IN DATA 6	40, 55
-Y GC TAGR IN DATA 1	42
-Y GC TAGR IN DATA 2	42
-Y GC TAGR IN DATA 3	42
-Y GC TAGR IN DATA 4	42
-Y GC TAGR IN DATA 5	42
-Y GC TAGR IN DATA 6	41
-Y GC TAGR IN DATA 7	41
-Y GC TAGR IN DATA 8	41
-Y NA SIM IN DATA 01	44
-Y NA SIM IN DATA 02	44
-Y NA SIM IN DATA 03	44
-Y NA SIM IN DATA 04	44
-Y NA SIM IN DATA 05	44
-Y NA SIM IN DATA 06	44
-Y NA SIM IN DATA 07	43
-Y NA SIM IN DATA 08	43
-Y NA SIM IN DATA 09	43
-Y NA SIM IN DATA 10	43
-Y NA SIM IN DATA 11	43
-Y NA SIM IN DATA 12	42
-Y NA SIM IN DATA 13	42
-Y NA SIM IN DATA 14	42
-Y NA SIM IN DATA 15	42
-Y NA SIM IN DATA 16	42
-Y NA SIM IN DATA 17	41
-Y NA SIM IN DATA 18	41
-Y NA SIM IN DATA 19	41
-Y NA SIM IN DATA 20	41
-Y NA SIM IN DATA 21	41
-Y NA SIM IN DATA 22	40
-Y NA SIM IN DATA 23	40
-Y NA SIM IN DATA 24	40
-Y NA SIM IN DATA 25	40
-Y NA SIM IN DATA 26	40
-Y OOC IN DATA 01	44
-Y SSR IN DATA 01	42
-Y SSR IN DATA 02	42
-Y SSR IN DATA 03	42
-Y SSR IN DATA 04	42
-Y SSR IN DATA 05	42
-Y SSR IN DATA 06	41
-Y SSR IN DATA 07	41
-Y SSR IN DATA 08	41
-Y SSR IN DATA 09	41
-Y SSR IN DATA 10	41
-Y SSR IN DATA 11	40
-Y SSR IN DATA 12	40
-Y SSR IN DATA 13	40
-Y SSR IN DATA 14	40
-Y SSR IN DATA 15	40
-Y TEL DA I DATA 01	71
-Y TEL DA I DATA 02	71
-Y TEL DA I DATA 03	71
-Y TEL DA I DATA 04	71
-Y TEL DA I DATA 05	71
-Y TEL DA I DATA 06	71
-Y TEL DA I DATA 07	71
-Y TEL DA I DATA 08	71
-Y TEL DA I DATA 09	71
-Y TEL DA I DATA 10	71
-Y TEL DA I DATA 11	71
-Y TEL DA I DATA 12	71
-Y TEL DA I DATA 13	71
-Y TEL DA I DATA 14	71
-Y TEL DA I DATA 15	71
-Y GC RTR IN DATA 1	41

OUTPUTS	
SIGNAL	DESTINATION
-Y TEL DA I DATA 16	71
-Y TEL DA I DATA 17	71
-Y TEL DA I DATA 18	71
-Y TEL DA I DATA 19	71
-Y TEL DA I DATA 20	71
-Y TEL DA I DATA 21	71
-Y TEL DA I DATA 22	71
-Y TEL DA I DATA 23	71
-Y TEL DA I DATA 24	71
-Y TEL DA I DATA 25	71
-Y TEL DA I DATA 26	71
-Y TEL RTR IN DATA 1	71
-Y TEL RTR IN DATA 2	71
-Y TEL RTR IN DATA 3	71
-Y TEL RTR IN DATA 4	71
-Y TEL RTR IN DATA 5	71
-Y TEL TAGR IN DATA 1	71
-Y TEL TAGR IN DATA 2	71
-Y TEL TAGR IN DATA 3	71
-Y TEL TAGR IN DATA 4	71
-Y TEL TAGR IN DATA 5	71
-Y TEL TAGR IN DATA 6	71
-Y TEL TAGR IN DATA 7	71
-Y TEL TAGR IN DATA 8	71
-Y TEL TPB IN DATA 1	71

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05.10.40.1

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MATL

HARD / SOFT (HEAT) CASE DEPTH

CONTRACT NO

DESIGNED — DATE

DESIGN CHECK — W.K. Healey — 8-7-69

DRAWN — MIDSTATE — 7-30-69

DRAWING CHECK

DESIGN APPROVAL — M.P. Brumpton — 8-7-69

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: DA INPUTS

CODE IDENT NO. | SIZE: F | 6942020

SCALE | WT | SHEET 71

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 74)

INPUTS	
SIGNAL	ORIGIN
+Y CR DATA 01 thru 14	36
+Y DDAS DATA 01 thru 16	36
+Y DIN DATA 03 thru 26	38
+Y DIS DATA 01 thru 08	38
+Y GC DATA 01 thru 14	36
+Y INTREG DATA 01 thru 10	37
+Y SSFB DATA 01 thru 08	36
+Y DIN DATA 01	38
+Y DIN DATA 2A	38
+Y DIN DATA 28	38

OUTPUTS	
SIGNAL	DESTINATION
CR1 thru CR14	73
CR11X	73
CR12X	73
DIN1X	73
DIN2AX	73
DIN3X thru DIN20X	73
DIN21X	73
DIN22X	73
DIN23X	73
DIN24X	73
DIN25X	73
DIN26X	73
DISIX thru DISBX	73
GCI thru GC14	73
INTR1X thru INTR7X	73
NDO1 thru NDO 8	73
OCINT	73
SSFB1X thru SSFB8X	73

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+Y DIS DATA 01 — TSLI — DIS1X
+Y DIS DATA 02 — TSLI — DIS2X
+Y DIS DATA 03 — TSLI — DIS3X
+Y DIS DATA 04 — TSLI — DIS4X
+Y DIS DATA 05 — TSLI — DIS5X
+Y DIS DATA 06 — TSLI — DIS6X
+Y DIS DATA 07 — TSLI — DIS7X
+Y DIS DATA 08 — TSLI — DIS8X
+Y NA DIS DATA 01 — TSLI — NDO 1
+Y NA DIS DATA 02 — TSLI — NDO 2
+Y NA DIS DATA 03 — TSLI — NDO 3
+Y NA DIS DATA 04 — TSLI — NDO 4
+Y NA DIS DATA 05 — TSLI — NDO 5
+Y NA DIS DATA 06 — TSLI — NDO 6
+Y NA DIS DATA 07 — TSLI — NDO 7
+Y NA DIS DATA 08 — TSLI — NDO 8

+Y DDAS DATA 01 — TSLI — T501 / +B DDAS 01
+Y DDAS DATA 02 — TSLI — T502 / +B DDAS 02
+Y DDAS DATA 03 — TSLI — T503 / +B DDAS 03
+Y DDAS DATA 04 — TSLI — T504 / +B DDAS 04
+Y DDAS DATA 05 — TSLI — T505 / +B DDAS 05
+Y DDAS DATA 06 — TSLI — T506 / +B DDAS 06
+Y DDAS DATA 07 — TSLI — T507 / +B DDAS 07
+Y DDAS DATA 08 — TSLI — T508 / +B DDAS 08
+Y DDAS DATA 09 — TSLI — T509 / +B DDAS 09
+Y DDAS DATA 10 — TSLI — T510 / +B DDAS10
+Y INT REG DATA 01 — TSLI — INTR1X
+Y INT REG DATA 02 — TSLI — INTR2X
+Y INT REG DATA 03 — TSLI — INTR3X
+Y INT REG DATA 04 — TSLI — INTR4X
+Y INT REG DATA 05 — TSLI — INTR5X
+Y INT REG DATA 06 — TSLI — INTR6X
+Y INT REG DATA 07 — TSLI — INTR7X
+Y INT REG DATA 08 — TSLI — CR11X
+Y INT REG DATA 09 — TSLI — CR12X
+Y INT REG DATA 10 — TSLI — OCINT / +B OCINTX

+Y SSFB DATA 01 — TSLI — SSFB1X
+Y SSFB DATA 02 — TSLI — SSFB2X
+Y SSFB DATA 03 — TSLI — SSFB3X
+Y SSFB DATA 04 — TSLI — SSFB4X
+Y SSFB DATA 05 — TSLI — SSFB5X
+Y SSFB DATA 06 — TSLI — SSFB6X
+Y SSFB DATA 07 — TSLI — SSFB7X
+Y SSFB DATA 08 — TSLI — SSFB8X
+Y GC DATA 01 — TSLI — GC1
+Y GC DATA 02 — TSLI — GC2
+Y GC DATA 03 — TSLI — GC3
+Y GC DATA 04 — TSLI — GC4
+Y GC DATA 05 — TSLI — GC5
+Y GC DATA 06 — TSLI — GC6
+Y GC DATA 07 — TSLI — GC7
+Y GC DATA 08 — TSLI — GC8
+Y GC DATA 09 — TSLI — GC9
+Y GC DATA 10 — TSLI — GC10
+Y GC DATA 11 — TSLI — GC11
+Y GC DATA 12 — TSLI — GC12
+Y GC DATA 13 — TSLI — GC13
+Y GC DATA 14 — TSLI — GC14

+Y CR DATA 01 — TSLI — CR1
+Y CR DATA 02 — TSLI — CR2
+Y CR DATA 03 — TSLI — CR3
+Y CR DATA 04 — TSLI — CR4
+Y CR DATA 05 — TSLI — CR5
+Y CR DATA 06 — TSLI — CR6
+Y CR DATA 07 — TSLI — CR7
+Y CR DATA 08 — TSLI — CR8
+Y CR DATA 09 — TSLI — CR9
+Y CR DATA 10 — TSLI — CR10
+Y CR DATA 11 — TSLI — CR11
+Y CR DATA 12 — TSLI — CR12
+Y CR DATA 13 — TSLI — CR13
+Y CR DATA 14 — TSLI — CR14
+Y DIN DATA 01 — TSLI — DIN1X
+Y DIN DATA 2A — TSLI — DIN2AX
+Y DIN DATA 03 — TSLI — DIN3X
+Y DIN DATA 04 — TSLI — DIN4X
+Y DIN DATA 05 — TSLI — DIN5X

+Y DIN DATA 06 — TSLI — DIN6X
+Y DIN DATA 07 — TSLI — DIN7X
+Y DIN DATA 08 — TSLI — DIN8X
+Y DIN DATA 09 — TSLI — DIN9X
+Y DIN DATA 10 — TSLI — DIN10X
+Y DIN DATA 11 — TSLI — DIN11X
+Y DIN DATA 12 — TSLI — DIN12X
+Y DIN DATA 13 — TSLI — DIN13X
+Y DIN DATA 14 — TSLI — DIN14X
+Y DIN DATA 15 — TSLI — DIN15X
+Y DIN DATA 16 — TSLI — DIN16X
+Y DIN DATA 17 — TSLI — DIN17X
+Y DIN DATA 18 — TSLI — DIN18X
+Y DIN DATA 19 — TSLI — DIN19X
+Y DIN DATA 20 — TSLI — DIN20X
+Y DIN DATA 21 — TSLI — DIN21X
+Y DIN DATA 22 — TSLI — DIN 22X
+Y DIN DATA 23 — TSLI — DIN 23X
+Y DIN DATA 24 — TSLI — DIN 24X
+Y DIN DATA 25 — TSLI — DIN 25 BIT
+Y DIN DATA 28 — TSLI — DIN 28X

REFERENCE ALD PAGES
05.09.27.1
05.09.28.1
05.09.29.1
05.09.30.1
05.09.31.1
05.09.32.1

REFERENCE DRAWING

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CONTRACT NO

DESIGNED — DATE
DESIGN CHECK W.K. Hurley 8-7-67
DRAWN MIDSTATE 73066
DRAWING CHECK
DESIGN APPROVAL M.P. Livingston 8-7-67

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE., NEW YORK 22, N.Y.

TITLE: TRANSLATE LOGIC

CODE IDENT NO | SIZE F | 6942020
SCALE | WT | SHEET 72

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 75)

OUTPUTS	
SIGNAL	DESTINATION
-Y SSFB DATA 01 OUT THRU	
-Y SSFB DATA 08 OUT	41, 42
-Y CR DATA 01 OUT THRU	
-Y CR DATA 14 OUT	40, 41, 42
-Y DIN DATA 01 OUT	44
-Y DIN DATA 2A OUT	44
-Y DIN DATA 2B OUT	44
-Y DIN DATA 25 OUT	44
-Y DIN DATA 03 OUT THRU	
-Y DIN DATA 24 OUT	40, 41, 42, 43, 44
-Y DIS DATA 01 OUT THRU	
-Y DIS DATA 08 OUT	40, 41
-Y NA DIS DATA 01 OUT THRU	
-Y NA DIS DATA 08 OUT	43, 44
-Y DDAS DATA 01 OUT THRU	
-Y DDAS DATA 10 OUT	40, 41
-Y INT REG DATA 01 OUT THRU	
-Y INT REG DATA 10 OUT	40, 41, 42

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CR14 TSLT -Y CR DATA 14 OUT
CR13 TSLT -Y CR DATA 13 OUT
CR12 TSLT -Y CR DATA 12 OUT
CR11 TSLT -Y CR DATA 11 OUT
CR10 TSLT -Y CR DATA 10 OUT
CR9 TSLT -Y CR DATA 09 OUT
CR8 TSLT -Y CR DATA 08 OUT
CR7 TSLT -Y CR DATA 07 OUT
CR6 TSLT -Y CR DATA 06 OUT
CR5 TSLT -Y CR DATA 25 OUT
CR4 TSLT -Y CR DATA 04 OUT
CR3 TSLT -Y CR DATA 03 OUT
CR2 TSLT -Y CR DATA 02 OUT
CR1 TSLT -Y CR DATA 01 OUT
DIN 25 BIT TSLT -Y DIN DATA 25 OUT
DIN 24 X TSLT -Y DIN DATA 24 OUT
DIN 23 X TSLT -Y DIN DATA 23 OUT
DIN 22 X TSLT -Y DIN DATA 22 OUT
DIN 21 X TSLT -Y DIN DATA 21 OUT
DIN 2BX TSLT -Y DIN DATA 2B OUT

DIN20X TSLT -Y DIN DATA 20 OUT
DIN19X TSLT -Y DIN DATA 19 OUT
DIN18X TSLT -Y DIN DATA 18 OUT
DIN17X TSLT -Y DIN DATA 17 OUT
DIN16X TSLT -Y DIN DATA 16 OUT
DIN15X TSLT -Y DIN DATA 15 OUT
DIN14X TSLT -Y DIN DATA 14 OUT
DIN13X TSLT -Y DIN DATA 13 OUT
DIN12X TSLT -Y DIN DATA 12 OUT
DIN11X TSLT -Y DIN DATA 11 OUT
DIN10X TSLT -Y DIN DATA 1C OUT
DIN9X TSLT -Y DIN DATA 09 OUT
DIN8X TSLT -Y DIN DATA 08 OUT
DIN7X TSLT -Y DIN DATA 07 OUT
DIN6X TSLT -Y DIN DATA C6 OUT
DIN5X TSLT -Y DIN DATA 05 OUT
DIN4X TSLT -Y DIN DATA 04 OUT
DIN3X TSLT -Y DIN DATA 03 OUT
DIN2AX TSLT -Y DIN DATA 2A OUT
DIN1X TSLT -Y DIN DATA 01 OUT

DIS8X TSLT -Y DIS DATA 08 OUT
DIS7X TSLT -Y DIS DATA 07 OUT
DIS6X TSLT -Y DIS DATA 06 OUT
DIS5X TSLT -Y DIS DATA 05 OUT
DIS4X TSLT -Y DIS DATA 04 OUT
DIS3X TSLT -Y DIS DATA 03 OUT
DIS2X TSLT -Y DIS DATA 02 OUT
DIS1X TSLT -Y DIS DATA 01 OUT
NDO 8 TSLT -Y NA DIS DATA 08 OUT
NDO 7 TSLT -Y NA DIS DATA 07 OUT
NDO 6 TSLT -Y NA DIS DATA 06 OUT
NDO 5 TSLT -Y NA DIS DATA 05 OUT
NDO 4 TSLT -Y NA DIS DATA 04 OUT
NDO 3 TSLT -Y NA DIS DATA 03 OUT
NDO 2 TSLT -Y NA DIS DATA 02 OUT
NDO 1 TSLT -Y NA DIS DATA 01 OUT

SSF8X TSLT -Y SSFB DATA 08 OUT
SSF7X TSLT -Y SSFB DATA 07 OUT
SSF6X TSLT -Y SSFB DATA 06 OUT
SSF5X TSLT -Y SSFB DATA 05 OUT
SSF4X TSLT -Y SSFB DATA 04 OUT
SSF3X TSLT -Y SSFB DATA 03 OUT
SSF2X TSLT -Y SSFB DATA 02 OUT
SSF1X TSLT -Y SSFB DATA 01 OUT

GC14 TSLT -Y GC DATA 14 OUT
GC13 TSLT -Y GC DATA 13 OUT
GC12 TSLT -Y GC DATA 12 OUT
GC11 TSLT -Y GC DATA 11 OUT
GC10 TSLT -Y GC DATA 10 OUT
GC9 TSLT -Y GC DATA 09 OUT
GC8 TSLT -Y GC DATA 08 OUT
GC7 TSLT -Y GC DATA 07 OUT
GC6 TSLT -Y GC DATA 06 OUT
GC5 TSLT -Y GC DATA 05 OUT
GC4 TSLT -Y GC DATA 04 OUT
GC3 TSLT -Y GC DATA 03 OUT
GC2 TSLT -Y GC DATA 02 OUT
GC1 TSLT -Y GC DATA 01 OUT

+8 DDAS 10 TSLI I -Y DDAS DATA 10 OUT
+8 DDAS 09 TSLI I -Y DDAS DATA 09 OUT
+8 DDAS 08 TSLI I -Y DDAS DATA 08 OUT
+8 DDAS 07 TSLI I -Y DDAS DATA 07 OUT
+8 DDAS 06 TSLI I -Y DDAS DATA 06 OUT
+8 DDAS 05 TSLI I -Y DDAS DATA 05 OUT
+8 DDAS 04 TSLI I -Y DDAS DATA 04 OUT
+8 DDAS 03 TSLI I -Y DDAS DATA 03 OUT
+8 DDAS 02 TSLI I -Y DDAS DATA 02 OUT
+8 DDAS 01 TSLI I -Y DDAS DATA 01 OUT

+8 OCINT X TSLT I -Y INT REG DATA 10 OUT
CR12X TSLT -Y INT REG DATA 09 OUT
CR11X TSLT -Y INT REG DATA 08 OUT
INTR7X TSLT -Y INT REG DATA 07 OUT
INTR6X TSLT -Y INT REG DATA 06 OUT
INTR5X TSLT -Y INT REG DATA 05 OUT
INTR4X TSLT -Y INT REG DATA 04 OUT
INTR3X TSLT -Y INT REG DATA 03 OUT
INTR2X TSLT -Y INT REG DATA 02 OUT
INTR1X TSLT -Y INT REG DATA 01 OUT

REFERENCE ALD PAGES
01.15.25.1
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01.15.27.1
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01.15.29.1
01.15.30.1

REFERENCE DRAWING

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DESIGN APPROVAL M.A. Livingston 8-7-69

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FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

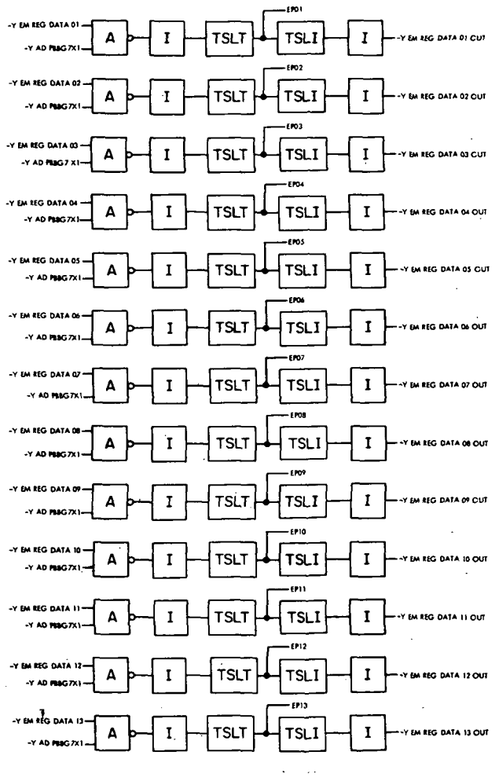
TITLE TRANSLATE LOGIC

CODE IDENT NO. SIZE F 6942020
SCALE WT SHEET 73

Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 76)

INPUTS	
SIGNAL	ORIGIN
-Y AD P88G7X1	10
-Y AD P88G7X2	10
-Y CSA0	37
-Y CSA1	37
-Y CSB0	37
-Y CSB1	37
-Y CSC0	37
-Y CSC1	37
-Y EM REG DATA 01	37
-Y EM REG DATA 02	37
-Y EM REG DATA 03	37
-Y EM REG DATA 04	37
-Y EM REG DATA 05	37
-Y EM REG DATA 06	37
-Y EM REG DATA 07	37
-Y EM REG DATA 08	37
-Y EM REG DATA 09	37
-Y EM REG DATA 10	37
-Y EM REG DATA 11	37
-Y EM REG DATA 12	37
-Y EM REG DATA 13	37
-Y EM REG DATA 14	37
-Y EM REG DATA 15	37
-Y EM REG DATA 16	37

OUTPUTS	
SIGNAL	DESTINATION
-Y EM REG DATA 01 OUT	43, 47
-Y EM REG DATA 02 OUT	42, 47
-Y EM REG DATA 03 OUT	42, 47
-Y EM REG DATA 04 OUT	42, 47
-Y EM REG DATA 05 OUT	42, 47
-Y EM REG DATA 06 OUT	42, 47
-Y EM REG DATA 07 OUT	41, 46
-Y EM REG DATA 08 OUT	41, 46
-Y EM REG DATA 09 OUT	41, 46
-Y EM REG DATA 10 OUT	41, 46
-Y EM REG DATA 11 OUT	41, 46
-Y EM REG DATA 12 OUT	40, 46
-Y EM REG DATA 13 OUT	40, 46
-Y EM REG DATA 14 OUT	46
-Y EM REG DATA 15 OUT	46
-Y EM REG DATA 16 OUT	46



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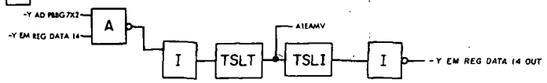

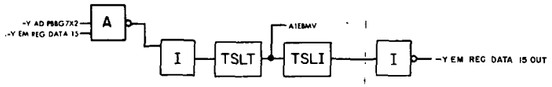

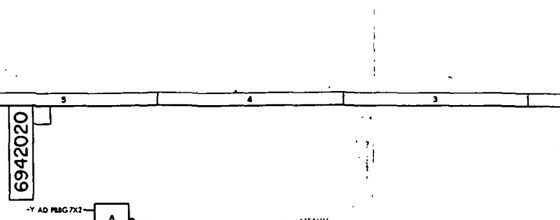

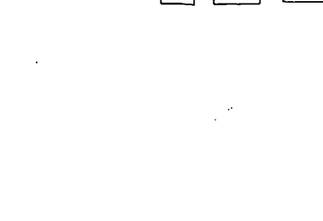

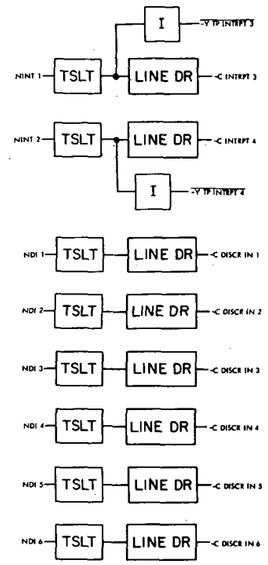

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	DRAWN MIDSTATE	9-4-64	
	DRAWING CHECK		
	DESIGN APPROVAL M. A. Livingston	9-7-67	CODE IDENT NO. F SIZE 6942020
			SCALE WT SHEET 74

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Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 77)

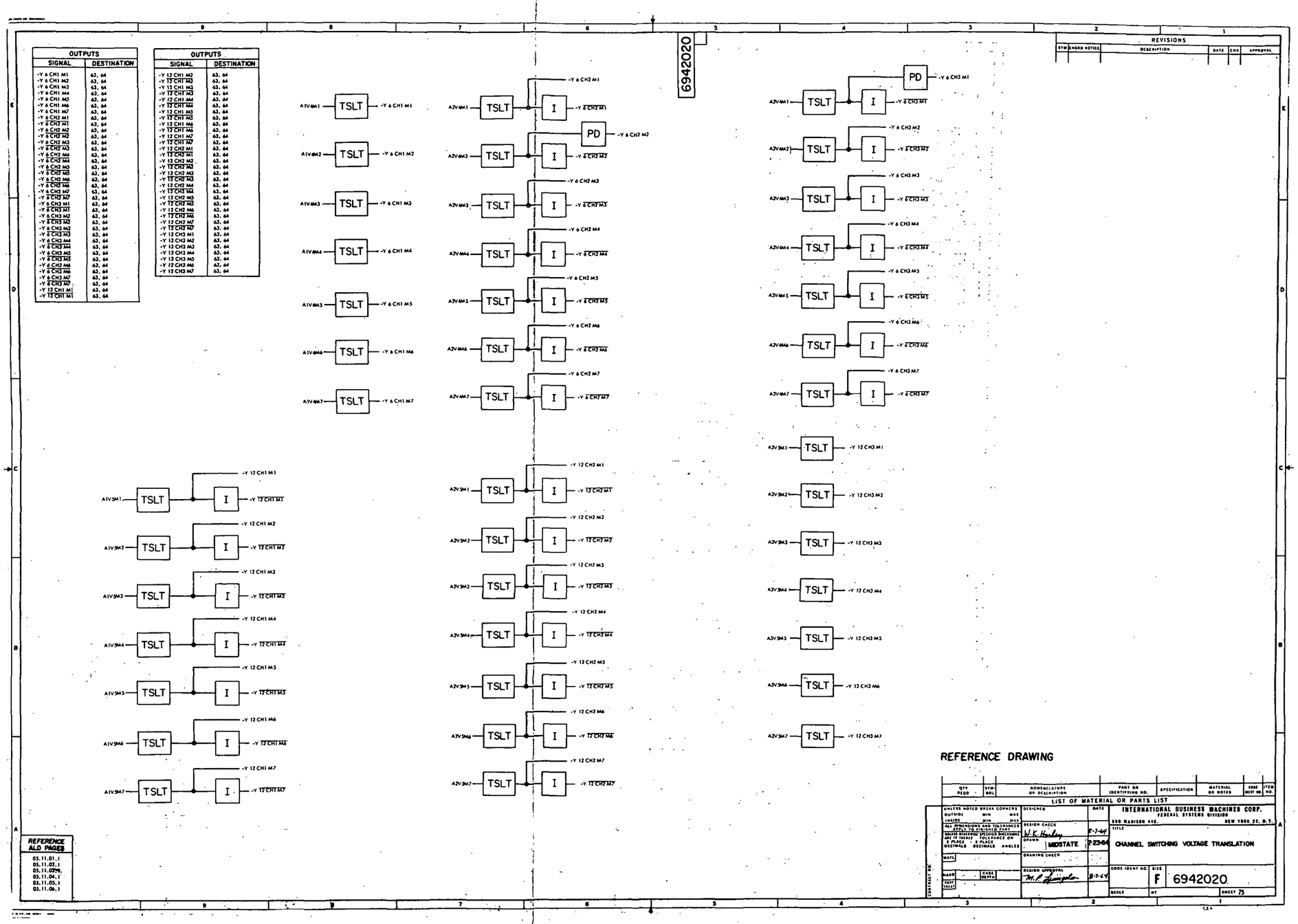
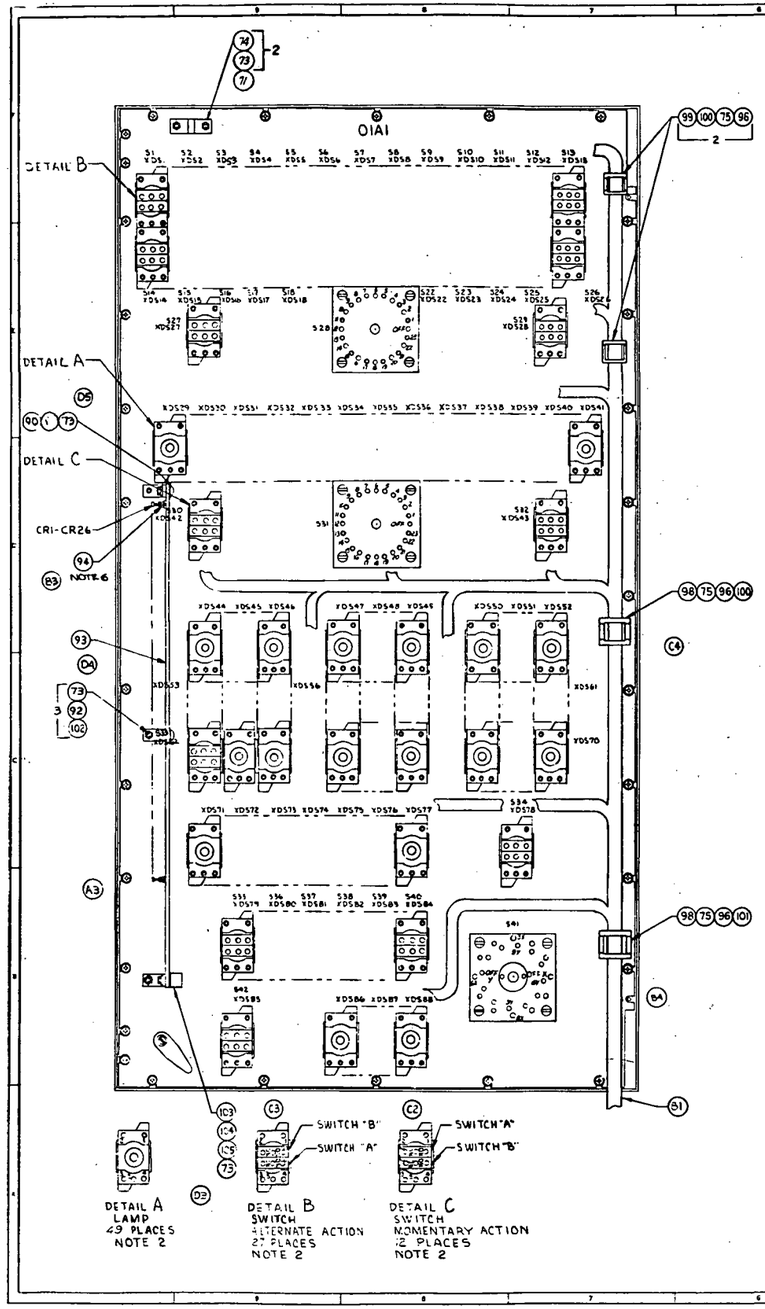


Figure 10-50. LVDAME Second Level Logic Diagrams (Sheet 78)



6942300

REF DES	ITEM NO
S1	13
S2	12
S3	11
S4	10
S5	9
S6	8
S7	7
S8	6
S9	5
S10	4
S11	3
S12	2
S13	1
S14	26
S15	25
S16	24
S17	23
S18	22
S19	21
S20	20
S21	19
S22	18
S23	17
S24	16
S25	15
S26	14
S27	40
S29	41
S30	43
S32	42
S33	43
S34	54
S35	47
S36	57
S37	58
S38	59

REF DES	ITEM NO.
S39	56
S40	55
S42	60
XDS 29	39
30	38
31	37
32	36
33	35
34	34
35	33
36	32
37	31
38	30
39	29
40	28
41	27
44	44
45	45
46	
47	44
48	45
49	
50	
51	
52	
53	
54	
55	
56	
57	
58	

REF DES	ITEM NO.
XDS 60	45
61	
63	44
64	
65	
66	95
67	
68	
69	
70	45
71	53
72	52
73	51
74	50
75	49
76	48
77	46
80	49
87	48
88	96
XDS 59	45

NOTES
1. IBM GEN. ASSY SPEC 6000003 APPLIES
2. SWITCH AND LAMP IDENTIFICATION ONLY (SHEET 1 OF 2)
3. IDENTIFICATION OF SYMBOLS.
   V- VENDOR ITEM- SEE SPEC OR SOURCE CONTROL DWG
   R- REFERENCE QTY
4. WIRE PER 6942300 JUMPER LIST
5. INSTALL LAMPS ITEM NO. 84 IN POSITIONS 1 & 3 ON ALL INDICATORS EXCEPT AS FOLLOWS: XDS44 THRU XDS70 AND XDS72 INSTALL LAMPS IN POSITIONS 1, 2 & 4.
6. CATHODE END OF DIODES ARE ON EVEN NUMBERED SIDE OF TERMINAL BOARD.
7. LATCH SPACERS ARE SUPPLIED WITH LATCH. USE AS DIRECTED ON LATCH INSTALLATION INSTRUCTIONS INCLUDED WITH LATCH.

REVISIONS			
STA	ENGRG NOTICE	DESCRIPTION	DATE	APPROVAL
	66115FD	RELEASE	7-64	
A	66115GR	(1-4) SEE ENGRG NOTICE R	9-64	
B	66115JD	(1-6) SEE ENGRG NOTICE R	9-64	
C	66115KJ	(1-7) SEE ENGRG NOTICE R	9-64	
D	66115MS	(1-8) SEE ENGRG NOTICE R	10-64	

1		SWITCH ASS'Y	6078693				60
1			6081876				59
1			6081732				58
1			6082018				57
1			6082006				56
1			6082005				55
1			6082000				54
1			6081968				53
1			6081967				52
1			6081966				51
1			6081965				50
2			6081964				49
2			6081963				48
1			6081959				47
2			6081951				46
17			6081950				45
9			6081949				44
2			6081948				43
1			6081947				42
1			6081945				41
1			6081946				40
1			6081944				39
1			6081943				38
1			6081942				37
1			6081941				36
1			6081940				35
1			6081939				34
1			6081938				33
1			6081937				32
1			6081936				31
1			6081935				30
1			6081934				29
1			6081933				28
1			6081932				27
1			6081930				26
1			6081929				25
1			6081928				24
1			6081927				23
1			6081926				22
1			6081925				21
1			6081924				20
1			6081923				19
1			6081922				18
1			6081921				17
1			6081920				16
1			6081919				15
1			6081916				14
1			6081917				13
1			6081916				12
1			6081915				11
1			6081914				10
1			6081913				9
1			6081912				8
1			6081911				7
1			6081910				6
1			6081909				5
1			6081908				4
1			6081907				3
1			6081906				2
1	V	SWITCH ASS'Y	6061931				1

1		SCREW (6035701)	MS35216-15				105
1	V	"D" WASHER	6013352				104
1	V	CLAMP	6072583				103
3		SCREW, FL HD (6035633)	MS 24693C4				102
1	V	CLIP (N5)	6079358				101
3	V	CLIP (N1)	6079357				100
2	V	CRADLE (C1)	6079352				99
2	V	CRADLE (C2)	6079353				98
4		SPACER	6477103				97
4		SCREW, PAN HD (6035709)	MS35216-25				96
4	V	SWITCH ASSY	6078703				95
26		DIODE	492543			5836	94
1		TERMINAL BOARD	6942329				93
3		BRACKET	6942328				92
38		WASHER, FL (6048641)	MS15795-303				91
5		SCREW (6035700)	MS35216-14				90
6		SCREW, FL HD (6035658)	MS24693C48				89
2	V	KNOB	6072801				88
1	V	SWITCH, ROTARY	6035436				87
2	V	SWITCH, ROTARY	6081131				86
2 FT		WIRE #20 (6032192)	TYPE NO. 20				85
202	V	LAMP	6078990				84
4		WASHER LK (6029218)	MS35338-78				83
4		SCREW, FIL HD (6028009)	AN500AD4-6				82
1		HARNESS	6942395				81
15 FT	V.R	WIRE #22 BLACK 1 COND	6032061				80
50 FT	V.R	WIRE #22 RED 1 COND	6032145				79
25 FT	V.R	WIRE #22 YELLOW 1 COND	6032141				78
AR		SOLDER (6032357)	SN60AR	QQS-571			77
1		PANEL, OVERLAY	6942325				76
180		SCREW, FL (6035644)	MS24693C25				75
2		SCREW, FL HD (6035631)	MS24693C2				74
11		NUT, LK #4 (6072821)	NAS1291A04M				73
1		SUB, PANEL	6942325				72
1		STRIKE	597097			8836	71
1		BAR, HINGE	597088				70
1		BAR, LATCH	597087				69
2		SCREW, SET	257956				68
2		HINGE, PIN	597098				67
2		HINGE	597093			8836	66
31		SCREW, PAN HD (6035699)	MS35216-13				65
							64
2		BAR, PANEL	597089			8836	63
1	V	LATCH	6079797				62
							61

QTY REQD	STA	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	ITEM NO.	LN

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED DECIMAL TOLERANCES: BUSHING ±1/64 MAX, HOLES ±1/64 MAX. ALL MACHINED SURFACES 125 MICRO INCHES OR BETTER. TOLERANCE ON 2 PLACE DECIMALS ±.01 MAX, 3 PLACE DECIMALS ±.005 MAX, ANGLES ±1°. MATL: NEXT ASSY USED ON

RELEASED: Jon Fiddler 9-64
DESIGN CHECK: Jon Fiddler 9-64
DRAWING CHECK: Ed Hamba 9-64
DESIGN APPROVAL: R F Engel 9-64
7-64

INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION, 590 MADISON AVE., NEW YORK 22, N.Y.

TITLE: PANEL ASSY-INTERFACE MONITOR LVDA MANUAL EXERCISER

01A1

CODE IDENT NO 01640 | SIZE E | 6942300

SCALE NONE | WT | SHEET 1 OF 2

Figure 10-51. Interface Monitoring Panel (01A1) Assembly Drawing (Sheet 1 of 2)

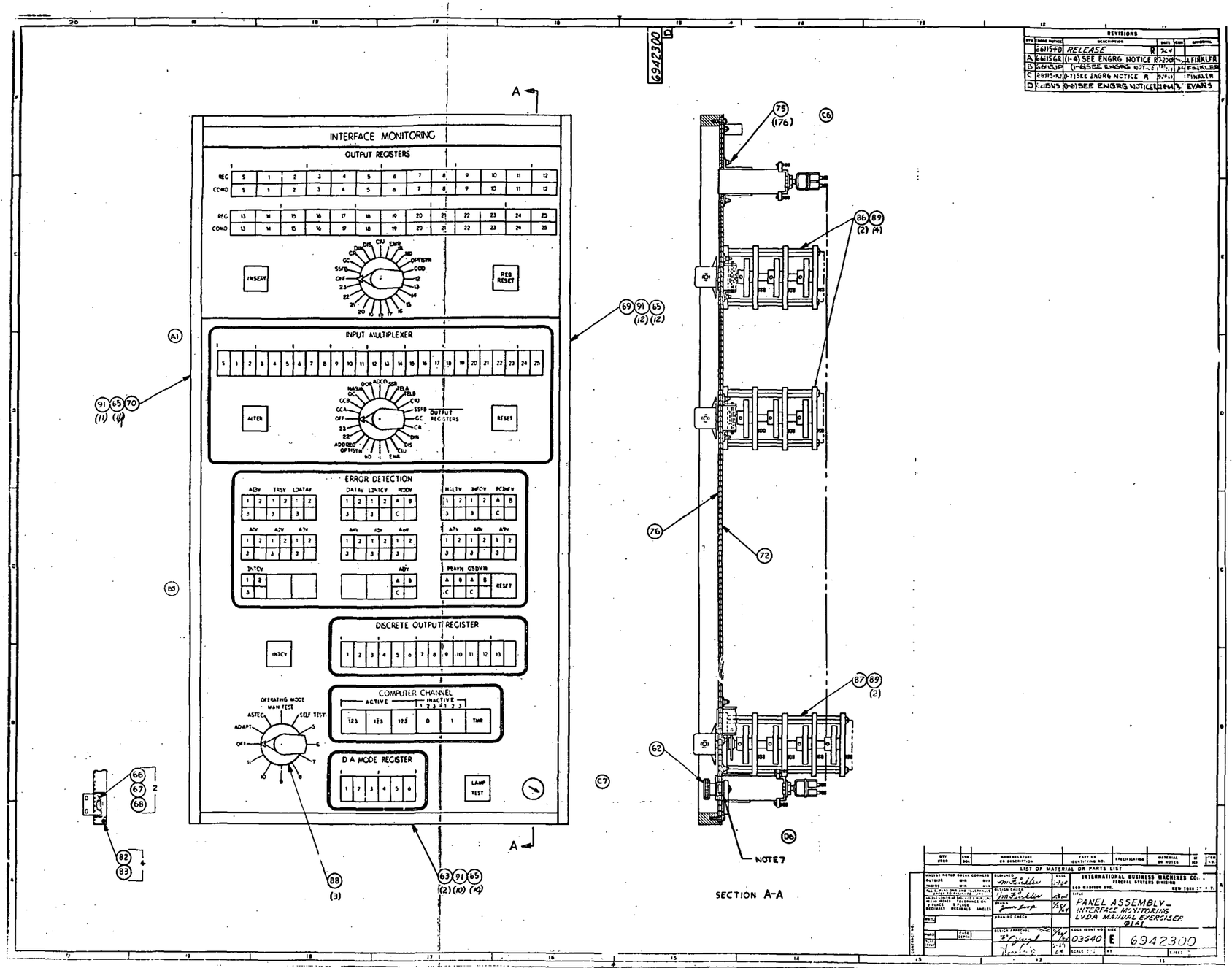
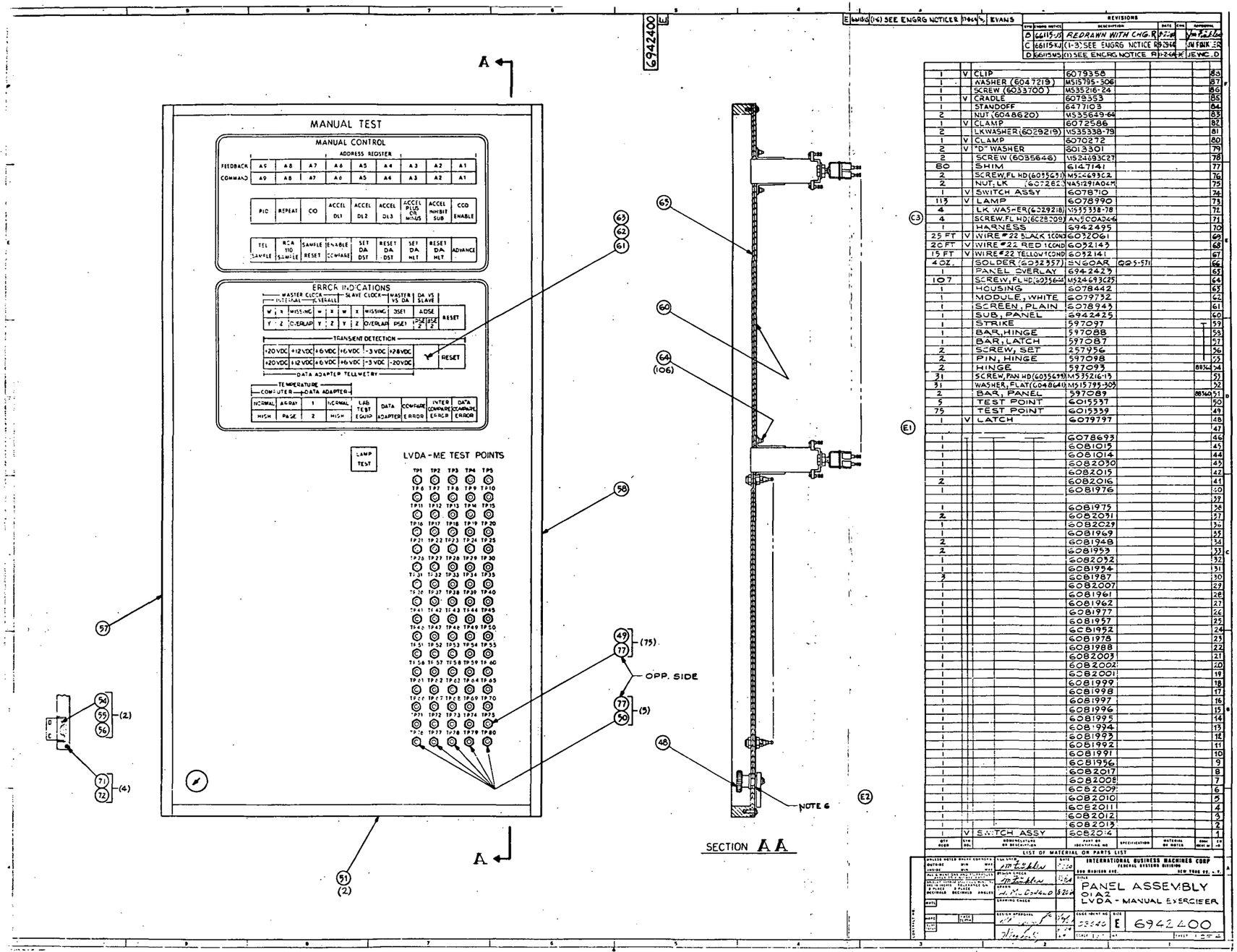
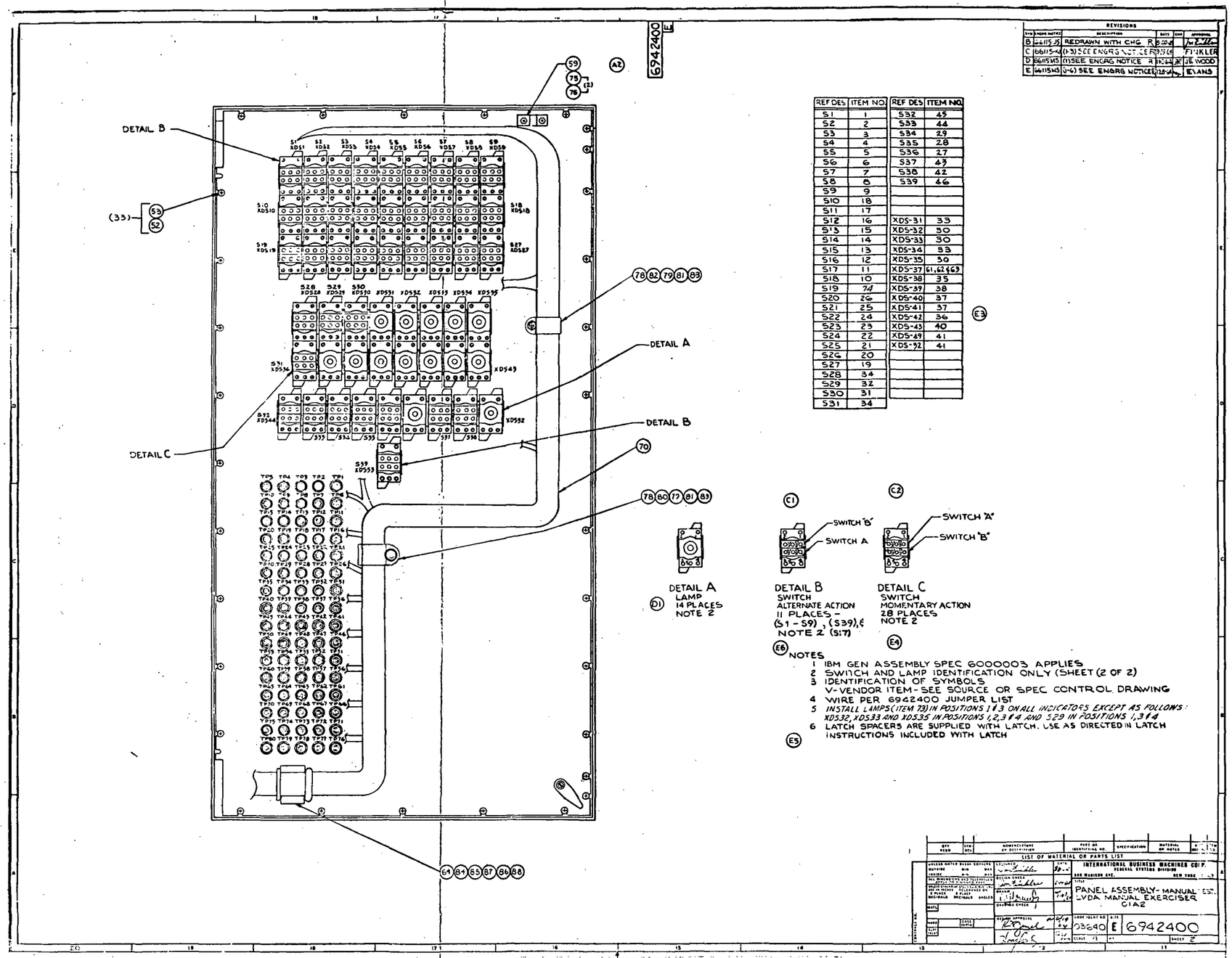


Figure 10-51. Interface Monitoring Panel (01A1) Assembly Drawing (Sheet 2)



1	V	CLIP	6079358					85
1		WASHER (6047219)	MS15795-306					87
1		SCREW (6033700)	MS35216-24					86
1	V	CRADLE	6079353					85
1		STANDOFF	6477103					84
2		NUT (6048620)	MS35649-64					83
1	V	CLAMP	6072586					82
2		LKWASHER (6029219)	MS35338-79					81
1	V	CLAMP	6070272					80
2	V	"D" WASHER	6013301					79
2		SCREW (6035648)	MS24693C27					78
80		SHIM	6147141					77
2		SCREW, FL HD (6035631)	MS24693C2					76
2		NUT, LK (6072621)	MS51291A04M					75
1	V	SWITCH ASSY	6078710					74
113	V	LAMP	6078990					73
4		LK WASHER (6029218)	MS35338-78					72
4		SCREW, FL HD (6028309)	AN5004D4-6					71
1		HARNESS	6942495					70
25 FT	V	WIRE #22 BLACK 1 COND	6032061					69
20 FT	V	WIRE #22 RED 1 COND	6032143					68
15 FT	V	WIRE #22 YELLOW 1 COND	6032141					67
4 OZ.		SOLDER (6032357)	SN60AR	QQS-571				66
1		PANEL OVERLAY	6942423					65
107		SCREW, FL HD (6035634)	MS24693C25					64
1		HOUSING	6078442					63
1		MODULE, WHITE	6079732					62
1		SCREEN, PLAIN	6078943					61
1		SUB, PANEL	6942425					60
1		STRIKE	597097				T	59
1		BAR, HINGE	597088					58
1		BAR, LATCH	597087					57
2		SCREW, SET	257956					56
2		PIN, HINGE	597098					55
2		HINGE	597093				88360	54
31		SCREW, PAN HD (6035629)	MS35216-13					53
31		WASHER, FLAT (6048641)	MS15795-309					52
2		BAR, PANEL	597089				88360	51
5		TEST POINT	6015537					50
75		TEST POINT	6015539					49
1	V	LATCH	6079797					48
								47
1			6078693					46
1			6081015					45
1			6081014					44
1			6082030					43
1			6082015					42
2			6082016					41
1			6081976					40
								39
1			6081975					38
2			6082031					37
1			6082029					36
1			6081969					35
2			6081968					34
2			6081953					33
1			6082032					32
1			6081954					31
3			6081987					30
1			6082007					29
1			6081961					28
1			6081962					27
1			6081977					26
1			6081957					25
1			6081952					24
1			6081978					23
1			6081988					22
1			6082003					21
1			6082002					20
1			6082001					19
1			6081999					18
1			6081998					17
1			6081997					16
1			6081996					15
1			6081995					14
1			6081994					13
1			6081993					12
1			6081992					11
1			6081991					10
1			6081956					9
1			6082017					8
1			6082008					7
1			6082009					6
1			6082010					5
1			6082011					4
1			6082012					3
1			6082013					2
1	V	SWITCH ASSY	6082014					1

Figure 10-52. Manual Exerciser Panel (01A2) Assembly Drawing (Sheet 1 of 2)



REF DES	ITEM NO
S1	1
S2	2
S3	3
S4	4
S5	5
S6	6
S7	7
S8	8
S9	9
S10	18
S11	17
S12	16
S13	15
S14	14
S15	13
S16	12
S17	11
S18	10
S19	74
S20	26
S21	25
S22	24
S23	23
S24	22
S25	21
S26	20
S27	19
S28	34
S29	32
S30	31
S31	34

REF DES	ITEM NO
S32	45
S33	44
S34	29
S35	28
S36	27
S37	43
S38	42
S39	46
XDS-31	33
XDS-32	30
XDS-33	30
XDS-34	33
XDS-35	30
XDS-37	61, 62, 63
XDS-38	35
XDS-39	38
XDS-40	37
XDS-41	37
XDS-42	36
XDS-43	40
XDS-69	41
XDS-92	41

Figure 10-52. Manual Exerciser Panel (01A2) Assembly Drawing (Sheet 2)

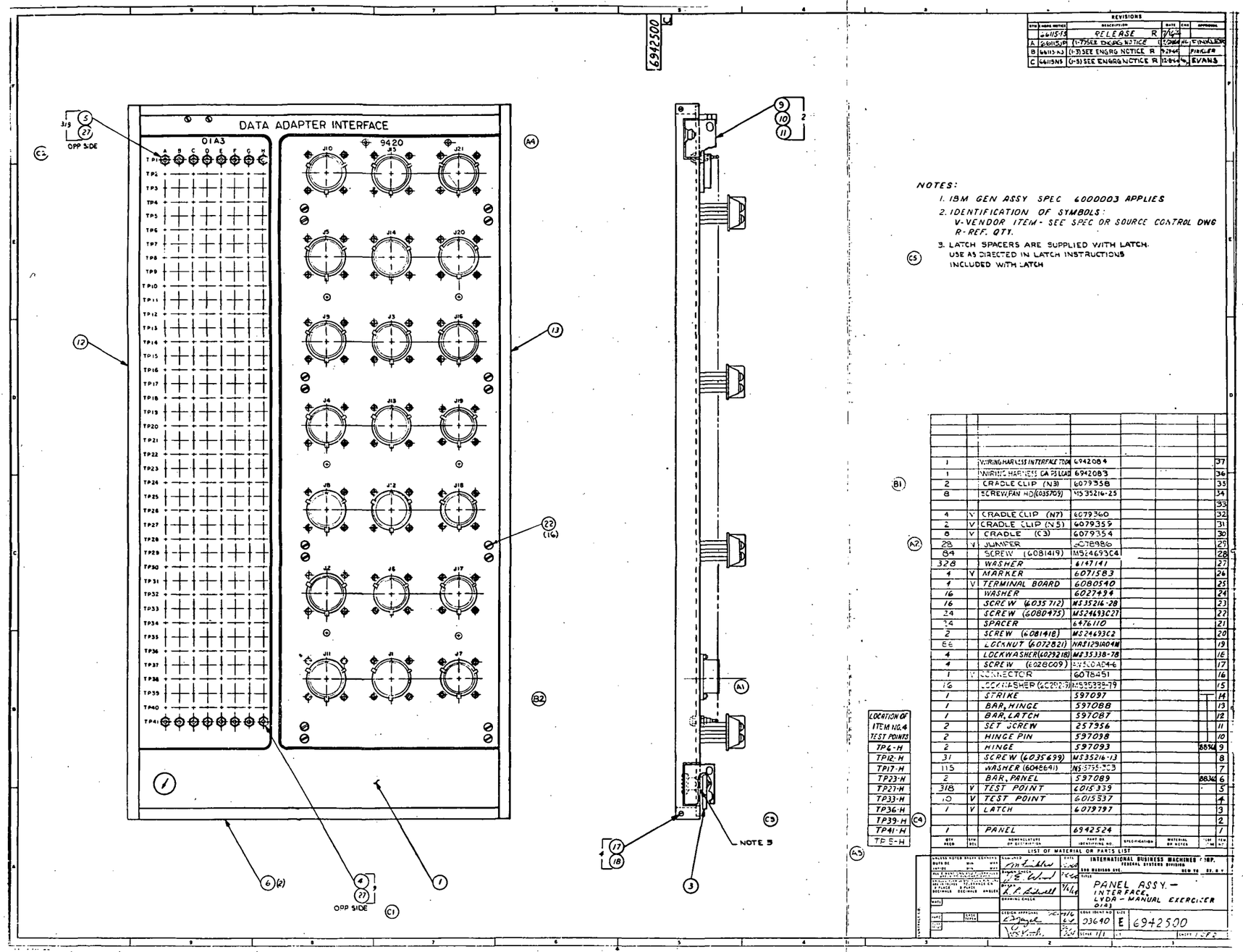
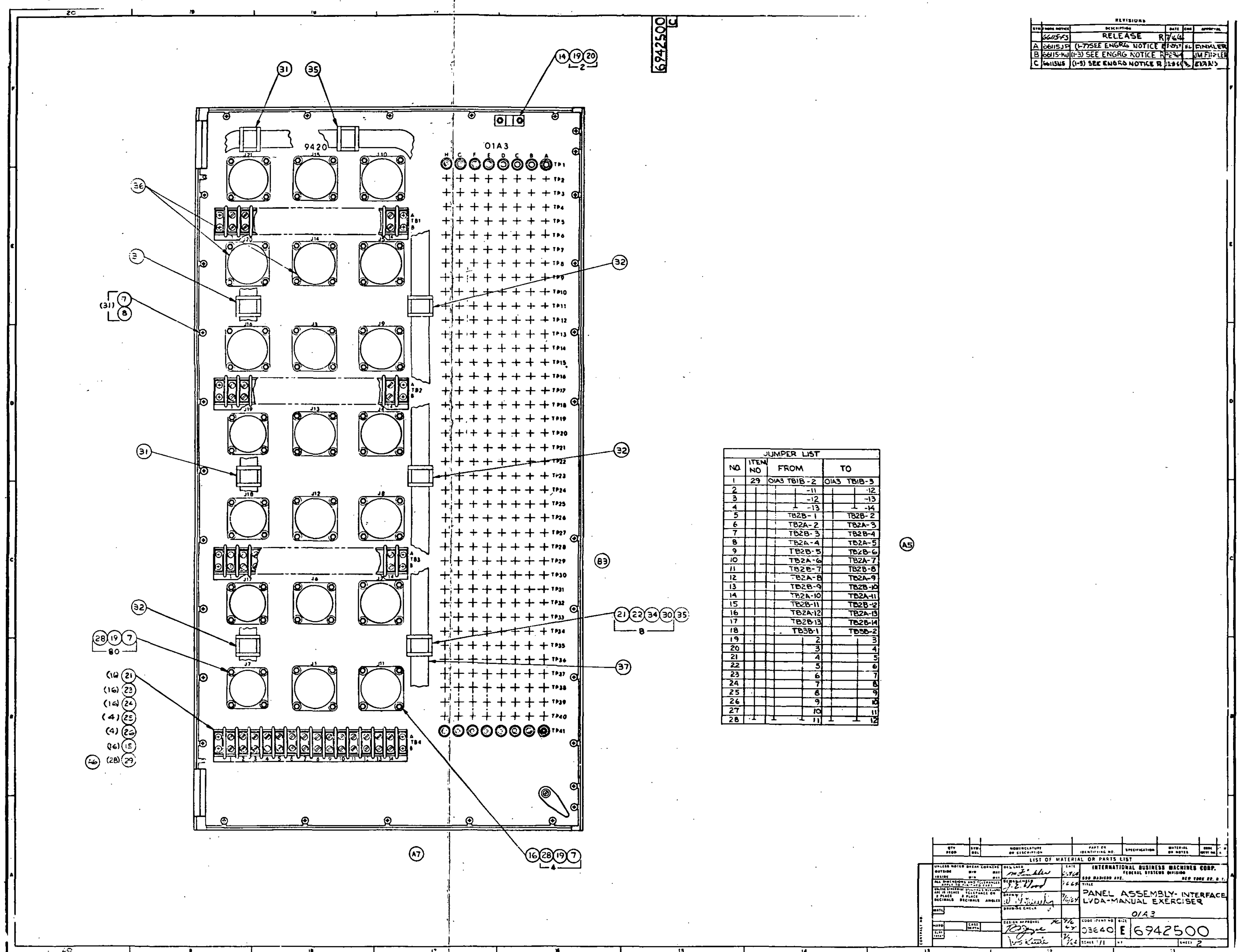
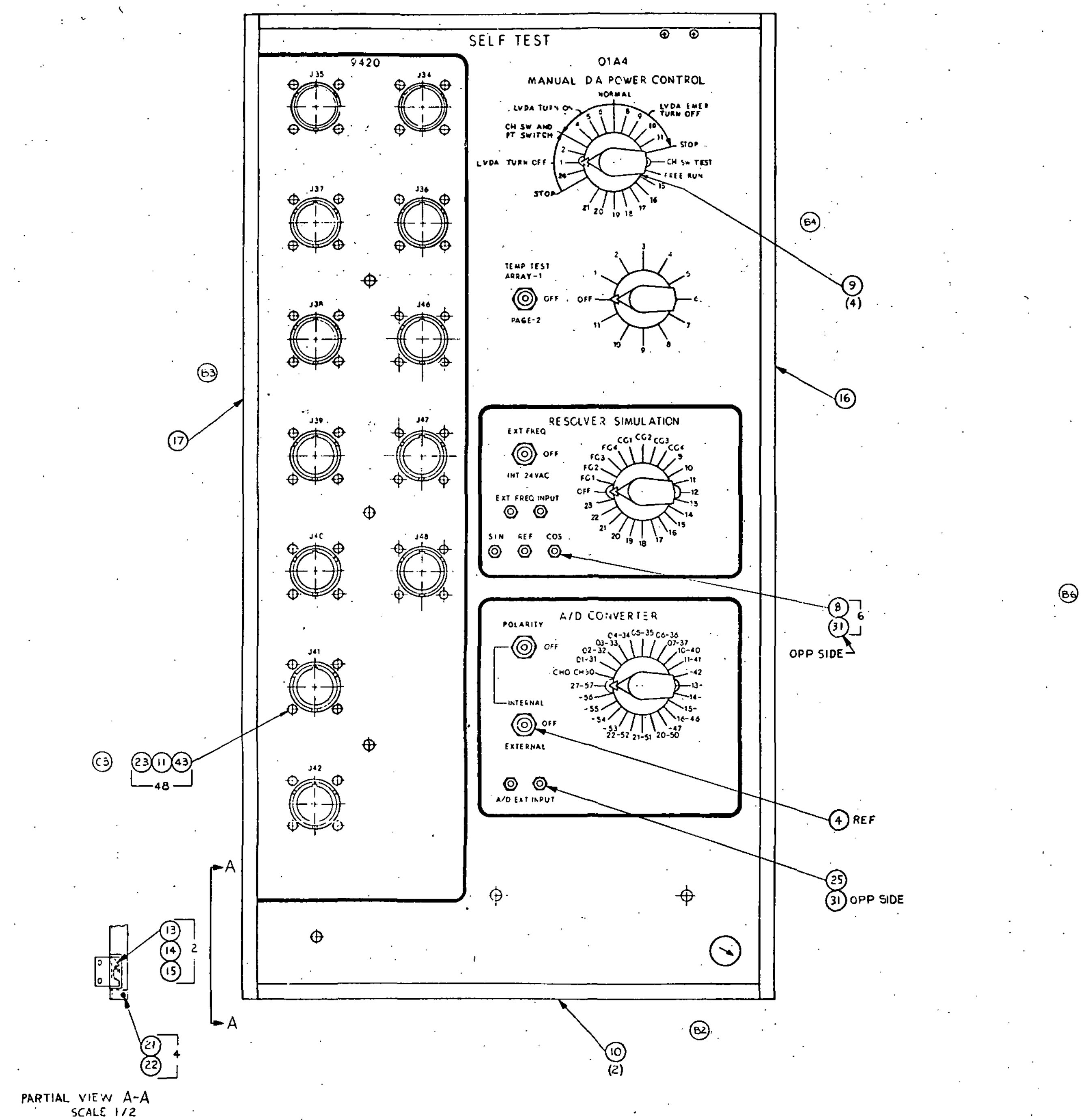


Figure 10-53. Data Adapter Interface Panel (01A3) Assembly Drawing (Sheet 1 of 2)



JUMPER LIST			
NO	ITEM NO	FROM	TO
1	29	01A3 TB1B-2	01A3 TB1B-3
2		-11	-12
3		-12	-13
4		-13	-14
5		TB2B-1	TB2B-2
6		TB2A-2	TB2A-3
7		TB2B-3	TB2B-4
8		TB2A-4	TB2A-5
9		TB2B-5	TB2B-6
10		TB2A-6	TB2A-7
11		TB2B-7	TB2B-8
12		TB2A-8	TB2A-9
13		TB2B-9	TB2B-10
14		TB2A-10	TB2A-11
15		TB2B-11	TB2B-12
16		TB2A-12	TB2A-13
17		TB2B-13	TB2B-14
18		TB3B-1	TB3B-2
19		2	3
20		3	4
21		4	5
22		5	6
23		6	7
24		7	8
25		8	9
26		9	10
27		10	11
28		11	12

Figure 10-53. Data Adapter Interface Panel (01A3) Assembly Drawing (Sheet 2)



NOTES.

1. IBM GEN ASSY SPEC 6000003 APPLIES
2. IDENTIFICATION OF SYMBOLS:
   V-VENDOR ITEM - SEE SPEC OR SOURCE CONTROL DWG
   R-REFERENCE QTY
3. INSTALL ITEM NO. 33 BETWEEN FRONT OF PANEL AND LOCKWASHER.
4. (C2) SET ADJUSTABLE STOP ON S1 SWITCH AT POSITION NO 22
5. LATCH SPACERS ARE SUPPLIED WITH LATCH. USE AS DIRECTED ON LATCH INSTALLATION INSTRUCTIONS INCLUDED WITH LATCH

QTY REQD	SYM NOTE	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
54	V	TAPER PINS	6073042				55
1 FT.	V,R	WIRE, #20 AWG GREEN	6032034				54
1 FT.	V,R	WIRE, #20 AWG YELLOW	6032033				53
1		SCREW (6033700)	MS51957-27				52
1		NUT, LK (6072822)	NAS1291A06M				51
1		SCREW (6080476)	MS24693C28				50
1		BRACKET, SUPPORT	6942134				49
3		SCREW (6079432)	MS24693C26				48
1	V	CLIP	6079360				47
5		WASHER (6047219)	MS15795-306				46
3		SCREW (6035709)	MS35216-25				45
2		SCREW (6080479)	MS24693C25				44
48		SCREW (6081419)	MS24693C4				43
3	V	CLIP	6079359				42
4	V	CRADLE	6079354				41
3		STANDOFF	6477103				40
1		HARNESS	6942082				39
2		NUT LK (6072823)	NAS1291A08M				38
2		WASHER, FLAT (6048639)	MS15795-307				37
2		SPACER	6942620				36
2		SCREW (6081490)	MS24693C64				35
3	V	BLOCK TAPER PIN	6073067				34
4		WASHER, FLAT	6027431				33
6 IN.	V,R	WIRE, AWG NO. 20, BLACK	6032029				32
7		WASHER	6147141				31
8		TERM LUG NO. 20 (6013350)	MS25036-1				30
4		(6081417)	MS24693C47				29
							28
2		(6081416)	MS24693C47				27
2		SCREW (6082132)	MS24693C3				26
1	V	TEST POINT	6015537				25
1 FT.	PV	WIRE, AWG NO. 20 RED	6032031				24
50		NUT LOCK (6072821)	NAS1291A04M				23
4		WASHER (6029218)	MS35338-78				22
4		SCREW (6028009)	AN500AD4-6				21
2 FT.	R	WIRE (6032192)	TYPE NO 20	MIL-W-3861			20
4 OZ.	R	SOLDER (6032357)	SN60 AR	QQ-S-571			19
1		STRIKE	597097				18
1		BAR, HINGE	597088				17
1		BAR, LATCH	597087				16
2		SET SCREW	257956				15
2		HINGE, PIN	597098				14
2		HINGE	597093			88630	13
31		SCREW (6035699)	MS35216-13				12
79		WASHER (6048641)	MS15785-303				11
2		BAR, PANEL	597089			88630	10
4	V	KNOB	6072801				9
6	V	TEST POINT	6015339				8
1	V	LATCH	6079797				7
							6
1		PANEL	6942624				5
4	V	SWITCH, TOGGLE	6034112				4
1			6081375				3
1			6035431				2
2	V	SWITCH, ROTARY	6035435				1

LIST OF MATERIAL OR PARTS LIST

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PANEL ASSY- SELF TEST LVDA-MANUAL EXERCISER 01A4

SIZE E 6942600

Figure 10-54. Self-Test Panel (01A4) Assembly Drawing (Sheet 1 of 2)

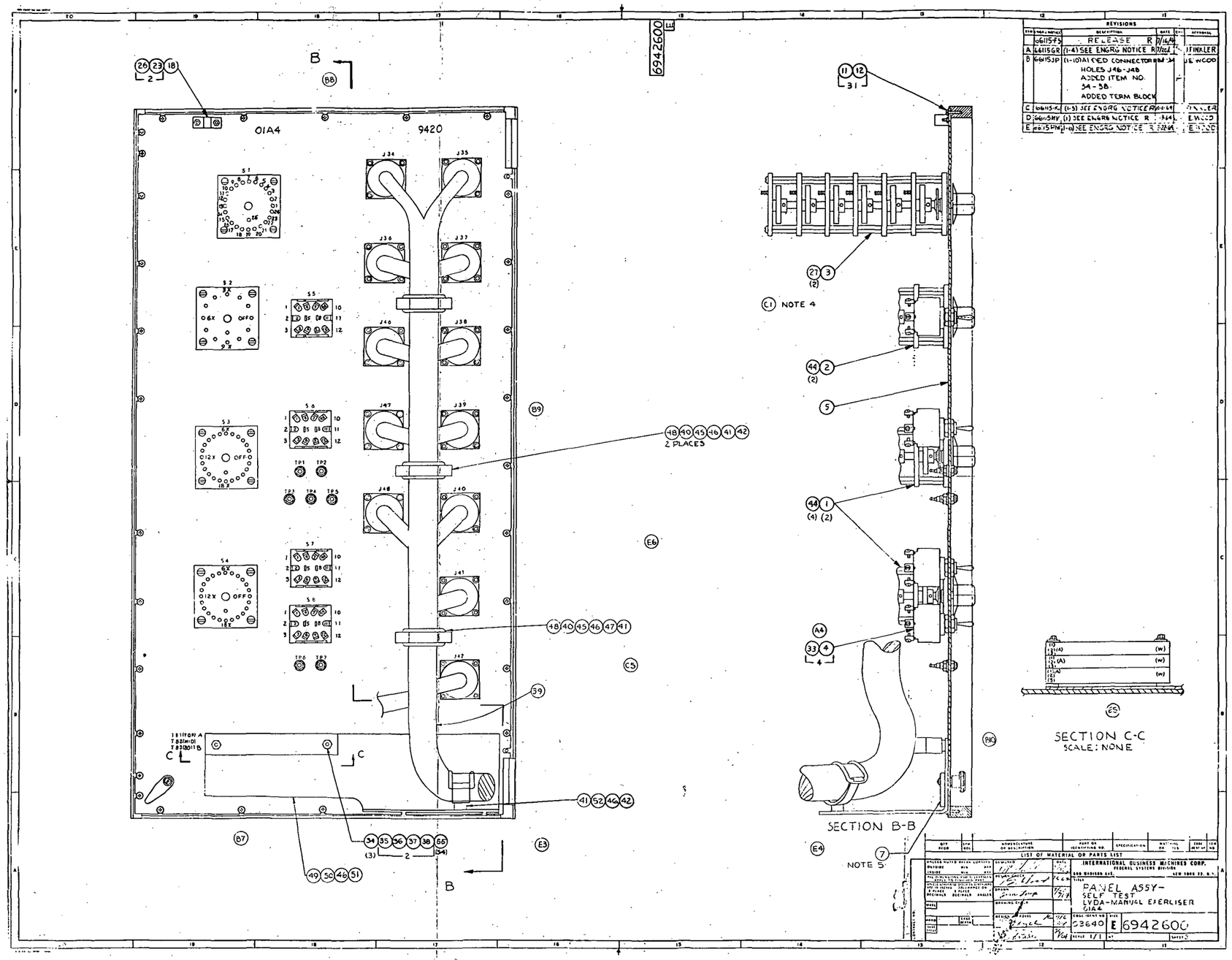


Figure 10-54. Self-Test Panel (01A4) Assembly Drawing (Sheet 2)

JUMPER LIST

NO.	ITEM NO.	FROM	TO	NO.	ITEM NO.	FROM	TO
1	5	01A10TB4A1	01A10TB4A2	17	15	01A10TB2B11	01A10TB2B12
2		TB4B2	TB4B3	18		TB2B12	TB2B13
3		TB4A3	TB4A4	19		TB2B13	TB2B14
4		TB4B4	TB4B5	20		TB2B14	TB2B15
5		TB4A5	TB4A6	21		TB3B1	TB3B2
6		TB4A7	TB4A8	22		TB3B2	TB3B3
7		TB4B8	TB4B9	23		TB3B3	TB3B4
8		TB4A9	TB4A10	24		TB3B4	TB3B5
9		TB4B10	TB4B11	25		TB3B5	TB3B6
10		TB4A11	TB4A12	26		TB3B6	TB3B7
11		TB2B5	TB2B6	27		TB3B7	TB3B8
12		TB2B6	TB2B7	28		TB3B8	TB3B9
13		TB2B7	TB2B8	29		TB3B9	TB3B10
14		TB2B8	TB2B9	30		TB3B10	TB3B11
15		TB2B9	TB2B10	31		TB3B11	TB3B12
16		TB2B10	TB2B11				

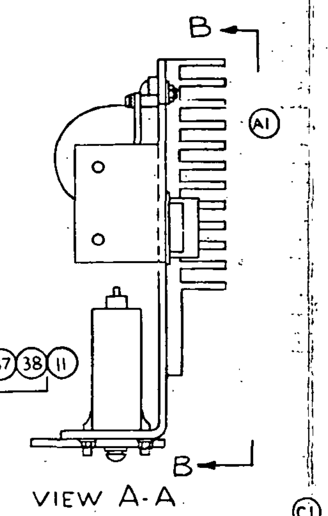
SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT OR PN

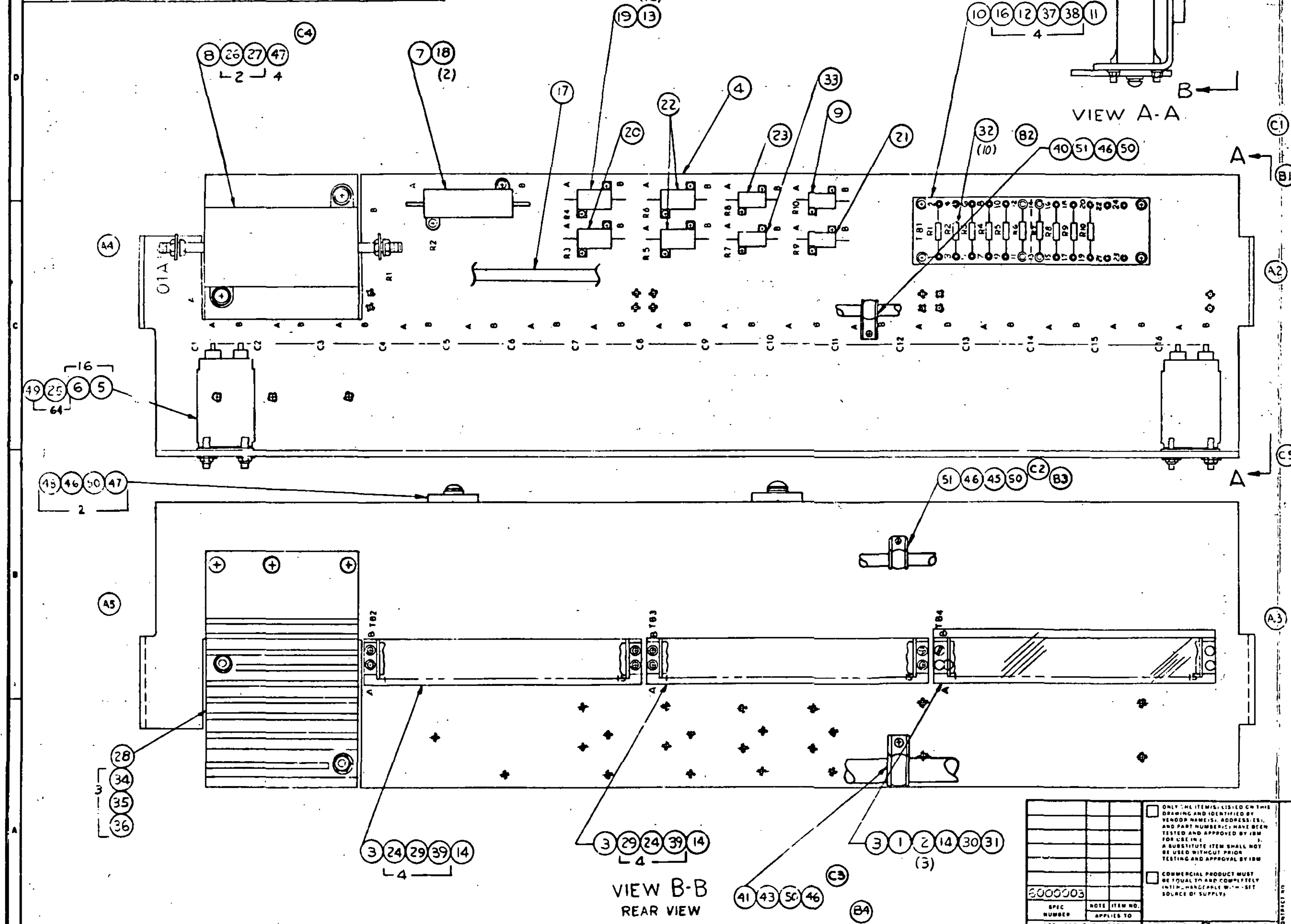
6942216 C

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115 HC	RELEASE R	8/3/4		
A	66115 JP	(1-5) SEE ENGRG NOTICE R			M.FINWLER
B	66115 LG	(1-5) SEE ENGRG NOTICE R			EVANS
C	66115 NZ	(1-5) SEE ENGRG NOTICE R			J.E. WOOD



NOTE
1. IBM GEN ASSY SPEC 6000003 APPLIES



QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO
2	V	D WASHER	6013352				51
5		LOCKWASHER (6029220)	MS35338-80				50
64		WASHER (6047219)	MS15795-306				49
2		SUPPORT BRACKET	69420:9				48
6		WASHER (6048639)	MS157:5-307				47
5		SCREW (6035721)	MS51957-42				46
1	V	CABLE CLAMP	6072584				45
							44
1	V	CABLE CLAMP	6070272				43
							42
1	V	WASHER 'D'	6013301				41
1	V	CABLE CLAMP	6072585				40
8		LOCKWASHER (6029219)	MS35338-79				39
4		LOCKWASHER (6029218)	MS35338-78				38
4		WASHER (6048641)	MS15795-303				37
3		WASHER (.6301812)	MS15795-308				36
3		WASHER LK (6029221)	MS35338-81				35
3		SCREW (6035736)	MS35217-55				34
1	V	RESISTOR 10K, 5W, ±3%	6081164				33
10		RESISTOR (6011557)	RC20GF512J				32
1		SCREW	210984			88360	31
1		COVER, SAFETY	192596			88360	30
8		SCREW (6035712)	MS35216-28				29
1		HEAT SINK	6902047				28
2		SCREW (6035726)	MS35216-44				27
2		NUT. LK (6072823)	NAS1291A08M				26
64		NUT. LK (6072822)	NAS1291-A06M				25
8		WASHER, FLAT	6027494				24
1	V	9.75Ω, 5W, ±3%	6081439				23
2	V	53Ω, 10W, ±3%	6081442				22
1	V	13Ω, 5W, ±3%	6081440				21
1	V	31Ω, 10W, ±5%	6081441				20
1	V	RESISTOR 1.27Ω, 10W, ±3%	6081163				19
2		SCREW (6035699)	MS35216-13				18
1		HARNESS	6942195				17
4		SPACER	6035599				16
31	V	JUMPER	6078986				15
3	V	MARKER STRIP	6070257				14
16		SCREW (6035693)	MS35216-3				13
4		SCREW (6035703)	MS35216-17				12
AR		SOLDER (6032357)	SN60 AR	QQ-S-571			11
1		TERMINAL BOARD	6942128				10
1	V	750Ω, 5W, ±3%	6081443				9
1	V	.536Ω, 100W, ±3%	6081162				8
1	V	RESISTOR 662:50W ±3%	6081438				7
16	V	BRACKET	6081446				6
16	V	CAPACITOR 155MF, 30V	6081445				5
1		BRACKET	6942130				4
3	V	TERMINAL BLOCK	6070256				3
3		STUD	210884			88360	2
1		STUD	210883			88360	1

LIST OF MATERIAL OR PARTS LIST

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN ... A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH LISTED SOURCE OF SUPPLY

CHECK BLOCK ☒ IF APPLICABLE

6000003 — APPLICABLE IBM SPEC

IDENT. OF SYM V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

DESIGNED / DESIGN CHECK E. Wood / DRAWN VMD 7-20-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: BRACKET ASSY-RESISTOR, CAPACITOR-MTG, LVDA-MANUAL EXERCISER, 01A10

03640 F 6942216

SCALE 1/1

Figure 10-55. Resistor - Capacitor Mounting Bracket (01A0) Assembly Drawing

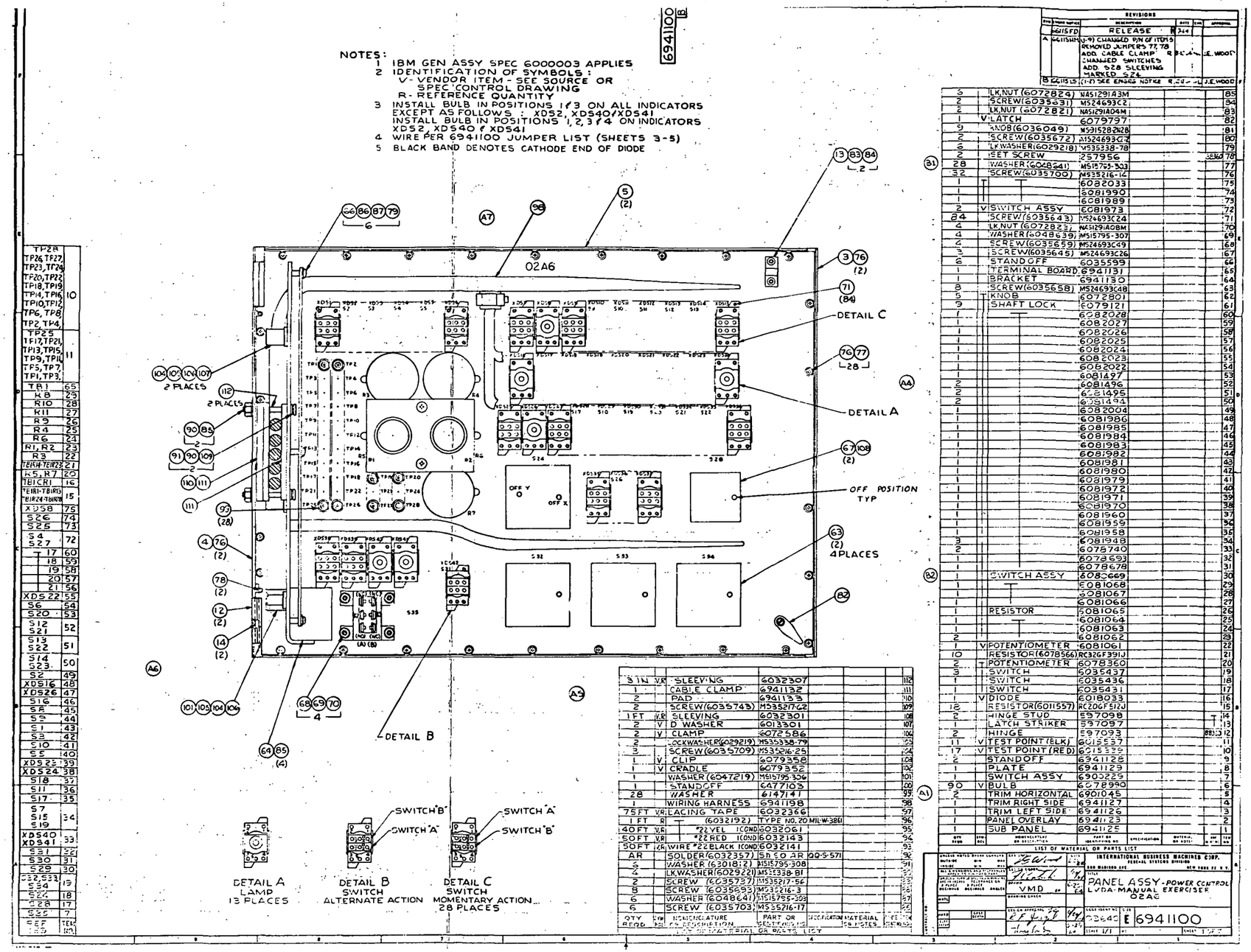


Figure 10-56. Power Control Panel (02A6) Assembly Drawing (Sheet 1 of 2)

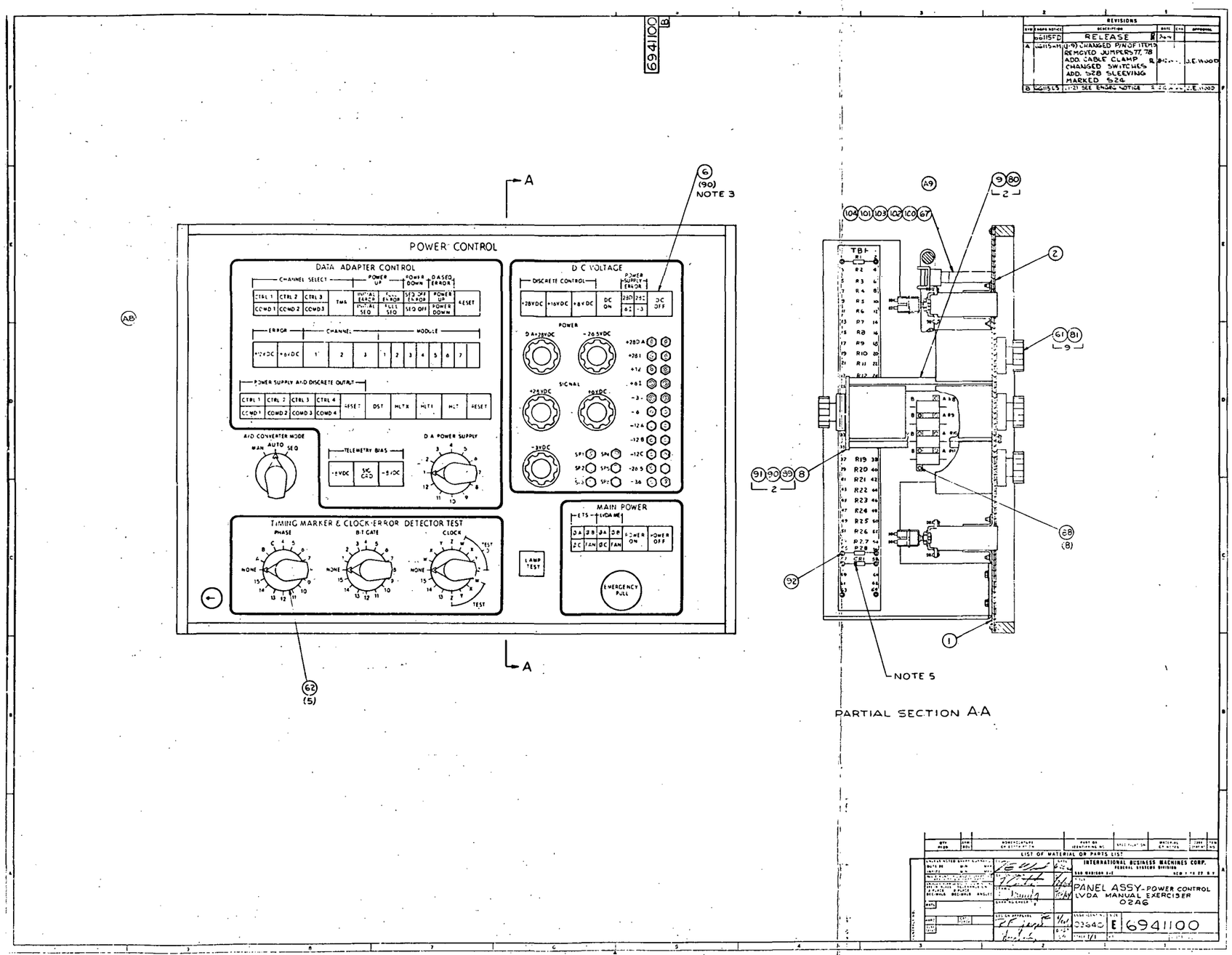


Figure 10-56. Power Control Panel (02A6) Assembly Drawing (Sheet 2)

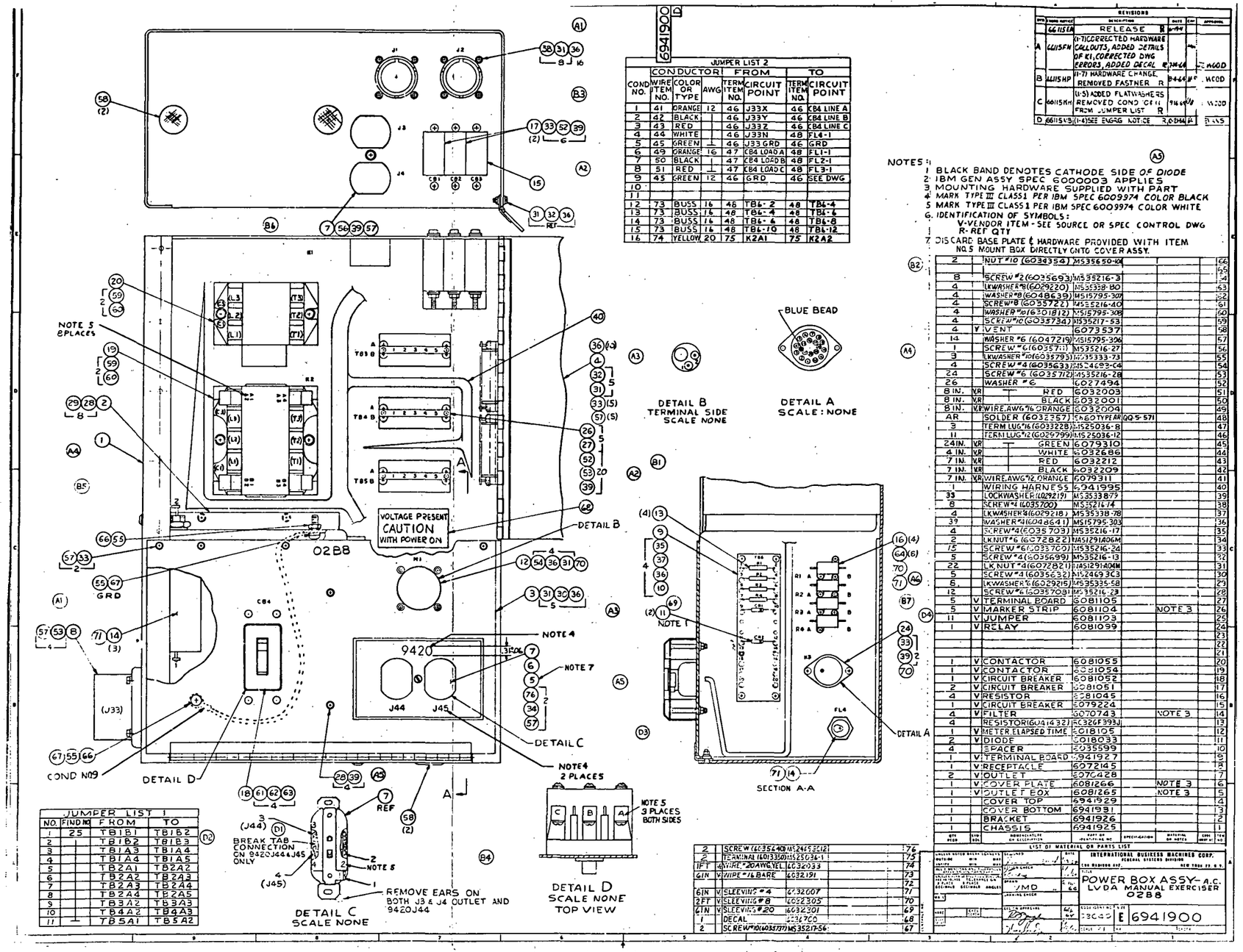
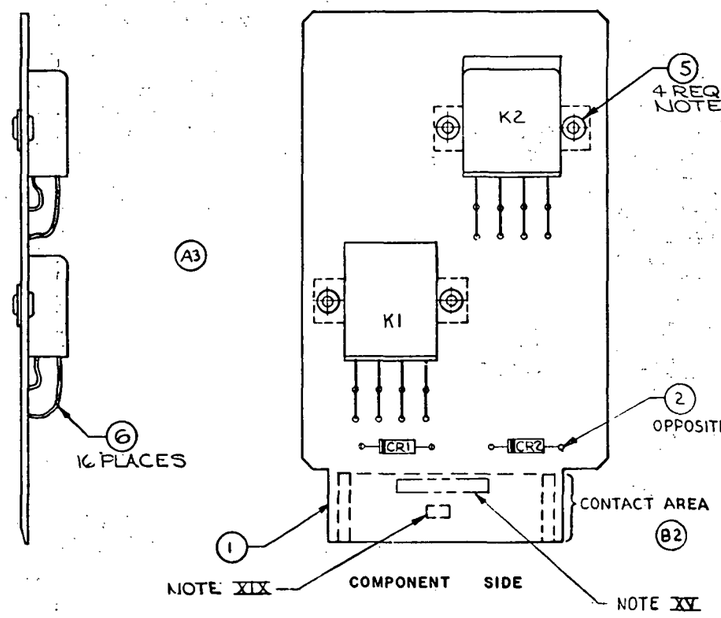
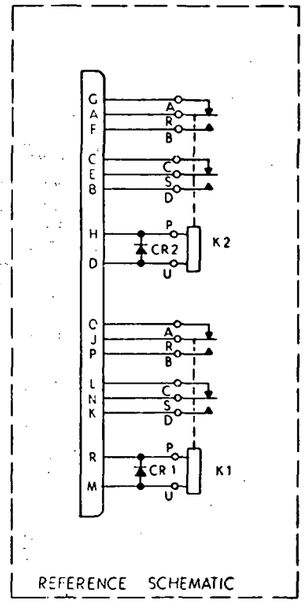


Figure 10-57. AC Power Box (02B8) Assembly Drawing

6901030 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BB	RELEASE	11-11-63		
A	66121 CJ	(1-3) SEE ENGRG NOTICE	12-3-63		JE WOOD
B	66115 JF	(1-2) COATED WIRING TO PREVENT CORROSION	12-3-63		JE WOOD





NOTES

- I IBM GEN ASSY SPEC 6000003 APPLIES
- II MIN ELECTRICAL CLEARANCE TO BE .018
- III COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- IV COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- V LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- VI PARTMARK 6901030 ASSY PER IBM SPEC 6009974, COLOR BLACK
- VII JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE SOLDERING
- VIII BLACK BAND DENOTES CATHODE END OF DIODE
- IX IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REF QTY
- A1 XIX MARK REVISION SYMBOL PER IBM SPEC 6009974 COLOR BLACK
- XX RELAY MTG HOLES IN FLANGE MAY REQUIRE REAMING TO ACCEPT EYELET.
- XXI ALL COPPER CONDUCTOR SURFACES SHALL BE TINNED WITH ITEM NO.2 OR THE CONDUCTOR (WIRING) SIDE OF THE CARD SHALL BE COATED WITH SEALANT ITEM NO.7. CONTACT AREA MUST BE KEPT FREE OFF SURFACE TREATMENT

B1

REF DES	ITEM NO.
K2	4
K1	4
CR2	3
CR1	3

A2

QTY REQD	SEM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
AR	V	SEALANT	6075477				7
16 IN.	VR	SLEEVING	6032850				6
4	V	EYELET	6027021				5
2	V	RELAY	6080231				4
2	V	DIODE	6018033				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901017				1

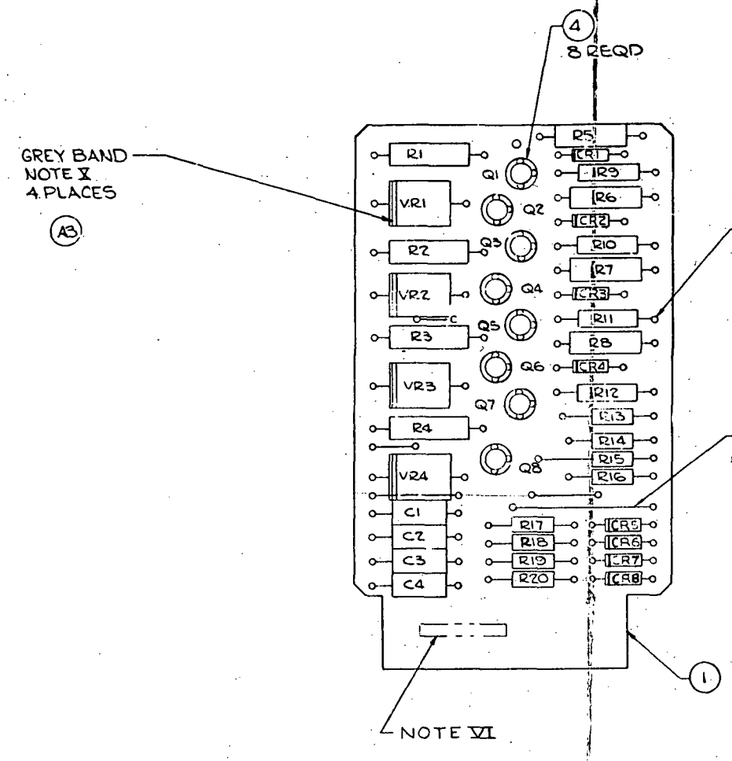
LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX	DESIGNED J.E. Wood	DATE 11-18-63	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 590 MADISON AVE. NEW YORK 22, N.Y.
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART	DESIGN CHECK	12-1-63	TITLE PRINTED CIRCUIT BOARD ASSY-- RELAY CARD
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES	DRAWN J.E. Wood	12-18-63	
MATL	DRAWING CHECK		
HARD CASE DEPTH SURF TREAT	DESIGN APPROVAL	12-18-63	CODE IDENT NO. 03640 SIZE D 6901030
CONTRACT NO.		12-18-63	SCALE 2/1 WT SHEET

Figure 10-58. Relay Card Printed Circuit Board Assembly (6901030)

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BC	RELEASE	31 1 64		
A	66112DB	(1-3) ADD NOTE X	12-2-64		EVANS

6901330 A



NOTES

I IBM GENERAL ASSEMBLY SPECIFICATION 6000003 APPLIES
II MIN ELECTRICAL CLEARANCE TO BE .08
III COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
IV COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
V LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
VI PARTMARK 6901330 ASSY PER IBM SPEC 6009974 COLOR BLACK
VII JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
VIII BLACK BAND DENOTES CATHODE END OF DIODE
IX IDENTIFICATION OF SYMBOLS
V- VENDOR ITEM- SEE SPEC OR SOURCE CONTROL DWG
R- REFERENCE QUANTITY
A1 X GREY BAND ON (6) DENOTES ANODE SIDE OF DIODE

QTY PER	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
4	V	RES, 1.4K, 1/8W, ±1%	6079011				13
4	V	RES, 1.24K, 1/8W, ±1%	6079010				12
4	V	RES, 1.1K, 1/4W, ±1%	6079003				11
4	V	RES, 383Ω, 1/2W, ±1%	6079047				10
4	V	RES, 402Ω, 1/2W, ±1%	6079009				9
8	V	TRANSISTOR	6079006				8
8	V	DIODE	5017645		NOTE VIII		7
4	V	DIODE, ZENER	6079005		NOTE X		6
4		CAP., .01UF, 100VDC ±10%	491228			88360	5
8		PAD	483070			88360	4
AR		SOLDER (60/32/35)	SN60 AR	QQ-S-571			3
10 IN	VR	WIRE #22 AWG, YEL	6036152				2
1		SMS CARD	6901331				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS SHARP. OUTSIDE MIN MAX, INSIDE MIN MAX. ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ±.01, 3 PLACE DECIMALS ±.005, ANGLES ±1°. MATL. HARD SURF TREAT CASE DEPTH. CONTRACT NO.

DESIGNED — DATE 12-18-63
DESIGN CHECK — 12-19-63
DRAWN MOSE — 12-23-63
DRAWING CHECK
DESIGN APPROVAL — 12-18-63, 12-19-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT BOARD ASSY-TRANSLATOR, AN1

CODE IDENT NO. 03640 — SIZE D — 6901330

SCALE 2/1 — SHEET 1 OF 2

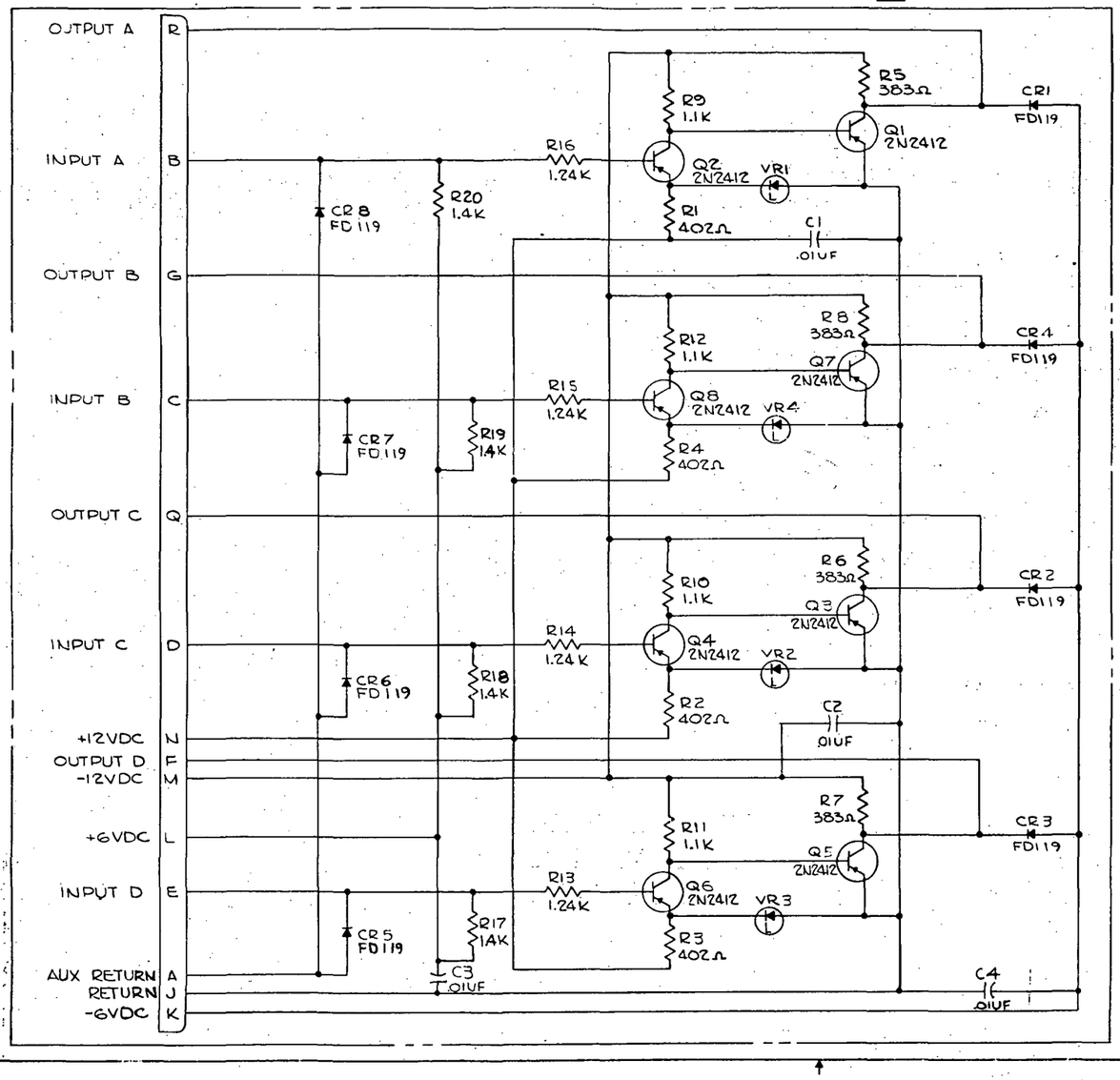
CIRCUIT	INPUT PIN	OUTPUT PIN
A	B	R
B	C	G
C	D	Q
D	E	F

Q1 THRU Q8	8
R17 THRU R20	13
R13 THRU R16	12
R9 THRU R12	11
R5 THRU R8	10
R1 THRU R4	9
CR5 THRU CR8	7
CR1 THRU CR4	7
VR1 THRU VR4	6
C1 THRU C4	5
REF DES	ITEM NO.

Figure 10-59. AN1 Translator Printed Circuit Board Assembly (6901330) (Sheet 1 of 2)

6901330 A

REVISIONS					
SYM	ENGRD NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BC	RELEASE	81 7		
A	66112DB	(1-3) ADD NOTE X	2154 JAN EVANS		



Q'TY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS ON EDGE MIN MAX

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES

MATL

HARD CASE DEPTH

SURF FINISH

CONTRACT NO.

DESIGNED J.E. Wood 9/4/63

DESIGN CHECK

DRAWN MDGE 9/23/63

DRAWING CHECK

DESIGN APPROVAL 10/18/63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY-
TRANSLATOR, AN1

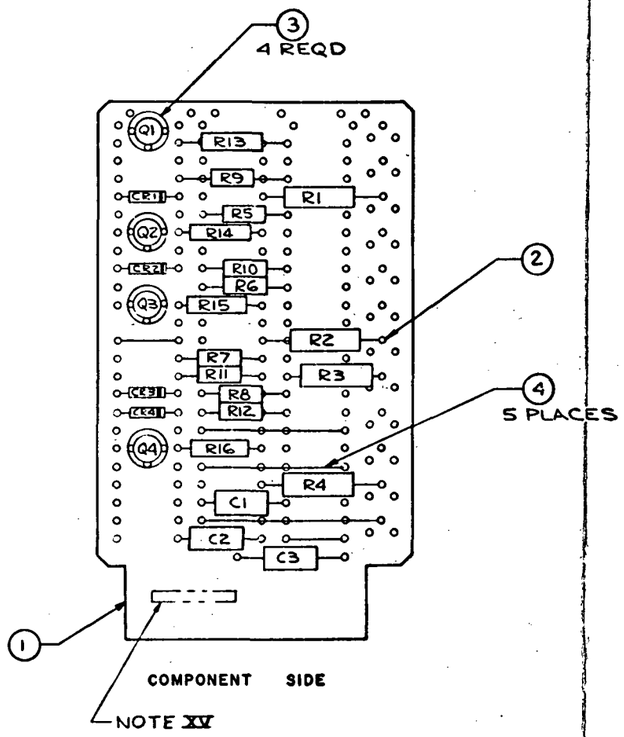
CODE IDENT NO. 03640 SIZE D 6901330

SCALE NONE WT SHEET 2

Figure 10-59. AN1 Translator Printed Circuit Board Assembly (6901330) (Sheet 2)

6901342 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6611288	RELEASE	12 31 6		
A	GG1216 (1)	CHANGE TRANSISTOR	2-8-6		EVANS



CIRCUIT	INPUT	OUTPUT
A	C	A
B	D	B
C	E	R
D	F	Q

C1,C2,C3	5
CR1 THRU CR4	6
Q1 — Q4	7
R1 — R4	8
R5 — R8	9
R9 — R12	10
R13 — R16	11
REF DES	ITEM NO.

NOTES

I IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901342 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
4	V	RES 330Ω ±1% 1/4W	6079238				11
4	V	RES 1.58K ±1% 1/8W	6079235				10
4	V	RES 3.32Ω ±1% 1/8W	6079236				9
4	V	RES 768Ω ±1% 1/2W	6079229				8
4	V	TRANSISTORS	369587				7
4	V	DIODE	6017645				6
3		CAP .01UF ±10% 100VDC	491228			56360	5
10 IN.	N/R	WIRE #22 AWG YELLOW	6036152				4
4		PAD	483070			88360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901341				1

(A)

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES 3 PLACE DECIMALS ± TOLERANCE ON 2 PLACE DECIMALS ANGLES ±
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

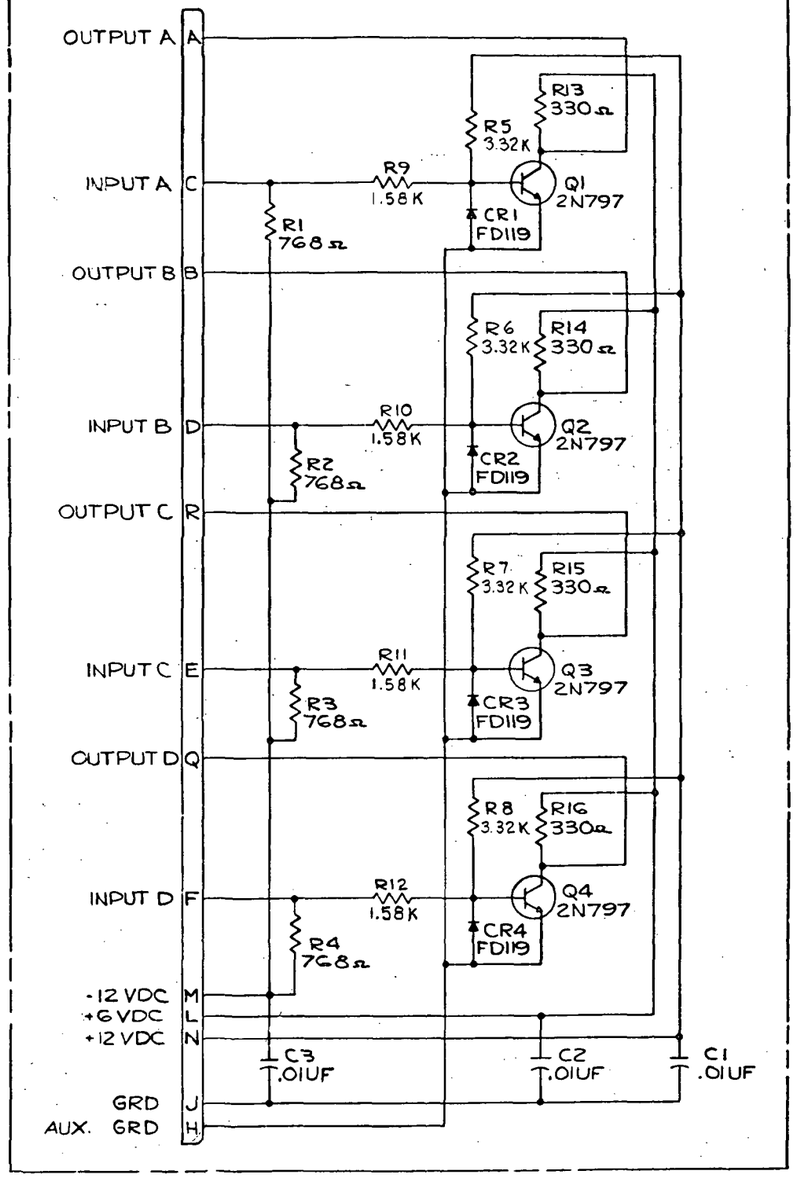
DESIGNED I. G. Wood 7-7-63
DESIGN CHECK 9/11/63
DRAWN MDE 9/11/63
DRAWING CHECK
DESIGN APPROVAL 12-11-63 12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY - NA2, TRASLATOR

CODE IDENT NO. 03640 SIZE D 6901342
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-60. NA2 Translator Printed Circuit Board Assembly (6901342) (Sheet 1 of 2)



6901342 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BB	RELEASE	12.31.63		
A	66112HG	(1) CHANGE TRANSISTOR	5/6/64		ELANS

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED J. S. Wood 9.26.63
DESIGN CHECK Tony Hilton 11/26/63
DRAWN MDE 9/12/63
DRAWING CHECK
DESIGN APPROVAL R. Page 12/2/63

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N. Y.

TITLE
PRINTED CIRCUIT BOARD ASSY - NA2, TRANSLATOR

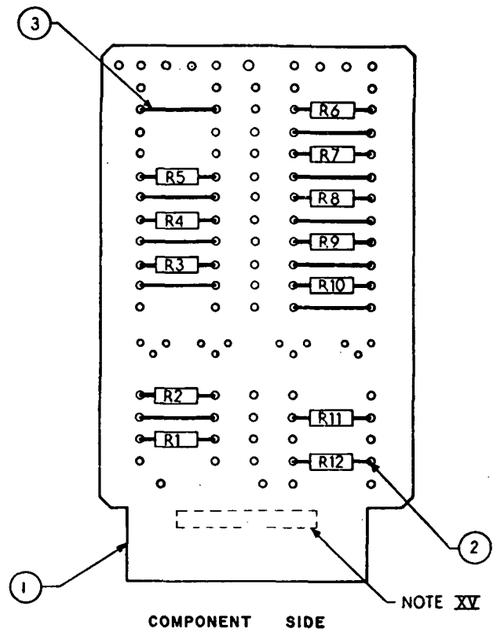
CODE IDENT NO. 03640 | SIZE D | 6901342

SCALE NONE WT SHEET 2

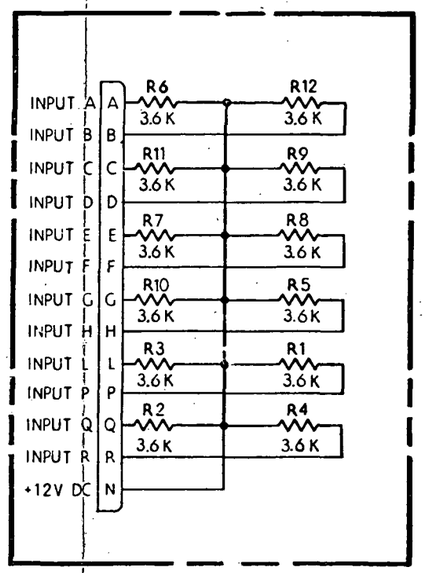
Figure 10-60. NA2 Translator Printed Circuit Board Assembly (6901342) (Sheet 2)

6901349

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6112BB	RELEASE	12-31-63		



COMPONENT SIDE



NOTES

- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6901349 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY

REF DES	ITEM NO.
R1 TO R12	4

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
12		RESISTOR 3.6K,1/4W ±5%	334523			88360	4
16 IN	R	WIRE #22 AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	492345			88360	1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES 2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±1°
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED — DATE 12-6-63
DESIGN CHECK — 12-6-63
DRAWN — 9-25-63
DRAWING CHECK
DESIGN APPROVAL — 12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

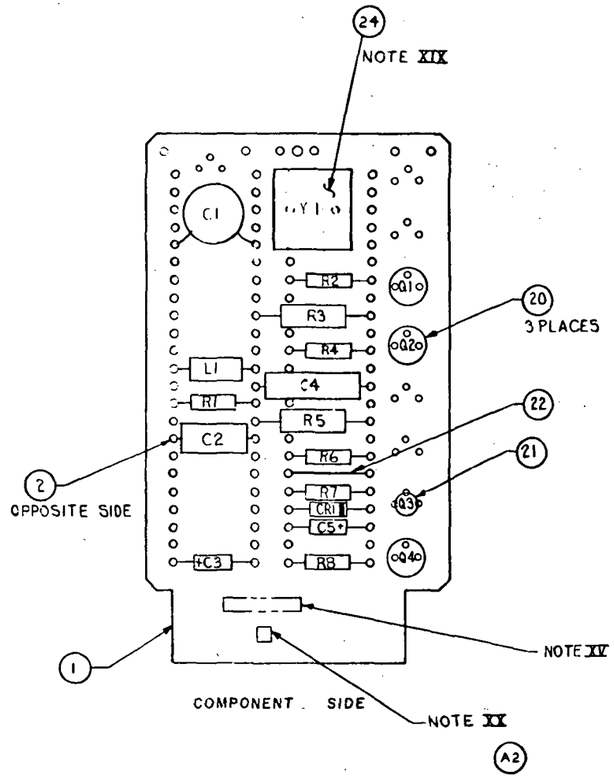
TITLE: PRINTED CIRCUIT BOARD ASS'Y— 3.6K RESISTOR

CODE IDENT NO. 03640 | SIZE D | 6901349
SCALE 2/1 | WT | SHEET

Figure 10-61. 3.6K Resistor Printed Circuit Board Assembly (6901349)

6901352 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BU	RELEASE	[illegible]		
A	66115 KG	(1-2) ADDED NOTES XIX AND XX AND ITEM 24 R-2641			J.E. WOOD



C2	23
Y1	19
Q4	18
Q3	17
Q1-Q2	16
R8	15
R7	14
R6	13
R5	12
R4	11
R3	10
R2	9
R1	8
L1	7
CR1	6
C4	5
C3, C5	4
C1	3
REF DES	ITEM NO.

XI MARK CHANGE LEVEL TYPE I CLASS I COLOR BLACK PER SPEC 6009974

NOTES

- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6901352 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY
- XIX UPPER HALF OF CRYSTAL CAN SHALL BE INSULATED WITH SEALANT INDICATED PER IBM SPEC 6009341. CRYSTAL SHOULD NOT BE SUBJECTED TO TEMP OVER 150°F IN CURING

A1

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
AR	V	SEALANT	6075477				24
1		CAPACITOR 7PF±5%500V	492515			58360	23
3 IN	V,R	WIRE, #22AWG, YELLOW	6036152				22
1		SPACER	483070				21
3		SPACER	491299			58360	20
1	V	CRYSTAL 2.048 MC	6079504				19
1			318325				18
1			369177				17
2		TRANSISTOR	526798				16
1		510Ω ±5% 1/2W	317012				15
1		1.6K ±5% 1/2 W	317018				14
1		2.94K ±1% 1/8W	479127				13
1		1.78K ±1% 1/4W	479226				12
1		1.3K ±1% 1/8W	550093				11
1		1.0K ±1% 1/4W	491010				10
1		1.5K ±5% 1/2 W	317017				9
1		RESISTOR 523Ω ±1% 1/8W	491238				8
1		INDUCTOR 12 UH ±5%	217136				7
1		DIODE	491008				6
1		75PF	492464				5
2		1UF	124582				4
1		CAPACITOR 430PF ±5% 100V	483309			58360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901353				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX, INSIDE MIN MAX. ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ±.01, 3 PLACE DECIMALS ±.005, ANGLES ±1°. MATL. HARD. TEST BY. CASE DEPTH. CONTRACT NO.

DESIGNED [illegible] DATE [illegible]
DESIGN CHECK [illegible] 7/1/63
DRAWN [illegible] 6/21/63
DRAWING CHECK
DESIGN APPROVAL [illegible] 6-27
[illegible] 7-8 64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT BOARD ASSY-2.048 M.C. OSCILLATOR, SDTDL

CODE IDENT NO. 0364C | SIZE D | 6901352
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-62. 2.048 MC Oscillator Printed Circuit Board Assembly (6901352) (Sheet 1 of 2)

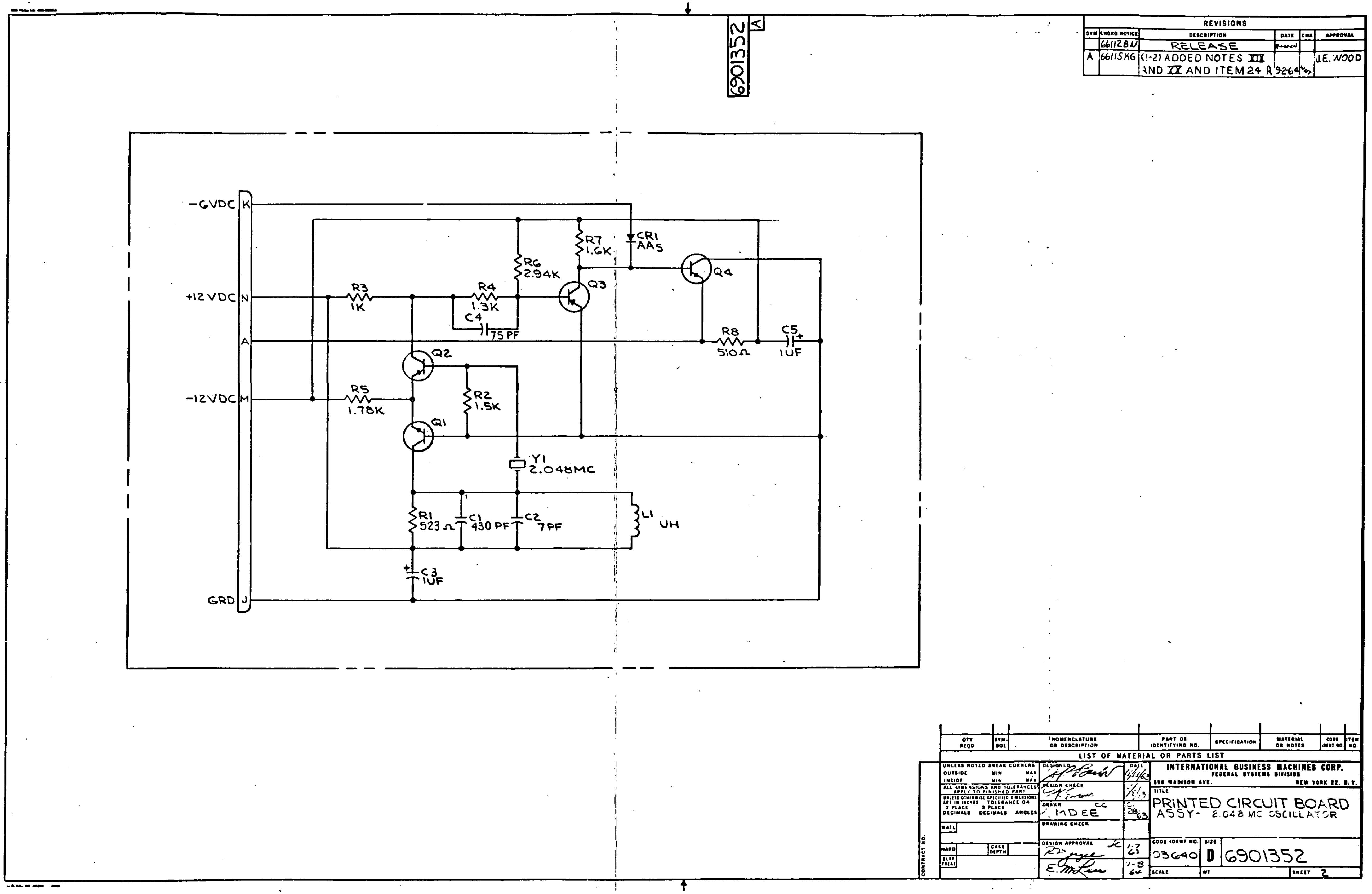
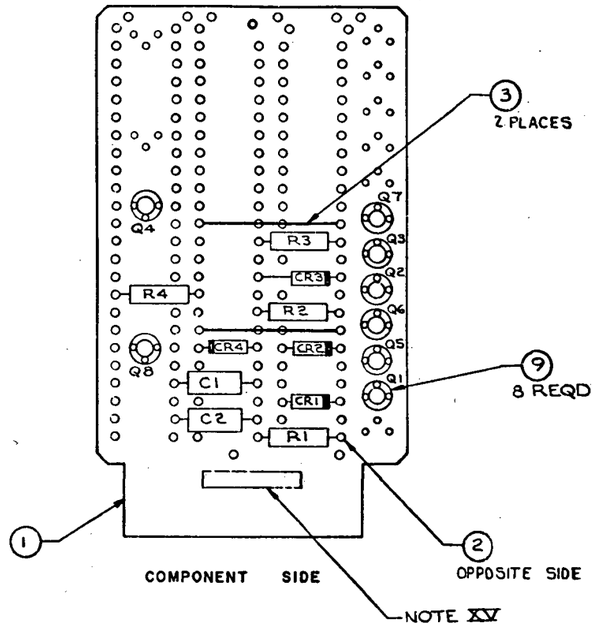


Figure 10-62. 2.048 MC Oscillator Printed Circuit Board Assembly (6901352) (Sheet 2)

6901356

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66128N	RELEASE			



CIRCUIT	INPUT PIN	OUTPUT PIN
A	G	B
B	E	A
C	D	C
D	R	Q

R1-R4	8
Q5-Q8	7
Q1-Q4	6
CR1-CR4	5
C1 & C2	4
REF DES	ITEM NO.

NOTES

XI IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901356 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

QTY REQD.	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
8		PAD	483070			88360	9
4	V	RESISTOR 26.1Ω ±1% 1/4W	6079906				8
4	V	TRANSISTOR	6079006				7
4	V	TRANSISTOR	6079221				6
4	V	DIODE	6017645				5
2		CAP, .01UF ±10% 100VDC	491228			88360	4
6 IN.	VR	WIRE NO.22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901357				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

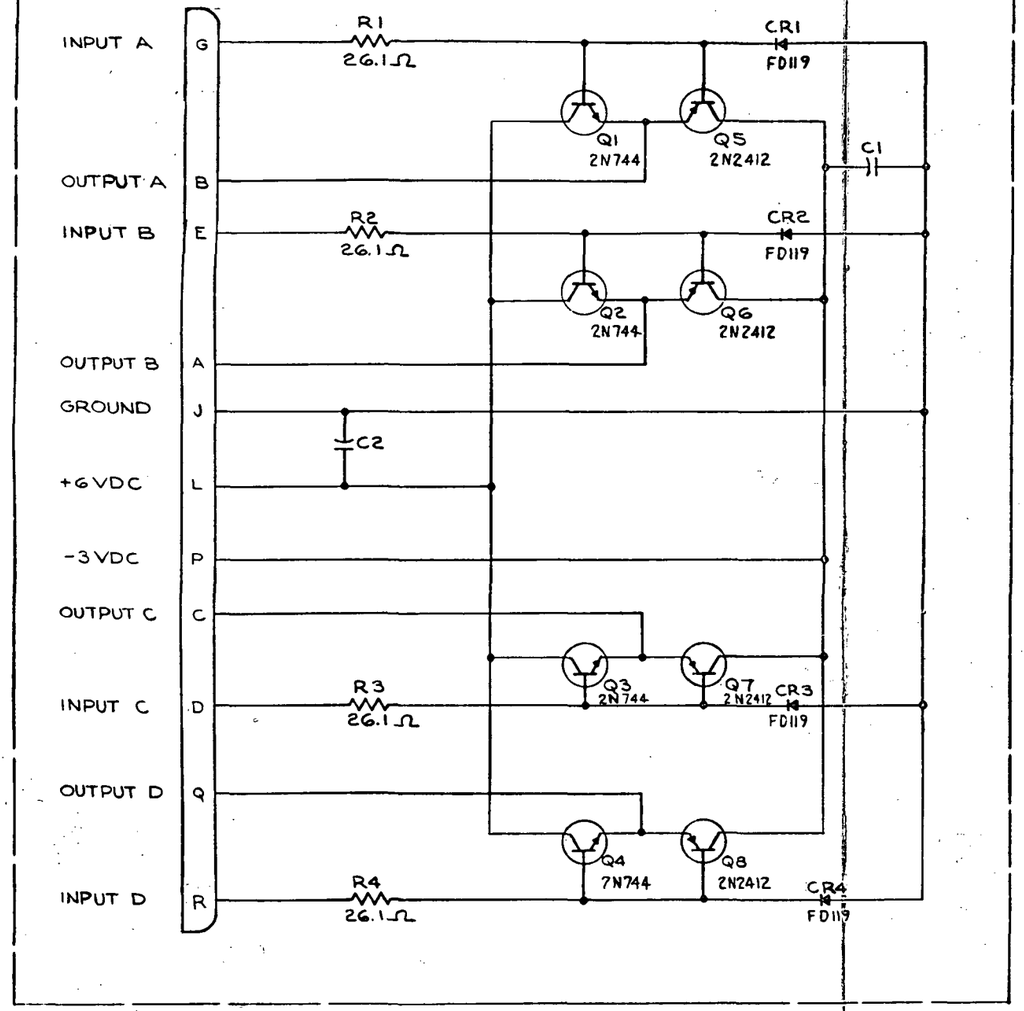
DESIGNED R. L. Wood 12-6-64
DESIGN CHECK L. A. Nelson 12-2-64
DRAWN MD: E 12-18-63
DRAWING CHECK
DESIGN APPROVAL R. J. Joyce 1-7-65
E. McLure 1-8-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.
TITLE PRINTED CIRCUIT BOARD ASSY-CD1
CODE IDENT NO. 03640 SIZE D 6901356
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-63. CD1 Printed Circuit Board Assembly (6901356) (Sheet 1 of 2)

6901356

REVISIONS					
SYM	ENGR'G NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	64112BM	RELEASE			



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES

MATL
HARD
SURF TREAT
CASE DEPTH

DESIGN	J. E. Wood	1-2-64
DESIGN CHECK	W. A. Morton	1-2-64
DRAWN	MD&E	1-10-64
DRAWING CHECK		
DESIGN APPROVAL	R. Jaeger	1-7-64
	E. McLean	1-8-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY- CD

CODE IDENT NO. 03640 | SIZE D | 6901356

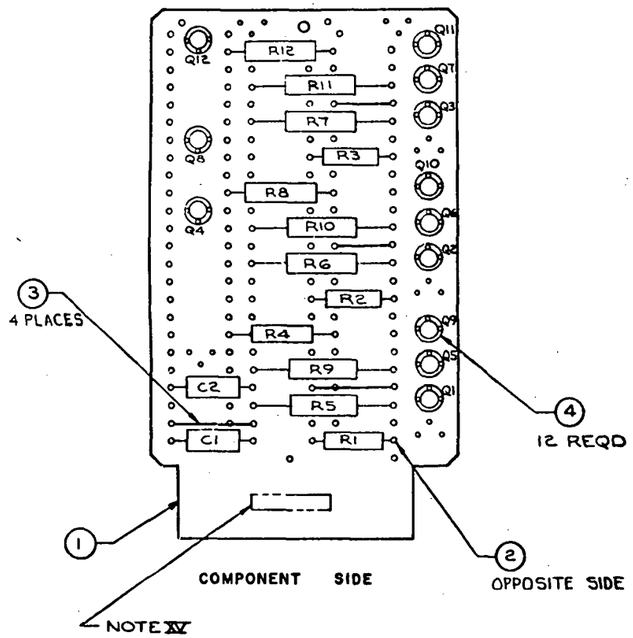
SCALE NONE | WT | SHEET 2

CONTRACT NO.

Figure 10-63. CD1 Printed Circuit Board Assembly (6901356) (Sheet 2)

6901358

REVISIONS					
SYS	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BN	RELEASE			



CIRCUIT	INPUT PIN	OUTPUT PIN
A	G	A
B	F	B
C	D	C
D	E	R

R9-R12	10
R5-R8	9
R1-R4	8
Q1-Q4, Q9-Q12	7
Q5-Q8	6
C1 & C2	5
REF DES	ITEM NO.

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901358 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	6.49Ω ±1% 1/2W	6079907				10
4	V	1.0K ±1% 1/4W	6079905				9
4	V	RESISTOR 1.0K ±1% 1/8W	6079220				8
8	V	TSTR	6079909				7
4	V	TSTR	6079006				6
2		CAP, .01UF ±10% 100VDC	491228			88340	5
12		PAD	483070			88340	4
10 IN	VR	WIRE NO. 22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901359				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED FOR DECIMAL DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED T.C. Wood DATE 12-2-64
DESIGN CHECK 1/1/64
DRAWN MD & E 12-18-63
DRAWING CHECK
DESIGN APPROVAL 12-23-63
1/6/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

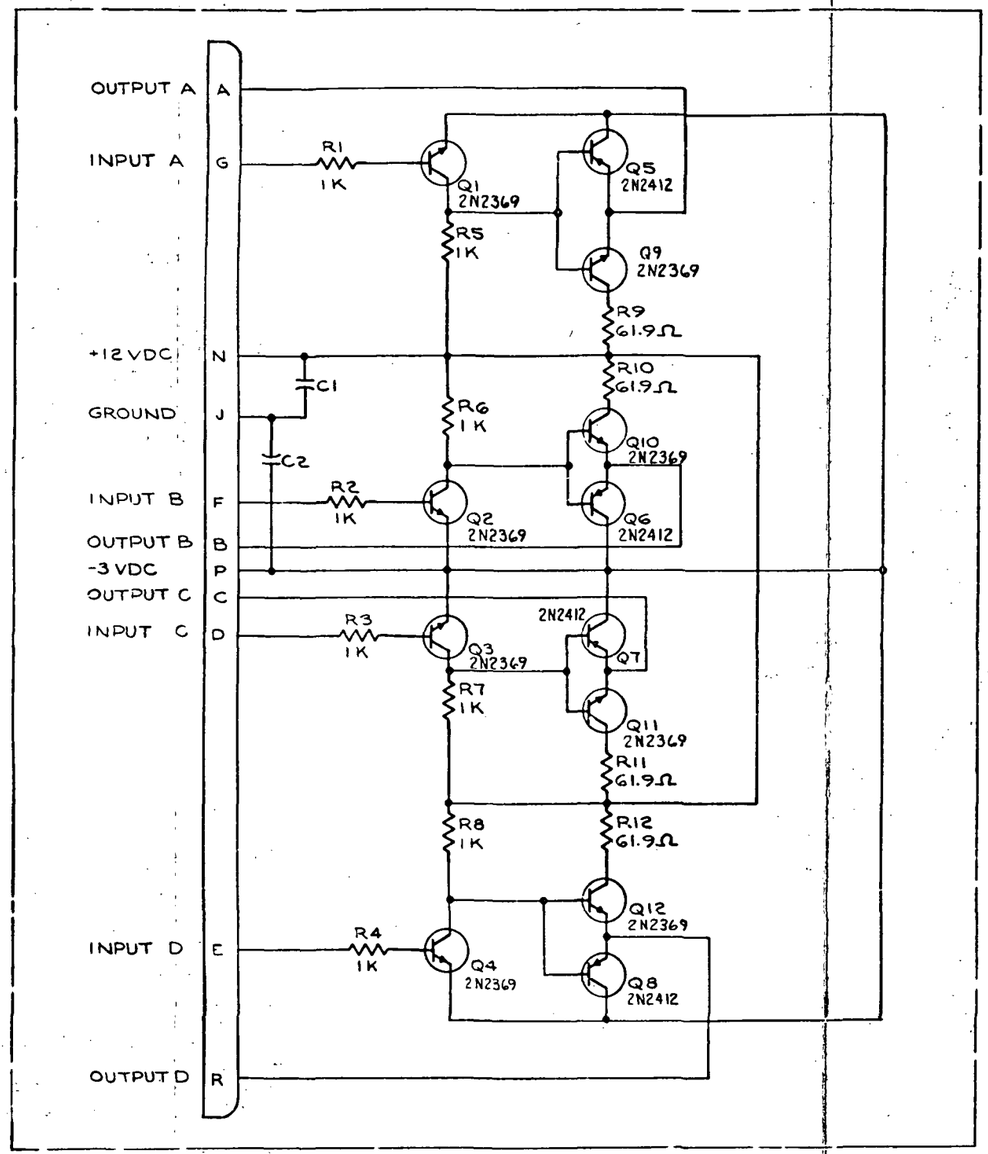
TITLE
PRINTED CIRCUIT BOARD ASSY- SC3

CODE IDENT NO. 03640 SIZE D 6901358
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-64. SC3 Printed Circuit Board Assembly (6901358) (Sheet 1 of 2)

6901358

REVISIONS					
SYM	CHANG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BU	RELEASE			



QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED J. E. Wood 12-30-63
DESIGN CHECK 1/4/64
DRAWN MD & E 2-18-63
DRAWING CHECK
DESIGN APPROVAL 1-7-64
1-8-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY- SC3

CODE IDENT NO. 03640 | SIZE D | 6901358

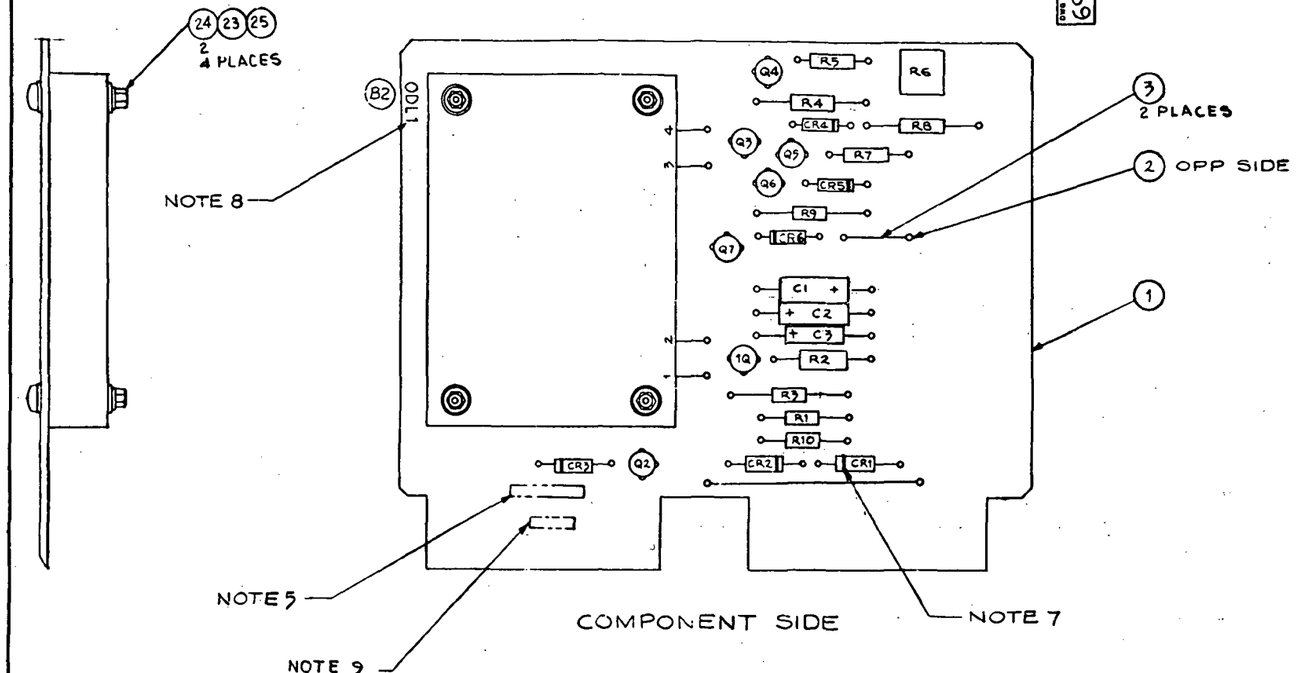
SCALE NONE | WT | SHEET 2

Figure 10-64. SC3 Printed Circuit Board Assembly (6901358) (Sheet 2)

SOURCE OF SUPPLY			
VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR PR

DWG NO. 6942024 B

REVISIONS						
SYM	ENGRG NOTICE	DESCRIPTION R	DATE	CHK	APPROVAL
A	66115KF	REDRAWN WITH CHANGE	8-31-66		J.E.Wood
B	66-1515	(1-21) SEE ENGRG NOTICE R	10-26-66		J.E.WOOD



NOTES

1. MIN ELECTRICAL CLEARANCE TO BE .018
2. COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
3. COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCH
4. LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
5. MARK 6942024 ASSY TYPE I CLASS 1 COLOR BLACK
6. JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
7. BLACK BAND DENOTES CATHODE END OF DIODE
8. MARK TYPE III CLASS 1 COLOR BLACK
9. MARK REV. LEVEL .12 HIGH CHARACTERS TYPE I CLASS 1 COLOR BLACK

REF DES	ITEM NO
CR2	26
Q6,7	21
Q5	20
Q2,3,4	19
Q1	18
CR3	17
CR1, 4,5,6	16
DL1	15
C1,2	14
C3	13
R10	12
R9	11
R7,8	10
R6	9
R5	8
R4	7
R3	6
R2	5
R1	4

B1

QTY REQD	SYM SOC	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
1	VI	DIODE	6082082				26
4		LOCKNUT (6072821)	NAS1291A04M				25
8		WASHER (6048641)	MS15795-303				24
4		SCREW (6035704)	MS35216-18				23
7		PAD	483070			88360	22
2	VI	(152)	369587			88360	21
1	VI	(2N744)	6079221				20
3	VI	(2N2412)	6079006				19
1	VI	TRANSISTOR (102)	369179			88360	18
1		DIODE (6076930)	USN IN3600				17
5		DIODE (6034674)	USN IN3064				16
1		DELAY LINE 80.456 MSEC	6081631				15
2		CAPACITOR 4.7mF, 35V ±20%	6018793				14
1		CAPACITOR 4.7mF, 10V ±20%	6018707				13
1		(6078199)	RC07GF561J				12
1		(6020825)	RC07GF682J				11
2		(6017158)	RN60C5760F				10
1		VARIABLE 2K	6079650				9
1		(6081630)	RN60C2211F				8
1		(6081629)	RN60C1132F				7
1		(6056034)	RC07GF332J				6
1		(6012288)	RC20GF681J				5
1		RESISTOR (6037004)	RC07GF752J				4
5 IN	V,R	WIRE, YELLOW #22	6036152				3
AR		SOLDER (6032357)	SN60AR	QQ-S-571			2
1		SMS CARD	6942025				1

LIST OF MATERIAL OR PARTS LIST

6009974 589
6003003

SPEC NUMBER | NOTE | ITEM NO. APPLIES TO

APPLICABLE IBM SPEC

☐ ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S), HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN (1). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

☐ COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG P-PART QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES

MATL

HARD | CASE DEPTH

S-BY CLASS

DESIGNED	J.E. Wood	8/31/66
DESIGN CHECK	J.J. Ulrich	9-4-66
DRAWN	J. McDonald	6-28-67
DRAWING CHECK		
DESIGN APPROVAL		6/9/67

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE
PRINTED CIRCUIT ASSY
ODL1
LVDA - MANUAL EXERCISER

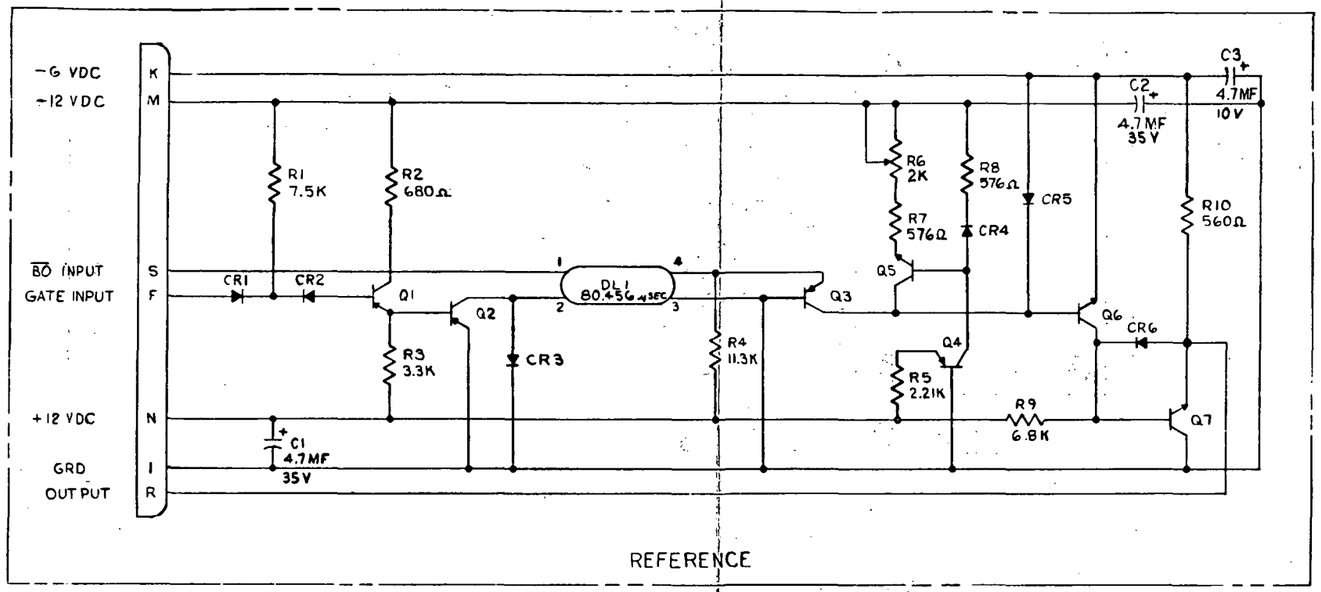
CODE IDENT NO.	SIZE	DRAWING NO.
03640	D	6942024

SCALE 2/1 WT SHEET 1 OF 2

Figure 10-65. ODL1 Printed Circuit Board Assembly (6942024) (Sheet 1 of 2)

6942024 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
A	66115KF	REDRAWN WITH CHANGE R	3-31-		J.E. Wood
B	66115LS	SEE ENGRG NOTICE	R 3-31-66	H.	J.E. WOOD



REFERENCE

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS SHARP
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±1°
MATL
HARD
SURF TREAT
CASE DEPTH
CONTRACT NO.

DESIGNED J.E. Wood
DESIGN CHECK T.J. Ulrich
DRAWN J.E. Wood 3-31-66
DRAWING CHECK
DESIGN APPROVAL R Engel 4/8/66 4-10-66

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

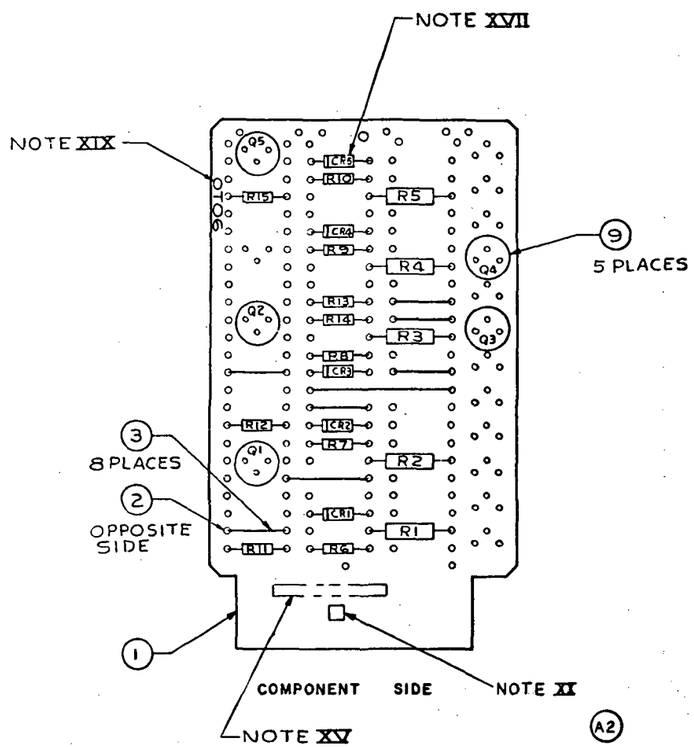
TITLE PRINTED CIRCUIT ASSY-ODL 1

CODE IDENT NO. 03640 | SIZE D | 6942024
SCALE NONE | WT | SHEET 2

Figure 10-65. ODL1 Printed Circuit Board Assembly (6942024) (Sheet 2)

6942026 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115Z	RELEASE R	5-20-64		
A	66115KG	(1-3) CHG ITEM 5, ADD NOTE XX R	9-24-64		J.E. WOOD
B	66115MS	(1) CHG P/N ITEM 4 R	11-2-64		J.E. WOOD



NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6942026 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX APPLY.09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK
XX MARK LATEST REV LEVEL TYPE I CLASS I COLOR BLACK PER 6009974

Q1 - Q5	8
CR1 - CR5	7
R11 - R15	6
R6 - R10	5
R1 - R5	4
REF DES	ITEM NO.

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
5		SPACER	491299			88360	9
5		TRANSISTOR	318324			88360	8
5	V	DIODE	6079734				7
5		T (6078199)	RC07GF561J				6
5		6081432	RN60C3011F				5
5		RESISTOR (6010101)	RN60C1002F				4
6 IN.	V,R	WIRE #22AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942027				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE .010 MAX INSIDE .010 MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±1°
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED E Hack 5-4-64
DESIGN CHECK L E Wood 5-7-64
DRAWN VMD 4-27-64
DRAWING CHECK
DESIGN APPROVAL R D Joyce 5-21-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

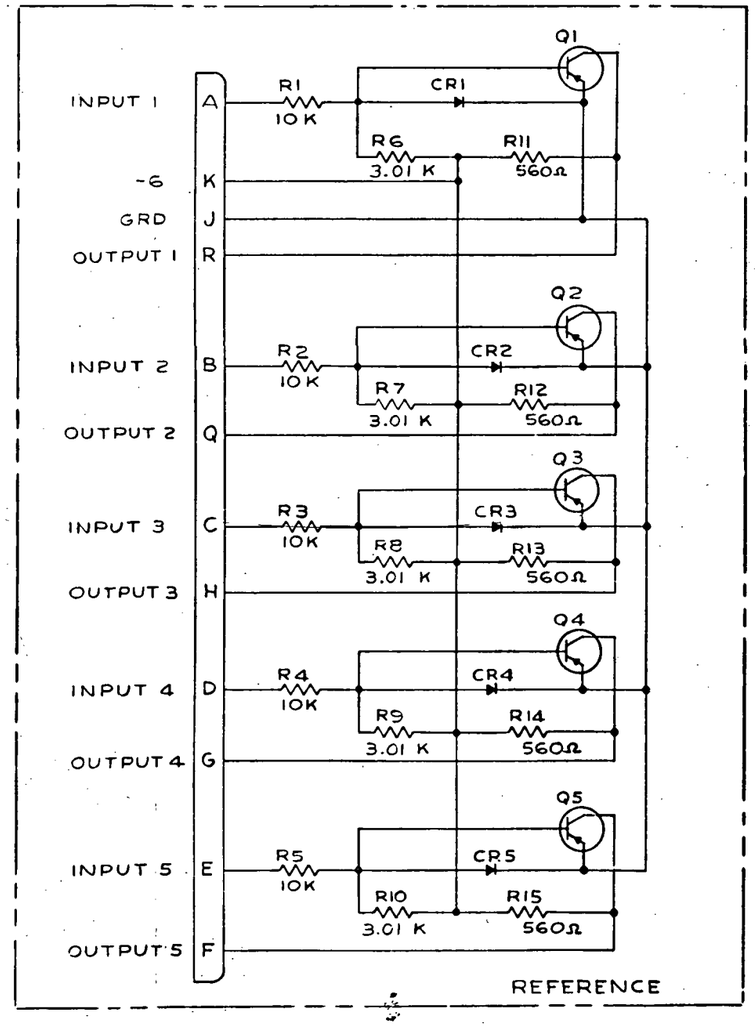
TITLE PRINTED CIRCUIT ASSY-OTO6

CODE IDENT NO. 03640 SIZE D 6942026
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-66. OTO6 Printed Circuit Board Assembly (6942026) (Sheet 1 of 2)

6942026 B

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115Z	RELEASE	5-20-64	K	
A	66-15KG	(1-4) CHG ITEM 5, ADD NOTE XX	7-24-64		J.E. WOOD
B	66115MS	(1) CHG P/N ITEM 4	9-28-64		J.E. WOOD



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ±, 3 PLACE DECIMALS ±, ANGLES ±
MATL
HARD
SURFACE
CASE DEPTH
CONTRACT NO.

DESIGNED E Hudnut 5-7-64
DESIGN CHECK R.E. Wood 5-7-64
DRAWN VMD 4-27-64
DRAWING CHECK
DESIGN APPROVAL R Bryck 5-11-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

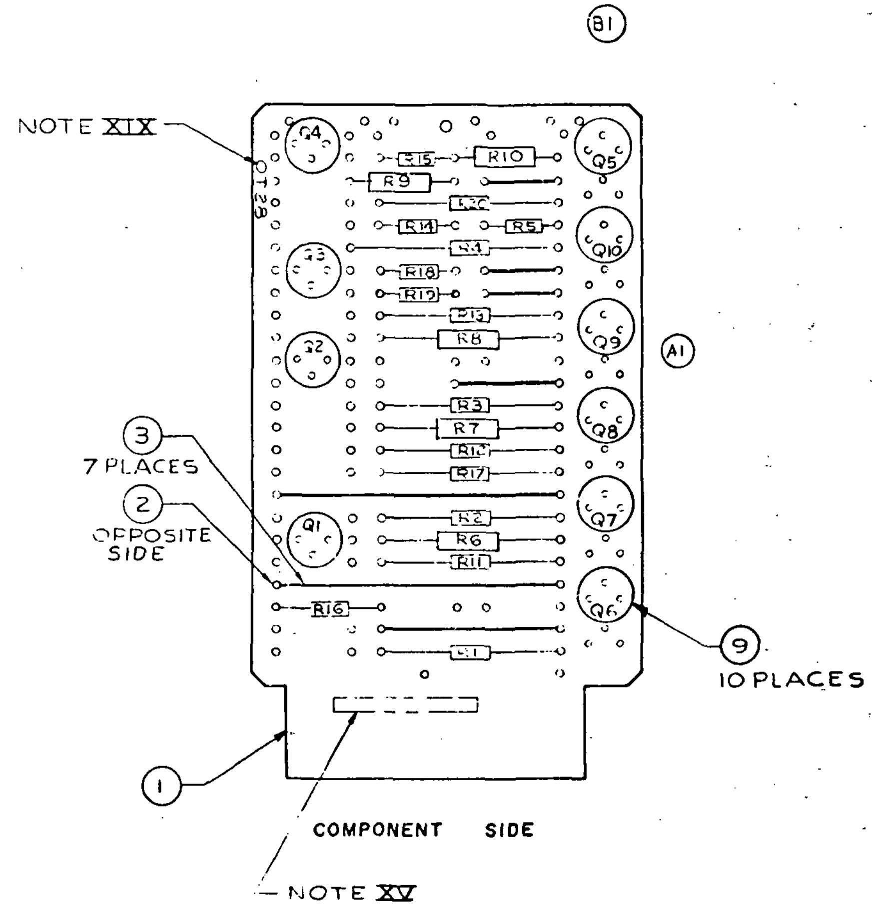
TITLE PRINTED CIRCUIT ASSY-OTO6

CODE IDENT NO. C3640 | SIZE D | 6942026
SCALE NONE | WT | SHEET 2

Figure 10-66. OTO6 Printed Circuit Board Assembly (6942026) (Sheet 2)

6942028 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6115 Z	RELEASE	5-20-4		
A	6115FA	(1-5) CHGD R1-R10	6/29/64		J.E. WOOD
B	56115-B	(1) R20 WAS S-OWN AS R16	9/23/64		J.E. WOOD



NOTES

- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6942028 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY
- XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

(A3)

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
5		RESISTOR (6081377)	RN60C8871F				10
10		SPACER	491259			88360	9
5		TRANSISTOR	492452			88360	8
5		TRANSISTOR	369114			88360	7
5	V	(6020133)	RC07GF271J				6
5	V	(6020826)	RC07GF103J				5
5	V	RESISTOR (6020824)	RC07GF362J				4
24 IN.	R	WIRE #22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942029				1

LIST OF MATERIAL OR PARTS LIST

REF DES	ITEM NO.
R6-R10	10
Q6-Q10	8
Q1-Q5	7
R11-R15	6
R16-R20	5
R1-R5	4

(A2)

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE 3 PLACE DECIMALS DECIMALS ANGLES

DESIGNED: E. [signature] DATE 5-4-64
DESIGN CHECK: J.S. Wood
DRAWN: VMD 5-64
DRAWING CHECK
DESIGN APPROVAL: [signature]

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT ASSY-OT28

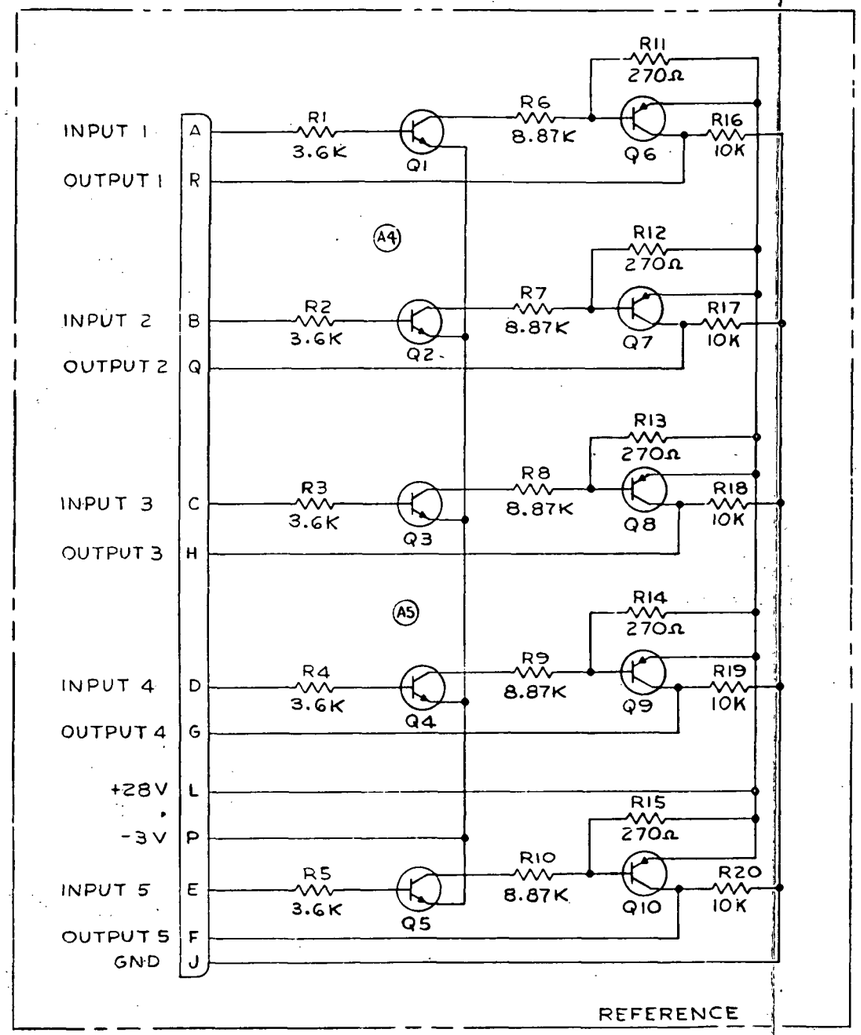
CODE IDENT NO. 03640 SIZE D 6942028

SCALE 2/1 SHEET 1 OF 2

Figure 10-67. OT28 Printed Circuit Board Assembly (6942028) (Sheet 1 of 2)

6942028 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115 Z	RELEASE R	5-20-64		
A	66115FA	(1-5) CHGD R1-R10	6/5/64	VC	J.E. WOOD
B	66115_3	(1) R20 WAS SHOWN AS R15	8/28/64	VC	JE WOOD



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±

MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED E Hudak 5-6-64
DESIGN CHECK
DRAWN VMD 5-5-64
DRAWING CHECK
DESIGN APPROVAL 5-11-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

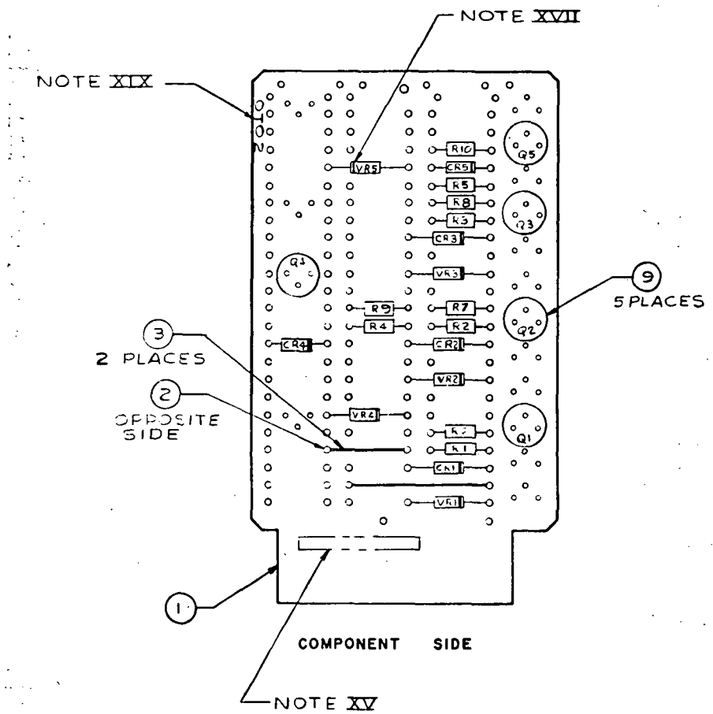
TITLE
PRINTED CIRCUIT ASSY-
OT28

CODE IDENT NO. 03640 SIZE D 6942028
SCALE NONE SHEET 2

Figure 10-67. OT28 Printed Circuit Board Assembly (6942028) (Sheet 2)

6942030

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115AD	RELEASE			



NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6942030 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

21	8
CR1-CR5	7
VR1-VR5	6
R6-R10	5
R1-R5	4
REF DES	ITEM NO.

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
5		SPACER	491299				9
5		TRANSISTOR	313324				8
5	V	DIODE	6079734				7
5	V	DIODE, ZENER	6020220				6
5		RESISTOR (6078139)	RC07GF561J				5
5		RESISTOR (6056035)	RC07GF472J				4
3 IN.	VR	WIRE, INS #22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942031				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS AND TOLERANCE ON 3 PLACE DECIMALS 2 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF FINISH

DESIGNED — DATE
DESIGN CHECK J.C. Wood 5-22-64
DRAWN V.M.C. 5-14-64
DRAWING CHECK
DESIGN APPROVAL E.B. Jezzi 5-29-64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT ASSY-OTO2

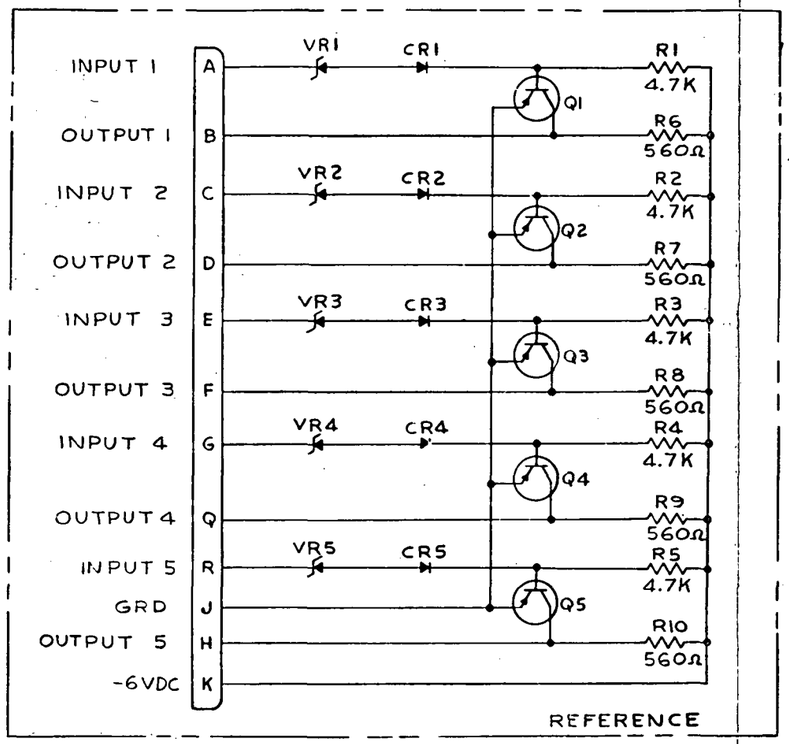
CODE IDENT NO 03640 | SIZE D | 6942030

SCALE 2/1 WT SHEET 1 OF 2

Figure 10-68. OTO2 Printed Circuit Board Assembly (6942030) (Sheet 1 of 2)

6942030

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115AD	RELEASE	R 3/24		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAY
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS DIMENSIONS ARE IN INCHES 2 PLACE DECIMALS ± TOLERANCE ON 3 PLACE DECIMALS ANGLES ±
MATL
HARD SURF TREAT CASE DEPTH
CONTRACT NO.

DESIGNED C Hudock 6-11-64
DESIGN CHECK J.S. Wood 5-22-64
DRAWN VMD 5-11-64
DRAWING CHECK
DESIGN APPROVAL 5/25/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE PRINTED CIRCUIT ASSY-OTO2

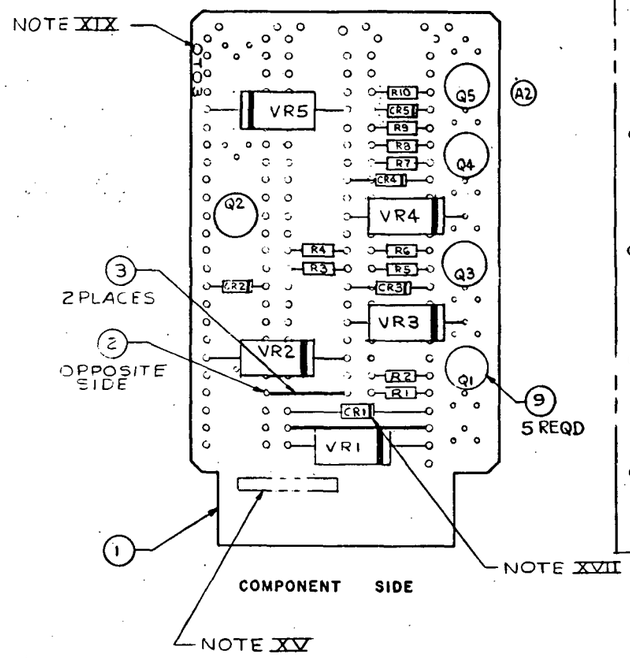
CODE IDENT NO. 03640 | SIZE D | 6942030

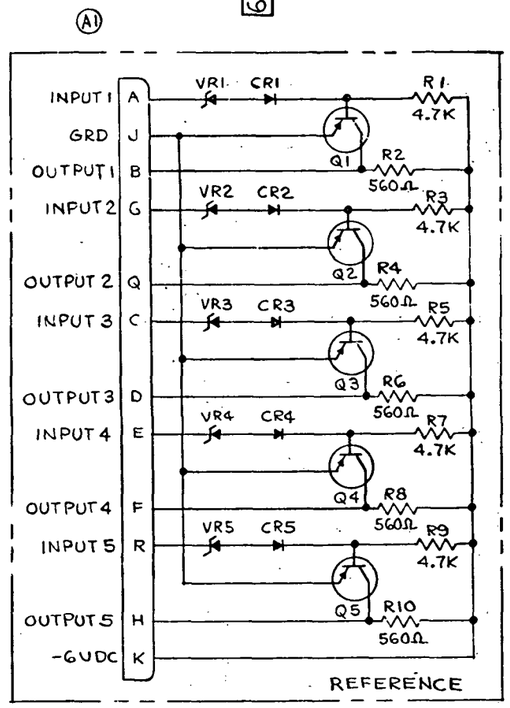
SCALE JONE | SHEET 2

Figure 10-68. OTO2 Printed Circuit Board Assembly (6942030) (Sheet 2)

6942032 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115AD	RELEASE			
A	66115FA	(1-9 ADDED 4 MORE CIRCUITS, PER ECO [illegible]			





NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PART MARK 6942032 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

Q1-Q5	8
CR1-CR5	7
VR1-VR5	6
R2, R4, R6, R8, R10	5
R1, R3, R5, R7, R9	4
REF DES	ITEM NO.

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
5		SPACER	491299			89369	9
5		TRANSISTOR	318324			28360	8
5	V	DIODE	6079734				7
5	V	DIODE, ZENER	6016360				6
5		RESISTOR (6078199)	RC07GF561J				5
5		RESISTOR (6056035)	RC07GF472J				4
3 IN	V	WIRE, INS #22AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942031				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± .01, 3 PLACE DECIMALS ± .005, ANGLES ± 1°
MATL
HARD CASE DEPTH
SURF FINISH

DESIGNED E Hudock 5-7-64
DESIGN CHECK E Wood 5-7-64
DRAWN VMD 5-7-64
DRAWING CHECK
DESIGN APPROVAL [signature] 5/7/64

CONTRACT NO.

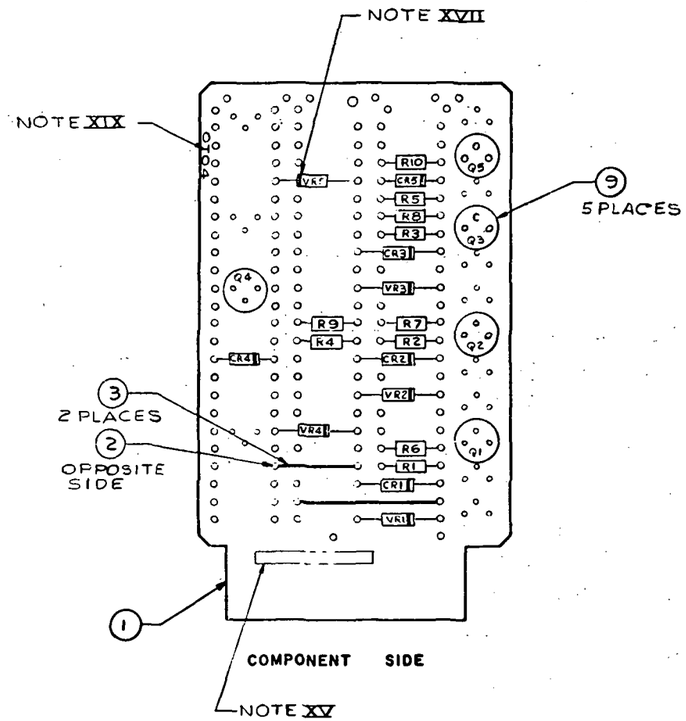
INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
326 MADISON AVE. NEW YORK 22, N.Y.

TITLE PRINTED CIRCUIT ASSY-OTO3

CODE IDENT NO 03640 | SIZE D | 6942032

SCALE 2/1 | WT | SHEET

Figure 10-69. OTO3 Printed Circuit Board Assembly (6942032)



Q1	8
CR1-CR5	7
VR1-VR5	6
R6-R10	5
R1-R5	4
REF DES	ITEM NO.

6942033

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	661154D	RELEASE			

NOTES

- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6942033 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY
- XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
5		SPACER	491299			88360	9
5		TRANSISTOR	318324			88360	8
5	V	DIODE	6079734				7
5	V	DIODE, ZENER	6077221				6
5		RESISTOR(6078199)	RC07GF561J				5
5		RESISTOR(6056035)	RC07GF472J				4
3 IN.	VR	WIRE, INS. #22AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942031				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD
BUFF TREAT
CASE DEPTH
CONTRACT NO.

DESIGNED E. Mark 5/9/64
CLASS CHECK J.E. Wood 5/12/64
DRAWN VMD 5/9/64
DRAWING CHECK
DESIGN APPROVAL 5/9/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

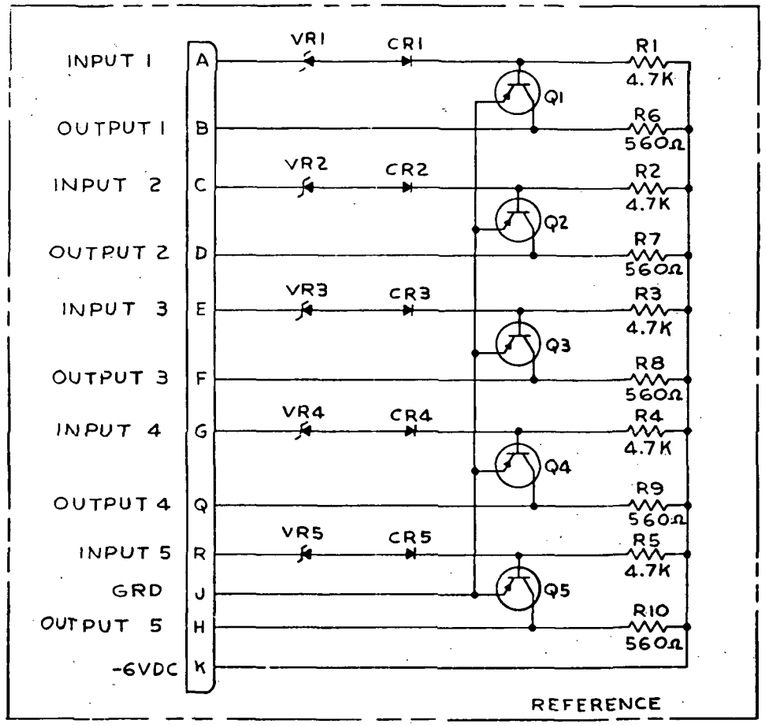
TITLE PRINTED CIRCUIT ASSY. OTO4

CODE IDENT NO. 03640 SIZE D 6942033
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-70. OTO4 Printed Circuit Board Assembly (6942033) (Sheet 1 of 2)

6942033

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115AD	RELEASE	5/28/64		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE STATED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD
STRESS RELIEF
CASE DEPTH
CONTRACT NO.

DESIGNED E Hubsch 5-11-64
DESIGN CHECK R.E. Wood 5-22-64
DRAWN VMD " 5-11-64
DRAWING CHECK
DESIGN APPROVAL R Jagel 5-25-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

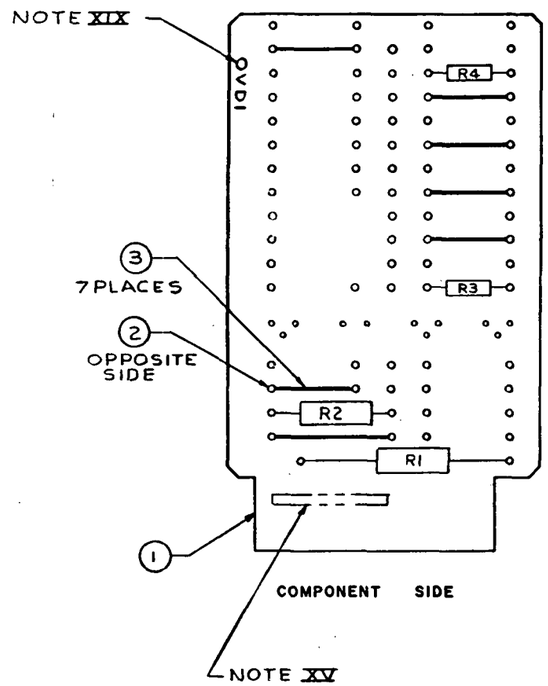
TITLE PRINTED CIRCUIT ASSY. OTO4

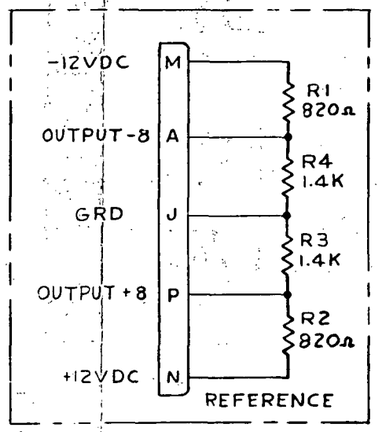
CODE IDENT NO. 03640 SIZE D 6942033
SCALE NONE WT SHEET 2

Figure 10-70. OTO4 Printed Circuit Board Assembly (6942033) (Sheet 2)

6942036

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115AD	RELEASE	5/18/64		





NOTES

- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6942036 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY
- XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

REF DES	ITEM NO.
R3, R4	5
R1, R2	4

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
2	V	RESISTOR 1.4K, ±1%, 1/8W	6017392				5
2	V	RESISTOR 820Ω, ±1%, 1/4W	6010165				4
10 IN	VR	WIRE, #22 AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	492345			88360	1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS. OUTSIDE MIN MAX, INSIDE MIN MAX. ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ±.01, 3 PLACE DECIMALS ±.005, ANGLES ±1°. MATL. HARD. SURF TREAT. CASE DEPTH. CONTRACT NO.

DESIGNED E. Hudak 5-12-64
DESIGN CHECK E. W. [illegible]
DRAWN VMD 5-12-64
DRAWING CHECK
DESIGN APPROVAL [illegible]

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT ASSY-OVD1

CODE IDENT NO. 03640 | SIZE D | 6942036

SCALE 2/1 | WT | SHEET

Figure 10-71. OVD1 Printed Circuit Board Assembly (6942036)

SOURCE OF SUPPLY

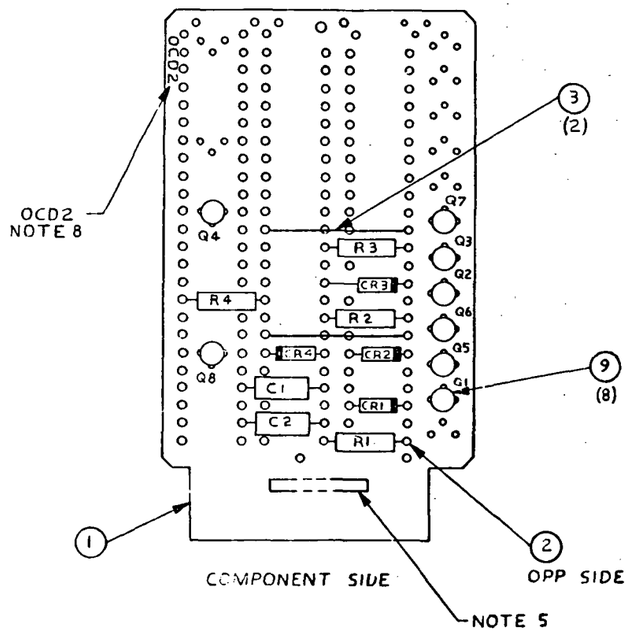
VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

DWG NO. 6942037

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115FL	RELEASE			

NOTES.

1. MIN ELECTRICAL CLEARANCE TO BE .018
2. COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
3. COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
4. LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
5. MARK 6942037 ASSY TYPE I CLASS I COLOR BLACK
6. JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
7. BLACK BAND DENOTES CATHODE END OF DIODE
8. MARK TYPE III CLASS I COLOR BLACK



CIRCUIT	INPUT PIN	OUTPUT PIN
A	G	B
B	E	A
C	D	C
D	R	Q

R1-R4	8
Q5-Q8	7
Q1-Q4	6
CR1-CR4	5
C1, C2	4
REF DES	ITEM NO.

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
8		PAD	483070			88360	9
4	V	RESISTOR 50Ω ±1% 1/4W	6017937				8
4	V	TRANSISTOR	6079006				7
4	V	TRANSISTOR	6079221				6
4	V	DIODE	6017645				5
2		CAP., .01UF ±10% 100VDC	491228			88360	4
6 IN.	V,R	WIRE NO 22 AWG YEL	6036152				3
AR		SOLDER (6032357)	SN 60 AR	QQ-S-571			2
1		SMS CARD	6901357				1

LIST OF MATERIAL OR PARTS LIST

6009974	5,E	
6000003		

SPEC NUMBER | NOTE (ITEM NO. APPLIES TO) | APPLICABLE IBM SPEC

☐ ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN (A) SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

☐ COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOL PCE CONT DWG R-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ±, 3 PLACE DECIMALS ±, ANGLES

MATL

HARD | CASE DEPTH

SURF TREAT

DESIGNED J.E. Ward 6-29-64

DRAFTSMANSHIP

DRAWN Jim Loop 6/29/64

DRAWING CHECK

DIVISION APPROVAL D.D. Boyd 6/30/64

W.J. Stutz 7/1/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY-OCD2

CODE IDENT NO. 03640 | SIZE D | DRAWING NO. 6942037

SCALE 2/1 | WT | SHEET OF 2

Figure 10-72. OCD2 Printed Circuit Board Assembly (6942037) (Sheet 1 of 2)

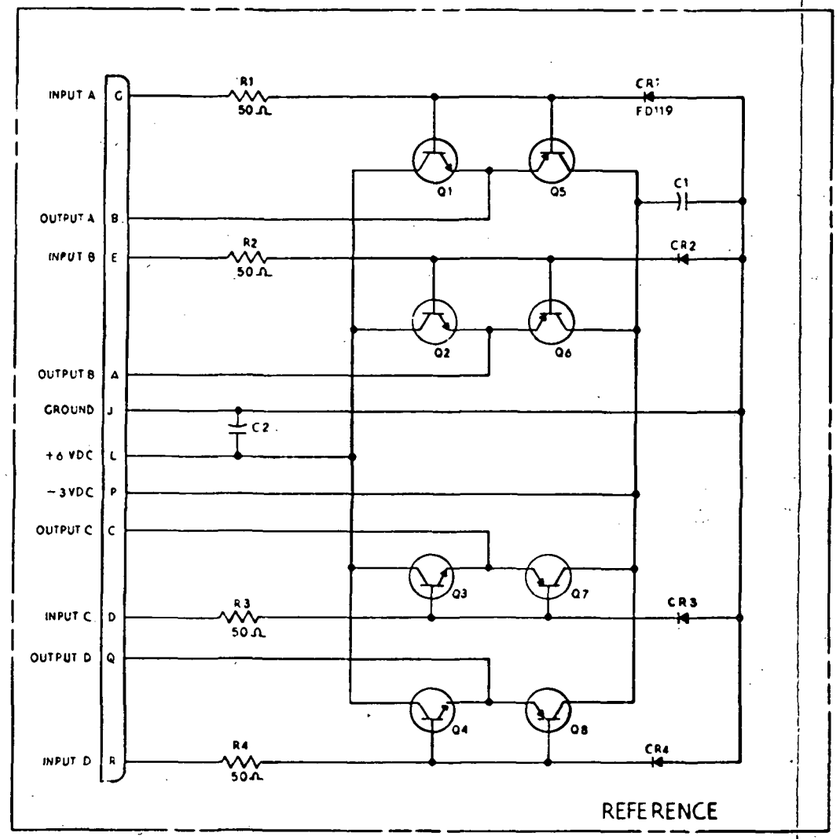
SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR PN

DWG NO. 6942037

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115 FL	RELEASE			



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					

SPEC NUMBER	NOTE	ITEM NO.
APPLICABLE IBM SPEC	APPLIES TO	

☐ ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN ( ). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

☐ COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM: V=VENDOR ITEM S/N, SPEC OR SOURCE CONT DWG M=MFG QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±

MATL

HARD

CASE DEPTH

SURF FINISH

		DATE
DESIGNED		
DESIGN CHECK		
DRAWN	J. J. Brumagin	10/20/64
DRAWING CHECK		
DESIGN APPROVAL	R. Bryant	10/20/64
	W. S. Kuhn	10/26/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: PRINTED CIRCUIT BOARD ASSEMBLY-OCD2

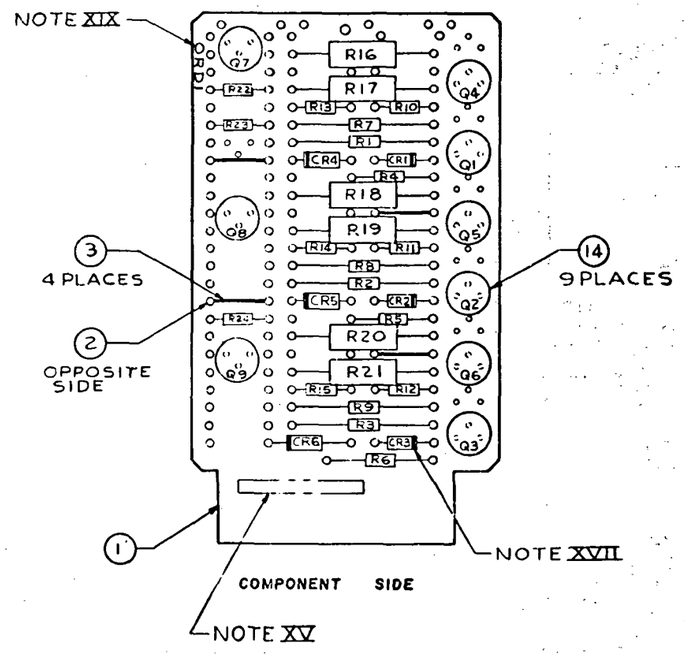
CODE IDENT NO.	SIZE	DRAWING NO.
03640	D	6942037

SCALE | WT | SHEET 2

Figure 10-72. OCD2 Printed Circuit Board Assembly (6942037) (Sheet 2)

6942038

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115 BV	RELEASE	6-6-64		



NOTES

- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6942038 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY
- XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

REF DES	ITEM NO.
Q7-Q9	13
Q4-Q6	12
Q1-Q3	11
CR4-CR6	10
CR1-CR3	9
R22-R24	8
R16-R21	7
R13-R15	6
R4-R12	5
R1-R3	4

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
9		SPACER	491299			88360	14
3		⊤	535441			88360	13
3			369114			88360	12
3		TRANSISTOR	318324			88360	11
3		DIODE (6033887)	IN645 JAN				10
3	V	DIODE	6079734				9
3		⊤ (6076583)	RC07GF241J				8
6		⊤ (6012224)	RC32GF332J				7
3		⊤ (6055224)	RC07GF272J				6
9		⊤ (6078194)	RC07GF161J				5
3		RESISTOR (6078207)	RC07GF242J				4
4 IN.	VR	WIRE INS. #22AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942039				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS. OUTSIDE MIN MAX, INSIDE MIN MAX. ALL DIMENSION AND TOLERANCES APPLY TO FINISHED PART. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS, 3 PLACE DECIMALS, ANGLES. MATL. HARD, SOFT. CASE DEPTH. CONTRACT NO.

DESIGNED — DATE 5-7-64
DESIGN CHECK — 5-25-64
DRAWN V M D — 5-14-64
DRAWING CHECK
DESIGN APPROVAL — 6-4-64

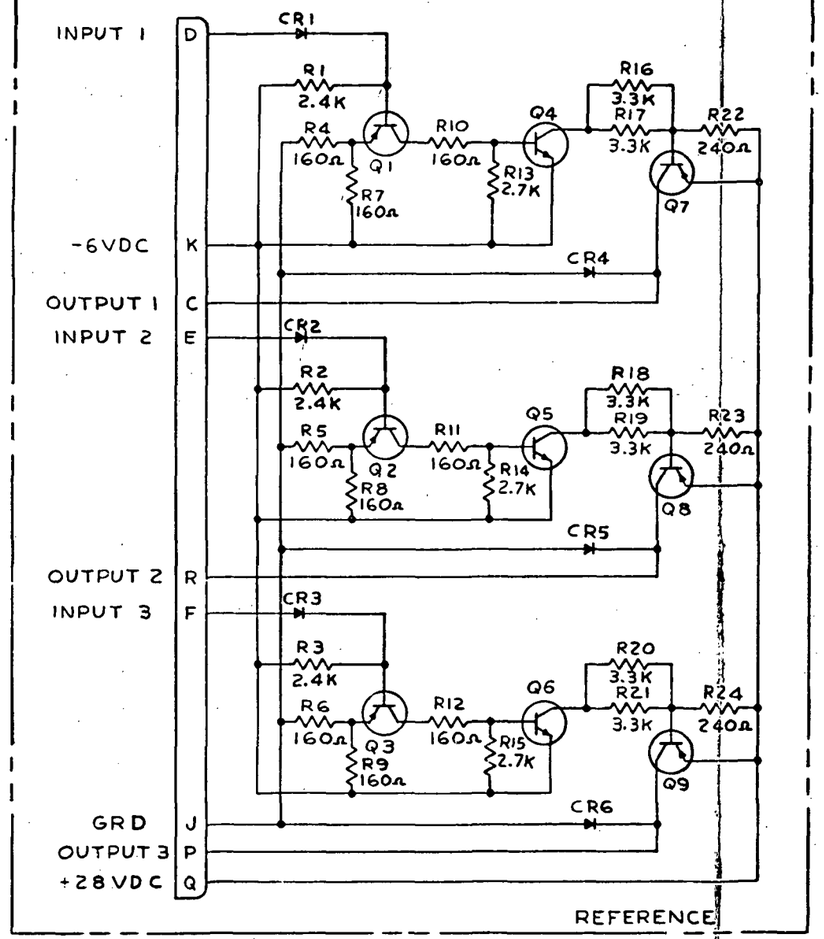
INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT ASSY. ORD1

CODE IDENT NO. 03640 | SIZE D | 6942038

SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-73. ORD1 Printed Circuit Board Assembly (6942038) (Sheet 1 of 2)



SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

DWG. NO. 6942038

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115BV	RELEASE	4-6-67		

LIST OF MATERIAL OR PARTS LIST

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN ( ). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

SPEC NUMBER | NOTE | ITEM NO. | APPLIES TO

APPLICABLE IBM SPEC | CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG R-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± .01 3 PLACE DECIMALS ± .005 ANGLES ±

MATL

HARD | CASE DEPTH

SURF TREAT

DESIGNED	E Hubard	5-15-66
DESIGN CHECK	J.E. Wood	5-22-66
DRAWN	VMD	5-19-66
DRAWING CHECK		
DESIGN APPROVAL	R.F. Jaegle	6/14/66

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: PRINTED CIRCUIT ASSY. ORD1

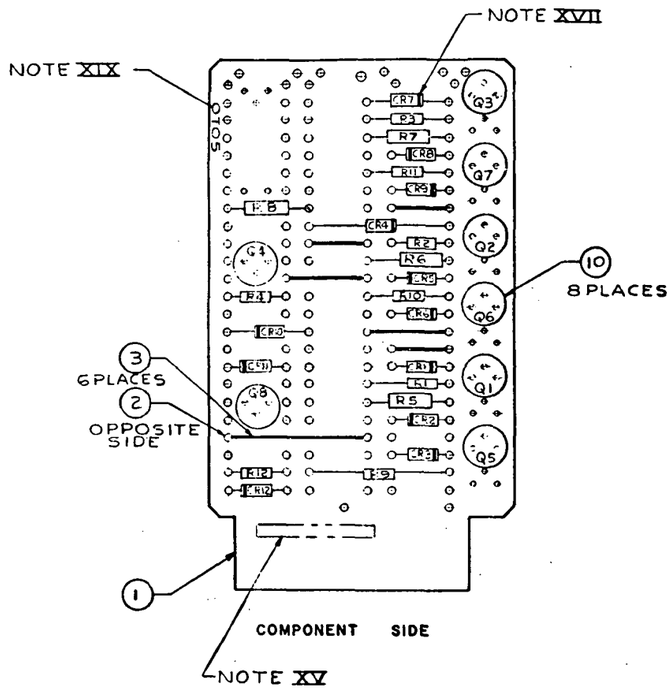
CODE IDENT NO.	SIZE	DRAWING NO.
03640	D	6942038

SCALE NONE WT SHEET 2

Figure 10-73. ORD1 Printed Circuit Board Assembly (6942038) (Sheet 2)

6942040

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115BV	RELEASE	R.[illegible]-67		



Q5-Q8	9
Q1-Q4	8
CR1-CR12	7
R9-R12	6
R5-R8	5
R1-R4	4
REF DES	ITEM NO.

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6942040 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM - SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX APPLY .09 HIGH CHARACTERS APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
8		SPACER	491299			88360	10
4		TRANSISTOR	369114			88360	9
4		TRANSISTOR	318324			88360	8
12	V	DIODE	3079734				7
4		(6020826)	RC07GF103J				6
4		(6011518)	RC20GF121J				5
4		RESISTOR (6078206)	RC07GF222J				4
8 IN.	VR	WIRE INS. #22 AWG. YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942041				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES 2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±1°
MATL
HARD CASE DEPTH
SURFACE

DESIGNED E Hedrick 5-18-64
DESIGN CHECK [illegible] 5-[illegible]-64
DRAWN VMD 5-18-64
DRAWING CHECK
DESIGN APPROVAL [illegible] 6/4/64
[illegible] 6/4/64

CONTRACT NO.

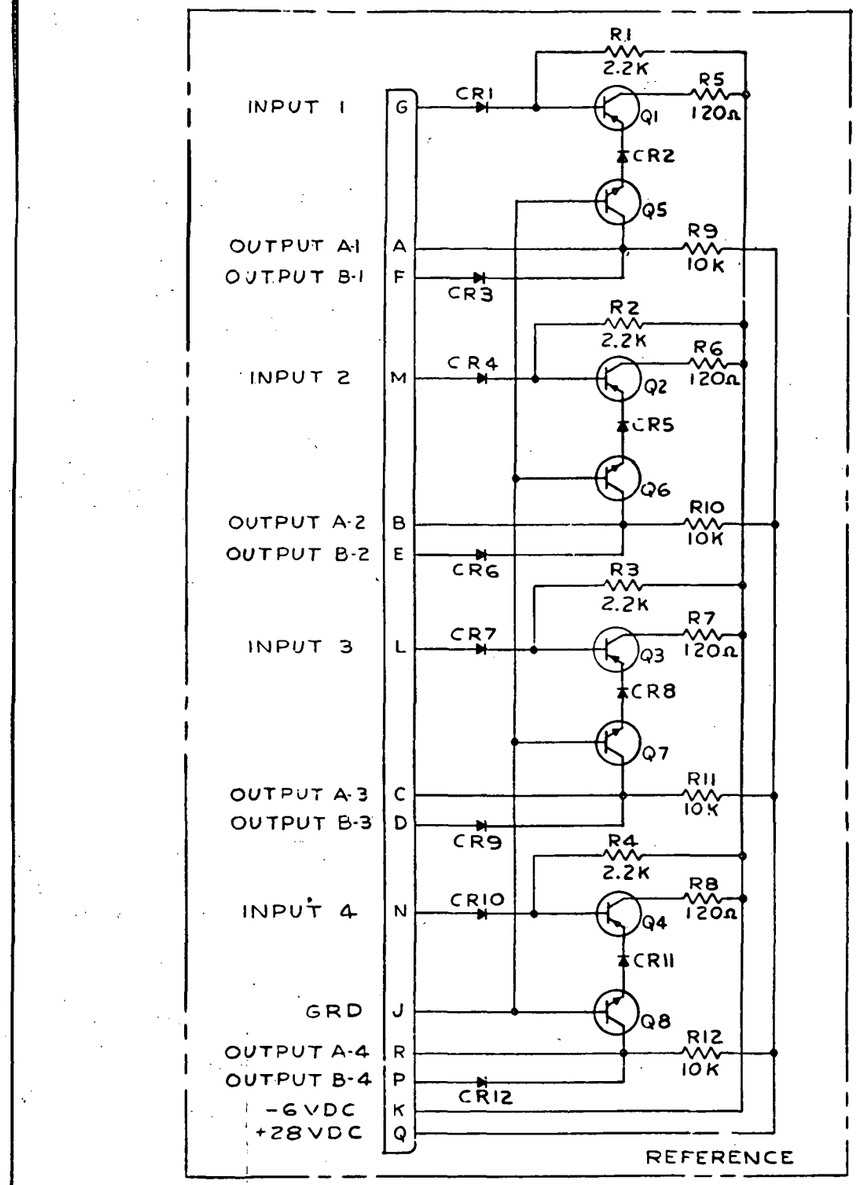
INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE PRINTED CIRCUIT ASSY. OTO5

CODE IDENT NO. 03640 SIZE D 6942040

SCALE 2/1 WT SHEET 1 OF 2

Figure 10-74. OTO5 Printed Circuit Board Assembly (6942040) (Sheet 1 of 2)



SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR PB

DWG NO. 6942040

REVISIONS

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
·	66115DV	RELEASE	6-14-4	·	

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					

SPEC NUMBER | NOTE | ITEM NO. | APPLIES TO | APPLICABLE IBM SPEC

☐ ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN ( ). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

☐ COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

CHECK BLOCK ☒ IF APPLICABLE

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG R-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON: 2 PLACE DECIMALS ± ; 3 PLACE DECIMALS ± ; ANGLES ±

MATL | HARD | CASE DEPTH | SURF TREAT

CONTRACT NO.

DESIGNED E. Hubert 5-18-64
DESIGN CHECK E. Lind 5-25-64
DRAWN VMD 5-18-64
DRAWING CHECK
DESIGN APPROVAL R.J. Siegel 6/4/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE
PRINTED CIRCUIT ASSY
OTO5

CODE IDENT NO.	SIZE	DRAWING NO.
03640	D	6942040

SCALE NONE | WT | SHEET 2

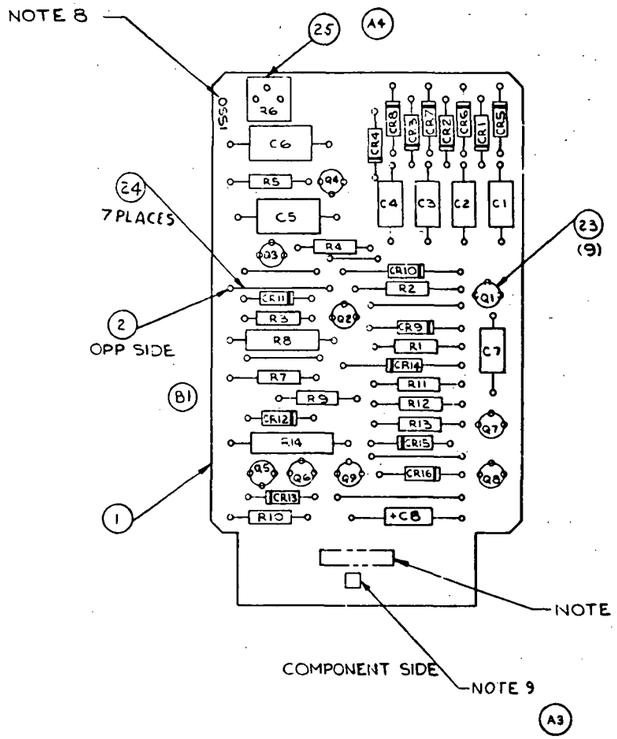
Figure 10-74. OTO5 Printed Circuit Board Assembly (6942040) (Sheet 2)

SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

DWG NO. 6942042 B

SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115FK	RELEASE R	7/2/64		
A	66115KG	(1-4) ADD NOTE 9, CHG P/N OF ITEM 8, ADD ITEM NO 25 R	9264		J.E.WOOD
B	66115 KH	(1) CHG CR9 DES. TO R9 R	9-8-64		F.CONTENTO



R12	13
Q3,6	22
Q1,2,4,5,7-9	21
R14	14
R11 & 13	12
R10	11
R8	10
R7	9
R6	8
R5	7
R4	6
R3	5
R2	4
R1 & R9	3
CR1-CR16	15
C3	20
C7	19
C6	18
C5	17
C1-C4	16
REF DES	ITEM NO.

NOTES

1. MIN ELECTRICAL CLEARANCE TO BE .018
2. COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
3. COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
4. LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
5. MARK 6942042 ASSY TYPE I, CLASS I COLOR BLACK
6. JUMPER AND COMPONENT LEADS BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
7. BLACK BAND DENOTES CATHODE END OF DIODE
8. MARK TYPE III CLASS I COLOR BLACK
9. (A2) MARK LATEST REV LEVEL TYPE I CLASS I COLOR BLACK

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
		LIST OF MATERIAL OR PARTS LIST					
1		SPACER	492199			88360	25
1 FT	VR	WIRE #22 AWG, YEL	6036152				24
9		SPACER	483070			88360	23
2	V	T	6079006				22
7		TRANSISTOR	6079909			88360	21
1	V	T 4.7UF, 20%, 10V	6018707				20
1	V	130PF, 1%, 500V	6026584				19
1	V	1200PF, 10%, 300V	6081194				18
1	V	430PF, 1%, 500V	6081195				17
4	V	CAPACITOR. 120PF, 10%, 500V	6011904				16
16		DIODE (6034674)	1N3064				15
1	V	T 1K, 1/4W 1%	6010100				14
1	V	2.4K, 1/8W. 1%	6020638				13
2	V	360Ω, 1/8W, 1%	6010287				12
1		(6010263)	RN60C9101F				11
1	V	430Ω, 1/4W, 1%	6017325				10
1		(6020820)	RN60C8001F				9
1	V	VARIABLE 500Ω 5%	6081355				8
1		(6020653)	RN60C1501F				7
1		(6020647)	RN60C499CF				6
1		(6020655)	RN60C5111F				5
1		RES. (6036186)	RN60C2742F				4
2	V	RESISTOR. 1.2K, 1/8W, 1%	6014115				3
AR		SOLDER (6032357)	SN60AR	QQ-S-571			2
1		SMS CARD	6942043				1

(A1)

6009974	E3,9	
6000903		
SPEC NUMBER	NOTE	ITEM NO. APPLIES TO
APPLICABLE IBM SPEC		

☐ ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S), HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN (1). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

☐ COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

CHECK BLOCK ☑ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM. V: VENDOR ITEM SEE SPEC OR SOURCE CONT DWG R: REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE STATED DIMENSIONS ARE IN INCHES. TOLERANCE ON X PLACE DECIMALS ± .XX PLACE DECIMALS ± ANGLES

MATL

HARD

SURF TREAT

CASE HARDEN

		DATE
DESIGNED	C.K. Rinkard	7/1/64
DESIGN CHECK	R.E. Ward	7/2/64
DRAWN	[illegible]	7/2/64
DRAWING CHECK		
DESIGN APPROVAL	R.J. Fogel	7/6/64
	[illegible]	7/8/64

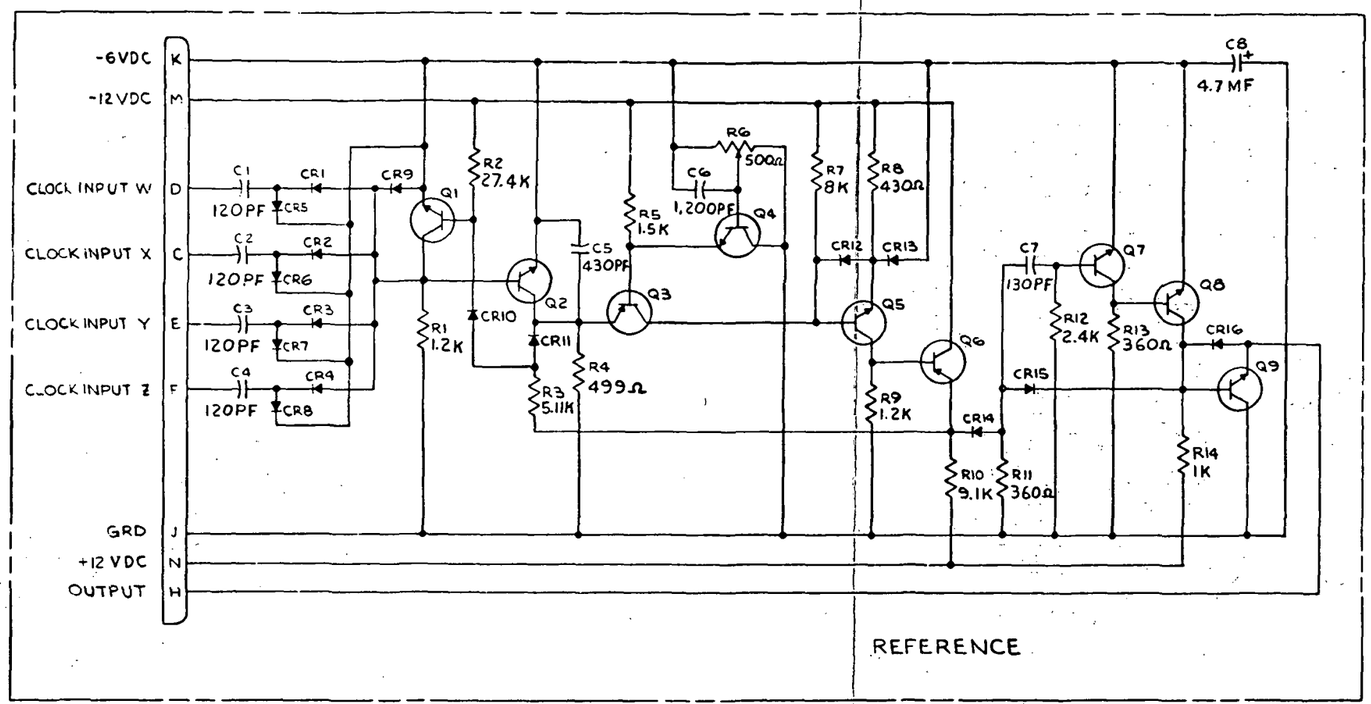
INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: PRINTED CIRCUIT ASSEMBLY-OSS1

CODE IDENT NO.	SIZE	DRAWING NO.
03640	D	6942042

SCALE 2/1 WT SHEET 1 OF 2

Figure 10-75. OSS1 Printed Circuit Board Assembly (6942042) (Sheet 1 of 2)



SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P/N

DWG NO. 6942042 B

SYM	ENGRG NOTICE	DESCRIPTION		DATE	CHK	APPROVAL
	66115-K	RELEASE	R	7/14/64		
A	66115KG	(1-4) ADD NOTE 9, CHG P/N OF ITEM 8, ADD ITEM NO 25	R	9-2-64		J.E. WOOD
B	66115KH	(1) CHG CR9 DES. TO R9	R	9-8-64		F. CONTENTO

REVISIONS

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S), HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN:
1. A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO A-D COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

SPEC NUMBER | NOTE | ITEM NO. APPLIES TO

APPLICABLE IBM SPEC

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM. V-VENDOR ITEM S-SPEC OR SOURCE CONT DWG A-ANY QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON: 2 PLACE DECIMALS ± | 3 PLACE DECIMALS ± | ANGLES ±

MATL | HARD | CASE DEPTH | SURF FINISH

		DATE
DESIGNED	E A Hedrick	7-1-64
DESIGN CHECK	L S Wood	7-1-64
DRAWN	W. Perrella	7/1/64
DRAWING CHECK		
DESIGN APPROVAL	R F Yeager	7/1/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: PRINTED CIRCUIT ASSEMBLY-OSS1

CODE IDENT NO.	SIZE	DRAWING NO.
03640	D	6942042

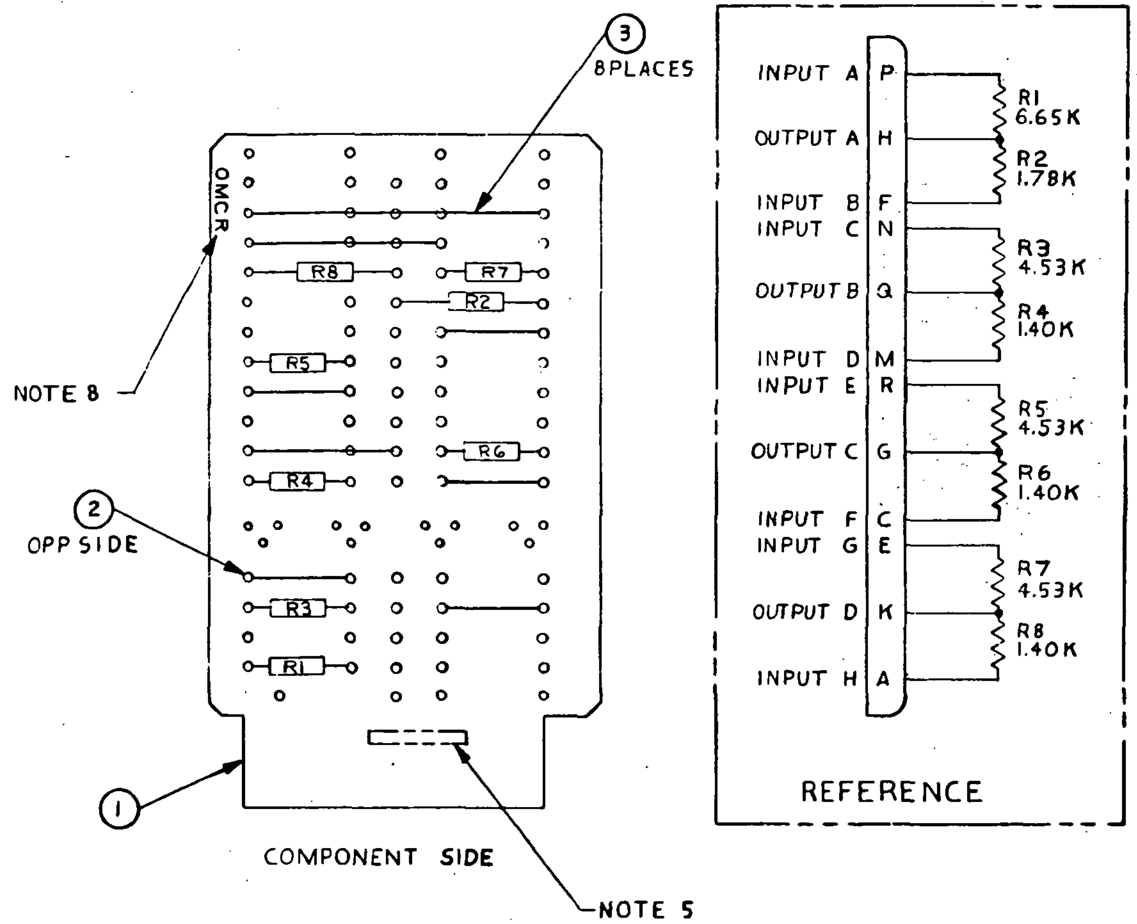
SCALE NONE | WT | SHEET 2

Figure 10-75. OSS1 Printed Circuit Board Assembly (6942042) (Sheet 2)

SOURCE OF SUPPLY			
VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P/N

DWG NO. 6942044

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115FL	RELEASE			



NOTES.

1. MIN ELECTRICAL CLEARANCE TO BE .018
2. COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
3. COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
4. LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
5. MARK 6942044 ASSY TYPE I CLASS I COLOR BLACK
6. JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
7. BLACK BAND DENOTES CATHODE END OF DIODE
8. MARK TYPE III CLASS I COLOR BLACK

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
3		4.53K±1%,1/8W	6079981				7
1		1.78K±1%,1/8W	6079980				6
1		6.65K±1%,1/8W	6079979				5
3	V	RES. 1.4K ±1%,1/8W	6079011				4
12 IN.	V.R	WIRE NO.22 AWG YEL	6036152				3
AR		SOLDER (6032357)	SN 60 AR	QQ-S-571			2
1		SMS CARD	492345			88360	1

LIST OF MATERIAL OR PARTS LIST

REF DES	ITEM NO.
R3,R5,R7	7
R2	6
R1	5
R4,R6,R8	4

SPEC NUMBER	NOTE	ITEM NO. APPLIES TO
6005974	5,8	
6000003		

APPLICABLE IBM SPEC

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN ( ). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

IDENT. OF SYM: V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG R-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES

MATL

HARD | CASE DEPTH

SURF TREAT

DESIGNED | DATE 6/30/64
DESIGN CHECK | 6-30-64
DRAWN | 6/30/64
DRAWING CHECK
DESIGN APPROVAL | 6/30/64
| 7/1/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE PRINTED CIRCUIT BOARD ASSY-OMCR

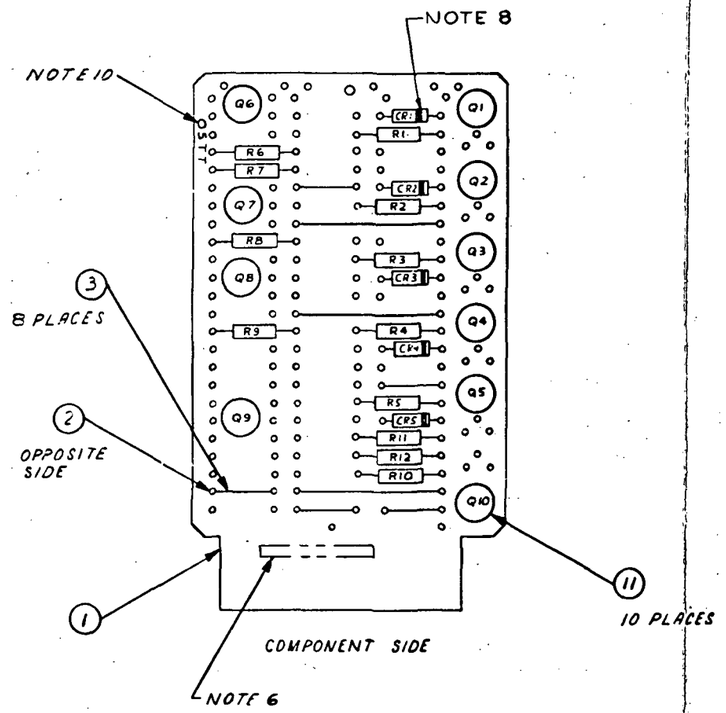
CODE IDENT NO. 03640 | SIZE D | DRAWING NO. 6942044

SCALE 2/1 | WT | SHEET

Figure 10-76. OMCR Printed Circuit Board Assembly (6942044)

6942045 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	36115FK	RELEASE	7/14/64		
A	36115-6	(1-2) CHG RESISTOR ITEM 4	[illegible]		[illegible]



Q6 - Q10	10
Q1 - Q5	9
CR1 - CR5	8
R12	7
R11	6
R6 - R10	5
R1 - R5	4
REF DES	ITEM NO.

NOTES:

1. IBM GEN ASSY SPEC 6000003 APPLIES
2. MIN ELECTRICAL CLEARANCE TO PE .018
3. COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND / OR OTHER COMPONENTS
4. COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
5. LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
6. MARK 6942045 TYPE I, CLASS 1, PER IBM SPEC 6009974, COLOR BLACK
7. JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
8. BLACK BAND DENOTES CATHODE END OF DIODE
9. IDENTIFICATION OF SYMBOLS:
   V - VENDOR ITEM - SEE SPEC OR SOURCE CONTROL DWG.
   R - REFERENCE QUANTITY
10. MARK TYPE III, CLASS I, APPROX AS SHOWN PER IBM SPEC 6009974, COLOR BLACK

(A1)

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.
10		SPACER	491299				11
5		TRANSISTOR	318324				10
5		TRANSISTOR	318325			88360	9
5	V	DIODE	6079734				8
1	V	RESISTOR 47Ω, ⅛W, 1%	6010657				7
1		RESISTOR (6023674)	RN60B1210F				6
5		RESISTOR (6020183)	RC07GF271J				5
5	V	RESISTOR (6081660)	RN60C2491F				4
8 IN.	V,R	WIRE #22 AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942046				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS: OUTSIDE MIN MAX, INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE STIPULATED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± .1 PLACE DECIMALS ± ANGLES ±
MATL
HARD
CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED S A [illegible] DATE 7-1-64
DESIGN CHECK [illegible] 7-1-64
DRAWN J. K. Bidwell 7-2-64
DRAWING CHECK
DESIGN APPROVAL [illegible] 7/4/64

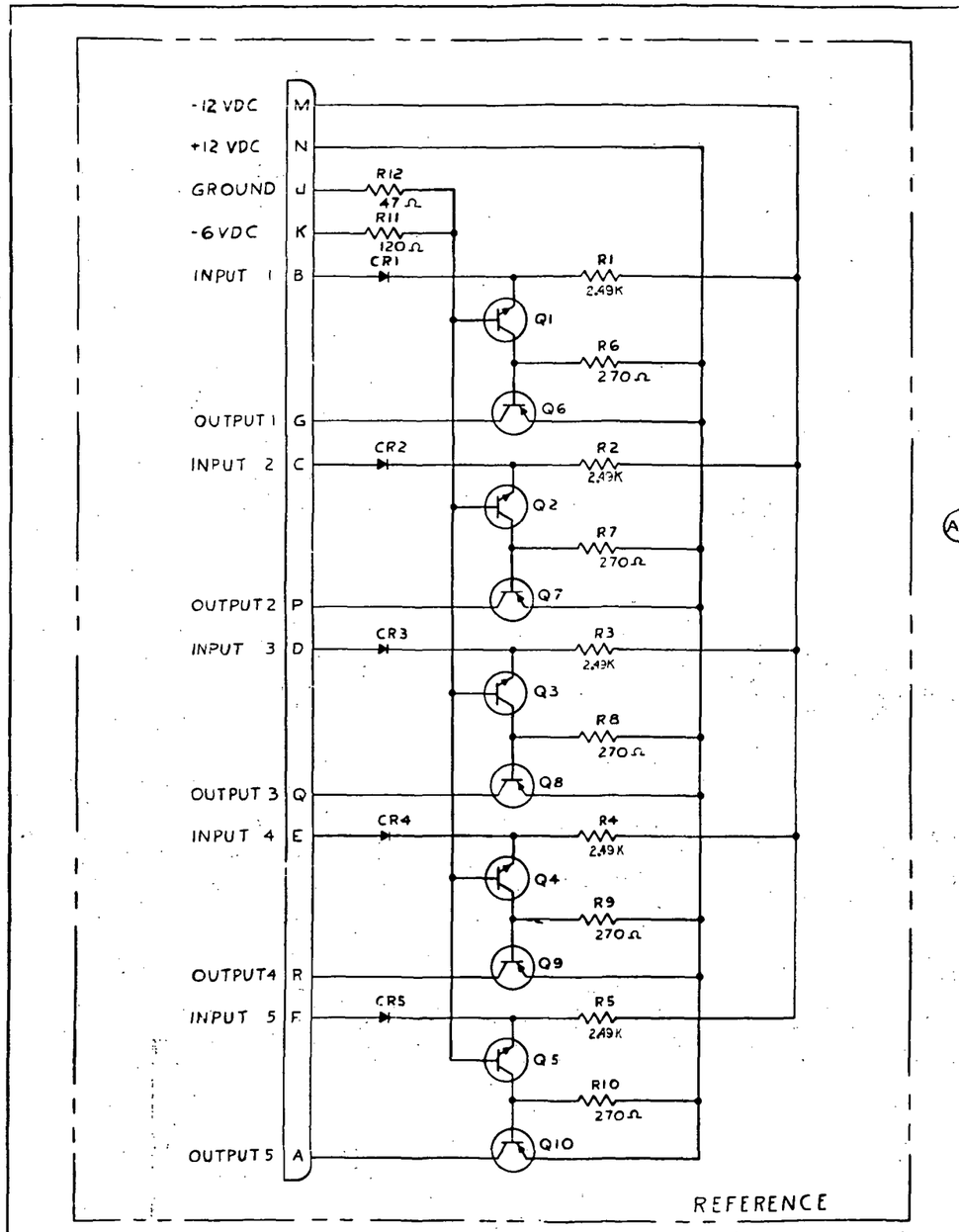
INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT ASSY OSTT

CODE IDENT NO. 03640 | SIZE D | 6942045

SCALE 2:1 | WT | SHEET 1 OF 2

Figure 10-77. OSTT Printed Circuit Board Assembly (6942045) (Sheet 1 of 2)



6942045 A

A2

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115FK	RELEASE	7-4-64		
A	66115LS	(1-2) CHG RESISTOR ITEM 4 R	8-28-64	CE. WOOD	

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD SURF TREAT CASE DEPTH
CONTRACT NO.

DESIGNED E M Hedrick 7-7-64
DESIGN CHECK E. Wood 7-8-64
DRAWN L. R. Bidwell 7/8/64
DRAWING CHECK
DESIGN APPROVAL R. D. Jegel 7/8/64
7/8/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE PRINTED CIRCUIT ASSY-OSTT

CODE IDENT NO. 03640 | SIZE D | 6942045

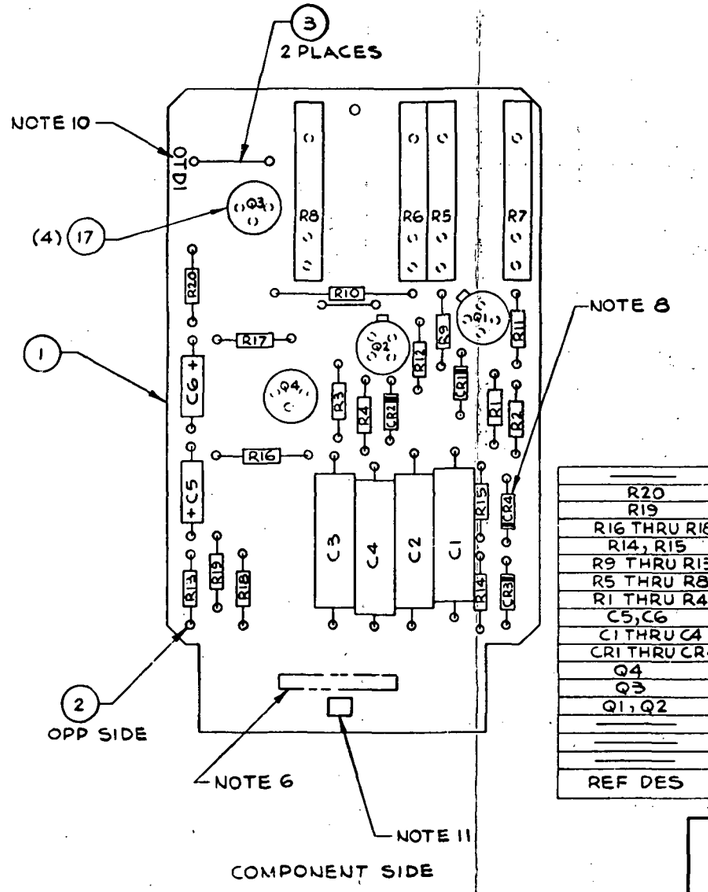
SCALE NONE WT SHEET 2

Figure 10-77. OSTT Printed Circuit Board Assembly (6942045) (Sheet 2)

6942047

REVISIONS					
SYM	EKGRG NOTICE	DESCRIPTION R	DATE	CHK	APPROVAL
A	66115LG	REVISED AND REDRAWN	10234		

NOTES:
1 IBM GEN ASSY SPEC 6000003 APPLIES
2 MIN ELECTRICAL CLEARANCE TO BE .018
3 COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
4 COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCH
5 LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
6 MARK 6942047 ASSY TYPE 1, CLASS 1 COLOR BLACK PER IBM SPEC 6009974
7 JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
8 BLACK BAND DENOTES CATHODE END OF DIODE
9 IDENTIFICATION OF SYMBOLS:
V-VENDOR ITEM-SEE SOURCE OR SPEC CONTROL DRAWING
R-REFERENCE QUANTITY
10 MARK TYPE III CLASS 1 COLOR BLACK PER IBM SPEC 6009974
11 MARK REV LEVEL TYPE III CLASS 1 COLOR BLACK PER SPEC 6009974



REF DES	QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
	4		SPACER	491299			88360	17
R20	1		(6078201)	RC07GF821J				16
R19	1		(6078199)	RC07GF561J				15
R16 THRU R18	3		(6078207)	RC07GF242J				14
R14, R15	2		(6033888)	RC07GF113J				13
R9 THRU R13	5		(6020826)	RC07GF103J				12
R5 THRU R8	4	V	1K, 1W, ±5%	6020262				11
R1 THRU R4	4		RESISTOR (6020890)	RC07GF102J				10
C5, C6	2		4.7MF, ±20%, 10V	6018707				9
C1 THRU C4	4		CAPACITOR, 2.5MF, ±10%, 60V	6072344				8
CR1 THRU CR4	4	V	DIODE	6079734				7
Q4	1			318324			88360	6
Q3	1			318325			88360	5
Q1, Q2	2	V	TRANSISTOR	6080110				4
	3IN	V,R	WIRE, 22 AWG, YELLOW	6036152				3
	AR		SOLDER (6032357)	SN60AR	QQ-S-571			2
	1		PC BOARD	6942048				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Wood 9-2-64
DESIGN CHECK 9/60
DRAWN R. Bohanesky 10/19/64
DRAWING CHECK
DESIGN APPROVAL 10/4/64
10/5/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

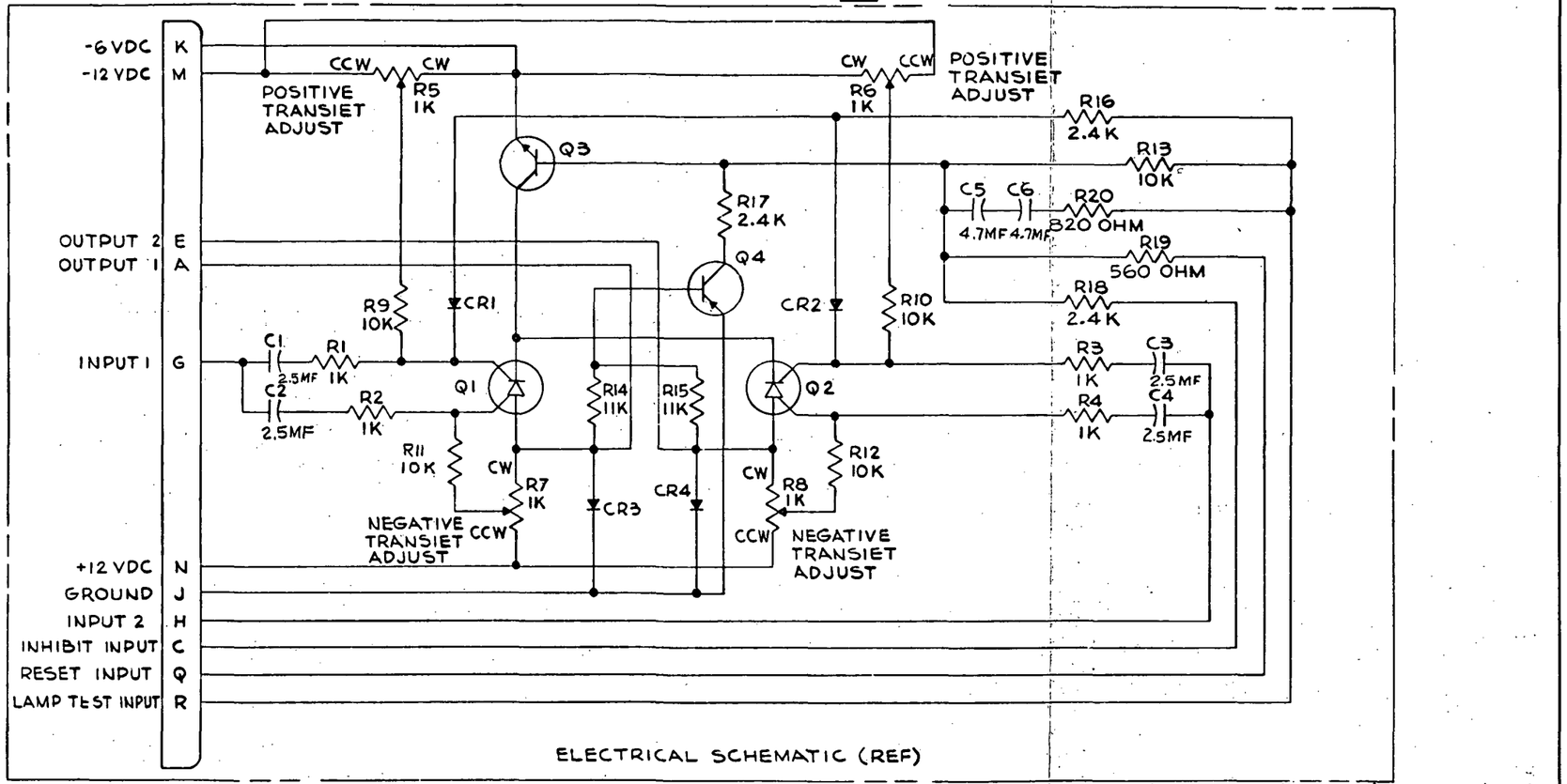
TITLE PRINTED CIRCUIT ASSY OTD1

CODE IDENT NO. 03640 SIZE C 6942047
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-78. OTD1 Printed Circuit Board Assembly (6942047) (Sheet 1 of 2)

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
A	66115LG	REVISED AND REDRAWN R	10-64		

6942047



ELECTRICAL SCHEMATIC (REF)

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

		DATE
DESIGNED	J.E. Wood	10-20-64
DESIGN CHECK	A.H. Evans	11/24/64
DRAWN	R. Bobransky	10/20/64
DRAWING CHECK		
DESIGN APPROVAL		12/1/64
		12/1/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

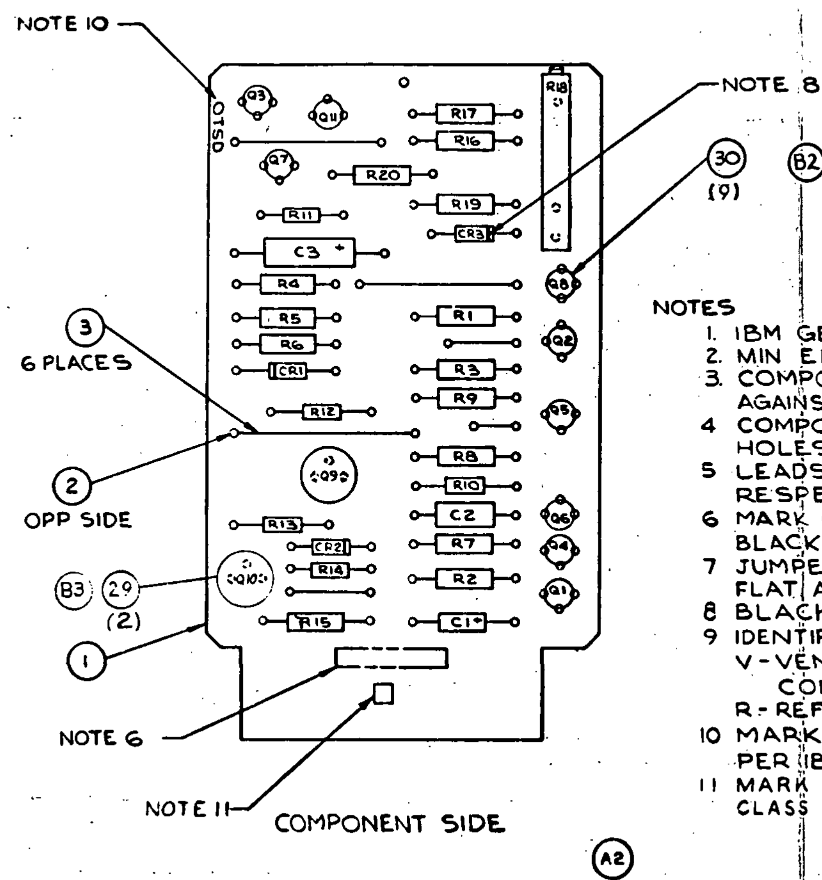
TITLE
PRINTED CIRCUIT ASSY

CODE IDENT NO. 03640 | SIZE C | 6942047
SCALE NONE | WT | SHEET 2

Figure 10-78. OTD1 Printed Circuit Board Assembly (6942047) (Sheet 2)

6942049 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115FZ	RELEASE R	7-1-64		
A	66115JN	(1-2) ADDED TEST POINT, MARK REV LEVEL CHGD ITEMS 27, 30 DELETED ITEM 29 R	8-18-64		E. WOOD
B	66115MC	(1-3) SEE ENGRG NOTICE R	9/27	HC	EVANS



REF DES	ITEM NO.
Q9, Q10	28
Q6, Q7	27
Q4, Q5, Q8, Q11	26
Q1 - Q3	25
C3	24
C2	23
C1	22
CR1, 2, 3	21
R20	20
R19	19
R18	18
R17	17
R16	16
R15	15
R13	14
R12	13
R11, R14	12
R10	11
R9	10
R7, R8	9
R6	8
R5	7
R4	6
R2, R3	5
R1	4

NOTES

1. IBM GEN. ASSY SPEC 6000003 APPLIES
2. MIN ELECTRICAL CLEARANCE TO BE .018
3. COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
4. COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCH
5. LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
6. MARK 6942049 ASSY TYPE I CLASS 1 COLOR BLACK PER IBM SPEC 6009974
7. JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
8. BLACK BAND DENOTES CATHODE END OF DIODE
9. IDENTIFICATION OF SYMBOLS
   V - VENDOR ITEM - SEE SOURCE OR SPEC CONTROL DRAWING
   R - REF QTY
10. MARK TYPE III, CLASS 1 COLOR BLACK PER IBM SPEC 6009974
11. MARK REV LEVEL .12 HIGH CHARACTERS TYPE I CLASS I COLOR BLACK PER IBM SPEC 6009974

B1

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
9		SPACER	483070				30
2		SPACER	491299				29
2			318324			98360	28
2	V		6081468				27
4	V		6081429				26
3	V	TRANSISTOR	6081430				25
1	V	4.7MF, ±20%, 35V	6018793				24
1		.01MF, ±10%, 100V	491228			98360	23
1	V	CAPACITOR 4.7MF, ±20%, 10V	6018707				22
3	V	DIODE	6079734				21
1		(6081434)	RN60C4752F				20
1		(6081431)	RN60C1101F				19
1	V	500Ω, 1W, 5%	6020346				18
1		(6034586)	RN60C9090F				17
1		(6081391)	RN60C2152F				16
1		(6078199)	RC07GF561J				15
1		(6033983)	RC07GF562J				14
1		(6020184)	RC07GF513J				13
2		(6078208)	RC07GF822J				12
1		(6033125)	RC07GF274J				11
1		(6081433)	RN60C4022F				10
2		(6076587)	RN60C4221F				9
1		(6081435)	RN60C5491F				8
1		(6034587)	RN60C3831F				7
1		(6081437)	RN60C9761F				6
2		(6081436)	RN60C9531F				5
1		RESISTOR (6081432)	RN60C3011F				4
8 IN.	V, R	WIRE NO. 22 AWG - YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6942023				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON .2 PLACE DECIMALS .3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED E. A. Hudock DATE 7-1-64
DESIGN CHECK
DRAWN 7/1/64
DRAWING CHECK
DESIGN APPROVAL 7/10/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

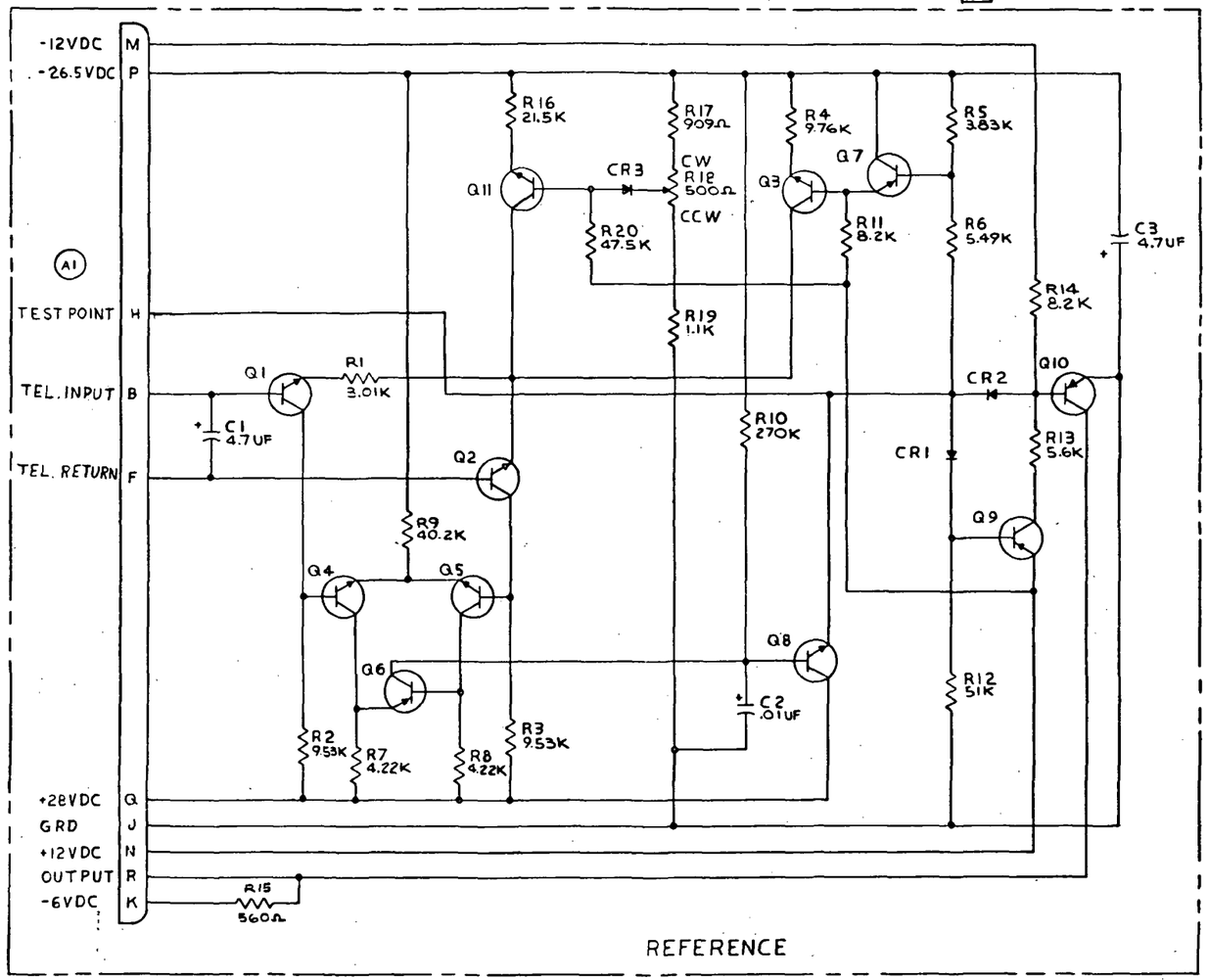
TITLE PRINTED CIRCUIT ASSEMBLY-OTSD

CODE IDENT NO. 03640 SIZE D 6942049
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-79. OTSD Printed Circuit Board Assembly (6942049) (Sheet 1 of 2)

6942049 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66115FZ	RELEASE R	7-1-64		
A	66115JN	(1-2) ADDED TEST POINT MARK REV LEVEL CHG ITEMS 27, 30 DELETED ITEM 29 R	9-8-64		J.E.WOOD
B	66115VC	(1-3) SEE ENGRG NOTICE R	12-4-64	HL	EVANS



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS ± 0 PLACE DECIMALS ± ANGLES ±
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED E A Hulsh 7-1-64
DESIGN CHECK J.E. Wood 7-7-64
DRAWN Jim Loop 7/8/64
DRAWING CHECK
DESIGN APPROVAL R.D. Joyce 7/10/64
W.E. Kuntz 7/13/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT ASSY-OTSD

CODE IDENT NO. 03640 SIZE D 6942049
SCALE NONE WT SHEET 2

Figure 10-79. OTSD Printed Circuit Board Assembly (6942049) (Sheet 2)

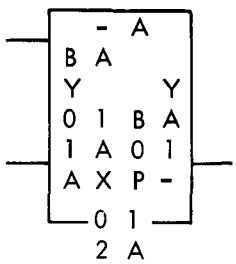
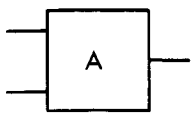
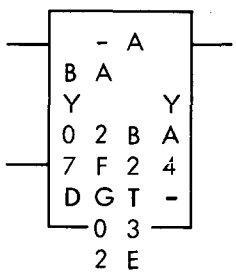
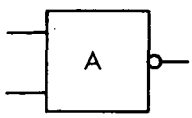
LOGIC SYMBOLS

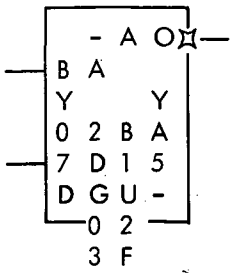
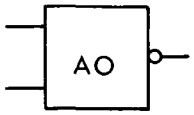
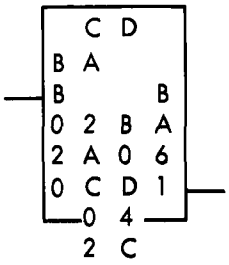
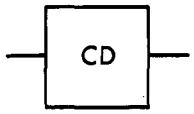
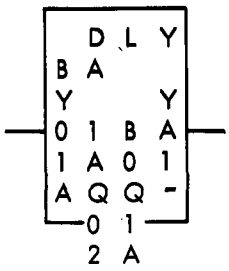
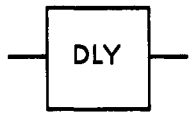
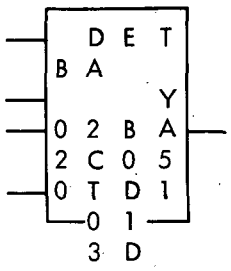
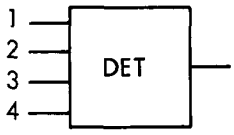
In the list that follows, each type of logic symbol on the LVDAME ALD's is described. Each typical ALD symbol is shown with the corresponding symbol (if any) used in the Second Level Logic diagrams on figure 10-50; some of the circuits indicated on the ALD's (such as resistive loads and diodes) were not indicated on figure 10-50 because they performed no logic function.

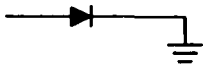
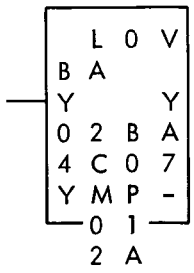
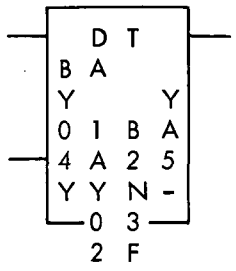
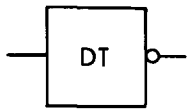
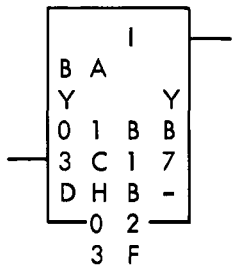
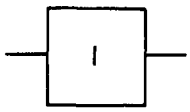
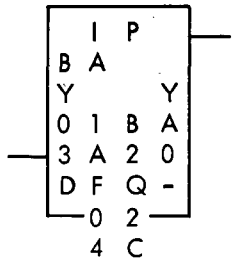
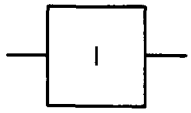
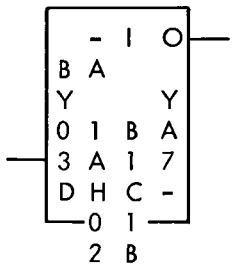
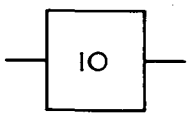
The two letters on the third line of each ALD symbol indicate the nominal levels of input and output voltage for that circuit. The levels respresented by these letters are shown in the following table.

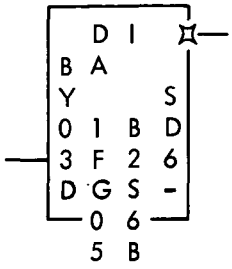
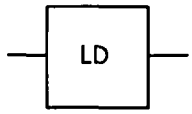
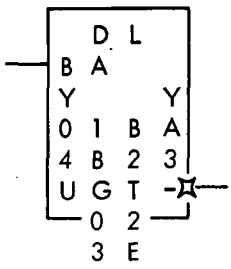
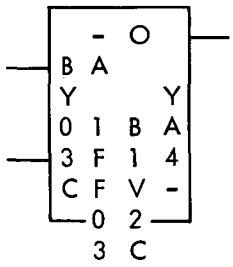
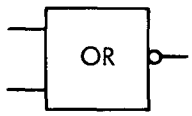
Symbol	Voltage Levels (Nominal)	
	"0" Level	"1" Level
Y	0 VDC	-6 VDC
S	0 VDC	-12 VDC
V	Special	Special
B	Special	Special

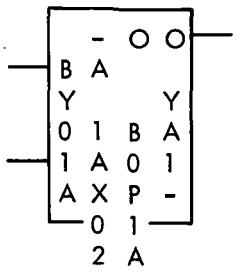
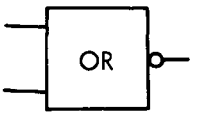
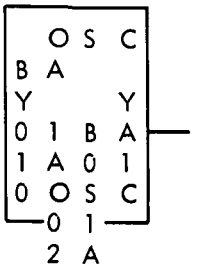
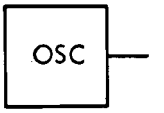
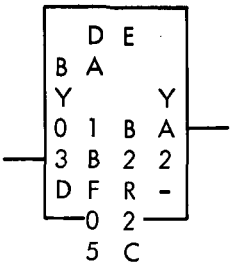
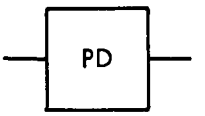
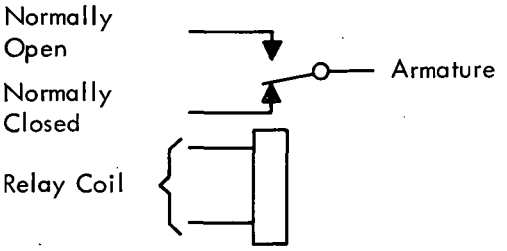
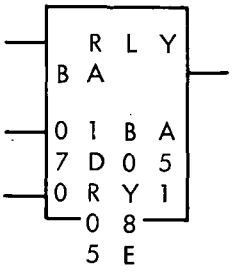
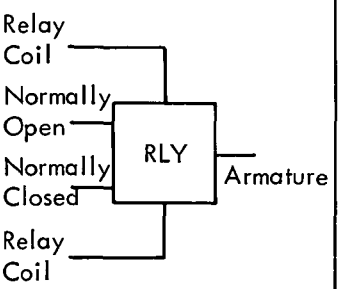
The "Special" levels indicated by B and V are explained in the description of the logic circuits to which they apply; the B notation usually indicates positive logic levels.

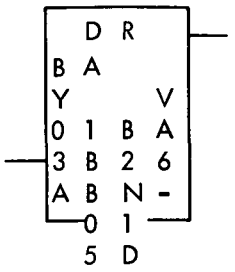
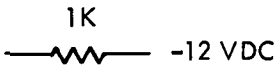
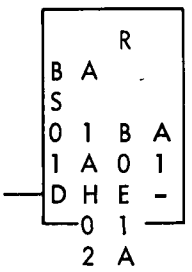
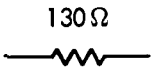
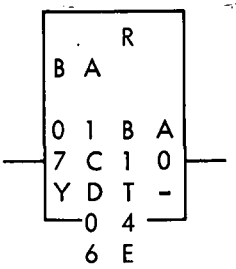
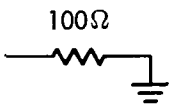
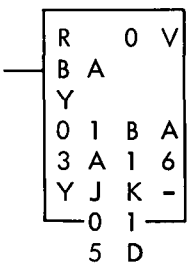
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
1. AND. The output of an AND circuit is the logical AND of its inputs. When all inputs are "1's", the output is a "1"; if any input is a "0", the output is a "0". The AND circuit may have two or more inputs.		
2. AND-INVERTER. This circuit performs the logical AND and INVERT functions. When all inputs are "1's", the output is a "0"; if any input is a "0", the output is a "1". The AND-INVERTER circuit may have two or more inputs.		
	Note: The functional symbol "+O" may be substituted for "-A".	

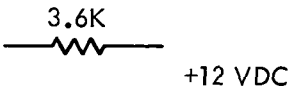
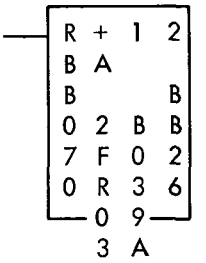
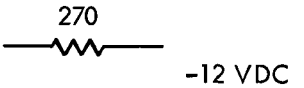
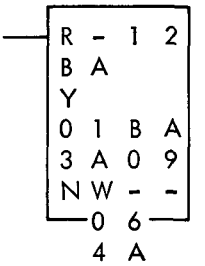
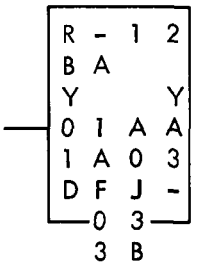
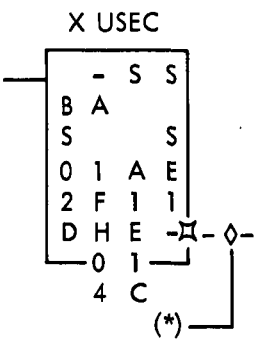
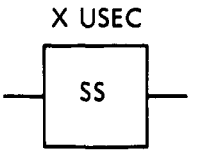
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
3. AND-OR-INVERTER. This circuit performs the logical AND, OR, and INVERT functions. The relation between the inputs and outputs is the same as the AND-INVERTER circuit. However the output transistor of this circuit allows the outputs of several AND-OR-INVERTER circuits to be connected (OR'd) together. A "0" output from any AND-OR-INVERTER circuit of an "ORed" group of circuits will force a "0" output from the group. The AND-OR-INVERTER circuit may have two or more inputs.	 Note The functional symbol "O O" may be substituted for "-AO".	
4. CLOCK DRIVER. This circuit is used as a level shifter to drive a TRANSLATOR-INVERTER circuit. A low positive voltage input produces a "1" output (+6 VDC); a low negative voltage input produces a "0" output (0 VDC).		
5. DELAY. This circuit delays only the positive transition of its input; a delay occurs only when the input changes from a "1" (-6 VDC) to a "0" (0 VDC). The nominal delay duration is indicated above the symbol. A "1" input causes a "1" output.	X USEC 	X USEC 
6. TRANSIENT DETECTOR. This circuit produces "1" when a transient is detected at either input 1 or input 4 while a "0" is at input 2. A "0" at input 3 forces a 0 output.		

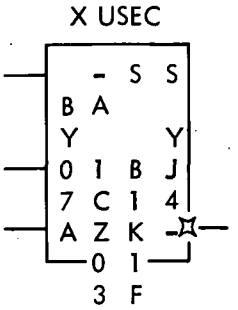
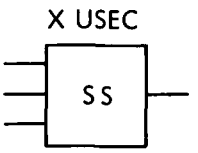
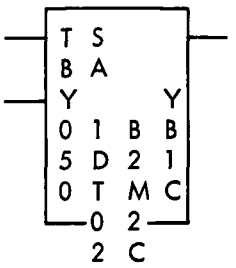
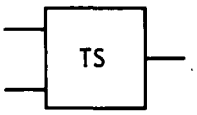
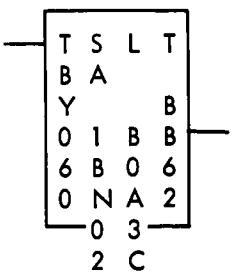
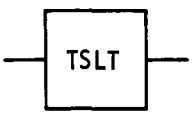
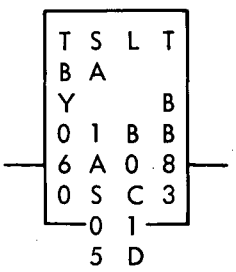
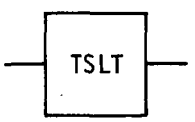
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure (10-50)
7. DIODE. This circuit is a diode connected to ground 		None
8. DRIVER TERMINATOR. This circuit is a signal shaper, inverter, and low impedance matching device.		
9. INVERTER. The output of this circuit is the inverse of its input; a "1" input results in a "0" output and vice versa.		
10. INVERTER (POWER). This circuit performs signal inversion and amplification; a "1" input results in a "0" output and vice versa.		
11. INVERTER-OR. This circuit performs signal inversion; a "1" input results in a "0" output and vice versa. The output transistor of this circuit allows several INVERTER-OR circuits to be connected ("ORed") together. A "0" output from any INVERTER-OR circuit of an "ORed" group of circuits will force a "0" output from the group.		

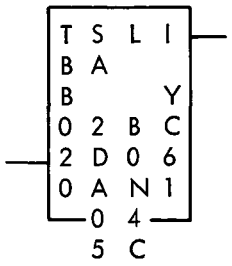
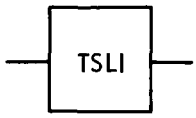
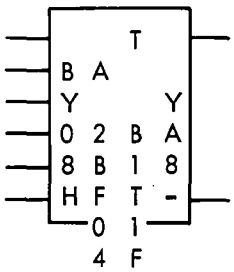
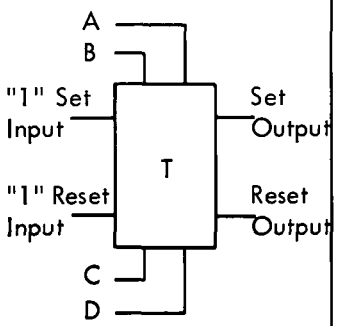
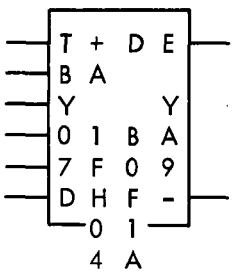
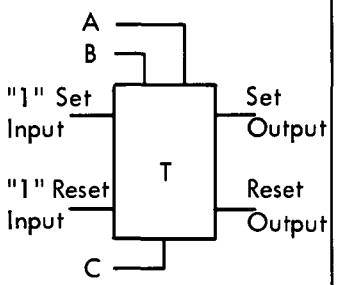
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
12. LAMP DRIVER. A "1" input causes the LAMP DRIVER to turn on its associated indicator lamp; a "0" input causes the LAMP DRIVER to turn off its associated indicator lamp. The input-output levels are as follows: Input — Output "1" (-6 VDC) — 0 VDC "0" (0 VDC) — -12 VDC Note One side of the indicator lamp is connected to -12 VDC; the other side is connected to the output of the LAMP DRIVER. When the output of the LAMP DRIVER is 0 VDC, the potential difference of 12 volts across the lamp lights the lamp.	 Note The "DI" functional symbol represents "Driver, Indicator".	
13. LINE DRIVER. This circuit functions as a signal driver and low impedance matching device.	 Note The "DL" functional symbol represents "Driver, Line".	
14. OR-INVERTER. This circuit performs the logical OR and INVERT functions. When all inputs are "0's", the output is a "1"; if any input is a "1", the output is a "0". This circuit may have two or more inputs.	 Note: The functional symbol "+A" may be substituted for "-O".	

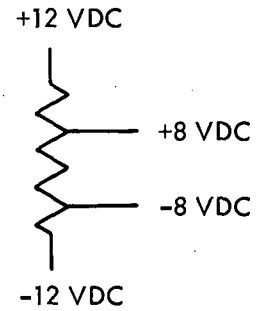
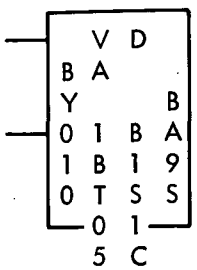
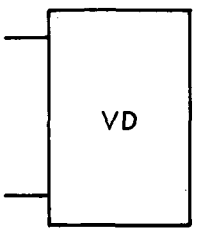
Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
15. OR-INVERTER-OR. This circuit functions in the same manner as the OR-INVERTER. The outputs of many OR-INVERTER-OR's may be connected (OR'd) together. A "0" output from any OR-INVERTER-OR circuit of an "ORed" group of circuits will force a "0" output from the group. This circuit may have two or more inputs.		
16. OSCILLATOR. This circuit generates a square wave signal (0 VDC to -6 VDC) at a 2.048 MC frequency.	2.048MC 	2.048MC 
17. POWER DRIVER. This circuit provides circuit matching and power amplification. A "1" input causes a "1" output; a "0" input causes a "0" output.	 Note The "DE" functional symbol represents "Driver, Emitter". The output portion of this circuit is an emitter follower.	
18. RELAY. 		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
19. RELAY DRIVER. This circuit functions as a level shifter to enable a "1" to energize a relay coil. The input-output relationship is as follows: Input — Output "1" (-6 VDC) — 0 VDC "0" (0 VDC) — -26.5 VDC Note One side of the relay coil is connected to -26.5 VDC; the other side is connected to the output of the RELAY DRIVER. When the output of the RELAY DRIVER is 0 VDC, the potential difference of 26.5 volts across the relay coil energizes the relay coil.	 Note The "DR" functional symbol represents "Driver, Relay".	
20. RESISTOR. This circuit is a 1K resistor connected to -12 VDC. 		None
21. RESISTOR. This circuit is a 130 ohm resistor. 		None
22. RESISTOR. This circuit is a 100 ohm resistor connected to ground. 		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
23. RESISTOR. This circuit is a 3.6K resistor connected to +12 VDC. 		None
24. RESISTOR. This circuit is a 270 ohm resistor connected to -12 VDC. 		None
25. RESISTOR. This circuit is a 1.6K resistor connected to -12 VDC. 		None
26. SINGLE SHOT. A negative going transition at the input causes the SINGLE SHOT to produce a negative output whose negative transition is coincident with the negative transition at the input. The nominal duration of the negative output is shown above the symbol. Note The output (*) may be connected to a RESISTOR (item 25) or it may be fed back to the SINGLE SHOT to hold the SINGLE SHOT' on for the duration of the pulse.		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
27. SINGLE SHOT (Tri-Input). Any or all three inputs may be connected; an unconnected input (indicated by the absence of that input) is effectively a "1" input. All inputs must be "1's" to trigger the SINGLE SHOT. The negative-going transition of the last input to become a "1" triggers the single shot, forcing it to produce a negative output pulse whose negative transition is coincident with the triggering transition of its input. The nominal duration of the pulse is shown above the symbol.		
28. TEMPERATURE SENSOR. This resistor circuit is used to simulate a data adapter thermistor during self-check.		
29. TRANSLATOR. This circuit is a level shifter that converts the negative logic levels used in the LVDAME logic to the positive levels used in the computer and LVDAME self-check circuitry. A "1" input causes a "1" output, and a "0" input causes a "0" output. The nominal input-output levels are as follows: Input — Output "1" (-6 VDC) — "1" (+6 VDC) "0" (0 VDC) — "0" (0 VDC)		
30. TRANSLATOR. This level shifter is used only in the LVDAME self-check circuitry. The nominal input-output levels are as follows: Input — Output "1" (-6 VDC) — "1" (+8 VDC) "0" (0 VDC) — "0" (-2 VDC) A "1" input causes a "1" output, and a "0" input causes a "0" output.		

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used On figure 10-50)
31. TRANSLATOR-INVERTER. This circuit performs level shifting and inversion. This circuit converts the positive logic levels used in the computer and LVDAME self-check circuitry to the negative logic levels used in the LVDAME logic. A "1" input causes a "0" output, and a "0" input causes a "1" output. The nominal input-output levels are as follows: Input — Output "1" (+6 VDC) — "0" (0 VDC) "0" (0 VDC) — "1" (-6 VDC)		
32. TRIGGER 1. This circuit is a bistable device that becomes set (1) if the "1" Set Input becomes a "1" or, (2) if input A is a "0" and input B changes from a "1" to a "0". Similarly, the circuit becomes reset (1) if the "1" Reset Input becomes a "1" or, (2) if input D is a "0" and input C changes from a "1" to a "0".		
33. TRIGGER 2. This circuit is very similar to the TRIGGER 1. The basic difference is that the circuit becomes reset when input C is a "0" and input B changes from a "1" to a "0". This circuit also provides power amplification.	 Note The functional symbol "T + DE" represents "Trigger and Driver, Emitter", "T" may be substituted for "T + DE".	

Circuit Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-50)
34. VOLTAGE DIVIDER. This circuit is a tapped resistor that provides +8 VDC and -8 VDC.  	 	

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