SATURN V

Simplex Models

Laboratory Maintenance Instructions for LVDA

Volume II

Maintenance Data

Space Guidance Center, Owego, New York IBM

VOLUME II OF II

Laboratory Maintenance Instructions

SATURN V
LAUNCH VEHICLE DATA ADAPTER

Simplex Models

NASA Part No. 50M35011
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VOLUME II OF II

MAINTENANCE DATA

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NOTICE

Section V of this manual includes procedures which require the use of the Purging Cart (Tool Number 657900) and the Transport Dolly (Tool Number 656360). As of the publication date of this manual, this equipment has not been delivered; therefore the procedures cannot be performed. Although the procedures have not been verified on the equipment they have been included in the manual for informational purposes.

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SECTION III

INTERFACE AND ADJUSTMENTS

3-1. INTERFACE.

3-2. The data adapter interface is diagrammed in figure 3-1. Figure 3-2 lists all data adapter signals alphabetically by connector and provides a brief description of each signal function.

NOTE

Figure 3-2 is a complete listing of the data adapter signals. Signals identified as belonging to channel 2 or channel 3 are not applicable to the breadboard model.

3-3. ADJUSTMENTS.

3-4. No provision is made for adjustment of data adapter interface signals in the field.

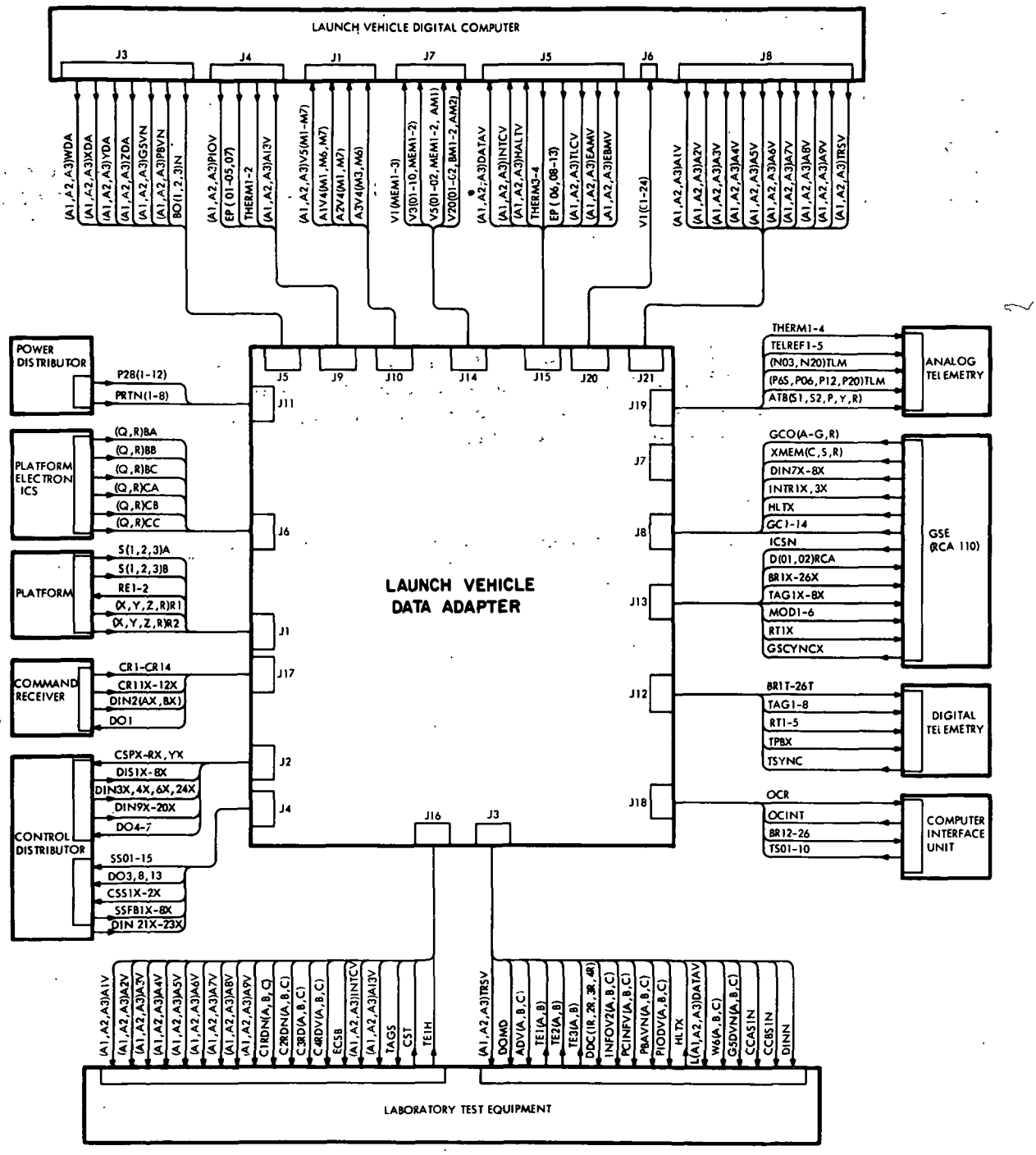


Figure 3-1. Interface Block Diagram

NAME	CONNECTOR	PIN	FUNCTION
RE1EX	J1	A	RESOLVER EXCIT 1
*RE1RTN	J1	B	RESOLVER EXCIT 1 RET
RE1SHD	J1	CC	RESOLVER EXCITATION 1 SHIELD
RE2EX	J1	C	RESOLVER EXCIT 2
*RE2RTN	J1	D	RESOLVER EXCIT 2 RET
RE2SHD	J1	DD	RESOLVER EXCITATION 2 SHIELD
*RR1PA	J1	□D	R RESOLVER FINE PHASE A
*RR1PB	J1	□E	R RESOLVER FINE PHASE B
*RR1RTN	J1	□C	R RESOLVER FINE RET
RR1SHD	J1	FF	R FINE RES SHIELD
*RR2PA	J1	□A	R RESOLVER COARSE PHASE A
*RR2PB	J1	□B	R RESOLVER COARSE PHASE B
*RR2RTN	J1	Z	R RESOLVER COARSE RET
RR2SHD	J1	EE	R COARSE RES SHIELD
*S1ACOS	J1	□G	XA ACCEL COARSE RESOLVER COSINE
*S1ARTN	J1	□F	XA ACCEL COARSE RESOLVER RETURN
S1ASHD	J1	EE	X ACCEL 1 SHIELD
*S1ASIN	J1	□H	XA ACCEL COARSE RESOLVER SINE
*S1BCOS	J1	□J	XB ACCEL COARSE RESOLVER COS
*S1BRTN	J1	□I	XB ACCEL COARSE RESOLVER RET
S1BSHD	J1	EE	X ACCEL 2 SHIELD
*S1BSIN	J1	□K	XB ACCEL COARSE RESOLVER SIN
*S2ACOS	J1	□N	YA ACCEL FINE RESOLVER COS
*S2ARTN	J1	□M	YA ACCEL FINE RESOLVER RET
S2ASHD	J1	EE	Y ACCEL 1 SHIELD
*S2ASIN	J1	□P	YA ACCEL FINE RESOLVER SIN
*S2BCOS	J1	□R	YB ACCEL COARSE RESOLVER COS
*S2BRTN	J1	□Q	YB ACCEL COARSE RESOLVER RET
S2BSHD	J1	FF	Y COARSE RES
S2BSHD	J1	FF	Y ACCEL 2 SHIELD
*S2BSIN	J1	□S	YB ACCEL COARSE RESOLVER SIN
*S3ACOS	J1	□U	ZA ACCEL FINE RESOLVER COS
*S3ARTN	J1	□T	ZA ACCEL FINE RESOLVER RET
S3ASHD	J1	FF	Z ACCEL 1 SHIELD
*S3ASIN	J1	□V	ZA ACCEL FINE RESOLVER SIN
*S3BCOS	J1	□X	ZB ACCEL FINE RESOLVER COS
*S3BRTN	J1	□W	ZB ACCEL FINE RESOLVER RET
S3BSHD	J1	FF	Z ACCEL 2 SHIELD
*S3BSIN	J1	□Y	ZB ACCEL FINE RESOLVER SIN
*XR1PA	J1	R	X RESOLVER FINE RET
*XR1PB	J1	S	X RESOLVER FINE PHASE B
*XR1RTN	J1	P	X RESOLVER FINE PHASE A
XR1SHD	J1	EE	X FINE RES SHIELD
*XR2PA	J1	M	X RESOLVER FINE RET
*XR2PB	J1	N	X RESOLVER FINE PHASE B
*XR2RTN	J1	L	X RESOLVER FINE PHASE A
XR2SHD	J1	FF	X COARSE RES SHIELD
*YR1PA	J1	X	Y RESOLVER FINE PHASE A
*YR1PB	J1	Y	Y RESOLVER FINE PHASE B
*YR1RTN	J1	W	Y RESOLVER FINE RET
YR1SHD	J1	EE	Y FINE RES SHIELD
*YR2PA	J1	U	Y RESOLVER COARSE PHASE A
*YR2PB	J1	V	Y RESOLVER COARSE PHASE B
*YR2RTN	J1	T	Y RESOLVER COARSE RET
YR2SHD	J1	FF	Y COARSE RES SHIELD

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 1 of 20)

NAME	CONNECTOR	PIN	FUNCTION
*ZR1PA	J1	J	Z RESOLVER FINE PHASE A
*ZR1PB	J1	K	Z RESOLVER FINE PHASE B
*ZR1RTN	J1	H	Z RESOLVER FINE RET
ZR1SHD	J1	FF	Z FINE RES SHIELD
*ZR2PA	J1	F	Z RESOLVER COARSE PHASE A
*ZR2PB	J1	G	Z RESOLVER COARSE PHASE B
*ZR2RTN	J1	E	Z RESOLVER COARSE RET
ZR2SHD	J1	EE	Z COARSE RES SHIELD
	J1	HH	CHASSIS
	J1	□Z	
	J1	AA	
	J1	BB	
	J1	GG	
CSPRTN	J2	□W	CHI X COMMAND RET
CSPRTND	J2	□X	CHI X COMMAND RET DUPL
CSPSHD	J2	□F	CHI X COMMAND SHIELD
CSPX	J2	FF	CHI X COMMAND
CSPXD	J2	□Y	CHI X COMMAND DUPL
CSRRTN	J2	□I	CHI Y COMMAND RET
CSRRTND	J2	P	CHI Y COMMAND RET DUPL
CSRSHD	J2	□F	CHI Y COMMAND SHIELD
CSRX	J2	□J	CHI Y COMMAND
CSRXD	J2	R	CHI Y COMMAND DUPL
CSYRTN	J2	L	CHI Z COMMAND RET
CSYRTND	J2	M	CHI Z COMMAND RET DUPL
CSYSHD	J2	□F	CHI Z COMMAND SHIELD
CSYX	J2	□G	CHI Z COMMAND
CSYXD	J2	□H	CHI Z COMMAND DUPL
*DIN10X	J2	□T	S3 SEPARATION
*DIN11X	J2	□N	S2 SKIRT SEPARATE
*DIN12X	J2	□P	S1C SEPARATION
*DIN13X	J2	□Q	S2 ENGINE OUT
*DIN14X	J2	□R	S1 ENGINE OUT
*DIN15X	J2	Z	S3 THRUST TERMINATION
*DIN16X	J2	E	S2 THRUST TERMINATION
*DIN17X	J2	U	S1 THRUST TERMINATION
*DIN18X	J2	X	SPARE 11 DISCRETE
*DIN19X	J2	V	SIV MANUAL VENT
*DIN20X	J2	W	SIV THRUST SEQUENCE
*DIN3X	J2	BB	AUTO VENT 2
*DIN5X	J2	□S	LIFT OFF
*DIN6X	J2	□A	SIV INJECT DELAY
*DIN6X	J2	CC	AUTO VENT 1
*DIN9X	J2	F	SWITCH S4 TO SC
*DIS1X	J2	AA	SPARE 3 DISCRETE
*DIS2X	J2	□M	SPARE 4 DISCRETE
*DIS3X	J2	S	SPARE 5 DISCRETE
*DIS4X	J2	□B	SPARE 6 DISCRETE
*DIS5X	J2	T	SPARE 7 DISCRETE
*DIS6X	J2	DD	SPARE 8 DISCRETE
*DIS7X	J2	□Z	SPARE 9 DISCRETE
*DIS8X	J2	□K	SPARE 10 DISCRETE
D04	J2	EE	GUIDANCE FAILURE
D05	J2	□U	SPARE 2 D0

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 2)

NAME	CONNECTOR	PIN	FUNCTION
D06	J2	□C	SPARE 1 D0
D07	J2	G	CUT OFF 1 SIVB
*INTR2X	J2	B	S1 LOW LEVEL SENSR
*INTR4X	J2	C	GUIDANCE RELEASE
*INTR5X	J2	A	S1 PROPELLANT DEPL
*INTR6X	J2	D	S2 PROPELLANT DEPL
*INTR7X	J2	Y	SPARE 3 INTERRUPT
SIGSHD	J2	□V	SHIELD
	J2	HH	CHASSIS
	J2	H	
	J2	J	
	J2	K	
	J2	N	
	J2	□D	
	J2	□E	
	J2	GG	
ADVA	J3	D	BIT GATE GEN LATCH
ADVB	J3	Z	BIT GATE GEN LATCH
ADVC	J3	□S	BIT GATE GEN LATCH
A1DATAV	J3	□U	SERIALIZER LATCH, CH 1
A2DATAV	J3	FF	SERIALIZER LATCH, CH 2
A3DATAV	J3	□H	SERIALIZER LATCH, CH3
A1TRSV	J3	A	TRANSFER REG CH 1
A2TRSV	J3	V	TRANSFER REG CH 2
A3TRSV	J3	U	TRANSFER REG CH 3
CCASIN	J3	X	COD COUNTER A SERIALIZER LATCH
CCBSIN	J3	□Q	COD COUNTER B SERIALIZER LATCH
G5DVNA	J3	W	DA BIT GATE 5
G5DVNB	J3	□P	DA BIT GATE 5
G5DVNC	J3	AA	DA BIT GATE 5
INFOV2A	J3	G	COMPUTER INFO DELAYED
INFOV2B	J3	□J	COMPUTER INFO DELAYED
INFOV2C	J3	P	COMPUTER INFO DELAYED
INTRLK	J3	K	LTE INTERLOCK
INTRLK	J3	L	LTE INTERLOCK
DDC1R	J3	□C	DELAY DC1R
DDC2R	J3	□Y	DELAY DC2R
DDC3R	J3	□I	DELAY DC3R
DDC4R	J3	N	DELAY DC4R
DINN	J3	□B	DOM DELAY LINE INPUT LATCH
DOMD	J3	C	DATA OUTPUT MULTIPLEXER DELAYED
*HLTX	J3	□A	LTE HALT
PBAVNA	J3	□N	DA PHASE B
PBAVNB	J3	T	DA PHASE B
PBAVNC	J3	□M	DA PHASE B
PCINFVA	J3	H	PHASE C INFO TRANSFER LATCH
PCINFVB	J3	□D	PHASE C INFO TRANSFER LATCH
PCINFVC	J3	J	PHASE C INFO TRANSFER LATCH
PIODVA	J3	Y	PIO DRIVER
PIODVB	J3	CC	PIO DRIVER
PIODVC	J3	□B	PIO DRIVER
SIGRET	J3	B	SIGNAL RETURN
SIGRET	J3	□E	SIGNAL RET
SIGRET	J3	□R	SIGNAL RET

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 3)

NAME	CONNECTOR	PIN	FUNCTION
SIGRET	J3	□T	SIGNAL RET
SIGRET	J3	□X	SIGNAL RETURN
SIGRET	J3	□Z	SIGNAL RET
*TE1A	J3	DD	LTE INPUT LINE 1A
*TE1B	J3	EE	LTE INPUT LINE 1B
*TE2A	J3	□W	LTE INPUT LINE 2A
*TE2B	J3	□G	LTE INPUT LINE 2B
*TE3A	J3	F	LTE INPUT LINE 3A
*TE3B	J3	E	LTE INPUT LINE 3B
W6A	J3	S	W CLOCK PULSE DRIVER OUTPUT 6A
W6B	J3	□K	W CLOCK PULSE DRIVER OUTPUT 6B
W6C	J3	R	W CLOCK PULSE DRIVER OUTPUT 6C
	J3	HH	FRAME
	J3	M	
	J3	□F	
	J3	□V	
	J3	GG	
CSS1RTD	J4	□X	SPARE LADDER 1 RET DUPL
CSS1RTN	J4	□Y	SPARE LADDER RET
CSS1SHD	J4	□H	SHIELD
CSS1X	J4	FF	SPARE LADDER 1
CSS1XD	J4	□W	SPARE LADDER 1 DUPL
CSS2X	J4	□J	SPARE LADDER
CSS2XD	J4	R	SPARE LADDER 2 DUPL
CSS2RTD	J4	P	SPARE LADDER 2 RET DUPL
CSS2RTN	J4	□I	SPARE LADDER RET
CSS2SHD	J4	□H	SHIELD
D013	J4	S	DO SPARE 3
D03	J4	AA	DO SPARE 1
D08	J4	□M	DO SPARE 2
*SSFB1X	J4	□B	SW SEL FEEDBACK 1
*SSFB2X	J4	□T	SW SEL FEEDBACK 2
*SSFB3X	J4	DD	SW SEL FEEDBACK 3
*SSFB4X	J4	EE	SW SEL FEEDBACK 4
*SSFB5X	J4	□U	SW SEL FEEDBACK 5
*SSFB6X	J4	□C	SW SEL FEEDBACK 6
*SSFB7X	J4	G	SW SEL FEEDBACK 7
*SSFB8X	J4	H	SW SEL FEEDBACK 8
SS01	J4	C	SW SEL ADDRESS 1
SS02	J4	B	SW SEL ADDRESS 2
SS03	J4	A	SW SEL ADDRESS 3
SS04	J4	D	SW SEL ADDRESS 4
SS05	J4	Y	SW SEL ADDRESS 5
SS06	J4	X	SW SEL ADDRESS 6
SS07	J4	W	SW SEL ADDRESS 7
SS08	J4	V	SW SEL ADDRESS 8
SS09	J4	□Q	SW SEL STAGE 1
SS09D	J4	□R	SW SEL STAGE 1D
SS10	J4	Z	SW SEL STAGE 2
SS10D	J4	E	SW SEL STAGE 2D
SS11	J4	F	SW SEL STAGE 3
SS11D	J4	J	SW SEL STAGE 3 DUP
SS12	J4	□S	SW SEL STAGE 4
SS12D	J4	K	SW SEL STAGE 4 DUP

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 4)

NAME	CONNECTOR	PIN	FUNCTION
SS13	J4	CC	SW SEL STAGE 5
SS13D	J4	BB	SW SEL STAGE 5 DUP
SS14	J4	U	SW SEL RESET
SS14D	J4	T	SW SEL RESET DUP
SS15	J4	□N	SW SEL READ
SS15D	J4	□P	SW SEL READ DUP
	J4	HH	FRAME
	J4	L	
	J4	M	
	J4	N	
	J4	□A	
	J4	□D	
	J4	□E	
	J4	□F	
	J4	□G	
	J4	□K	
	J4	□V	
	J4	□Z	
	J4	GG	
*A1G5VN	J5	C	NOT TIMING GATE 5 CH 1
*A2G5VN	J5	□Y	NOT TIMING GATE 5 CH 2
*A3G5VN	J5	□P	NOT TIMING GATE 5 CH 3
*A1PBVN	J5	□S	NOT PHASE B CH 1
*A2PBVN	J5	□A	NOT PHASE B CH 2
*A3PBVN	J5	R	NOT PHASE B CH 1
*A1WDA	J5	□B	W CLOCK TO DA CH 1
*A2WDA	J5	K	W CLOCK TO DA CH 2
*A3WDA	J5	N	W CLOCK TO DA CH 3
*A1XDA	J5	F	X CLOCK TO DA CH 1
*A2XDA	J5	J	X CLOCK TO DA CH 2
*A3XDA	J5	HH	X CLOCK TO DA CH 3
*A1YDA	J5	H	Y CLOCK TO DA CH 1
*A2YDA	J5	□H	Y CLOCK TO DA CH 2
*A3YDA	J5	□K	Y CLOCK TO DA CH 3
*A1ZDA	J5	G	Z CLOCK TO DA CH 1
*A2ZDA	J5	M	Z CLOCK TO DA CH 2
*A3ZDA	J5	□J	Z CLOCK TO DA CH 3
*B01N	J5	DD	BUFFER OSC NOT CH 1
*B02N	J5	□F	BUFFER OSC NOT CH 2
*B03N	J5	□V	BUFFER OSC NOT CH 3
SR07	J5	E	SIGNAL RETURN 07
SR08	J5	L	SIGNAL RETURN 08
SR09	J5	P	SIGNAL RETURN 09
SR10	J5	S	SIGNAL RETURN 10
SR11	J5	Z	SIGNAL RETURN 11
SR12	J5	□C	SIGNAL RETURN 12
SR13	J5	□D	SIGNAL RETURN 13
SR14	J5	□E	SIGNAL RETURN 14
SR15	J5	□G	SIGNAL RETURN 15
SR16	J5	□I	SIGNAL RETURN 16
SR17	J5	□N	SIGNAL RETURN 17
SR18	J5	□R	SIGNAL RETURN 18
SR19	J5	□T	SIGNAL RETURN 19
SR20	J5	□U	SIGNAL RETURN 20

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 5)

NAME	CONNECTOR	PIN	FUNCTION
SR21	J5	□W	SIGNAL RETURN 21
SR22	J5	□X	SIGNAL RETURN 22
SR23	J5	□Z	SIGNAL RETURN 23
SR24	J5	CC	SIGNAL RETURN 24
SR25	J5	EE	SIGNAL RETURN 25
SR26	J5	FF	SIGNAL RETURN 26
SR27	J5	GG	SIGNAL RETURN 27
	J5	A	
	J5	B	
	J5	D	
	J5	T	
	J5	U	
	J5	V	
	J5	W	
	J5	X	
	J5	Y	
	J5	□M	
	J5	□Q	
	J5	AA	
	J5	BB	
*QBA	J6	A	X ACCEL OPTISYN 1 Q
*QBB	J6	B	Y ACCEL OPTISYN 1 Q
*QBC	J6	X	Z ACCEL OPTISYN 1 R
*QCA	J6	E	Y ACCEL OPTISYN 2 Q
*QCC	J6	H	X ACCEL OPTISYN 2 Q
*QCB	J6	□A	Z ACCEL OPTISYN 2 Q
*QRARTN	J6	□K	Z ACCEL RET
*QRBRTN	J6	□N	Y ACCEL RET
*QRCRTN	J6	□P	X ACCEL RET
*RBA	J6	Y	X ACCEL OPTISYN 1 R
*RBB	J6	D	Y ACCEL OPTISYN 1 R
*RBC	J6	Z	Z ACCEL OPTISYN 1 R
*RCA	J6	□C	Y ACCEL OPTISYN 2R
*RCB	J6	J	Z ACCEL OPTISYN 2 R
*RCC	J6	□D	X ACCEL OPTISYN 2R
XASHD	J6	□M	X ACCEL SHIELD
YASHD	J6	□M	Y ACCEL SHIELD
ZASHD	J6	□M	Z ACCEL SHIELD
	J6	□T	CHASSIS
	J6	C	
	J6	F	
	J6	G	
	J6	K	
	J6	L	
	J6	M	
	J6	N	
	J6	P	
	J6	R	
	J6	S	
	J6	T	
	J6	U	
	J6	V	
	J6	W	
	J6	□B	

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 6)

NAME	CONNECTOR	PIN	FUNCTION
	J6	□E	
	J6	□F	
	J6	□G	
	J6	□H	
	J6	□I	
	J6	□J	
	J6	□Q	
	J6	□R	
	J6	□S	
*DIN21X	J7	M	LOCKON 4 DISC INPUT
*DIN22X	J7	L	LOCKON 3 DISC INPUT
*DIN23X	J7	K	LOCKON 2 DISC INPUT
*DIN24X	J7	J	LOCKON 1 DISC INPUT
DO09	J7	H	SCAN 4 DISC OUTPUT
DO10	J7	G	SCAN 3 DISC OUTPUT
DO11	J7	F	SCAN 2 DISC OUTPUT
DO12	J7	E	SCAN 1 DISC OUTPUT
HS1PA	J7	□I	HS 1 RESOLVER PHASE A
HS1PB	J7	□G	HS 1 RESOLVER PHASE B
HS1RTN	J7	□H	HS 1 RESOLVER RET
HS2PA	J7	□D	HS 2 RESOLVER PHASE A
HS2PB	J7	□B	HS 2 RESOLVER PHASE B
HS2RTN	J7	□C	HS 2 RESOLVER RET
HS2SHD	J7	□K	SHIELD
HS3PA	J7	Y	HS 3 RESOLVER PHASE A
HS3PB	J7	W	HS 3 RESOLVER PHASE B
HS3RTN	J7	X	HS 3 RESOLVER RET
HS3SHD	J7	□R	SHIELD
HS4PA	J7	T	HS 4 RESOLVER PHASE A
HS4PB	J7	R	HS 4 RESOLVER PHASE B
HS4RTN	J7	S	HS 4 RESOLVER RET
HS4SHD	J7	□K	SHIELD
H1C	J7	□E	HS 1 RESOLVER COMP
H1CRTN	J7	□F	HS 1 RESOLVER COMP RET
H2C	J7	Z	HS 2 RESOLVER COMP
H2CRTN	J7	□A	HS 2 RESOLVER COMP RET
H2CSHD	J7	□K	SHIELD
H3C	J7	U	HS 3 RESOLVER COMP
H3CRTN	J7	V	HS 3 RESOLVER COMP RET
H4C	J7	N	HS 4 RESOLVER COMP
H4CRTN	J7	P	HS 4 RESOLVER COMP RET
RE1EXH	J7	A	RESOLVER EXCIT 1
RE2EXH	J7	C	RESOLVER EXCIT 2
R1RTNH	J7	B	RESOLVER EXCIT 1 RET
R1SHDH	J7	□M	RESOLVER EXCIT 1 SHIELD
R2RTNH	J7	D	RESOLVER EXCIT 2 RET
R2SHDH	J7	□N	RESOLVER EXCIT 2 SHIELD
	J7	□T	CHASSIS
	J7	□J	
	J7	□P	
	J7	□Q	
	J7	□S	

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 7)

NAME	CONNECTOR	PIN	FUNCTION
*DIN7X	J8	□I	DISCRETE INPUT INTERFACE LINE 7
*DIN8X	J8	N	DISCRETE INPUT INTERFACE LINE 8
*GC0A	J8	EE	GSE INPUT LINE A
*GC0B	J8	DD	GSE INPUT LINE B
*GC0C	J8	□S	GSE INPUT LINE C
*GC0D	J8	Z	GSE INPUT LINE D
*GC0E	J8	D	GSE INPUT LINE E
*GC0F	J8	E	GSE INPUT LINE F
*GC0G	J8	□A	GSE INPUT LINE G
*GC0R	J8	□T	GSE INPUT LINE RESET
*GC1	J8	U	GSE INPUT LINE 1
*GC2	J8	T	GSE INPUT LINE 2
*GC3	J8	S	GSE INPUT LINE 3
*GC4	J8	A	GSE INPUT LINE 4
*GC5	J8	V	GSE INPUT LINE 5
*GC6	J8	□N	GSE INPUT LINE 6
*GC7	J8	□M	GSE INPUT LINE 7
*GC8	J8	□K	GSE INPUT LINE 8
*GC9	J8	R	GSE INPUT LINE 9
*GC10	J8	B	GSE INPUT LINE 10
*GC11	J8	W	GSE INPUT LINE 11
*GC12	J8	□P	GSE INPUT LINE 12
*GC13	J8	AA	GSE INPUT LINE 13
*GC14	J8	□Z	GSE INPUT LINE 14
*HLTX	J8	□Y	LTE HALT
H3CSHD	J8	□R	SHIELD
H4CSHD	J8	□R	SHIELD
*INTR1X	J8	BB	INTERRUPT 1X
*INTR3X	J8	□Q	INTERRUPT 3X
*XMEMC	J8	M	GSE INPUT MEMORY CONNECT
*XMEMR	J8	□W	GSE INPUT MEMORY RELEASE
*XMEMS	J8	□G	GSE INPUT MEMORY SHORT
	J8	HH	FRAME
	J8	C	
	J8	F	
	J8	G	
	J8	H	
	J8	J	
	J8	K	
	J8	L	
	J8	P	
	J8	X	
	J8	Y	
	J8	□B	
	J8	□C	
	J8	□D	
	J8	□E	
	J8	□F	
	J8	□H	
	J8	□J	
	J8	□R	
	J8	□U	
	J8	□V	
	J8	□X	
	J8	CC	

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 8)

NAME	CONNECTOR	PIN	FUNCTION
	J8	FF	
	J8	GG	
*A1AI3V	J9	□M	ACC-INST CTR CH 1
*A2AI3V	J9	□Z	ACC-INST CTR CH 2
*A3AI3V	J9	□G	ACC-INST CTR CH 3
*A1PIOV	J9	GG	PROCESS IN/OUT CH 1
*A2PIOV	J9	U	**PROCESS IN/OUT CH 2**
*A3PIOV	J9	C	PROCESS IN/OUT CH 3
	J9	E	
*EP01	J9	W	ERROR SIGNAL 01
*EP02	J9	□R	ERROR SIGNAL 02
*EP03	J9	T	ERROR SIGNAL 03
*EP04	J9	AA	ERROR SIGNAL 04
*EP06	J9	V	ERROR SIGNAL 06
*EP07	J9	□N	ERROR SIGNAL 07
SR28	J9	A	SIGNAL RETURN 28
SR29	J9	B	SIGNAL RETURN 29
SR30	J9	P	SIGNAL RETURN 30
SR31	J9	S	SIGNAL RETURN 31
SR32	J9	X	SIGNAL RETURN 32
SR33	J9	Z	SIGNAL RETURN 33
SR34	J9	□P	SIGNAL RETURN 34
SR35	J9	□S	SIGNAL RETURN 35
SR36	J9	BB	SIGNAL RETURN 36
SR37	J9	CC	SIGNAL RETURN 37
SR38	J9	HH	SIGNAL RETURN 38
*THERM1	J9	Y	THERMISTOR 1 LEAD 1
*THERM2	J9	D	THERMISTOR 1 LEAD 2
	J9	F	
	J9	G	
	J9	H	
	J9	J	
	J9	K	
	J9	L	
	J9	M	
	J9	N	
	J9	R	
	J9	□A	
	J9	□B	
	J9	□C	
	J9	□E	
	J9	□F	
	J9	□G	
	J9	□H	
	J9	□I	
	J9	□J	
	J9	□K	
	J9	□T	
	J9	□U	
	J9	□V	
	J9	□W	
	J9	□X	
	J9	□Y	
	J9	DD	

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 9)

NAME	CONNECTOR	PIN	FUNCTION
	J9	EE	
	J9	FF	
A1V4M1	J10	HH	PLUS 6 MOD SW CH 1 MOD 1
A2V4M1	J10	J	PLUS 6 MOD SW CH 2 MOD 1
A3V4M1	J10	FF	PLUS 6 MOD SW CH 3 MOD 1
A1V4M2	J10	BB	PLUS 6 MOD SW CH 1 MOD 2
A2V4M2	J10	¤E	PLUS 6 MOD SW CH 2 MOD 2
A3V4M2	J10	¤W	PLUS 6 MOD SW CH 3 MOD 2
A1V4M3	J10	AA	PLUS 6 MOD SW CH 1 MOD 3
A2V4M3	J10	¤F	PLUS 6 MOD SW CH 2 MOD 3
A3V4M3	J10	¤I	PLUS 6 MOD SW CH 3 MOD 3
A1V4M4	J10	CC	PLUS 6 MOD SW CH 1 MOD 4
A2V4M4	J10	¤G	PLUS 6 MOD SW CH 2 MOD 4
A3V4M4	J10	EE	PLUS 6 MOD SW CH 3 MOD 4
A1V4M5	J10	¤Q	PLUS 6 MOD SW CH 1 MOD 5
A2V4M5	J10	¤D	PLUS 6 MOD SW CH 2 MOD 5
A3V4M5	J10	¤V	PLUS 6 MOD SW CH 3 MOD 5
A1V4M6	J10	GG	PLUS 6 MOD SW CH 1 MOD 6
A2V4M6	J10	K	PLUS 6 MOD SW CH 2 MOD 6
A3V4M6	J10	¤U	PLUS 6 MOD SW CH 3 MOD 6
A1V4M7	J10	¤Y	PLUS 6 MOD SW CH 1 MOD 7
A2V4M7	J10	L	PLUS 6 MOD SW CH 2 MOD 7
A3V4M7	J10	DD	PLUS 6 MOD SW CH 3 MOD 7
A1V5M1	J10	Y	PLUS 12 MOD SW CH 1 MOD 1
A2V5M1	J10	¤T	PLUS 12 MOD SW CH 2 MOD 1
A3V5M1	J10	¤P	PLUS 12 MOD SW CH 3 MOD 1
A1V5M2	J10	¤R	PLUS 12 MOD SW CH 1 MOD 2
A2V5M2	J10	G	PLUS 12 MOD SW CH 2 MOD 2
A3V5M2	J10	V	PLUS 12 MOD SW CH 3 MOD 2
A1V5M3	J10	C	PLUS 12 MOD SW CH 1 MOD 3
A2V5M3	J10	¤C	PLUS 12 MOD SW CH 2 MOD 3
A3V5M3	J10	W	PLUS 12 MOD SW CH 3 MOD 3
A1V5M4	J10	B	PLUS 12 MOD SW CH 1 MOD 4
A2V5M4	J10	H	PLUS 12 MOD SW CH 2 MOD 4
A3V5M4	J10	A	PLUS 12 MOD SW CH 3 MOD 4
A1V5M5	J10	¤S	PLUS 12 MOD SW CH 1 MOD 5
A2V5M5	J10	¤A	PLUS 12 MOD SW CH 2 MOD 5
A3V5M5	J10	¤N	PLUS 12 MOD SW CH 3 MOD 5
A1V5M6	J10	D	PLUS 12 MOD SW CH 1 MOD 6
A2V5M6	J10	F	PLUS 12 MOD SW CH 2 MOD 6
A3V5M6	J10	T	PLUS 12 MOD SW CH 3 MOD 6
A1V5M7	J10	Z	PLUS 12 MOD SW CH 1 MOD 7
A2V5M7	J10	¤B	PLUS 12 MOD SW CH 2 MOD 7
A3V5M7	J10	U	PLUS 12 MOD SW CH 3 MOD 7
SR01	J10	E	SIGNAL RETURN 01
SR02	J10	M	SIGNAL RETURN 02
SR03	J10	X	SIGNAL RETURN 03
SR04	J10	¤M	SIGNAL RETURN 04
SR05	J10	¤X	SIGNAL RETURN 05
SR06	J10	¤Z	SIGNAL RETURN 06
	J10	N	
	J10	P	
	J10	R	
	J10	S	

* INDICATES INPUT ¤ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 10)

NAME	CONNECTOR	PIN	FUNCTION
	J10	□H	
	J10	□J	
	J10	□K	
*PRTN-1	J11	J	POWER RETURN
*PRTN-2	J11	K	POWER RETURN
*PRTN-3	J11	L	POWER RETURN
*PRTN-4	J11	M	POWER RETURN
*PRTN-5	J11	N	POWER RETURN
*PRTN-6	J11	P	POWER RETURN
*PRTN-7	J11	R	POWER RETURN
*PRTN-8	J11	S	POWER RETURN
*P28-1	J11	A	PLUS 28 VOLTS
*P28-2	J11	B	PLUS 28 VOLTS
*P28-3	J11	C	PLUS 28 VOLTS
*P28-4	J11	D	PLUS 28 VOLTS
*P28-5	J11	E	PLUS 28 VOLTS
*P28-6	J11	F	PLUS 28 VOLTS
*P28-7	J11	G	PLUS 28 VOLTS
*P28-8	J11	H	PLUS 28 VOLTS
*P28-9	J11	T	PLUS 28 VOLTS
*P28-10	J11	U	PLUS 28 VOLTS
*P28-11	J11	V	PLUS 28 VOLTS
*P28-12	J11	W	PLUS 28 VOLTS
	J11	X	
BR01	J12	A	BRD01 H DRIVER OUTPUT
BR02	J12	W	BUFFER REG LATCH 02 OUTPUT DRIVER
BR03	J12	V	BUFFER REG LATCH 03 OUTPUT DRIVER
BR04	J12	U	BUFFER REG LATCH 04 OUTPUT DRIVER
BR05	J12	□P	BUFFER REG LATCH 05 OUTPUT DRIVER
BR06	J12	□N	BUFFER REG LATCH 06 OUTPUT DRIVER
BR07	J12	T	BUFFER REG LATCH 07 OUTPUT DRIVER
BR08	J12	AA	**BUFFER REG LATCH 08 OUTPUT DRIVER**
BR09	J12	□M	BUFFER REG LATCH 09 OUTPUT DRIVER
BR10	J12	S	BUFFER REG LATCH 10 OUTPUT DRIVER
BR11	J12	□Y	BUFFER REG LATCH 11 OUTPUT DRIVER
BR12	J12	□J	BUFFER REG LATCH 12 OUTPUT DRIVER
BR13	J12	R	BUFFER REG LATCH 13 OUTPUT DRIVER
BR14	J12	□X	BUFFER REG LATCH 14 OUTPUT DRIVER
BR15	J12	□I	BUFFER REG LATCH 15 OUTPUT DRIVER
BR16	J12	P	BUFFER REG LATCH 16 OUTPUT DRIVER
BR17	J12	□G	BUFFER REG LATCH 17 OUTPUT DRIVER
BR18	J12	N	BUFFER REG LATCH 18 OUTPUT DRIVER
BR19	J12	M	BUFFER REG LATCH 19 OUTPUT DRIVER
BR20	J12	L	BUFFER REG LATCH 20 OUTPUT DRIVER
BR21	J12	J	BUFFER REG LATCH 21 OUTPUT DRIVER
BR22	J12	K	BUFFER REG LATCH 22 OUTPUT DRIVER
BR23	J12	□E	BUFFER REG LATCH 23 OUTPUT DRIVER
BR24	J12	H	BUFFER REG LATCH 24 OUTPUT DRIVER
BR25	J12	□D	BUFFER REG LATCH 25 OUTPUT DRIVER
BR26	J12	□V	BUFFER REG LATCH 26 OUTPUT DRIVER
FILRTN1	J12	□K	FILTER POWER RET
FILRTN2	J12	□H	FILTER POWER RET
FILRTN3	J12	□U	FILTER POWER RET

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 11)

NAME	CONNECTOR	PIN	FUNCTION
FILRTN4	J12	DD	FILTER POWER RET
GP1SHD	J12	¤Z	SHIELD
GP2SHD	J12	¤Z	SHIELD
GP3SHD	J12	¤Z	SHIELD
GP4SHD	J12	¤Z	SHIELD
RT1	J12	¤S	DIG TEL TAG 10
RT2	J12	CC	DIG TEL TAG 11
RT3	J12	BB	DIG TEL TAG 12
RT4	J12	¤B	REAL TIME REG LATCH 4
RT5	J12	¤A	REAL TIME REG LATCH 5
STRTN1	J12	D	
STRTN2	J12	E	
TAG01	J12	¤F	DIG TEL TAG 1
TAG02	J12	¤W	DIG TEL TAG 2
TAG03	J12	FF	DIG TEL TAG 3
TAG04	J12	EE	DIG TEL TAG 4
TAG05	J12	X	DIG TEL TAG 5
TAG06	J12	¤R	DIG TEL TAG 6
TAG07	J12	¤Q	DIG TEL TAG 7
TAG08	J12	F	DIG TEL TAG 8
TPBX	J12	¤T	DIG TEL PARITY BIT
*TSRTN	J12	¤C	SAMPLE PULSE RET
TSSHD	J12	¤Z	SHIELD
*TSYNC	J12	G	SAMPLE PULSE
	J12	HH	FRAME
	J12	B	
	J12	C	
	J12	Y	
	J12	Z	
	J12	GG	
BR1X	J13	¤R	BUFFER REG LATCH 1 GSE OUTPUT
BR2X	J13	CC	BUFFER REG LATCH 2 GSE OUTPUT
BR3X	J13	Z	BUFFER REG LATCH 3 GSE OUTPUT
BR4X	J13	¤S	BUFFER REG LATCH 4 GSE OUTPUT
BR5X	J13	E	BUFFER REG LATCH 5 GSE OUTPUT
BR6X	J13	¤A	BUFFER REG LATCH 6 GSE OUTPUT
BR7X	J13	F	BUFFER REG LATCH 7 GSE OUTPUT
BR8X	J13	¤B	BUFFER REG LATCH 8 GSE OUTPUT
BR9X	J13	G	BUFFER REG LATCH 9 GSE OUTPUT
BR10X	J13	¤T	BUFFER REG LATCH 10 GSE OUTPUT
BR11X	J13	¤C	BUFFER REG LATCH 11 GSE OUTPUT
BR12X	J13	DD	BUFFER REG LATCH 12 GSE OUTPUT
BR13X	J13	¤U	BUFFER REG LATCH 13 GSE OUTPUT
BR14X	J13	EE	BUFFER REG LATCH 14 GSE OUTPUT
BR15X	J13	FF	BUFFER REG LATCH 15 GSE OUTPUT
BR16X	J13	¤Z	BUFFER REG LATCH 16 GSE OUTPUT
BR17X	J13	¤Y	BUFFER REG LATCH 17 GSE OUTPUT
BR18X	J13	¤K	BUFFER REG LATCH 18 GSE OUTPUT
BR19X	J13	¤J	BUFFER REG LATCH 19 GSE OUTPUT
BR20X	J13	R	BUFFER REG LATCH 20 GSE OUTPUT
BR21X	J13	P	BUFFER REG LATCH 21 GSE OUTPUT
BR22X	J13	¤I	BUFFER REG LATCH 22 GSE OUTPUT
BR23X	J13	¤X	BUFFER REG LATCH 23 GSE OUTPUT
BR24X	J13	¤W	BUFFER REG LATCH 24 GSE OUTPUT

* INDICATES INPUT ¤ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 12)

NAME	CONNECTOR	PIN	FUNCTION
BR25X	J13	□V	BUFFER REG LATCH 25 GSE OUTPUT
BR26X	J13	□D	BUFFER REG LATCH 26 GSE OUTPUT
*DIN1X	J13	□H	DISCRETE INPUT INTERFACE LINE 1
D01RCA	J13	J	DISCRETE OUTPUT REG LATCH 1 GSE OUTPUT
D02RCA	J13	□E	DISCRETE OUTPUT REG LATCH 2 GSE OUTPUT
*GCSYNCX	J13	□G	GSE SYNC
ICSN	J13	□F	
MOD1	J13	D	MODE REG LATCH 1
MOD2	J13	Y	MODE REG LATCH 2
MOD3	J13	C	MODE REG LATCH 3
MOD4	J13	B	MODE REG LATCH 4
MOD5	J13	X	MODE REG LATCH 5
MOD6	J13	W	MODE REG LATCH 6
RT1X	J13	H	REAL TIME LATCH 1 GSE OUTPUT
TAG1X	J13	T	TAG REG LATCH 1 GSE OUTPUT
TAG2X	J13	S	TAG REG LATCH 2 GSE OUTPUT
TAG3X	J13	□N	TAG REG LATCH 3 GSE OUTPUT
TAG4X	J13	□M	TAG REG LATCH 4 GSE OUTPUT
TAG5X	J13	□P	TAG REG LATCH 5 GSE OUTPUT
TAG6X	J13	AA	TAG REG LATCH 6 GSE OUTPUT
TAG7X	J13	□Q	TAG REG LATCH 7 GSE OUTPUT
TAG8X	J13	BB	TAG REG LATCH 8 GSE OUTPUT
	J13	HH	FRAME
	J13	A	
	J13	K	
	J13	L	
	J13	M	
	J13	N	
	J13	U	
	J13	V	
	J13	GG	
ETI-1	J14	E	ELAPSED TIME IND 1
ETI-2	J14	F	ELAPSED TIME IND 2
INTRLK	J14	GG	LTE INTERLOCK
INTRLK	J14	HH	LTE INTERLOCK
SRMEM01	J14	A	SIGNAL RETURN MEM 01
SRMEM02	J14	B	SIGNAL RETURN MEM 02
SRMEM03	J14	C	SIGNAL RETURN MEM 03
SRMEM04	J14	D	SIGNAL RETURN MEM 04
SRMEM05	J14	U	SIGNAL RETURN MEM 05
SRMEM06	J14	V	SIGNAL RETURN MEM 06
SRMEM07	J14	Y	SIGNAL RETURN MEM 07
SRMEM08	J14	□B	SIGNAL RETURN MEM 08
SRMEM09	J14	G	SIGNAL RETURN MEM 09
SRMEM10	J14	□Q	SIGNAL RETURN MEM 10
SRMEM11	J14	AA	SIGNAL RETURN MEM 11
SR73	J14	□D	SIGNAL RETURN 73
SR75	J14	J	SIGNAL RETURN 75
SR76	J14	M	SIGNAL RETURN 76
SR77	J14	□G	SIGNAL RETURN 77
SR78	J14	□I	SIGNAL RETURN 78
SR79	J14	□J	SIGNAL RETURN 79
SR80	J14	□M	SIGNAL RETURN 80
SR82	J14	□X	SIGNAL RETURN 82

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 13)

NAME	CONNECTOR	PIN	FUNCTION
SR83	J14	□Z	SIGNAL RETURN 83
SR85	J14	EE	SIGNAL RETURN 85
V1MEM1	J14	□R	PLUS 6 VDC MEM 01
V1MEM2	J14	BB	PLUS 6 VDC MEM 02
V1MEM3	J14	CC	PLUS 6 VDC MEM 03
V20AM1	J14	□A	PLUS 20 VDC MEM A1
V20AM2	J14	□T	PLUS 20 VDC MEM A2
V20BM1	J14	W	PLUS 20 VDC MEM B1
V20BM2	J14	□N	PLUS 20 VDC MEM B2
V20 01	J14	L	PLUS 20 VDC 01
V20 02	J14	□F	PLUS 20 VDC 02
V3MEM1	J14	X	MINUS 3 VDC MEM 01
V3MEM2	J14	□P	MINUS 3 VDC MEM 02
V3 01	J14	□H	MINUS 3 VDC 01
V3 02	J14	N	MINUS 3 VDC 02
V3 03	J14	P	MINUS 3 VDC 03
V3 04	J14	R	MINUS 3 VDC 04
V3 05	J14	S	MINUS 3 VDC 05
V3 06	J14	□V	MINUS 3 VDC 06
V3 07	J14	□Y	MINUS 3 VDC 07
V3 08	J14	□K	MINUS 3 VDC 08
V3 09	J14	□W	MINUS 3 VDC 09
V3 10	J14	FF	MINUS 3 VDC 10
V5MEM1	J14	Z	PLUS 12 VDC MEM 01
V5MEM2	J14	□S	PLUS 12 VDC MEM 02
V5 01	J14	K	PLUS 12 VDC 01
V5 02	J14	□E	PLUS 12 VDC 02
	J14	H	
	J14	T	
	J14	□C	
	J14	□U	
	J14	DD	
A1DATAV	J15	R	I/O TSFR REG CH 1
A2DATAV	J15	GG	I/O TSFR REG CH 2
A3DATAV	J15	□B	I/O TSFR REG CH 3
*A1EAMV	J15	□P	EV MEM ERROR, CH 1
*A2EAMV	J15	□Z	EV MEM ERROR, CH 2
*A3EAMV	J15	AA	EV MEM ERROR, CH 3
*A1EBMV	J15	U	ODD MEM ERROR, CH 1
*A2EBMV	J15	□J	ODD MEM ERROR, CH 2
*A3EBMV	J15	□K	ODD MEM ERROR, CH 3
A1HALTV	J15	P	HALT SIG FOR CH 1
A2HALTV	J15	A	HALT SIG FOR CH 2
A3HALTV	J15	G	HALT SIG FOR CH 3
A1INTCV	J15	N	INTERRUPT COMP CH 1
A2INTCV	J15	FF	INTERRUPT COMP, CH 2
A3INTCV	J15	□C	INTERRUPT COMP, CH 3
*A1TLCV	J15	T	SIMUL MEM ERR, CH 1
*A2TLCV	J15	S	SIMUL MEM ERR, CH 2
*A3TLCV	J15	□I	SIMUL MEM ERR, CH 3
*EP05	J15	H	ERROR SIGNAL 05
*EP08	J15	Z	ERROR SIGNAL 08
*EP09	J15	□N	ERROR SIGNAL 09
*EP10	J15	V	ERROR SIGNAL 10

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 14)

NAME	CONNECTOR	PIN	FUNCTION
*EP11	J15	E	ERROR SIGNAL 11
EP12	J15	□Q	ERROR SIGNAL 12
*EP13	J15	BB	ERROR SIGNAL 13
SR39	J15	B	SIGNAL RETURN 39
SR40	J15	C	SIGNAL RETURN 40
SR41	J15	W	SIGNAL RETURN 41
SR42	J15	□A	SIGNAL RETURN 42
SR43	J15	□D	SIGNAL RETURN 43
SR44	J15	□H	SIGNAL RETURN 44
SR45	J15	□S	SIGNAL RETURN 45
SR46	J15	□X	SIGNAL RETURN 46
SR47	J15	CC	SIGNAL RETURN 47
SR90	J15	□R	SIGNAL RETURN 90
*THERM3	J15	Y	THERMISTOR 2 LEAD 1
*THERM4	J15	D	THERMISTOR 2 LEAD 2
	J15	F	
	J15	J	
	J15	K	
	J15	L	
	J15	M	
	J15	X	
	J15	□E	
	J15	□F	
	J15	□G	
	J15	□M	
	J15	□T	
	J15	□U	
	J15	□V	
	J15	□W	
	J15	□Y	
	J15	DD	
	J15	EE	
	J15	HH	
A1A1V	J16	A	ADDRESS REG LATCH 1, CH 1
A2A1V	J16	B	ADDRESS REG LATCH 1, CH 2
A3A1V	J16	□J	ADDRESS REG LATCH 1, CH 3
A1A2V	J16	V	ADDRESS REG LATCH 2, CH 1
A2A2V	J16	□N	ADDRESS REG LATCH 2, CH 2
A3A2V	J16	M	ADDRESS REG LATCH 2, CH 3
A1A3V	J16	□K	ADDRESS REG LATCH 3, CH 1
A2A3V	J16	R	ADDRESS REG LATCH 3, CH 2
A3A3V	J16	W	ADDRESS REG LATCH 3, CH 3
A1A4V	J16	□P	ADDRESS REG LATCH 4, CH 1
A2A4V	J16	AA	ADDRESS REG LATCH 4, CH 2
A3A4V	J16	P	ADDRESS REG LATCH 4, CH 3
A1A5V	J16	C	ADDRESS REG LATCH 5, CH 1
A2A5V	J16	X	ADDRESS REG LATCH 5, CH 2
A3A5V	J16	BB	ADDRESS REG LATCH 5, CH 3
A1A6V	J16	□Q	ADDRESS REG LATCH 6, CH 1
A2A6V	J16	FF	ADDRESS REG LATCH 6, CH 2
A3A6V	J16	G	ADDRESS REG LATCH 6, CH 3
A1A7V	J16	□I	ADDRESS REG LATCH 7, CH 1
A2A7V	J16	N	ADDRESS REG LATCH 7, CH 2
A3A7V	J16	Y	ADDRESS REG LATCH 7, CH 3

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 15)

NAME	CONNECTOR	PIN	FUNCTION
A1A8V	J16	□Y	ADDRESS REG LATCH 8, CH 1
A2A8V	J16	CC	ADDRESS REG LATCH 8, CH 2
A3A8V	J16	H	ADDRESS REG LATCH 8, CH 3
A1A9V	J16	J	ADDRESS REG LATCH 9, CH 1
A2A9V	J16	□B	ADDRESS REG LATCH 9, CH 2
A3A9V	J16	□H	ADDRESS REG LATCH 9, CH 3
A1A13V	J16	U	INTERFACE SIGNAL, LVDC TO LVDA
A2A13V	J16	T	INTERFACE SIGNAL, LVDC TO LVDA
A3A13V	J16	S	INTERFACE SIGNAL, LVDC TO LVDA
A1INTCV	J16	□C	INTERFACE OUTPUT LATCH, CH 1
A2INTCV	J16	□D	INTERFACE OUTPUT LATCH, CH 2
A3INTCV	J16	K	INTERFACE OUTPUT LATCH, CH 3
*CST	J16	□E	SINGLE STEP
C1RDNA	J16	□S	**CH 1 READ LATCH DELAY NOT, CH A**
C1RDNB	J16	DD	**CH 1 READ LATCH DELAY NOT, CH B**
C1RDNC	J16	EE	**CH 1 READ LATCH DELAY NOT, CH C**
C2RDNA	J16	□W	**CH 2 READ LATCH DELAY NOT, CH A**
C2RDNB	J16	□G	**CH 2 READ LATCH DELAY NOT, CH B**
C2RDNC	J16	□M	**CH 2 READ LATCH DELAY NOT, CH C**
C3RDA	J16	E	**CH 3 READ LATCH DELAY, CH A**
C3RDB	J16	□A	**CH 3 READ LATCH DELAY, CH B**
C3RDC	J16	□U	**CH 3 READ LATCH DELAY, CH C**
C4RDVA	J16	□V	**CH 4 READ LATCH DELAY, CH A**
C4RDVB	J16	□F	**CH 4 READ LATCH DELAY, CH B**
C4RDVC	J16	L	**CH 4 READ LATCH DELAY, CH C**
ECSB	J16	F	ERROR CLOCK SIGNAL LATCH B
INTRLK	J16	□Z	LTE INTERLOCK
INTRLK	J16	GG	LTE INTERLOCK
SIGRET	J16	□R	SIGNAL RET
SIGRET	J16	□T	SIGNAL RET
SIGRET	J16	□X	SIGNAL RET
TAGS	J16	Z	TAG SERIALIZER LATCH
*TEIH	J16	D	LTE INPUT LINE 1
	J16	HH	FRAME
*CR1	J17	N	CR DATA BIT 1
*CR2	J17	M	CR DATA BIT 2
*CR3	J17	L	CR DATA BIT 3
*CR4	J17	K	CR DATA BIT 4
*CR5	J17	P	CR DATA BIT 5
*CR6	J17	□E	CR DATA BIT 6
*CR7	J17	□D	CR DATA BIT 7
*CR8	J17	J	CR DATA BIT 8
*CR9	J17	□F	CR DATA BIT 9
*CR10	J17	□C	CR DATA BIT 10
*CR11	J17	H	CR DATA BIT 11
*CR1IX	J17	A	CR INTERRUPT 1
D01	J17	□H	RESPONSE LIRO
*DIN2AX	J17	X	SYNC 1 REQUEST
*DIN2BX	J17	Y	SYNC 2 REQUEST
*CR12	J17	R	CR DATA BIT 12
*CR12X	J17	B	CR INTERRUPT 2
*CR13	J17	□G	CR DATA BIT 13
*CR14	J17	□Q	CR MODE BIT
	J17	□T	CHASSIS

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 16)

NAME	CONNECTOR	PIN	FUNCTION
	J17	C	
	J17	D	
	J17	E	
	J17	F	
	J17	G	
	J17	S	
	J17	T	
	J17	U	
	J17	V	
	J17	W	
	J17	Z	
	J17	□A	
	J17	□B	
	J17	□I	
	J17	□J	
	J17	□K	
	J17	□M	
	J17	□N	
	J17	□P	
	J17	□R	
	J17	□S	
BR12	J18	W	DDAS ADDRESS 1
BR13	J18	X	DDAS ADDRESS 2
BR14	J18	V	DDAS ADDRESS 3
BR15	J18	□J	DDAS ADDRESS 4
BR16	J18	□K	DDAS ADDRESS 5
BR17	J18	U	DDAS ADDRESS 6
BR18	J18	□I	DDAS ADDRESS 7
BR19	J18	□P	DDAS ADDRESS 8
BR20	J18	□D	DDAS ADDRESS 9
BR21	J18	T	DDAS ADDRESS 10
BR22	J18	□H	DDAS ADDRESS 11
BR23	J18	□R	DDAS ADDRESS 12
BR24	J18	□Q	DDAS ADDRESS 13
BR26	J18	□G	DDAS ADDRESS 15
CS1SHD	J18	□C	DDAS SHIELD
DARTN	J18	F	DA REG DC RET
*OCINT	J18	G	DATA READY INTERRUPT
OCR	J18	A	ORBIT CHECK READY
*TS01	J18	B	DS DATA BIT 1
*TS02	J18	Y	DS DATA BIT 2
*TS03	J18	C	DS DATA BIT 3
*TS04	J18	□M	DS DATA BIT 4
*TS05	J18	Z	DS DATA BIT 5
*TS06	J18	D	DS DATA BIT 6
*TS07	J18	□N	DS DATA BIT 7
*TS08	J18	□A	DS DATA BIT 8
*TS09	J18	E	DS DATA BIT 9
*TS10	J18	□B	DS DATA BIT 10
	J18	□T	FRAME
	J18	H	
	J18	J	
	J18	K	
	J18	L	

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 17)

NAME	CONNECTOR	PIN	FUNCTION
	J18	M	
	J18	N	
	J18	P	
	J18	R	
	J18	S	
	J18	□E	
	J18	□F	
	J18	□S	
ATBP	J19	U	PITCH ANALOG TELEMETRY BUFFER
ATBR	J19	□I	ROLL ANALOG TELEMETRY BUFFER
ATBSHD	J19	□Q	ANALOG TELEMETRY BUFFER SHIELD
ATBS1	J19	N	ANALOG TELEMETRY BUFFER, SPARE 1
ATBS2	J19	□E	ANALOG TELEMETRY BUFFER, SPARE 2
ATBY	J19	S	YAEV ANALOG TELEMETRY BUFFER
N03TLM	J19	□A	-3 VOLT ANALOG TEL SIG
N20TLM	J19	E	-20 VOLT ANALOG TEL SIG
P06TLM	J19	□C	6 VOLT ANALOG TEL SIG
P12TLM	J19	□N	12 VOLT ANALOG TEL SIG
P20TLM	J19	F	20 VOLT ANALOG TEL SIG
P6STLM	J19	□B	6 VOLT ANALOG TEL SIG
TELREF1	J19	T	TELEMETRY REFERENCE 1
TELREF2	J19	□H	TELEMETRY REFERENCE 2
TELREF3	J19	H	TELEMETRY REFERENCE 3
TELREF4	J19	□F	TELEMETRY REFERENCE 4
TELREF5	J19	M	TELEMETRY REFERENCE 5
THERM1	J19	A	LOGIC PAGE THERMISTOR 1
THERM2	J19	B	LOGIC PAGE THERMISTOR 2
THERM3	J19	C	MEMORY SECTION THERMISTOR 3
THERM4	J19	D	MEMORY SECTION THERMISTOR 4
THERM1D	J19	W	THERMISTOR 1D
THERM2D	J19	X	THERMISTOR 2D
THERM3D	J19	Y	THERMISTOR 3D
THERM4D	J19	Z	THERMISTOR 4D
THERSHD	J19	□M	SHIELD
TLMGRD	J19	G	TELEMETRY RETURN
TLMSHD	J19	□M	SHIELD
	J19	□T	FRAME
	J19	J	
	J19	K	
	J19	L	
	J19	P	
	J19	R	
	J19	V	
	J19	□D	
	J19	□G	
	J19	□J	
	J19	□K	
	J19	□P	
	J19	□R	
	J19	□S	
SR48	J20	H	SIGNAL RETURN 48
SR49	J20	N	SIGNAL RETURN 49
SR50	J20	P	SIGNAL RETURN 50

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 18)

NAME	CONNECTOR	PIN	FUNCTION
SR51	J20	R	SIGNAL RETURN 51
SR52	J20	□C	SIGNAL RETURN 52
SR53	J20	□D	SIGNAL RETURN 53
SR54	J20	□E	SIGNAL RETURN 54
SR55	J20	□F	SIGNAL RETURN 55
SR56	J20	□G	SIGNAL RETURN 56
SR57	J20	J	SIGNAL RETURN 57
SR58	J20	□H	SIGNAL RETURN 58
SR59	J20	□I	SIGNAL RETURN 59
SR60	J20	□J	SIGNAL RETURN 60
SR61	J20	□K	SIGNAL RETURN 61
SR62	J20	□M	SIGNAL RETURN 62
SR63	J20	□U	SIGNAL RETURN 63
SR64	J20	□V	SIGNAL RETURN 64
SR65	J20	□W	SIGNAL RETURN 65
SR66	J20	□X	SIGNAL RETURN 66
SR67	J20	□Y	SIGNAL RETURN 67
SR68	J20	EE	SIGNAL RETURN 68
SR69	J20	FF	SIGNAL RETURN 69
SR70	J20	GG	SIGNAL RETURN 70
SR71	J20	HH	SIGNAL RETURN 71
V1 01	J20	A	PLUS 6 VDC 01
V1 02	J20	B	PLUS 6 VDC 02
V1 03	J20	C	PLUS 6 VDC 03
V1 04	J20	D	PLUS 6 VDC 04
V1 05	J20	E	PLUS 6 VDC 05
V1 06	J20	F	PLUS 6 VDC 06
V1 07	J20	T	PLUS 6 VDC 07
V1 08	J20	U	PLUS 6 VDC 08
V1 09	J20	V	PLUS 6 VDC 09
V1 10	J20	W	PLUS 6 VDC 10
V1 11	J20	X	PLUS 6 VDC 11
V1 12	J20	Y	PLUS 6 VDC 12
V1 13	J20	Z	PLUS 6 VDC 13
V1 14	J20	□A	PLUS 6 VDC 14
V1 15	J20	S	PLUS 6 VDC 15
V1 16	J20	□N	PLUS 6 VDC 16
V1 17	J20	□P	PLUS 6 VDC 17
V1 18	J20	□Q	PLUS 6 VDC 18
V1 19	J20	□R	PLUS 6 VDC 19
V1 20	J20	□S	PLUS 6 VDC 20
V1 21	J20	□Z	PLUS 6 VDC 21
V1 22	J20	AA	PLUS 6 VDC 22
V1 23	J20	BB	PLUS 6 VDC 23
V1 24	J20	CC	PLUS 6 VDC 24
	J20	G	
	J20	K	
	J20	L	
	J20	M	
	J20	□B	
	J20	□T	
	J20	DD	
*A1A1V	J21	T	OPERAND ADD 1, CH 1
*A2A1V	J21	□M	OPERAND ADD 1, CH 2

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 19)

NAME	CONNECTOR	PIN	FUNCTION
*A3A1V	J21	□P	OPERAND ADD 1, CH 3
*A1A2V	J21	DD	OPERAND ADD 2 CH 1
*A2A2V	J21	BB	OPERAND ADD 2 CH 2
*A3A2V	J21	AA	OPERAND ADD 2 CH 3
*A1A3V	J21	□N	OPERAND ADD 3, CH 1
*A2A3V	J21	CC	OPERAND ADD 3 CH 2
*A3A3V	J21	□Q	OPERAND ADD 3, CH 3
*A1A4V	J21	FF	OPERAND ADD 4 CH 1
*A2A4V	J21	GG	OPERAND ADD 4 CH 2
*A3A4V	J21	□Z	OPERAND ADD 4, CH 2
*A1A5V	J21	R	OPERAND ADD 5, CH 1
*A2A5V	J21	□W	OPERAND ADD 5, CH 2
*A3A5V	J21	□J	OPERAND ADD 5, CH 3
*A1A6V	J21	□V	OPERAND ADD 6, CH 1
*A2A6V	J21	□Y	OPERAND ADD 6, CH 1
*A3A6V	J21	□K	OPERAND ADD 6, CH 3
*A1A7V	J21	A	OPERAND ADD 7, CH 1
*A2A7V	J21	X	OPERAND ADD 7, CH 2
*A3A7V	J21	□R	OPERAND ADD 7, CH 3
*A1A8V	J21	EE	OPERAND ADD 8 CH 1
*A2A8V	J21	HH	OPERAND ADD 8 CH 2
*A3A8V	J21	S	OPERAND ADD 8, CH 3
*A1A9V	J21	Y	OPERAND ADD 9, CH 1
*A2A9V	J21	C	OPERAND ADD 9, CH 2
*A3A9V	J21	W	OPERAND ADD 9, CH 1
*A1TRSV	J21	F	TRANSFER REG CH 1
*A2TRSV	J21	E	TRANSFER REG CH 2
*A3TRSV	J21	D	TRANSFER REG CH 3
SR86	J21	V	SIGNAL RETURN 86
SR87	J21	Z	SIGNAL RETURN 87
SR88	J21	□I	SIGNAL RETURN 88
	J21	B	SPARE
	J21	G	
	J21	H	
	J21	J	
	J21	K	
	J21	L	
	J21	M	
	J21	N	
	J21	P	
	J21	U	
	J21	□A	
	J21	□B	
	J21	□C	
	J21	□D	
	J21	□E	
	J21	□F	
	J21	□G	
	J21	□H	
	J21	□S	
	J21	□T	
	J21	□U	
	J21	□X	

* INDICATES INPUT □ INDICATES LOWER CASE

Figure 3-2. List of Interface Signals (Sheet 20)

SECTION IV

TEST EQUIPMENT AND SPECIAL TOOLS

4-1. SCOPE.

4-2. This section lists the test equipment and special tools required for laboratory maintenance of the data adapter.

4-3. TEST EQUIPMENT.

4-4. STANDARD TEST EQUIPMENT.

4-5. The standard test equipment recommended for maintenance of the LVDA is listed in figure 4-1.

Name	Model or Type	Manufacturer
Oscilloscope	Model 585A	Tektronix, Inc.
Oscilloscope Plug-In Unit Adapter	Model M	Tektronix, Inc.
Preamplifier Adapter	Model 81	Tektronix, Inc.
Differential Voltmeter	Model 803B	John Fluke Mfg. Co., Inc.
Multimeter	Model 630A	Triplett Electrical Instrument Co.
Resistivity Meter	Distilled Water Purity Meter with B-1 Glass Dip Cell Model PM-4	Barnstead Still and Sterilizer Co.
pH Meter	Hydrogen Ion Meter Model 72	Beckman Instruments Inc.
Hydrometer	Hydrometer Cat. No. 11-530	Fisher Scientific Co.
Hydrometer Cylinder	Hydrometer Cylinder Cat. No. 8-530	Fisher Scientific Co.
Coolant Contamination Sampler	Bob Sampling Kit Cat. No. XX6403700	Millipore Filter Corp.
Collection Screen and Holder (water only)	Monitor Cat. No. MABG037P0	Millipore Filter Corp.
Collection Screen (methanol)	Filter with grid, 37mm, White Cat. No. 0HWG037P0	Millipore Filter Corp.
Collection Screen Holder (methanol)	Refillable Stainless Monitor Case Cat. No. M000037P0	Millipore Filter Corp.

Figure 4-1. Standard Test Equipment

4-6. SPECIAL TEST EQUIPMENT.

4-7. The special test equipment required for maintenance of the LVDA is listed in figure 4-2.

Name	Figure No.	Part No.	Used for:
Aerospace Data Adapter Programmable Tester (ADAPT)	4-4	6900500	All models
Aerospace Saturn Test and Evaluation Console (ASTEC)	4-5	6940000	All models
LVDA Functional Test Program Tape	(not shown)	6001240	Breadboard I and II
LVDA Detail Measurement Program Tape I	(not shown)	6001246	Breadboard I and II
LVDA Detail Measurement Program Tape II	(not shown)	6001242	Breadboard I and II
LVDA Crossover Detector Calibration Program Tape	(not shown)	6001244	Breadboard I and II
Data Adapter Load Simulator	(not shown)	6942100	All models

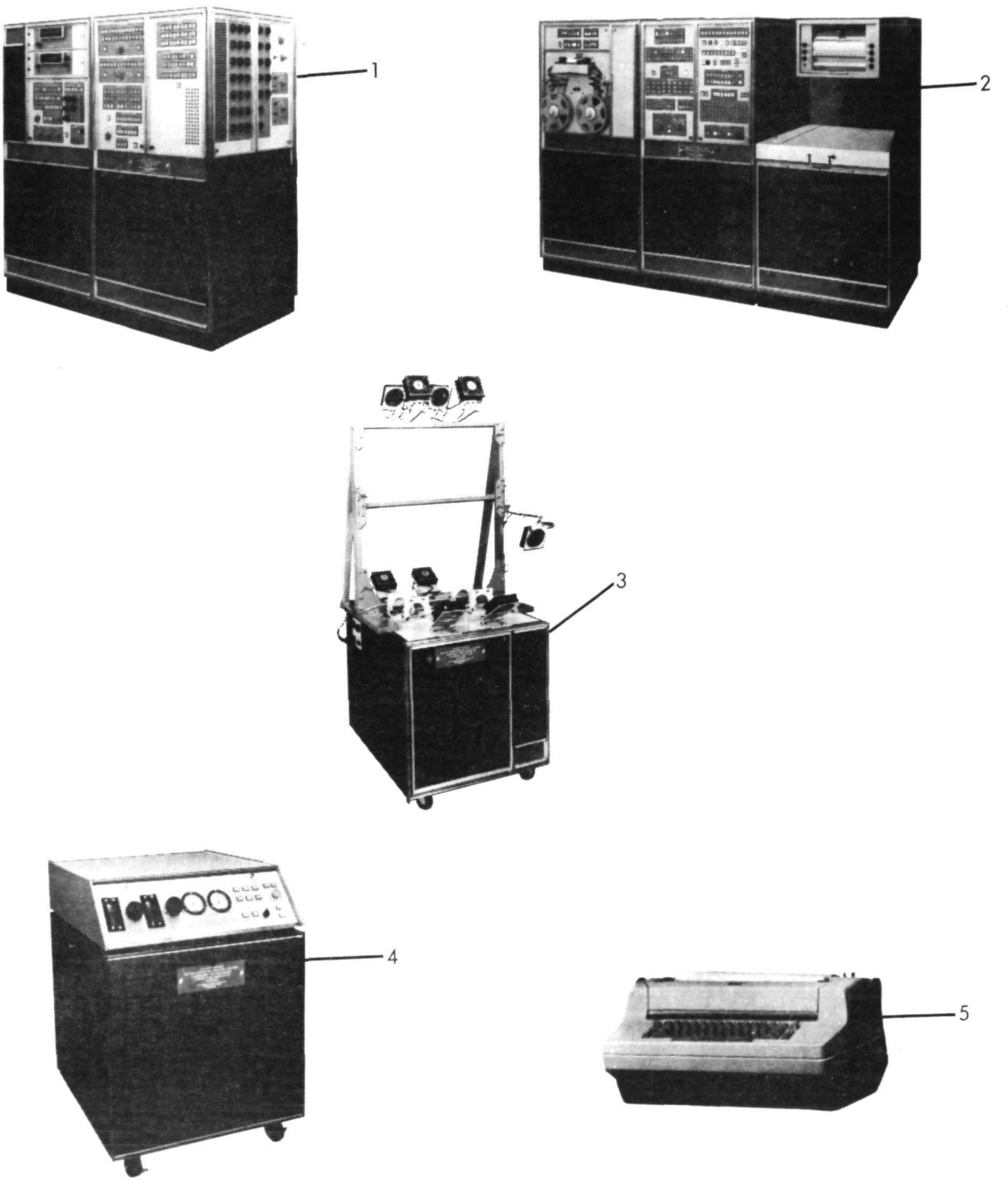
Figure 4-2. Special Test Equipment

4-8. SPECIAL TOOLS.

4-9. The special tools recommended for maintenance of the LVDA are listed in figure 4-3.

Name	Figure and Index No.	Part No.	Function
Insert-Extract Tool	4-6(1)	657922	Inserts and removes pages.
Test Point Adapter Probe	4-6(2)	6139524	Attaches to ordinary probes and fits into receptacles on the test point adapters.
2-Sided Test Point Adapter	4-6(3)	6139525	Provides access to test points on ULD-type pages from top of page.
1-Sided Test Point Adapter	4-6(4)	6139526	Provides access to test points on non-ULD type pages from top of page.
Torque Tool Kit	4-6(5)	658041	Tightens and measures torque of fastening screws.
Purging Cart	4-6(6)	657900	Fills and purges coolant.
Transport Dolly	4-6(7)	656360	Lifts and transports LVDA. Used for removing LVDA from shipping container, etc.

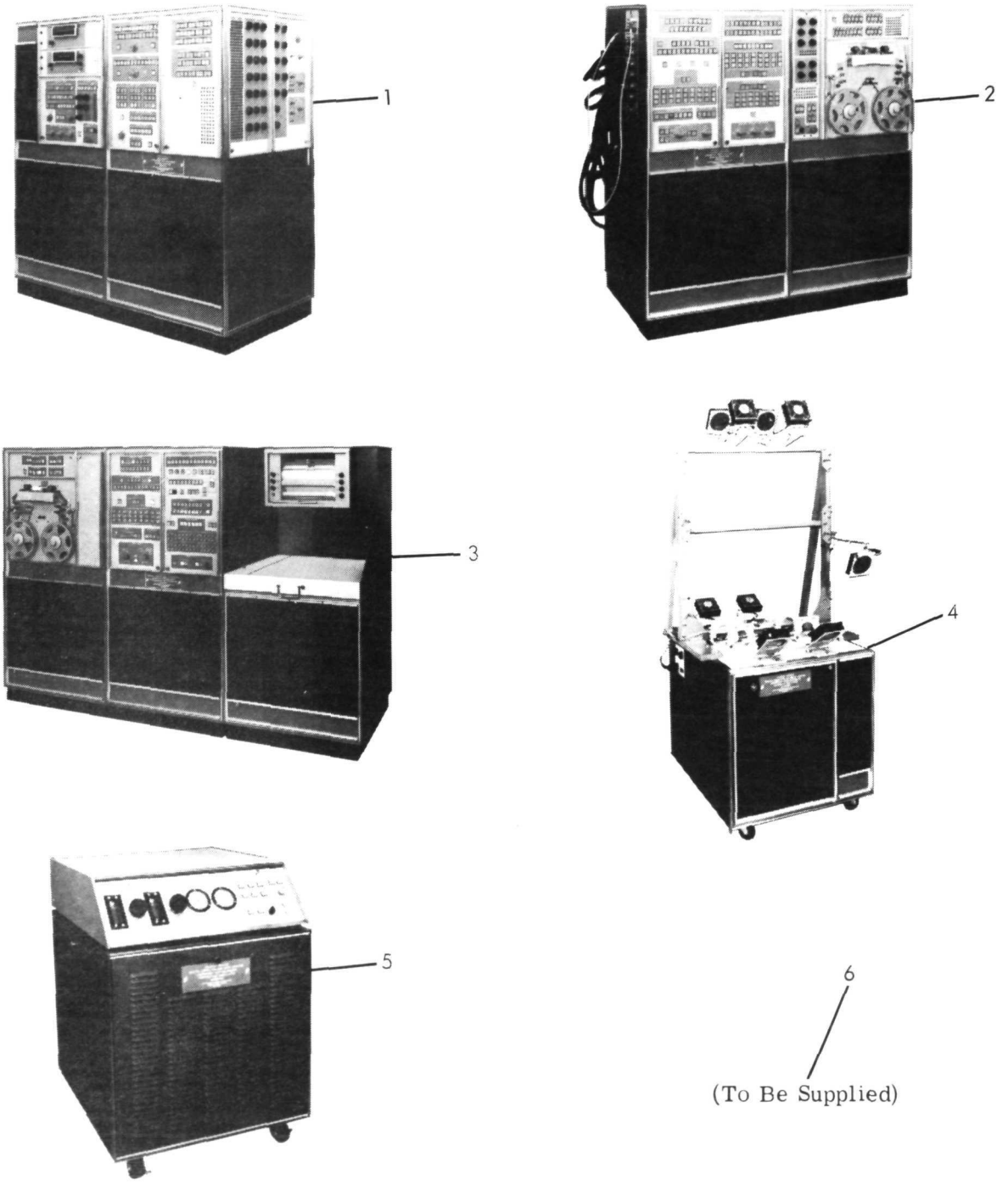
Figure 4-3. Special Tools



LEGEND

1 LVDAME	4 TEMPERATURE MODULATOR
2 PTC	5 INPUT/OUTPUT PRINTER
3 TEST STAND	

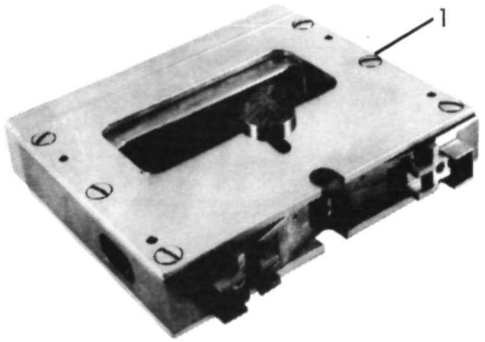
Figure 4-4. Aerospace Data Adapter Processor Tester



LEGEND

1 LVDAME	4 TEST STAND
2 LVDCME	5 TEMPERATURE MODULATOR
3 PTC	6 PRINTER

Figure 4-5. Aerospace Saturn Test and Evaluation Console (ASTEC)



2

(To Be Supplied)

3

(To Be Supplied)

4

(To Be Supplied)

5

(To Be Supplied)

6

(To Be Supplied)

7

(To Be Supplied)

LEGEND

1 INSERT-EXTRACT TOOL
2 TP ADAPTER PROBE
3 2-SIDED TP ADAPTER
4 1-SIDED TP ADAPTER
5 TORQUE TOOL KIT
6 PURGING CART
7 TRANSPORT DOLLY

Figure 4-6. Special Tools

SECTION V

PREPARATION FOR USE, STORAGE AND SHIPMENT

5-1. PREPARATION FOR USE.

5-2. UNPACKING. The data adapter is shipped in a reusable shipping container, IBM part number 6019802 (figure 5-1). Included in the shipping container is a shock recorder, IBM part number 6019637. The data adapter is removed from its shipping container as follows:

a. Turn pressure equalizing screw on shipping container two turns counterclockwise.

b. Unlatch and remove container cover.

c. Remove the four mounting bolts which secure the data adapter to the container frame.

NOTE

The following steps require the use of the Transport Dolly. (See section IV.)

d. Attach lift frame to Transport Dolly lift head.

e. Operate trunnion crank so that lift head is horizontal.

f. Crank lift head high enough to clear shipping container.

g. Maneuver Transport Dolly over shipping container so that lift frame is aligned with LVDA.

h. Crank lift head down so that lift frame surrounds LVDA.

i. Adjust lift pin knobs so that lift pins engage LVDA lift holes.

j. Lock lift pin knobs.

k. Crank to lift LVDA clear of shipping container.

l. Roll Transport Dolly clear of shipping container.

m. Reinstall the mounting bolts in the shipping container for safekeeping.

n. Remove the four socket head screws which secure the shock recorder to its bracket in the shipping container.

o. Detach and open the shock recorder. Remove the spool that contains the recorded portion of the chart paper (figure 5-2).

(To be supplied.)

Figure 5-1. Reusable Shipping Container.

CAUTION

When removing chart paper, handle chart paper carefully. Cut (do not tear) the chart paper to detach recorded portion. The paper is pressure sensitive, and data may be obliterated by rough or excessive handling.

p. Cut the chart paper, remove it from the spool, and replace the spool in the recorder.

NOTE

The clock mechanism will operate until its spring mechanism has run down. To prevent waste of chart paper if the recorder is not to be used immediately, do not rethread the roll chart, but instead, tape the loose end of the chart to the writing plate. In addition to saving the paper, this will protect the styluses which would otherwise rest on the hard surface of the plate.

q. Rethread the chart paper onto the takeup spool (figure 5-3), or tape the paper to the writing plate.

r. Close and latch the shock recorder.

s. Reinstall the shock recorder (handle side up) in the shipping container.

t. On a blank portion of the removed section of chart paper, record the

Government Bill of Lading Number

Receiving Location and Receiver Individuals Signature

Unit Name, Part Number and Serial Number

Container Serial Number and Recorder Serial Number

Date and Local Time Recorder was opened

u. Ship removed section of chart with added data to the following address:

Saturn Programs Office, Department 839
IBM Space Guidance Center
Owego, New York, 13827

v. Use vacuum cleaner to clean interior of container if foreign material or debris is in the shipping container.

w. Replace and latch cover on shipping container and store container for reuse.

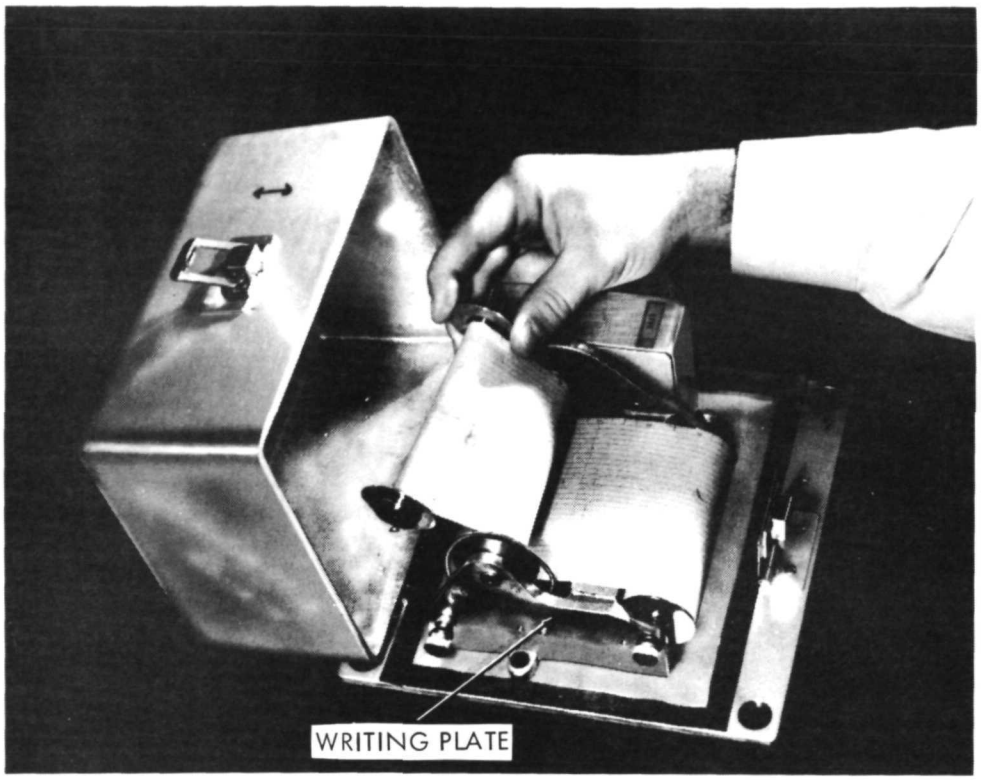
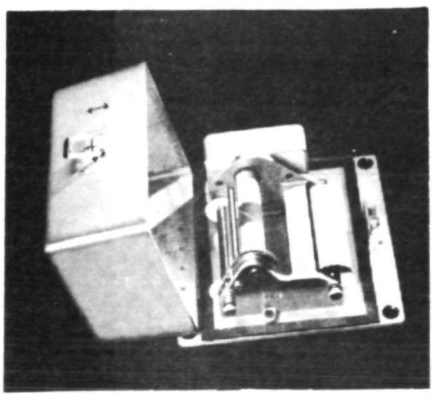
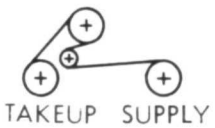


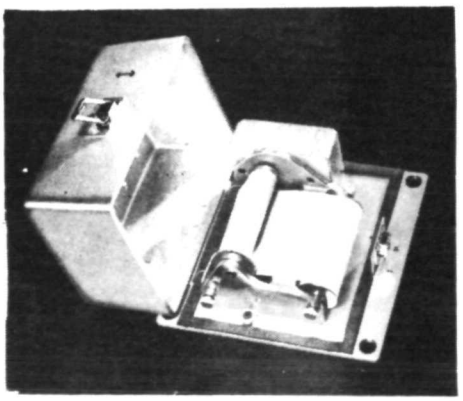
Figure 5-2. Removing Roll Chart From Shock Recorder.



(A) ROLL CHART PARTIALLY INSTALLED



(B) FEED DIAGRAM



(C) ROLL CHART COMPLETELY INSTALLED

Figure 5-3. Installing Roll Chart in Shock Recorder

5-3. INSPECTION AND TEST. After the data adapter has been unpacked, proceed as follows:

a. Examine the exterior of the data adapter for mechanical damage, noting especially any evidence of impact or other severe mechanical stress. Check for loose screws and broken or missing connector dust covers. If extensive abnormalities are noted, remove covers and inspect interior of the data adapter. (See section IX.)

b. Remove and store connector dust covers.

c. Fill the data adapter with distilled water as indicated in figure 5-4.

d. Perform an electrical checkout of the data adapter. (See Technical Manual, Check-out Procedures for Saturn LVDC and LVDA).

e. Purge the data adapter of coolant as indicated in figure 5-6. If required, fill with 60-40 coolant indicated in figure 5-5.

5-4. PREPARATION FOR STORAGE.

5-5. The data adapter is stored in the reusable container in which it was shipped. To prepare the data adapter for storage, proceed as follows:

a. Purge the data adapter of coolant as indicated in figure 5-6.

b. Disconnect all cables and ground straps from the data adapter.

c. Completely assemble the data adapter, including covers. Tighten all screws to the proper torque. (See section IX.)

d. Install dust covers on the data adapter connector jacks. Part numbers and location of dust covers are as follows:

IBM Part No.	Vendor Part No.	Quantity	Used On
6014453	MS25177-22	5	J2, J7, J17, J18, J19
6036037	MS25178-22	16	All other connectors.

NOTE

The following steps require the use of the Transport Dolly. (See section IV.)

e. Attach lift frame to Transport Dolly lift head.

f. Operate trunnion crank so that lift head is vertical.

g. Crank lift head so that lift frame is level with the data adapter on the test stand.

h. Detach logic support handles from the data adapter. Stow the support handles and mounting screws in the places provided on the Test Stand.

i. On the Test Stand, extract the hinge pivot pins.

j. Remove the pivot locking screws and washers, and swing each hinge block down to the table top.

k. Remove the hinge halves from the data adapter logic sections; then fasten the hinge halves to the hinge blocks with the pivot pins, and stow the mounting screws in the place provided on the Test Stand.

l. Lock casters on test stand. Remove mounting screws from the data adapter and have someone hold the data adapter so that it can not slide off its locating pins.

m. Maneuver Transport Dolly toward test stand until lift frame surrounds the data adapter.

n. Adjust lift pin knobs so that lift pins engage data adapter lift holes.

o. Lock lift pin knobs.

p. Pull Transport Dolly and data adapter away from test stand.

q. Unlatch and remove shipping container cover.

r. Verify that there is no foreign material or debris in the shipping container. Use vacuum cleaner, if necessary, to completely clean interior of container.

s. Detach data adapter mounting bolts from shipping container.

t. Operate trunnion crank so that lift head is vertical.

u. Maneuver Transport Dolly over shipping container so that data adapter is properly aligned with its container mounting pads.

v. Crank data adapter down onto its mounting pads in the container.

w. Install and tighten the data adapter mounting bolts. The recommended torque for these bolts is 250 inch-pounds maximum.

x. Recheck shipping container for dirt and debris, and clean if necessary.

y. Install and latch container cover.

z. Turn pressure equalizer screw fully clockwise.

NOTE

During storage, the container humidity indicator should be checked at least once a week (more often if high humidity conditions prevail). If the "40" sector of the humidity indicator turns pink, the container desiccant should be replaced.

5-6. REPLACING DESICCANT.

5-7. The shipping container uses desiccant packaged in bags according to military specification MIL-D-3464. The amount of desiccant in each bag is called unit content, and is printed on the bag.

5-8. The shipping container requires 17 units of desiccant. It is recommended that these 17 units be supplied in the form of two 8-unit bags and one 1-unit bag. Desiccant bags which have been replaced may be reactivated by heating according to directions printed on the bag. IBM part numbers for the recommended desiccant bags are:

6019623, 8-unit bag
6019653, 1-unit bag

5-9. PREPARATION FOR SHIPMENT.

5-10. The data adapter is prepared for shipment as follows:

a. Unlatch and remove container cover.

b. Detach and remove shock recorder.

c. Open the shock recorder and check for damage. Check especially for loose mounting screws.

d. Rethread chart paper as shown in figure 5-3.

e. Close cover and strike recorder sharply against floor. Open cover and verify that all three styluses have made a discernable impression on the chart paper.

f. Write the following data on the chart paper:

Sending Location and Sender's Initials
Date and Local Time

NOTE

The chart paper is calibrated in hours A. M. and P. M., but it is not necessary to align the paper with local time. Simply write the local time at the point where the recorder was started.

g. Wind the shock recorder and observe long enough to verify that the paper is moving and that all three styluses are tracking.

h. Close and latch the shock recorder, but DO NOT LOCK.

i. Install the shock recorder (handle side up) in the shipping container.

j. Proceed in the same manner as though preparing for storage.

Step	Operation	Normal Indication
	NOTE This procedure requires the use of the Purging Cart, IBM Tool number 657900. If a normal indication cannot be obtained as specified in this procedure, refer to the technical manual, Laboratory Maintenance Instructions, Purging Cart, IBM Tool number 657900.	
	CAUTION Unless data adapter cooling system is known to be empty, perform purging procedure, figure 5-6.	
1.	Observe the WATER level indicator on the back of the purging cart.	WATER level is on or between OPERATING RANGE marks.
2.	Check MOISTURE INDICATOR.	MOISTURE INDICATOR is blue (not pink).
3.	Make sure FILL WATER and FILL 60-40 valves are off (fully clockwise).	
4.	Connect an 80(±20) psi compressed air source to the adapter hose assembly provided with the cart. Connect adapter hose assembly to AIR coupling.	
5.	Connect power cable to 115 VAC, 60 cps, single-phase power source.	MAIN POWER OFF lamp is lit.
6.	Press LAMP TEST switch.	All lamps are lit except MAIN POWER ON.

Figure 5-4. Water Filling Procedure. (Sheet 1 of 4)

Step	Operation	Normal Indication
7.	Operate the following switches so that their lamps are off: VACUUM PUMP DE-AIR SYSTEM FILL WATER PURGE WATER FILL 60/40 PURGE 60/40	
8.	Press MAIN POWER ON switch.	MAIN POWER ON lamp is lit.
9.	Adjust LOW PRESSURE REGULATOR control so that LOW PRESSURE gage indicates 5 psi.	
10.	Press FILL WATER switch.	FILL WATER lamp is lit.
11.	Connect fluid sampling adapter provided with cart to the DISTILLED WATER OUTLET coupling.	
12.	Hold a perfectly clean beaker under the fluid sampling adapter and draw off about a quarter-pint (120 ml) of coolant by opening and closing FILL WATER valve.	
13.	Using a resistivity meter and a pH meter (see section IV), measure the resistivity and the pH of the coolant sample.	Resistivity ≥ 100,000 ohm-cm. pH = 7(±1)
14.	Connect a coolant contaminant sampler to the fluid sampling adapter. Fill the sampler by opening and closing the FILL WATER valve.	
15.	Press FILL WATER switch.	FILL WATER lamp is not lit.
	WARNING Look away from coupling or wear safety glasses when detaching fluid sampling adapter. In case of valve failure, coolant may be deflected into eyes.	

Figure 5-4. Water Filling Procedure. (Sheet 2)

Step	Operation	Normal Indication
16.	Remove fluid sampling adapter (with coolant contaminant sampler attached) from DISTILLED WATER OUTLET coupling. Disassemble coolant contaminant sampler, remove collection screen and holder and examine screen under 300X microscope.	Maximum partical size in any dimension shall be no greater than 175 microns.
17.	Using hose assemblies provided with cart, connect DISTILLED WATER OUTLET coupling to data adapter INLET coupling; connect LIQUID RETURN coupling to data adapter OUTLET coupling.	
18.	Press VACUUM PUMP switch.	VACUUM PUMP lamp is lit.
19.	Press DE-AIR SYSTEM switch.	DE-AIR SYSTEM lamp is lit. VACUUM CONTROLLER gage indicates 5(+0, -1) mm Hg within 3 minutes.
20.	Five minutes after VACUUM CONTROLLER gage reaches 5(+0, -1) mm Hg, press DE-AIR SYSTEM switch.	DE-AIR SYSTEM lamp is not lit.
21.	Press VACUUM PUMP switch.	VACUUM PUMP lamp is not lit.
22.	Press FILL WATER switch.	FILL WATER lamp is lit.
23.	Observe FILL MONITOR window. Open FILL WATER valve until liquid is visible through FILL MONITOR window; then close FILL WATER valve.	
	WARNING Look away from couplings or wear safety glasses when detaching hose assemblies. In case of valve failure, coolant may be deflected into eyes.	

Figure 5-4. Water Filling Procedure. (Sheet 3)

Step	Operation	Normal Indication
24.	Remove hose assemblies from data adapter and purging cart. Cover ends of hose assemblies with dust caps provided.	
25.	Cover purging cart coupling adapters with dust caps provided.	
26.	Cover data adapter coolant fittings with dust caps provided.	
27.	Press FILL WATER switch.	FILL WATER lamp is not lit.
28.	Press MAIN POWER OFF switch.	MAIN POWER OFF lamp is lit.
29.	If purging cart is not to be used within a reasonable length of time, disconnect compressed air source and power cable.	
	CAUTION Always disconnect power cable before disconnecting compressed air source. Air source prevents buildup of combustible vapors in switch housing.	

Figure 5-4. Water Filling Procedure. (Sheet 4)

Step	Operation	Normal Operation
	NOTE This procedure requires the use of the Purging Cart, IBM Tool number 657900. If a normal indication cannot be obtained as specified in this procedure, refer to the technical manual, Laboratory Maintenance Instructions, Purging Cart, IBM Tool number 657900. CAUTION Unless data adapter cooling system is known to be empty, perform purging procedure, figure 5-6.	
1.	Observe the 60-40 level indicator on the back of the purging cart.	60-40 level is on or between OPERATING RANGE marks.
2.	Check MOISTURE INDICATOR.	MOISTURE INDICATOR is blue (not pink).
3.	Make sure FILL WATER and FILL 60-40 valves are off (fully clockwise).	
4.	Connect an 80(±20) psi compressed air source to the adapter hose assembly provided with the cart. Connect adapter hose assembly to AIR coupling.	
5.	Connect power cable to 115 VAC, 60 cps, single-phase power source.	MAIN POWER OFF lamp is lit.
6.	Press LAMP TEST switch.	All lamps are lit except MAIN POWER ON.

Figure 5-5. 60-40 Filling Procedure. (Sheet 1 of 4)

Step	Operation	Normal Indication
7.	Operate the following switches so that their lamps are off: VACUUM PUMP DE-AIR SYSTEM FILL WATER PURGE WATER FILL 60/40 PURGE 60/40	
8.	Press MAIN POWER ON switch.	MAIN POWER ON lamp is lit.
9.	Adjust LOW PRESSURE REGULATOR control so that LOW PRESSURE gage indicates 5 psi.	
10.	Press FILL 60/40 switch.	FILL 60/40 lamp is lit.
11.	Connect fluid sampling adapter provided with cart to the 60-40 OUTLET coupling.	
12.	Hold a perfectly clean beaker under the fluid sampling adapter and draw off about a quarter-pint (120 ml) of coolant by opening and closing FILL 60-40 valve.	
13.	Using a resistivity meter and a pH meter (see section IV), measure the resistivity and the pH of the coolant sample.	Resistivity $\geq$ 100,000 ohm-cm. pH = 7(±1).
14.	Connect a coolant contaminant sampler to the fluid sampling adapter. Fill the sampler by opening and closing the FILL 60-40 valve.	
15.	Press FILL 60/40 switch.	FILL 60/40 lamp is not lit.
	WARNING Look away from coupling or wear safety glasses when detaching fluid sampling adapter. In case of valve failure, coolant may be deflected into eyes.	

Figure 5-5. 60-40 Filling Procedure. (Sheet 2)

Step	Operation	Normal Indication
16.	Remove fluid sampling adapter (with coolant contaminant sampler attached) from 60-40 OUTLET coupling. Disassemble coolant contaminant sampler, remove collection screen and holder and examine screen under 300X microscope.	Maximum particle size in any dimension shall be no greater than 175 microns.
17.	Using hose assemblies provided with cart, connect 60-40 OUTLET coupling to data adapter INLET coupling; connect LIQUID RETURN coupling to data adapter OUTLET coupling.	
18.	Press VACUUM PUMP switch.	VACUUM PUMP lamp is lit.
19.	Press DE-AIR SYSTEM switch.	DE-AIR SYSTEM lamp is lit. VACUUM CONTROLLER gage indicates 5(+0, -1) mm Hg within 3 minutes.
20.	Five minutes after VACUUM CONTROLLER gage reaches 5(+0, -1) mm Hg, press DE-AIR SYSTEM switch.	DE-AIR SYSTEM lamp is not lit.
21.	Press VACUUM PUMP switch.	VACUUM PUMP lamp is not lit.
22.	Press FILL 60/40 switch.	FILL 60/40 lamp is lit.
23.	Observe FILL MONITOR window. Open FILL 60-40 valve until liquid is visible through FILL MONITOR window; then close FILL 60-40 valve.	
	WARNING Look away from couplings or wear safety glasses when detaching hose assemblies. In case of valve failure, coolant may be deflected into eyes.	

Figure 5-5. 60-40 Filling Procedure. (Sheet 3)

Step	Operation	Normal Indication
24.	Remove hose assemblies from data adapter and purging cart. Cover ends of hose assemblies with dust caps provided.	
25.	Cover purging cart coupling adapters with dust caps provided.	
26.	Cover data adapter coolant fittings with dust caps provided.	
27.	Press FILL 60/40 switch.	FILL 60/40 lamp is not lit.
28.	Press MAIN POWER OFF switch.	MAIN POWER OFF lamp is lit.
29.	If purging cart is not to be used within a reasonable length of time, disconnect compressed air source and power cable.	
	CAUTION Always disconnect power cable before disconnecting compressed air source. Air source prevents buildup of combustible vapors in switch housing.	

Figure 5-5. 60-40 Filling Procedure. (Sheet 4)

Step	Operation	Normal Operation
	NOTE This procedure requires the use of the Purging Cart, IBM Tool number 657900. If a normal indication cannot be obtained as specified in this procedure, refer to the technical manual, Laboratory Maintenance Instructions, Purging Cart, IBM Tool number 657900.	
1.	Observe the WATER level indicator on the back of the service cart.	WATER level is on or below FULL mark.
2.	Check MOISTURE INDICATOR.	MOISTURE INDICATOR is blue (not pink).
3.	Make sure FILL WATER and FILL 60-40 valves are off (fully clockwise).	
4.	Connect an 80(±20) psi compressed air source to the adapter hose assembly provided with the cart. Connect adapter hose assembly to AIR coupling.	
5.	Connect power cable to 115 VAC, 60 cps, single-phase power source.	MAIN POWER OFF lamp is lit.
6.	Press LAMP TEST switch.	All lamps are lit except MAIN POWER ON.
7.	Operate the following switches so that their lamps are off: VACUUM PUMP DE-AIR SYSTEM FILL WATER FILL 60/40 PURGE WATER PURGE 60/40	
8.	Press MAIN POWER ON switch.	MAIN POWER ON lamp is lit.

Figure 5-6. Purging Procedure. (Sheet 1 of 4)

Step	Operation	Normal Indication
9.	Adjust HIGH PRESSURE REGULATOR control so that HIGH PRESSURE gage indicates 5 psi.	
10.	Using hose assemblies provided with cart, connect DISTILLED WATER OUTLET coupling to data adapter INLET coupling; connect remaining hose assembly to data adapter OUTLET coupling.	
11.	Remove sampling screen and holder from coolant contaminant sampler and attach 850 ml. bottle to sampler. (See section IV.) Attach fluid sampling adapter provided with cart to coolant contaminant sampler and couple entire assembly to hose from data adapter OUTLET coupling.	
12.	Press PURGE WATER switch.	PURGE WATER lamp is lit. Coolant flows into coolant contaminant sampler.
13.	When coolant stops flowing, press PURGE WATER switch.	PURGE WATER lamp is not lit.
14.	Detach fluid sampling adapter and coolant contaminant sampler from hose assembly. Using hydrometer, measure specific gravity of coolant.	If coolant is 60-40 mixture of methanol and water, specific gravity will be 0.895(±.010) at 20° C. If coolant is distilled water, specific gravity will be 1.00 (±.005) at 20° C. NOTE Specific gravity readings outside the limits specified may indicate severe contamination. If S.G. readings are out of limits, tag the data adapter and save the coolant for factory analysis. Otherwise, discard coolant.

Figure 5-6. Purging Procedure. (Sheet 2)

Step	Operation	Normal Indication
15.	Adjust HIGH PRESSURE REGULATOR control so that HIGH PRESSURE gage indicates 30 psi. If coolant is distilled water, proceed to step 16. If coolant is 60-40 mixture, proceed to step 19.	
16.	Connect hose from data adapter OUTLET coupling to LIQUID RETURN coupling.	
17.	Press PURGE WATER switch.	PURGE WATER lamp is lit.
18.	Wait 5 minutes, the press PURGE WATER switch again. Proceed to step 22.	PURGE WATER lamp is not lit.
19.	Remove hose from DISTILLED WATER OUTLET coupling and connect to 60-40 OUTLET coupling. Connect hose from data adapter OUTLET coupling to LIQUID RETURN coupling.	
20.	Press PURGE 60-40 switch.	PURGE 60-40 lamp is lit.
21.	Wait 5 minutes, then press PURGE 60-40 switch again.	PURGE 60-40 lamp is not lit.
22.	Press DE-AIR SYSTEM switch.	DE-AIR SYSTEM lamp is lit.
23.	Press VACUUM PUMP switch.	VACUUM PUMP lamp is lit. VACUUM CONTROLLER gage indicates 5(-0, -1) mm Hg within 3 minutes.
24.	Five minutes after VACUUM CONTROLLER gage reaches 5(-0, -1) mm Hg, press DE-AIR SYSTEM switch.	DE-AIR SYSTEM lamp is not lit.
25.	Press VACUUM PUMP switch.	VACUUM PUMP lamp is not lit.
26.	Remove hose assemblies from data adapter and purging cart. Cover ends of hose assemblies with dust caps provided.	

Figure 5-6. Purging Procedure. (Sheet 3)

Step	Operation	Normal Indication
26. (cont)	If new coolant is to be loaded, proceed as directed in figure 5-4 or 5-5 (as appropriate), starting with step 9. Otherwise, continue with remainder of this procedure.	
27.	Cover purging cart coupling adapters with dust caps provided.	
28.	Cover data adapter coolant fittings with dust caps provided.	
29.	Press MAIN POWER OFF switch.	MAIN POWER OFF lamp is lit. 60-40 lamp is lit.
30.	If purging cart is not to be used within a reasonable length of time, disconnect compressed air source and power cable.	
	CAUTION Always disconnect power cable before disconnecting compressed air source. Air source prevents buildup of combustible vapors in switch housing.	

Figure 5-6. Purging Procedure. (Sheet 4)

SECTION VI

PREVENTIVE MAINTENANCE

6-1. INSPECTION.

6-2. The data adapter should be inspected daily for external evidence of physical damage. Data adapters in storage should have their container humidity indicators checked at least once a week (more often under high-humidity conditions). If the "40" sector of the humidity indicator turns pink, the container desiccant should be replaced. (See "Replacing Desiccant", section V.)

6-3. PERIODIC MAINTENANCE.

6-4. No periodic maintenance is required for the data adapter.

SECTION VII

CHECKOUT

7-1. Checkout of the data adapter is accomplished by the Aerospace Data Adapter Processor Tester or the Aerospace Saturn Test and Evaluation Console. (See section IV.)

7-2. For checkout procedures, refer to Technical Manual, Checkout Procedures for Saturn Launch Vehicle Data Adapter and Digital Computer.

SECTION VIII

TROUBLE ISOLATION

8-1. SCOPE.

8-2. Specific trouble isolation procedures will not be supplied for the simplex models of the data adapter, since these models are used for demonstration and evaluation, and actual procedures should be based upon experience gained in testing and evaluating these models. For the simplex models, this section briefly describes the data which is supplied for point-to-point location of signals.

8-3. DRAWINGS.

8-4. Detailed logic diagrams of each page MIB are included in section X. Also in section X is a signal origin list which shows the figure number for the MIB logic drawing on which any given signal is generated. Further information concerning the drawings is given in section X.

8-5. SIGNAL ROUTING LISTS.

8-6. Supplied as a reference manual is a signal routing list (not part of this manual). The signal routing list shows every location for each signal within the data adapter. A typical signal might be listed as follows:

Signal	Location
G1DVA	*2A1A03-18
G1DVA	2A1A08-81
G1DVA	2A3A06-14
G1DVA	2A3E01-21D
G1DVA	2A3J01-52
G1DVA	2A9E13-08B
G1DVA	2J11-H
G1DVA	2A0BB1-K010
G1DVA	2J20-M

The asterisk indicates the point of origin of the signal.

8-7. In the case of conventional point-to-point wiring, each entry is followed by an indented entry which represents the destination of the wire. In the example above, the last two entries represent the two ends of a wire which connects signal G1DVA from pin K10 on bus bar 1 on panel A10 (A0 is an abbreviation for A10) to pin M of system connector J20. Only the discrete wiring is shown in this manner, since the printed wiring is heavily branched and is generally inaccessible for inspection or repair.

8-8. The wire destinations (indented entries) are not in alphabetical order, but the listings are short enough for reasonably convenient reference.

8-9. Connections between panel assembly E-blocks are implied. For example:

Signal	Location
G1DVA	2A1E01-11E
G1DVA	2A2E02-04B

This listing shows G1DVA appearing on two separate E-blocks located on separate panel assemblies. Since E-blocks are wired together, the wire or printed circuit cable between 2A1E01-11E and 2A2E02-04B is implied and no indented entry is used in this case. If the signal is shown going to more than one E-block, wiring is assumed to exist between the closest two blocks. For instance, an entry involving 2A1E01, 2A2E02 and 2A6E01 would assume one connection between 2A1E01 and 2A2E02 and another between 2A2E02 and 2A6E01.

8-10. PROBING.

8-11. Probing should be limited to page assembly test points, using a test point adapter and adapter probe. (See section IV.) In the simplex models, additional probing may be necessary for evaluation purposes. All probing, however, must be done with the greatest care, since terminals are so close together that it is easy to short adjacent terminals together with the probing device. It is recommended that one person operate the probing device while another observes indications. This will help eliminate probe slippage while observations are being made.

SECTION IX

REPAIR

9-1. SCOPE.

9-2. This section describes the procedures for repairing the data adapter at the laboratory maintenance level.

9-3. PARTS AND ASSEMBLIES.

9-4. Laboratory repair of the data adapter is limited to replacement of page assemblies and converter-regulator assemblies. Replaceable assemblies are listed in figure 9-1. In order to gain access to the interior of the data adapter, it is necessary that the data adapter be mounted on the Equipment Test Stand (IBM part number 6943000). Assuming that the data adapter is mounted on the Transport Dolly (IBM part number 656360), the procedure for installing it on the Test Stand is as follows:

a. Operate Transport Dolly trunnion crank so that data adapter is vertical.

b. Maneuver Transport Dolly toward Test Stand so that rear side of data adapter faces front of Test Stand.

c. Operate lift crank so that data adapter mounting holes are level with locating pins on Test Stand. (The data adapter is mounted on the lower pair of locating pins.)

d. On the Test Stand, remove the pivot locking screws and washers and swing each hinge block down to the table top.

NOTE

If data adapter is not to be opened while on the Test Stand, or if only page assemblies are to be replaced, proceed with only steps g through j.

e. On the Test Stand, extract the hinge pivot pins and detach the hinge halves from the hinge block assemblies.

f. Using the black screws provided with the Test Stand, attach the hinge halves to the data adapter logic sections.

g. Make sure that casters are locked on Test Stand; then maneuver Transport Dolly toward Test Stand until data adapter mounting holes engage locating pins.

h. Secure data adapter to Test Stand with mounting bolts provided.

i. Unlock lift pin knobs on Transport Dolly.

Assembly	Location
6110241	A3A15, A3A31
6111710	A1A4
6111711	A1A18
6111712	A1A17
6111713	A2A1
6111714	A2A3
6111715	A2A4
6111716	A2A5
6111717	A2A6
6111718	A2A7
6111719	A2A24
6111730	A2A8
6111731	A2A9
6111732	A2A20
6111733	A2A22
6111734	A2A33
6111735	A2A31
6111736	A2A32
6111737	A3A11, A3A22, A3A33
6111738	A3A8, A3A19, A3A30
6111739	A3A5, A3A16
6111740	A3A24
6111741	A3A12, A3A23
6111742	A3A3
6111744	A4A7
6111745	A4A3
6111746	A4A4
6111747	A4A19
6111750	A4A17, A4A18
6111751	A4A12, A4A14
6111751	A4A22
6111752	A4A24
6111753	A4A5
6111754	A4A6
6111755	A6A18, A6A29
6111757	A6A19, A6A30
6111758	A6A31
6111759	A6A32
6111760	A7A21, A7A32
6111761	A4A25, A4A26
6111762	A7A11

Assembly	Location
6111763	A8A13, A8A22
6111765	A3A4, A3A7, A3A9, A3A17, A3A18, A3A20, A3A29
6111766	A1A22, A1A23
6111767	A1A19
6111768	A3A25, A3A32
6111769	A1A13
6111770	A2A30
6111771	A4A27
6111772	A1A12
6111773	A1A16
6111774	A1A3, A1A9
6111775	A1A27
6111776	A8A12, A8A16, A8A21, A8A25
6111777	A8A6
6111778	A8A3
6111779	A7A9, A7A20, A7A31
6111780	A7A17, A7A25, A7A28
6111781	A7A6
6111782	A5A3, A5A9, A5A13, A5A15, A5A21, A6A3, A6A11
6111783	A5A6, A5A12, A5A18, A5A24, A6A6, A6A22
6111784	A5A27
6111785	A6A25
6111786	A6A28
6111788	A2A16
6111791	A3A27
6111792	A3A14
6111793	A4A21
6111795	A4A16
6111820	A4A20
6112395	A10J4
6112396	A10J9
6112397	A10J6, A10J7, A10J10
6112398	A10J8
6112399	A10J5, A10J11

Figure 9-1. Replaceable Assemblies

j. Adjust Transport Dolly lift pin knobs so that lift pins disengage data adapter lift holes; then pull Transport Dolly away from Test Stand.

k. Pivot hinge blocks to their upright position and install pivot locking screws.

l. Mate hinge halves on data adapter to hinge block assemblies by backing off on either hinge half or hinge block mounting screws and adjusting as much as slotted screw holes will permit.

m. Reinstall the hinge pivot pins and tighten hinge screws.

9-5. REPLACEMENT OF PAGE ASSEMBLIES.

9-6. The page assemblies are located in the front and rear logic sections of the data adapter and are accessible after removal of either the front or rear logic cover. (See figure 9-2.) The replacement of page assemblies requires an insert-extract tool (IBM tool number 657922). To replace a page assembly proceed as follows:

a. Install the data adapter on the Test Stand. (See paragraph 9-4.)

b. Determine in which logic section (front or rear) that the page assembly to be replaced is located. (See figure 9-3.) Logic sections one through four are located in the data adapter rear logic section and logic sections five through eight are located in the data adapter front logic section.

CAUTION

Avoid scratching or damaging the cover contact surfaces of the data adapter frames or covers. This practice insures a good metal-to-metal radio frequency seal when the covers are reinstalled.

c. Remove the front (or rear) logic cover by removing and retaining the 42 mounting screws and washers.

d. Locate the page assembly to be replaced. (See figures 9-3 and 9-4.)

NOTE

Do not remove page assembly captive mounting screws from the page assembly until after the page assembly is removed.

e. Unscrew the two page assembly mounting screws until free of mounting holes.

f. Place insert-extract tool over top of page assembly; then push locking knob toward page assembly, securing the tool to assembly.

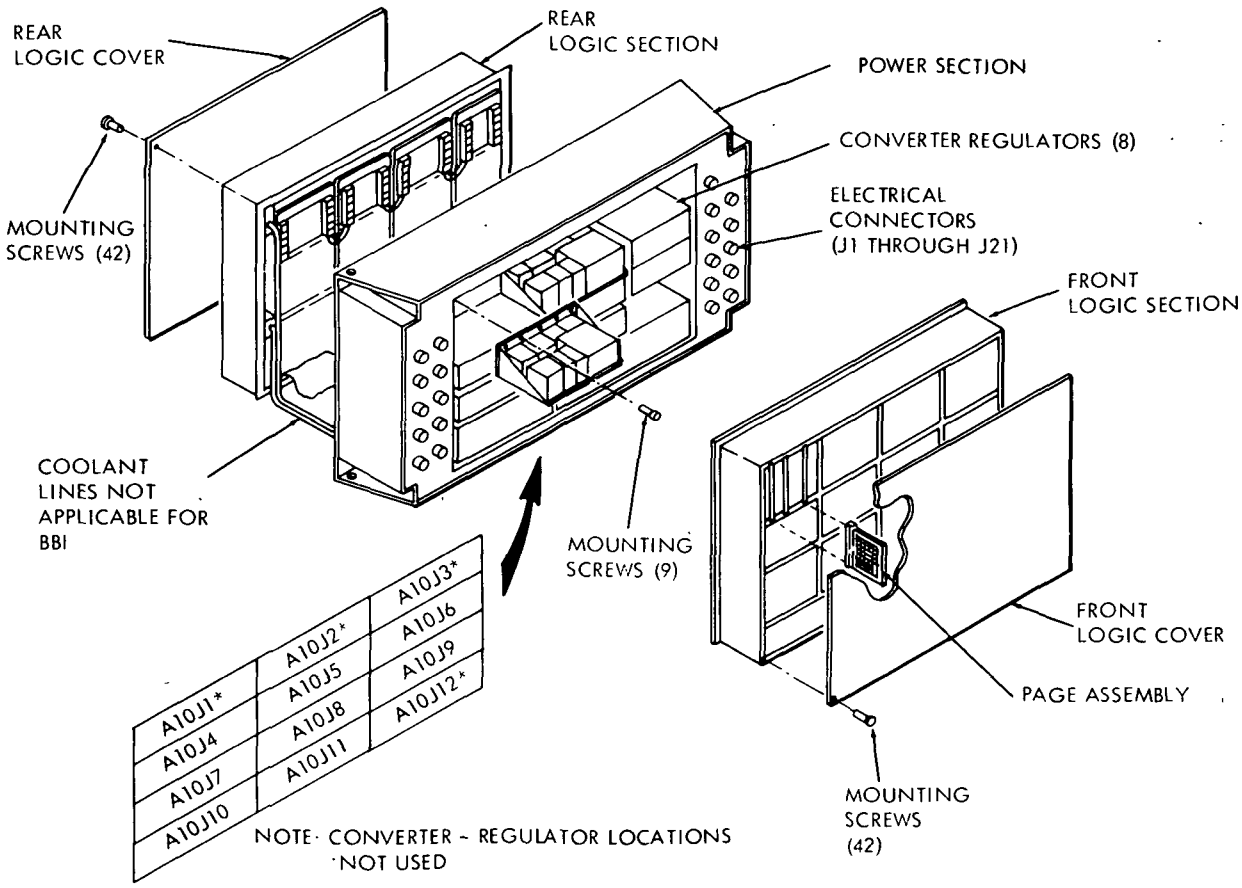


Figure 9-2. Data Adapter, Exploded View

g. Squeeze insert-extract tool handle to its limit (disengaging page assembly connector); then pull page assembly straight out.

CAUTION

Hold page assembly firmly to avoid dropping the page when releasing the insert-extract tool.

h. Release page assembly from insert-extract tool by pushing in the unlock knob and removing tool from page assembly.

i. Remove mounting screws with associated fiber washers from page assembly and retain for reuse.

j. Install page assembly mounting screws with associated washers (previously removed) in replacement page assembly.

k. Place insert-extract tool over top of replacement page assembly; then push locking knob toward page assembly, securing tool to assembly.

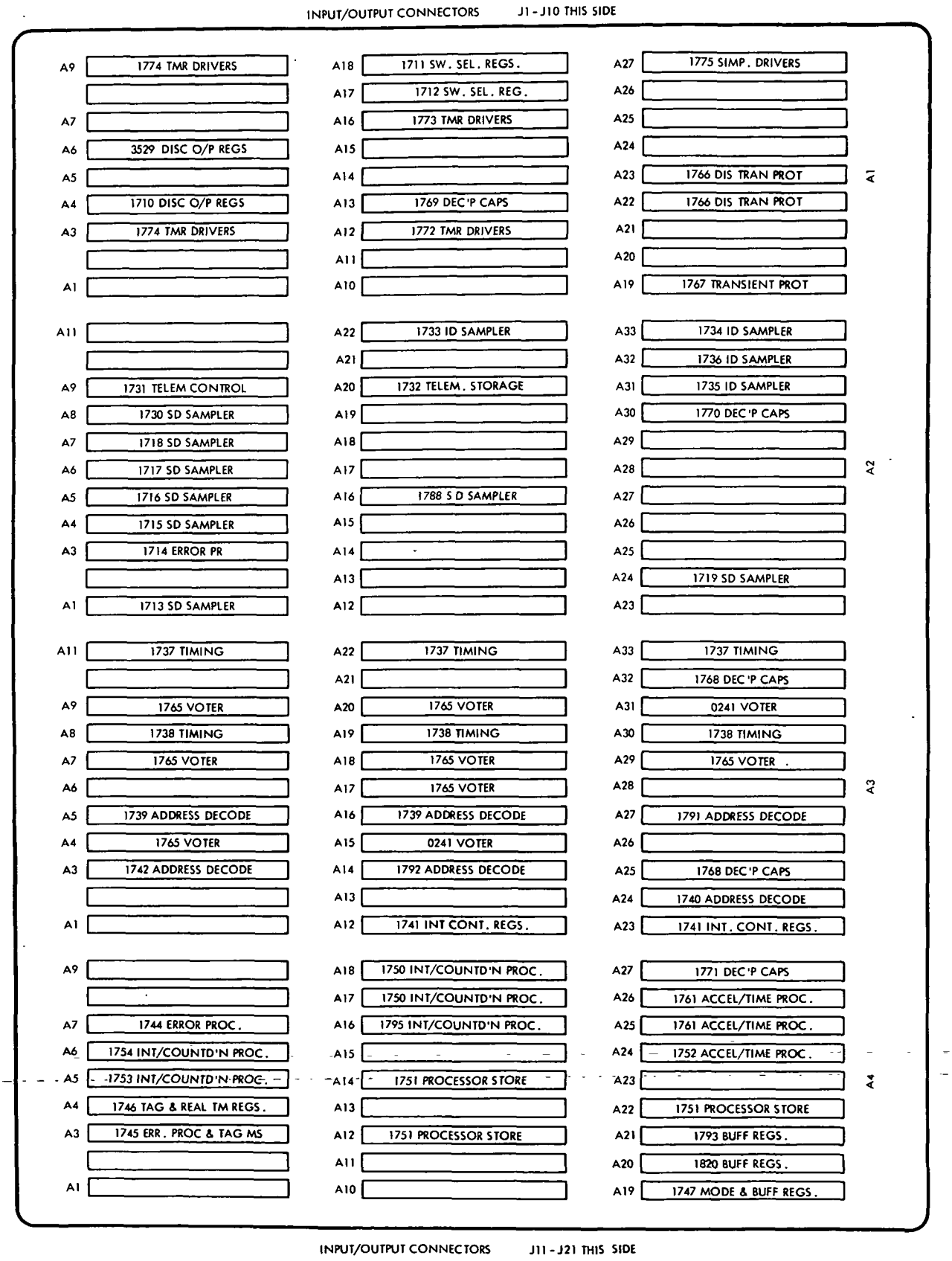


Figure 9-3. Page Assembly Location Guide, Front Logic Section

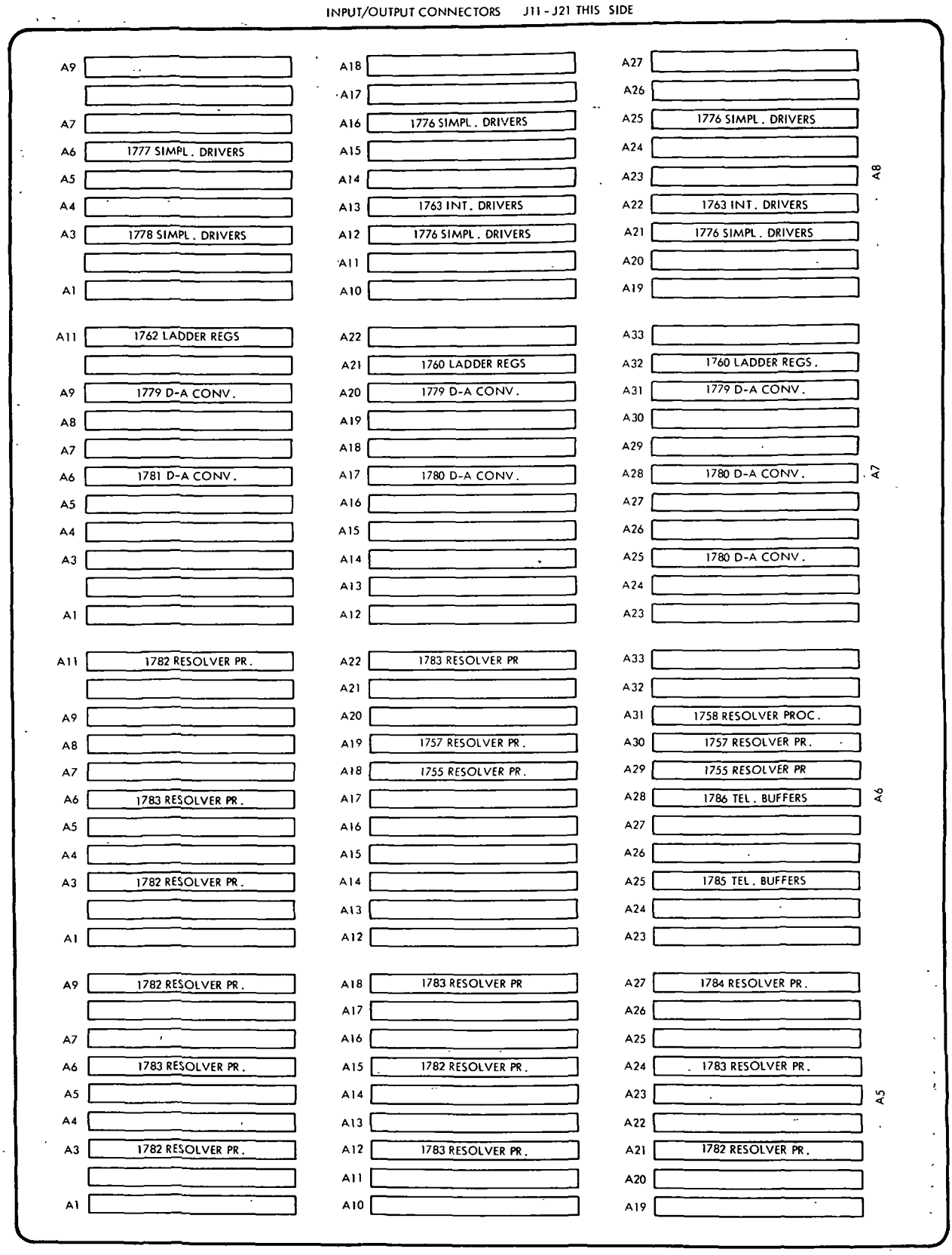


Figure 9-4. Page Assembly Location Guide, Rear Logic Section

CAUTION

Verify that page assembly A side faces left when inserting page assembly into data adapter logic section.

l. Insert page assembly into proper data adapter logic section location.

m. Push-in the unlock knob on insert-extract tool; then remove tool from page assembly.

n. Start the two page assembly mounting screws; then tighten screws to 15 inch-pounds.

NOTE

The page assembly installation is now complete. If the data adapter is to be tested immediately it shall remain mounted on the test stand. The logic section covers of LVDA Breadboard Model I, IBM part number 6109013, must be removed during testing to enable forced-air cooling of the components. The logic section covers of all other data adapter models may be installed during test if liquid cooling is provided. To install the logic section covers perform step o.

o. Secure front (or rear) logic cover with the 42 cover mounting screws and washers previously removed; then using the cross-over method, torque mounting screws to 20 inch-pounds.

9-7. REPLACEMENT OF CONVERTER-REGULATORS.

9-8. The converter-regulator assemblies are located in the data adapter center section. The converter-regulator assemblies are accessable after the data adapter front and rear logic sections are swung open at the top approximately 60 degrees. The logic sections are opened while the data adapter is mounted on the Test Stand. Hinges and logic support handles support the logic sections when opened. To replace a converter-regulator assembly proceed as follows:

a. Install the data adapter on the Test Stand. (Refer to paragraph 9-2.)

b. Using the light-colored screws provided with the Test Stand, attach a left and a right logic support handle to the front logic section of the data adapter.

c. Remove the 42 mounting screws from the front logic section and gently lower the logic section down on its support handles.

d. Back off mounting screws on support handles and adjust handles to support load equally.

e. Tighten mounting screws on support handles.

f. Repeat steps b. through e. for the rear logic section.

g. Locate the converter-regulator to be replaced. (See figure 9-2.)

NOTE

The +6 VDC and +20 VDC converter-regulators contain components which extend beyond the mounting flange of the converter-regulators mounted immediately above them. Consequently, to remove a converter-regulator mounted above a +6 VDC or a +20 VDC converter-regulator, the +6 VDC or +20 VDC converter-regulator must be removed first. The sequence for removal is as follows:

1. To remove A10J2, first remove A10J5.
2. To remove A10J3, first remove A10J6.
3. To remove A10J4, first remove A10J10, then A10J7 (in that order).
4. To remove A10J7, first remove A10J10.
5. To remove A10J8, first remove A10J11.
6. To remove A10J9, first remove A10J12.

h. On rear side of the converter-regulator section, unscrew the captive screws on the receptacle connector which mates with the connector of the converter-regulator to be removed.

i. Unscrew the nine converter-regulator captive mounting screws; then pull the converter-regulator assembly straight out.

j. Detach captive mounting screws from converter-regulator assembly and retain for reuse.

k. Install captive mounting screws (previously removed) in replacement converter-regulator assembly.

l. Insert replacement converter-regulator into its proper location.

m. Start the nine converter-regulator mounting screws; then tighten screws to 19 inch-pounds.

n. On rear side of converter-regulator section, tighten the two captive retaining screws on the converter-regulator receptacle connector.

o. Raise the rear logic section to its closed position; then secure with the 42 mounting screws and washers.

p. Using the cross-over method, tighten the rear logic section mounting screws to 20 inch-pounds.

q. Repeat steps o. and p. for the front logic section.

SECTION X

DIAGRAMS

10-1. GENERAL.

10-2. This section contains logic diagrams of the multilayer interconnection boards (MIBs) for each page assembly, figures 10-1 through 10-30. The following data has been provided to facilitate locating signals throughout the logic diagrams:

1. Functional grouping of logic diagrams. In general, the logic diagrams are grouped according to the manner in which they were discussed in the theory of operation section. For instance, all logic diagrams for MIBs containing timing logic are included under one figure title. Two notable exceptions to this arrangement are the voter logic and the decoupling capacitor logic which are grouped separately, since a given voter or capacitor page might contain voters or capacitors for a number of different functional circuits. Also, small portions of one functional circuit may be located on the pages of another functional circuit in the interests of packaging economy.

2. Signal origin list, figure 10-31. Every signal which is generated within the data adapter and is available at a page connector or test point is listed alphabetically with the figure and sheet number of the logic diagram depicting its origin.

NOTE

Signals not generated within the data adapter are diagrammed and listed alphabetically by system connector in section III.

3. Table of logic diagrams for each MIB, figure 10-32. In the event that the logic diagram of a particular MIB location is required, it may be located on this table. The numbers across the top of the table (2A1, 2A2, etc.) represent the back panels. The left column represents MIB designators. To find the logic diagram for the "B" MIB of page A23 on back panel 2A3 for instance, find the intersection of column 2A3 and row A23B; in this example, the logic diagram would be figure 10-6. Only the figure number is given for the logic diagram; therefore it may be necessary to search a number of sheets in some figures to locate the appropriate diagram. (The MIB reference designation is included on each logic diagram.)

10-3. LOGIC DIAGRAMS.

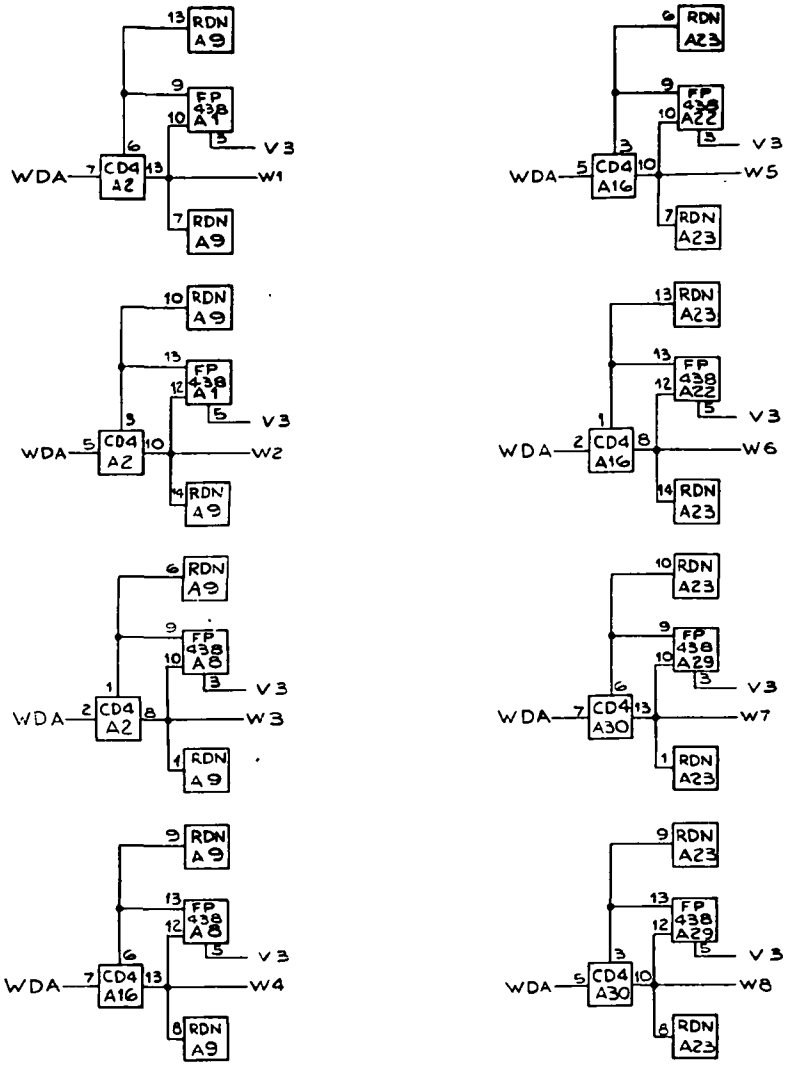
10-4. Logic symbols used in the MIB logic diagrams are defined in the List of MIB Logic Symbols appendix. Only one AND symbol is shown on the logic diagrams although three AND configuration identifications exist. The appropriate configuration identification for a given AND symbol may be located on the "ULD LOCATIONS" chart on each drawing. To find the proper configuration identifications, note the ULD location number included in the AND gate symbol. Then find the location number in the "ULD LOCATIONS" chart and the configuration identification will be given. The three configuration identifications are AA, AB and I. All three configuration identifications are described under symbol A in the List of MIB Logic Symbols located in the appendix.

10-5. Location of input and output signals for each side of a page are shown on the CONNECTOR PINS chart on each logic diagram. A THRU-PINS chart is provided for those signals which go from one side of a page to the other. In some cases, a single signal might be available from more than one page connector pin. In this case, the appropriate pin number is shown in parentheses following the signal name on the logic diagram, e.g., ABC (98). Also, some spare connections are occasionally shown which tie back to page connectors but have no signal name assigned. In this case only the pin number is shown.

10-6. Included in the notes on each MIB logic diagram is an identification number which consists of the IBM engineering drawing number for the logic, the revision level, and the latest engineering change level.

10-7. SIGNAL ROUTING LISTS.

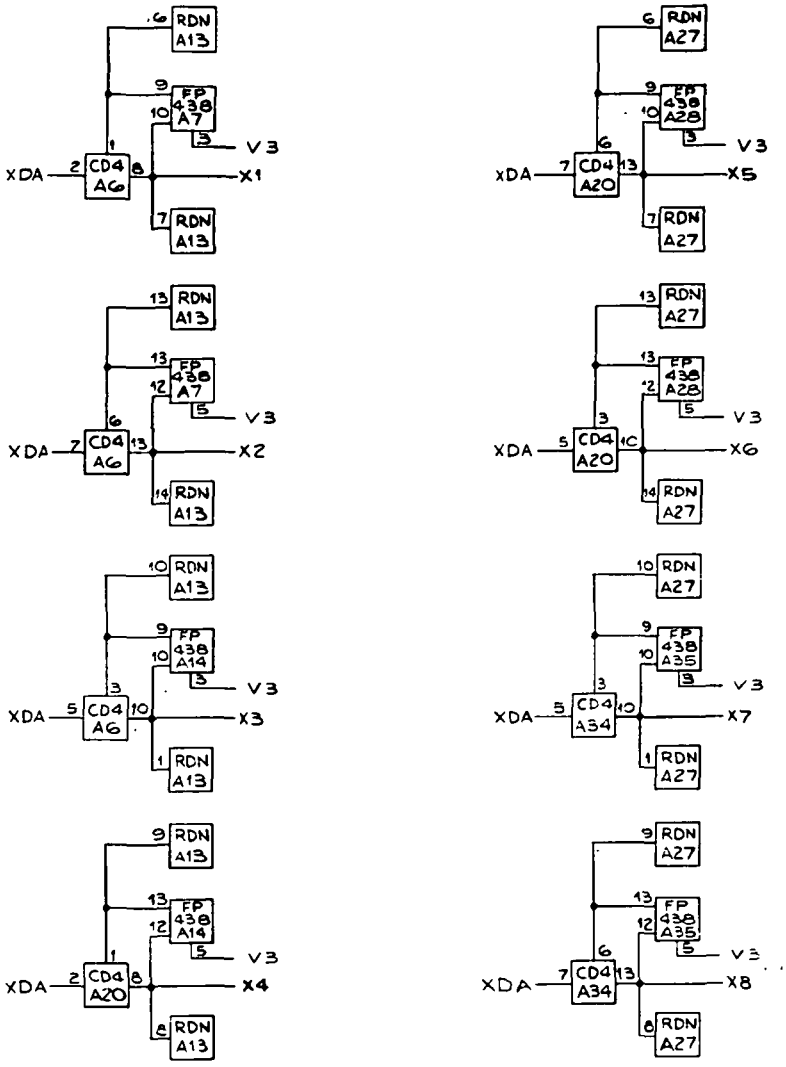
10-8. Signal routing lists are provided in a separate document. A description of these lists is provided in section VIII of this manual.



ULD LOCATIONS

A1 FP 438	A2 CD4	A3	A4	A5	A6 CD4	A7 FP 438
A8 FP 438	A9 RDN	A10	A11	A12	A13 RDN	A14 FP 438
A15	A16 CD4	A17	A18	A19	A20 CD4	A21
A22 FP 438	A23 RDN	A24	A25	A26	A27 RDN	A28 FP 438
A29 FP 438	A30 CD4	A31	A32	A33	A34 CD4	A35 FP 438

Figure 10-1. Timing Logic Diagram (Sheet 1 of 8)

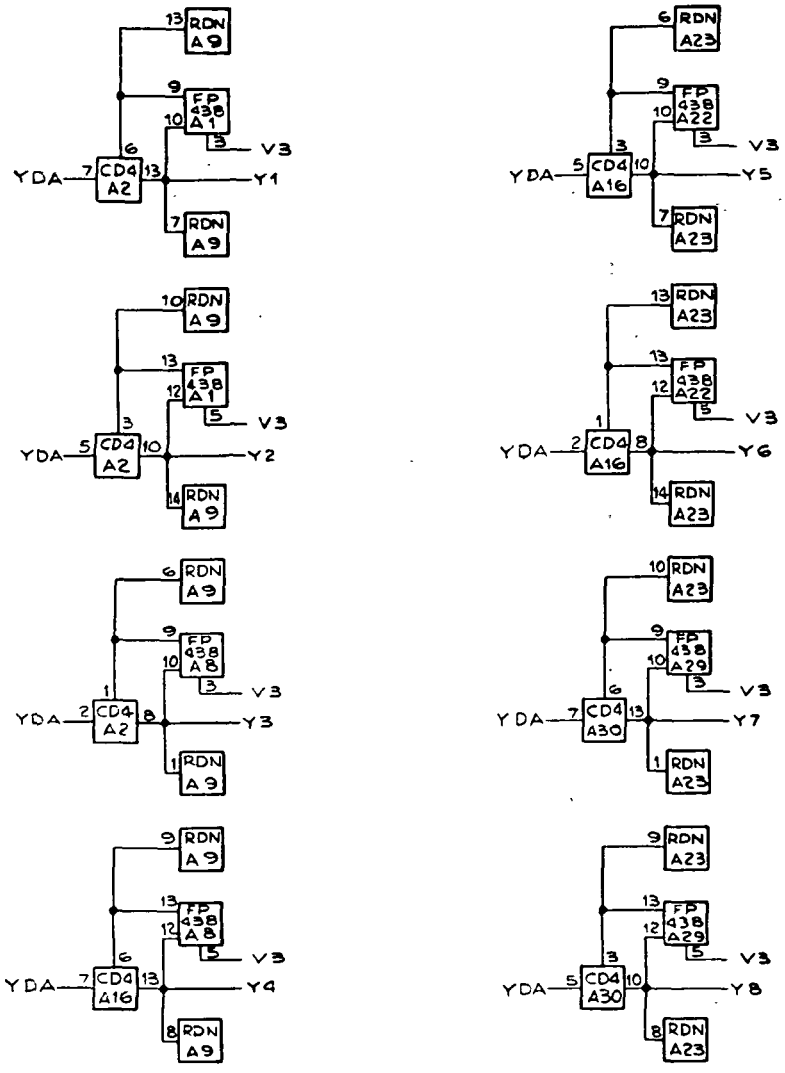


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	W1	51	
3	W3	53	
5	W2	55	
7	W5	57	
9	W4	59	
11	W7	61	
13	W8	63	
15	NC	65	
17	V1	67	
19	V3	69	XDA
21		71	X4
23	SIG-RET	73	
25		75	
27		77	
29	WDA	79	
31		81	
33		83	
35		85	X6
37		87	X7
39		89	X8
41		91	X3
43		93	X5
45		95	X1
47		97	X2
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A11 Side A, 2A3A22 Side A, 2A3A33 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112167-REL(66123BJ)

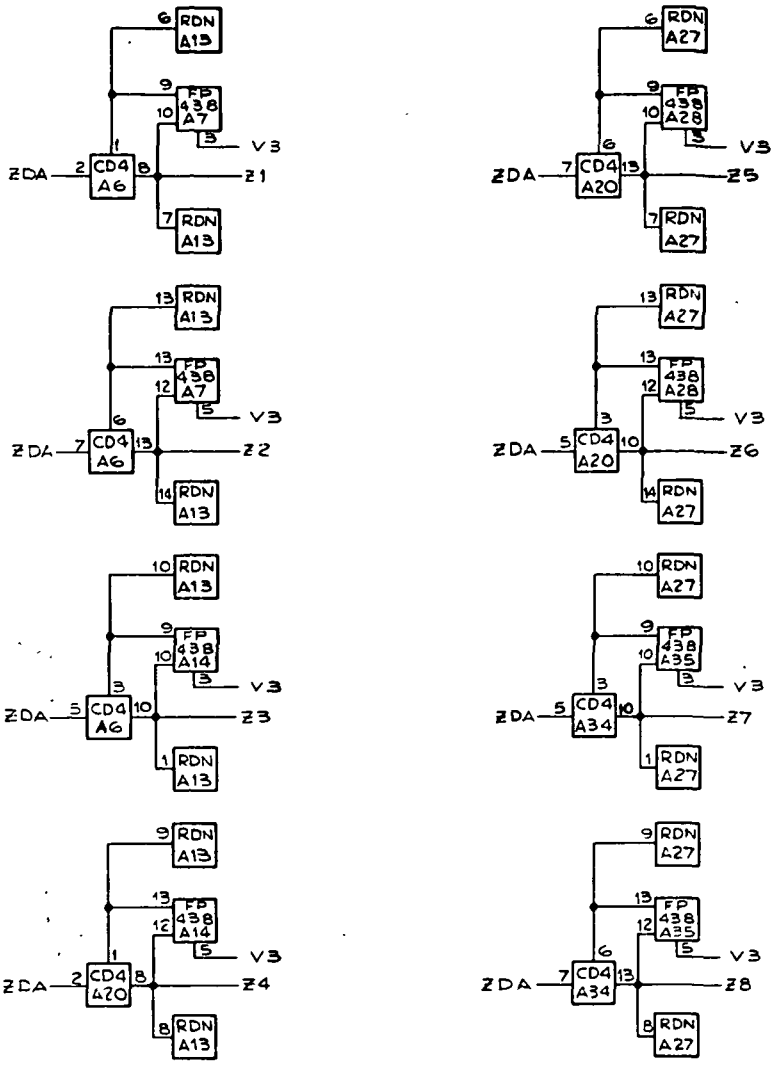
Figure 10-1. Timing Logic Diagram (Sheet 2)



ULD LOCATIONS

A1 FP 438	A2 CD4	A3	A4	A5	A6 CD4	A7 FP 438
A8 FP 438	A9 FDN	A10	A11	A12	A13 RDN	A14 FP 438
A15	A16 CD4	A17	A18	A19	A20 CD4	A21
A22 FP 438	A23 RDN	A24	A25	A26	A27 RDN	A28 FP 438
A29 FP 438	A30 CD4	A31	A32	A33	A34 CD4	A35 FP 438

Figure 10-1. Timing Logic Diagram (Sheet 3)



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A11 Side B, 2A3A22 Side B, 2A3A33 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112168-REL(66123ET)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	Z2	52	
4	Z1	54	
6	Z5	56	
8	Z3	58	
10	Z8	60	
12	Z7	62	
14	Z6	64	
16		66	
18		68	
20		70	YDA
22		72	
24		74	
26		76	SIG-RET
28	Z4	78	
30	ZDA	80	V3
32		82	V1
34		84	Y6
36		86	Y8
38		88	Y7
40		90	Y4
42		92	Y5
44		94	Y2
46		96	Y3
48		98	Y1
50			

Figure 10-1. Timing Logic Diagram (Sheet 4)

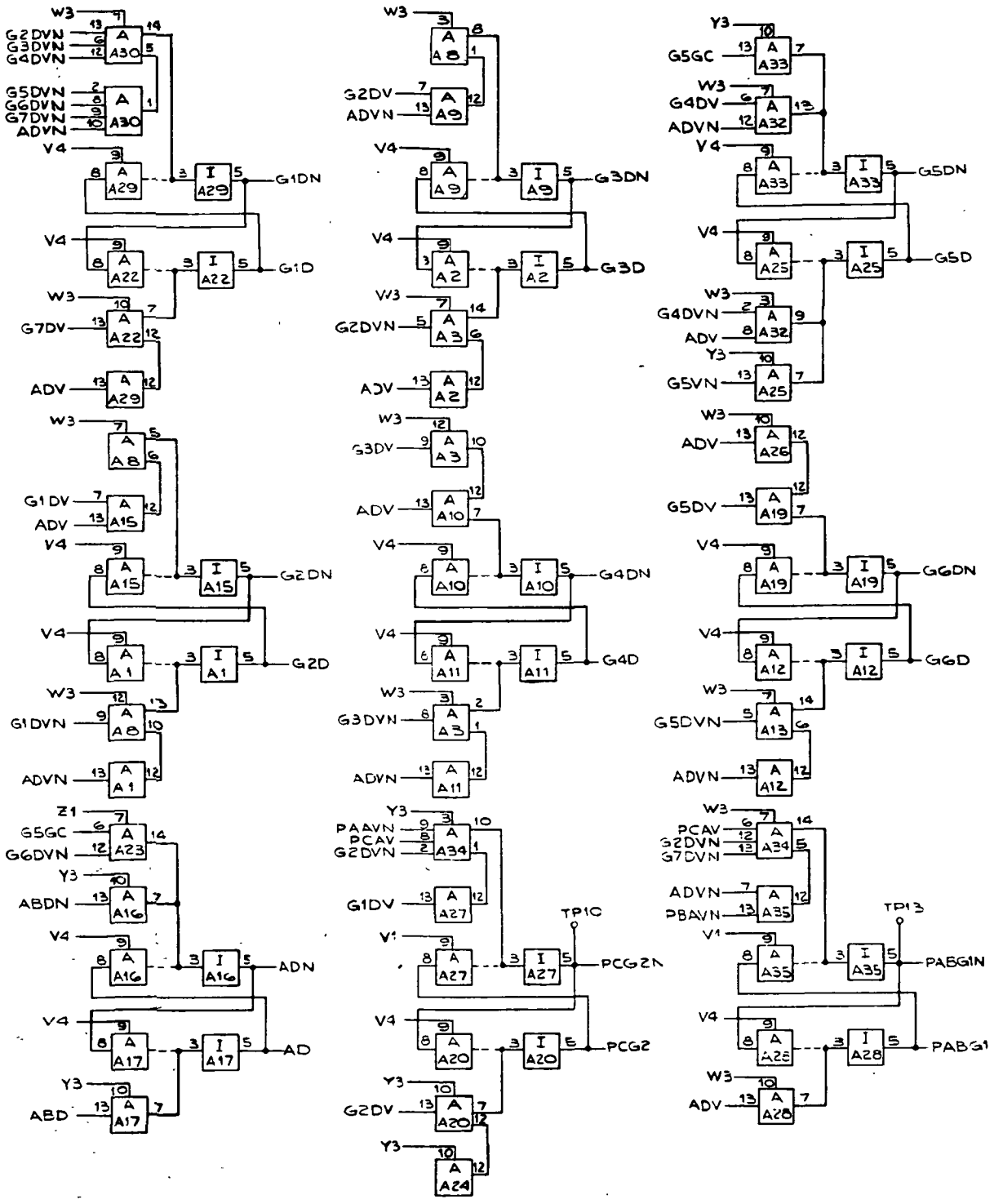
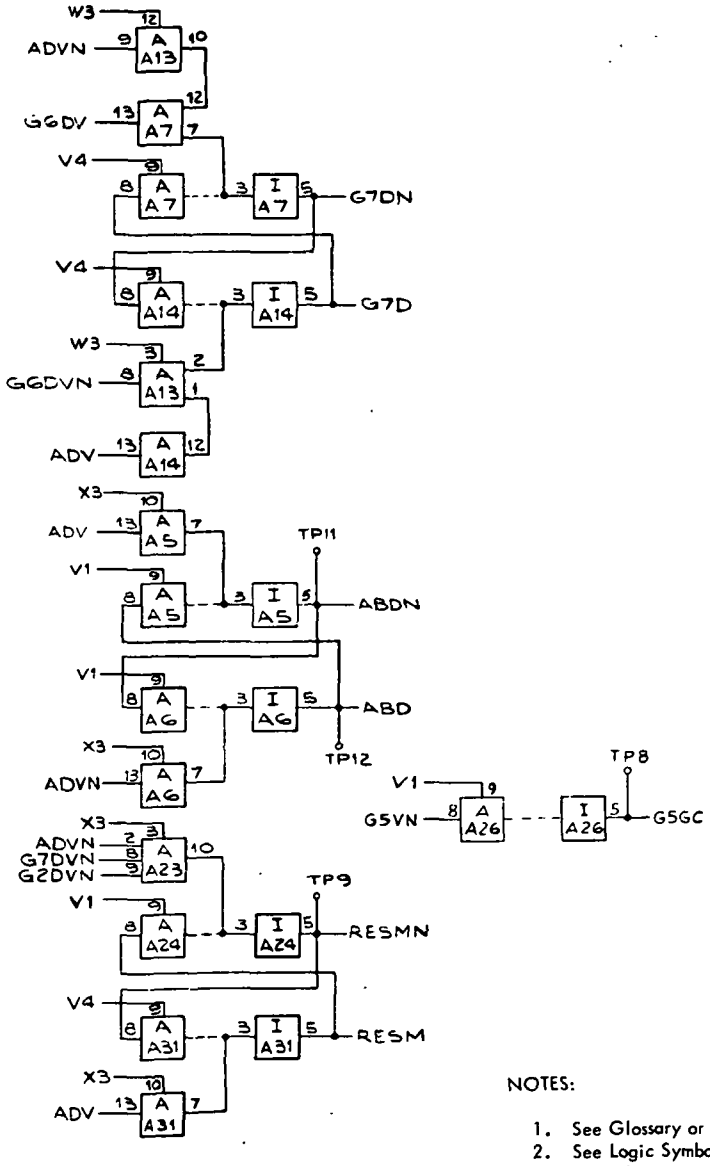


Figure 10-1. Timing Logic Diagram (Sheet 5)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	Z1
2	G2DVN	17	G7DVN
3		18	
4		19	
5		20	
6		21	G1DV
7		22	ADVN
8		23	
9		24	W3
10		25	G2DV
11		26	
12		27	Y3
13		28	PAAVN
14	PCAV	29	PBAVN
15		30	X3

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	G1DVN	51	G4DV
3	G2DN	53	SIG RET
5	G2D	55	G5VN
7	G7DV	57	V3
9	G1D	59	G5D
11	G3DN	61	
13	G3D	63	G4DN
15	G1DN	65	GGD
17	G7DVN	67	G5DV
19	G6DVN	69	GGDN
21	G5DVN	71	PCG2
23	G4DVN	73	G5DN
25	G3DVN	75	
27	G3DV	77	G2DVN
29	ADN	79	
31	AD	81	G1DV
33	V4	83	G2DV
35	V1	85	G7D
37		87	G7DN
39		89	PABG1
41	ADVN	91	X3
43	G4D	93	GGDV
45	ADV	95	
47	RESM	97	
49			

ULD LOCATIONS

A1 I	A2 I	A3 AB	A4	A5 I	A6 I	A7 I
A8 AB	A9 I	A10 I	A11 I	A12 I	A13 AB	A14 I
A15 I	A16 I	A17 I	A18	A19 I	A20 I	A21
A22 I	A23 AA	A24 I	A25 I	A26 I	A27 I	A28 I
A29 I	A30 AA	A31 I	A32 AA	A33 I	A34 AA	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A8 Side A, 2A3A19 Side A, 2A3A30 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112118-A(66123EA).

Figure 10-1. Timing Logic Diagram (Sheet 6)

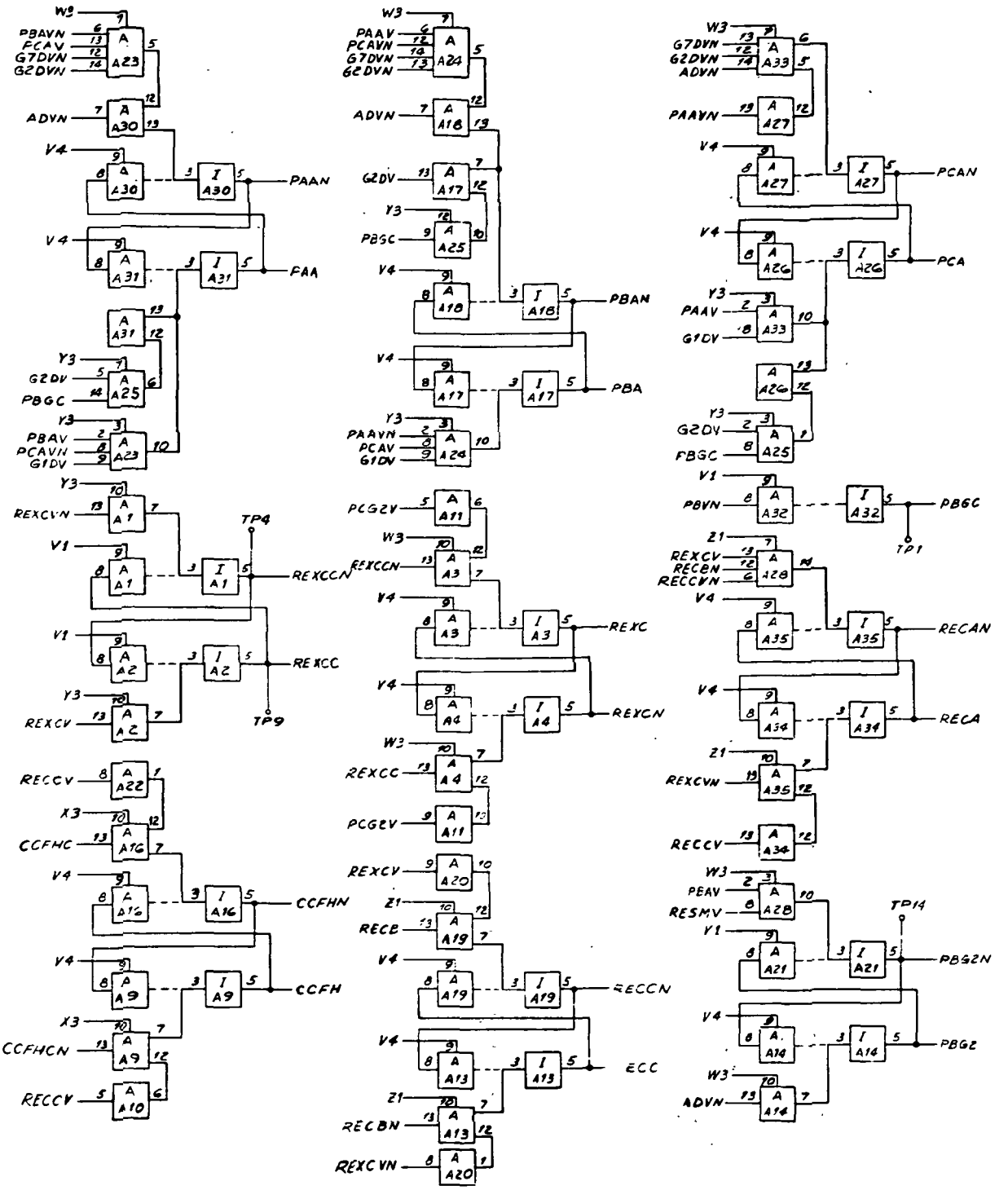
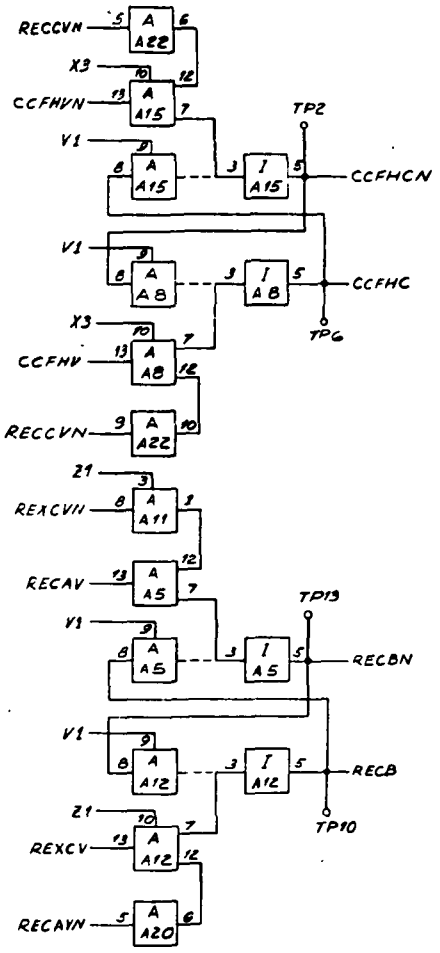


Figure 10-1. Timing Logic Diagram (Sheet 7)



THRU PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	Z3
2	G2DVN	17	G1DVN
3		18	
4		19	
5		20	
6		21	G1DV
7		22	ADVN
8		23	
9		24	W3
10		25	G2DV
11		26	
12		27	Y3
13		28	PAAVN
14	PCAV	29	PBAVN
15		30	X3

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	REXCV	52	
4	REXCVN	54	PBVN
6	RECCVN	56	PCAVN
8	RESMV	58	REXC
10	Z1	60	
12	Y3	62	
14	RECA	64	PBAV
16	PAAVN	66	PAAN
18	RECAVN	68	PCAV
20	RECCV	70	PBAVN
22	PBGZ	72	PBA
24		74	REXCN
26	V4	76	
28	RECAN	78	Y3
30	PCA	80	PAA
32	PCAN	82	V1
34	RECAV	84	CCFHV
36		86	CCFHVN
38	PAAV	88	CCFH
40	RECC	90	CCFHN
42	RECCN	92	
44	PCGZV	94	
46	PBAN	96	SIG RET
48		98	V3
50	W3		

ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5 I	A6	A7
A8 I	A9 I	A10 AB	A11 AB	A12 I	A13 I	A14 I
A15 I	A16 I	A17 I	A18 I	A19 I	A20 AE	A21 I
A22 AE	A23 AA	A24 AA	A25 AB	A26 I	A27 I	A28 AA
A29	A30 I	A31 I	A32 I	A33 AA	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A8 Side B, 2A3A19 Side B, 2A3A30 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112138-REL(66123N)

Figure 10-1. Timing Logic Diagram (Sheet 8)

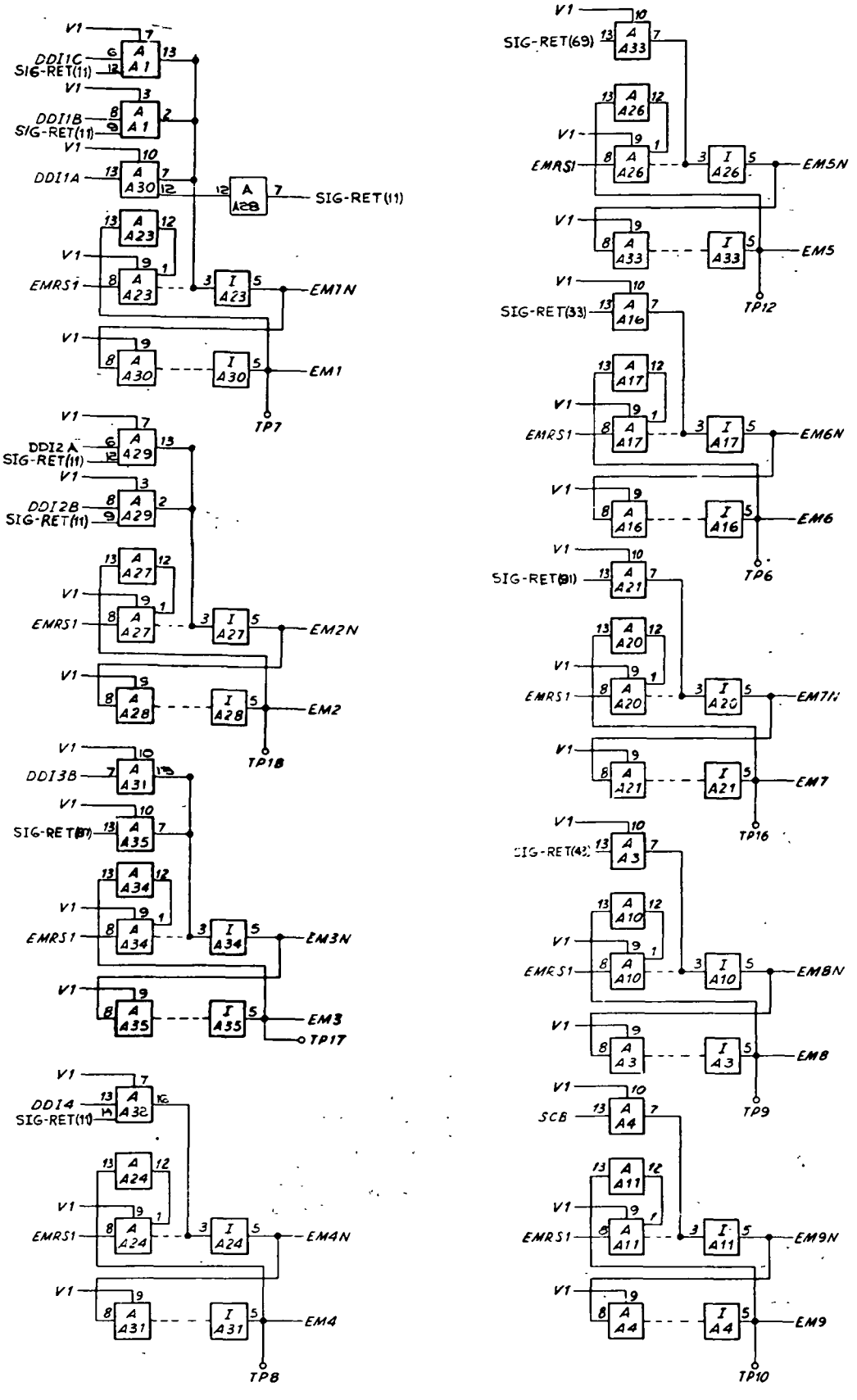
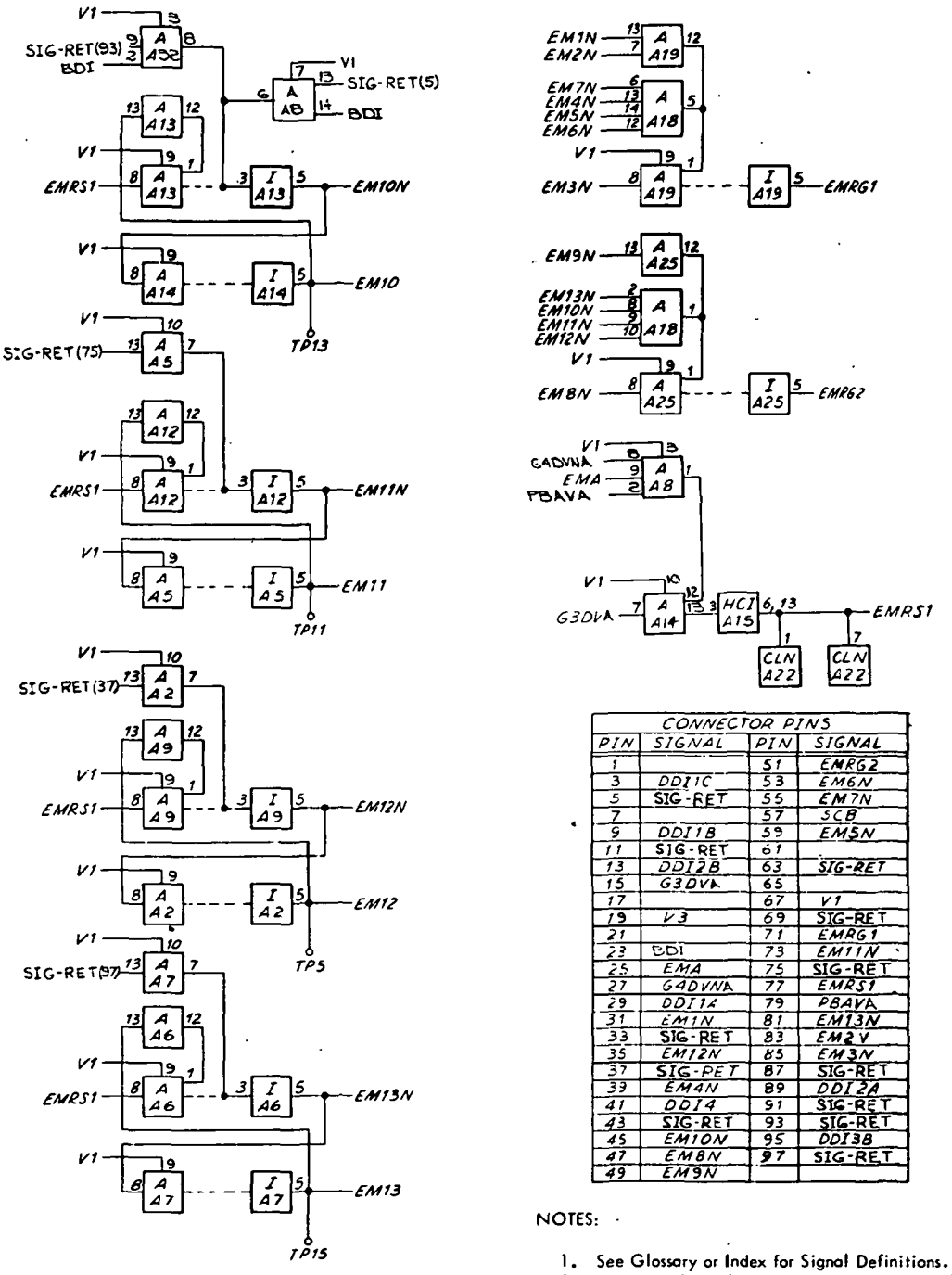


Figure 10-2. Error Processor Logic Diagram (Sheet 1 of 6)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1		51	EMRG2
3	DDI1C	53	EM6N
5	SIG-RET	55	EM7N
7		57	SCB
9	DDI1B	59	EM5N
11	SIG-RET	61	
13	DDI2B	63	SIG-RET
15	G3DVA	65	
17		67	V1
19	V3	69	SIG-RET
21		71	EMRG1
23	BDI	73	EM11N
25	EMA	75	SIG-RET
27	G4DVNA	77	EMRS1
29	DDI1A	79	PBAVA
31	EM1N	81	EM13N
33	SIG-RET	83	EM2V
35	EM12N	85	EM3N
37	SIG-RET	87	SIG-RET
39	EM4N	89	DDI2A
41	DDI4	91	SIG-RET
43	SIG-RET	93	SIG-RET
45	EM10N	95	DDI3B
47	EM8N	97	SIG-RET
49	EM9N		

ULD LOCATIONS

A1 AA	A2 I	A3 I	A4 I	A5 I	A6 I	A7 I
A8 AA	A9 I	A10 I	A11 I	A12 I	A13 I	A14 I
A15 HCI	A16 I	A17 I	A18 AA	A19 I	A20 I	A21 I
A22 CLN	A23 I	A24 I	A25 I	A26 I	A27 I	A28 I
A29 AA	A30 I	A31 I	A32 AA	A33 I	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A7 Side A.
6. This Drawing Derived From IBM DWG NO. 6112879-REL(66126EJ)

Figure 10-2. Error Processor Logic Diagram (Sheet 2)

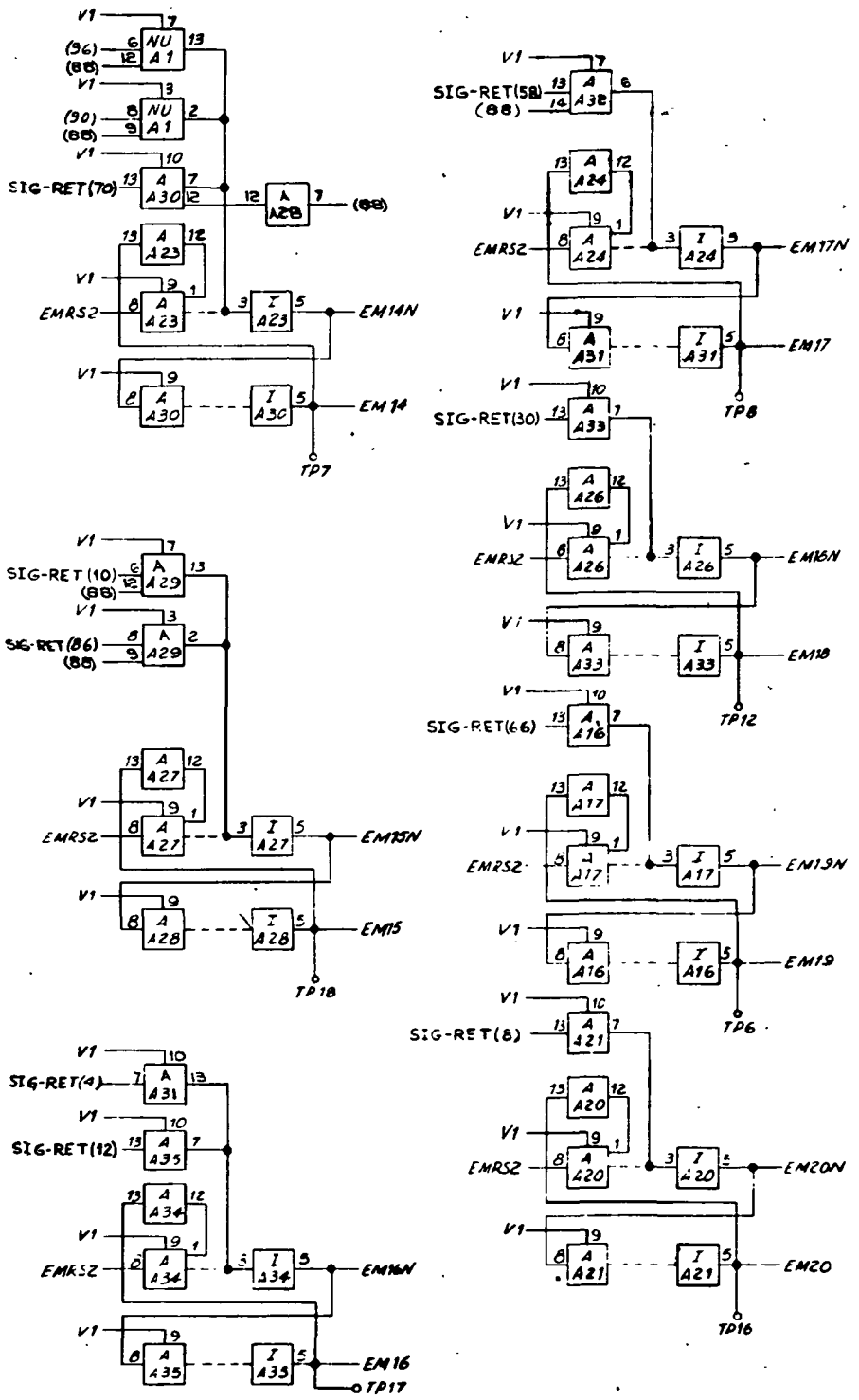
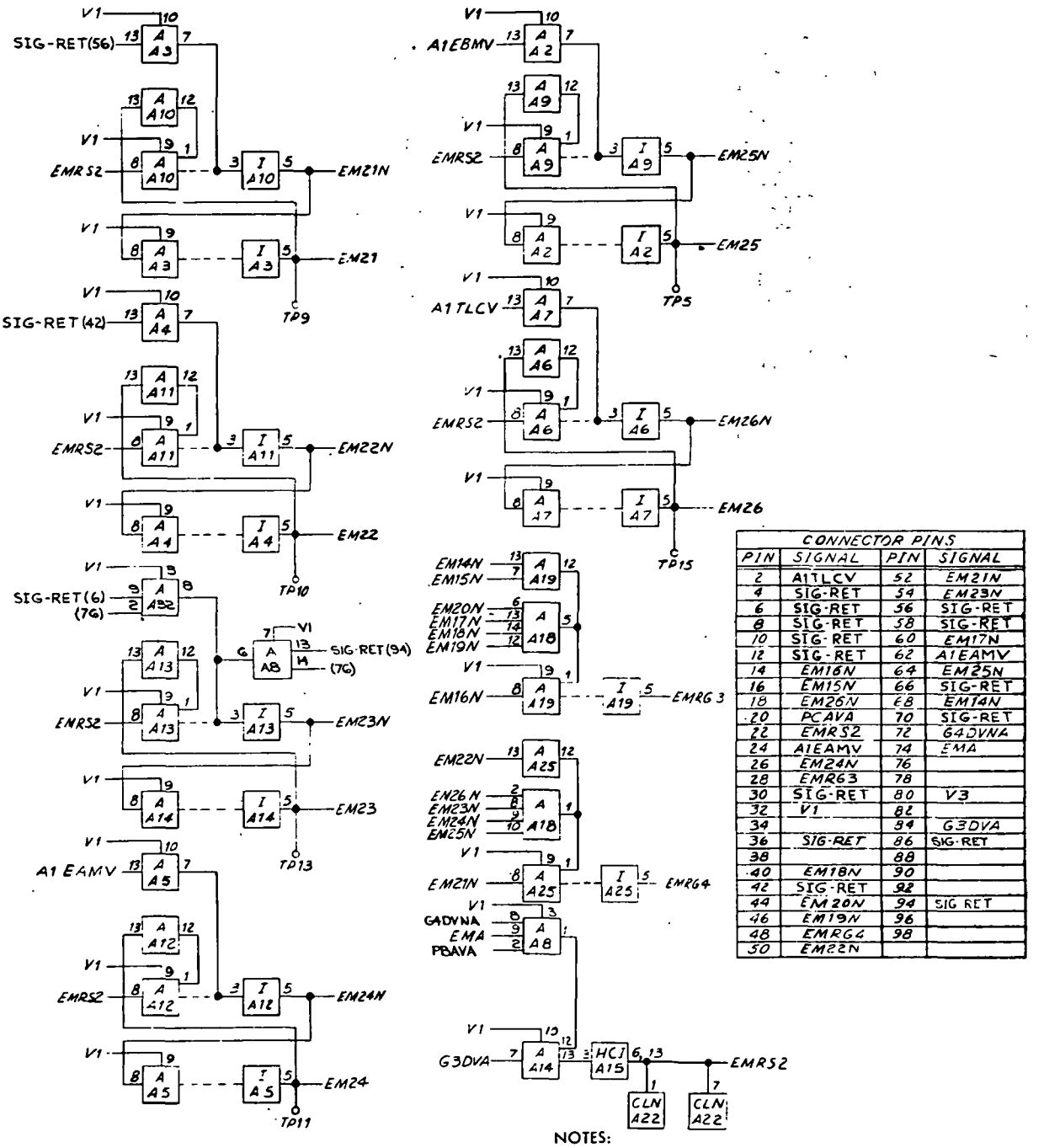


Figure 10-2. Error Processor Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	A1TLCV	52	EM21N
4	SIG-RET	54	EM23N
6	SIG-RET	56	SIG-RET
8	SIG-RET	58	SIG-RET
10	SIG-RET	60	EM17N
12	SIG-RET	62	A1EAMV
14	EM18N	64	EM25N
16	EM15N	66	SIG-RET
18	EM26N	68	EM14N
20	PCAVA	70	SIG-RET
22	EMRS2	72	G4DVNA
24	A1EAMV	74	EMA
26	EM24N	76	
28	EMRG3	78	
30	SIG-RET	80	V3
32	V1	82	
34		84	G3DVA
36	SIG-RET	86	SIG-RET
38		88	
40	EM18N	90	
42	SIG-RET	92	
44	EM20N	94	SIG RET
46	EM19N	96	
48	EMRG4	98	
50	EM22N		

ULD LOCATIONS

A1	A2 I	A3 I	A4 I	A5 I	A6 I	A7 I
A8 AA	A9 I	A10 I	A11 I	A12 I	A13 I	A14 I
A15 HCI	A16 I	A17 I	A18 AA	A19 I	A20 I	A21 I
A22 CLN	A23 I	A24 I	A25 I	A26 I	A27 I	A28 I
A29 AA	A30 I	A31 I	A32 AA	A33 I	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A7 Side B.
6. This Drawing Derived From IBM DWG NO. 6112959-REL(66126RJ)

Figure 10-2. Error Processor Logic Diagram (Sheet 4)

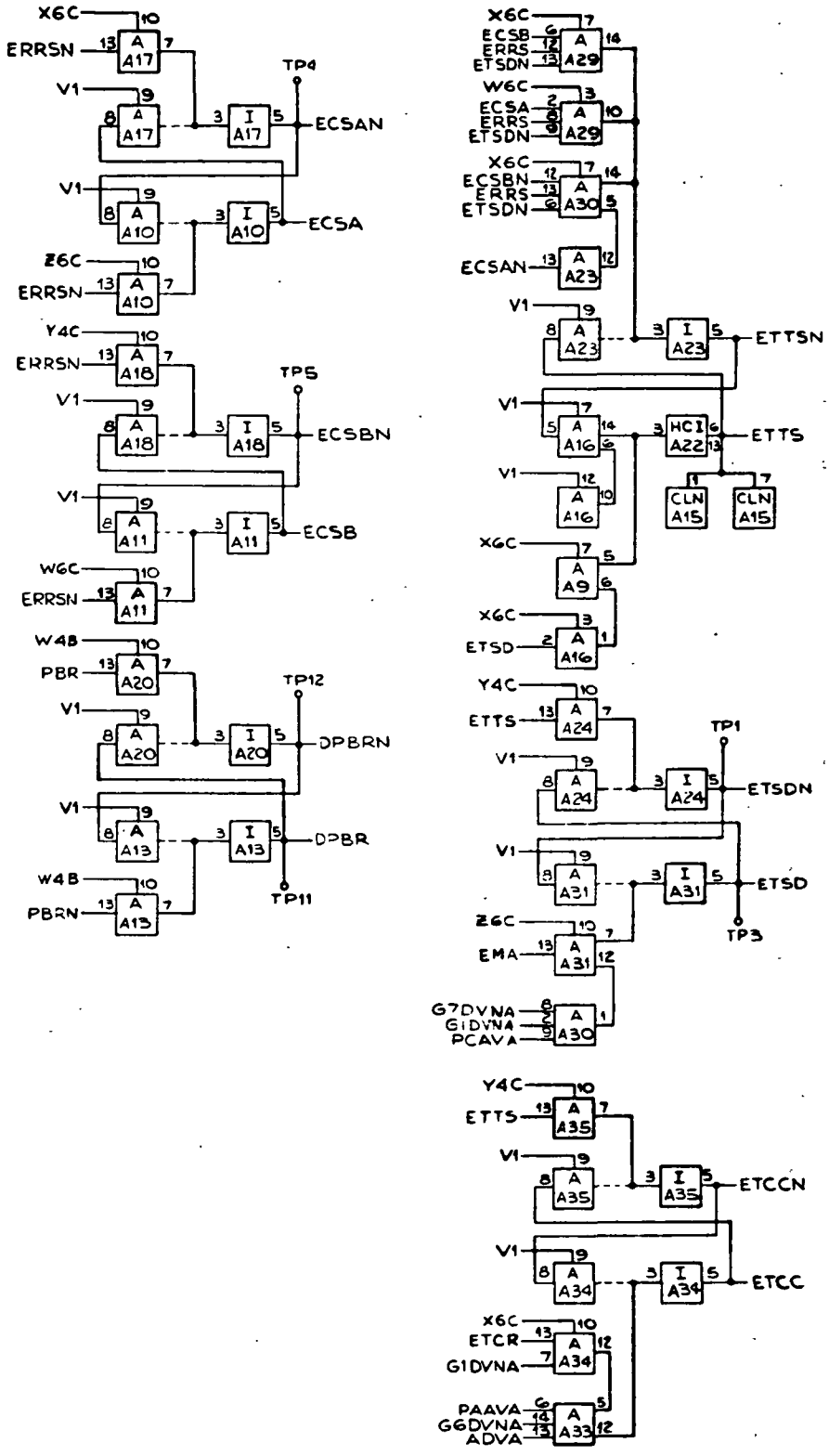
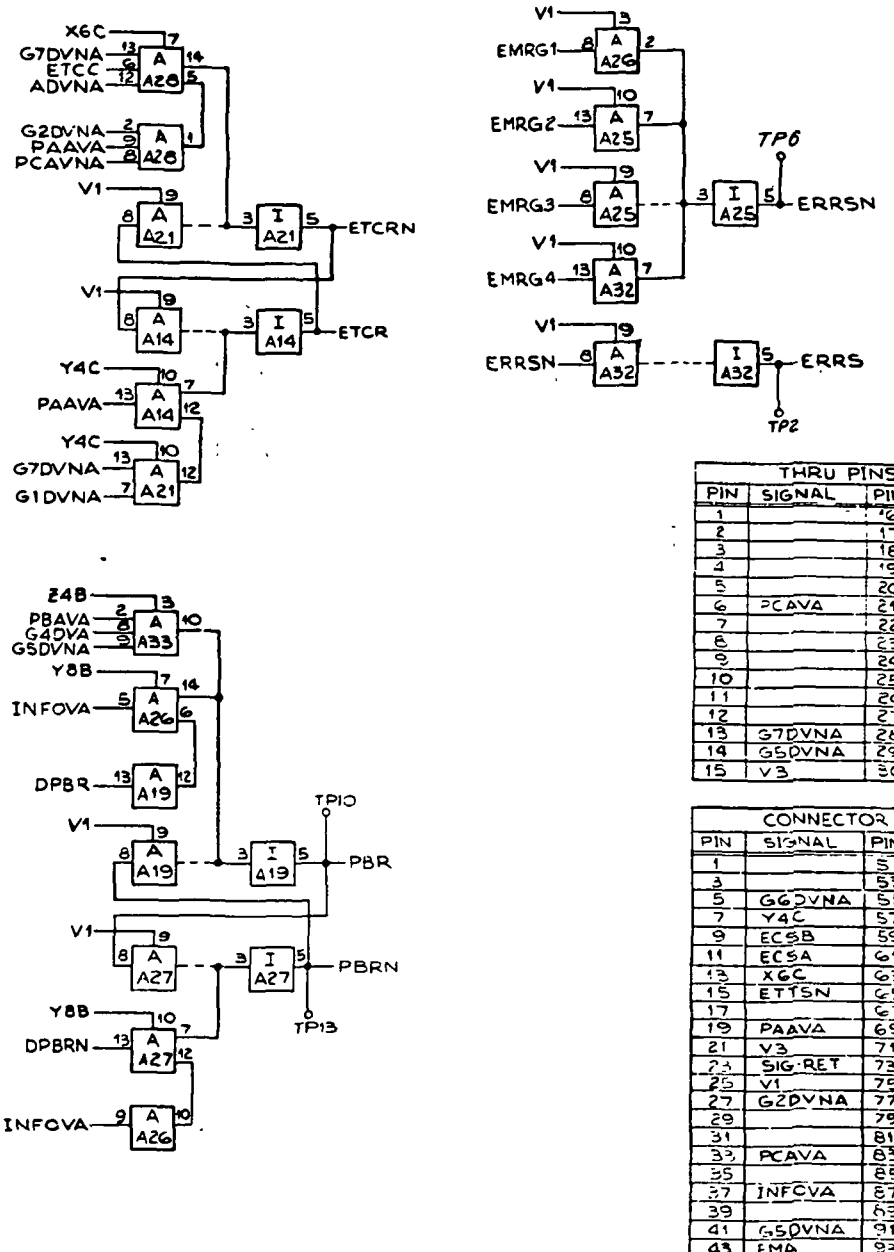


Figure 10-2. Error Processor Logic Diagram (Sheet 5)



THRU PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	X6C
2		17	Z6C
3		18	G4DVA
4		19	ADVA
5		20	G1DVNA
6	PCAVA	21	ADVNA
7		22	
8		23	W6C
9		24	G6DVNA
10		25	PBR
11		26	G2DVNA
12		27	V1
13	G7DVNA	28	SIG-RET
14	G5DVNA	29	PAAVA
15	V3	30	PBRN

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1		51	EMRG2
3		53	ADVNA
5	G6DVNA	55	G7DVNA
7	Y4C	57	EMRG1
9	ECSB	59	Z4B
11	ECSA	61	
13	X6C	63	
15	ETTSN	65	Y8B
17		67	
19	PAAVA	69	ADVA
21	V3	71	ETCCN
23	SIG-RET	73	ETCR
25	V1	75	G1DVNA
27	G2DVNA	77	
29		79	PBAVA
31		81	W4B
33	PCAVA	83	ETCRN
35		85	PCAVNA
37	INFOVA	87	W6C
39		89	G4DVA
41	G5DVNA	91	Z6C
43	EMA	93	ETTS
45		95	ETCC
47	EMRG4	97	
49	EMRG3		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9 AB	A10 I	A11 I	A12	A13 I	A14 I
A15 CLN	A16 AB	A17 I	A18 I	A19 I	A20 I	A21 I
A22 HCI	A23 I	A24 I	A25 I	A26 AB	A27 I	A28 AA
A29 AA	A30 AA	A31 I	A32 I	A33 AA	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A3 Side A.
6. This Drawing Derived From IBM DWG NO. 6112478-B(66126FB)

Figure 10-2. Error Processor Logic Diagram (Sheet 6)

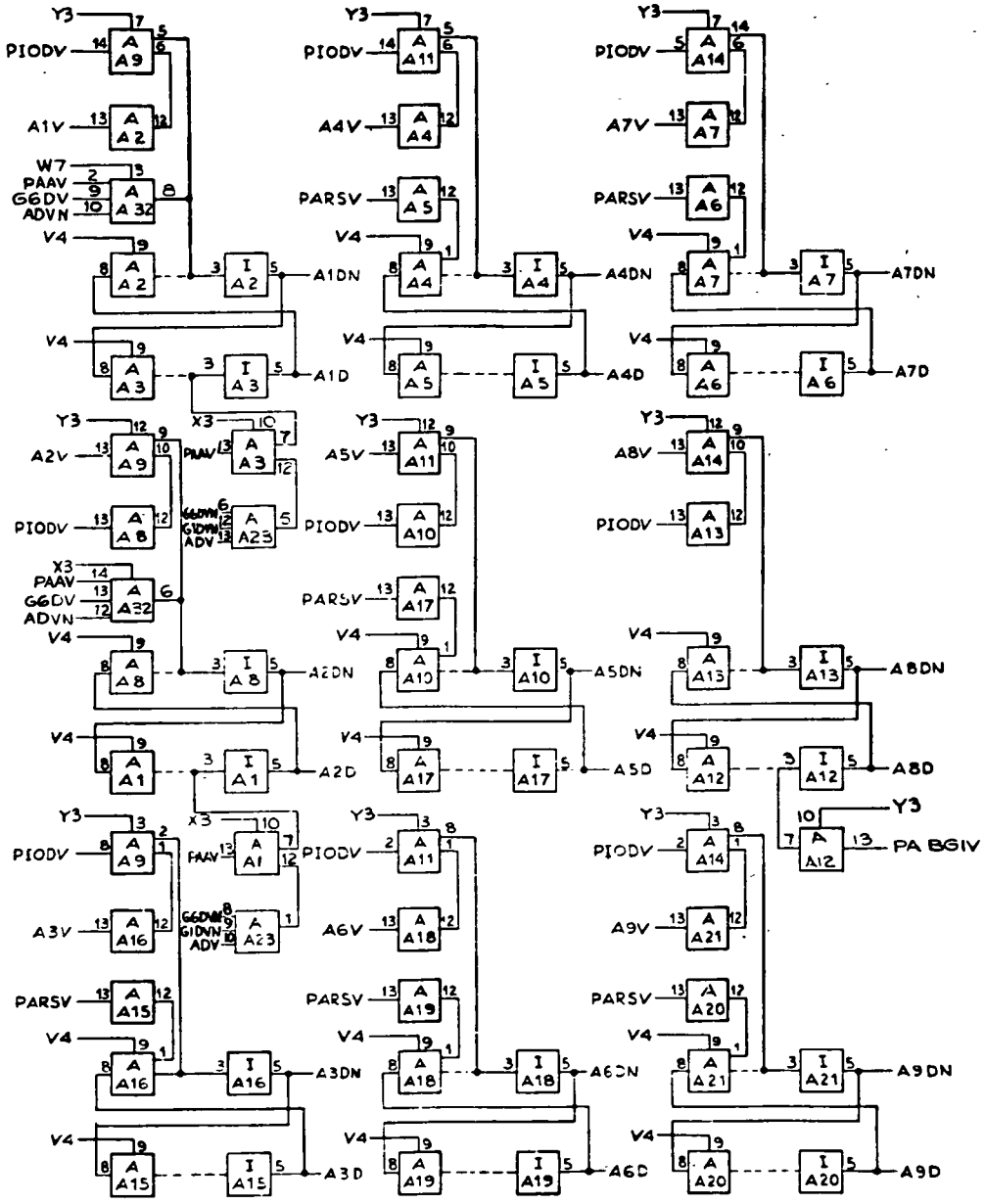
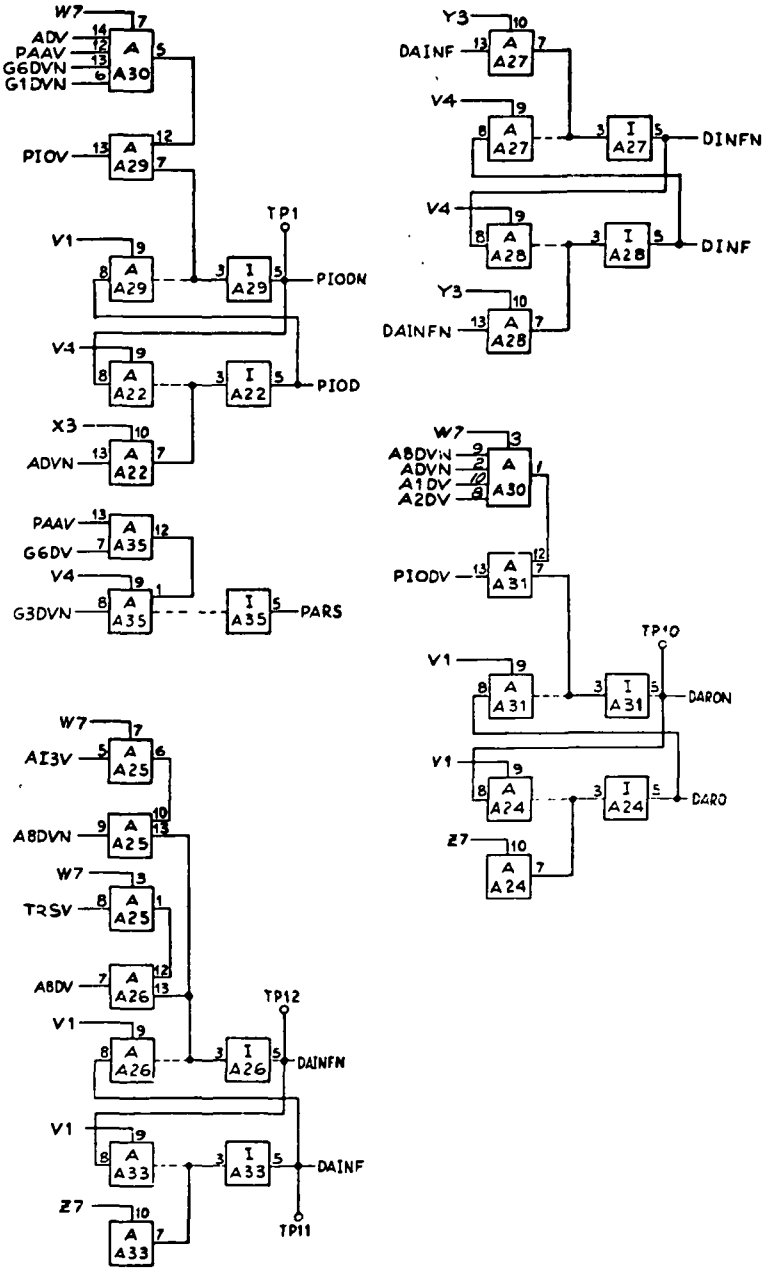


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 1 of 16)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	A2DV	16	ADVN
2	SIG·RET	17	A8DVN
3	V3	18	G1DVN
4	V1	19	PAAV
5		20	A1DV
6		21	PARSV
7		22	X3
8		23	W7
9		24	Z7
10		25	Y3
11		26	PIODV
12		27	V4
13		28	
14		29	
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	A2DN	51	A6V
3	A2D	53	A5V
5	PIOD	55	A4V
7	Y3	57	A4DN
9	A7D	59	A6DN
11		61	A4D
13	PIOV	63	A7DN
15	A1DN	65	A8D
17	A3D	67	A9DN
19	G6DVN	69	DAINF
21	A3V	71	A8DV
23		73	A6D
25	G3DVN	75	A9D
27	V4	77	PABGIV
29	A3DN	79	DINF
31	A2V	81	PARSV
33	A1V	83	PARS
35	DARO	85	DINFN
37	PIODV	87	A8DN
39	A5DN	89	X3
41	A5D	91	A8V
43	A1D	93	G6DV
45	ADV	95	A7V
47	AI3V	97	A9V
49	TRSV		

ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5 I	A6 I	A7 I
A8 I	A9 AB	A10 I	A11 AB	A12 I	A13 I	A14 AB
A15 I	A16 I	A17 I	A18 I	A19 I	A20 I	A21 I
A22 I	A23 AA	A24 I	A25 AB	A26 I	A27 I	A28 I
A29 I	A30 AA	A31 I	A32 AA	A33 I	A34	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A5 Side A, 2A3A16 Side A, 2A3A27 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112258-C(66126DN)

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 2)

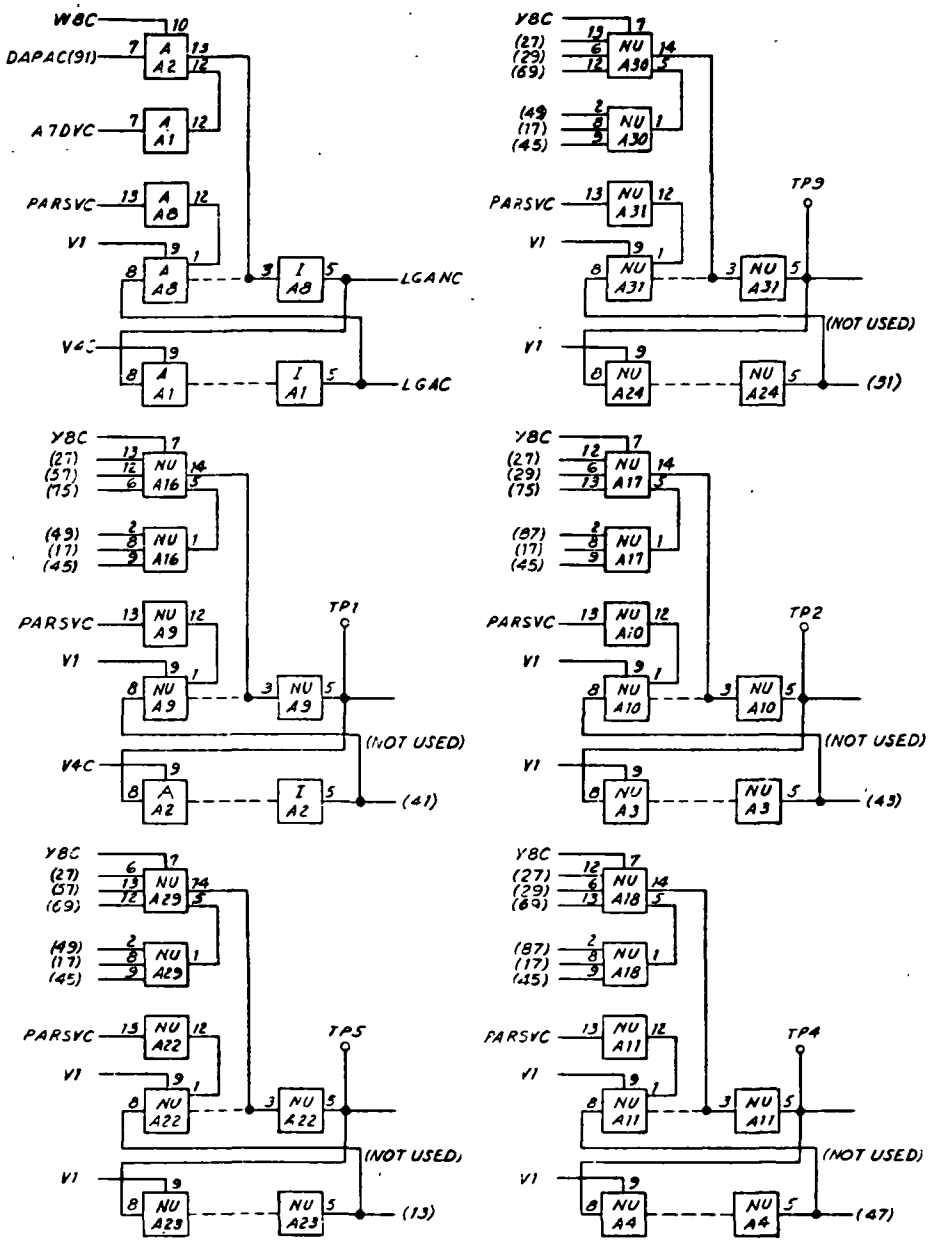
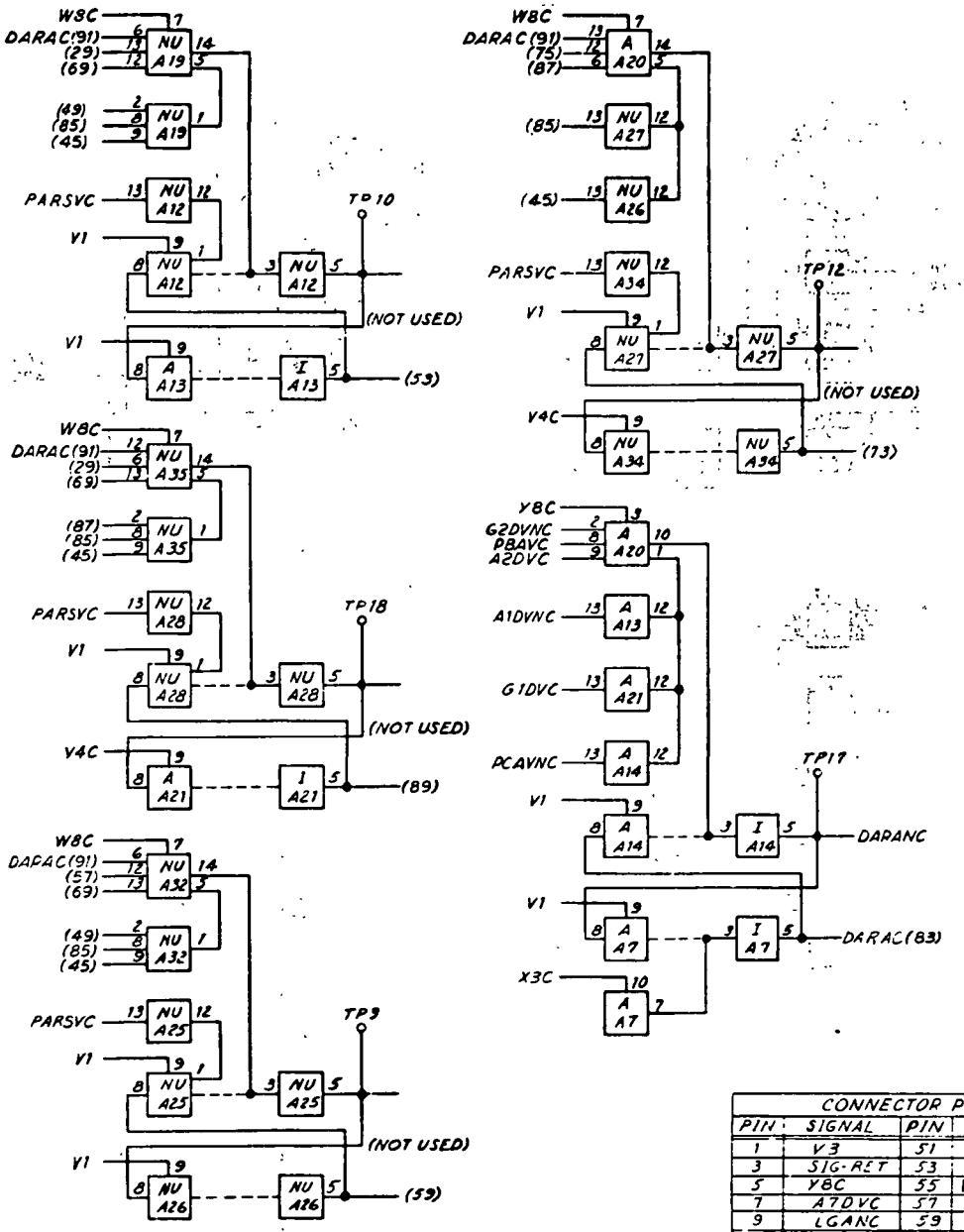


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 3)



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U."-Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A14 Side A.
6. This Drawing Derived From IBM DWG NO. 6112677-REL(66123KL)

ULD LOCATIONS

A1 I	A2 I	A3	A4	A5	A6	A7 I
A8 I	A9	A10	A11	A12	A13 I	A14 I
A15	A16	A17	A18	A19	A20 AA	A21 I
A22	A23	A24	A25	A26	A27	A28
A29	A30	A31	A32	A33	A34	A35

CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
1	V3	51	W8C
3	SIG-RET	53	
5	Y8C	55	PCAVNC
7	A1DVC	57	
9	LGANC	59	
11	LGAC	61	A1DVNC
13		63	A2DVC
15		65	PBAVC
17		67	
19		69	
21		71	V4C
23		73	
25	V1	75	
27		77	G2DVNC
29		79	G1DVC
31		81	PARSVC
33		83	DARAC
35		85	
37		87	
39		89	
41		91	DARAC
43		93	
45		95	
47		97	X3C
49			

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 4)

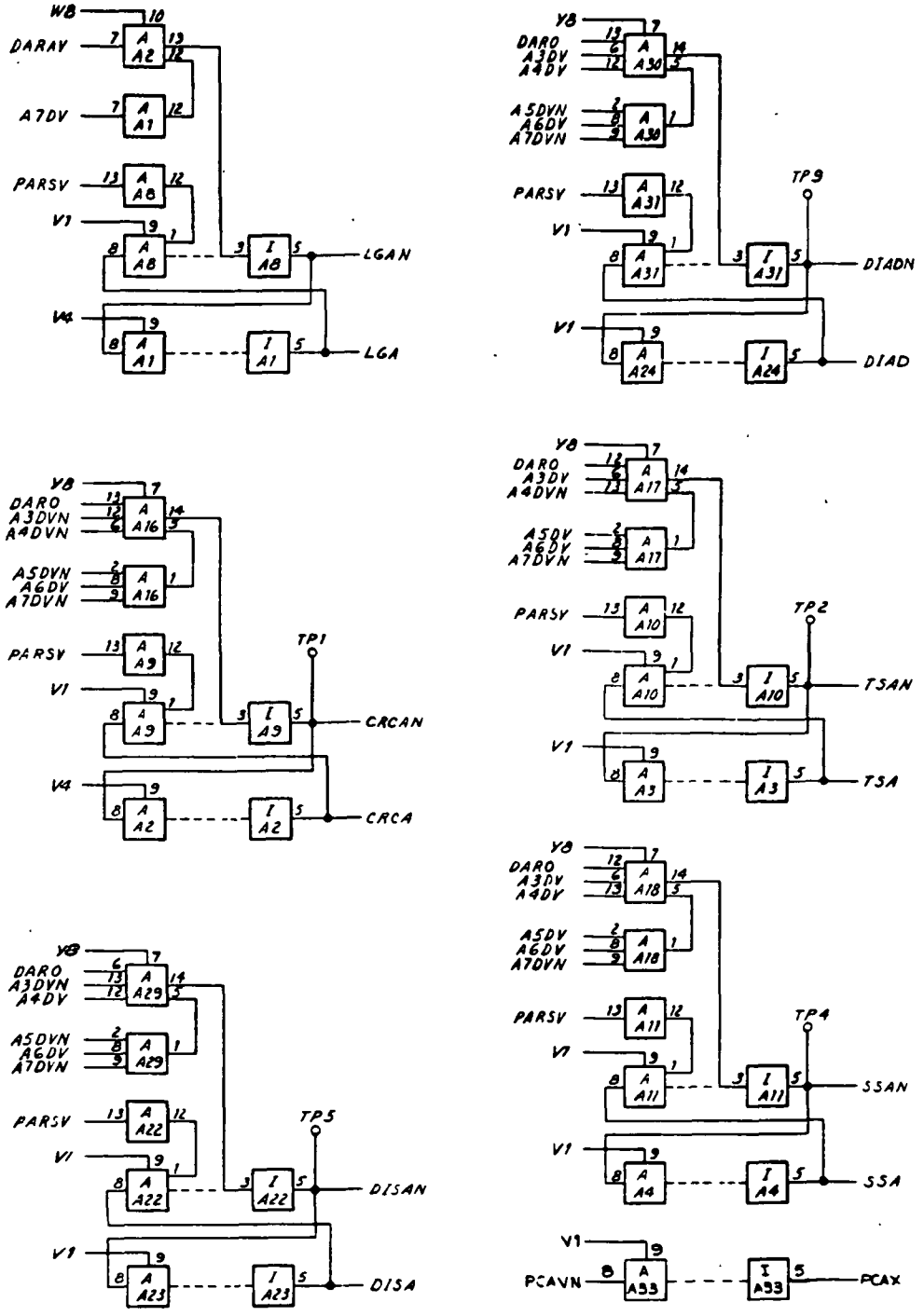
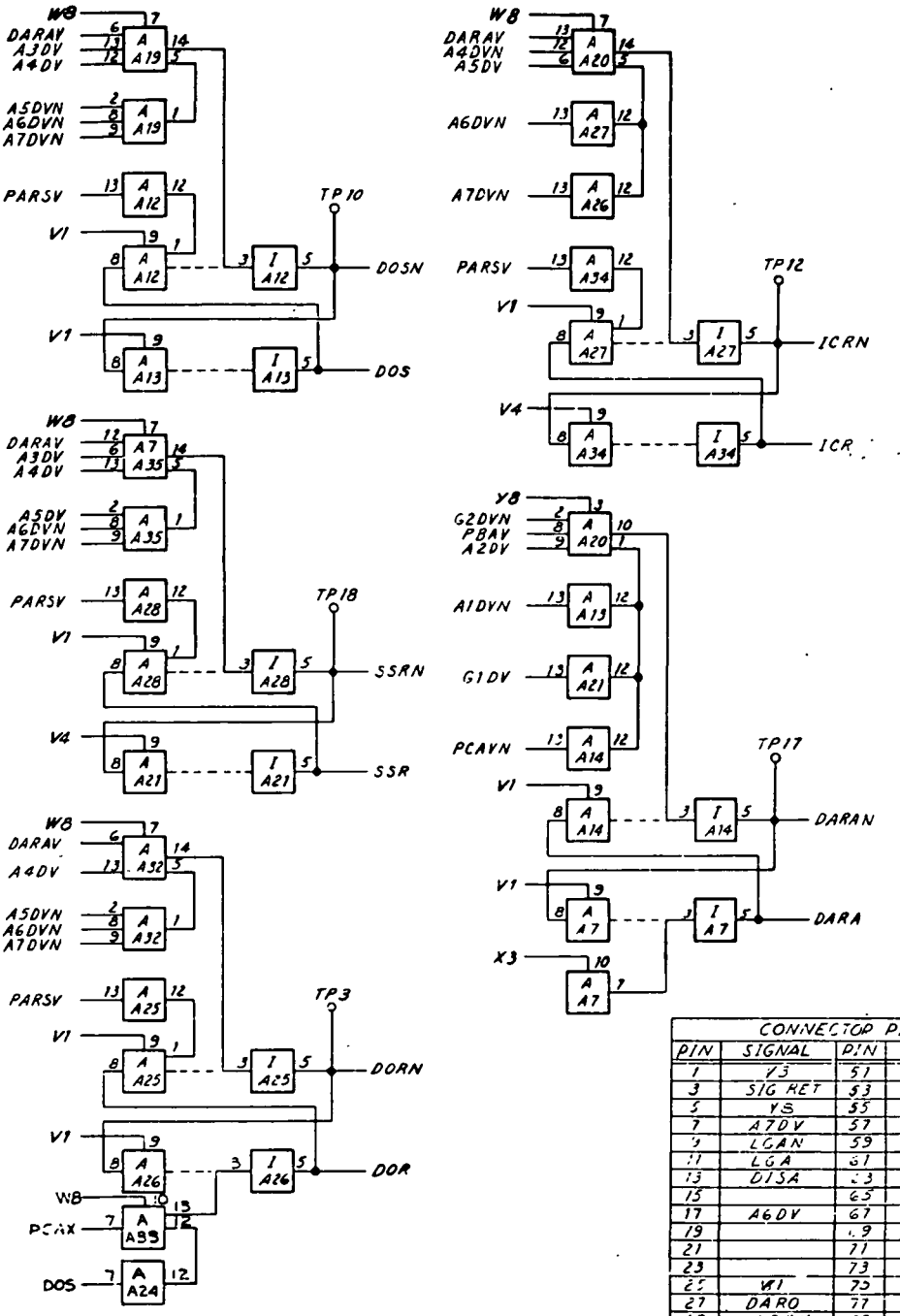


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 5)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	WB
3	SIG RET	53	DOS
5	V5	55	PCAVN
7	A7DV	57	A3DVN
9	LGAN	59	DOR
11	LGA	61	A1DVN
13	DISA	63	A2DV
15		65	PBAV
17	A6DV	67	
19		69	A4DV
21		71	V4
23		73	ICR
25	V81	75	A4DVN
27	DARO	77	G2DVN
29	A3DV	79	G1DV
31	DIAD	81	PARSV
33		83	DARA
35		85	A6DVN
37		87	A5DV
39		89	SSR
41	CRCA	91	DARAV
43	ISA	93	
45	A7DVN	95	
47	SSA	97	X3
49	A5DVN		

ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5	A6	A7 I
A8 I	A9 I	A10 I	A11 I	A12 I	A13 I	A14 I
A15	A15 AA	A17 AA	A18 AA	A19 AA	A20 AA	A21 I
A22 I	A23 I	A24 I	A25 I	A26 I	A27 I	A28 I
A29 AA	A30 AA	A31 I	A32 AA	A33 I	A34 I	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A3 Side A, 2A3A14 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112158-A(66126FB)

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 6)

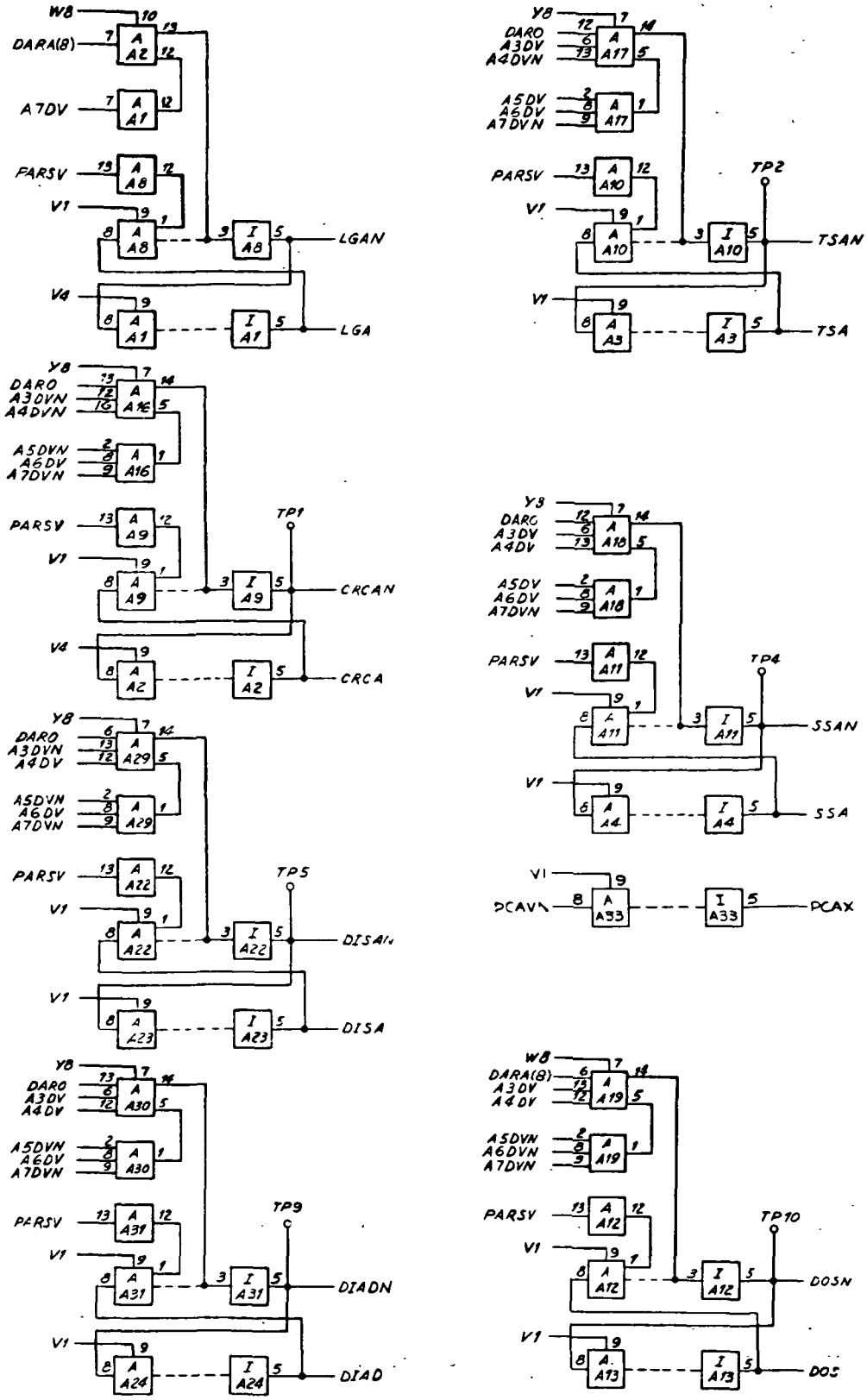
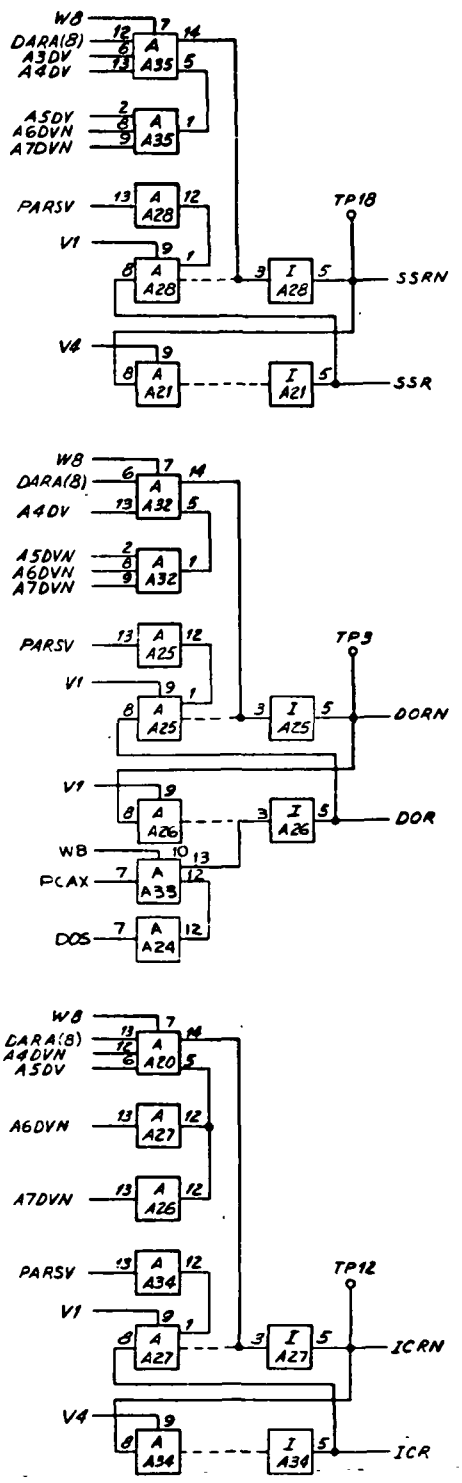
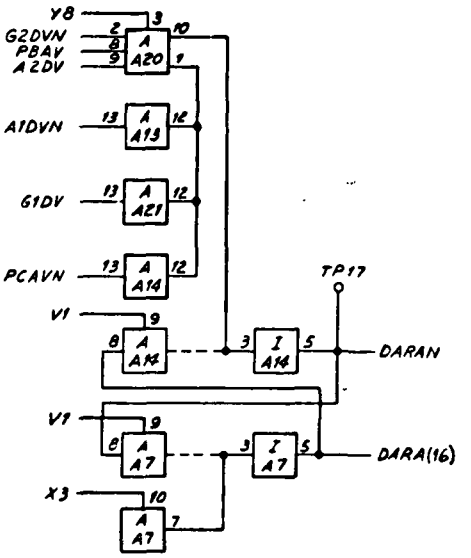


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 7)





ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5	A6	A7 I
A8 I	A9 I	A10 I	A11 I	A12 I	A13 I	A14 I
A15	A16 AA	A17 AA	A18 AA	A19 AA	A20 AA	A21 I
A22 I	A23 I	A24 I	A25 I	A26 I	A27 I	A28 I
A29 AA	A30 AA	A31 I	A32 AA	A33 I	A34 I	A35 AA

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	X3	52	SSA
4		54	A7DVN
6		56	TSA
8	DARA	58	CRCA
10	SSR	60	
12	A5DV	62	
14	A6DVN	64	
16	DARA	66	
18	PAPSV	68	DIAD
20	G1DV	70	A3DV
22	G2DVN	72	DARO
24	A4DVN	74	V1
26	ICR	76	
28	V4	78	
30	A4DV	80	
32		82	A6DV
34	PBAV	84	
36	A2DV	86	DISA
38	A1DVN	88	LGA
40	DCR	90	LGAR
42	A3DVN	92	A7DV
44	PCAVN	94	Y8
46	DOS	96	SIG-RET
48	WB	98	V3
50	A5DVN		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A3 Side B.
6. This Drawing Derived From IBM DWG NO. 6112157-A(66126FB)

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 8)

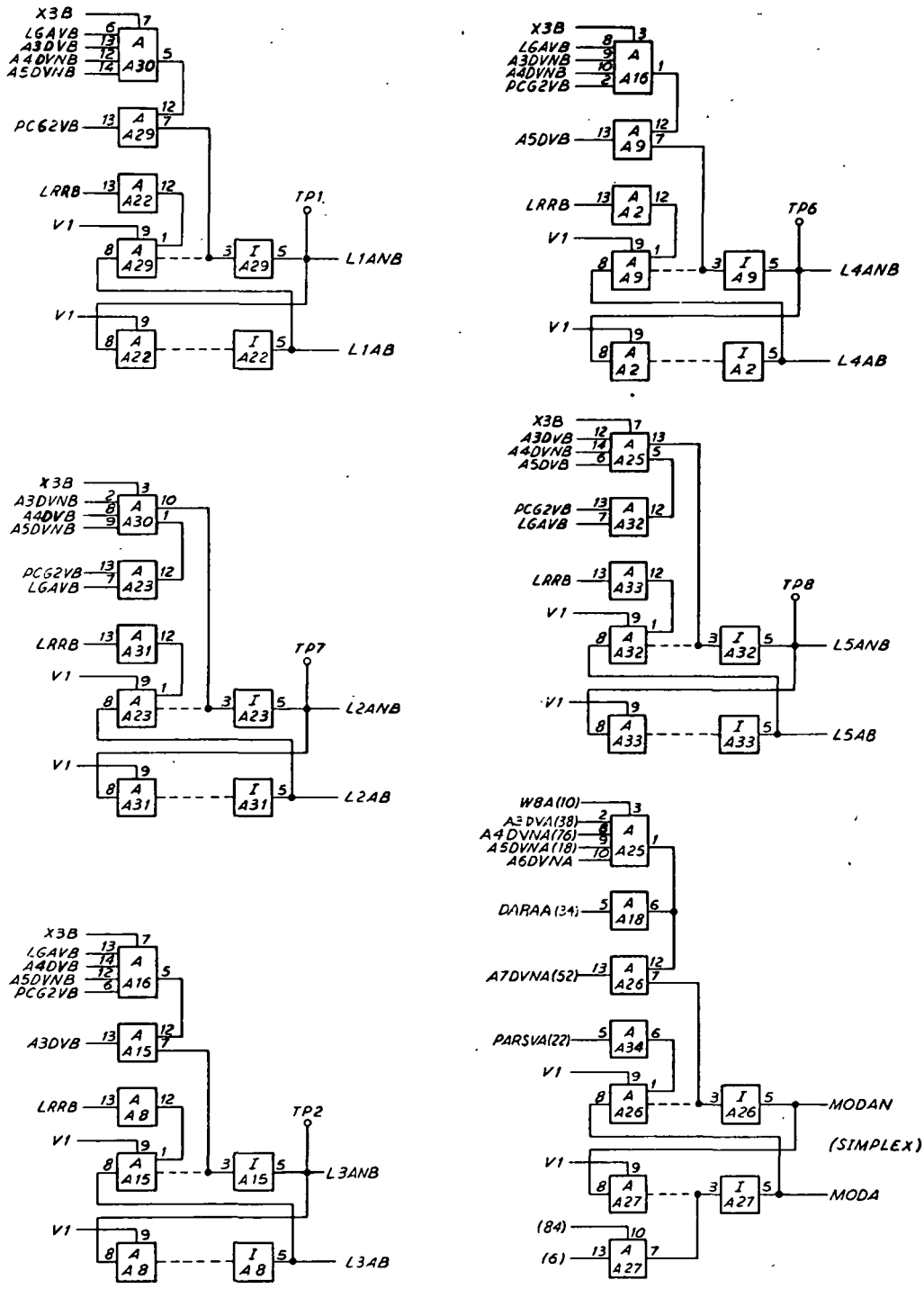
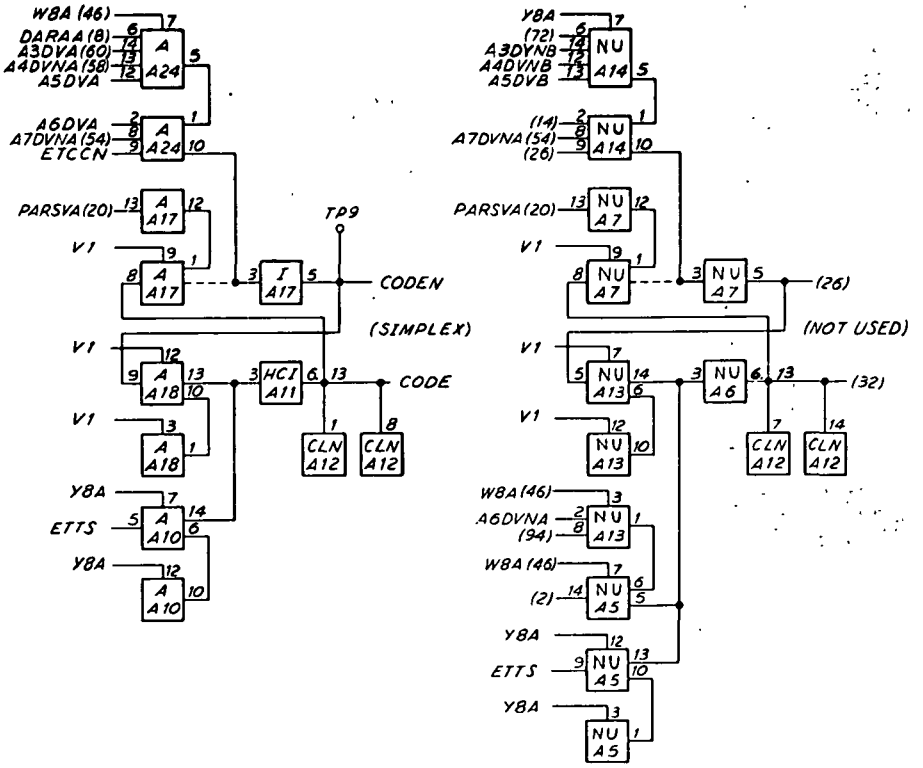


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 9)



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A24 Side B.
6. This Drawing Derived From IBM DWG NO. 6112278-A(66123TF)

ULD LOCATIONS

A1	A2 I	A3	A4	A5	A6	A7
A8 I	A9 I	A10 A6	A11 HCI	A12 CLN	A13	A14
A15 I	A16 AA	A17 I	A18 AB	A19	A20	A21
A22 I	A23 I	A24 AA	A25 AA	A26 I	A27 I	A28
A29 I	A30 AA	A31 I	A32 I	A33 I	A34 AB	A35

CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
2		52	A7DVNA
4	A3B	54	A7DVNA
6		56	L5AB
8	DJRAA	58	A4DVNA
10	W8A	60	A3DVA
12	A5DVB	62	A5DVA
14		64	PCG2VB
16		66	LRRB
18	A5DVNA	68	L2AB
20	PARSVA	70	A3DVB
22	PARSVA	72	
24	A4DVNB	74	A6DVNA
26		76	A4DVNA
28	MODAN	78	ETCCN
30	A4DVB	80	V3
32		82	A6DVA
34	DARAA	84	
36	ETTS	86	L1AB
38	A3DVA	88	CODE
40	V1	90	Y8A
42	MODA	92	SIG-RET
44	A3DVNB	94	
46	W8A	96	L3AB
48	LGAVB	98	L4AB
50	A5DVNB		

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 10)

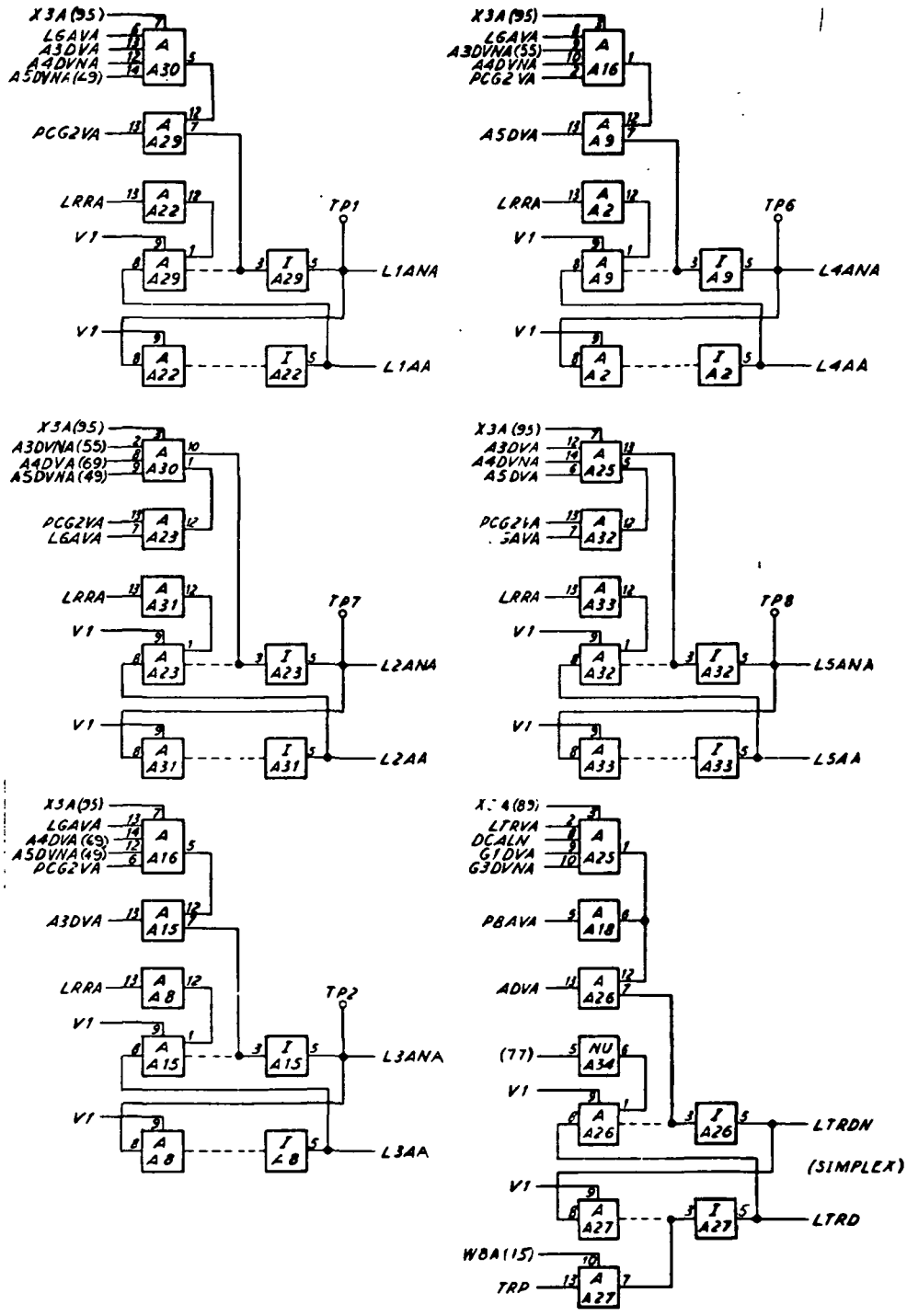
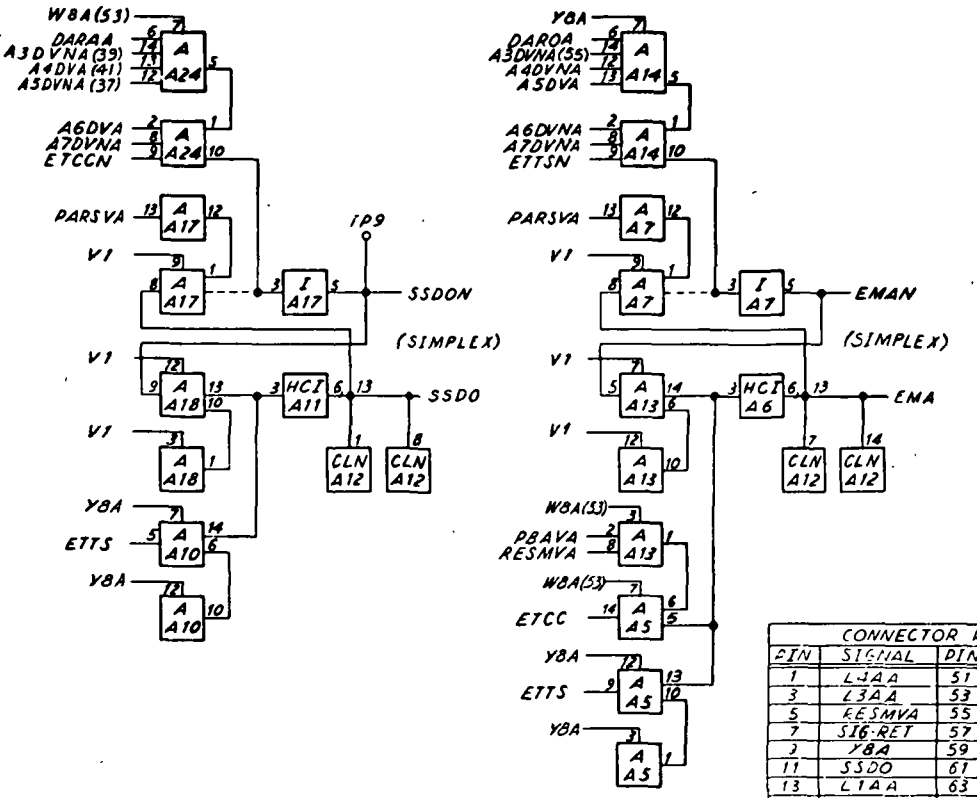


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 11)



ULD LOCATIONS

A1	A2 I	A3	A4	A5 AB	A6 HCI	A7 I
A8 I	A9 I	A10 AB	A11 HCI	A12 CLN	A13 AB	A14 AA
A15 I	A16 AA	A17 I	A18 AB	A19	A20	A21
A22 I	A23 I	A24 AA	A25 AA	A26 I	A27 I	A28
A29 I	A30 AA	A31 I	A32 I	A33 I	A34	A35

CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
1	L4AA	51	LGAVA
3	L3AA	53	W8A
5	EESMVA	55	A3DVNA
7	SIG-RET	57	LTRD
9	Y8A	59	V1
11	SSDO	61	LTRVA
13	L1AA	63	ETTS
15	W8A	65	PBAVA
17	A6DVA	67	EMA
19	V3	69	A4DVA
21	ETCCN	71	LTRDN
23	DCALN	73	ETTSN
25	G3DVNA	75	A4DVNA
27	DAROA	77	
29	A3DVA	79	PARSVA
31	L2AA	81	G1DVA
33	LRRA	83	EMAN
35	PCG2VA	85	A6DVNA
37	A5DVNA	87	A5DVA
39	A3DVNA	89	X3A
41	A4DVA	91	DARAA
43	L5AA	93	TRP
45	A7DVNA	95	X9A
47	ADVA	97	ETCC
49	A5DVNA		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A24 Side A.
6. This Drawing Derived From IBM DWG NO. 6112277-A(66123TF)

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 12)

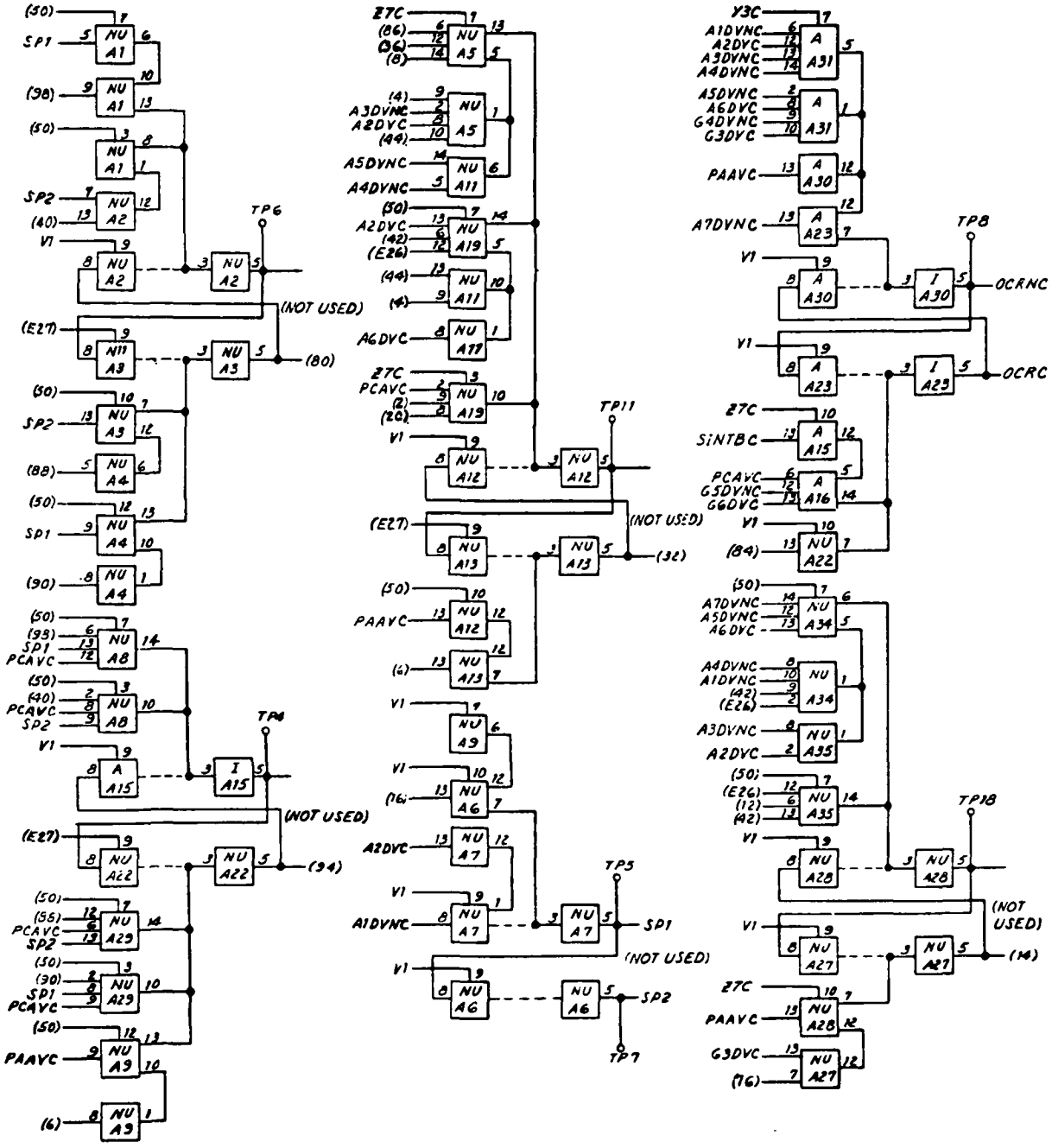
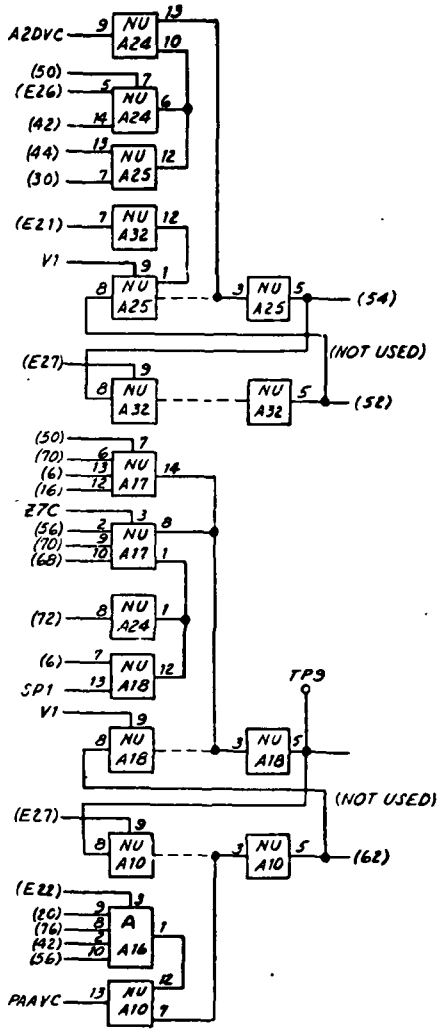


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 13)



THRU PINS			
PIN	SIGNAL	PIN	SIGNAL
1	A2DVC	16	(42)
2	SIG RET	17	(4)
3	V3	18	(2)
4	V1	19	PAAVC
5		20	(44)
6		21	
7		22	
8		23	(50)
9		24	27C
10		25	13C
11		26	
12		27	
13		28	
14		29	
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4		54	
6		56	
8		58	A3DVNC
10	27C	60	A1DVNC
12		62	
14		64	A2DVC
16		66	PCAVC
18	A6DVC	68	
20		70	
22	G5DVNC	72	
24	G4DVNC	74	OCRC
26	G3DVC	76	
28	SIG-RET	78	A4DVNC
30		80	
32		82	SINTBC
34	V3	84	
36		86	
38	PAAVC	88	
40		90	
42		92	G6DVC
44		94	
46	A7DVNC	96	V1
48	A5DVNC	98	
50		7	V3C

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9	A10	A11	A12	A13	A14
A15 I	A16 AA	A17	A18	A19	A20	A21
A22	A23 I	A24	A25	A26	A27	A28
A29	A30 I	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A27 Side B.
6. This Drawing Derived From IBM DWG NO. 6112679-REL(66123KL)

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 14)

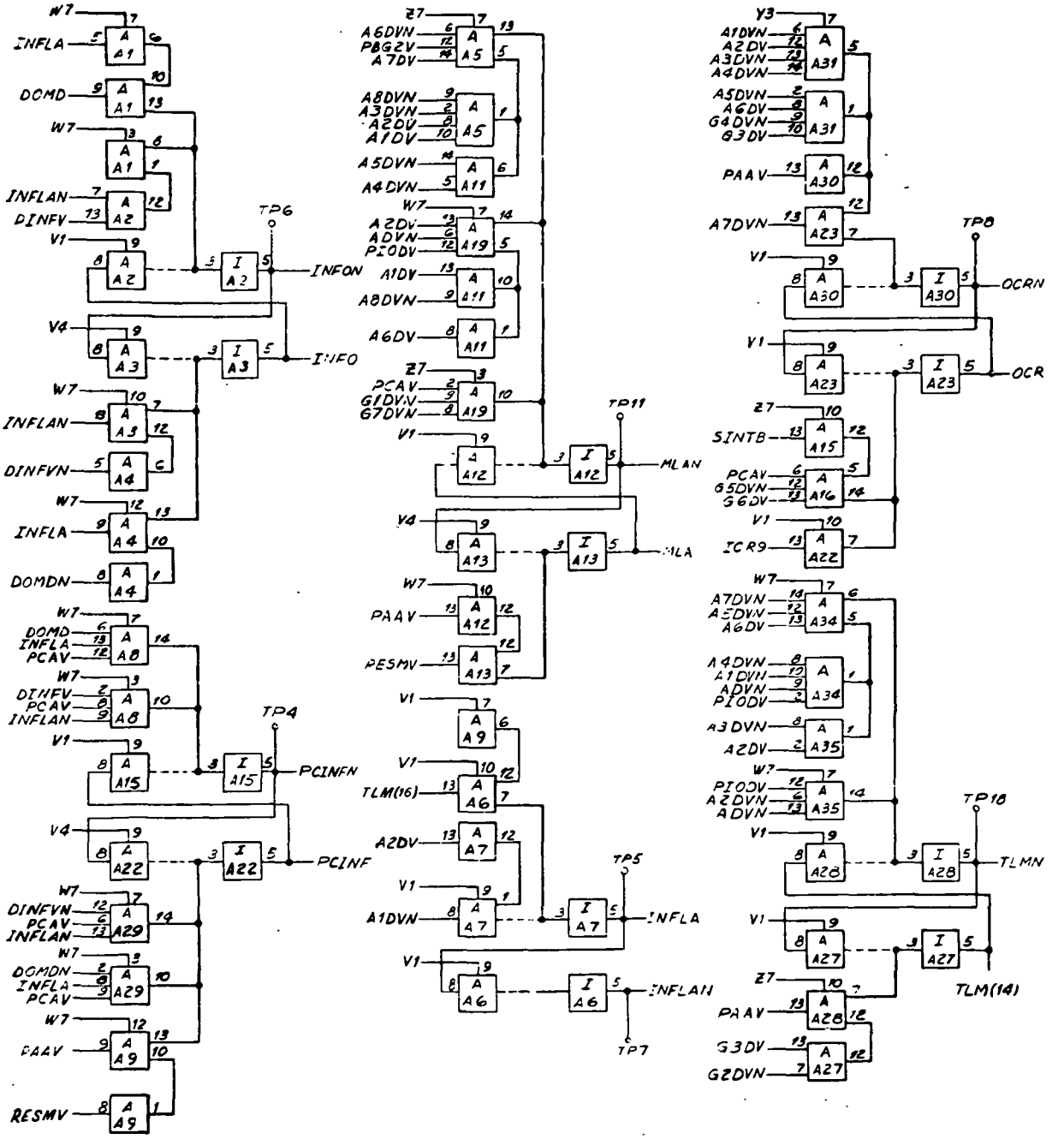
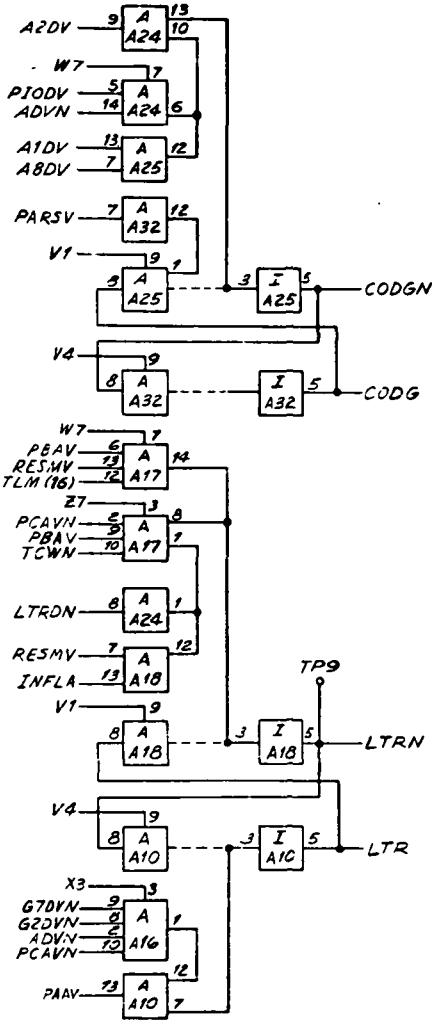


Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 15)



THRU PINS			
PIN	SIGNAL	PIN	SIGNAL
1	A2DV	16	ADVN
2	SIG·RET	17	A8DVN
3	V3	18	G1DVN
4	V1	19	PAAV
5		20	A1DV
6		21	PARSV
7		22	X3
8		23	W7
9		24	Z7
10		25	Y3
11		26	P10DV
12		27	V4
13		28	
14		29	
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	G1DVN	52	CODG
4	A8DVN	54	CODGN
6	RESMV	56	PCAVN
8	A7DV	58	A3DVN
10	Z7	60	A1DVN
12	A2DVN	62	LTR
14	TLM	64	A2DV
16	TLM	66	PCAV
18	AGDV	68	TCWN
20	G7DVN	70	PBAV
22	G5DVN	72	LTRDN
24	G4DVN	74	OCR
26	G3DV	76	G2DVN
28	SIG·RET	78	A4DVN
30	A8DV	80	INFO
32	MLA	82	SINTB
34	V3	84	ICR9
36	PARSV	86	A5DVN
38	PAAV	88	DINFVN
40	DINFV	90	DOMDN
42	ADVN	92	G6DV
44	A1DV	94	PCINF
46	A7DVN	96	V1
48	A5DVN	98	DOMD
50	W7		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A5 Side B, 2A3A16 Side B, 2A3A27 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112268-REL(66123AT)

ULD LOCATIONS

A1 AB	A2 I	A3 I	A4 AB	A5 AA	A6 I	A7 I
A8 AA	A9 AB	A10 I	A11 AB	A12 I	A13 I	A14
A15 I	A16 AA	A17 AA	A18 I	A19 AA	A20	A21
A22 I	A23 I	A24 AB	A25 I	A26	A27 I	A28 I
A29 AA	A30 I	A31 AA	A32 I	A33	A34 AA	A35 AA

Figure 10-3. Address Decode and Computer Data Select Logic Diagram (Sheet 16)

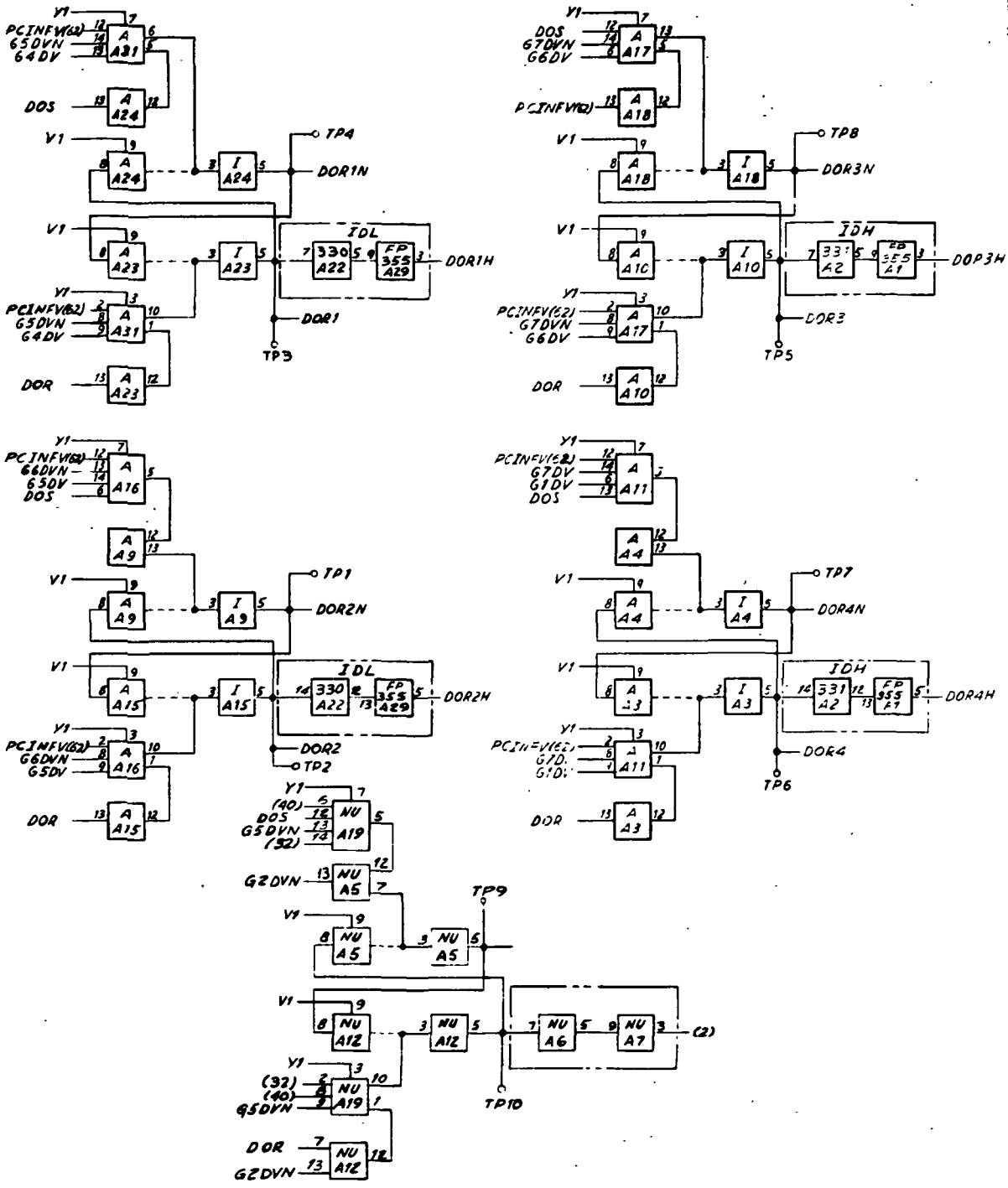
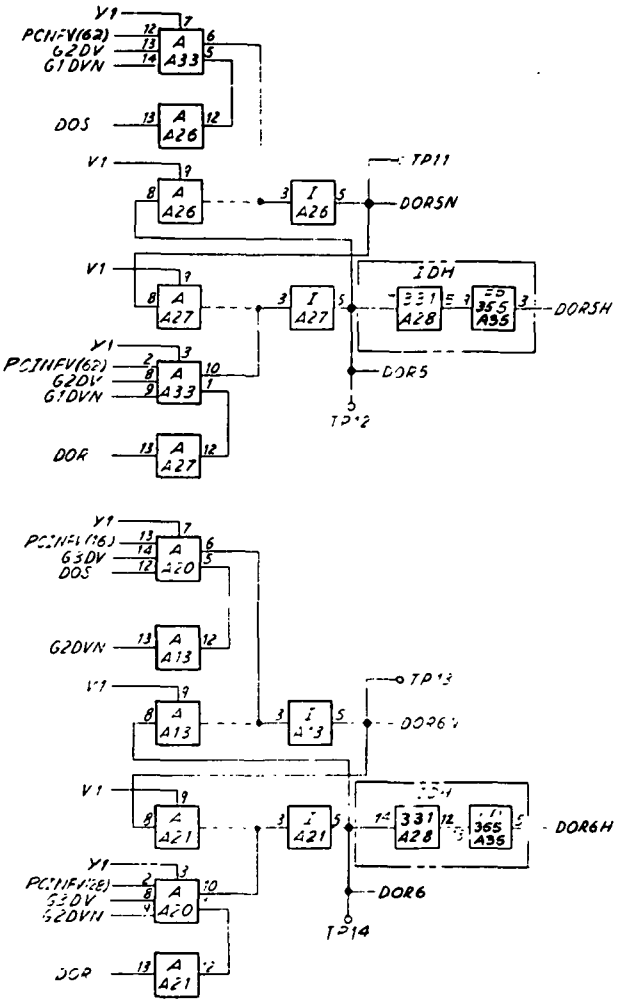


Figure 10-4. Discrete Output Register Logic Diagram (Sheet 1 of 10)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	I1
4	DOR6H	54	
6		56	G1DV
8		58	DOS
10		60	G5DVN
12		62	PCINFV
14	DOR3H	64	
16	DORJH	66	G7DVN
18	G3DV	68	G4DV
20		70	
22		72	G6DV
24		74	G5DV
26		76	V1
28	PCINFV	78	
30	G2DVN	80	
32		82	G3DVN
34	G1DVN	84	DOR1H
36		86	DOR2H
38		88	
40		90	DOR3H
42	G2DV	92	DORJH
44	G7DV	94	V2
46		96	SIG-RET
48		98	V3

ULD LOCATIONS

A1 A28 A35	A2 A33	A3 I	A4	A5	A6	A7
A8	A9 I	A10	A11 A2	A12	A13	A14
A15 I	A16 A2	A17 A2	A18 I	A19	A20 A2	A21 I
A22 A35	A23 I	A24	A25	A26	A27 I	A28 A33
A29 A28 A35	A30	A31 AA	A32	A33 A2	A34	A35 A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A4 Side B, 2A1A5 Side B, 2A1A6 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112148-REL(66123F)

Figure 10-4. Discrete Output Register Logic Diagram (Sheet 2)

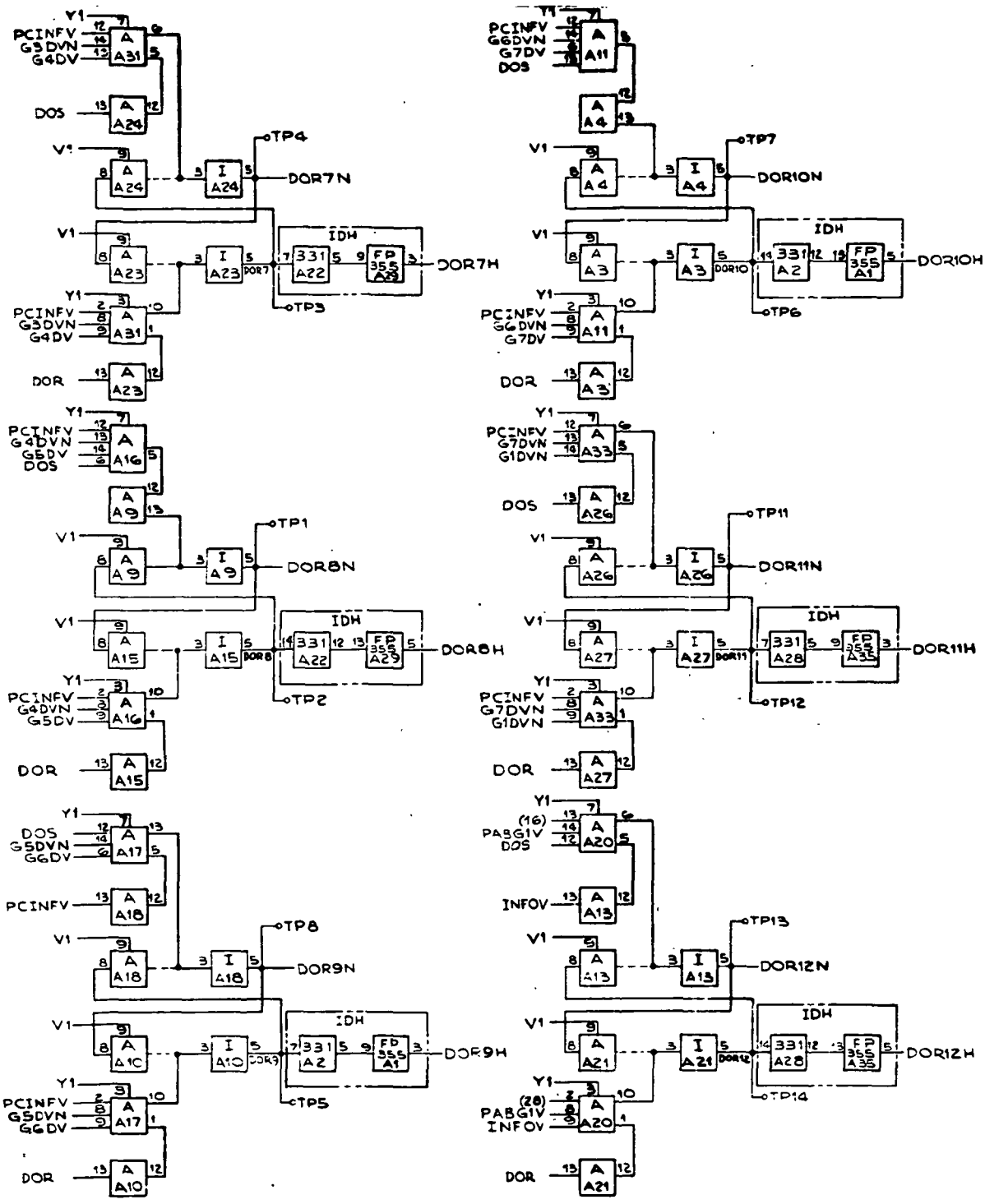
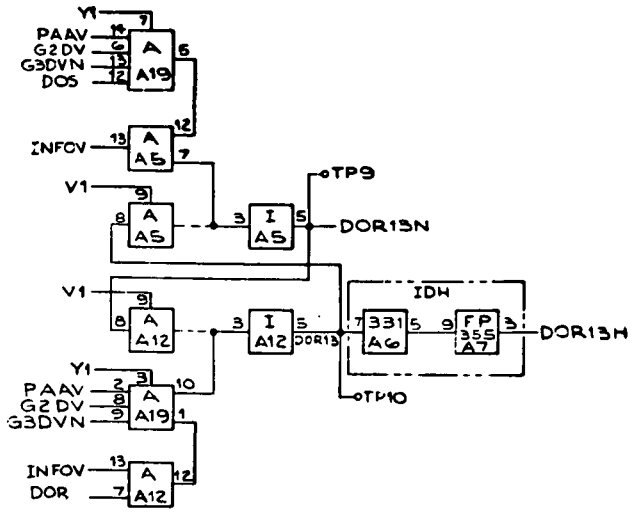


Figure 10-4. Discrete Output Register Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	
3	SIG-RET	53	
5	V20	55	G6DVN
7	DOR10H	57	G7DVN
9	DOR9H	59	G2DV
11		61	
13	DOR8H	63	
15	DOR7H	65	G1DVN
17	G4DVN	67	PAAV
19		69	INFOV
21		71	
23	V1	73	
25	G5DV	75	
27	G6DV	77	
29	DOR	79	
31	G4DV	81	PABG1V
33	G5DVN	83	
35		85	DOR11H
37	DCINFV	87	
39	G3DVN	89	
41	DOS	91	
43	G7DV	93	
45		95	DOR12H
47	V1	97	DOR13H
49			

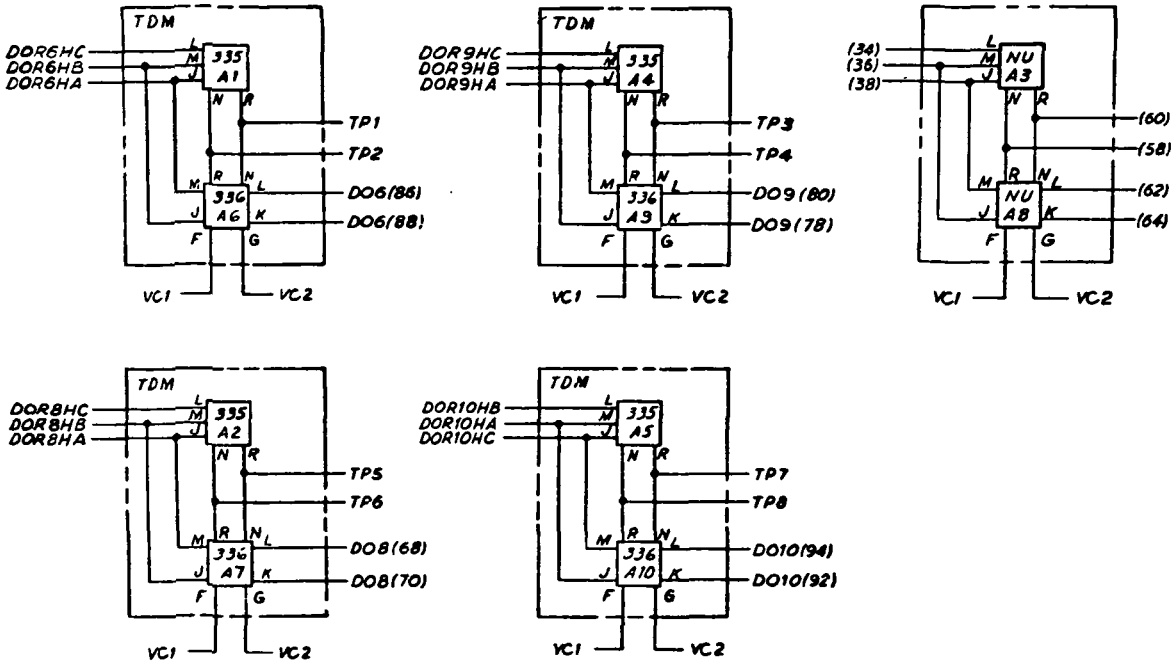
ULD LOCATIONS

A1 FP 355	A2 331	A3 I	A4 I	A5 I	A6 331	A7 FP 355
A8	A9 I	A10 I	A11 AA	A12 I	A13 I	A14
A15 I	A16 AA	A17 AA	A18 I	A19 AA	A20 AA	A21 I
A22 331	A23 I	A24 I	A25	A26 I	A27 I	A28 331
A29 FP 355	A30	A31 AA	A32	A33 AA	A34	A35 FP 355

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A4 Side A, 2A1A5 Side A, 2A1A6 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112147-REL(66123KL)

Figure 10-4. Discrete Output Register Logic Diagram (Sheet 4)

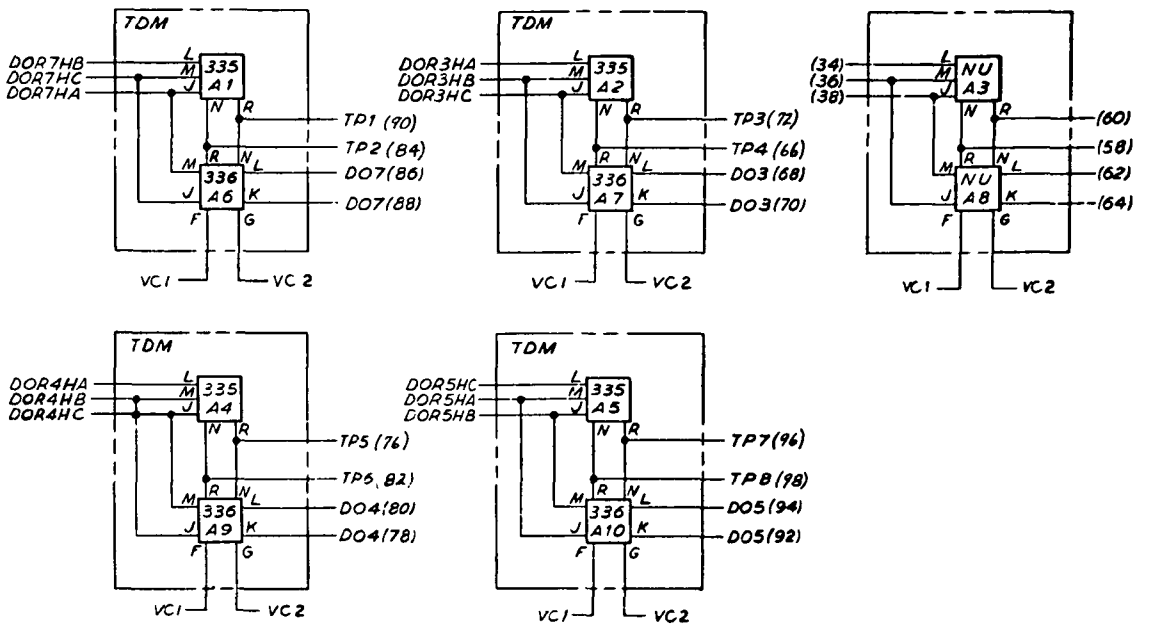


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	DOR5HA	52	VEE
4	DOR5HC	54	VEE
6	DOP5HE	56	VC2
8		58	
10	DOP10HC	60	
12	DOR10HB	62	
14	DOR10HA	64	
16		66	TP5
18		68	DO8
20	DOR9HC	70	DO8
22	DOR9HA	72	TP5
24	DOR9HB	74	
26		76	TP3
28		78	DO9
30		80	DO9
32		82	TP4
34		84	TP2
36		86	DO6
38		88	DO6
40	VC2	90	TP1
42	VC1	92	DO10
44	DOR8HC	94	DO10
46	DOR8HA	96	TP7
48	DOR8HB	98	TP8
50	VC1		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A3.
6. This Drawing Derived From IBM DWG NO. 6112687-A(6612685)

Figure 10-4. Discrete Output Register Logic Diagram (Sheet 5)



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A9.
6. This Drawing Derived From IBM DWG NO. 6112689-A(66126BS)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	DOR7HA	52	VEE
4	DOR7HB	54	VEE
6	DOR7HC	56	VC2
8		58	
10	DOR5HB	60	
12	DOR5HC	62	
14	DOR5HA	64	
16		66	TP4
18		68	DO3
20	DOR4HA	70	DO3
22	DOR4HC	72	TP3
24	DOR4HB	74	
26		76	TP5
28		78	DO4
30		80	DO4
32		82	TP6
34		84	TP2
36		86	DO7
38		88	DO7
40	VC2	90	TP1
42	VC1	92	DO5
44	DOR3HA	94	DO5
46	DOR3HC	96	TP7
48	DOR3HB	98	TP8
50	VC1		

Figure 10-4. Discrete Output Register Logic Diagram (Sheet 6)

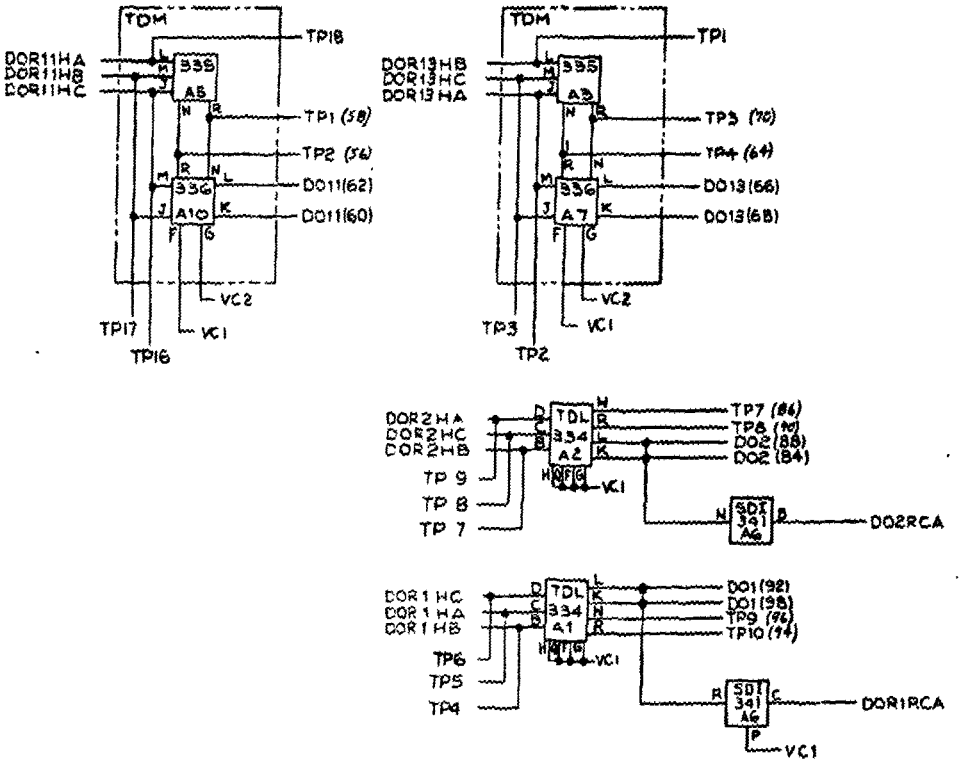
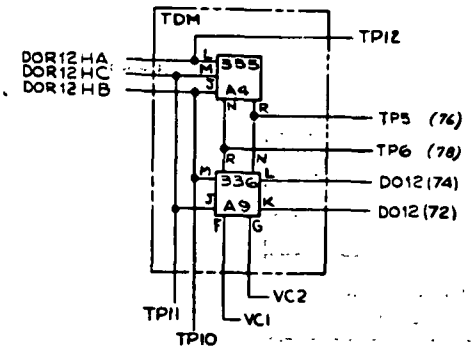


Figure 10-4. Discrete Output Register Logic Diagram (Sheet 7)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	DOR1HB	52	VC1
4	DOR1HA	54	VC2
6	DOR1HC	56	TP2
8	DOR2HB	58	TP1
10	DOR2HC	60	DO11
12	DOR2HA	62	DO11
14	DOR11HC	64	TP4
16		66	DO13
18	DOR11HA	68	DO13
20		70	TP3
22	DOR11HB	72	DO12
24		74	DO12
26	DOR12HA	76	TP5
28	DOR12HB	78	TP6
30	DOR12HC	80	DO2RCA
32		82	DO1RCA
34	DOR13HB	84	DO2
36	DOR13HA	86	TP7
38	DOR13HC	88	DO2
40	VC2	90	TP8
42	SIG-RET	92	DO1
44	V7	94	TP10
46	VEE	96	TP9
48	VEE	98	DO1
50	VC1		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A12.
6. This Drawing Derived From IBM DWG NO. 6112678-A(66126BR)

Figure 10-4. Discrete Output Register Logic Diagram (Sheet 8)

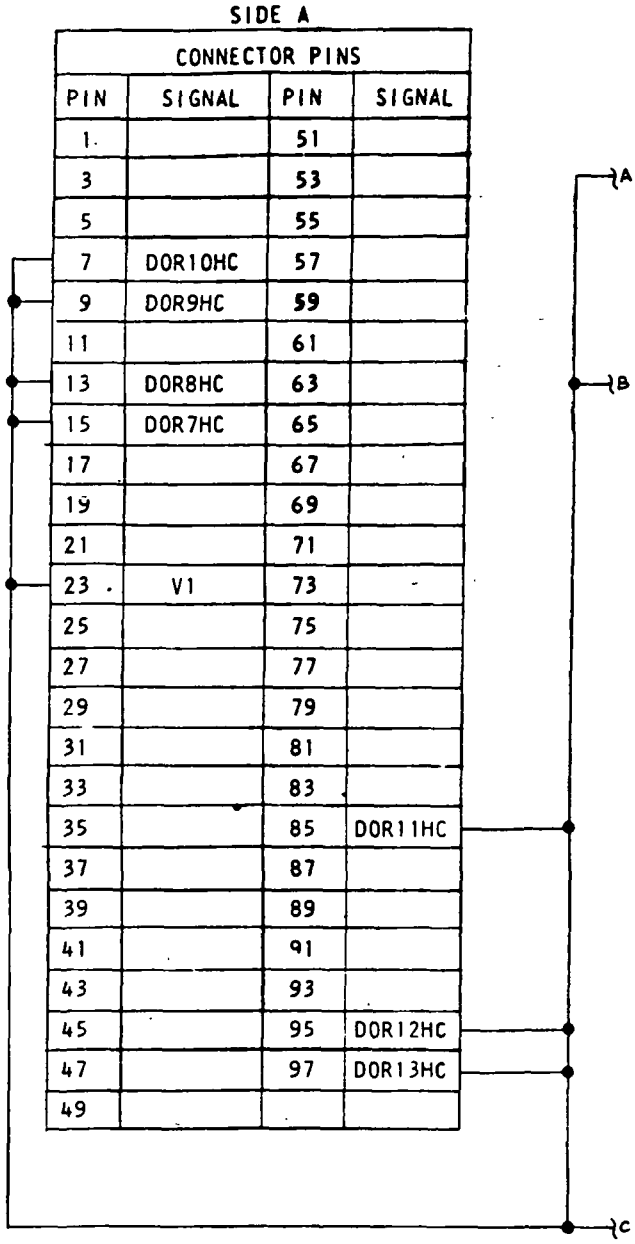
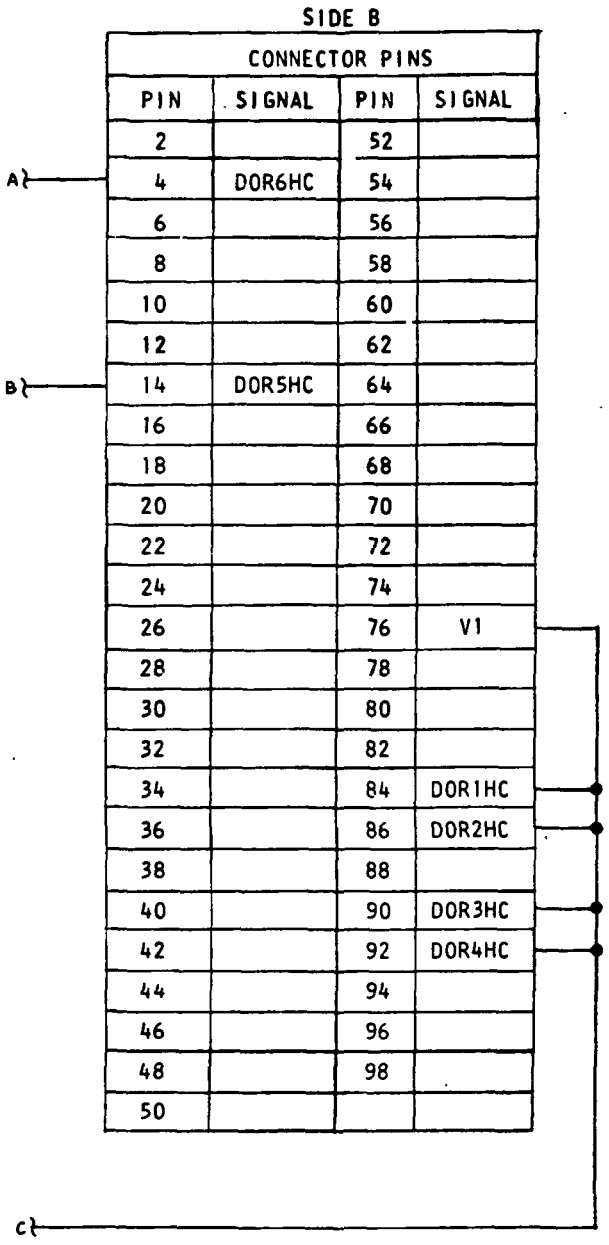


Figure 10-4. Discrete Output Register Logic Diagram (Sheet 9)



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A6.
6. This Drawing Derived From IBM DWG NO. 6112759-REL(66126HM)

Figure 10-4. Discrete Output Register Logic Diagram (Sheet 10)

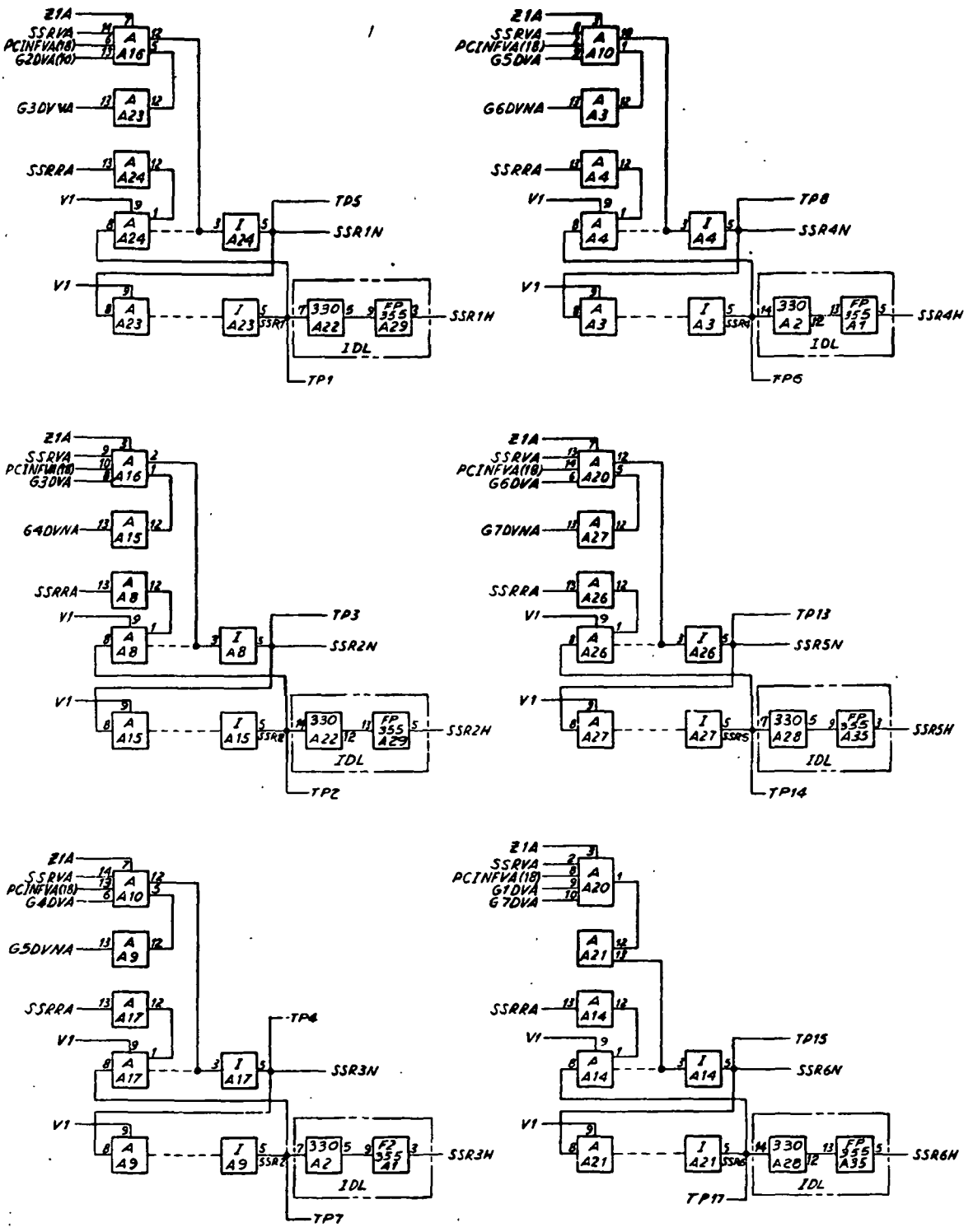
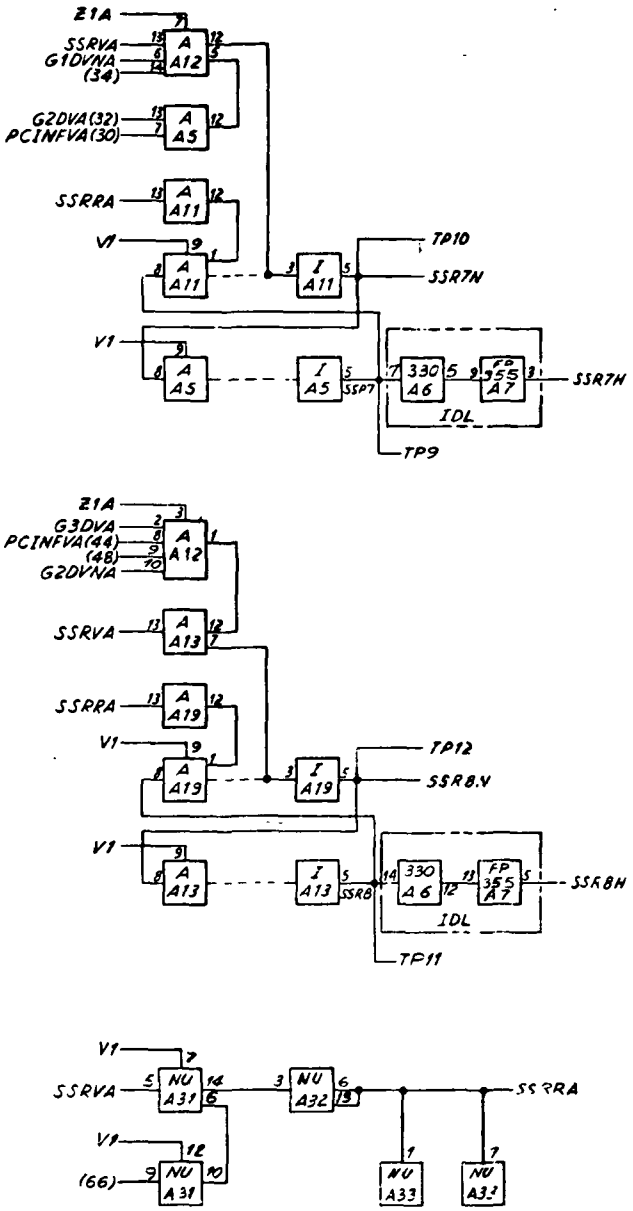


Figure 10-5. Switch Selector Register Logic Diagram (Sheet 1 of 8)



ULD LOCATIONS

A1 FP 355	A2 330	A3 I	A4 I	A5 I	A6 330	A7 FP 355
A8 I	A9 I	A10 AA	A11 I	A12 AA	A13 I	A14 I
A15 I	A16 AA	A17 I	A18	A19 I	A20 AA	A21 I
A22 330	A23 I	A24 I	A25	A26 I	A27 I	A28 330
A29 FP 355	A30	A31	A32	A33	A34	A35 FP 355

CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
2	SSR7H	52	
4	SSP8H	54	G6DVNA
6		56	G4DVA
8		58	G5DVA
10	SSR6H	60	V1
12	SSR5H	62	
14	SSRVA	64	Z1A
16	G6DVA	66	
18	PCINFVA	68	G5DVNA
20	G7DVNA	70	G2DVA
22	G7DVA	72	G3DVNA
24		74	
26		76	
28	G1DVA	78	
30	PCINFVA	80	
32	G2DVA	82	G3DVA
34		84	G4DVNA
36		86	SSR3H
38	SSRRA	88	V20A
40		90	SSR4H
42	G2DVNA	92	SIG-RET
44	PCINFVA	94	SSR1H
46	G1DVNA	96	SSR2H
48		98	V3
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A18 Side B.
6. This Drawing Derived From IBM DWG NO. 6112178-REL(66123E)

Figure 10-5. Switch Selector Register Logic Diagram (Sheet 2)

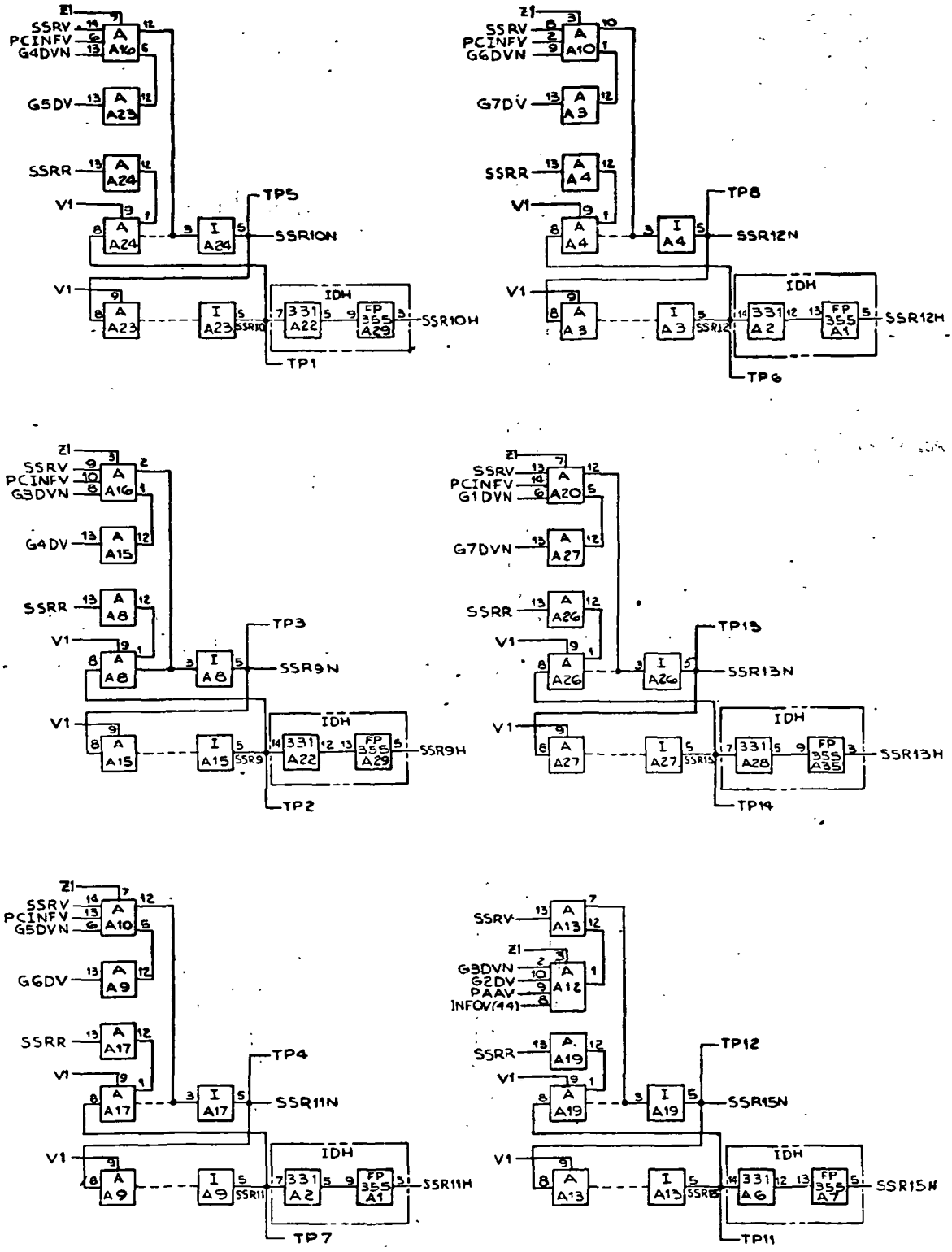
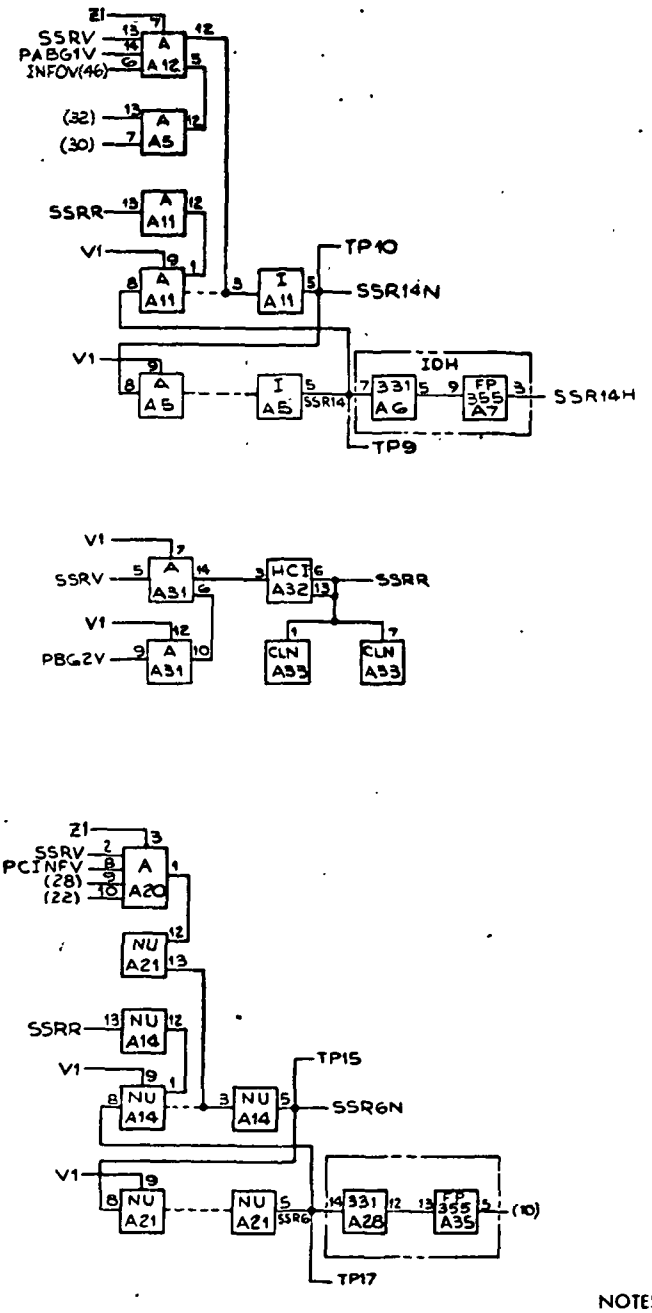


Figure 10-5. Switch Selector Register Logic Diagram (Sheet 3)



A1 FP 355	A2 331	A3 I	A4 I	A5 I	A6 331	A7 FP 355
A8 I	A9 I	A10 AA	A11 I	A12 AA	A13 I	A14
A15 I	A16 AA	A17 I	A18	A19 I	A20 AA	A21
A22 331	A23 I	A24 I	A25	A26 I	A27 I	A28 331
A29 FP 355	A30	A31 AB	A32 HCI	A33 CLN	A34	A35 FP 355

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	SSR14H	52	
4	SSR15H	54	G7DV
6		56	G5DVN
8		58	G6DVN
10		60	V1
12	SSR13H	62	
14	SSRV	64	Z1
16	G1DVN	66	PBG2V
18	PCINFV	68	G6DV
20	G7DVN	70	G4DVN
22		72	G5DV
24		74	
26		76	
28		78	
30		80	
32	PABG1V	82	G3DVN
34		84	G4DV
36		86	SSR11H
38	SSRR	88	V20
40		90	SSR12H
42	G2DV	92	SIG-RET
44	INFOV	94	SSR10H
46	INFOV	96	SSR9H
48	PAAV	98	V3
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A17 Side B.
6. This Drawing Derived From IBM DWG NO. 6112179-A(66123TF)

Figure 10-5. Switch Selector Register Logic Diagram (Sheet 4)

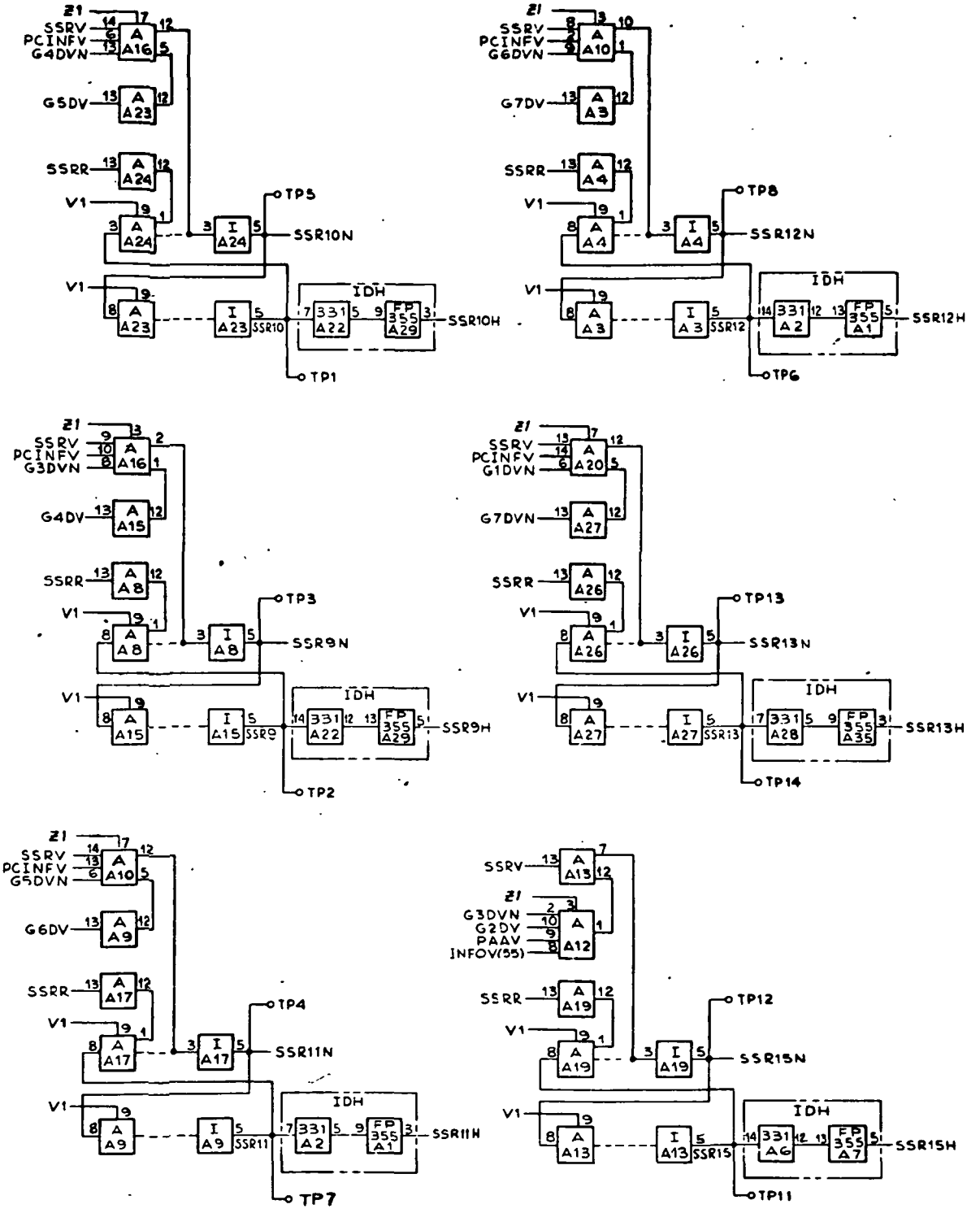
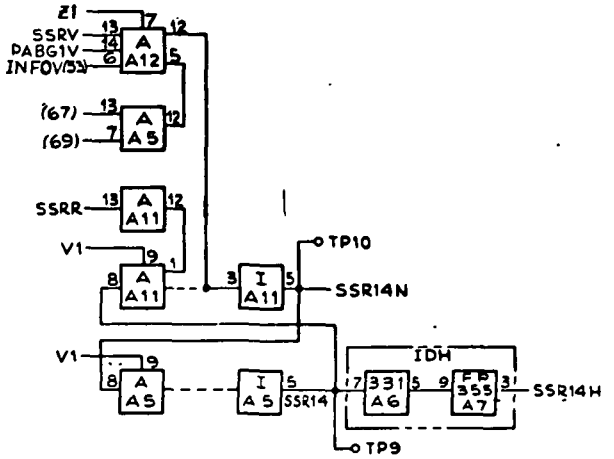
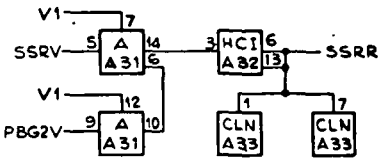
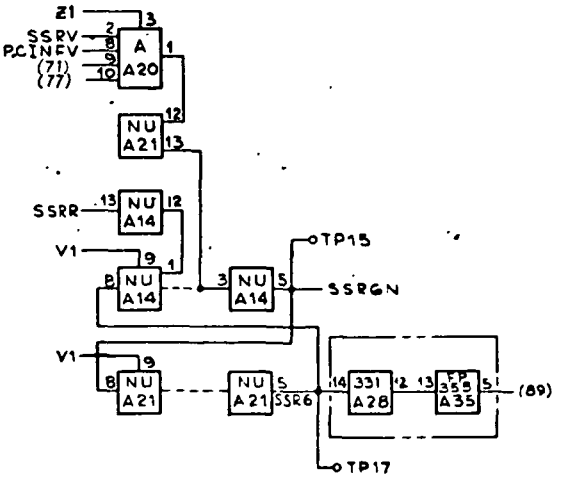


Figure 10-5. Switch Selector Register Logic Diagram (Sheet 5)







ULD LOCATIONS

A1 FP 355	A2 331	A3 I	A4 I	A5 I	A6 331	A7 FP 355
A8 I	A9 I	A10 AA	A11 I	A12 AA	A13 I	A14
A15 I	A16 AA	A17 I	A18	A19 I	A20 AA	A21
A22 331	A23 I	A24 I	A25	A26 I	A27 I	A28 331
A29 FP 355	A30	A31 AB	A32 HCI	A33 CLN	A34	A35 FP 355

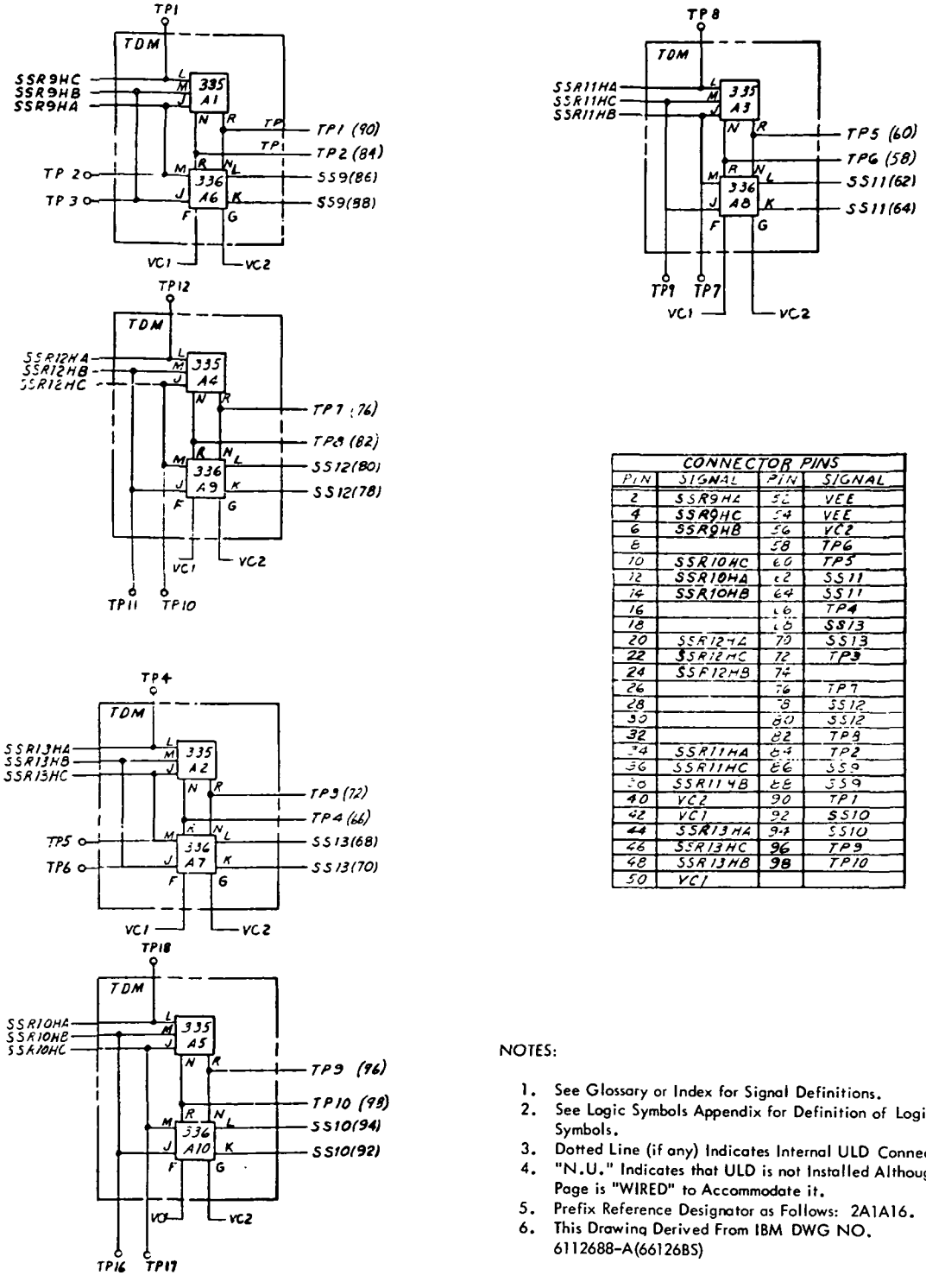
CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
1	V3	51	PAAV
3	SSR9H	53	INFOV
5	SSR10H	55	INFOV
7	SIG-RET	57	G2DV
9	SSR12H	59	
11	V20	61	SSRR
13	SSR11H	63	
15	G4DV	65	
17	G3DVN	67	PABG1V
19		69	
21		71	
23		73	
25		75	
27	G5DV	77	
29	G4DVN	79	G7DVN
31	G6DV	81	PCINFV
33	PBG2V	83	G1DVN
35	Z1	85	SSRV
37		87	SSR13H
39	V1	89	
41	G6DVN	91	
43	G5DVN	93	
45	G7DV	95	SSR15H
47		97	SSR14H
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A17 Side A, 2A1A18 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112177-A(66123TF)

Figure 10-5. Switch Selector Register Logic Diagram (Sheet 6)

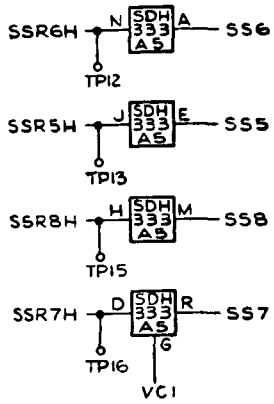


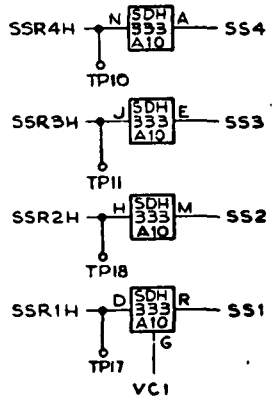
CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	SSR9HA	52	VEE
4	SSR9HC	54	VEE
6	SSR9HB	56	VC2
8		58	TP6
10	SSR10HC	60	TP5
12	SSR10HA	62	SS11
14	SSR10HB	64	SS11
16		66	TP4
18		68	SS13
20	SSR12HA	70	SS13
22	SSR12HC	72	TP3
24	SSR12HB	74	
26		76	TP7
28		78	SS12
30		80	SS12
32		82	TP8
34	SSR11HA	84	TP2
36	SSR11HC	86	SS9
38	SSR11HB	88	SS9
40	VC2	90	TP1
42	VC1	92	SS10
44	SSR13HA	94	SS10
46	SSR13HC	96	TP9
48	SSR13HB	98	TP10
50	VC1		

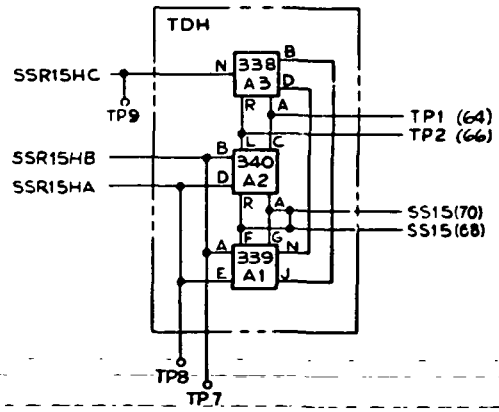
NOTES:

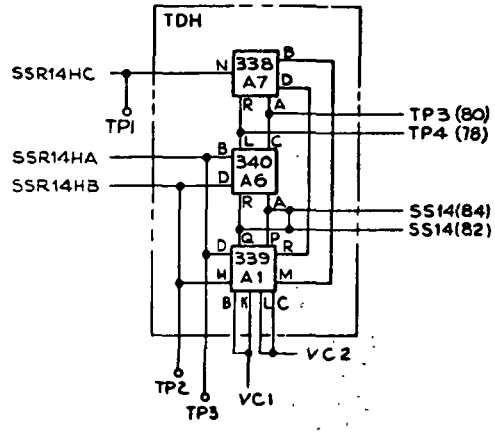
1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A16.
6. This Drawing Derived From IBM DWG NO. 6112688-A(66126BS)

Figure 10-5. Switch Selector Register Logic Diagram (Sheet 7)









NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A27.
6. This Drawing Derived From IBM DWG NO. 6112738-A(66126BS)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	VEE
4		54	VEE
6	SSR1H	56	SS1
8	SSR2H	58	SS2
10	SSR3H	60	SS3
12	SSR4H	62	SS4
14		64	TP1
16		66	TP2
18	SSR6H	68	SS15
20	SSR5H	70	SS15
22	SSR7H	72	
24	SSR8H	74	
26		76	
28		78	TP4
30	SSR15HA	80	TP3
32	SSR15HB	82	SS14
34	SSR15HC	84	SS14
36		86	
38	SSR14HB	88	
40	SSR14HA	90	
42	SSR14HC	92	SS8
44	VC2	94	SS7
46	VC2	96	SS5
48	VC1	98	SS6
50	VC1		

Figure 10-5. Switch Selector Register Logic Diagram (Sheet 8)

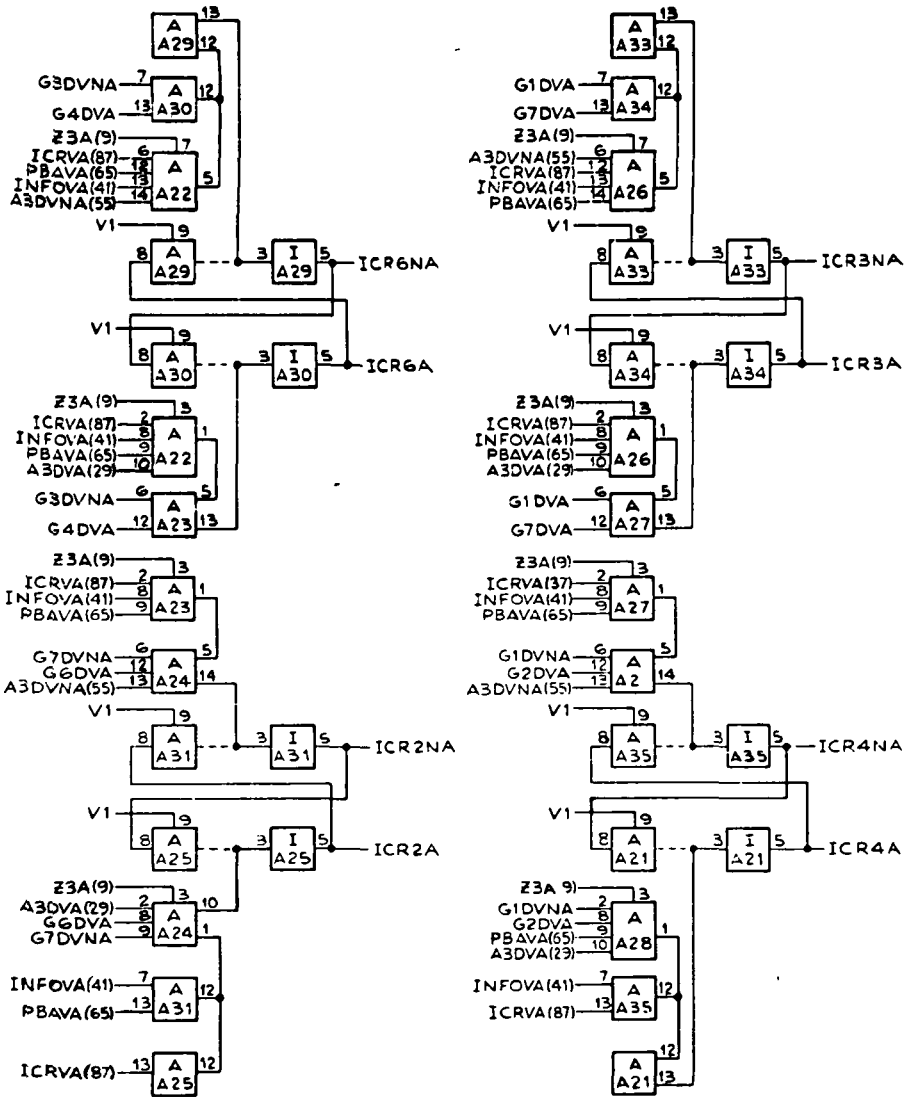
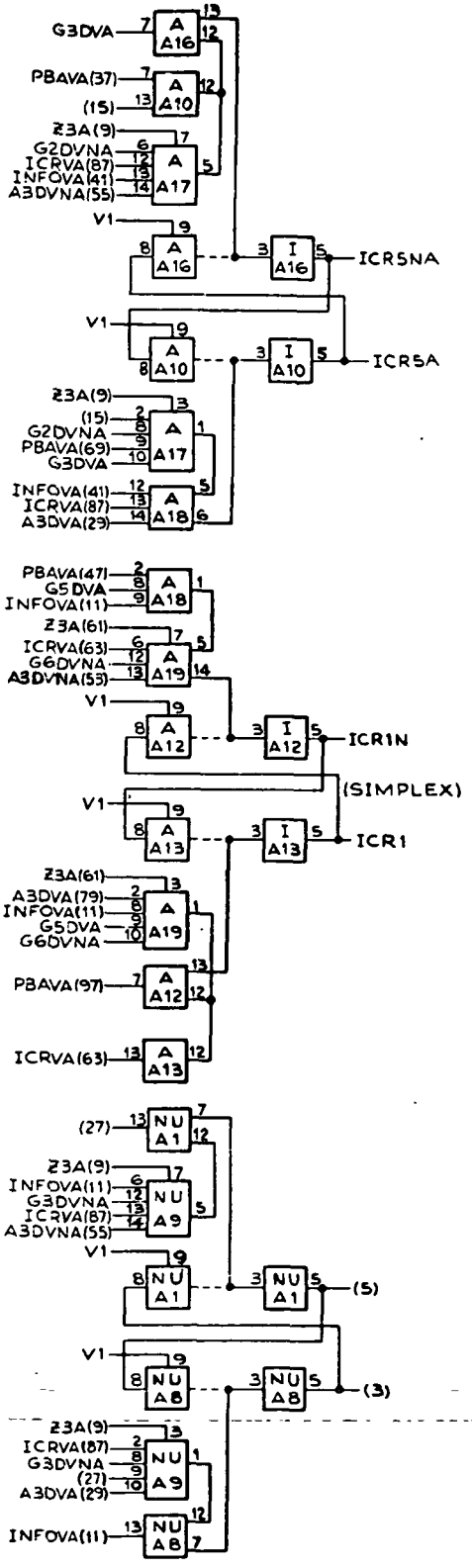


Figure 10-6. Internal Control Register Logic Diagram (Sheet 1 of 6)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	G1DVNA	51	
3		53	A3DVNA
5		55	A3DVNA
7	G7DVA	57	ICR3NA
9	Z3A	59	ICR3A
11	INFOVA	61	Z3A
13	ICR6NA	63	ICRVA
15		65	PBAVA
17	G2DVA	67	G4DVA
19	G1DVA	69	PBAVA
21	G7DVNA	71	V3
23	G3DVNA	73	SIG-RET
25	G6DVNA	75	V1
27		77	G2DVNA
29	A3DVA	79	A3DVA
31	ICR2A	81	G3DVA
33	ICR6A	83	G5DVA
35	ICR5NA	85	ICR4A
37	PBAVA	87	ICRVA
39		89	ICR1
41	INFOVA	91	ICR4NA
43	ICR2NA	93	G6DVA
45	ICR5A	95	ICR1N
47	PBAVA	97	PBAVA
49			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9	A10 I	A11	A12 I	A13 I	A14
A15	A16 I	A17 AA	A18 AA	A19 AA	A20	A21 I
A22 AA	A23 AA	A24 AA	A25 I	A26 AA	A27 AA	A28 AA
A29 I	A30 I	A31 I	A32	A33 I	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A23 Side A.
6. This Drawing Derived From IBM DWG NO. 6112357-REL(66123EV)

Figure 10-6. Internal Control Register Logic Diagram (Sheet 2)

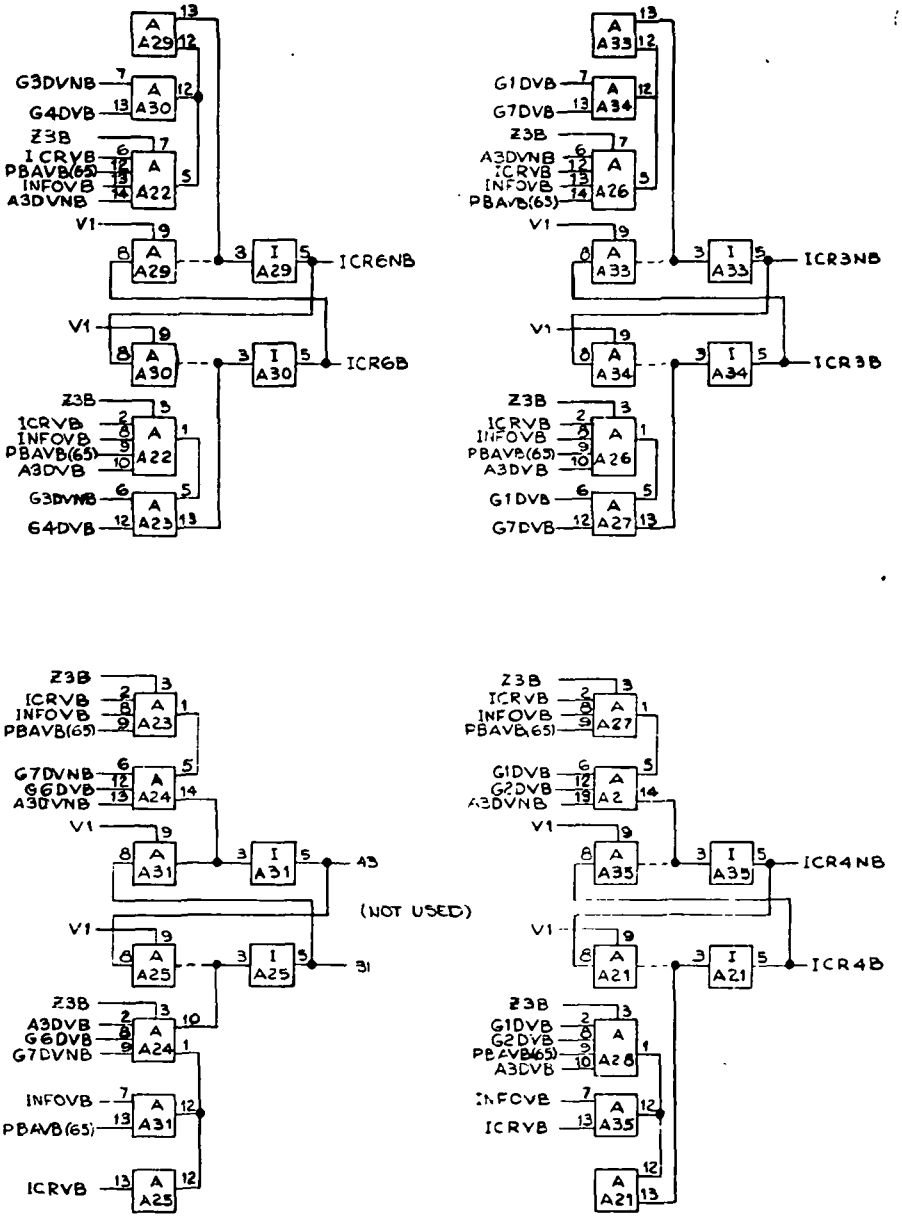
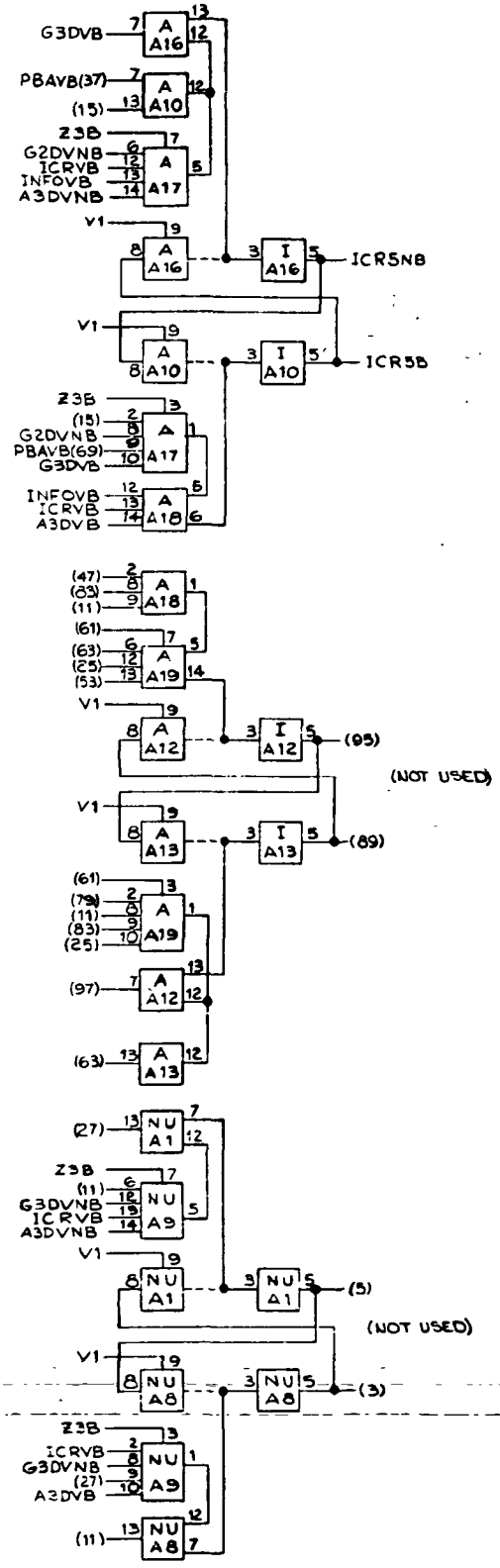


Figure 10-6. Internal Control Register Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	G1DVNB	51	
3		53	
5		55	A3DVNB
7	G7DVB	57	ICR3NB
9	Z3B	59	ICR3B
11		61	
13	ICR6NB	63	
15		65	PBAVB
17	G2DVB	67	G4DVB
19	G1DVB	69	PBAVB
21	G7DVNB	71	V3
23	G3DVNB	73	SIG-RET
25		75	V1
27		77	G2DVNB
29	A3DVB	79	
31		81	G3DVB
33	ICR6B	83	
35	ICR5NB	85	ICR4B
37	PBAVB	87	ICRVB
39		89	
41	INFOVB	91	ICR4NB
43		93	G6DVB
45	ICR5B	95	
47		97	
49			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9	A10 I	A11	A12 I	A13 I	A14
A15	A16 I	A17 AA	A18 AA	A19 AA	A20	A21 I
A22 AA	A23 AA	A24 AA	A25 I	A26 AA	A27 AA	A28 AA
A29 I	A30 I	A31 I	A32	A33 I	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A12 Side A.
6. This Drawing Derived From IBM DWG NO. 6112359-A(66123KJ)

Figure 10-6. Internal Control Register Logic Diagram (Sheet 4)

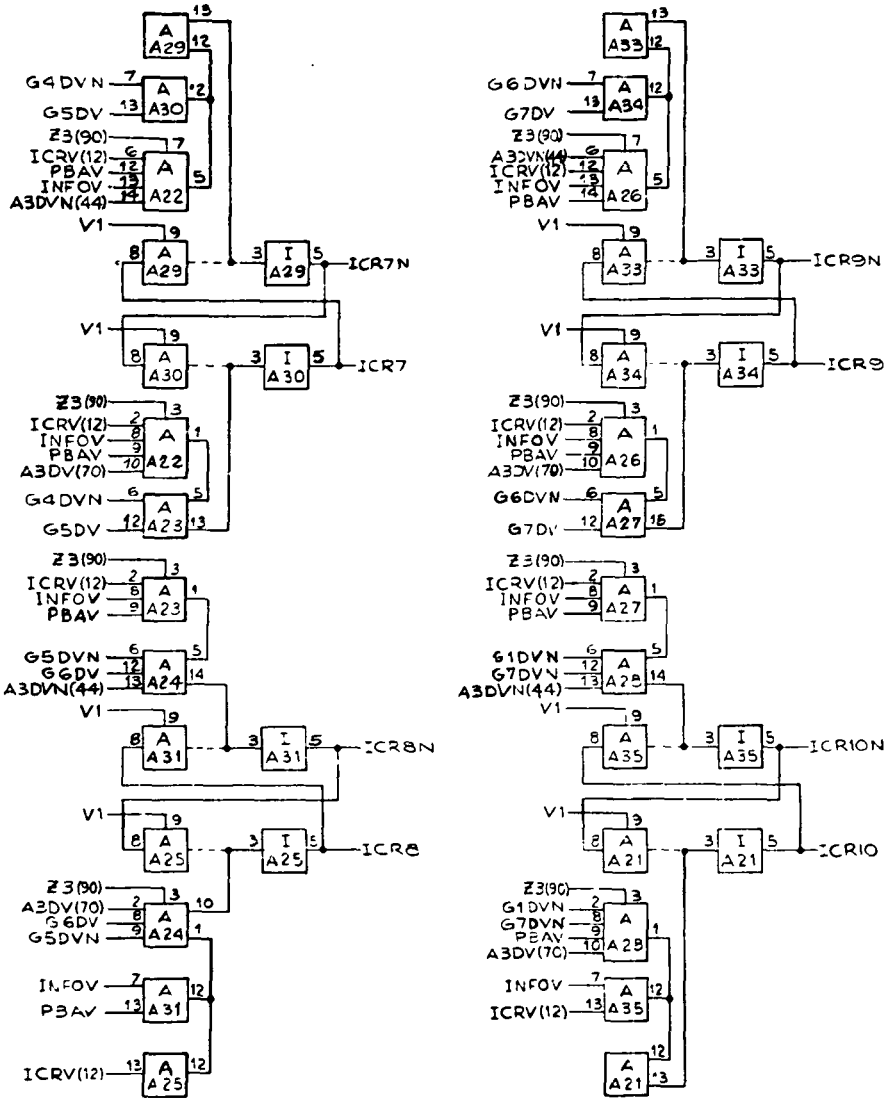
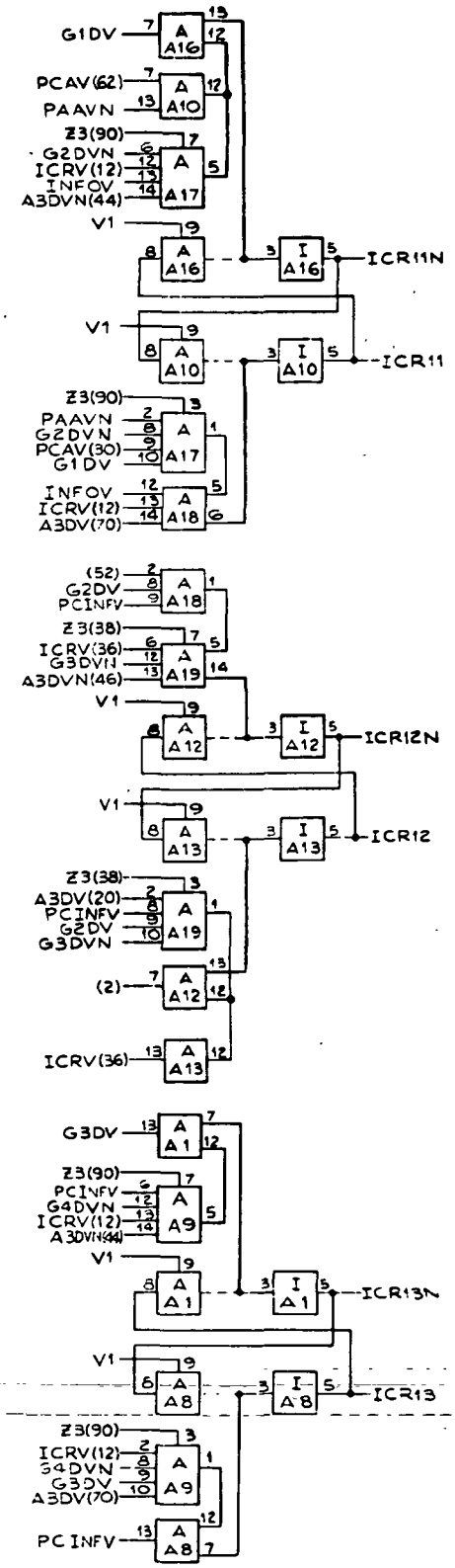


Figure 10-6. Internal Control Register Logic Diagram (Sheet 5)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4	ICR12N	54	ICR11
6	G6DV	56	ICR8N
8	ICR10N	58	INFOV
10	ICR12	60	
12	ICRV	62	PCAV
14	ICR10	64	ICR11N
16	G2DV	66	ICR7
18	G1DV	68	ICP8
20	A3DV	70	A3DV
22	G2DVN	72	G3DV
24	V1	74	G3DVN
26	SIG RET	76	G4DVN
28	V3	78	G5DVN
30	PCAV	80	G6DVN
32	G6DV	82	G7DVN
34	PBAV	84	PAAVN
36	ICRV	86	ICR7N
38	Z3	88	PCINFV
40	ICR9	90	Z3
42	ICR9N	92	G7DV
44	A3DVN	94	ICR13V
46	A3DVN	96	ICR13
48		98	G1DV11
50			

A1 I	A2	A3	A4	A5	A6	A7
A8 I	A9 AA	A10 I	A11	A12 I	A13 :	A14
A15	A16 I	A17 AA	A18 AA	A19 AA	A20	A21 :
A22 AA	A23 AA	A24 AA	A25 I	A26 AA	A27 AA	A28 AA
A29 I	A30 I	A31 1	A32	A33 :	A34 :	A35 :

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted-Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A12 Side B, 2A3A23 Side B, 2A3A14 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112358-REL(66123BT)

Figure 10-6. Internal Control Register Logic Diagram (Sheet 6)

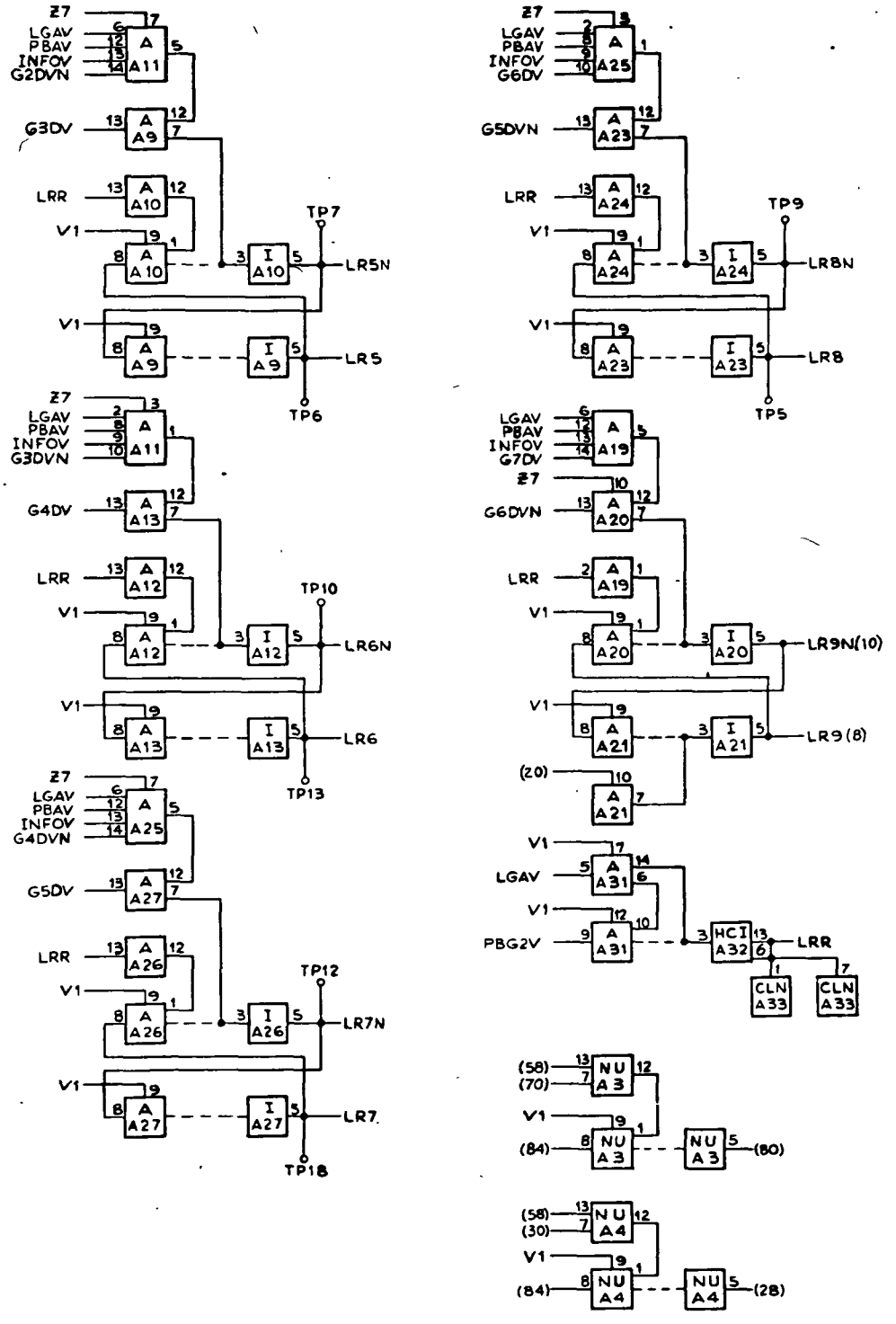
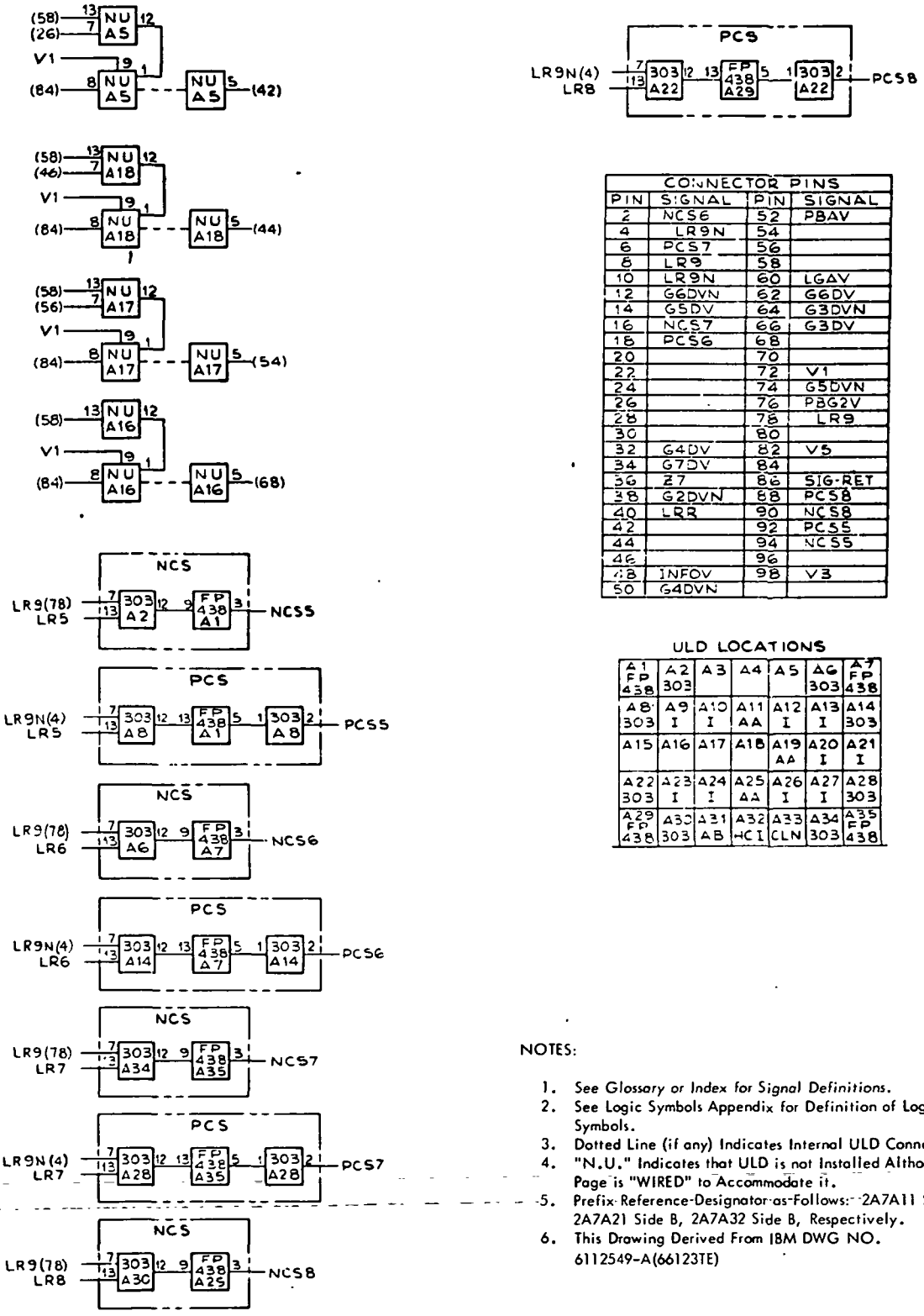


Figure 10-7. Ladder Register Logic Diagram (Sheet 1 of 8)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	NCS6	52	PBAV
4	LR9N	54	
6	PCS7	56	
8	LR9	58	
10	LR9N	60	LGAV
12	G6DVN	62	G6DV
14	G5DV	64	G3DVN
16	NCS7	66	G3DV
18	PCS6	68	
20		70	
22		72	V1
24		74	G5DVN
26		76	PBG2V
28		78	LR9
30		80	
32	G4DV	82	V5
34	G7DV	84	
36	Z7	86	SIG-RET
38	G2DVN	88	PCS8
40	LRR	90	NCS8
42		92	PCS5
44		94	NCS5
46		96	
48	INFOV	98	V3
50	G4DVN		

ULD LOCATIONS

A1 FP 438	A2 303	A3	A4	A5	A6 303	A7 FP 438
A8 303	A9 I	A10 I	A11 AA	A12 I	A13 I	A14 303
A15	A16	A17	A18	A19 AA	A20 I	A21 I
A22 303	A23 I	A24 I	A25 AA	A26 I	A27 I	A28 303
A29 FP 438	A30 303	A31 AB	A32 HCI	A33 CLN	A34 303	A35 FP 438

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A11 Side B; 2A7A21 Side B, 2A7A32 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112549-A(66123TE)

Figure 10-7. Ladder Register Logic Diagram (Sheet 2)

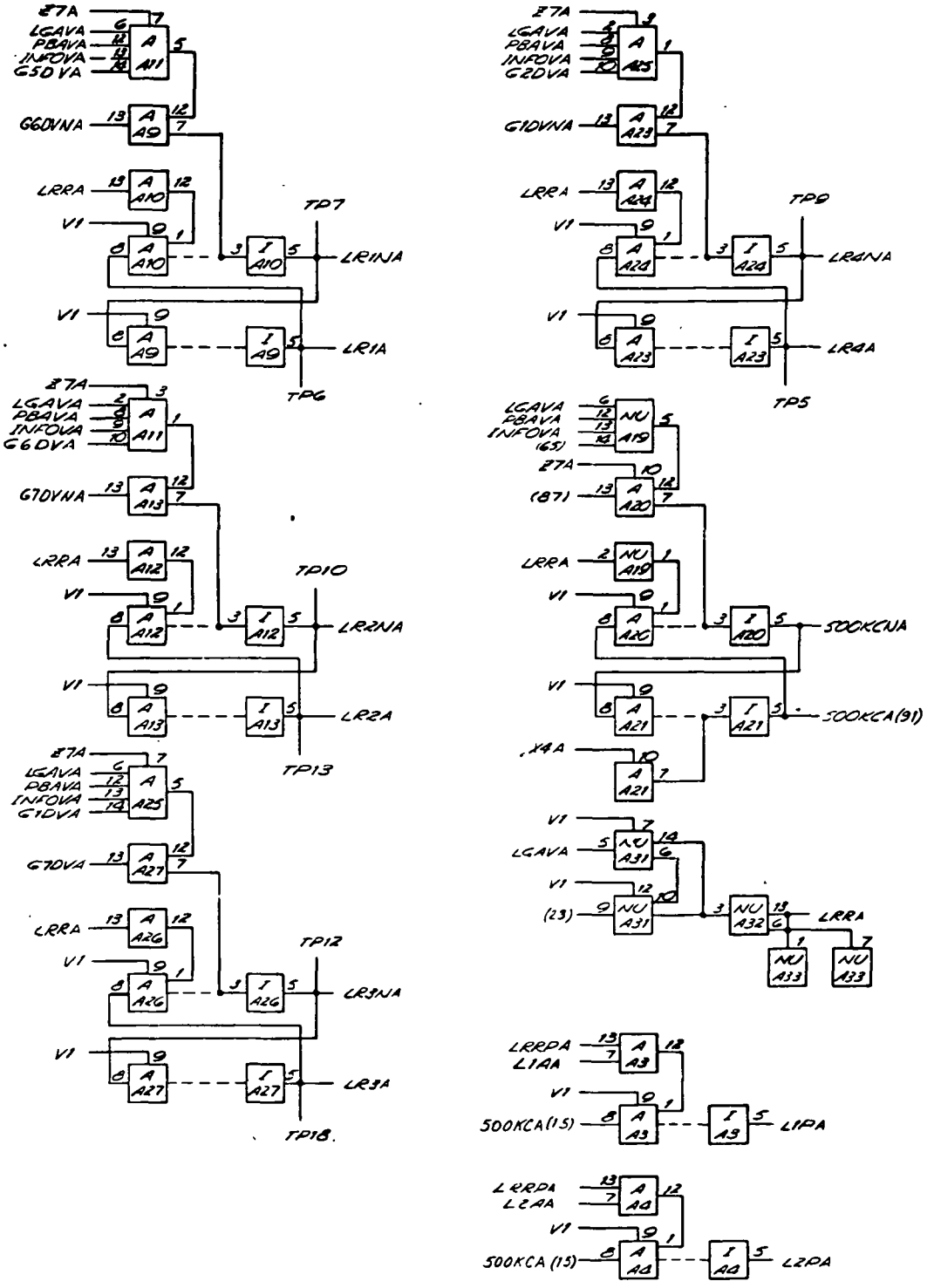
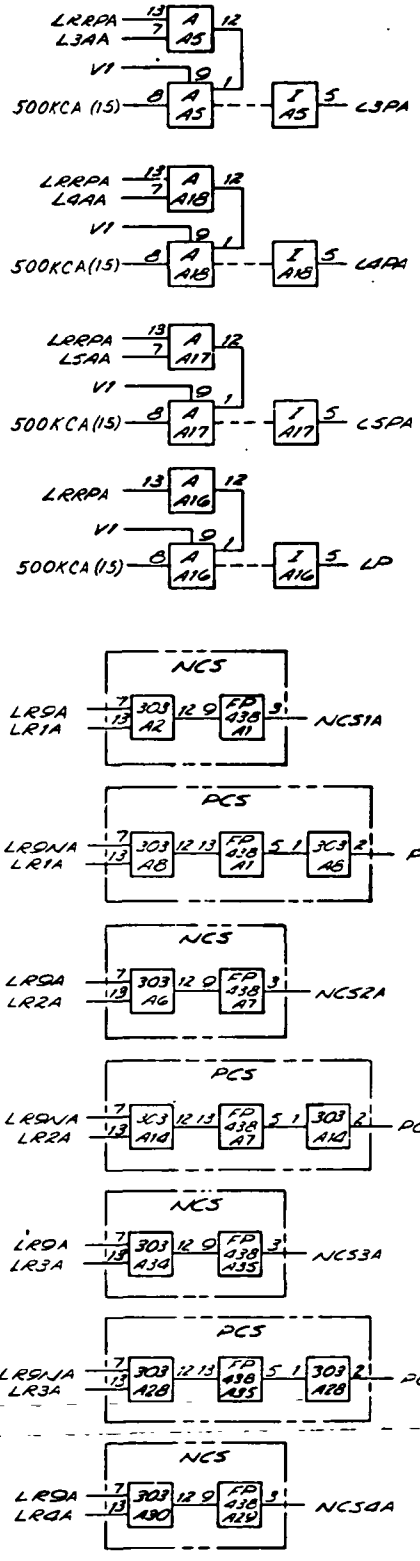
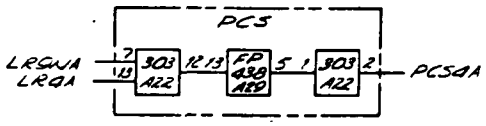


Figure 10-7. Ladder Register Logic Diagram (Sheet 3)





CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	INFOVA
3		53	L4AA
5	NCS1A	55	L4PA
7	PCS1A	57	L3PA
9	NCS4A	59	LRRA
11	PCS4A	61	G5DVA
13	SIG-RET	63	Z7A
15	500KCA	65	
17	V5A	67	G7DVNA
19	L1PA	69	L2AA
21	LR5A	71	L2PA
23		73	L3AA
25	G1DVNA	75	
27	V1	77	
29	L1AA	79	X4A
31	LP	81	PCS2A
33	G6DVNA	83	NCS3A
35	G6DVA	85	G7DVA
37	G2DVA	87	
39	LGAVA	89	500KCNA
41	LRRPA	91	500KCA
43	L5AA	93	PCS3A
45	L5PA	95	LR5NA
47	PBAUA	97	NCS2A
49	G1DVA		

ULD LOCATIONS

A1 FP 438	A2 303	A3 I	A4 I	A5 I	A6 303	A7 FP 438
A8 303	A9 I	A10 I	A11 AA	A12 I	A13 I	A14 303
A15	A16 I	A17 I	A18 I	A19	A20 I	A21 I
A22 303	A23 I	A24 I	A25 AA	A26 I	A27 I	A28 303
A29 FP 438	A30 303	A31	A32	A33	A34 303	A35 FP 438

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A32 Side A.
6. This Drawing Derived From IBM DWG NO. 6112548-A(66123TE)

Figure 10-7. Ladder Register Logic Diagram (Sheet 4)

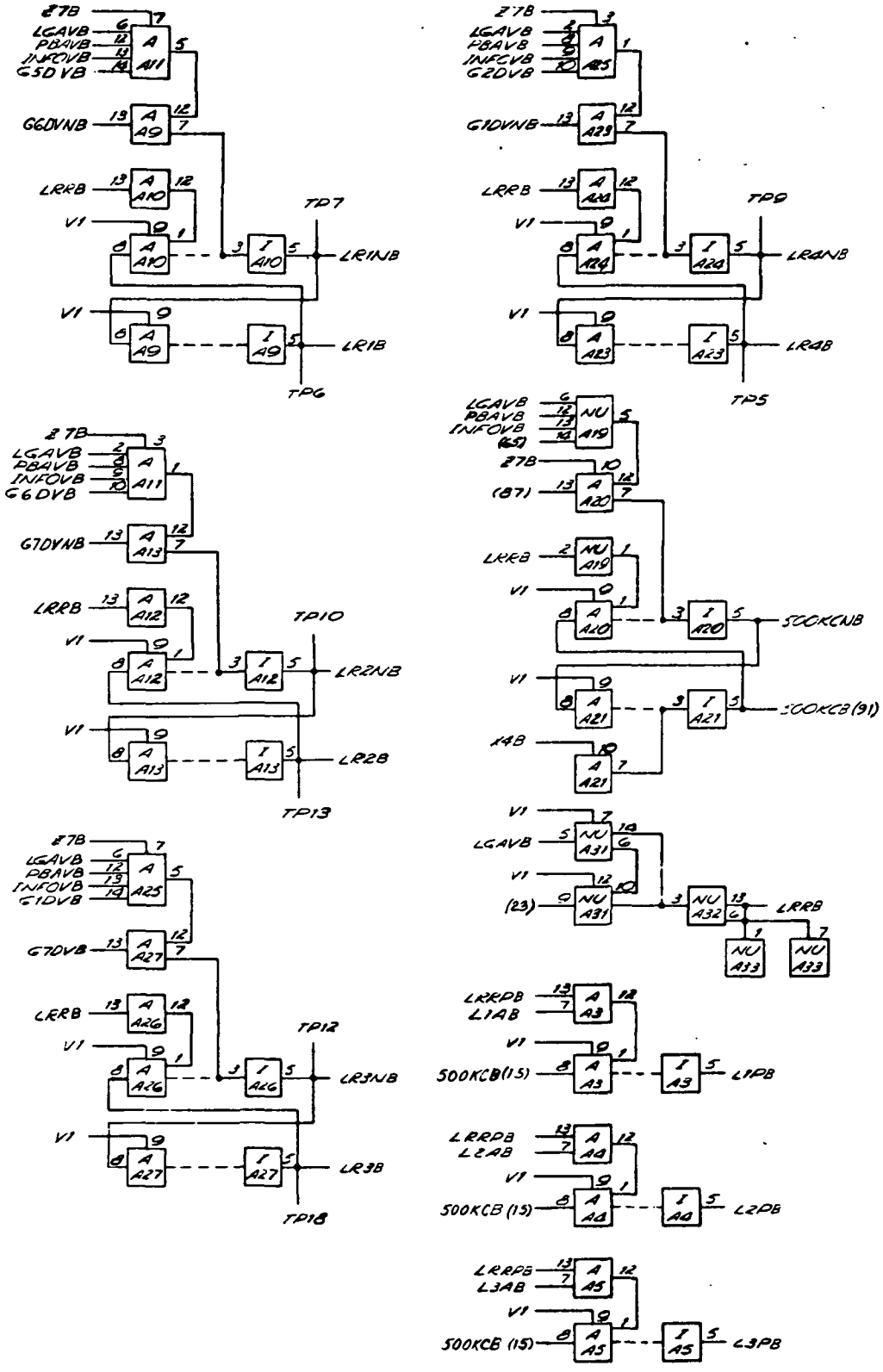
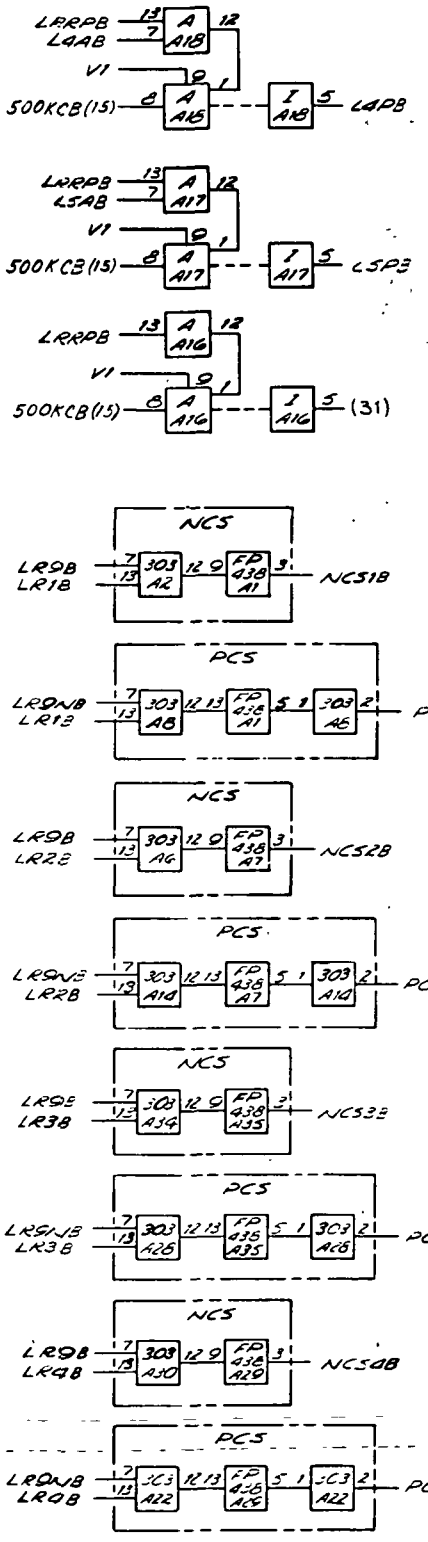


Figure 10-7. Ladder Register Logic Diagram (Sheet 5)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	INFOVB
3		53	L4AB
5	NCS1B	55	L4PB
7	PCS1B	57	L3PB
9	NCS4B	59	LRRB
11	PCS4B	61	G5DVB
13	SIG-RET	63	E7B
15	500KCB	65	
17	V5B	67	G7DVNB
19	L1PB	69	L2AB
21	LR9B	71	L2PB
23		73	L3AB
25	G1DVNB	75	
27	V1	77	
29	L1AB	79	X4B
31		81	PCS2B
33	G6DVNB	83	NCS3B
35	G6DVB	85	G7DVB
37	G2DVB	87	
39	LGAVB	89	500KCNB
41	LRRPB	91	500KCB
43	L5AB	93	PCS3B
45	L5PB	95	LR9NB
47	PBAVB	97	NCS2B
49	G1DVB		

ULD LOCATIONS

A1 FP 438	A2 303	A3 I	A4 I	A5 I	A6 303	A7 FP 438
A8 303	A9 I	A10 I	A11 AA	A12 I	A13 I	A14 303
A15	A16 I	A17 I	A18 I	A19	A20 I	A21 I
A22 303	A23 I	A24 I	A25 AA	A26 I	A27 I	A28 303
A29 FP 438	A30 303	A31	A32	A33	A34 303	A35 FP 438

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not-Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A21 Side A.
6. This Drawing Derived From IBM DWG NO. 6112547-A(66123TF)

Figure 10-7. Ladder Register Logic Diagram (Sheet 6)

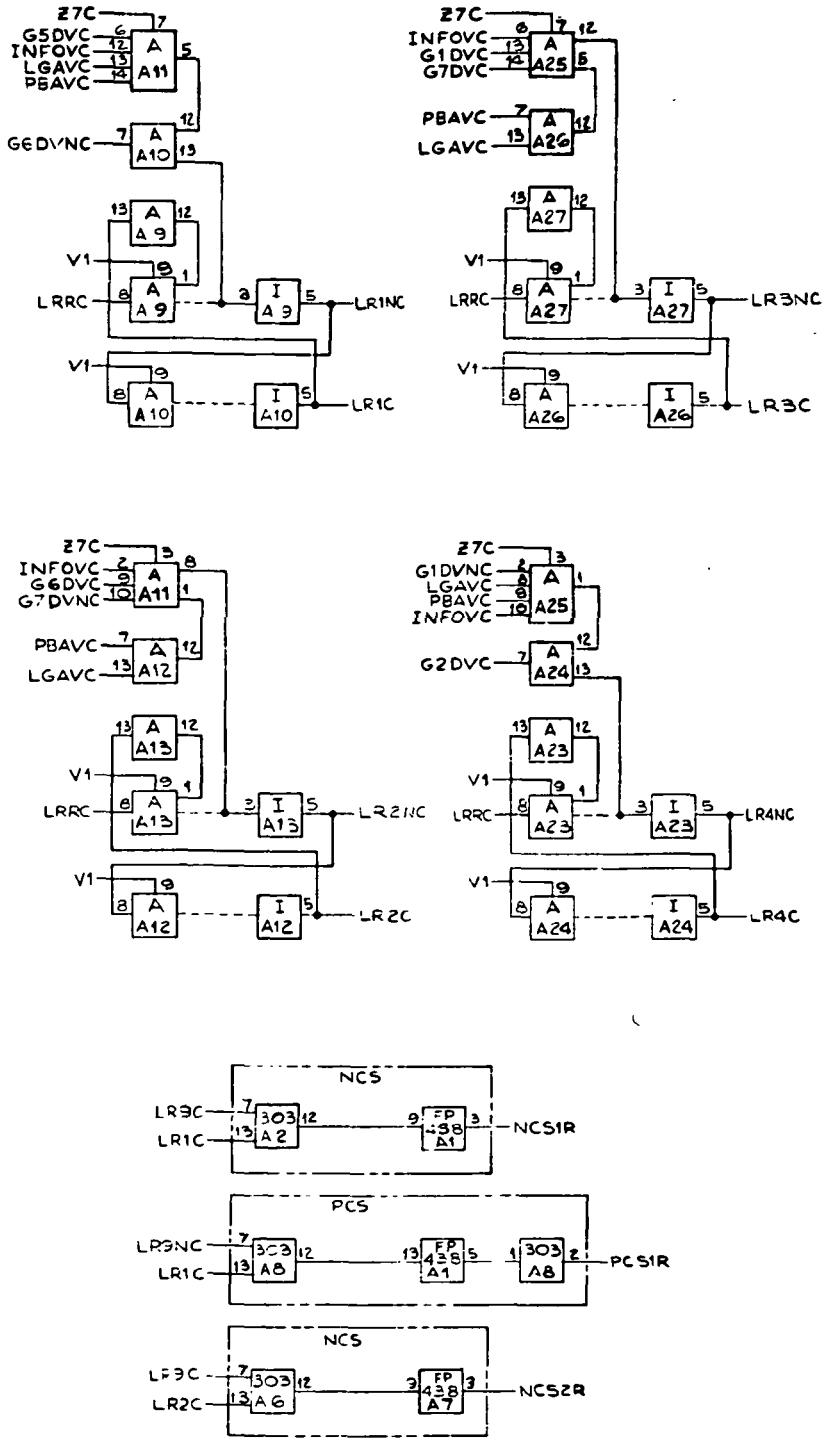
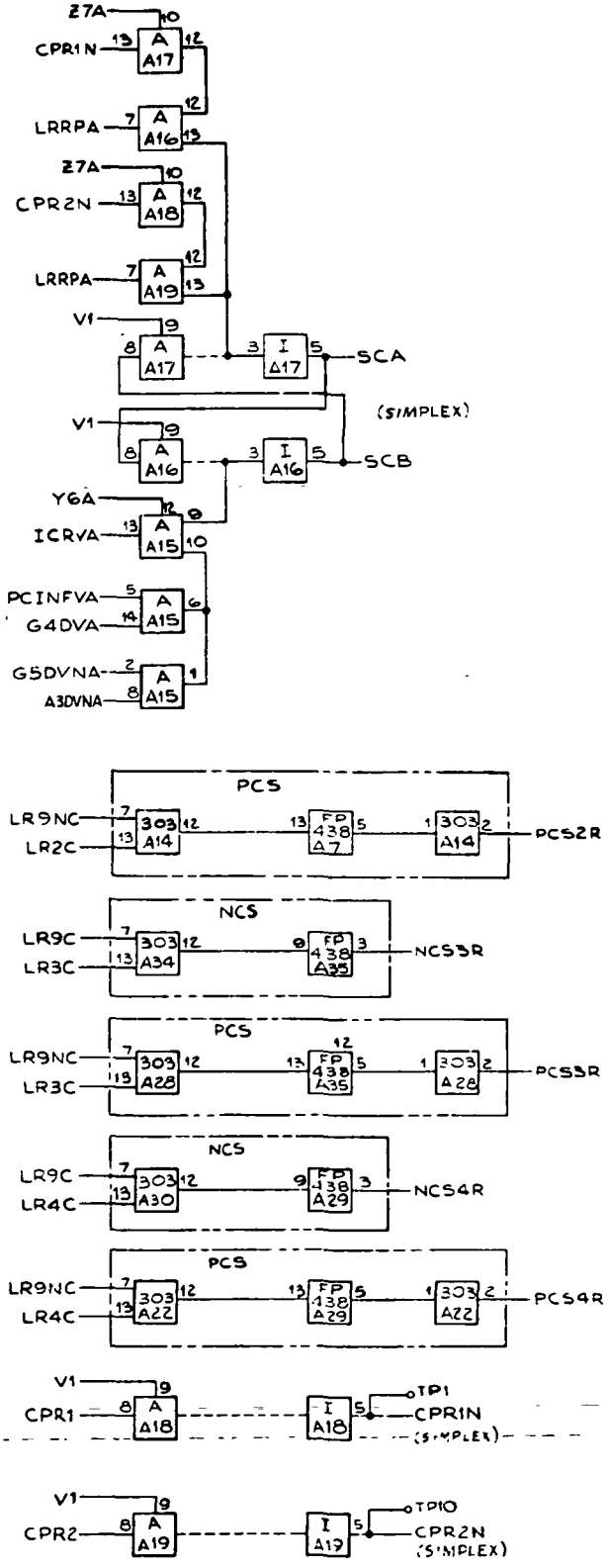


Figure 10-7. Ladder Register Logic Diagram (Sheet 7)



EDGE PINS			
PIN	SIGNAL	PIN	SIGNAL
1	NCS1R	51	INFOVC
3	A3DVNA	53	CPR1
5	NCS4R	55	G1DVNC
7	PCS4R	57	G1DVC
9	Z7A	59	LRRC
11	V3	61	G7DVNC
13	SIG-RET	63	Z7C
15	Y6A	65	G7DVC
17	V5C	67	G4DVA
19	ICRVA	69	CPR2
21	PCINFVA	71	LR2NC
23	SCA	73	LR3NC
25	G5DVNA	75	LR3C
27	V1	77	NCS2R
29	PCS1R	79	PCS2R
31	LR4C	81	PCS3R
33	LR1C	83	NCS3R
35	LR1NC	85	G5DVC
37	LR4NC	87	G6DVNC
39	LGAVC	89	LR9C
41	LRRPA	91	LR9NC
43	SCB	93	
45	G2DVC	95	LR2C
47	PBAVC	97	
49	G6DVC		

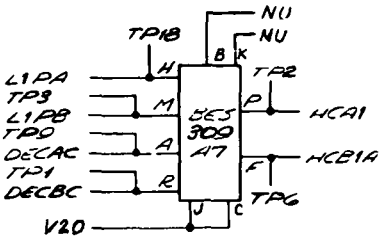
ULD LOCATION

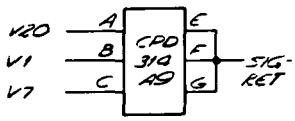
A1 FP 438	A2 303	A3	A4	A5	A6 303	A7 FP 438
A8 303	A9 I	A10 I	A11 AA	A12 I	A13 I	A14 303
A15 AB	A16 I	A17 I	A18 I	A19 I	A20	A21
A22 303	A23 I	A24 I	A25 AA	A26 I	A27 I	A28 303
A29 FP 438	A30 303	A31	A32	A33	A34 303	A35 FP 438

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A11 Side A.
6. This Drawing Derived From IBM DWG NO. 6112968-REL(66123DE)

Figure 10-7. Ladder Register Logic Diagram (Sheet 8)





CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	V7
4	CSP X	54	V7
6	CSP X	56	
8		58	DECAO
10		60	L1PA
12		62	L1PB
14		64	DECBO
16		66	HCA1A
18		68	HCB1A
20	V3	70	HCA1
22	SCA	72	
24	V3	74	
26	SIGRET	76	TELREF
28	SIGRET	78	TELREF
30		80	HCB1
32	V1	82	
34	V1	84	
36		86	
38	SCB	88	
40		90	
42		92	
44		94	ATBP
46		96	ATBP
48	V20	98	
50	V20		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A17.
6. This Drawing Derived From IBM DWG NO. 6112447-A(66123VJ)

Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 1 of 10)

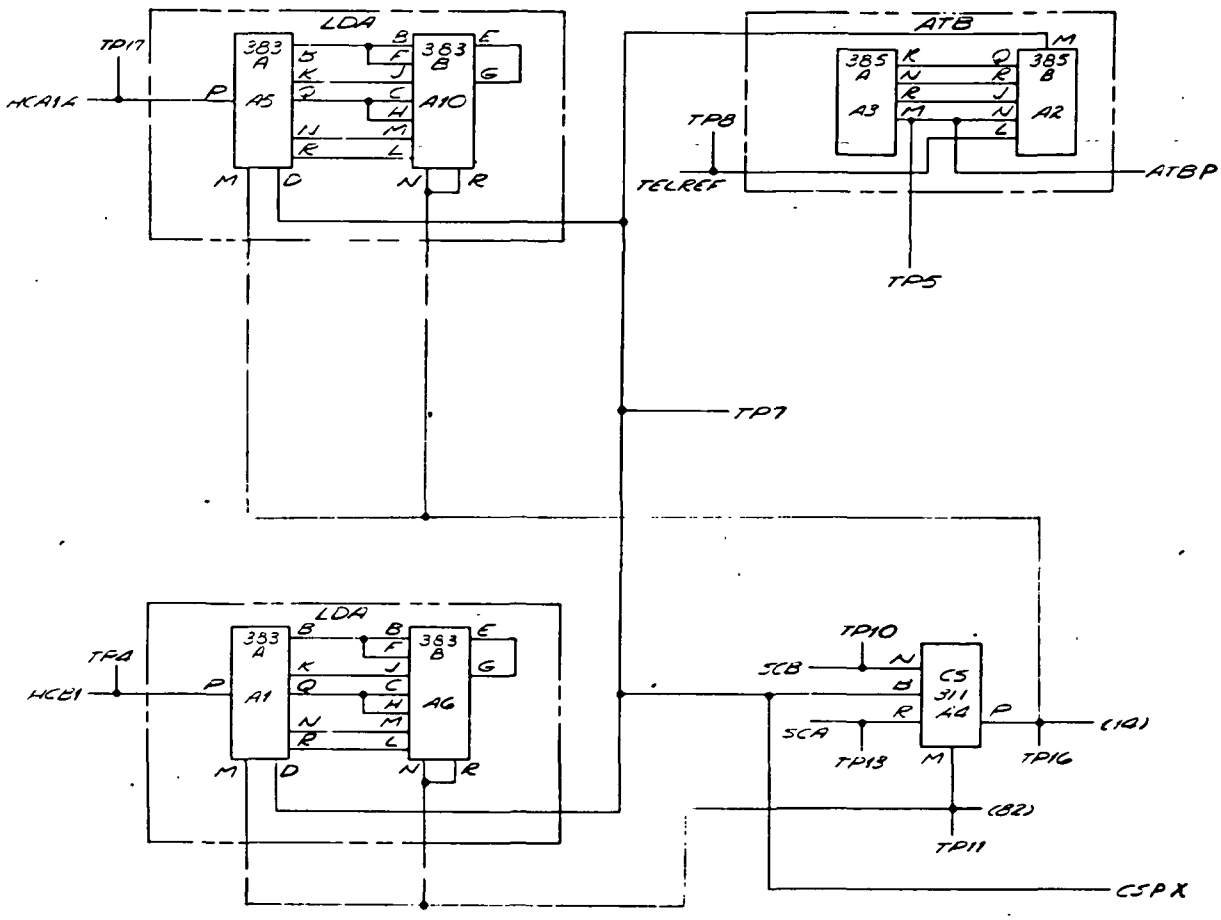
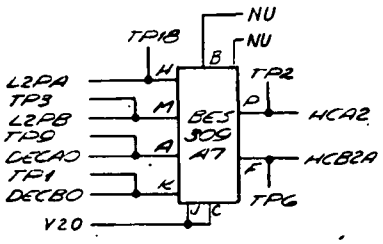
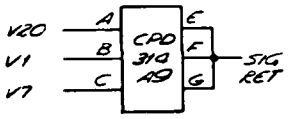


Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 2)





CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	V7
4	CSRX	54	V7
6	CSRX	56	
8		58	DECAO
10		60	L2PA
12		62	L2PB
14		64	DECBO
16		66	HCA2A
18		68	HCB2A
20	V3	70	HCA2
22	SCA	72	
24	V3	74	
26	SIG RET	76	TEL REF
28	SIG RET	78	TEL REF
30		80	HCB2
32	V1	82	
34	V1	84	
36		86	
38	SCB	88	
40		90	
42		92	
44		94	ATBR
46		96	ATBR
48	V20	98	
50	V20		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A28.
6. This Drawing Derived From IBM DWG NO. 6112448-A(66123VJ)

Figure 10-8. Digital-to-Analog Converters Logic Diagram (Sheet 3)

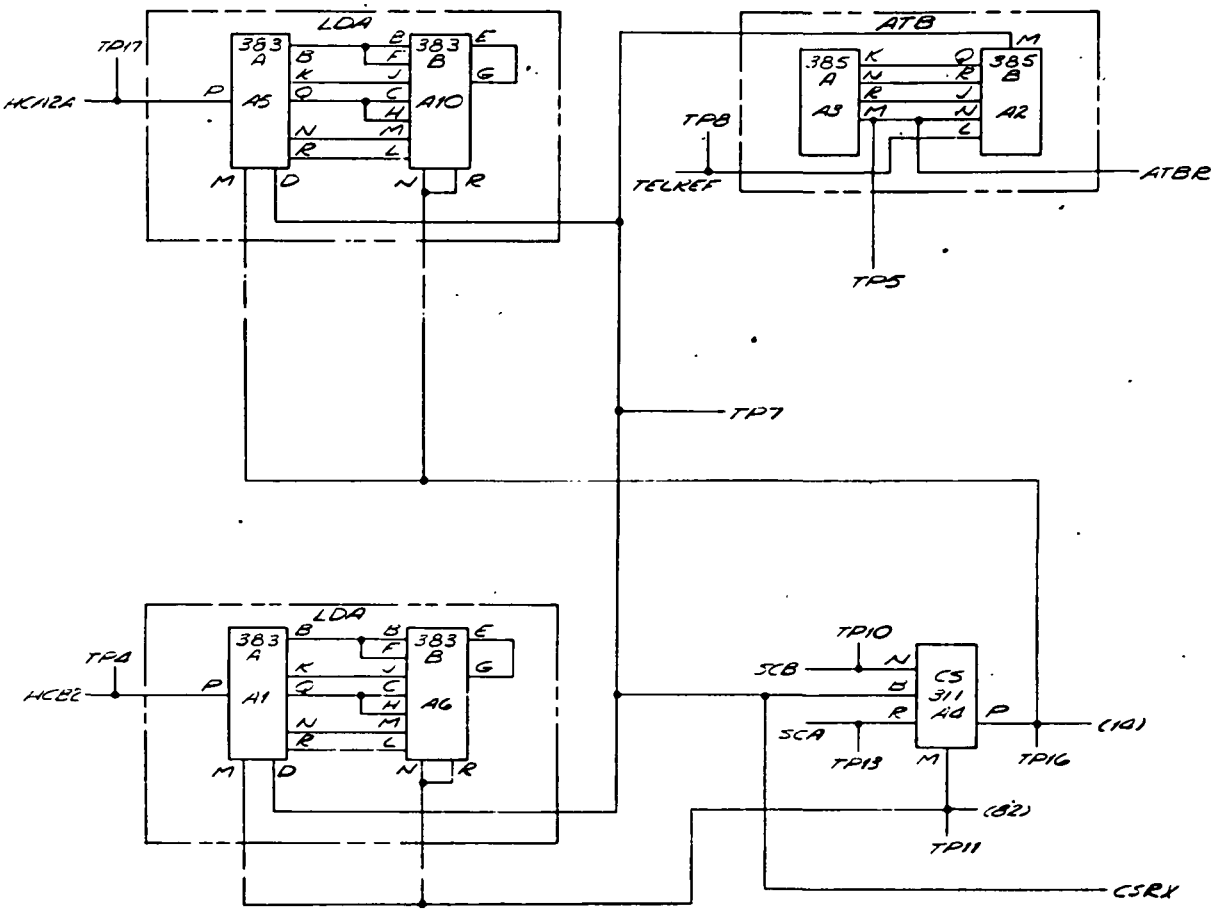
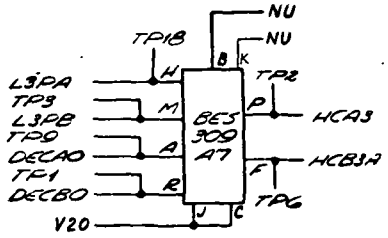
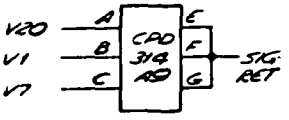


Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 4)





CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	V7
4	C5VX	54	V7
6	C5VX	56	
8		58	DECAO
10		60	L3PA
12		62	L3PB
14		64	DECBO
16		66	HCA3A
18		68	HCB3A
20	L3	70	HCA3
22	SCA	72	
24	V3	74	
26	SIGRET	76	TELREF
28	SIGRET	78	TELRET
30		80	HCB3
32	V1	82	
34	V1	84	
36		86	
38	SCB	88	
40		90	
42		92	
44		94	ATBV
46		96	ATBV
48	V20	98	
50	V20		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A25.
6. This Drawing Derived From IBM DWG NO. 6112449-A(66123VJ)

Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 5)

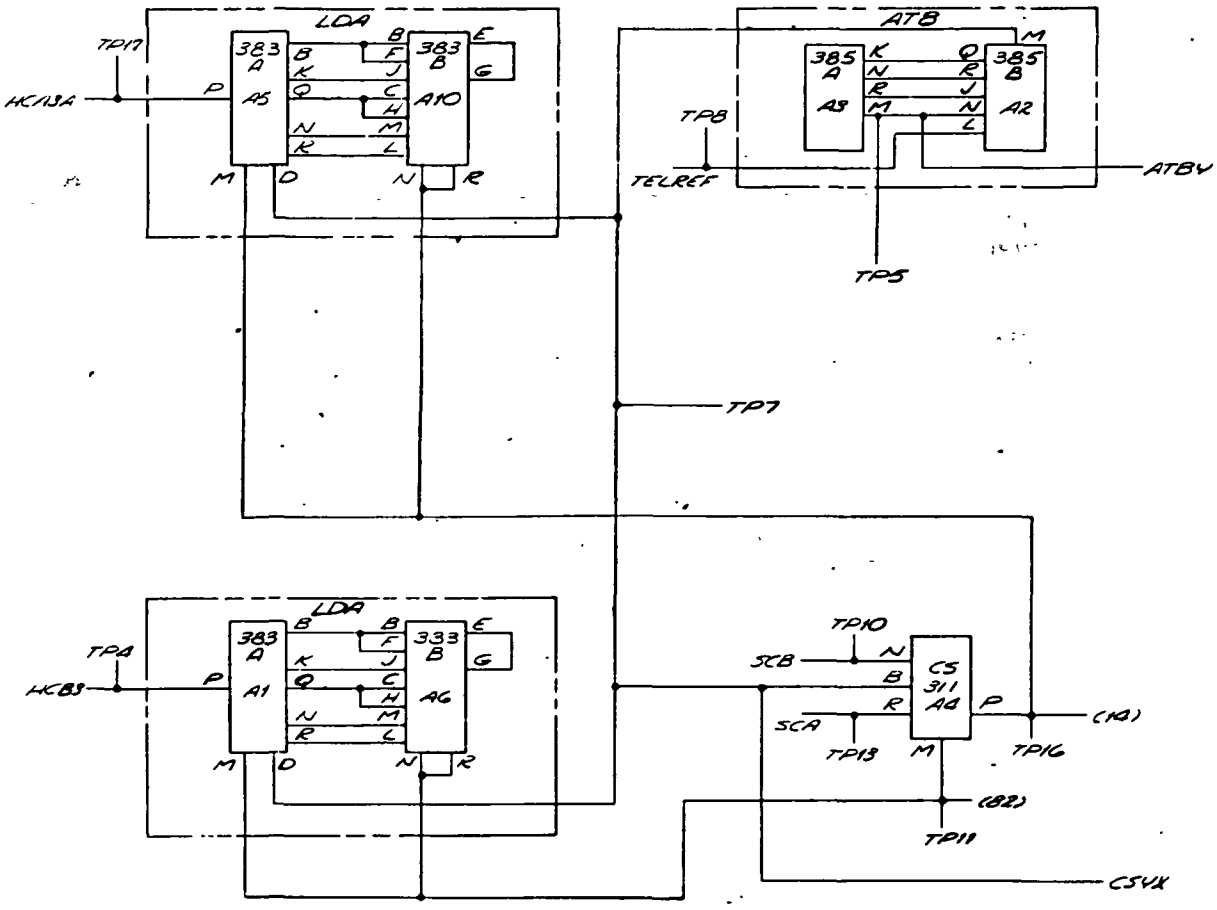


Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 6)

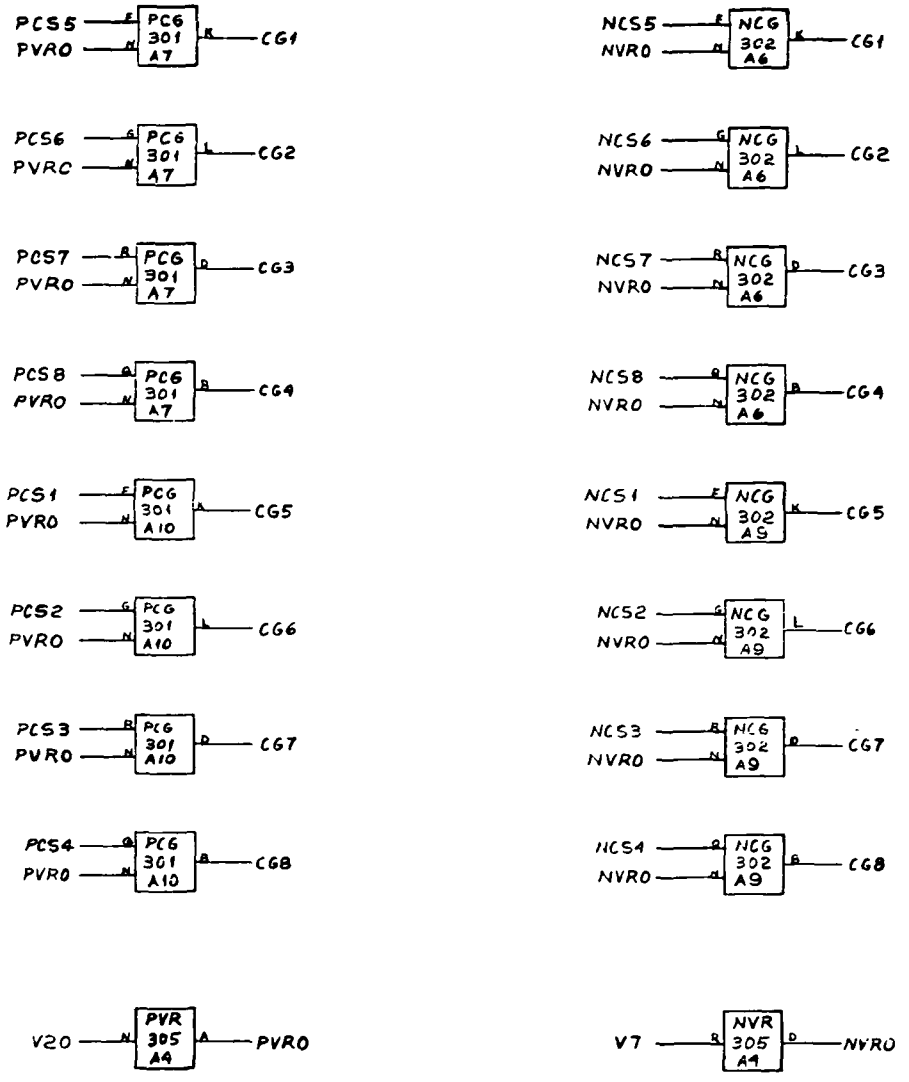
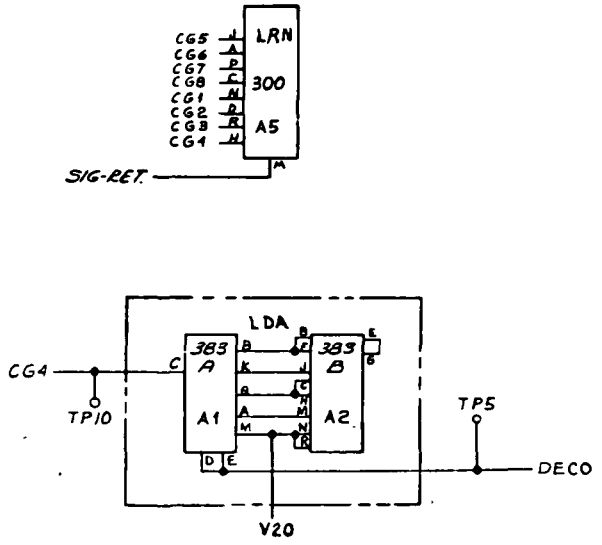


Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 7)



CONNECTOR PINS			
PIN	CONNECTOR	PIN	CONNECTOR
2		52	
4		54	DECRET
6	PCS3	56	
8	PCS2	58	
10	PCS4	60	
12		62	PCS7
14		64	
16		66	PCS8
18	PCS1	68	
20		70	
22		72	PCS5
24		74	
26	NCS3	76	
28	NCS2	78	PCS6
30	NCS4	80	
32		82	NCS7
34	NCS1	84	NCS6
36	SIG-RET	86	NCS8
38		88	
40	V7	90	NCS5
42		92	
44		94	
46		96	DECO
48	V20	98	
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." *Indicates that ULD is not Installed Although* Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A9, 2A7A20, 2A7A31, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112438-A(66123VJ)

Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 8)

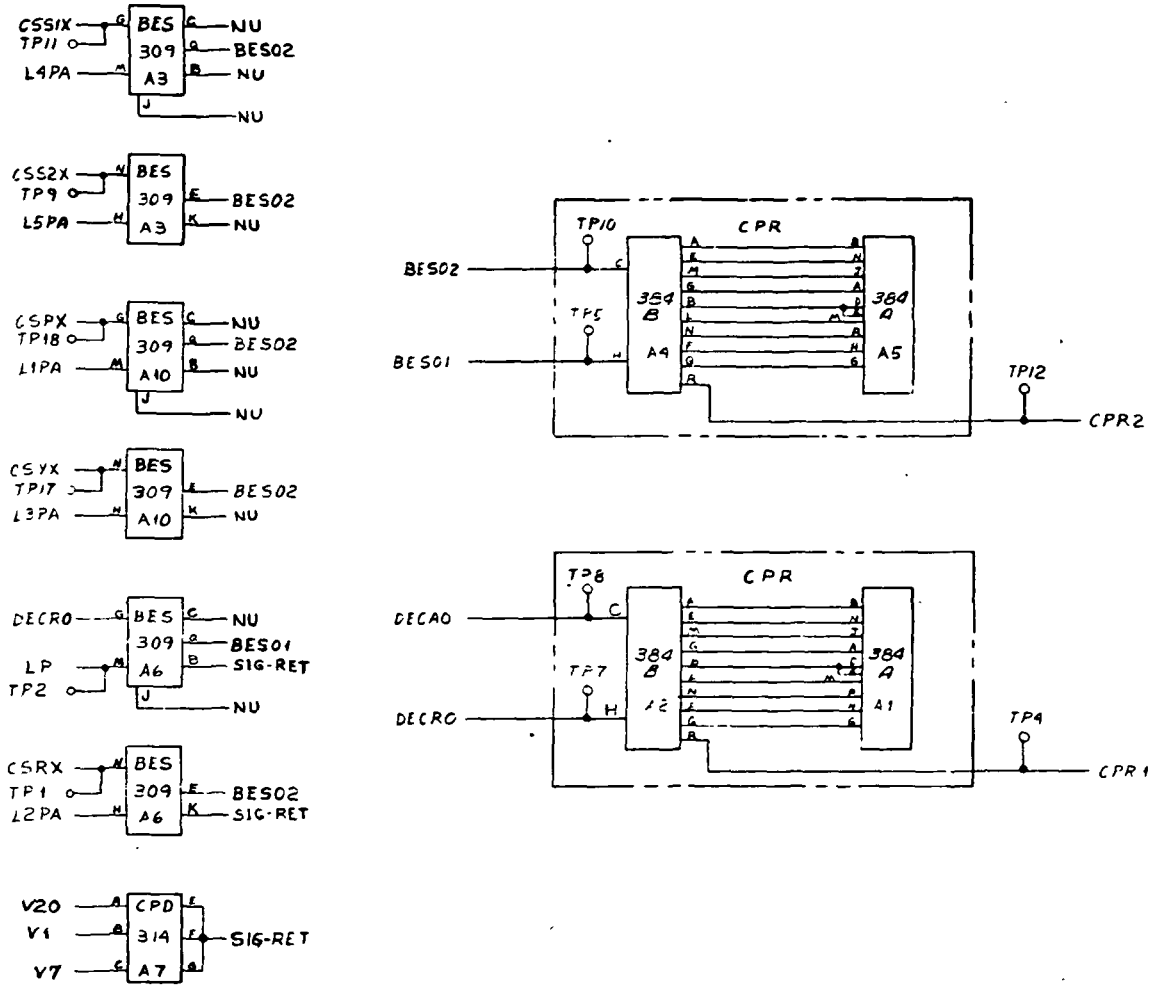


Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 9)

CONNECTOR PINS			
PIN	CONNECTOR	PIN	CONNECTOR
2	L3PA	52	V7
4	CSPX	54	V7
6	L1PA	56	CSS2X
8	CPR2	58	DECAO
10		60	DECRO
12		62	CPR1
14		64	
16		66	
18		68	
20	*CSYX	70	
22	"	72	
24		74	
26	SIG-RET	76	L2PA
28	SIG-RET	78	
30		80	LP
32	V1	82	
34	V1	84	
36		86	
38	L5PA	88	
40		90	
42	CSS1X	92	
44	L4PA	94	
46		96	CSRX
48	V20	98	
50	V20		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A7A6.
6. This Drawing Derived From IBM DWG NO. 6112458-A(66123VJ)

Figure 10-8. Digital-to-Analog Converter Logic Diagram (Sheet 10)

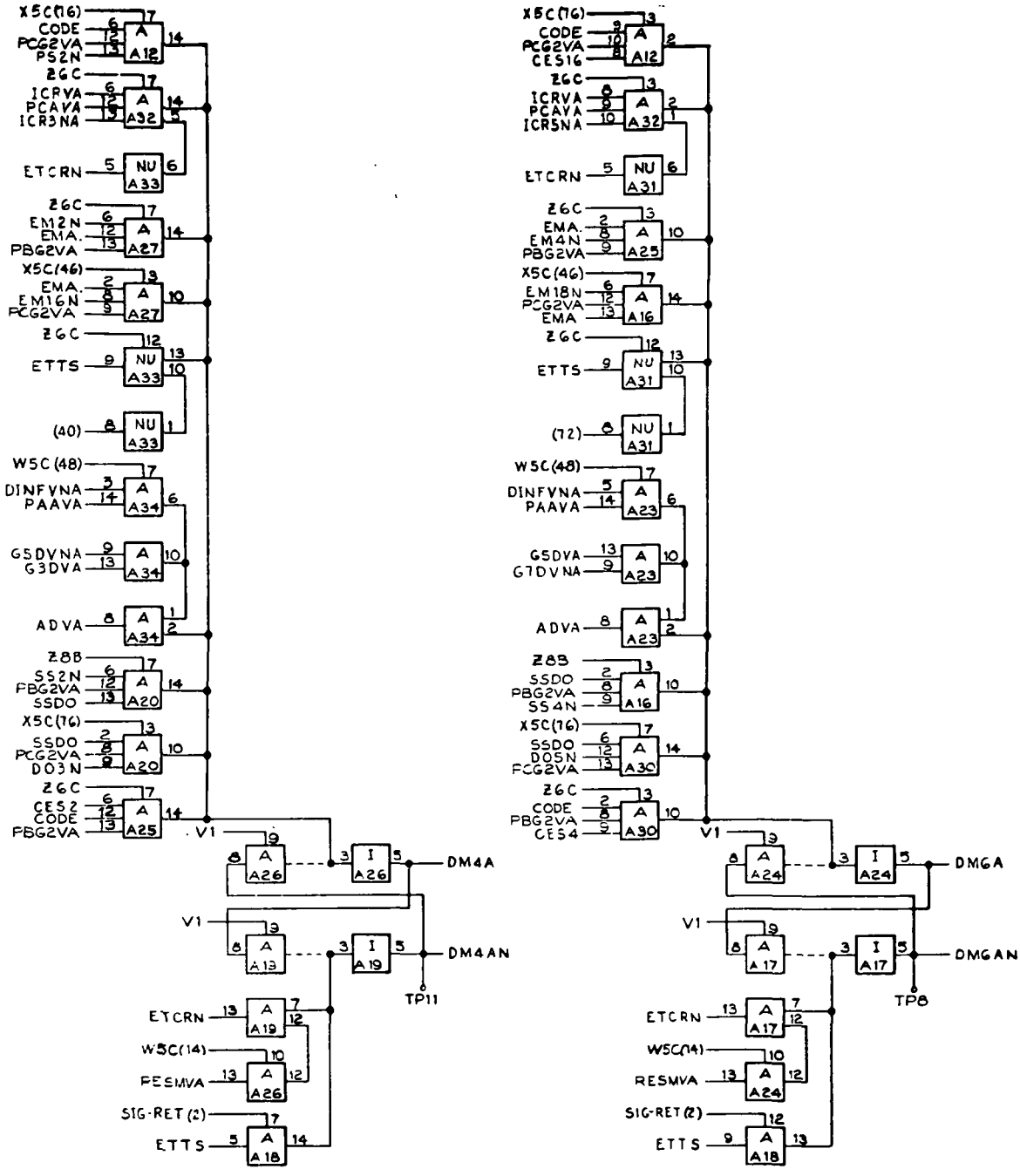
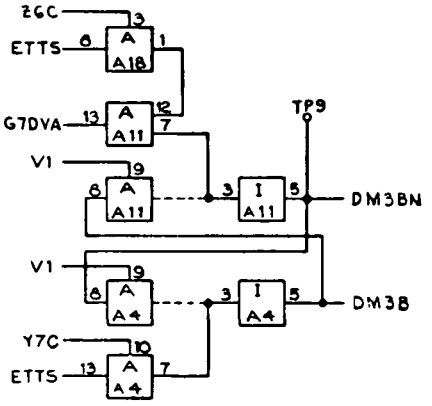
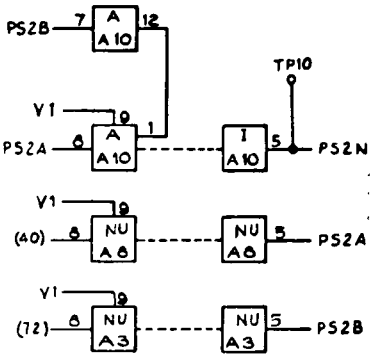
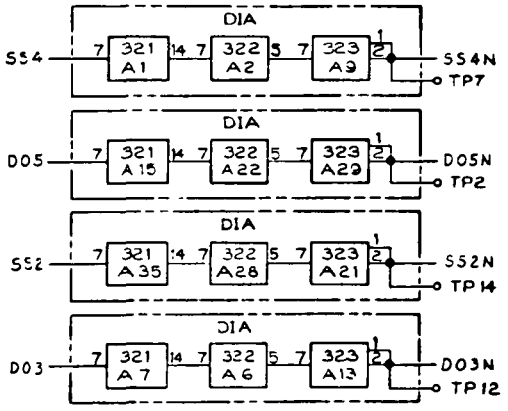


Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 1 of 14)







CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	SIG-RET	52	EM4N
4	DO3	54	G5DVA
6	SS2	56	Z8B
8	Y7C	58	ICR3NA
10	PS2B	60	PCAVA
12	V1	62	ICRVA
14	W5C	64	ICR5NA
16	ADYA	66	DM6A
18	G7DVA	68	Z6C
20	DM3B	70	RESMVA
22	EM1A	72	
24	EM2N	74	EM18N
26	DINFVBA	76	X5C
28	G3DVA	78	PCG2VA
30	PAAVA	80	SSDO
32	ETCRN	82	CODE
34	G5DVA	84	PBG2VA
36	EM16N	86	CES4
38	DM4A	88	PS2A
40		90	SIG-RET
42	ETTS	92	G7DVNA
44	CES2	94	DO5
46	X5C	96	SS4
48	W5C	98	CES16
50	V2		

A1 321	A2 322	A3	A4 I	A5	A6 322	A7 321
A8	A9 323	A10 I	A11 I	A12 AA	A13 323	A14
A15 321	A16 AA	A17 I	A18 AB	A19 I	A20 AA	A21 323
A22 322	A23 AB	A24 I	A25 AA	A26 I	A27 AA	A28 322
A29 323	A30 AA	A31	A32 AA	A33	A34 AB	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A22 Side B.
6. This Drawing Derived From IBM DWG NO. 6112818-REL(66123FN)

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 2)

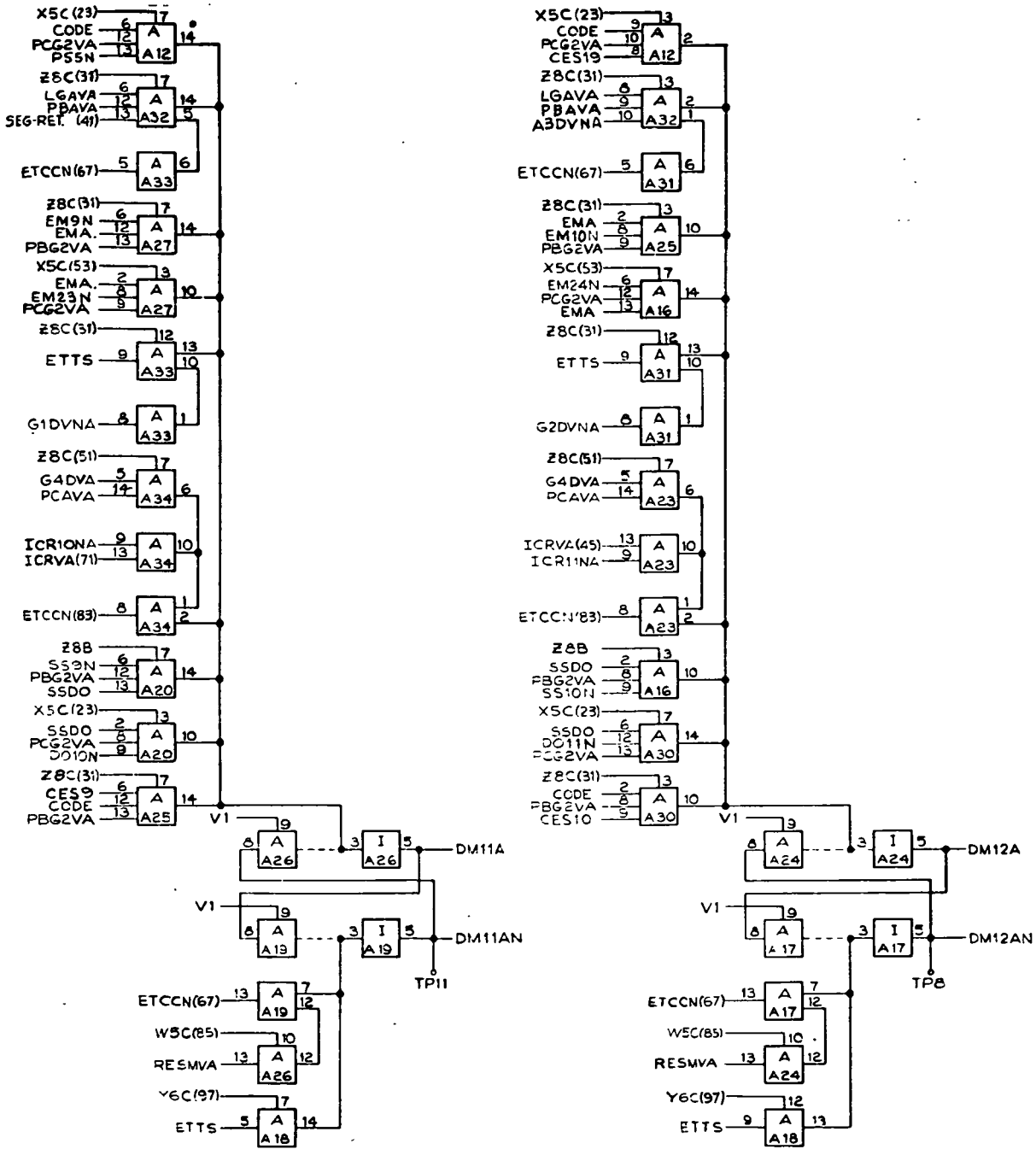
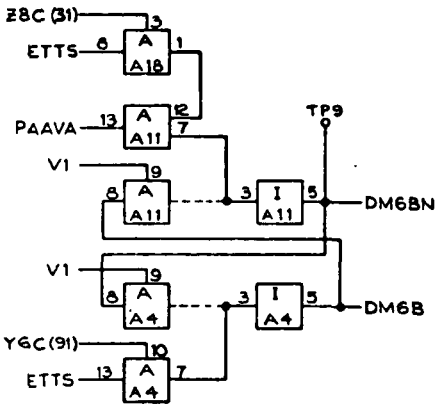
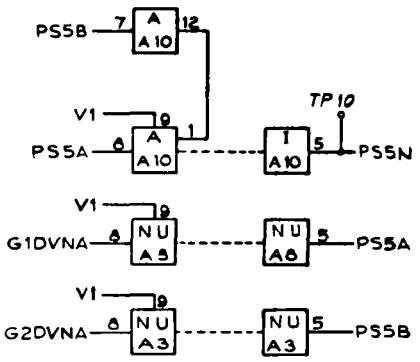
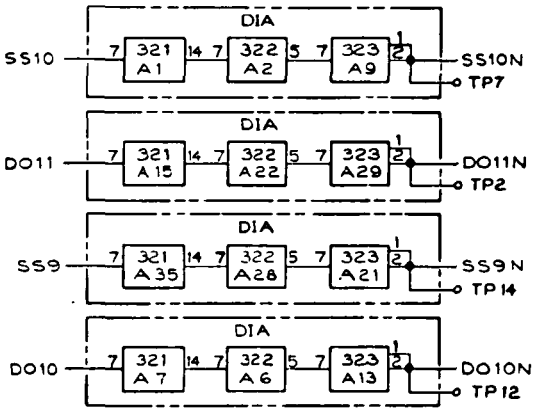


Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 3)







CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CES9	51	Z8C
3	SS10	53	X5C
5	DO11	55	CES9
7	ICR11NA	57	ETTS
9	SIG-RET	59	G1DVNA
11	PS5A	61	DM11A
13	CES10	63	EM23N
15	PB21A	65	ICR10NA
17	CORE	67	ETCCN
19	SS9	69	PC2/A
21	PC3VA	71	ICRVA
23	X5C	73	G4DVA
25	EM9N	75	EM9N
27	G2DVNA	77	EM4
29	RESMVA	79	DM6B
31	Z8C	81	PAAVA
33	DM12A	83	ETCCN
35	ABDVNA	85	W5C
37	LGAVA	87	V1
39	PBAVA	89	PS5B
41	SIG-RET	91	Y6C
43	Z8B	93	SS9
45	ICRVA	95	DO10
47	EM10N	97	Y6C
49	V3		

ULD LOCATIONS

A1 321	A2 322	A3	A4 I	A5	A6 322	A7 321
A8	A9 323	A10 I	A11 I	A12 AA	A13 323	A14
A15 321	A16 AA	A17 I	A18 AB	A19 I	A20 AA	A21 323
A22 322	A23 AB	A24 I	A25 AA	A26 I	A27 AA	A28 322
A29 323	A30 AA	A31 AB	A32 AA	A33 AB	A34 AB	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A32 Side A.
6. This Drawing Derived From IBM DWG NO. 6112839-REL(66123BW)

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 4)

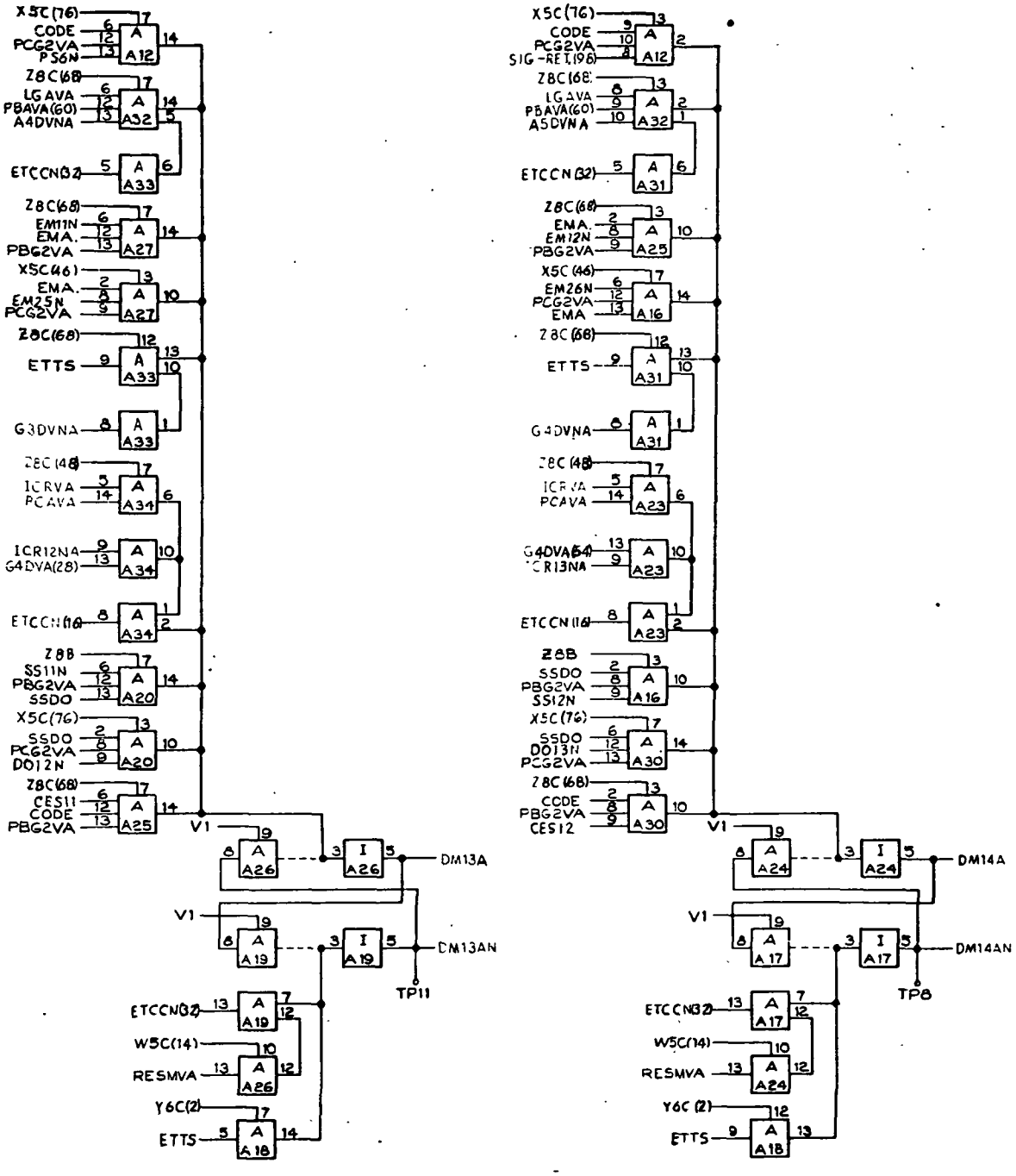
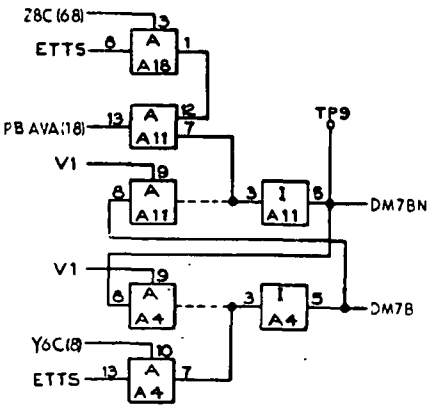
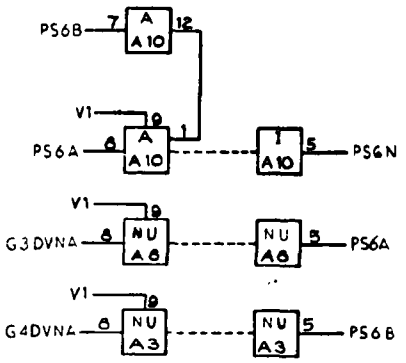
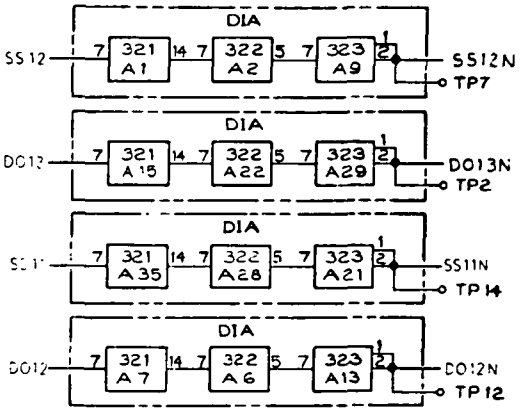


Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 5)







CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	Y6C	52	EM12N
4	DO12	54	G4DVA
6	SS11	56	Z8B
8	Y6C	58	A4DVNA
10	PS6B	60	PBAVA
12	V1	62	LGAVA
14	W5C	64	A5DVNA
16	ETCCH	66	DM14A
18	PB4VA	68	Z8C
20	DM7B	70	RESMJA
22	EMA	72	G4DVNA
24	EM11N	74	EM26N
26	TCRVA	76	Y5C
28	G4DVA	78	PCG2VA
30	PCLAVA	80	SSDO
32	ETCCN	82	CCDE
34	ICR12NA	84	PRG2VA
36	EM25N	86	CES12
38	DM13A	88	PS6A
40	G3DVNA	90	SIG-RET
42	ETTS	92	ICR13NA
44	CES11	94	DO13
46	X5C	96	SS12
48	Z8C	98	SIG-RET
50	V3		

A1 321	A2 322	A3	A4 I	A5	A6 322	A7 321
A8	A9 323	A10 I	A11 I	A12 AA	A13 323	A14
A15 321	A16 AA	A17 I	A18 AB	A19 I	A20 AA	A21 323
A22 322	A23 AB	A24 I	A25 AA	A26 I	A27 AA	A28 322
A29 323	A30 AA	A31 AB	A32 AA	A33 AB	A34 AB	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A32 Side B.
6. This Drawing Derived From IBM DWG NO. 6112539-REL(66123ET)

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 6)

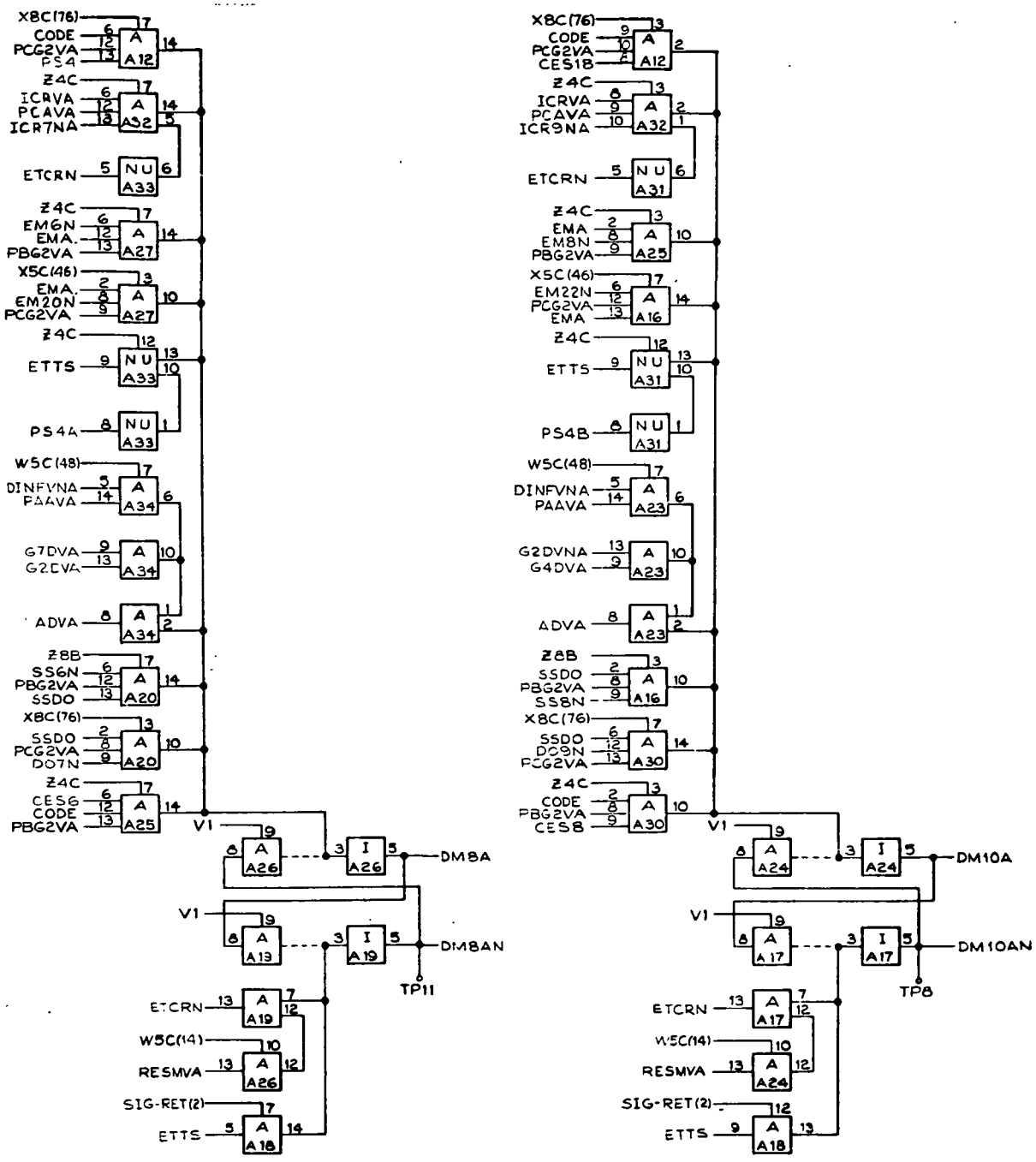
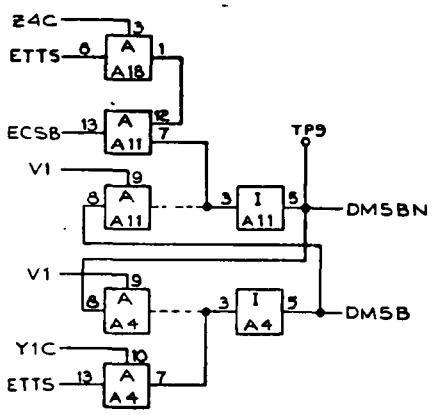
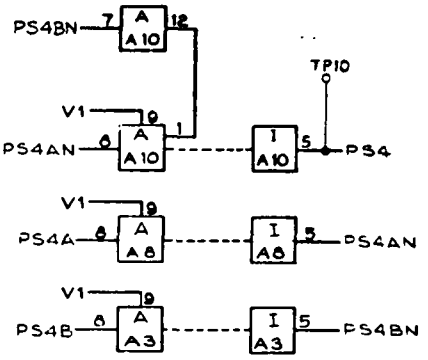
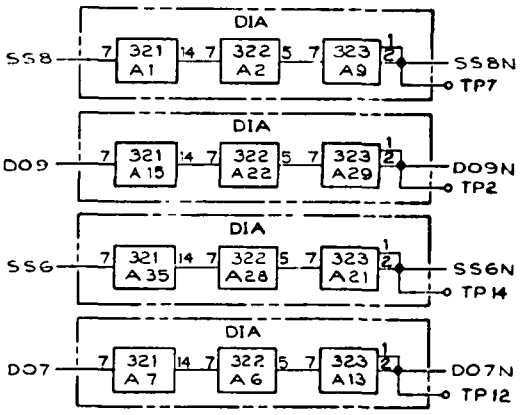


Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 7)







CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	SIG-RET	52	EM8N
4	DO7	54	G2DVNA
6	SS6	56	Z8B
8	Y1C	58	ICR7NA
10	PS4BN	60	PCLVA
12	V1	62	ICR7A
14	WBC	64	ICR9NA
16	AD7A	66	DM10A
18	ECSB	68	Z4C
20	DM5B	70	RESMVA
22	EM4	72	PS4B
24	EM8N	74	EM22N
26	DIL.FVNA	76	X8C
28	G2DVA	78	PCG2VA
30	PAAVA	80	SSDO
32	ETCRN	82	CODE
34	G7DVA	84	PBG2VA
36	EM2CN	86	CE*8
38	DM8A	88	PS4AN
40	[illegible]	90	SIG-RET
42	ETTS	92	G4DVA
44	CES8	94	DO9
46	X8C	96	SS8
48	WBC	98	CES1B
50	V3		

A1 321	A2 322	A3 I	A4 I	A5	A6 322	A7 321
A8 I	A9 323	A10 I	A11 I	A12 AA	A13 323	A14
A15 321	A16 AA	A17 I	A18 AB	A19 I	A20 AA	A21 323
A22 322	A23 AB	A24 I	A25 AA	A26 I	A27 AA	A28 322
A29 323	A30 AA	A31	A32 AA	A33	A34 AB	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A33 Side B.
6. This Drawing Derived From IBM DWG NO. 6112837-REL(66123FN)

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 8)

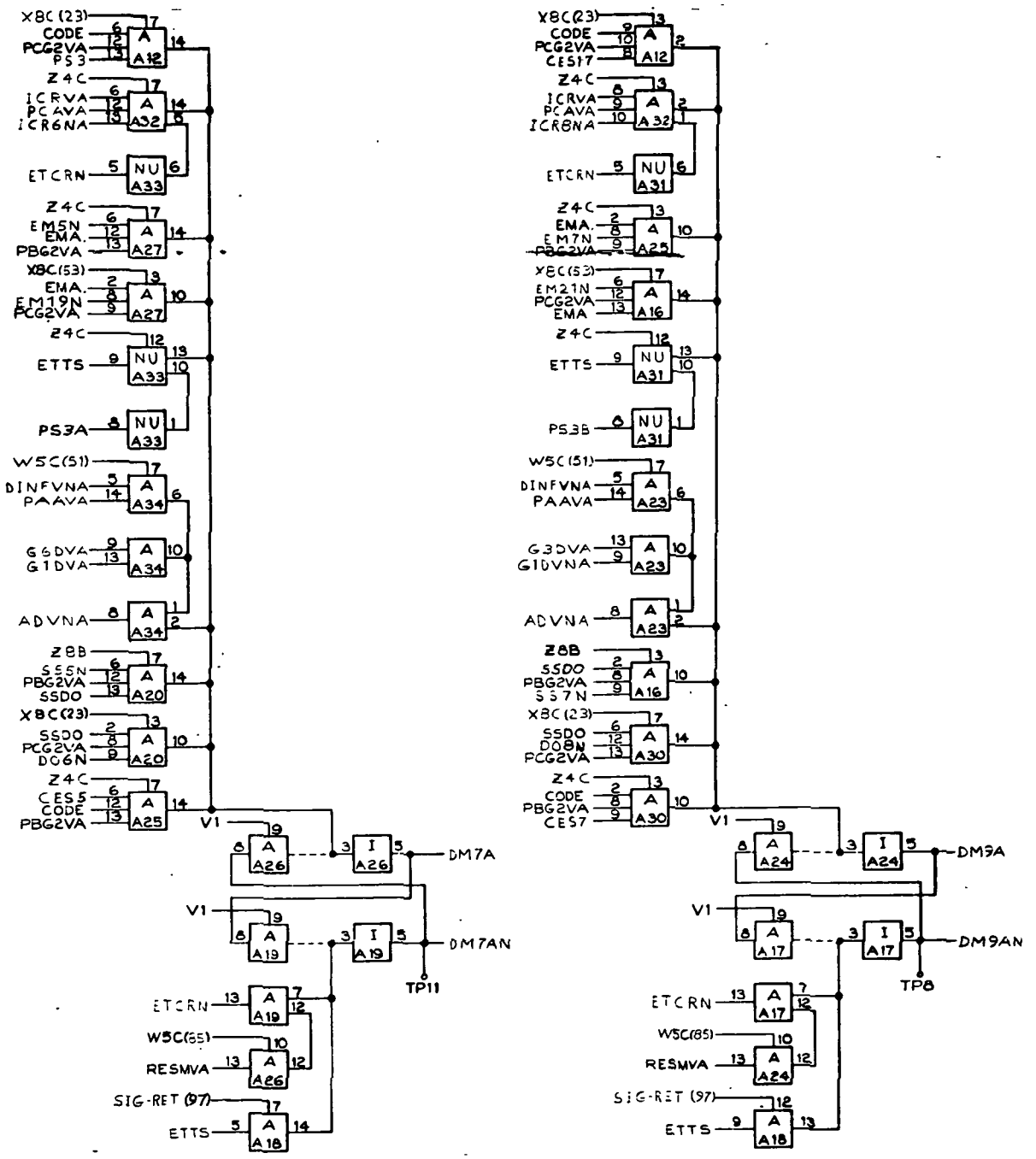
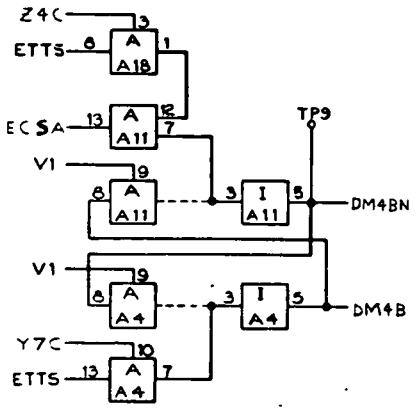
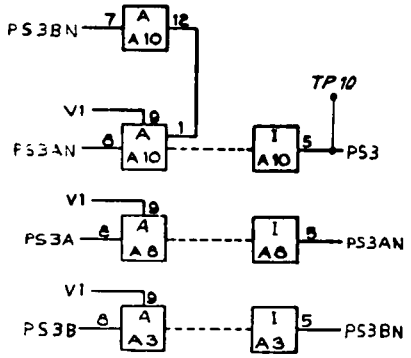
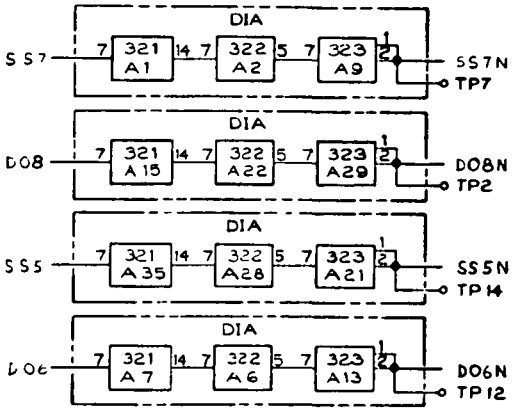


Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 9)







CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CES17	51	WSC
3	SS1	53	XBC
5	DCB	55	CES5
7	GIDVNA	57	ETTS
9	SIG-RET	59	PS3A
11	PS3AN	61	DM7A
13	CE=7	63	EM19N
15	PB6AVA	65	G1DVA
17	[illegible]	67	ETCKN
19	[illegible]	69	PAAVA
21	PEG2VA	71	G1DVA
23	X8C	73	DINFVNA
25	EM21N	75	EM5N
27	[illegible]	77	LM1A
29	PE_MVA	79	DM14B
31	E4C	81	ECCA
33	LM9A	83	ADVNA
35	L_8NA	85	WSC
37	ICRVA	87	V1
39	PAAVA	89	PS3BN
41	ECR6NA	91	Y7C
43	Z8B	93	SS5
45	G8DVA	95	DO6
47	EM1N	97	SIG-RET
49	V3		

A1 321	A2 322	A3 1	A4 1	A5	A6 322	A7 321
A8 1	A9 323	A10 1	A11 1	A12 AA	A13 323	A14
A15 321	A16 AA	A17 1	A18 AB	A19 1	A20 AA	A21 323
A22 322	A23 AB	A24 1	A25 AA	A26 1	A27 AA	A28 322
A29 323	A30 AA	A31	A32 AA	A33	A34 AB	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A33 Side A.
6. This Drawing Derived From IBM DWG NO. 6112819-REL(66123FN)

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 10)

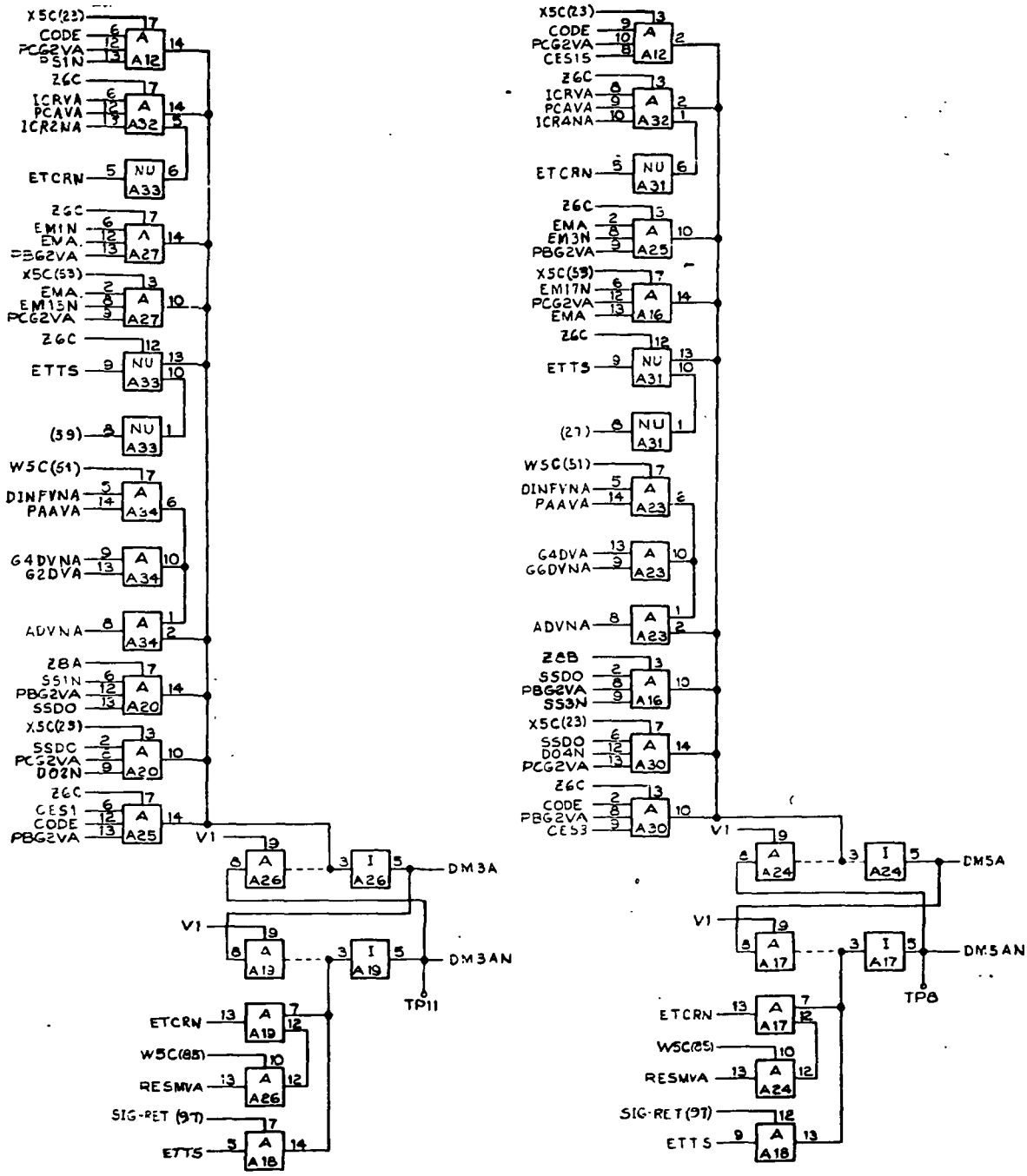
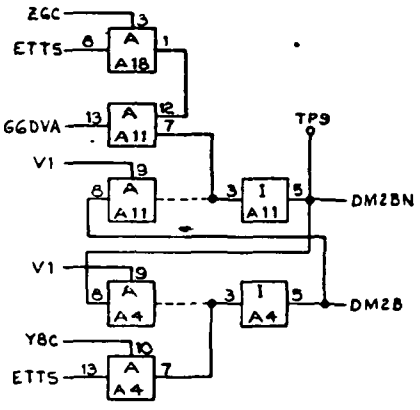
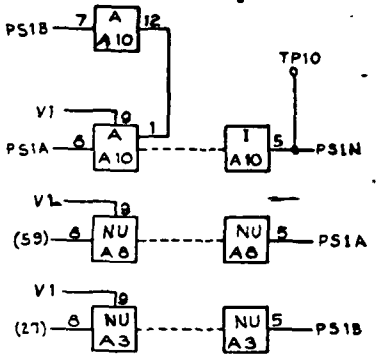
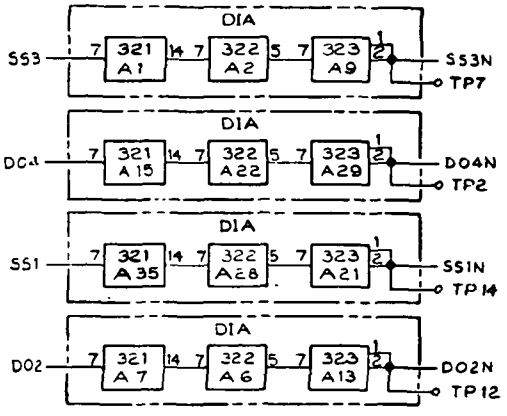


Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 11)







CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CES1S	51	Y5C
3	SS3	53	X5C
5	DO4	55	CES1
7	G6DVNA	57	ETTS
9	SIG-RET	59	
11	PS1A	61	DM3A
13	CES3	63	EM15N
15	PBGSTA	65	G4DVNA
17	CODE	67	ETCPN
19	SSDO	69	PAAVA
21	PCG2VA	71	G2DVA
23	X5C	73	DINFVNA
25	EM1SN	75	EM1N
27		77	EMA
29	RESMVA	79	DM2B
31	ZGC	81	G6DVA
33	DM1SA	83	ADVNA
35	ICR4NA	85	W5C
37	ICRVA	87	V1
39	FCAVA	89	PS1B
41	ICR2NA	91	Y8C
43	Z9B	93	SS1
45	G4DVA	95	DO2
47	EM3N	97	SIGRET
49	V3		

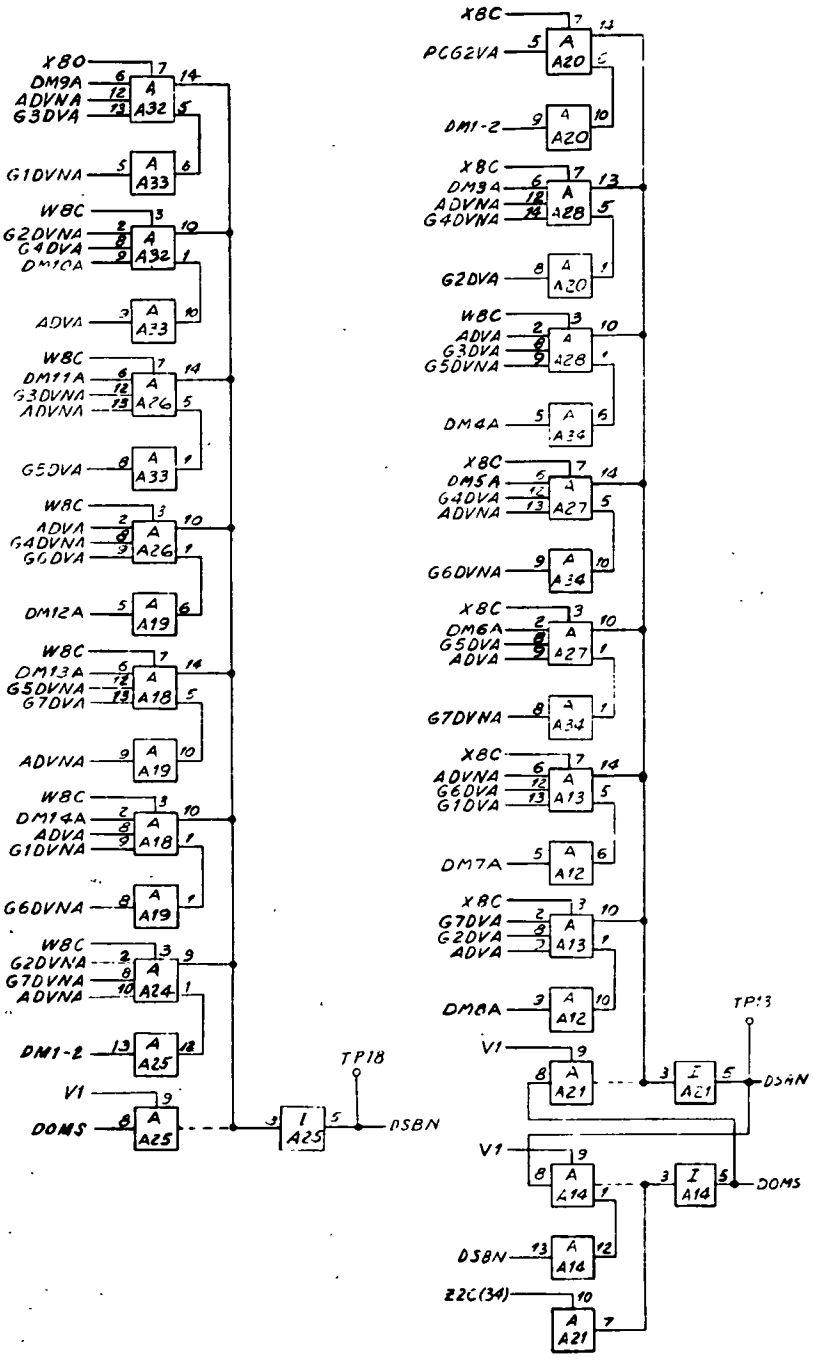
ULD LOCATIONS

A1 321	A2 322	A3	A4 I	A5	A6 322	A7 321
A8	A9 323	A10 I	A11 I	A12 AA	A13 323	A14
A15 321	A16 AA	A17 I	A18 AB	A19 I	A20 AA	A21 323
A22 322	A23 AB	A24 I	A25 AA	A26 I	A27 AA	A28 322
A29 323	A30 AA	A31	A32 AA	A33	A34 AB	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A22 Side A.
6. This Drawing Derived From IBM DWG NO. 6112817-REL(66123FN)

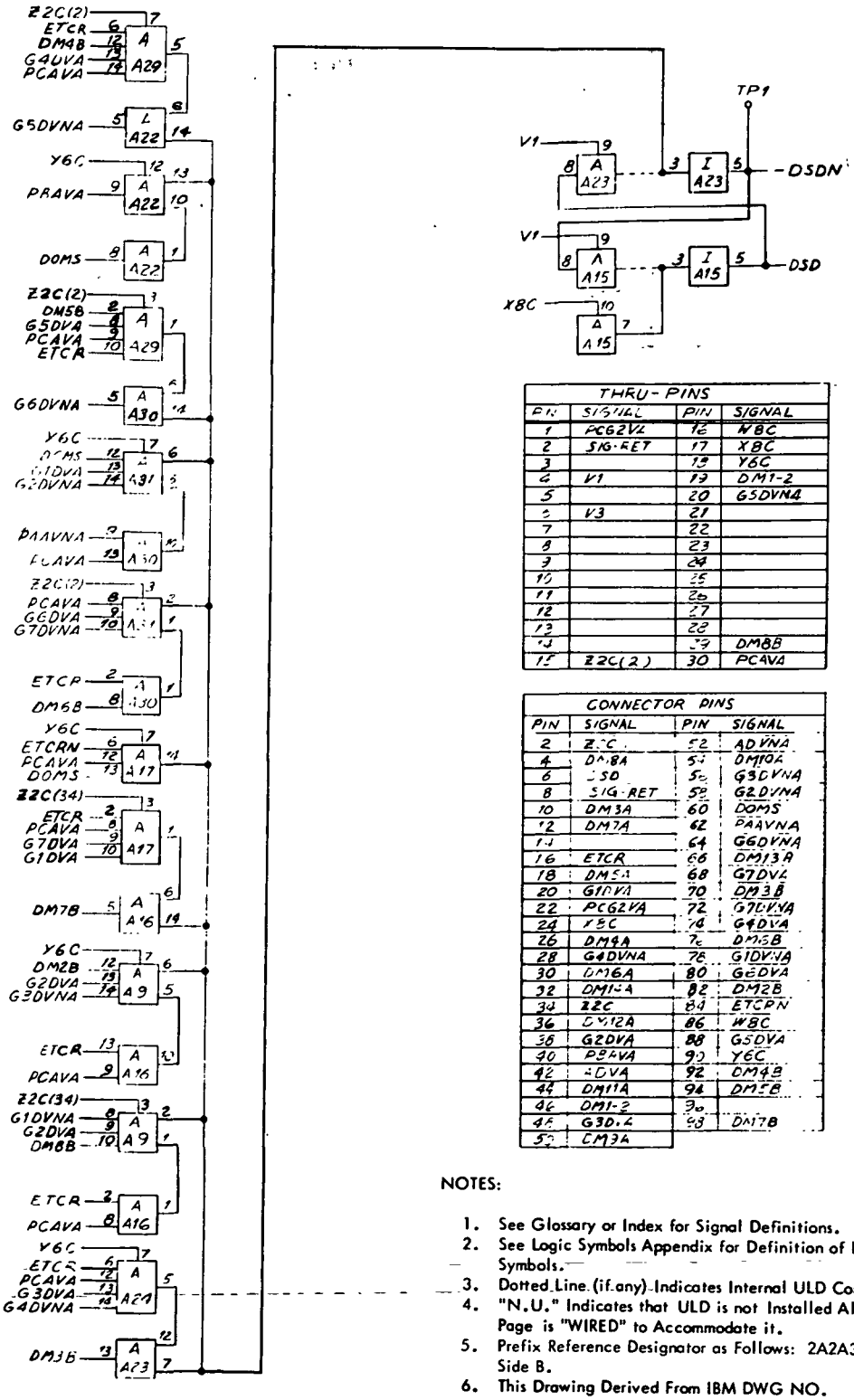
Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 12)



ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9 AA	A10	A11	A12 AB	A13 AC	A14 I
A15 I	A16 AB	A17 AA	A18 AA	A19 AB	A20 AE	A21 I
A22 AB	A23 I	A24 AA	A25 I	A26 AC	A27 AA	A28 AA
A29 AA	A30 AB	A31 AA	A32 AA	A33 AB	A34 AB	A35

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 13)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	PCG2VL	12	X8C
2	SIG·RET	17	X8C
3		19	Y6C
4	V1	19	DM1-2
5		20	G5DVNA
6	V3	21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	DM8B
15	Z2C(2)	30	PCAVA

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	Z2C	52	ADVNA
4	DM8A	54	DM10A
6	-SD	56	G3DVNA
8	SIG·RET	58	G2DVNA
10	DM3A	60	DOMS
12	DM7A	62	PAAVNA
14		64	G6DVNA
16	ETCR	66	DM13A
18	DM5A	68	G7DVL
20	G1DVA	70	DM3B
22	PCG2VA	72	G7DVNA
24	Y6C	74	G4DVA
26	DM9A	76	DM5B
28	G4DVNA	78	G1DVNA
30	DM6A	80	G6DVA
32	DM11A	82	DM2B
34	Z2C	84	ETCRN
36	DM12A	86	W8C
38	G2DVA	88	G5DVA
40	PRAVA	90	Y6C
42	ADVA	92	DM4B
44	DM11A	94	DM5B
46	DM1-2	96	
48	G3DVL	98	DM7B
50	DM3A		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A31 Side B.
6. This Drawing Derived From IBM DWG NO. 6112538-REL(66123CS)

Figure 10-9. Internal Data Sampler Logic Diagram (Sheet 14)

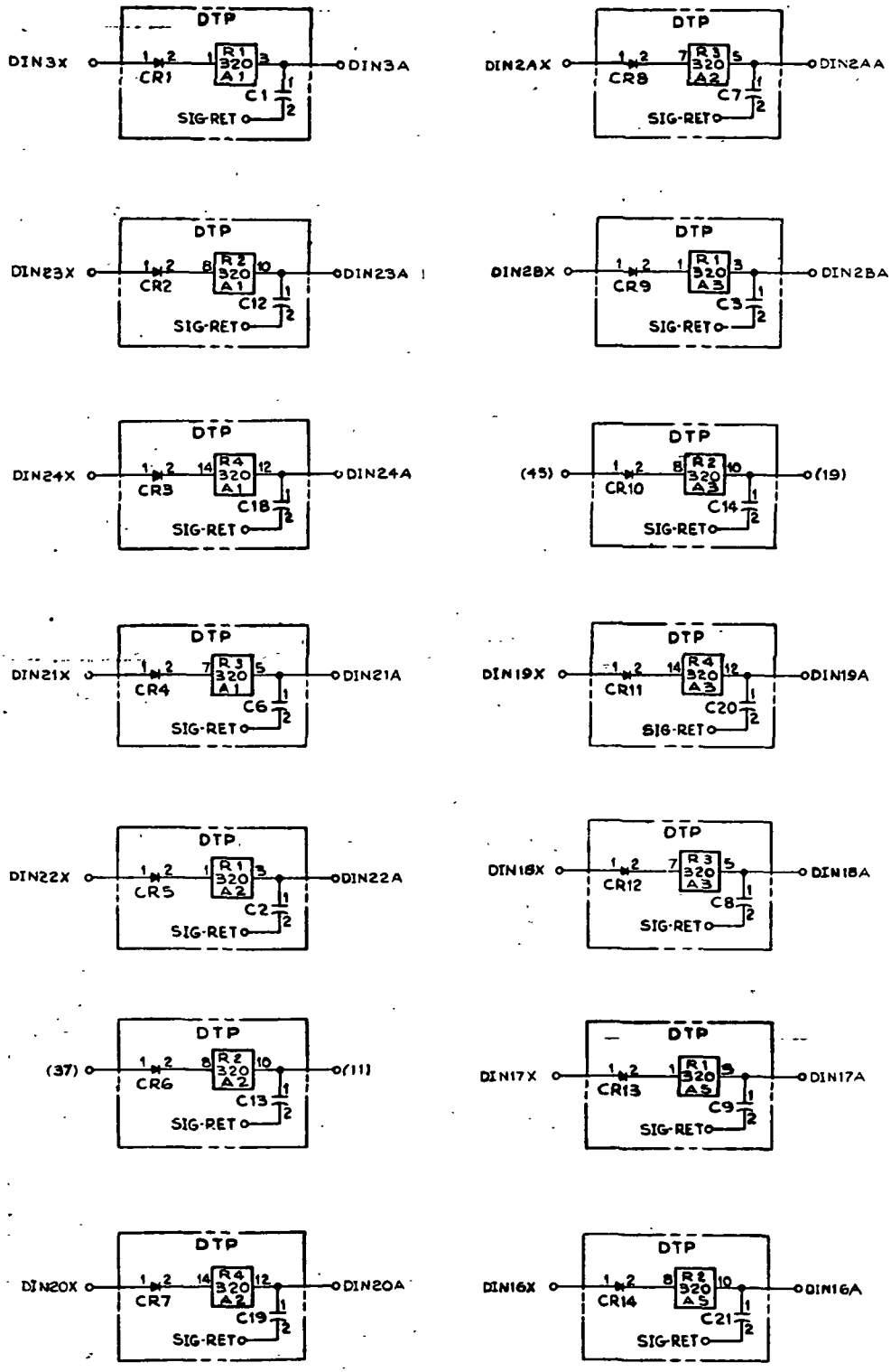
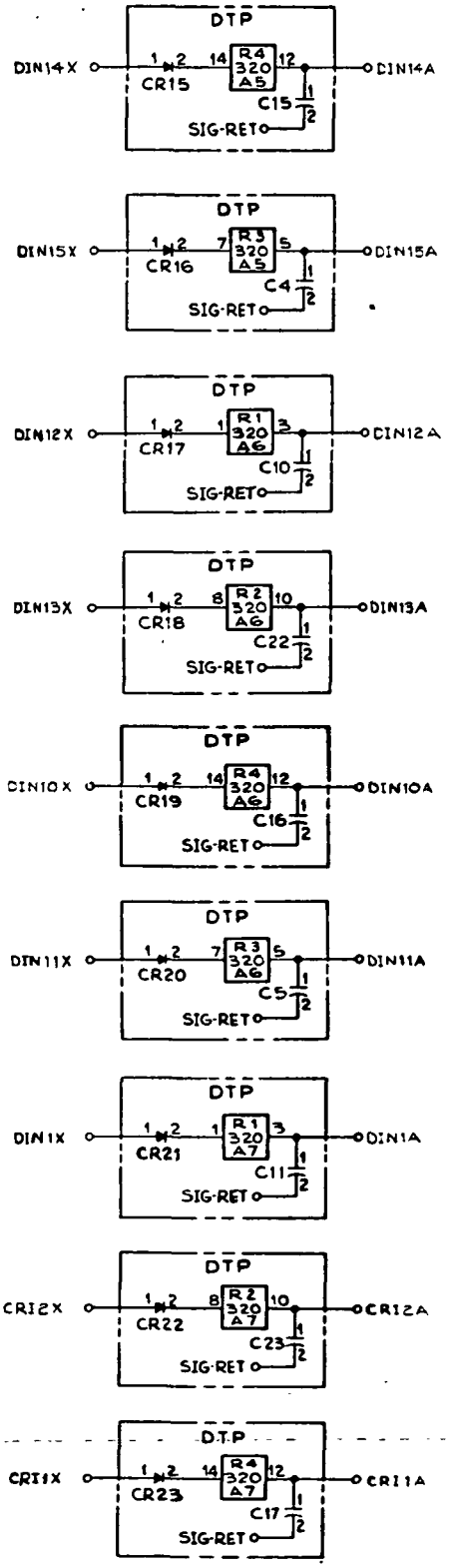


Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 1 of 10)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	DIN3A	51	DIN17X
3	DIN23A	53	DIN16X
5	DIN24A	55	DIN14X
7	DIN21A	57	DIN15X
9	DIN22A	59	DIN12X
11		61	DIN13X
13	DIN20A	63	DIN10X
15	DIN2AA	65	DIN11X
17	DIN2BA	67	DIN1X
19		69	CR12X
21	DIN19A	71	CR1X
23	DIN18A	73	SIG-RET
25	SIG-RET	75	DIN17A
27	DIN3X	77	DIN16A
29	DIN23X	79	DIN14A
31	DIN24X	81	DIN15A
33	DIN21X	83	DIN12A
35	DIN22X	85	DIN13A
37		87	DIN10A
39	DIN20X	89	DIN11A
41	DIN2AX	91	DIN1A
43	DIN2BX	93	CR12A
45		95	CR11A
47	DIN19X	97	
49	DIN18X		

COMPONENT LOCATIONS

C1	C2	C3	C4	C5		
C6	C7	C8	C9	C10	C11	
C12	C13	C14	C15	C16	C17	
C18	C19	C20	C21	C22	C23	
A1 320	A2 320	A3 320	A4	A5 320	A6 320	A7 320

CR1 ——— CR23

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A19 Side A.
6. This Drawing Derived From IBM DWG NO. 6112847-REL(66123FN)

Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 2)

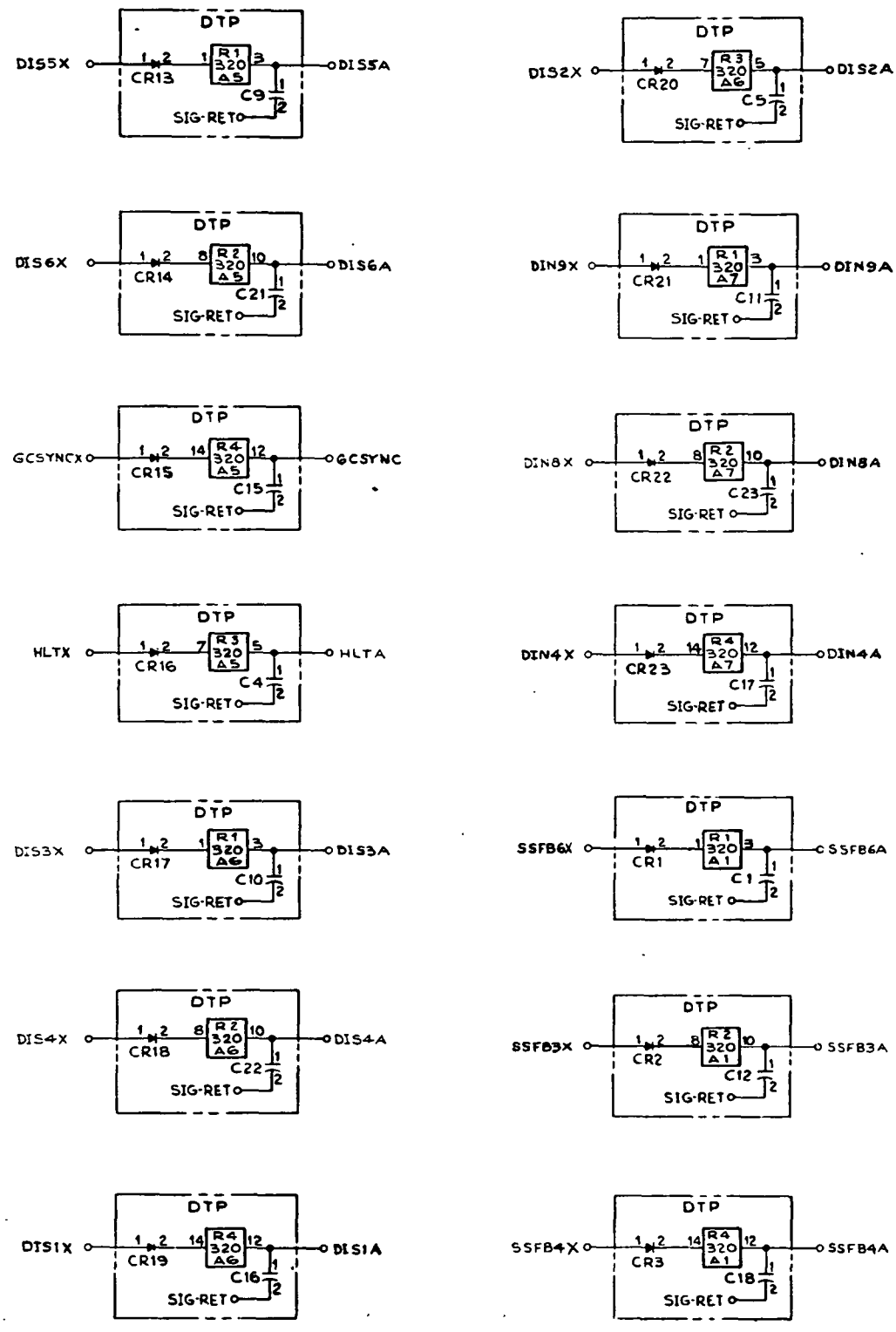
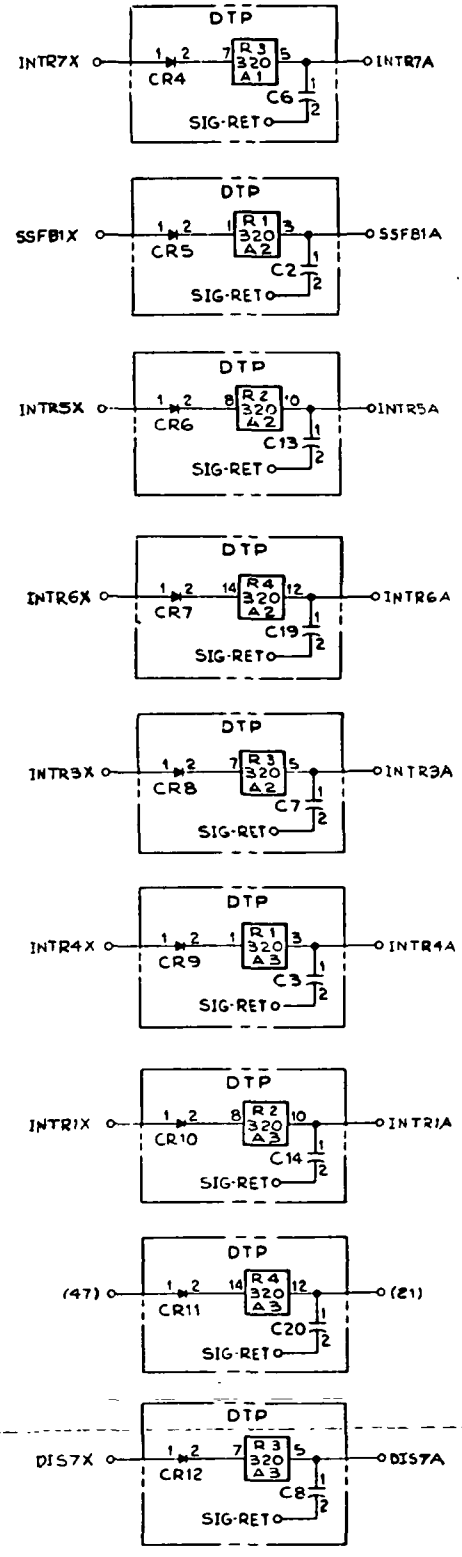


Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	SSFB6A	51	DIS5X
3	SSFB3A	53	DIS6X
5	SSFB4A	55	GCSYNCX
7	INTR7A	57	HLTX
9	SSFB1A	59	DIS3X
11	INTR5A	61	DIS4X
13	INTR6A	63	DIS1X
15	INTR3A	65	DIS2X
17	INTR4A	67	DIN9X
19	INTR1A	69	DIN8X
21		71	DIN4X
23	DIS7A	73	SIG-RET
25	SIG-RET	75	DIS5A
27	SSFB6X	77	DIS6A
29	SSFB3X	79	GCSYNC
31	SSFB4X	81	HLTA
33	INTR7X	83	DIS3A
35	SSFB1X	85	DIS4A
37	INTR5X	87	DIS1A
39	INTR6X	89	DIS2A
41	INTR3X	91	DIN9A
43	INTR4X	93	DIN8A
45	INTR1X	95	DIN4A
47		97	
49	DIS7X		

COMPONENT LOCATIONS

C1	C2	C3	C4	C5	
C6	C7	C8	C9	C10	C11
C12	C13	C14	C15	C16	C17
C18	C19	C20	C21	C22	C23

A1 320	A2 320	A3 320	A4	A5 320	A6 320	A7 320

CR1 ——— CR23

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A22 Side A.
6. This Drawing Derived From IBM DWG NO. 6112849-REL(66123FN)

Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 4)

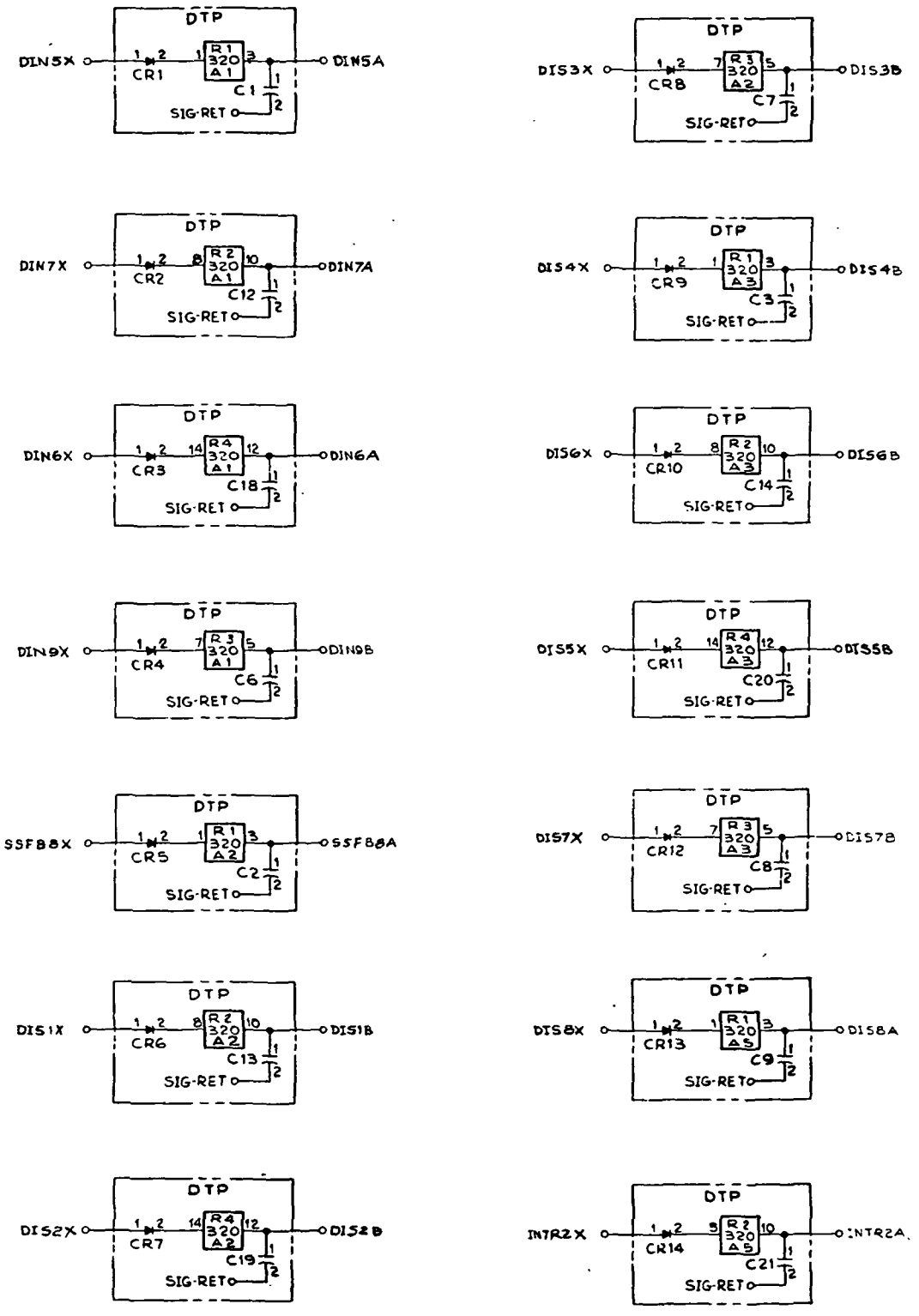
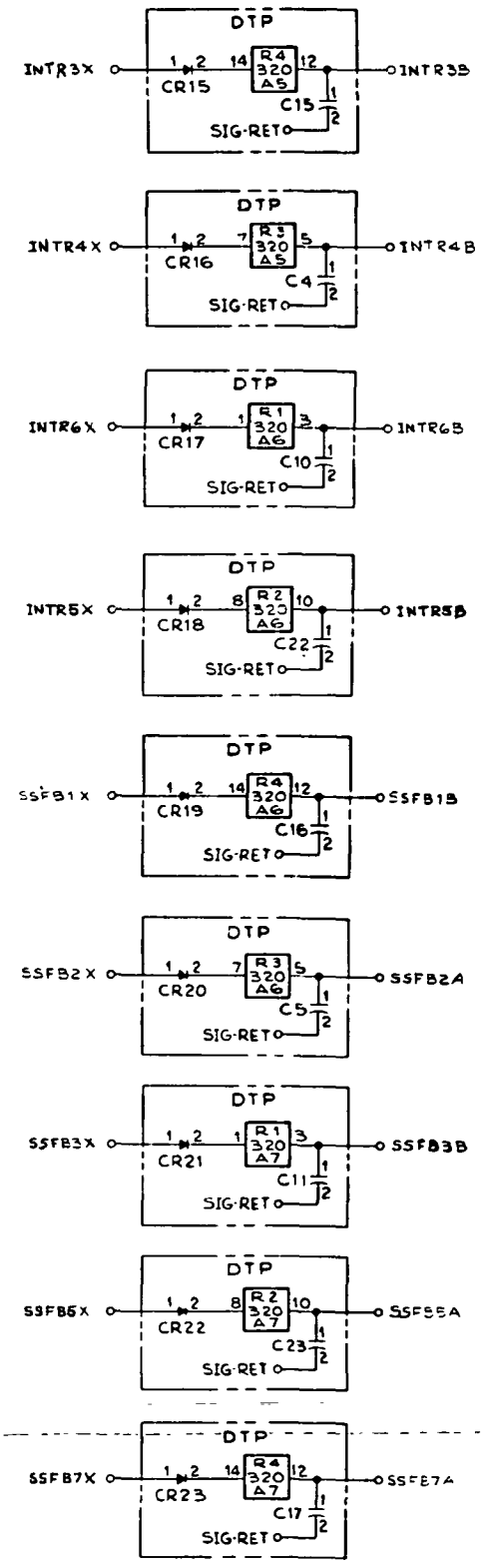


Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 5)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	DIS5X
4	SSFB7A	54	DIS6X
6	SSFB5A	56	DIS4X
8	SSFB3B	58	DIS3X
10	SSFB2A	60	DIS2X
12	SSFB1B	62	DIS1X
14	INTR5B	64	SSFB5X
16	INTR6B	66	DIN9X
18	INTR4B	68	DIN8X
20	INTR3B	70	DIN7X
22	INTR2A	72	DIN5X
24	DIS8A	74	SIG-RET
26	SIG-RET	76	DIS7B
28	SSFB7X	78	DIS5B
30	SSFB5X	80	DIS6B
32	SSFB3X	82	DIS4B
34	SSFB2X	84	DIS3B
36	SSFB1X	86	DIS2B
38	INTR5X	88	DIS1B
40	INTR6X	90	SSFB5A
42	INTR4X	92	DIN9B
44	INTR3X	94	DIN6A
46	INTR2X	96	DIN7A
48	DIS8X	98	DIN5A
50	DIS7X		

COMPONENT LOCATIONS

C1	C2	C3	C4	C5		
C6	C7	C8	C9	C10	C11	
C12	C13	C14	C15	C16	C17	
C18	C19	C20	C21	C22	C23	
A1 320	A2 320	A3 320	A4	A5 320	A6 320	A7 320

CR1 ——— CR23

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A22 Side B.
6. This Drawing Derived From IBM DWG NO. 6112637-REL(66123FN)

Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 6)

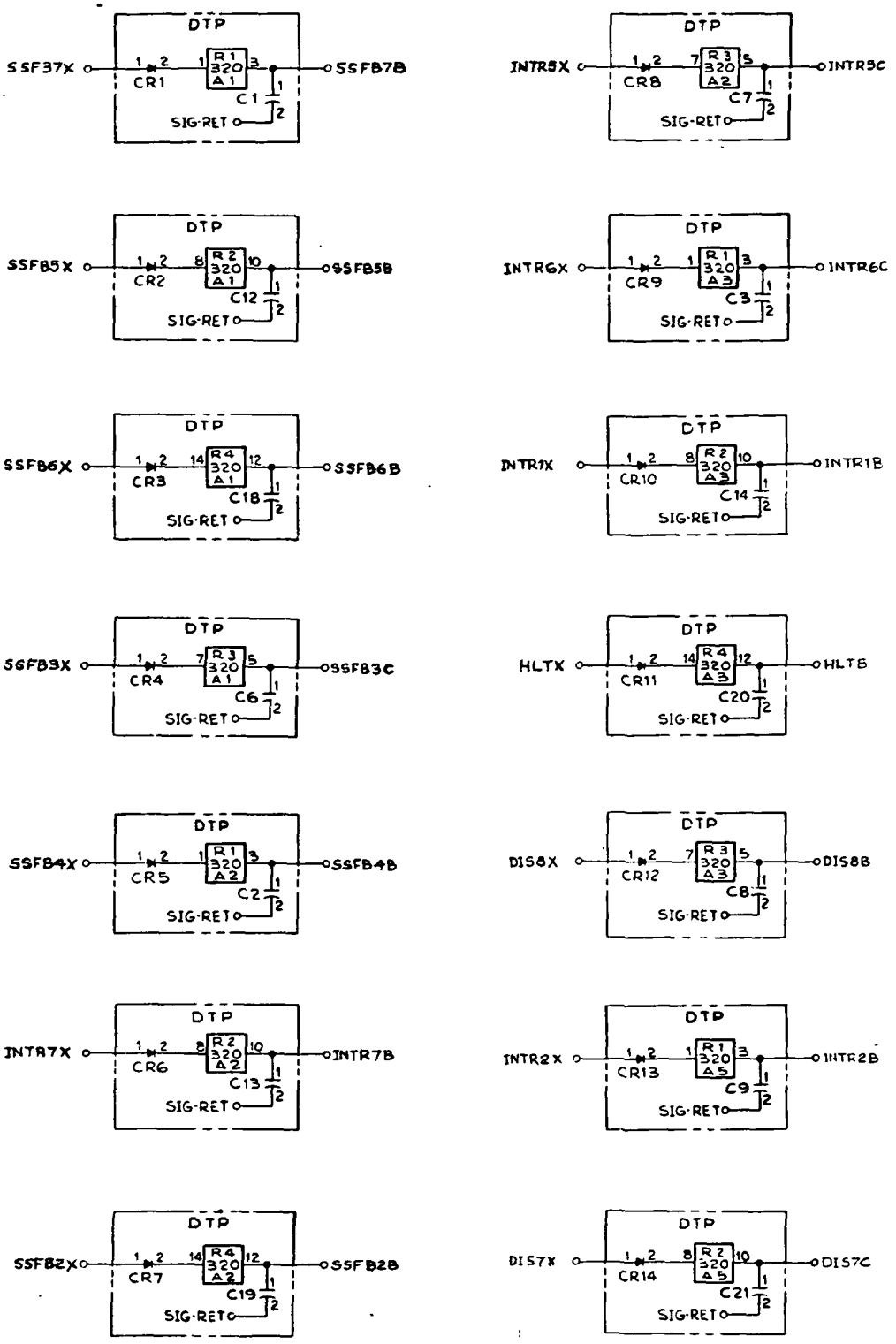
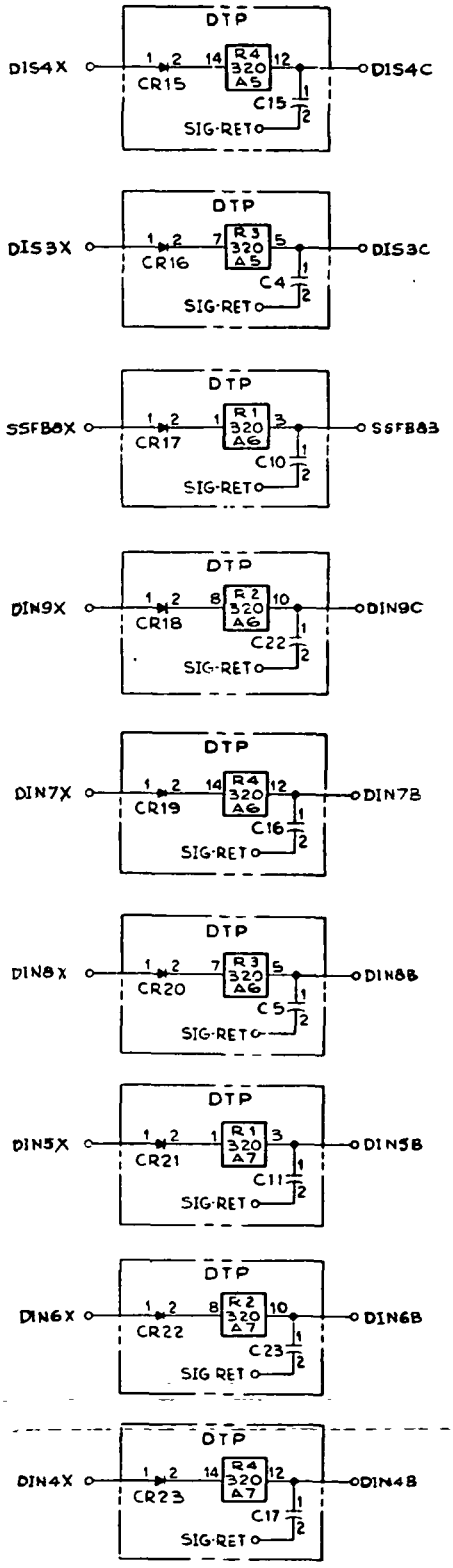


Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 7)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	SSFB7B	51	INTR2X
3	SSFB5B	53	DIS7X
5	SSFB6B	55	DIS4X
7	SSFB3C	57	DIS3X
9	SSFB4B	59	SSFB8X
11	INTR7B	61	DIN9X
13	SSFB2B	63	DIN7X
15	INTR5C	65	DIN8X
17	INTR6C	67	DIN5X
19	INTR1B	69	DIN6X
21	HLTB	71	DIN4X
23	DIS8B	73	SIG-RET
25	SIG-RET	75	INTR2B
27	SSFB7X	77	DIS7C
29	SSFB5X	79	DIS4C
31	SSFB6X	81	DIS8C
33	SSFB3X	83	SSFB8B
35	SSFB4X	85	DIN9C
37	INTR7X	87	DIN7B
39	SSFB2X	89	DIN8B
41	INTR5X	91	DIN5B
43	INTR6X	93	DIN6B
45	INTR1X	95	DIN4B
47	HLTX	97	
49	DIS8X		

COMPONENT LOCATIONS

C1	C2	C3	C4	C5		
C6	C7	C8	C9	C10	C11	
C12	C13	C14	C15	C16	C17	
C18	C19	C20	C21	C22	C23	
A1 320	A2 320	A3 320	A4	A5 320	A6 320	A7 320

CR1 ——— CR23

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." *Indicates that ULD is not Installed Although* Page is "WIRED" to Accommodate it.
5. *Prefix Reference Designator as Follows:* 2A1A23 Side A.
6. This Drawing Derived From IBM DWG NO. 6112149-REL(66123FM)

Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 8)

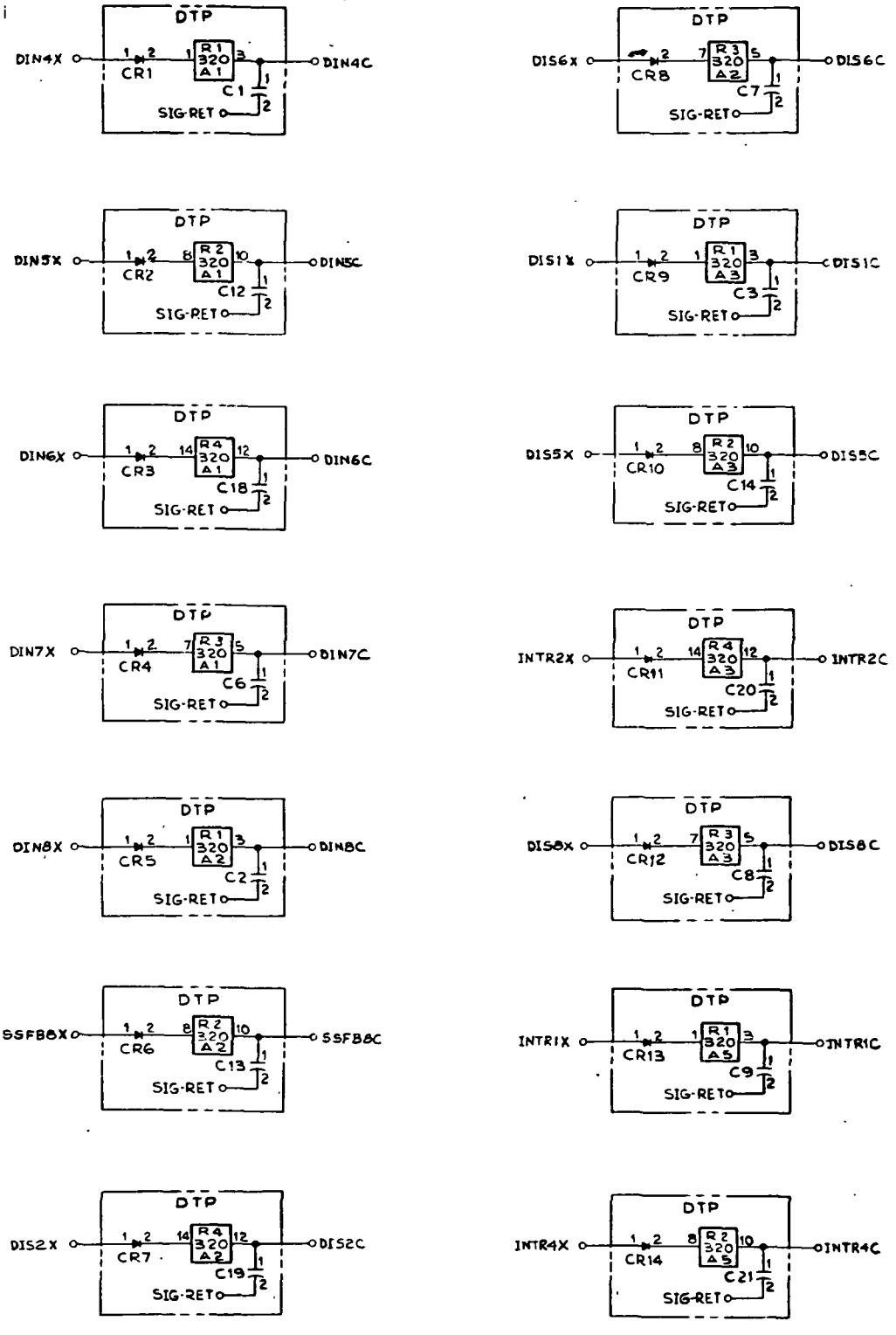
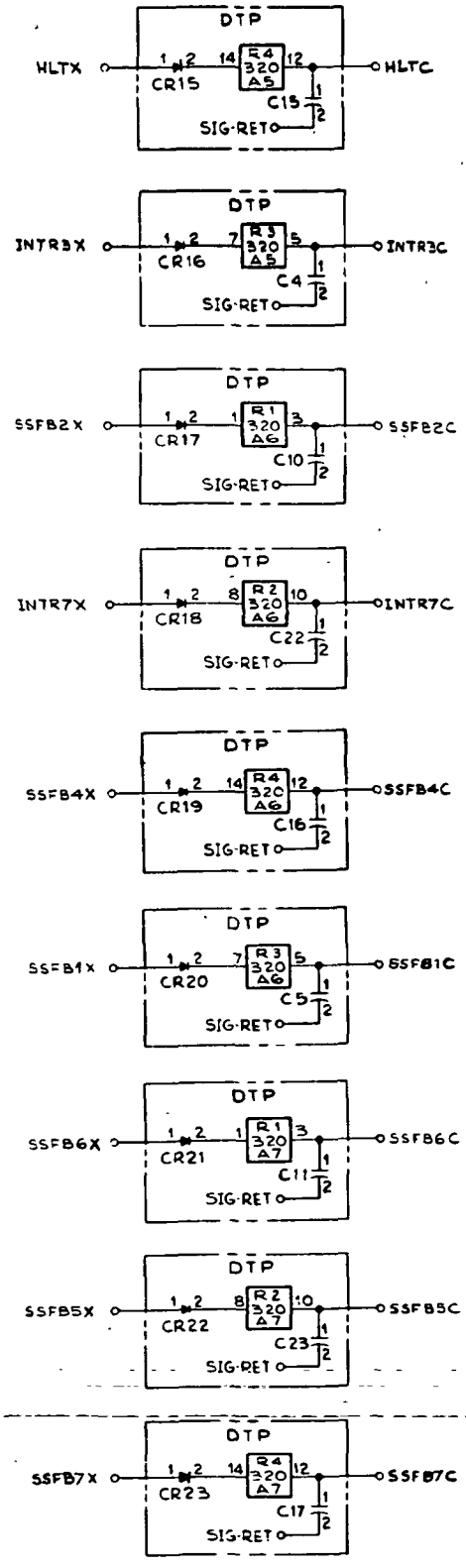


Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 9)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	INTR2X
4	SSFB7C	54	DIS5X
6	SSFB5C	56	DIS1X
8	SSFB6C	58	DIS6X
10	SSFB1C	60	DIS2X
12	SSFB4C	62	SSFB8X
14	INTR7C	64	DIN8X
16	SSFB2C	66	DIN7X
18	INTR3C	68	DIN6X
20	HLTC	70	DIN5X
22	INTR4C	72	DIN4X
24	INTR1C	74	SIG·RET
26	SIG·RET	76	DIS8C
28	SSFB7X	78	INTR2C
30	SSFB5X	80	DIS5C
32	SSFB6X	82	DIS1C
34	SSFB1X	84	DIS6C
36	SSFB4X	86	DIS2C
38	INTR7X	88	SSFB8C
40	SSFB2X	90	DIN8C
42	INTR3X	92	DIN7C
44	HLTX	94	DIN6C
46	INTR4X	96	DIN5C
48	INTR1X	98	DIN4C
50	DIS8X		

COMPONENT LOCATIONS

C1	C2	C3	C4	C5		
C6	C7	C8	C9	C10	C11	
C12	C13	C14	C15	C16	C17	
C18	C19	C20	C21	C22	C23	
A1 320	A2 320	A3 320	A4	A5 320	A6 320	A7 320

CR1 ——— CR23

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A23 Side B.
6. This Drawing Derived From IBM DWG NO. 6112589-REL(66123FN)

Figure 10-10. System Data Sampler (Discrete Transient Protectors) Logic Diagram (Sheet 10)

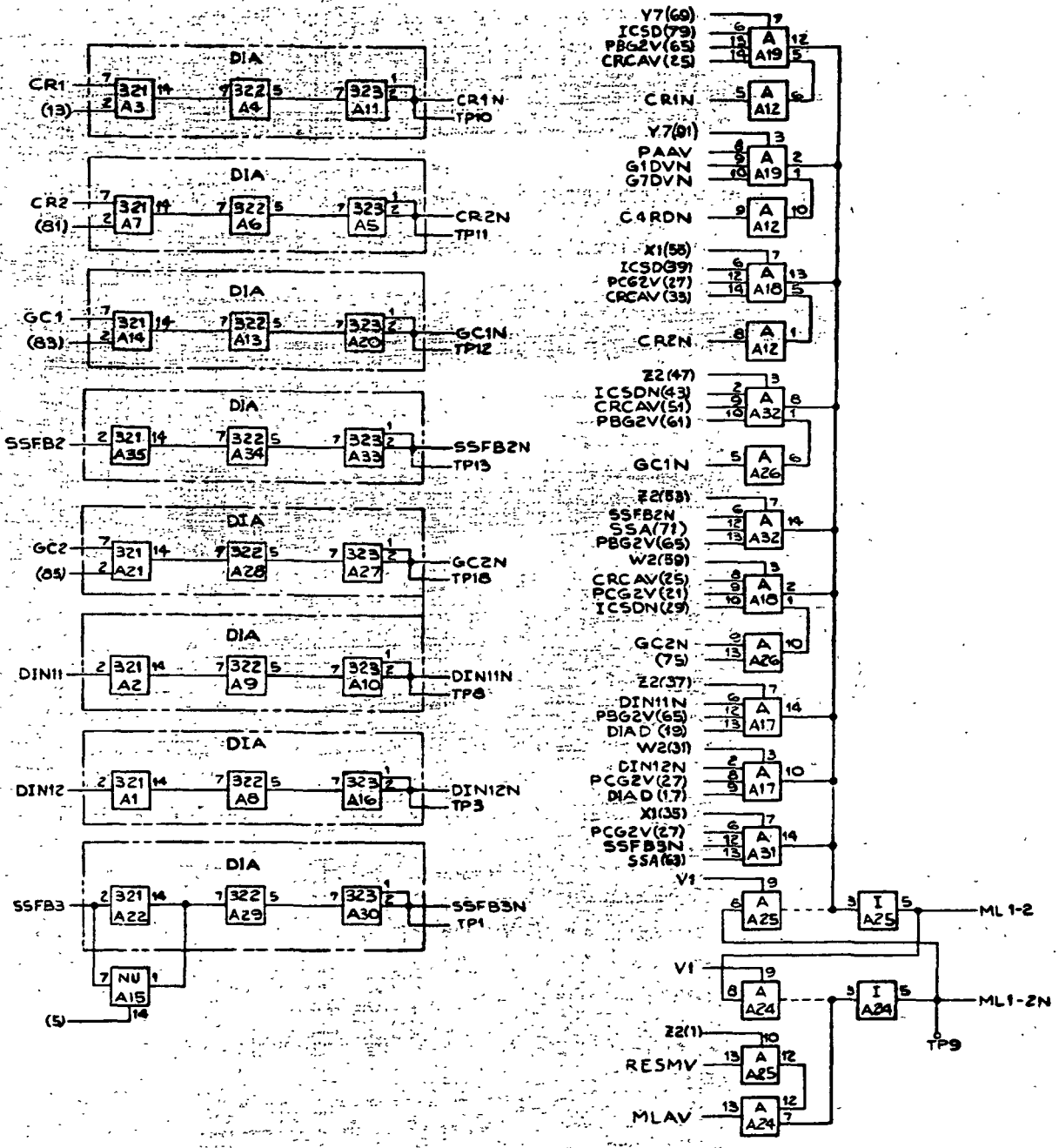
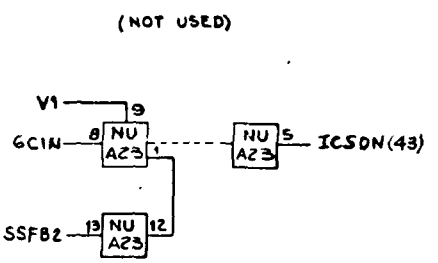


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 1 of 26)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	Z2	51	CRCAV
3	DIN12	53	Z2
5		55	X1
7	SSFB3	57	ML1-2
9	SIG-RET	59	W2
11	DIN11	61	PBG2V
13		63	SSA
15	CR1	65	PBG2V
17	DIAD	67	RESMV
19	DIAD	69	Y7
21	PCG2V	71	SSA
23	MLAV	73	G7DVN
25	CRCAV	75	
27	PCG2V	77	G1DVN
29	ICSDN	79	ICSD
31	W2	81	
33	CRCAV	83	
35	X1	85	
37	Z2	87	V1
39	ICSD	89	SSFB2
41	PAAV	91	Y7
43	ICSDN	93	GC2
45	C4RDN	95	GC1
47	Z2	97	CR2
49	V3		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
321	321	321	322	323	322	321
A8	A9	A10	A11	A12	A13	A14
322	322	323	323	AB	322	321
A15	A16	A17	A18	A19	A20	A21
	323	AA	AA	AA	323	321
A22	A23	A24	A25	A26	A27	A28
321		I	I	AB	323	322
A29	A30	A31	A32	A33	A34	A35
322	323	AA	AA	323	322	321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A24 Side A, 2A2A8 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112347-REL(66123ET)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 2)

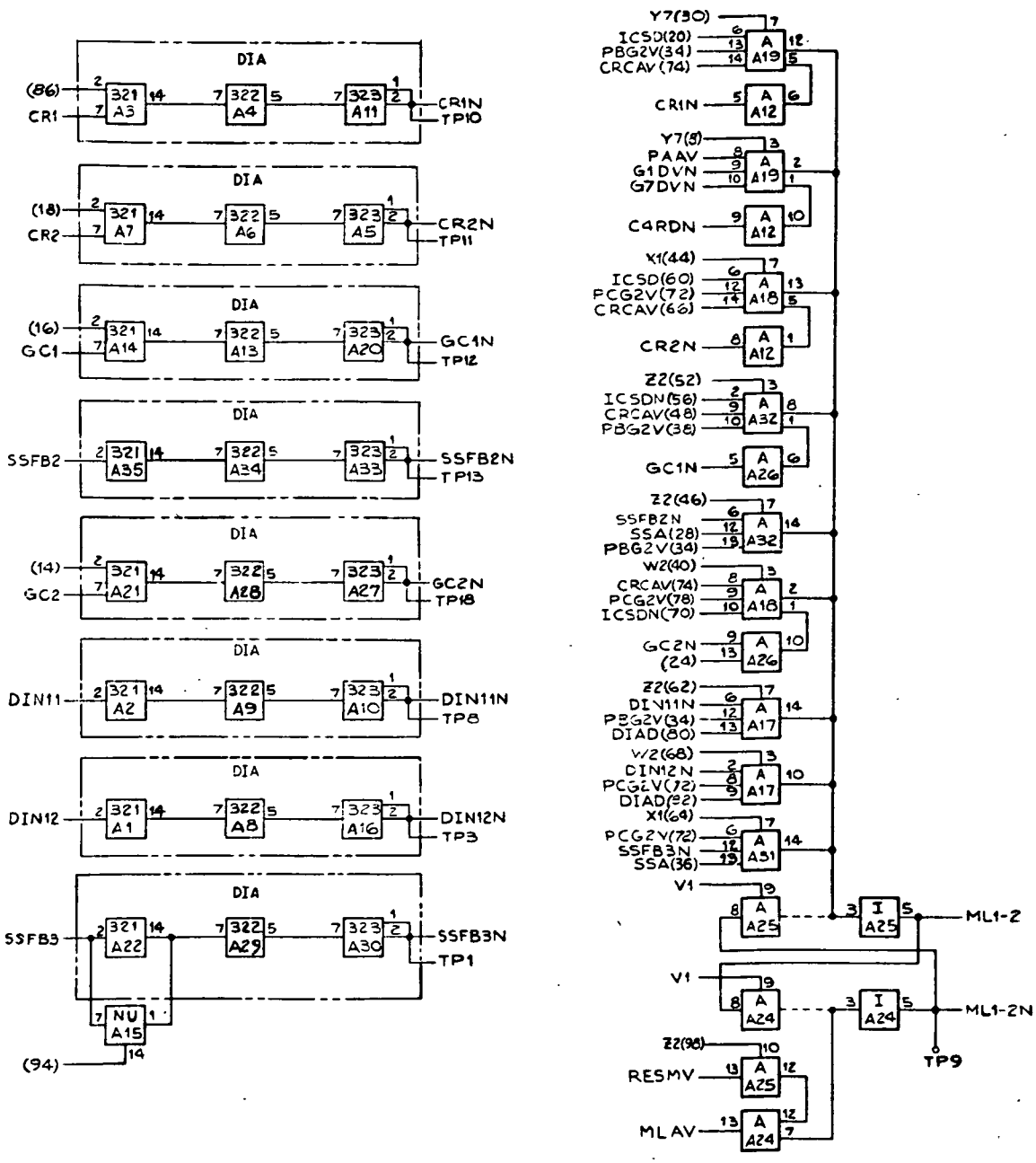
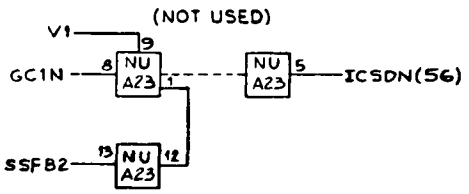


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CR2	52	Z2
4	GC1	54	C4RDN
6	GC2	56	ICSDN
8	Y7	58	PAAV
10	SSFB2	60	ICSD
12	V1	62	Z2
14		64	X1
16		66	CRCAV
18		68	W2
20	ICSD	70	ICSDN
22	G1DVN	72	PCG2V
24		74	CRCAV
26	G7DVN	76	MLAV
28	SSA	78	PCG2V
30	Y7	80	DIAD
32	RESMV	82	DIAD
34	PBG2V	84	CR1
36	SSA	86	
38	PBG2V	88	DIN11
40	W2	90	SIG RET
42	ML1-2	92	SSFB3
44	X1	94	
46	Z2	96	DIN12
48	CRCAV	98	Z2
50	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13 322	A14 321
A15	A16 323	A17 AA	A18 AA	A19 AA	A20 323	A21 321
A22 321	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32 AA	A33 323	A34 322	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A24 Side B.
6. This Drawing Derived From IBM DWG NO. 6112349-REL(66123DG)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 4)

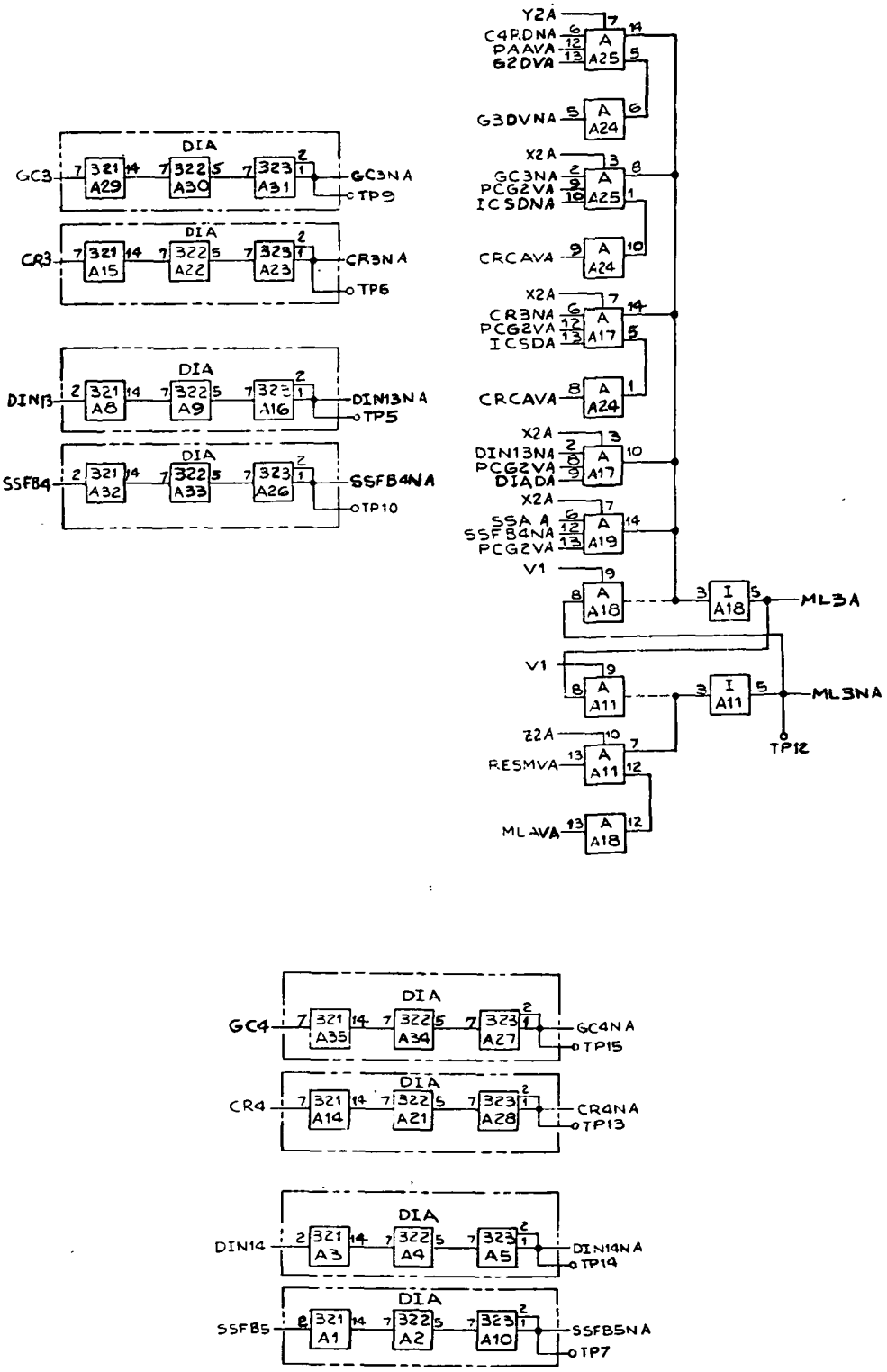
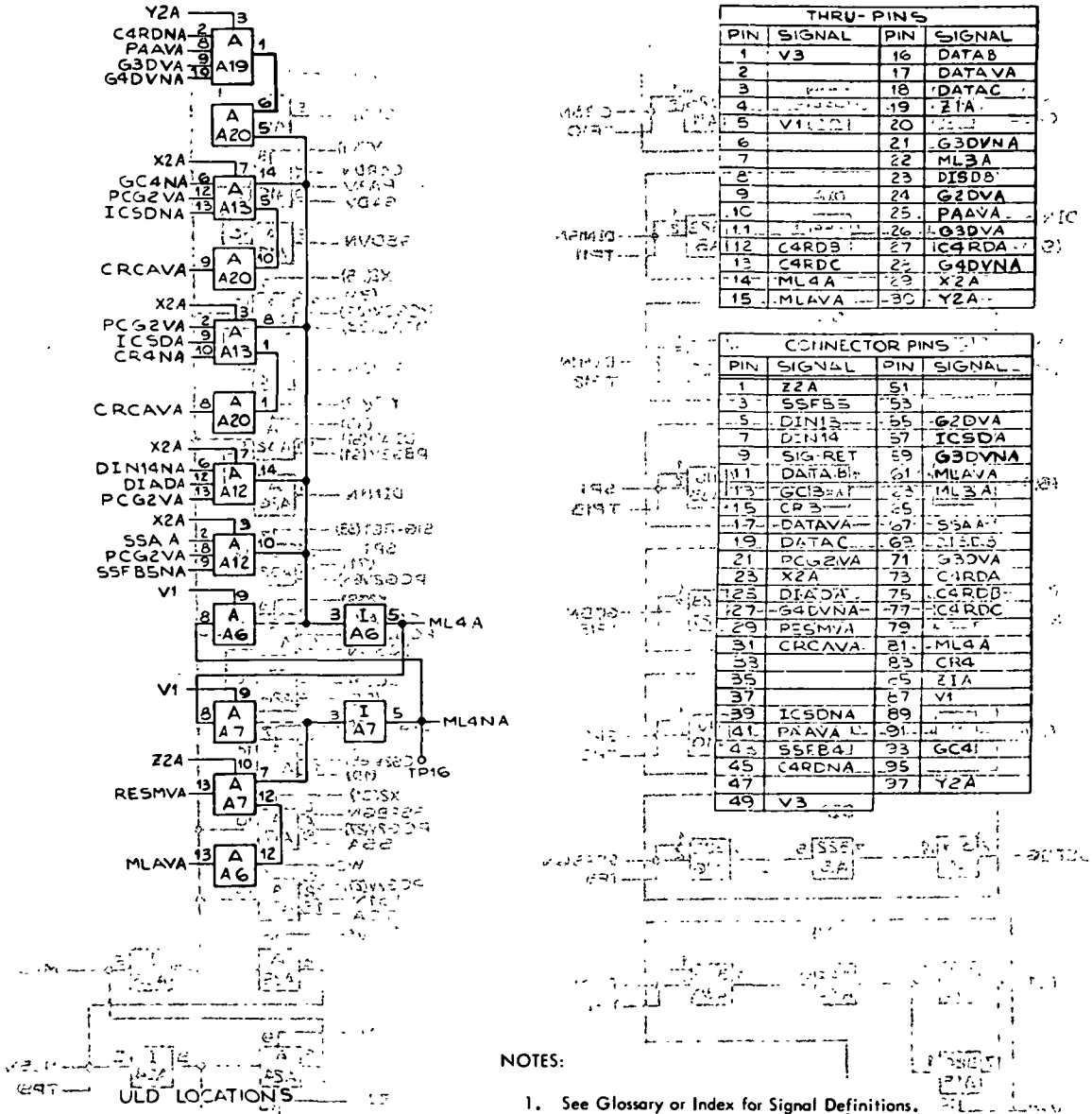


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 5)



THRU-PINS

PIN	SIGNAL	PIN	SIGNAL
1	V3	16	DATAB
2		17	DATAVA
3		18	DATAC
4		19	Z1A
5	V1	20	
6		21	G3DVNA
7		22	ML3A
8		23	DISDB
9		24	G2DVA
10		25	PAAVA
11		26	G3DVA
12	C4RDB	27	IC4RDA
13	C4RDC	28	G4DVNA
14	ML4A	29	X2A
15	MLAVA	30	Y2A

CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
1	Z2A	51	
3	SSFB5	53	
5	DIN13	55	G2DVA
7	DIN14	57	ICSDA
9	SIG RET	59	G3DVNA
11	DATA B	61	MLAVA
13	GC3	63	ML3A
15	CR3	65	
17	DATAVA	67	SSAA
19	DATAC	69	DISDB
21	PCG2VA	71	G3DVA
23	X2A	73	C1RDA
25	DIADA	75	C4RDB
27	G4DVNA	77	C4RDC
29	RESMVA	79	
31	CRCAVA	81	ML4A
33		83	CR4
35		85	Z1A
37		87	V1
39	ICSDNA	89	
41	PAAVA	91	
43	SSFB4	93	GC4
45	C4RDNA	95	
47		97	Y2A
49	V3		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A5 Side A.
6. This Drawing Derived From IBM DWG NO. 6112777-REL(66123CD)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 6)

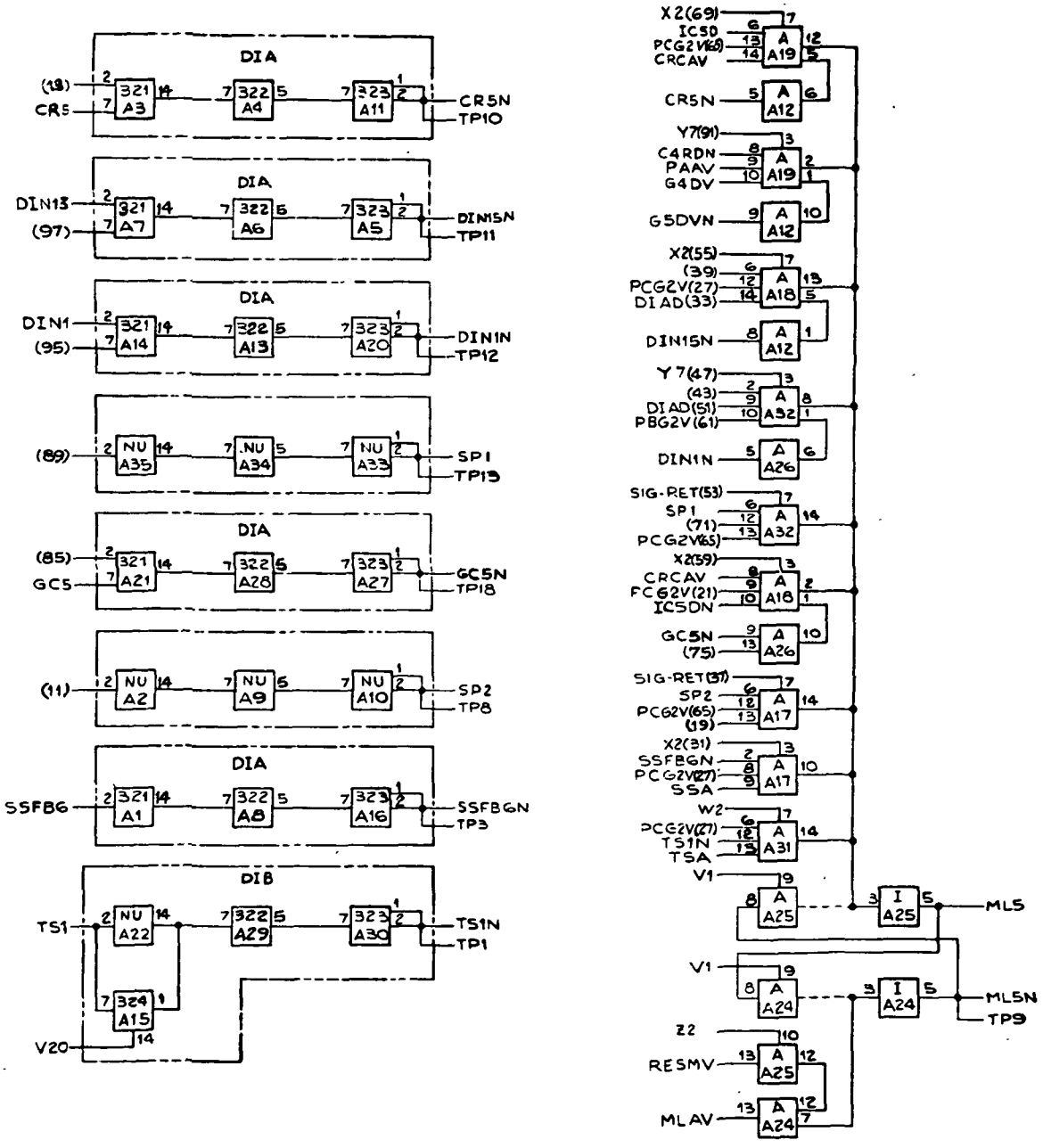
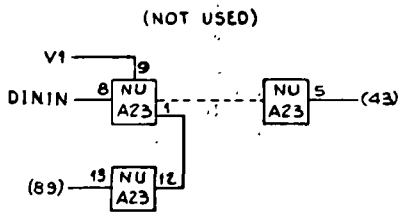


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 7)



CONNECTOR PIN			
PIN	SIGNAL	PIN	SIGNAL
1	Z2	51	DIAD
3	SSFBG	53	SIG-RET
5	V20	55	X2
7	TS1	57	ML5
9	SIG-RET	59	X2
11		61	PBG2V
13		63	TSA
15	CR5	65	PCG2V
17	SSA	67	RESMV
19		69	X2
21	PCG2V	71	
23	MLAV	73	G4DV
25	CRCAV	75	
27	PCG2V	77	PAAV
29	ICSDN	79	ICSD
31	X2	81	DIN15
33	DIAD	83	DIN1
35	W2	85	
37	SIG-RET	87	V1
39		89	
41	C4RDN	91	Y7
43		93	GC5
45	GSDVN	95	
47	Y7	97	
49	V3		

ULD LOCATIONS

A1 321	A2	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9	A10	A11 323	A12 AB	A13 322	A14 321
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20 323	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32 AA	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A1 Side A.
6. This Drawing Derived From IBM DWG NO. 6112867-REL(66123ET)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 8)

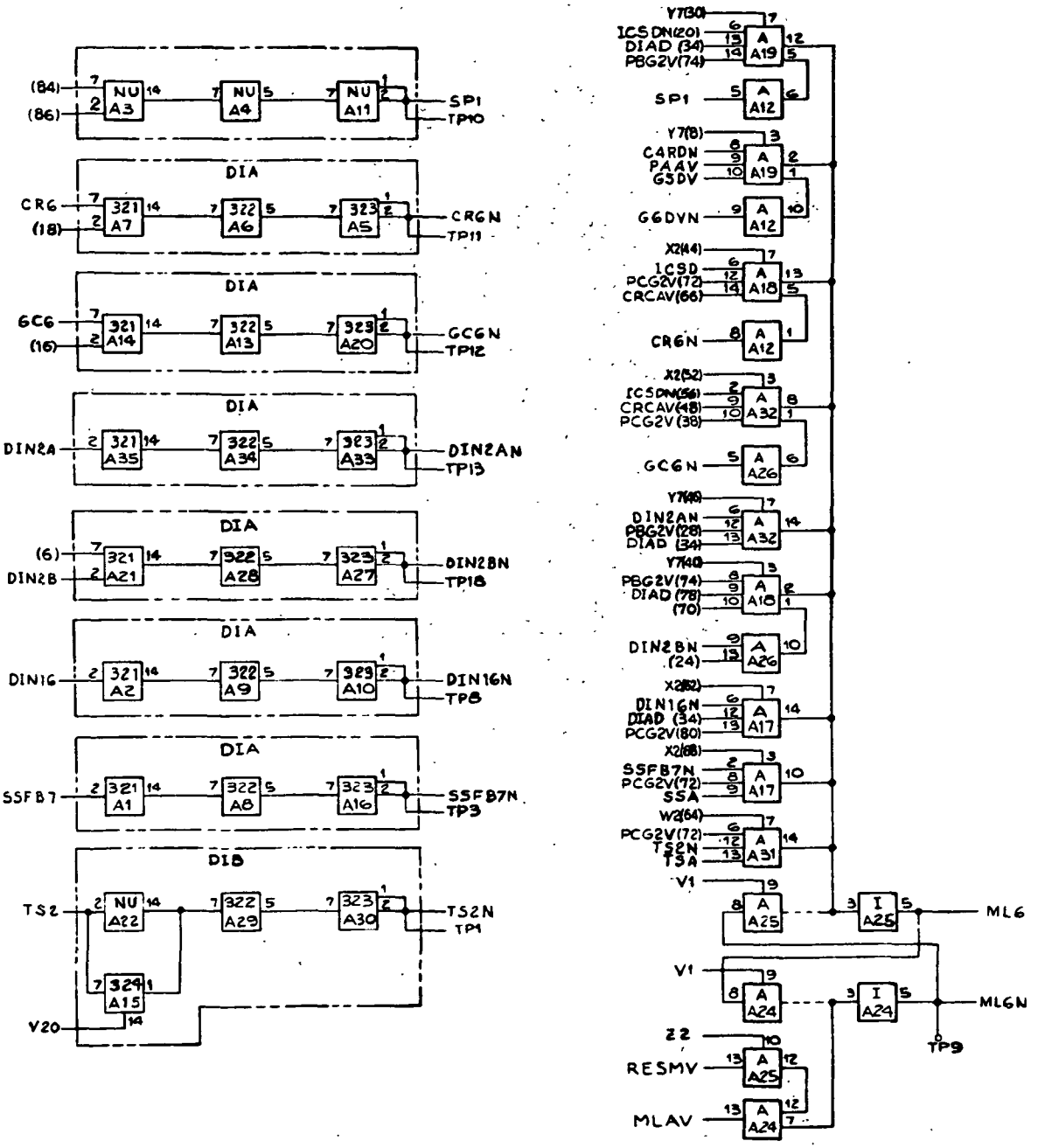
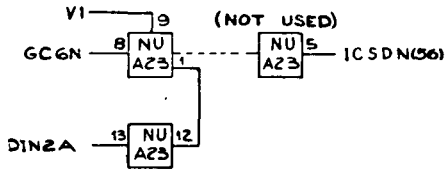


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 9)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CR6	52	X2
4	GC6	54	GGDVN
6		56	ICSDN
8	Y7	58	C4RDN
10	DIN2A	60	IC5D
12	V1	62	X2
14	DIN2B	64	W2
16		66	CRCAV
18		68	X2
20	ICSDN	70	
22	PAAV	72	PCG2V
24		74	PBG2V
26	G5DV	76	MLAV
28	PBG2V	78	DIAD
30	Y7	80	PCG2V
32	RESMV	82	SSA
34	DIAD	84	
36	TSA	86	
38	PCG2V	88	DIN16
40	Y7	90	SIG-RET
42	ML6	92	TS2
44	X2	94	V20
46	Y7	96	SSFBT
48	CRCAV	98	Z2
50	V3		

ULD LOCATIONS

A1 321	A2 321	A3	A4	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11	A12 AB	A13 322	A14 321
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20 323	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32 AA	A33 323	A34 322	A35 321

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A1 Side B.
6. This Drawing Derived From IBM DWG NO. 6112868-REL(66123FN)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 10)

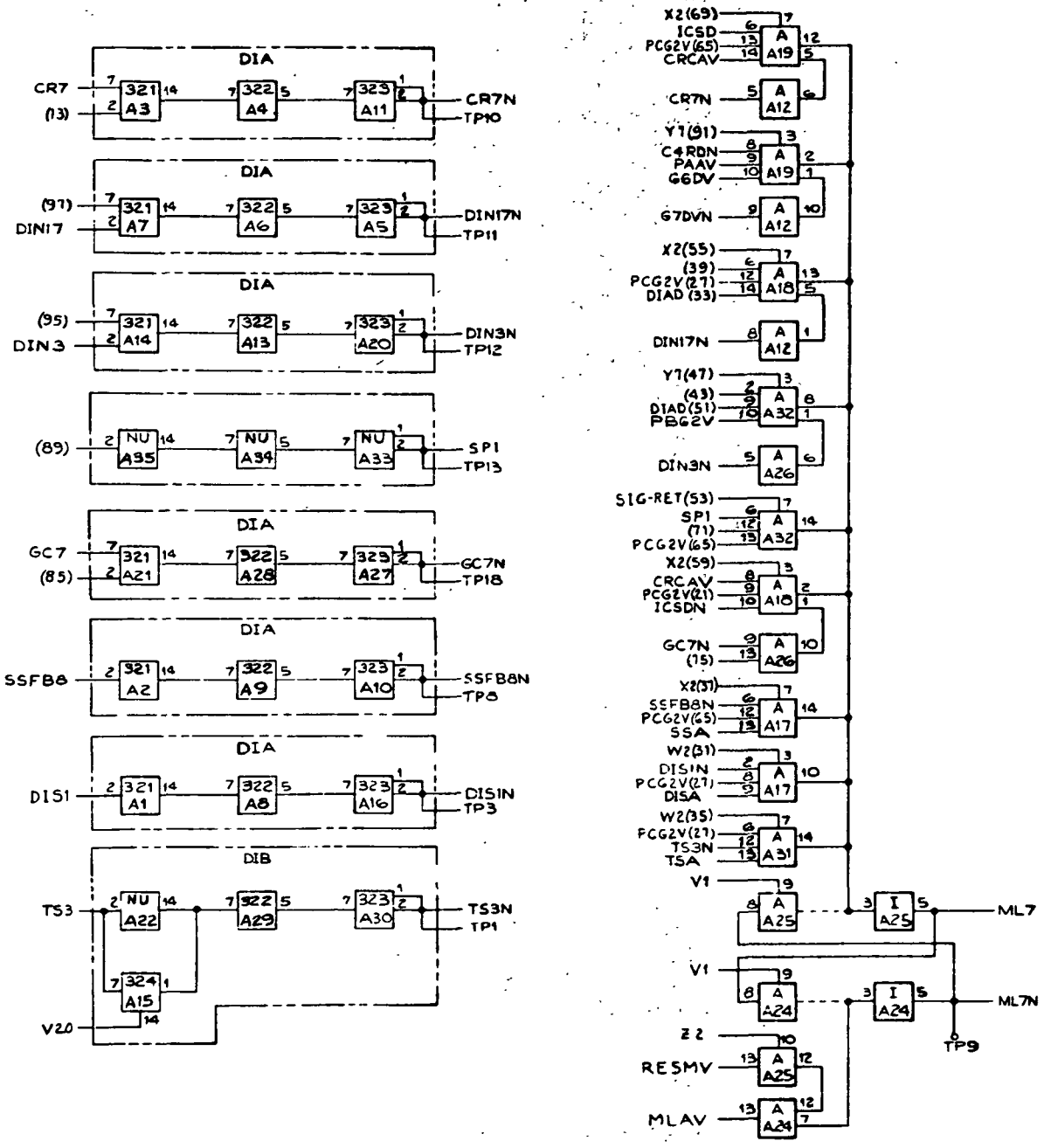
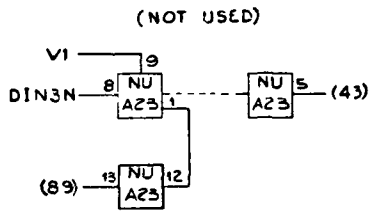


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 11)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	Z2	51	DIAD
3	DIST	53	SIG-RET
5	Y20	55	X2
7	TS3	57	ML7
9	SIG.-RET	59	X2
11	SSFB8	61	PBG2V
13		63	TSA
15	CR7	65	PCG2V
17	DISA	67	RESMV
19	SSA	69	X2
21	PCG2V	71	
23	MLAV	73	G6DV
25	CRCAV	75	
27	PCG2V	77	PAAV
29	ICSDN	79	ICSD
31	W2	81	DIN17
33	DIAD	83	DIN3
35	W2	85	
37	X2	87	V1
39		89	
41	C4RDN	91	Y7
43		93	GC7
45	G7DVN	95	
47	Y7	97	
49	V3		

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13 322	A14 321
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20 323	A21 321
A22	A23	A24 I	A25 J	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32 AA	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A3 Side A.
6. This Drawing Derived From IBM DWG NO. 6112869-REL(66123FN)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 12)

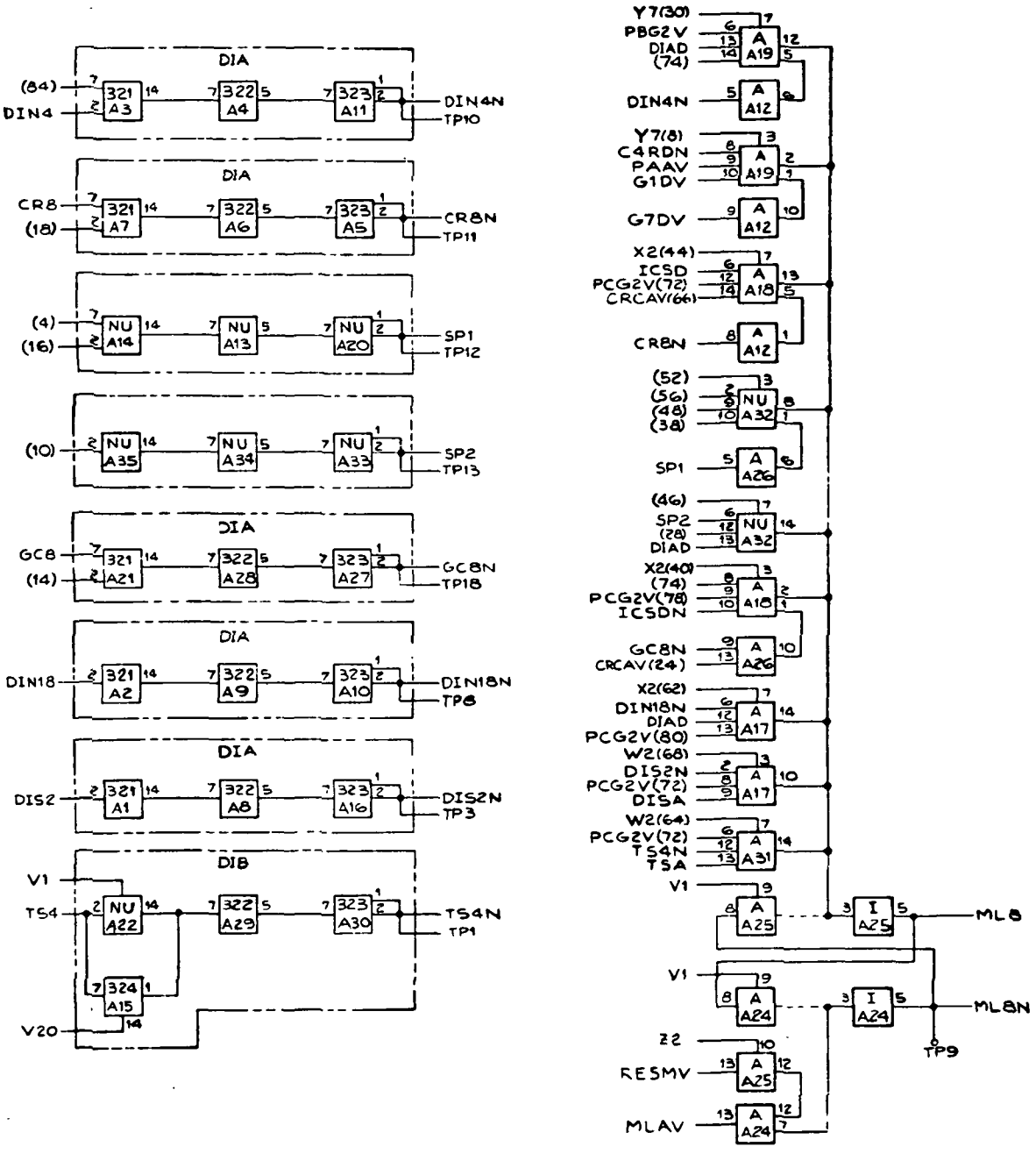
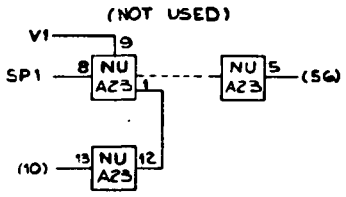


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 13)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CR8	52	
4		54	G7DV
6	GC8	56	
8	Y7	58	C4RDN
10		60	ICSD
12	V1	62	X2
14		64	W2
16		66	CRCAV
18		68	W2
20	PBG2V	70	ICSDN
22	PAAV	72	PCG2V
24	CRCAV	74	
26	G1DV	76	MLAV
28		78	PCG2V
30	Y7	80	PCG2V
32	RESMV	82	DISA
34	DIAD	84	
36	TSA	86	DIN4
38		88	DIN16
40	X2	90	SIG-RET
42	ML8	92	TS4
44	X2	94	V20
46		96	DIS2
48		98	B2
50	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13	A14
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A3 Side B.
6. This Drawing Derived From IBM DWG NO. 6112369-REL(66123ET)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 14)

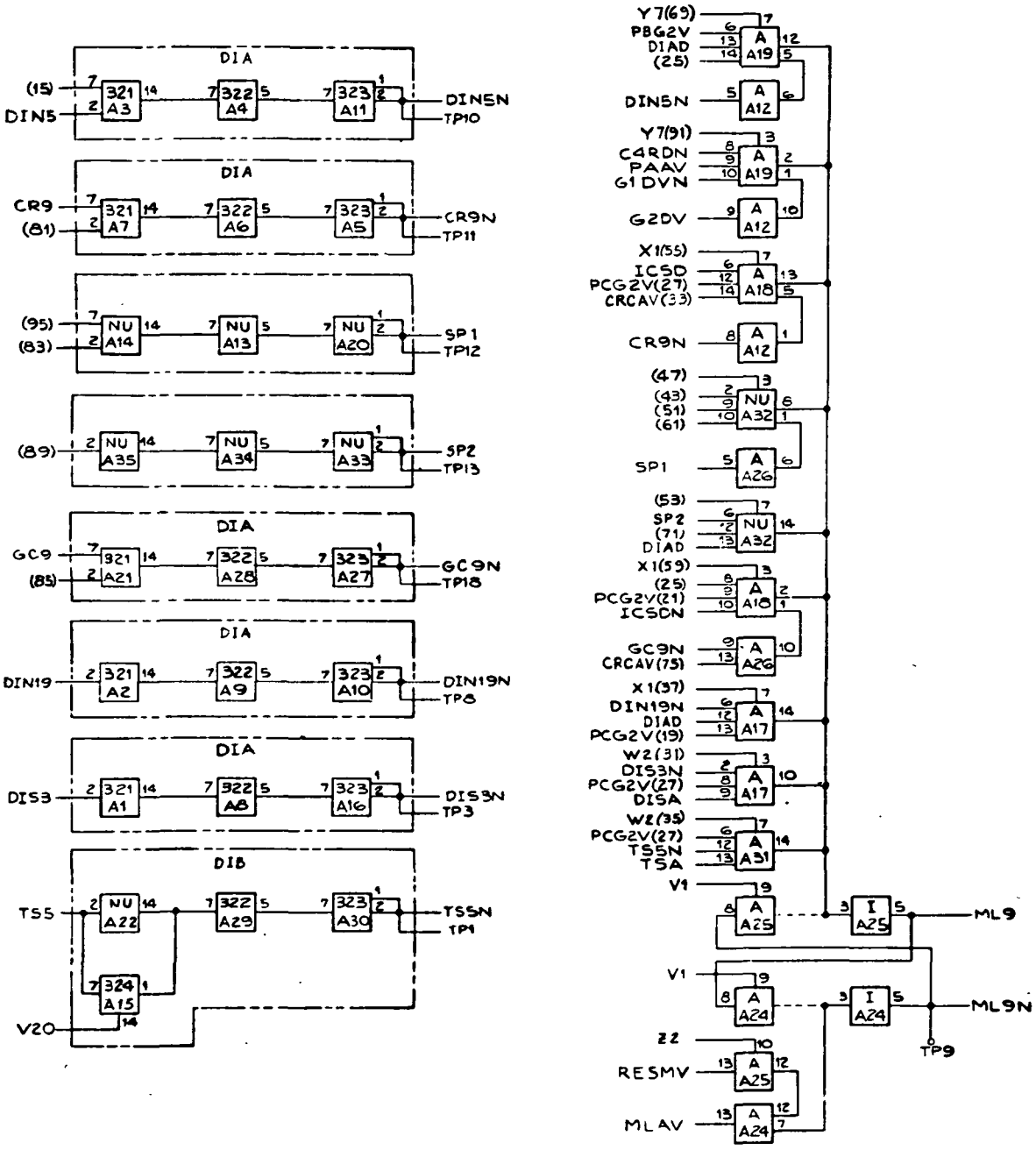
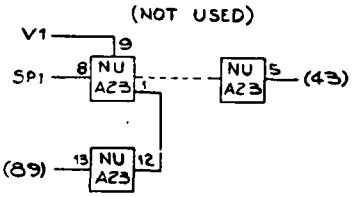


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 15)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	Z2	51	
3	DIS3	53	
5	V2O	55	X1
7	TS5	57	ML9
9	SIG·RET	59	X1
11	DIN19	61	
13	DIN5	63	TSA
15		65	DIAD
17	DISA	67	RESMV
19	PCG2V	69	Y7
21	PCG2V	71	
23	MLAV	73	G1DVN
25		75	CRCAV
27	PCG2V	77	PAAV
29	ICSDN	79	PBG2V
31	W2	81	
33	CRCAV	83	
36	W2	85	
37	X1	87	V1
39	ICSD	89	
41	C4RDN	91	Y7
43		93	GC9
45	G2DV	95	
47		97	CR9
49	V5		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 322
A8 322	A9 322	A10 323	A11 323	A12 AB	A13	A14
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A4 Side A.
6. This Drawing Derived From IBM DWG NO. 6112367-REL(66123ET)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 16)

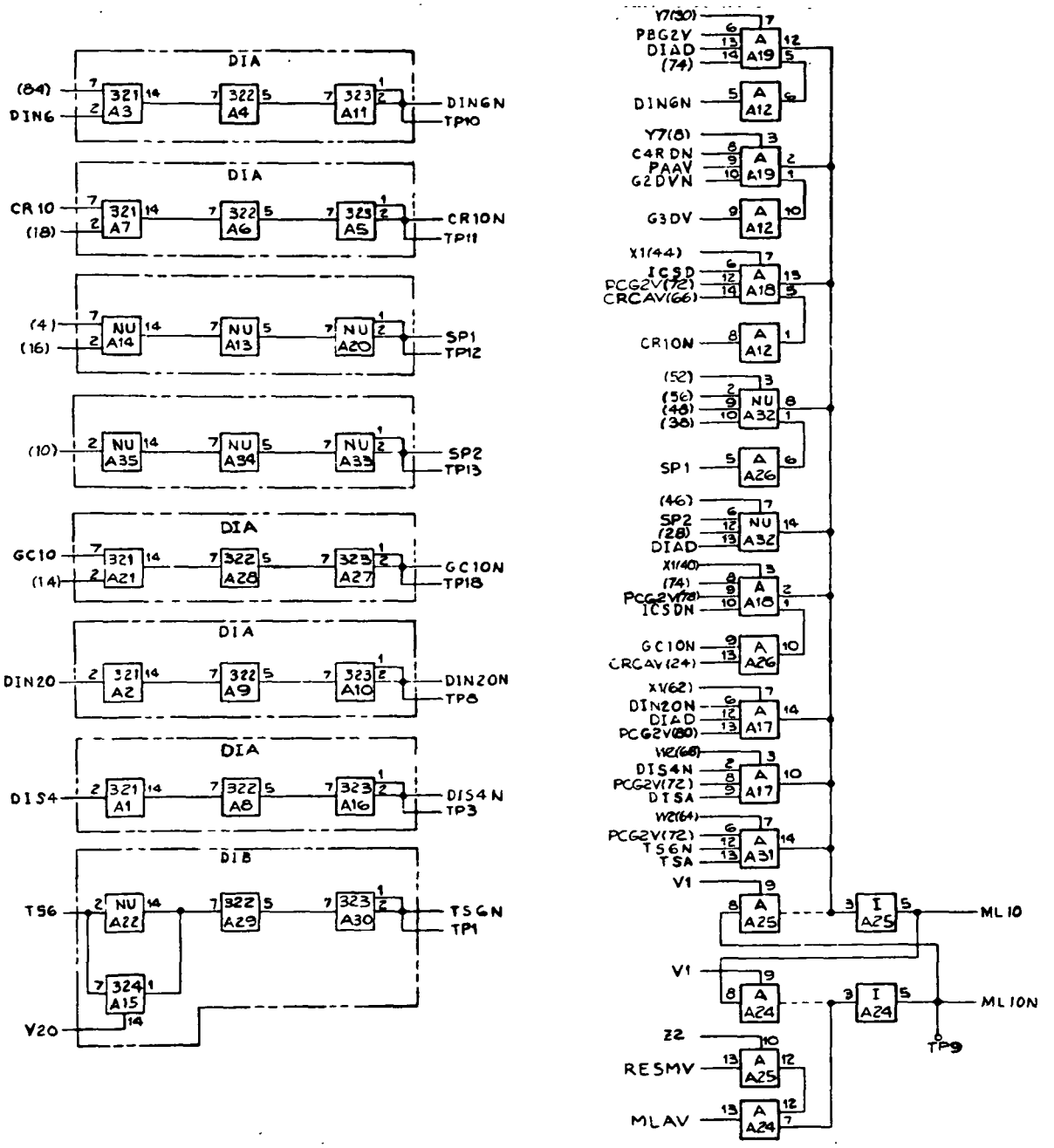
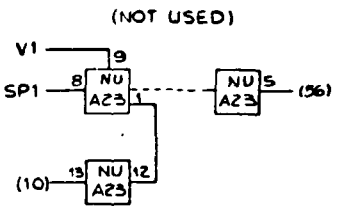


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 17)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CF10	52	
4		54	G3DV
6	GC10	56	
8	Y7	58	C4RDN
10		60	ICSD
12	V1	62	X1
14		64	W2
16		66	CRCAV
18		68	W2
20	PBG2V	70	ICSDN
22	PAAV	72	PCG2V
24	CRCAV	74	
26	G2DVN	76	MLAV
28		78	PCG2V
30	Y7	80	PCG2V
32	RESMV	82	DISA
34	DIAD	84	
36	TSA	86	DIN6
38		88	DIN20
40	X1	90	SIG-RET
42	ML10	92	TS6
44	X1	94	V20
46		96	DIS4
48		98	22
50	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13	A14
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A4 Side B.
6. This Drawing Derived From IBM DWG NO. 6112469-REL(66123FM)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 18)

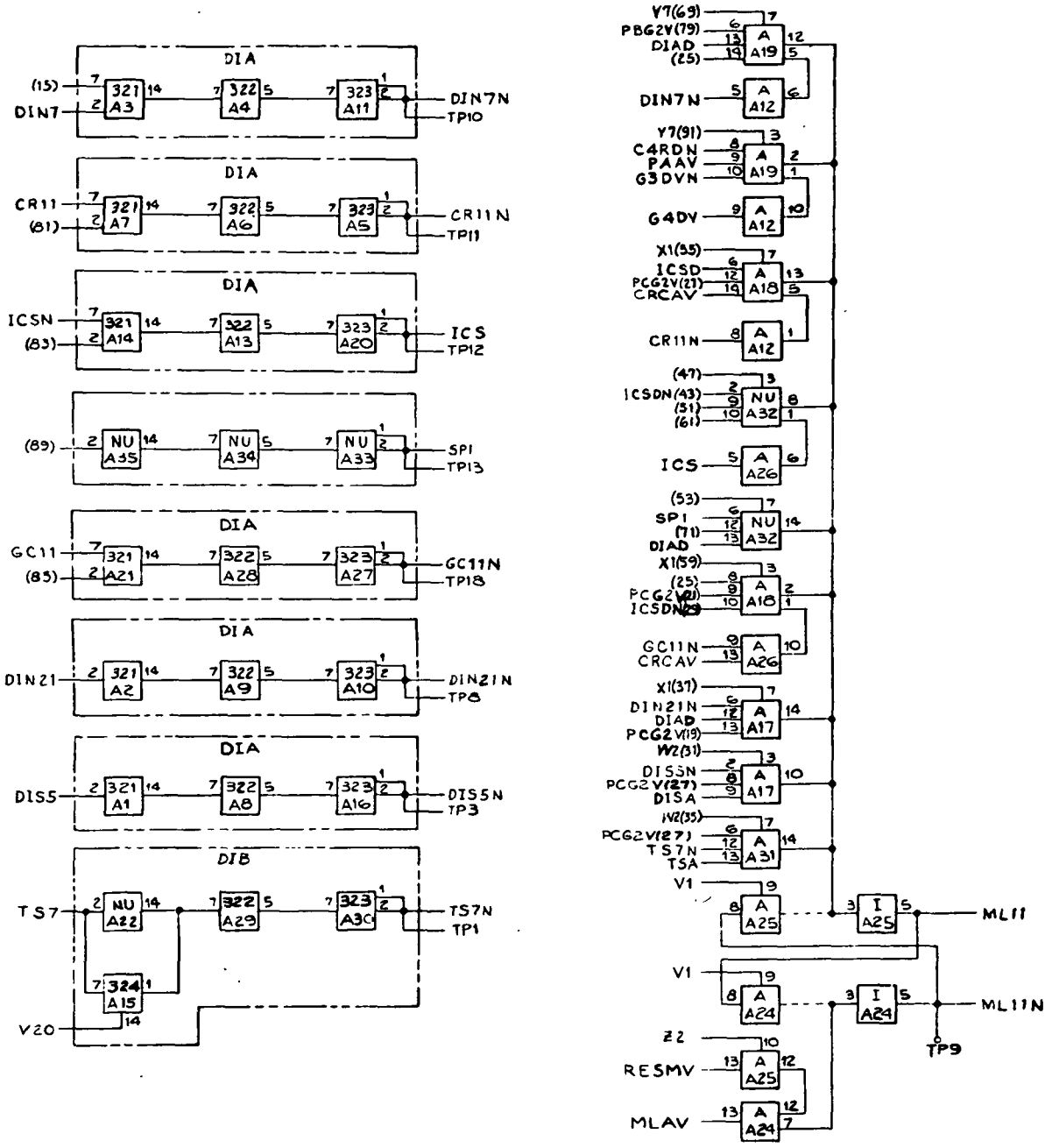
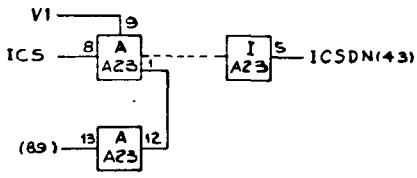


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 19)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	Z2	51	
3	DISS	53	
5	V20	55	X1
7	TS7	57	ML11
9	SIG-RET	59	X1
11	DIN21	61	
13	DIN7	63	TSA
15		65	DIAD
17	DISA	67	RESMV
19	PCG2V	69	Y7
21	PCG2V	71	
23	MLAV	73	G3DVN
25		75	CRCAV
27	PCG2V	77	PAAV
29	ICSDN	79	PBG2V
31	W2	81	
33	CRCAV	83	
35	W2	85	
37	X1	87	V1
39	ICSD	89	
41	C4RDN	91	Y7
43	ICSDN	93	GC11
45	G4DV	95	ICSN
47		97	CR11
49	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13 322	A14 321
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20 323	A21 321
A22	A23 I	A24 I	A25 :	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A6 Side A.
6. This Drawing Derived From IBM DWG NO. 6112487-REL(66123FM)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 20)

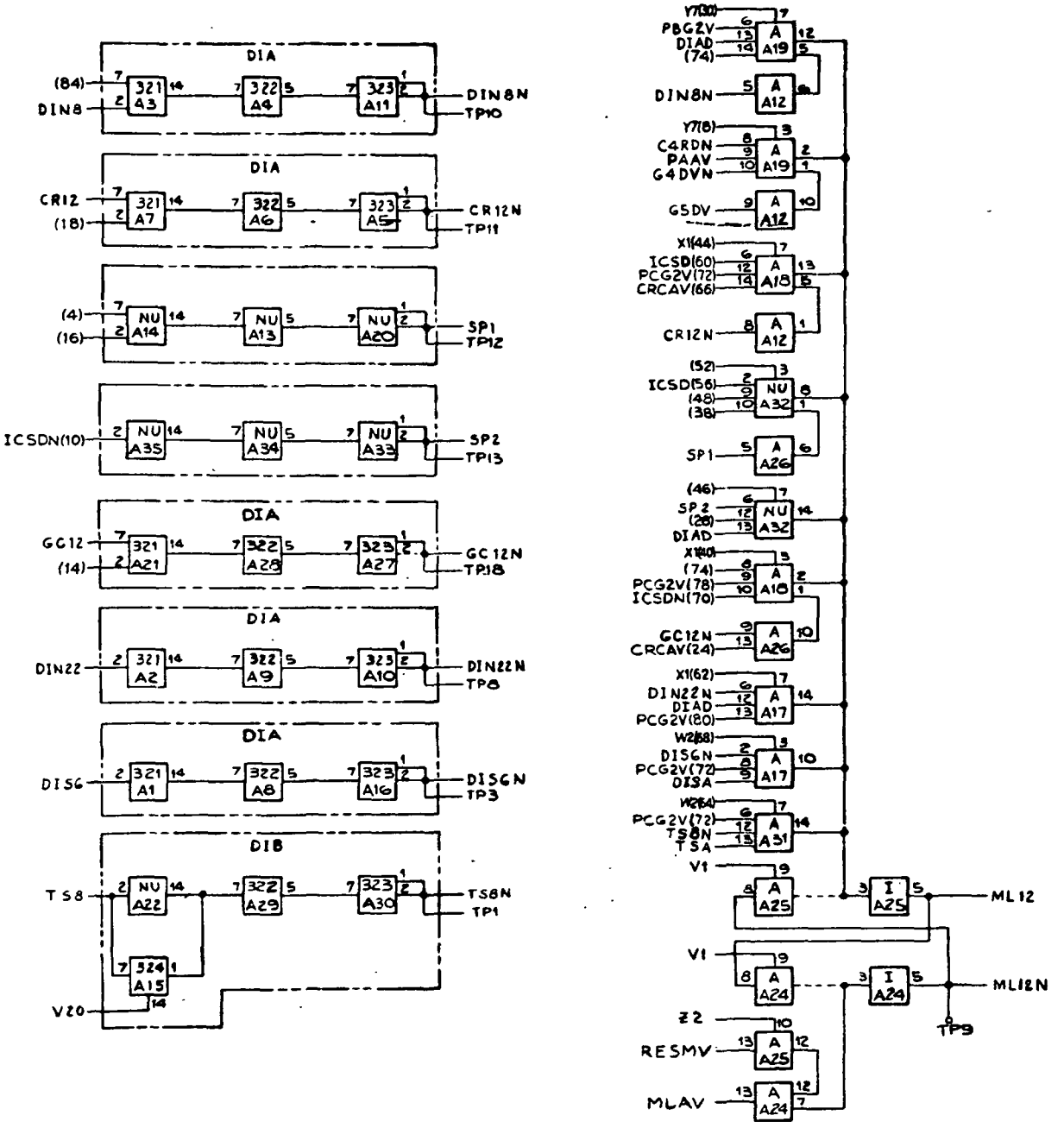
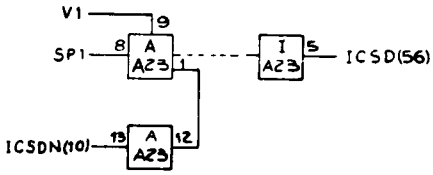


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 21)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CR12	52	
4		54	G5DV
6	GC12	56	ICSD
8	Y7	58	C4RDN
10	ICSDN	60	ICSD
12	V1	62	X1
14		64	W2
16		66	CRCAV
18		68	W2
20	PBG2V	70	ICSDN
22	PAAV	72	PCG2V
24	CRCAV	74	
26	G4DVN	76	MLAV
28		78	PCG2V
30	Y7	80	PCG2V
32	RESMV	82	DISA
34	DIAD	84	
36	TSA	86	DING
38		88	DIN22
40	X1	90	SIG-RET
42	ML12	92	TS8
44	X1	94	V20
46		96	DIS6
48		98	Z2
50	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13	A14
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20	A21 321
A22	A23 I	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A6 Side B.
6. This Drawing Derived From IBM DWG NO. 6112489-REL(66123FM)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 22)

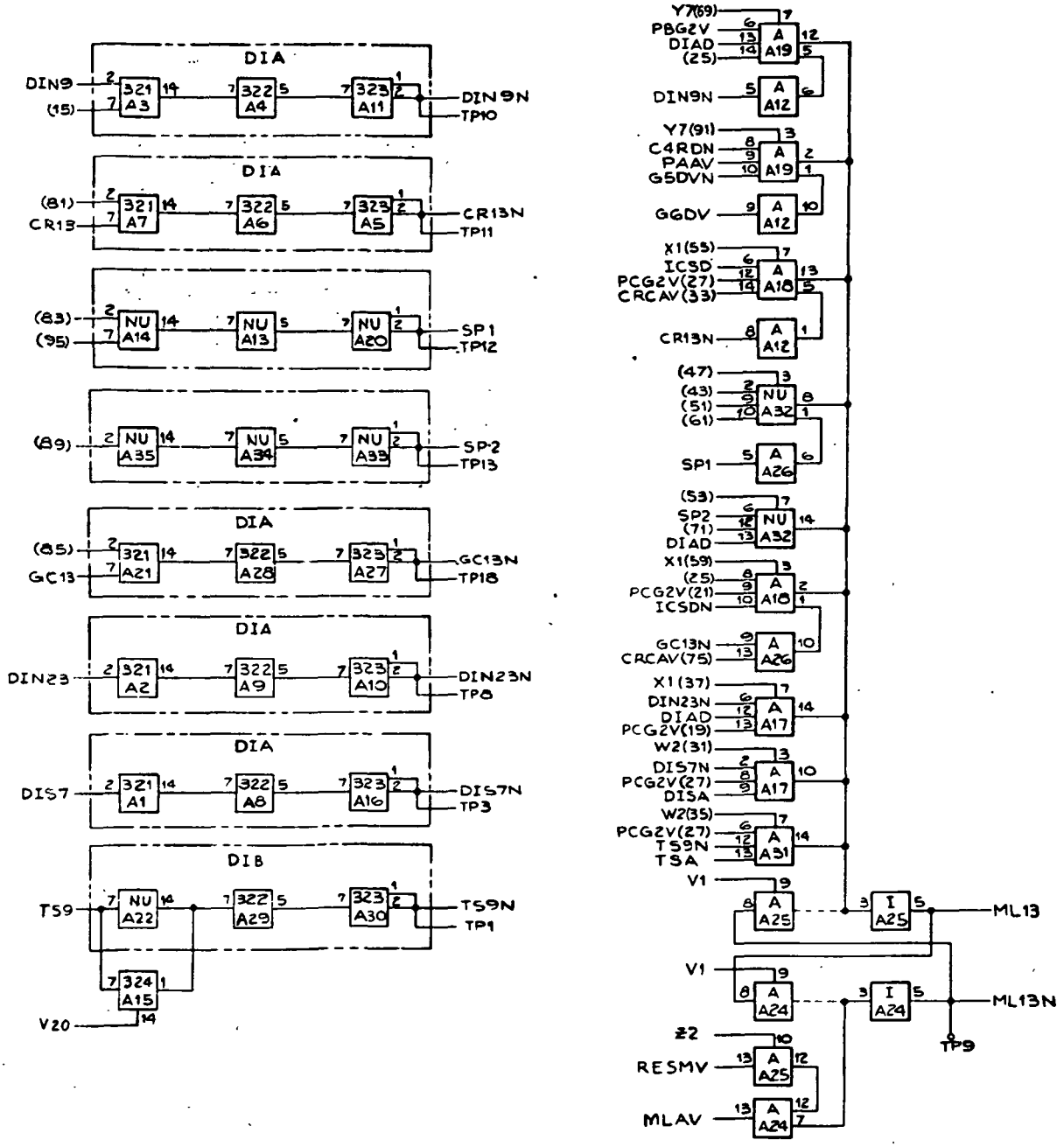
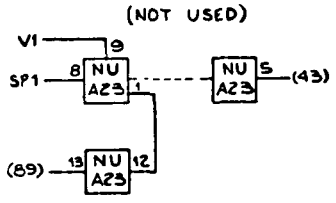


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 23)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	Z2	51	
3	DIS7	53	
5	Y20	55	X1
7	TS9	57	ML13
9	SIG-RET	59	X1
11	DIN23	61	
13	DIN9	63	TSA
15		65	DIAD
17	DISA	67	RESMV
19	PCG2V	69	Y7
21	PCG2V	71	
23	MLAV	73	G5DVN
25		75	CRCAV
27	PCG2V	77	PAAV
29	ICSDN	79	PBG2V
31	W2	81	
33	CRCAV	83	
35	W2	85	
37	X1	87	V1
39	ICSD	89	
41	C4RDN	91	Y7
43		93	GC13
45	G6DV	95	
47		97	CR13
49	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	AE 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13	A14
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A7 Side A.
6. This Drawing Derived From IBM DWG NO. 6112377-REL(66123ET)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 24)

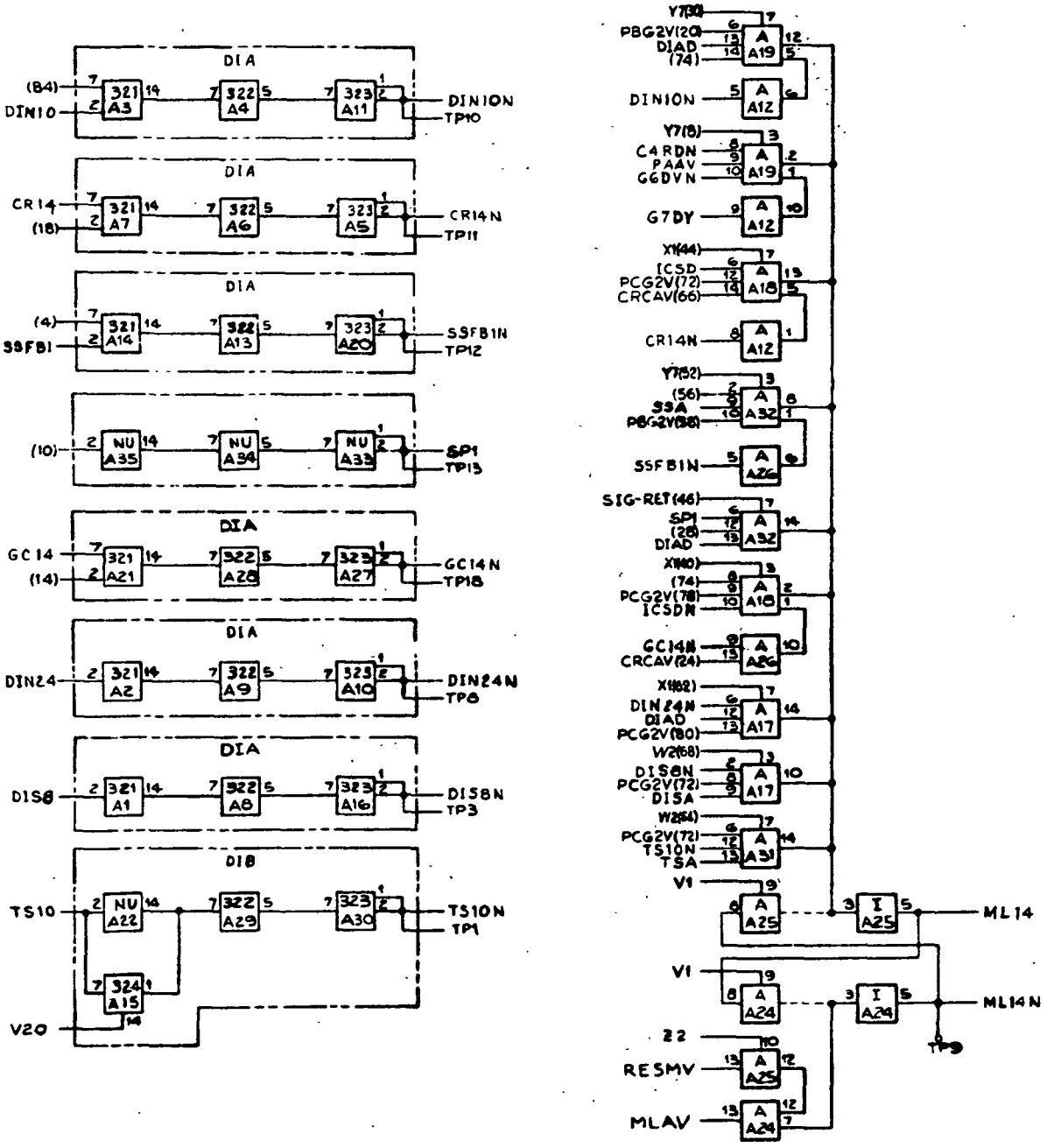
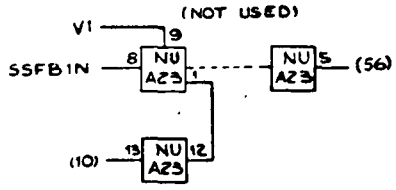


Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 25)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CR14	52	Y7
4		54	G7DV
6	GC14	56	
8	Y7	58	C4RDN
10		60	ICSD
12	V1	62	Y1
14		64	W2
16	SSFB1	66	CRCAV
18		68	W2
20	FBG2V	70	ICSDN
22	FAAV	72	PCG2V
24	CPCAV	74	
26	GGDYN	76	MLAV
28		78	PCG2V
30	Y7	80	PCG2V
32	RESMV	82	DISA
34	DIAD	84	
36	TSA	86	DIN 0
38	PBG2V	88	DIN24
40	X1	90	SIG-RET
42	ML14	92	TS10
44	X1	94	V20
46	SIG-RET	96	DI58
48	SSA	98	Z2
50	V3		

ULD LOCATIONS

A1 321	A2 321	A3 321	A4 322	A5 323	A6 322	A7 321
A8 322	A9 322	A10 323	A11 323	A12 AB	A13 322	A14 321
A15 324	A16 323	A17 AA	A18 AA	A19 AA	A20 323	A21 321
A22	A23	A24 I	A25 I	A26 AB	A27 323	A28 322
A29 322	A30 323	A31 AA	A32 AA	A33	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A7 Side B.
6. This Drawing Derived From IBM DWG NO. 6112379-REL(66123FM)

Figure 10-11. System Data Sampler (Multiplexer) Logic Diagram (Sheet 26)

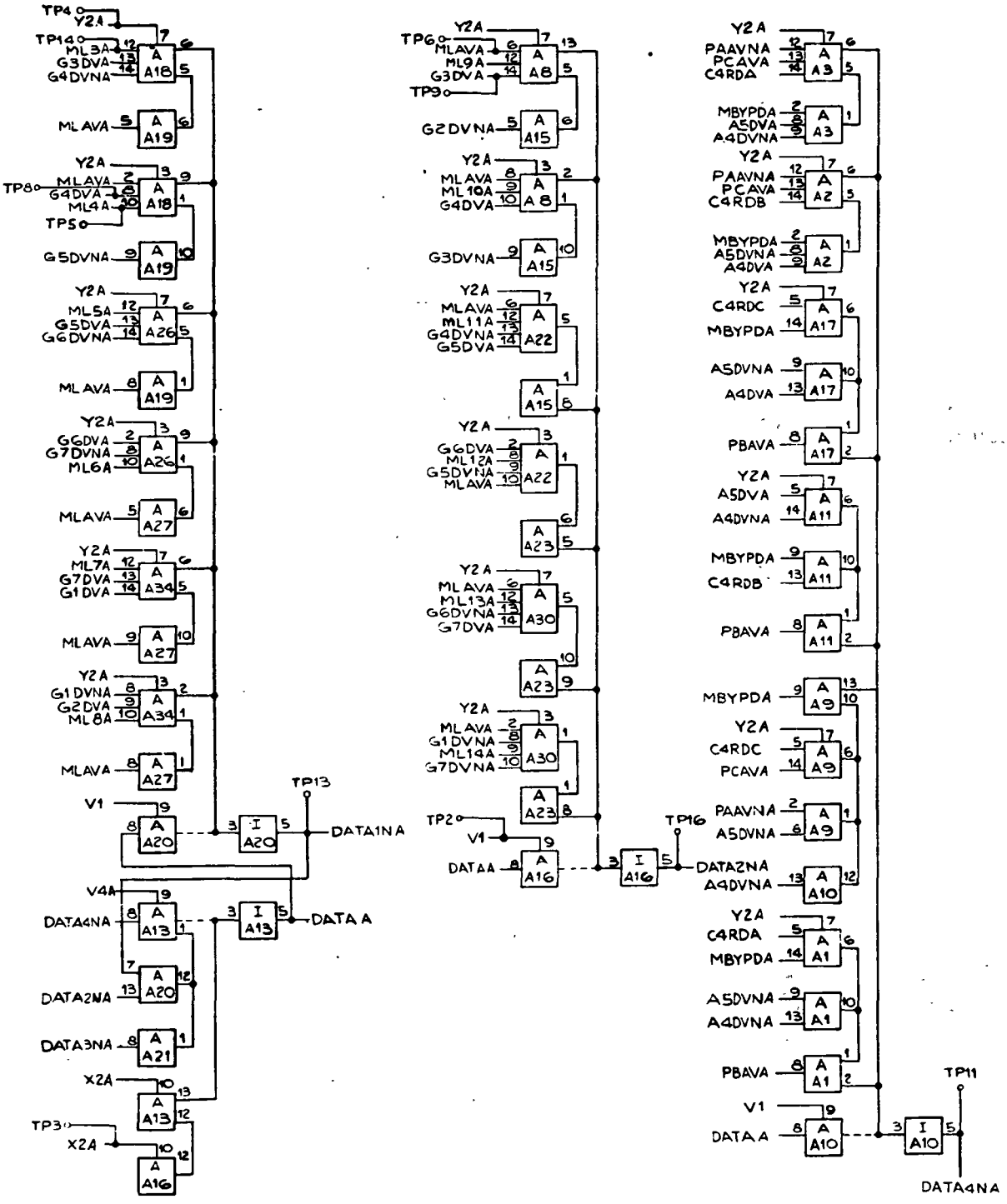
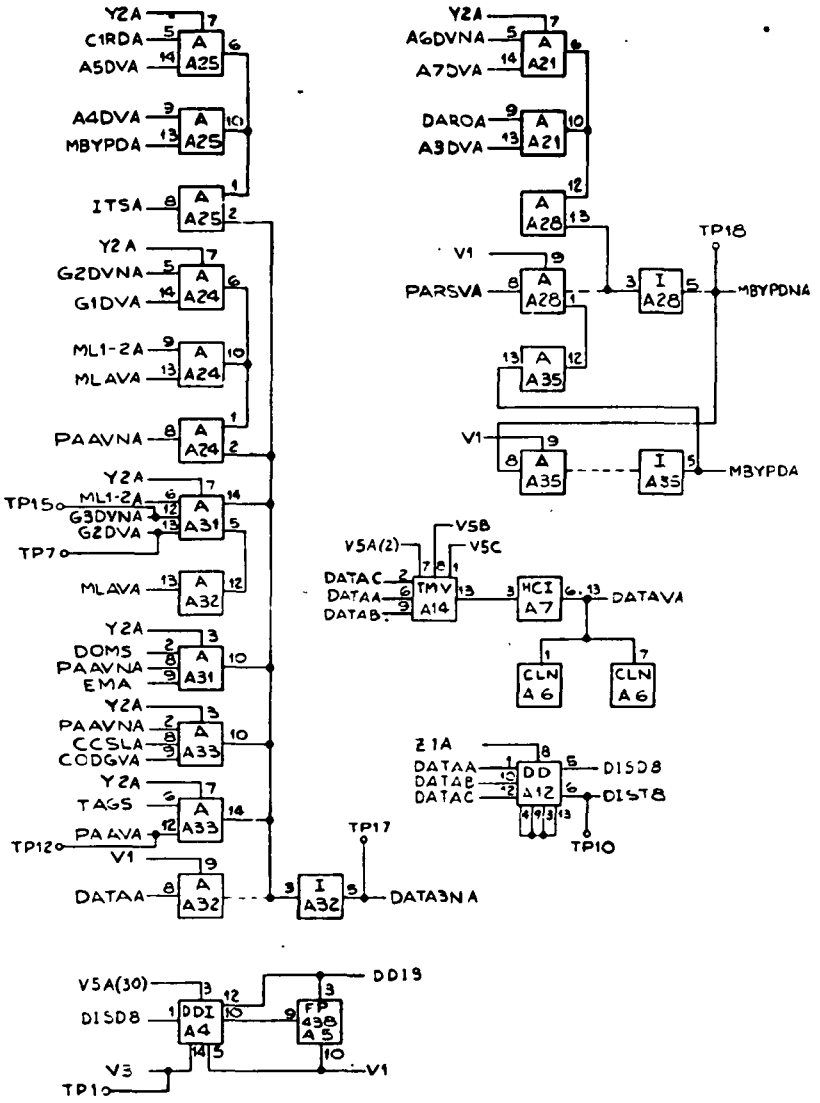


Figure 10-12. System Data Sampler (Serializer-Selector) Logic Diagram (Sheet 1 of 4)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	16	DATA8
2		17	DATAVA
3		18	DATAC
4		19	Z1A
5	V1	20	
6		21	G3DVNA
7		22	ML3A
8		23	DISD8
9		24	G2DVA
10		25	PAAVA
11		26	G3DVA
12	C4RDB	27	C4RDA
13	C4RDC	28	G4DVNA
14	ML4A	29	X2A
15	MLAVA	30	Y2A

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	V5A	52	DATAA
4	A6DVNA	54	A4DVA
6	A3DVA	56	G2DVNA
8	SIG RET	58	ML1-2A
10	A7DVA	60	DOMS
12	MBYPDA	62	PAAVNA
14	PARSVA	64	G6DVNA
16	DAR0A	66	G7DVA
18	V4A	68	PCAVA
20	V5C	70	ML13A
22	G1DVA	72	G4DVA
24	ML7A	74	G7DVNA
26	ML8A	76	EMA
28	V5B	78	G1DVNA
30	V5A	80	G6DVA
32	ASDVNA	82	ML14A
34	ML5A	84	ASDVA
36	ML6A	86	ML10A
38	PBAVA	88	G5DVA
40	A4DVNA	90	ML9A
42	TAGS	92	CODGVA
44	CCSLA	94	ML11A
46	DDI8	96	ML12A
48	C1RDA	98	G5DVNA
50	ITSA		

ULD LOCATIONS

A1 AB	A2 AA	A3 AA	A4 DDI	A5 FP 438	A6 CLN	A7 HCI
A8 AA	A9 AB	A10 I	A11 AB	A12 DD	A13 I	A14 TMV
A15 AB	A16 I	A17 AB	A18 AA	A19 AB	A20 I	A21 AB
A22 AA	A23 AB	A24 AB	A25 AB	A26 AA	A27 AB	A28 I
A29	A30 AA	A31 AA	A32 I	A33 AA	A34 AA	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A5 Side B.
6. This Drawing Derived From IBM DWG NO. 6112787-A(66123NT)

Figure 10-12. System Data Sampler (Serializer-Selector) Logic Diagram (Sheet 2)

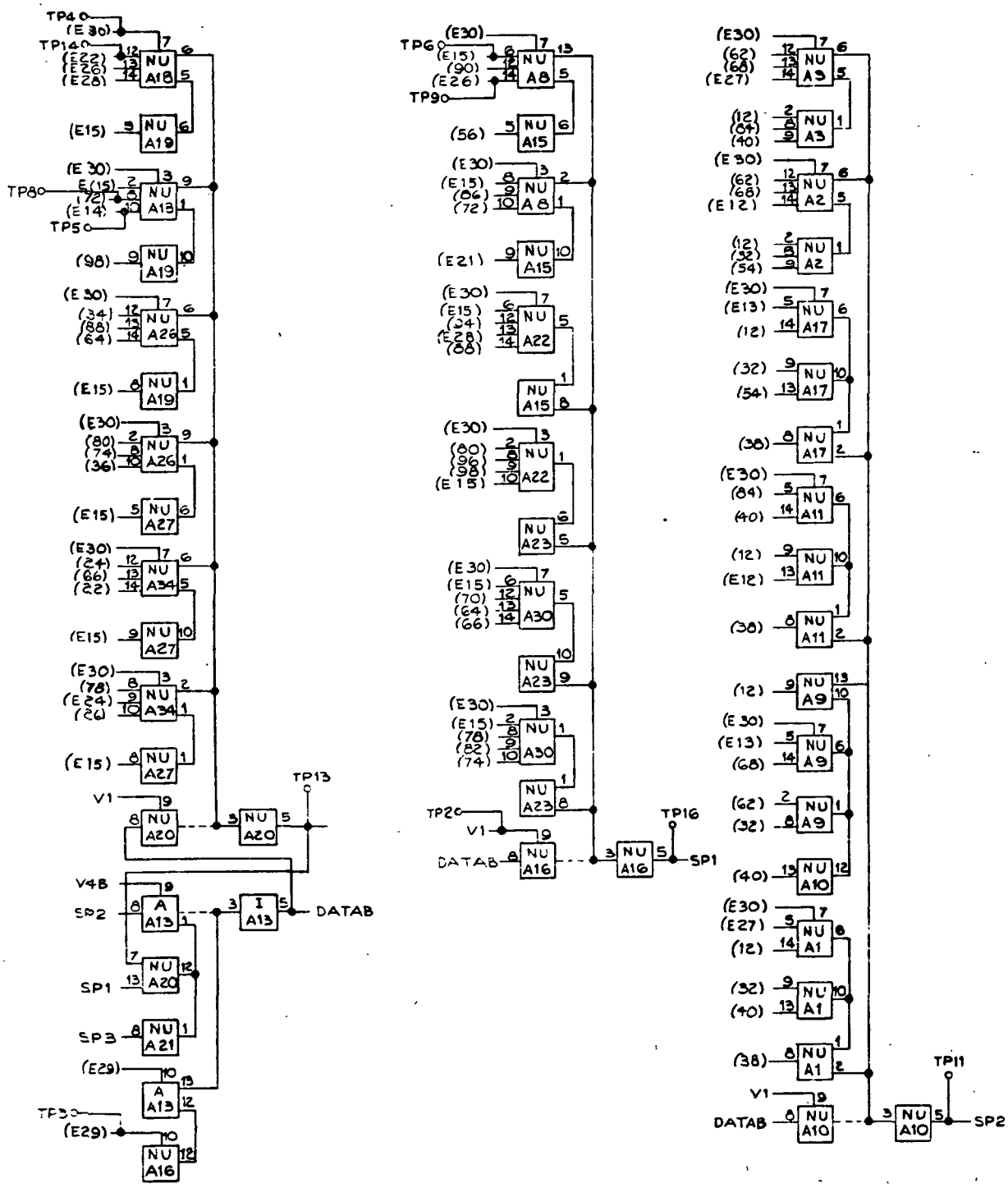
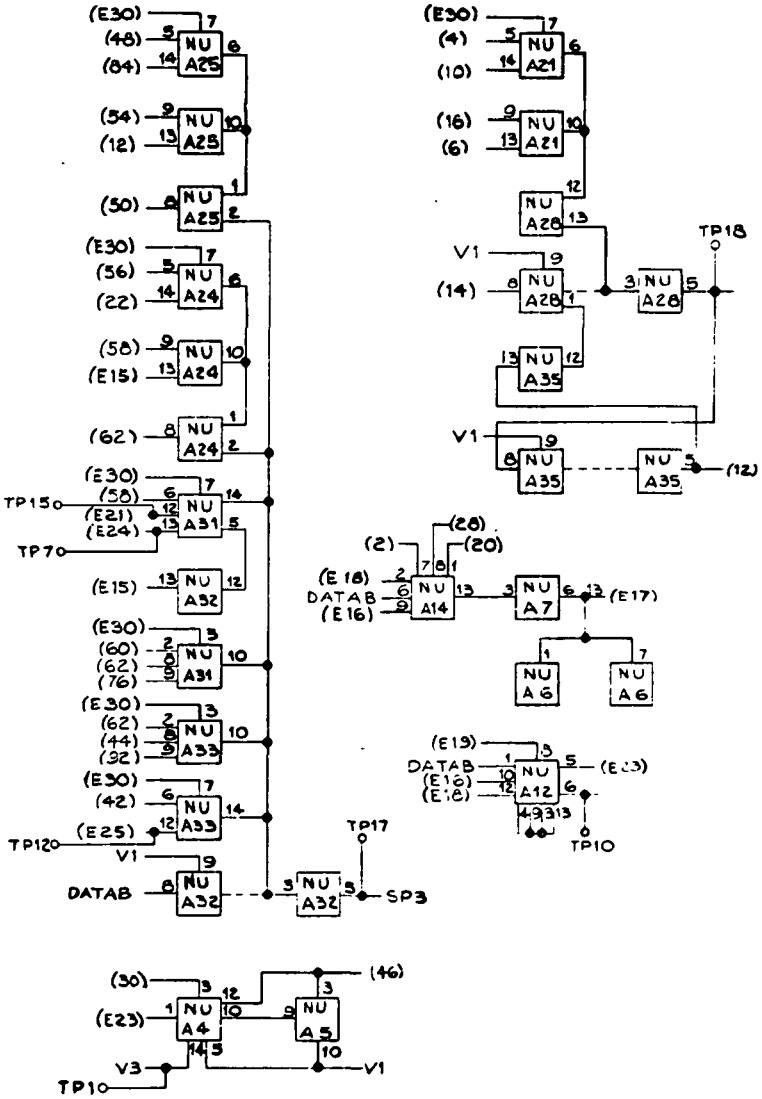


Figure 10-12. System Data Sampler (Serializer-Selector) Logic Diagram (Sheet 3)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	16	
2		17	
3		18	
4		19	
5	V1	20	
6		21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	DATAB
4		54	
6		56	
8	SIG-RET	58	
10		60	
12		62	
14		64	
16		66	
18	V48	68	
20		70	
22		72	
24		74	
26		76	
28		78	
30		80	
32		82	
34		84	
36		86	
38		87	V1
40		88	
42		90	
44		92	
46		94	
48		96	
49	V3	98	
50			

ULD LOCATIONS						
A1	A2	A3	A4	A5	A6	A7
A8	A9	A10	A11	A12	A13	A14
A15	A16	A17	A18	A19	A20	A21
A22	A23	A24	A25	A26	A27	A28
A29	A30	A31	A32	A33	A34	A35

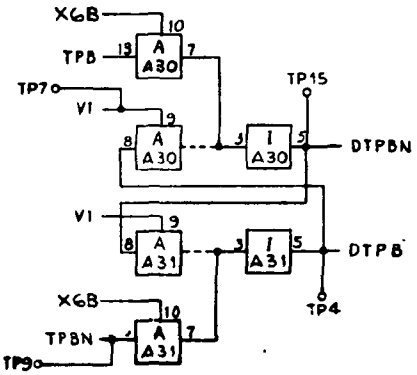
NOTES:

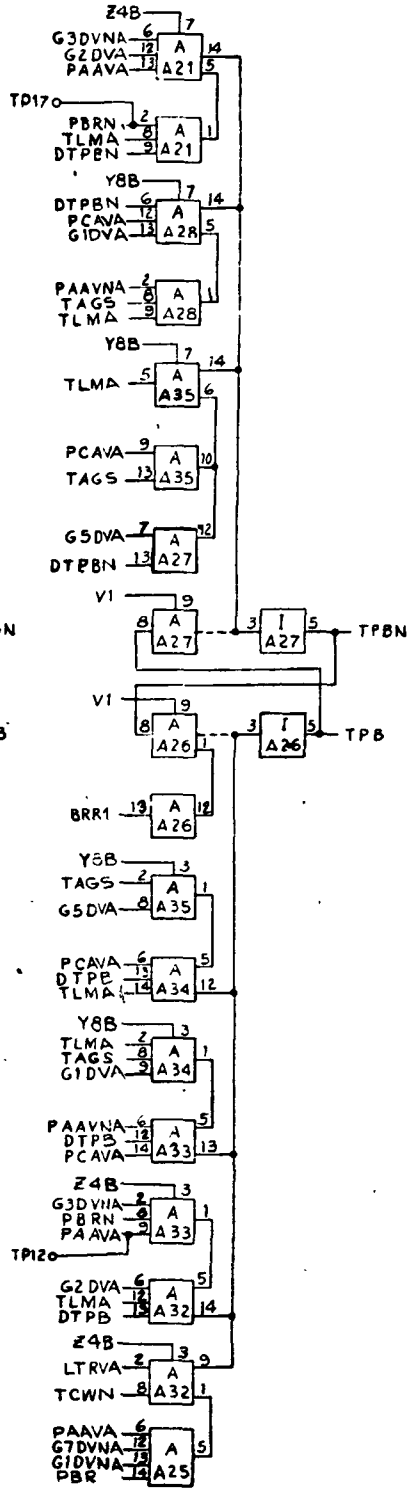
1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A16 Side B.
6. This Drawing Derived From IBM DWG NO. 6112737-REL(66123KL)

Figure 10-12. System Data Sampler (Serializer-Selector) Logic Diagram (Sheet 4)

THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	XGC
2		17	ZGC
3		18	G4DVA
4		19	ADVA
5		20	G1DVNA
6	PCAVA	21	ADVNA
7		22	
8		23	WGC
9		24	G6DVNA
10		25	PBR
11		26	G2DVNA
12		27	V1
13	G7DVNA	28	SIG-RET(TP2)
14	G5DVNA	29	PAAVA
15	V3(TP1)	30	PBRN

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	A9DVA	52	LTRVA
4	A2DVNA	54	TCWN
6	ML9A	56	Z4B
8		58	ML8A
10	A8DVA	60	ML6A
12	TAGS	62	ML5A
14	G5DVA	64	
16	A3DVA	66	A7CRA
18	Y8B	68	CODGVA
20	MODR1	70	XGB
22	MODR2	72	G3DVA
24	TLMA	74	TPB
26	G1DVA	76	A6DVA
28	G4DVNA	78	A5CRA
30	A1DVA	80	A7DVA
32		82	A6CRA
34	BRR1	84	A1DVNA
36	PAAVNA	86	A4CRA
38	G3DVNA	88	
40	ML7A	90	A3CRA
42	G1DVA	92	CODGNA
44	MODR3	94	A2DVA
46	G6DVA	96	RESMVA
48	A4DVA	98	A5DVA
50	G2DVA		





ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
	AE		AB	AA	AA	AB
A8	A9	A10	A11	A12	A13	A14
AA	AA	AA	AA	AA	I	AA
A15	A16	A17	A18	A19	A20	A21
AB	I	I	AB	AA	AA	AA
A22	A23	A24	A25	A26	A27	A28
AA	AA	AA	AA	I	I	AA
A29	A30	A31	A32	A33	A34	A35
AB	I	I	AA	AA	AA	AB

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A3 Side B.
6. This Drawing Derived From IBM DWG NO. 6112488-A(66123WC)

Figure 10-13. System Data Sampler (Tag Processor) Logic Diagram (Sheet 1 of 2)

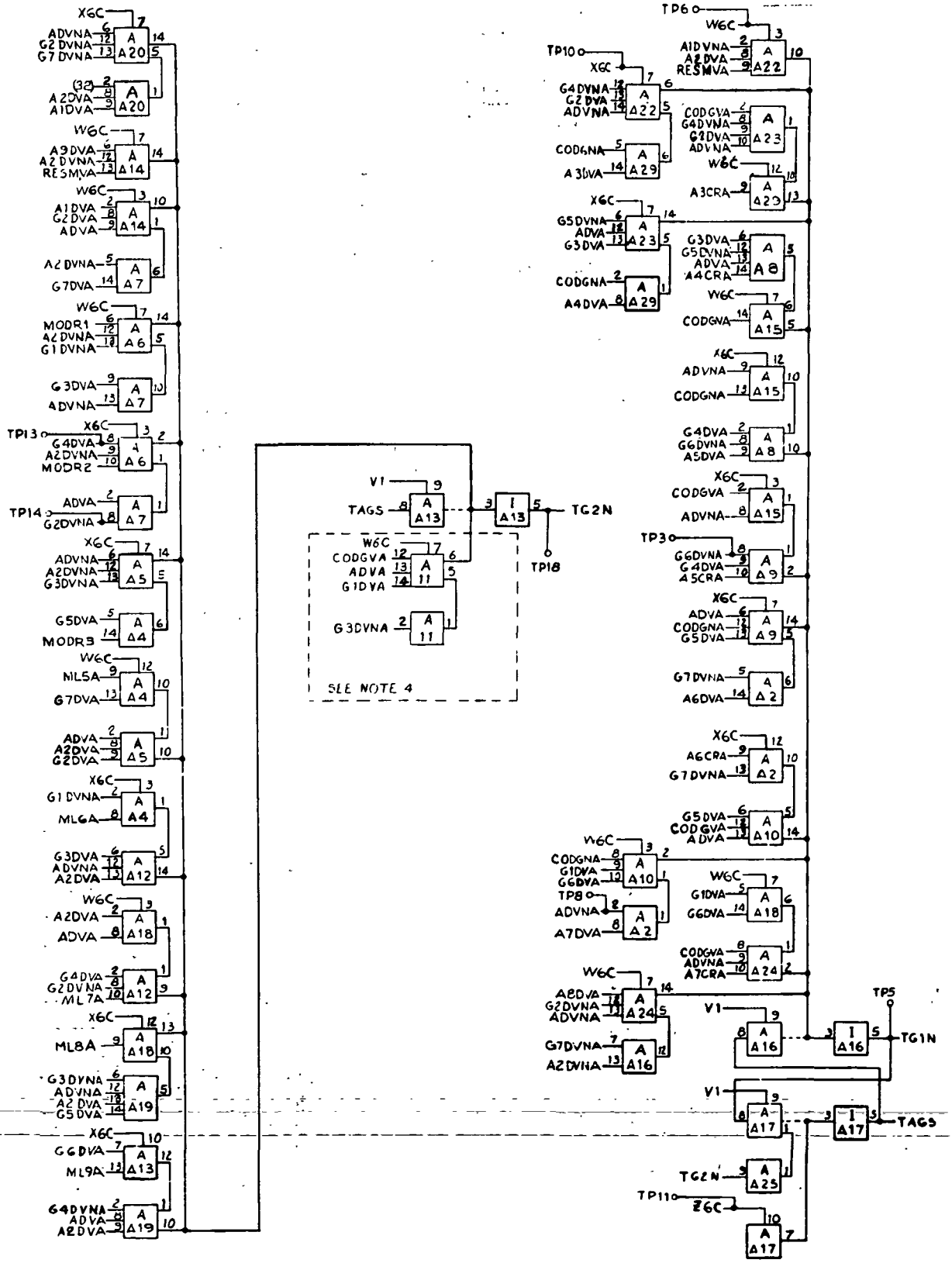
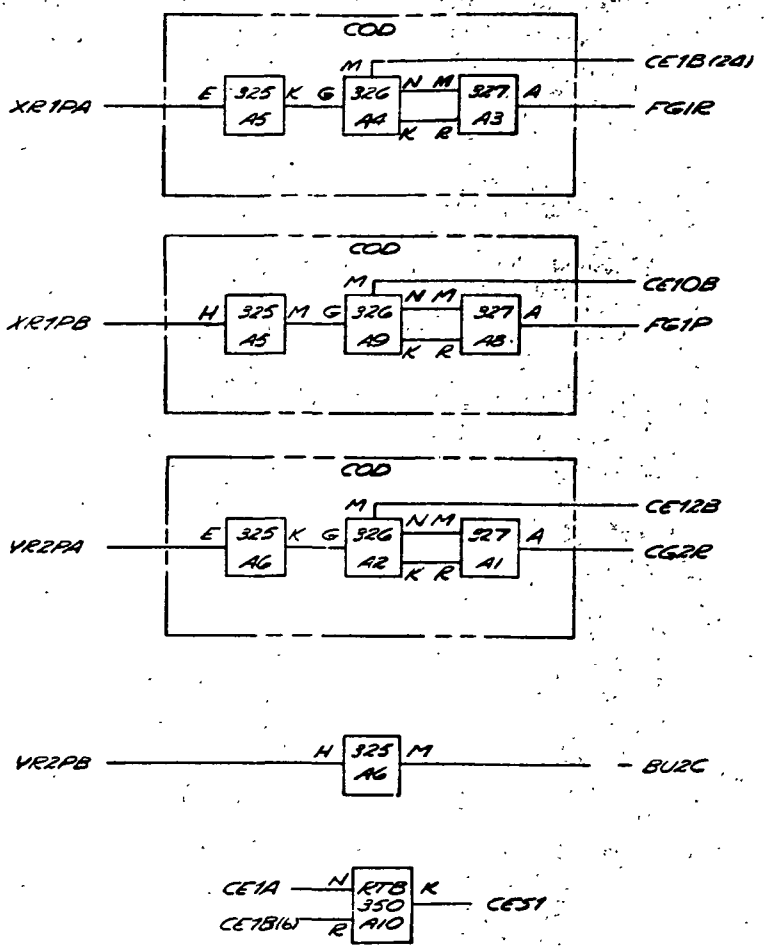


Figure 10-13. System Data Sampler (Tag Processor) Logic Diagram (Sheet 2)

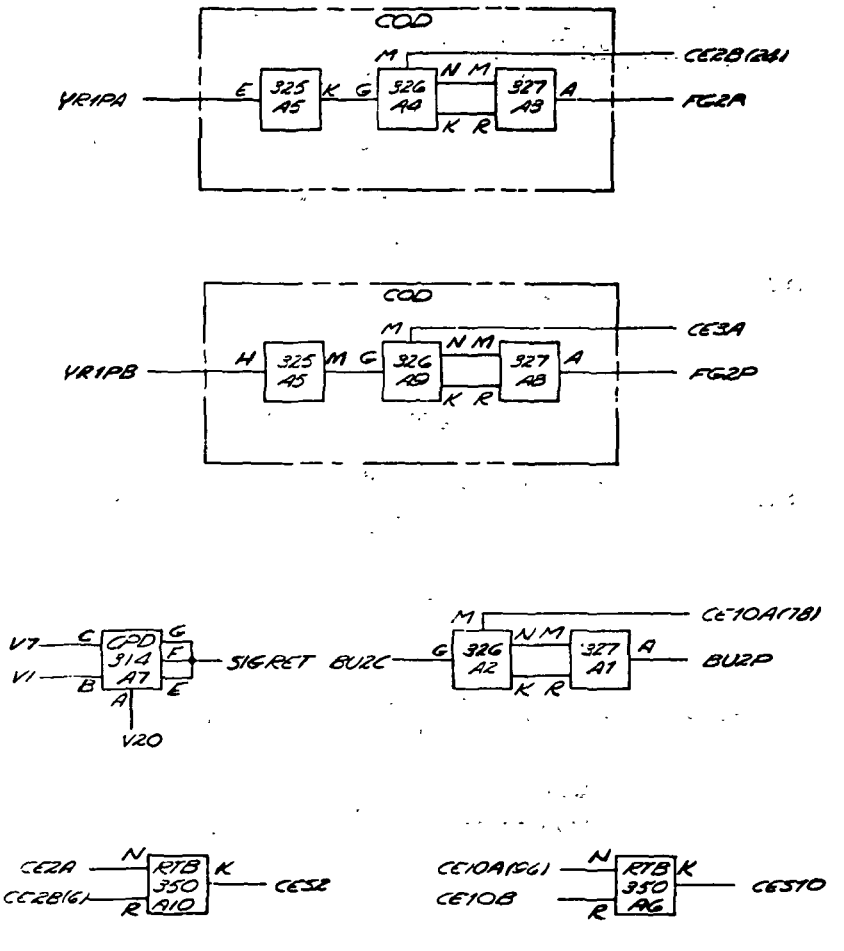


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	XR1PB	52	V7
4	XR1PA	54	
6	CE1B	56	V20
8		58	FG1P
10	V5	60	RFSRTNT
12		62	FG1R
14		64	RFSRTNT
16		66	
18	CE1A	68	
20		70	
22	CE10B	72	
24	CE1B	74	
26		76	
28		78	CE12B
30	SIG-RET	80	
32	V7	82	
34	V20	84	BU2C
36	V5	86	
38	V3	88	
40	CE51	90	
42	CG2R	92	
44	V1	94	
46	V3	96	VR2PB
48	V7	98	VR2PA
50	SIGRET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A3.
6. This Drawing Derived From IBM DWG NO. 6112647-REL(66123FP)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 1 of 13)

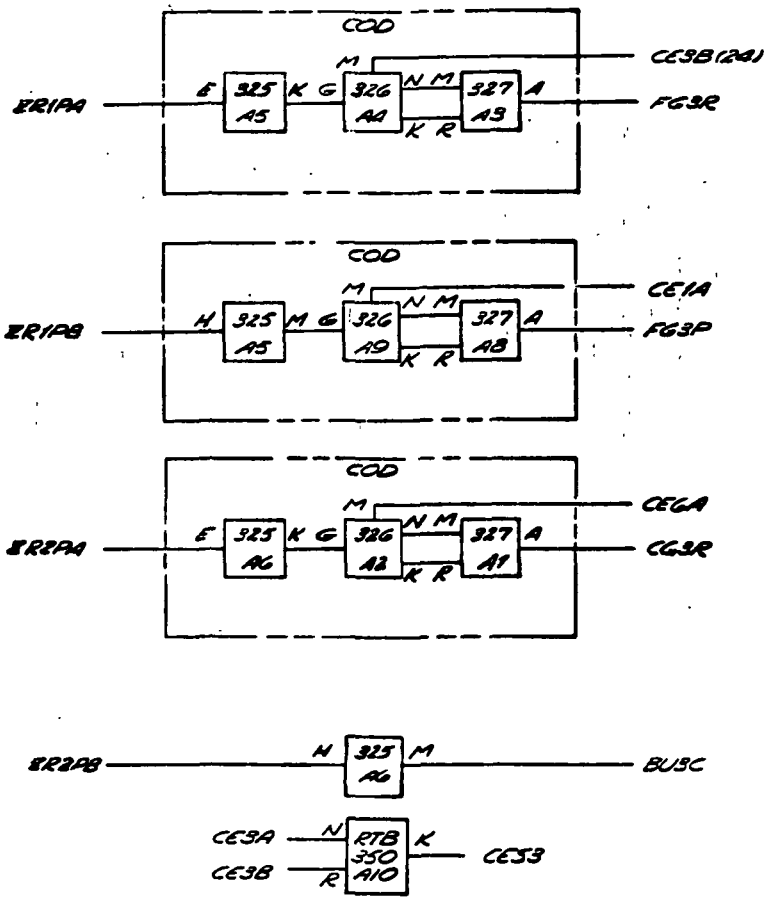


NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix-Reference-Designator as Follows: 2A5A6.
6. This Drawing Derived From IBM DWG NO. 6112657-REL(66123FP)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	VR1PB	52	V7
4	VR1PA	54	
6	CE2B	56	V20
8		58	FG2P
10		60	RFSRTN2
12		62	FG2A
14		64	RFSRTN2
16		66	
18	CE2A	68	
20		70	
22	CE3A	72	
24	CE2B	74	
26		76	
28		78	CE10A
30	SIGRET	80	CE510
32	V7	82	
34	V20	84	BU2C
36	V5	86	
38	V3	88	
40	BU2P	90	
42	CE52	92	V5
44	V1	94	
46	V3	96	CE10A
48	V1	98	CE10B
50	SIGRET		

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 2)

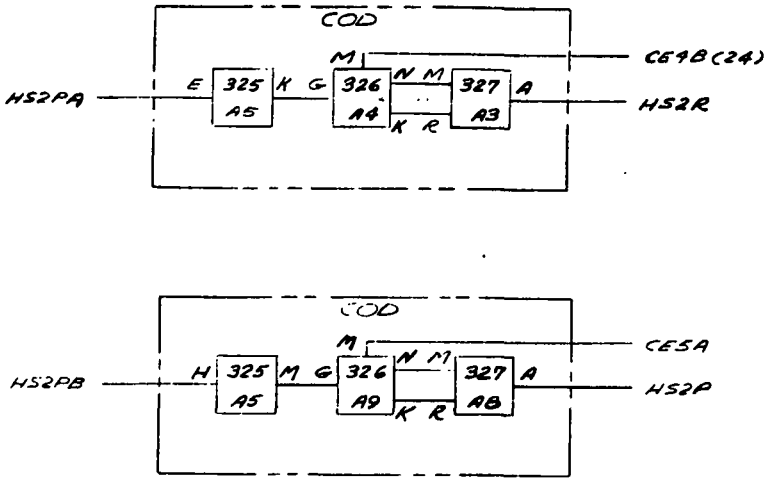


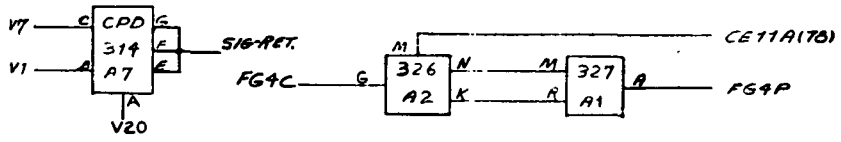
CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	ZR1PB	52	V7
4	ZR1PA	54	
6	CE3B	56	V20
8		58	FG3P
10	V5	60	RFSRTN3
12		62	FG3R
14		64	RFSRTN3
16		66	
18	CE3A	68	
20		70	
22	CE1A	72	
24	CE3B	74	
26		76	
28		78	CE6A
30	SIG-RET	80	
32	V7	82	
34	V20	84	BUSC
36	V5	86	
38	V3	88	
40	CE33	90	
42	CG3R	92	
44	V1	94	
46	V3	96	ZR2PB
48	V7	98	ZR2PA
50	SIG-RET		

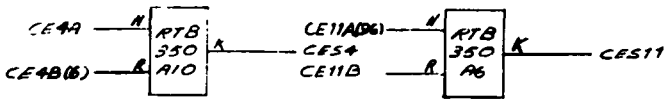
NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A9.
6. This Drawing Derived From IBM DWG NO. 6112648-REL(66123AH)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 3)







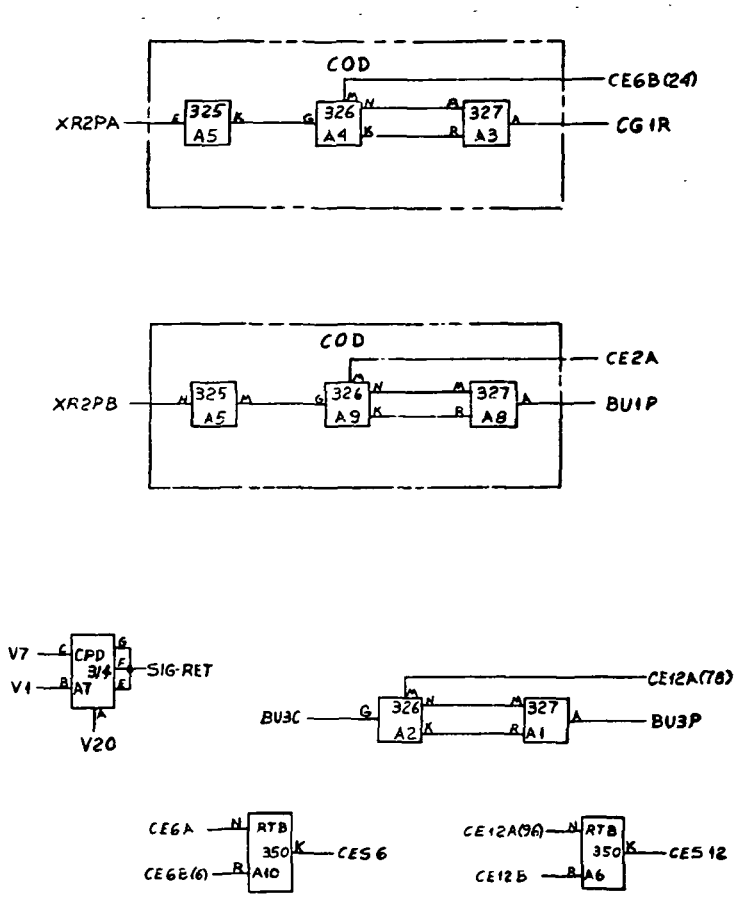
NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A12.
6. This Drawing Derived From IBM DWG NO. 6112658-REL(66123AJ)

CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
2	HS2PB	52	V7
4	HS2PH	54	
6	CE4B	56	V20
8		58	HS2P
10		60	RFSRTN4
12		62	HS2K
14		64	RFSRTN4
16		66	
18	CE4A	68	
20		70	
22	CE5A	72	
24	CE4B	74	
26		76	
28		78	CE11A
30	SIG-RET	80	CE5T1
32	V7	82	
34	V20	84	FG4C
36	V5	86	
38	V3	88	
40	FG4P	90	
42	CE54	92	V5
44	V1	94	
46	V3	96	CE11A
48	V1	98	CE11B
50	SIG-RET		

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 4)

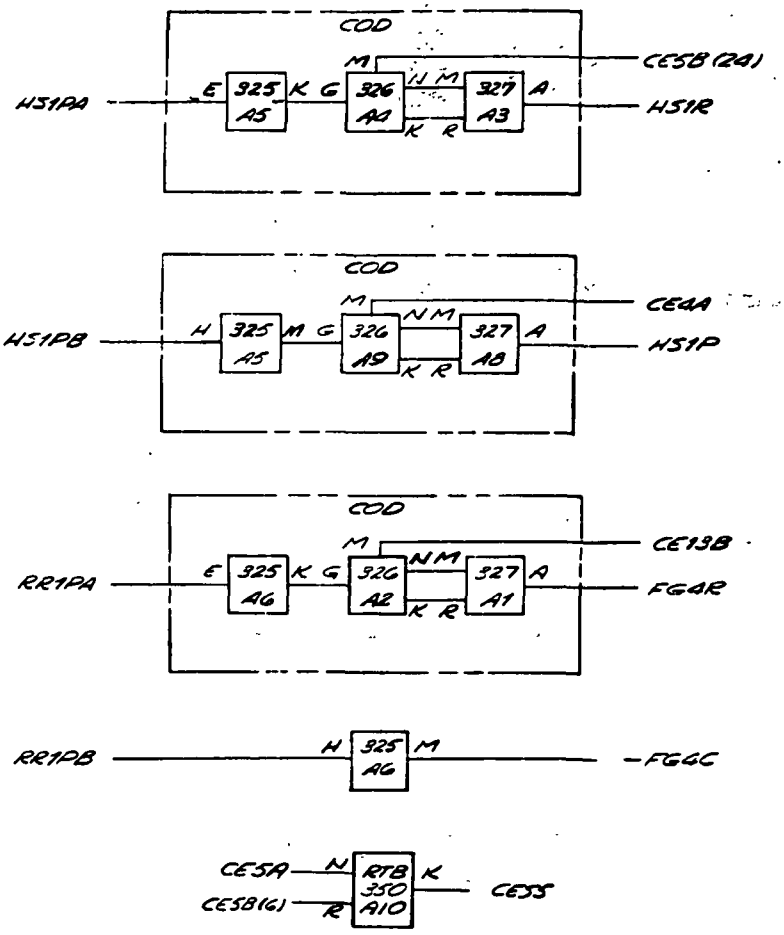


CONNECTOR PINS			
PIN	CONNECTOR	PIN	CONNECTOR
2	XR2PB	52	V7
4	XR2PA	54	
6	CE6B	56	V20
8		58	BU1P
10		60	RFSRTN6
12		62	CG1R
14		64	RFSRTN6
16		66	
18	CE6A	68	
20		70	
22	CE2A	72	
24	CE6B	74	
26		76	
28		78	CE12A
30	SIG-RET	80	CES12
32	V7	82	
34	V20	84	BU3C
36	V5	86	
38	V3	88	
40	BU3P	90	
42	CES6	92	V5
44	V1	94	
46	V3	96	CE12A
48	V1	98	CE12B
50	SIG-RET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A18.
6. This Drawing Derived From IBM DWG NO. 6112659-REL(66123FP)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 5)

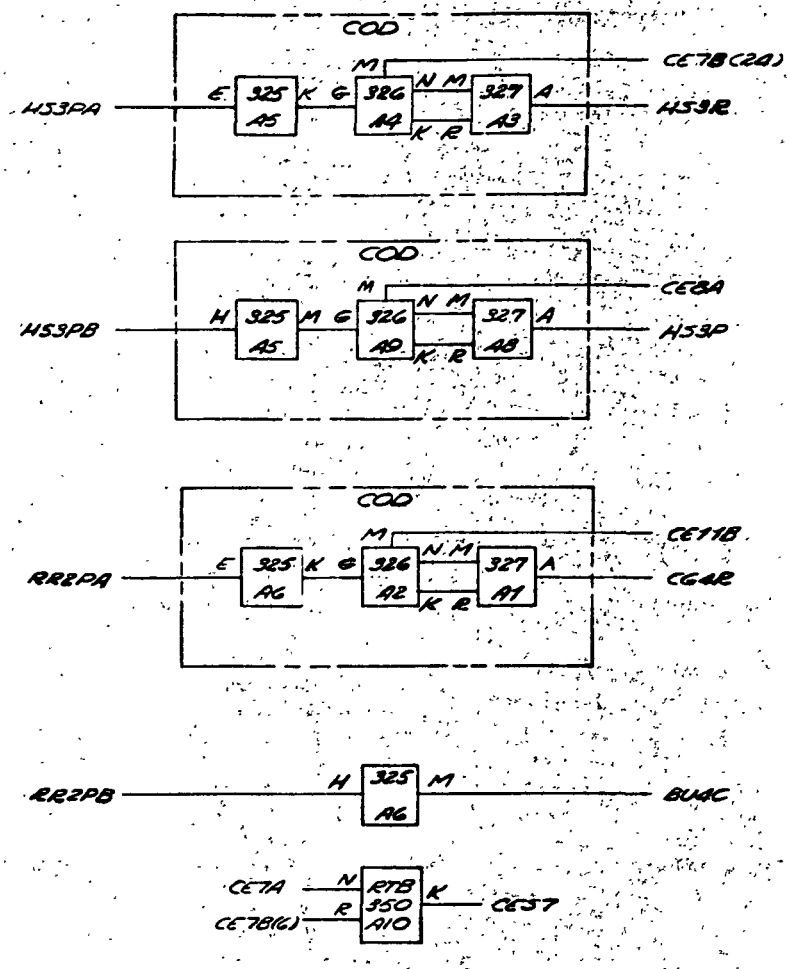


NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A15.
6. This Drawing Derived From IBM DWG NO. 6112649-REL(66123FP)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	HS1PP	52	V7
4	HS1PA	54	
6	CE5B	56	V20
8		58	HS1P
10	V5	60	RF:RTN5
12		62	HS1R
14		64	RF:RTN5
16		66	
18	CE5A	68	
20		70	
22	CE4A	72	
24	CE5B	74	
26		76	
28		78	CE13B
30	SIG:RET	80	
32	V7	82	
34	V20	84	FG4C
36	V5	86	
38	V3	88	
40	CE5S	90	
42	FG4R	92	
44	V1	94	
46	V3	96	RR1PB
48	V1	98	RR1PA
50	SIG:RET		

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 6)

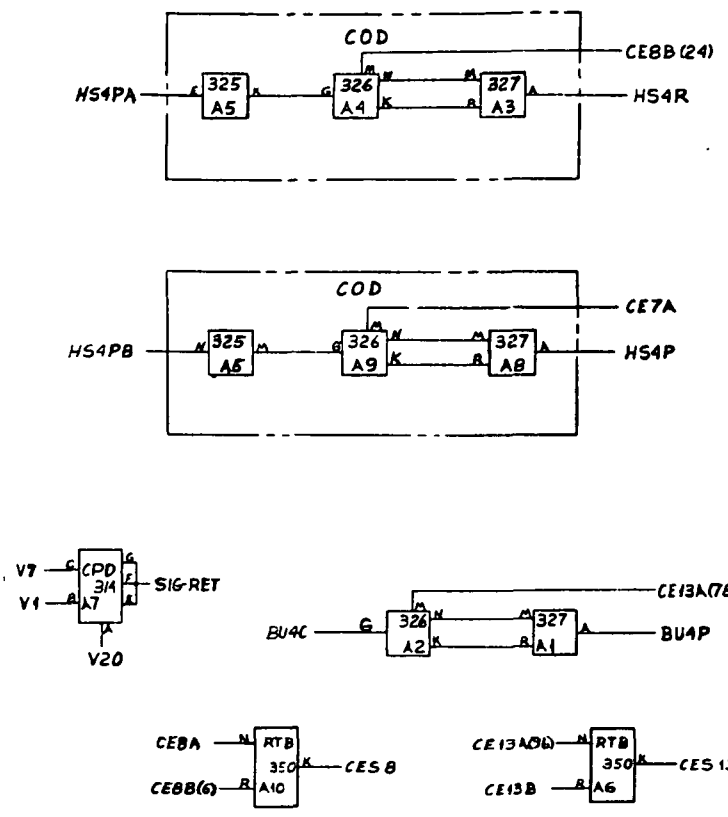


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	H53PB	52	V7
4	H53PA	54	
6	CE7B	56	V20
8		58	H53P
10	V5	60	RFSRTN7
12		62	H53R
14		64	RFSRTN7
16		66	
18	CE7A	68	
20		70	
22	CE8A	72	
24	CE7B	74	
26		76	
28		78	CE11B
30	SIGRET	80	
32	V7	82	
34	V20	84	BU4C
36	V5	86	
38	V3	88	
40	CE37	90	
42	CG4E	92	
44	V1	94	
46	V3	96	RR2PB
48	V1	98	RR2PA
50	SIGRET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A21.
6. This Drawing Derived From IBM DWG NO. 6112667-REL(66123FP)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 7)

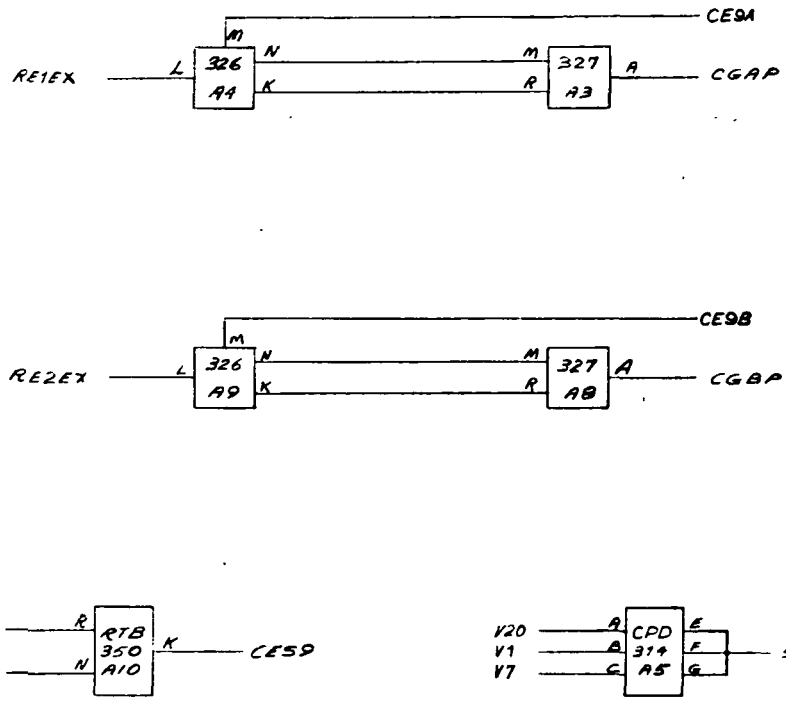


NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A24.
6. This Drawing Derived From IBM DWG NO. 6112669-REL(66123FP)

CONNECTOR PINS			
PIN	CONNECTOR	PIN	CONNECTOR
2	HS4PB	52	V7
4	HS4PA	54	
6	CE8B	56	V20
8		58	HS4P
10		60	RESRTN 8
12		62	HS4R
14		64	RESRTN 8
16		66	
18	CE8A	68	
20		70	
22	CE7A	72	
24	CE8B	74	
26		76	
28		78	CE13A
30	SIG-RET	80	CES 13
32	V7	82	
34	V20	84	BU4C
36	V5	86	
38	V3	88	
40	BU4P	90	
42	CES8	92	V5
44	V1	94	
46	V3	96	CE13A
48	V1	98	CE13B
50	SIG-RET		

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 8)

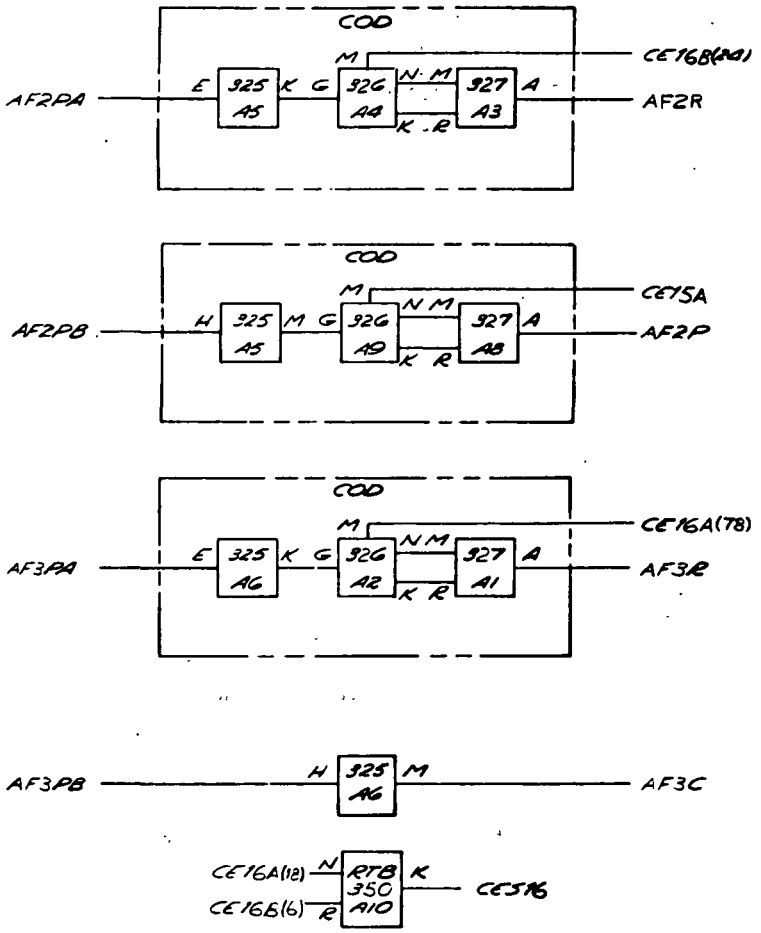


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	V7
4		54	V7
6	RE1EX	56	V20
8		58	CGBP
10		60	RE1RTN
12		62	CGAP
14		64	RE1RTN
16		66	V20
18		68	
20		70	
22		72	
24		74	
26		76	
28	RE2EX	78	
30		80	
32		82	
34	V5	84	
36	V5	86	
38	V3	88	
40	V3	90	
42	CE59	92	
44	SIG-RET	94	
46	V1	96	
48	V1	98	
50	SIG-RET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A5A27.
6. This Drawing Derived From IBM DWG NO. 6112668-REL(66123AK)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 9)

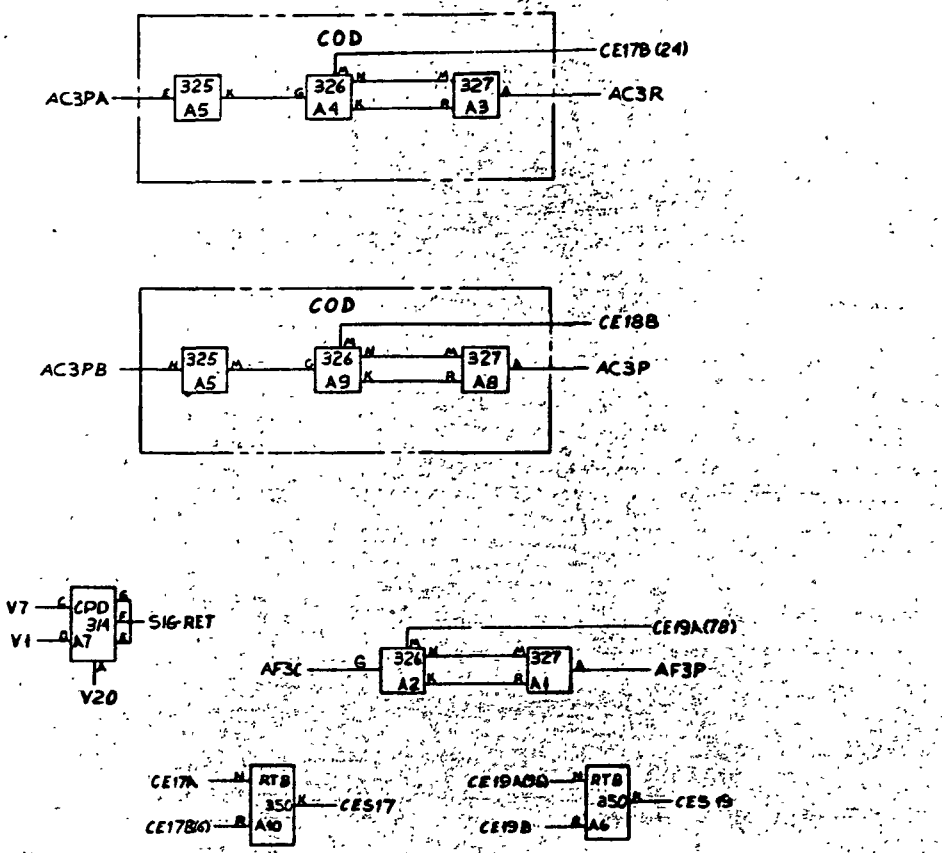


NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A3.
6. This Drawing Derived From IBM DWG NO. 6112437-REL(66123ZL)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	AF2PB	52	V7
4	AF2PA	54	
6	CE16B	56	V20
8		58	AF2P
10	V5	60	RFSRTN2S
12		62	AF2R
14		64	RFSRTN2S
16		66	
18	CE16A	68	
20		70	
22	CE15A	72	
24	CE16B	74	
26		76	
28		78	CE16A
30	SIG-RET	80	
32	V7	82	
34	V20	84	AF3C
36	V5	86	
38	V3	88	
40	CE5T6	90	
42	AF3R	92	
44	V1	94	
46	V3	96	AF3PB
48	V1	98	AF3PA
50	SIGRET		

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 10)

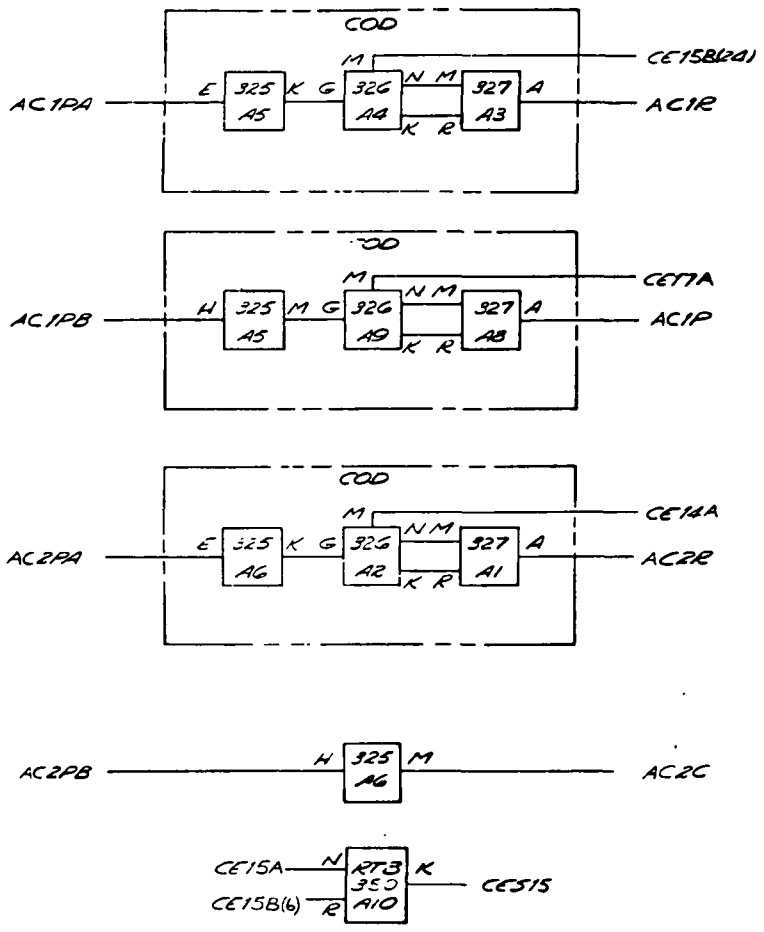


CONNECTOR PIN	CONNECTOR	PIN	CONNECTOR
2	AC3PB	52	V7
4	AC3PA	54	
6	CE17B	56	V20
8		58	AC3P
10		60	RESRTN2B
12		62	AC3R
14		64	RESRTN2B
16		66	
18	CE17A	68	
20		70	
22	CE18B	72	
24	CE17B	74	
26		76	
28		78	CE19A
30	SIG-RET	80	CE519
32	V7	82	
34	V20	84	AF3C
36	V5	86	
38	V3	88	
40	AF3P	90	
42	CE517	92	V5
44	V1	94	
46	V3	96	CE19A
48	V1	98	CE19B
50	SIG-RET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A6.
6. This Drawing Derived From IBM DWG NO. 6112439-REL(66123ZL)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 11)

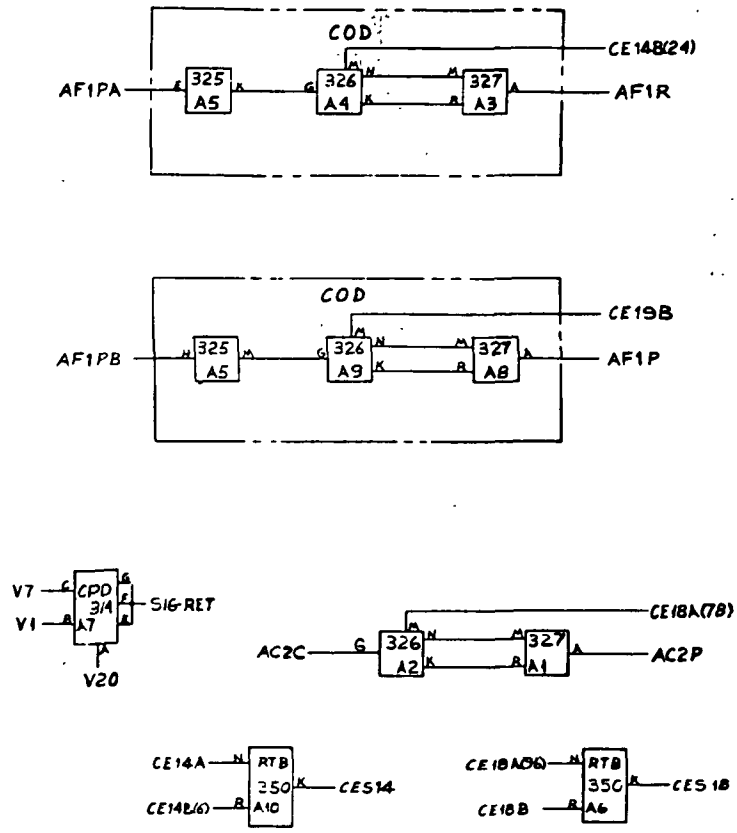


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	AC1PB	1	V7
4	AC1PA	3	
6	CE15B	5	120
8		7	AC1P
10	V5	60	RESRTNIT
12		2	AC1R
14		4	RESRTNIT
16		6	
18	CE15A	68	
20		70	
22	CE17A	72	
24	CE15B	74	
26		76	
28		78	CE14A
30	SIG-RET	80	
32	V7	82	
34	V120	84	AC2C
36	V5	86	
38	V3	88	
40	CE15	90	
42	AC2R	92	
44	V1	94	
46	V3	96	AC2PB
48	V1	98	AC2PA
50	SIGRET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A11.
6. This Drawing Derived From IBM DWG NO. 6112517-REL(66123ZL)

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 12)



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.

537 5. Prefix Reference Designator as Follows: 2A6A22.

6. This Drawing Derived From IBM DWG NO. 6112537-REL(66123ZL)

CONNECTOR PIN	CONNECTOR	PINS PIN	CONNECTOR
2	AF1PB	52	V7
4	AF1PA	54	
6	CE14B	56	V20
8		58	AF1P
10		60	RFSRTN1
12		62	AF1R
14		64	RFSRTN14
16		66	
18	CE14A	68	
20		70	
22	CE19B	72	
24	CE14B	74	
26		76	
28		78	CE18A
30	SIG-RET	80	CES18
32	V7	82	
34	V20	84	AC2C
36	V5	86	
38	V3	88	
40	AC2P	90	
42	CES14	92	V5
44	V1	94	
46	V3	96	CE18A
48	V1	98	CE18B
50	SIG-RET		

Figure 10-14. Resolver Processor (Crossover Detectors) Logic Diagram (Sheet 13)

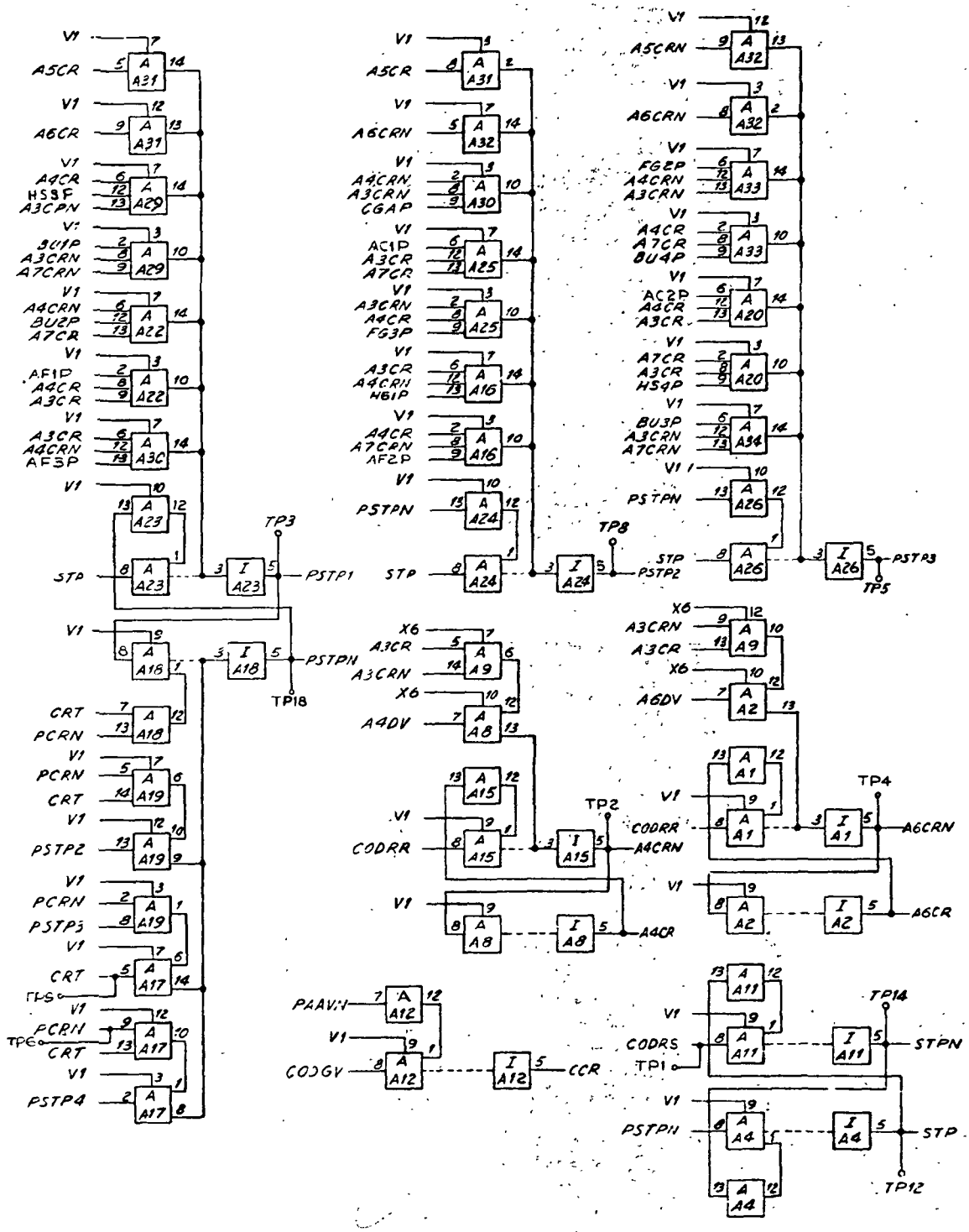
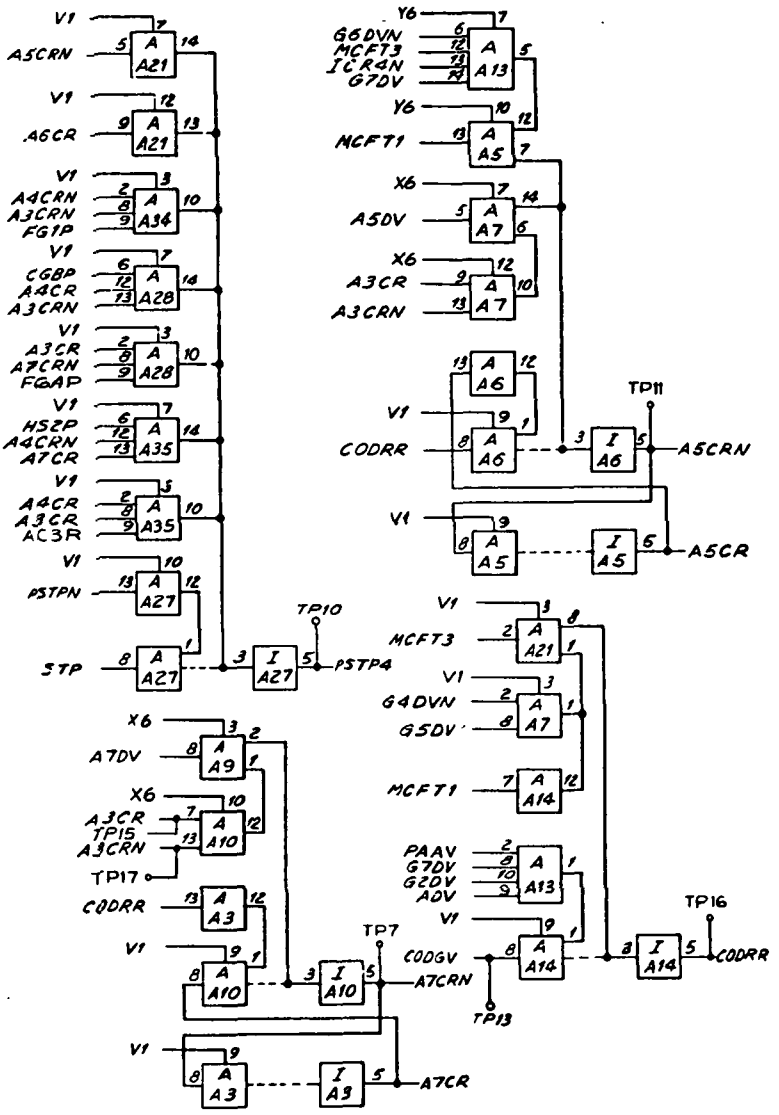


Figure 10-15. Resolver Processor (Multiplexer) Logic Diagram (Sheet 1 of 4)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	PSTPN	16	A4CR
2		17	STP
3		18	
4		19	G7DV
5	A3CR	20	A3CRN
6		21	A4CRN
7	G6DVN	22	PAAV
8		23	CODRR
9	G2DV	24	CCR
10	MCFT1	25	PCRN
11	A6CRN	26	MCFT3
12	A5CR	27	A7CR
13	A5CRN	28	CODGV
14	A5CR	29	A7CRN
15	CRT	30	CODRS

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	BU4P
3	BU1P	53	G4DVN
5	G6DVN	55	G5DV
7	A4DV	57	FG2P
9	HS3P	59	Y6
11	AF1P	61	FG1P
13	SU2P	63	A6DV
15	AF2P	65	HS4P
17	A5CR	67	AC2P
19	SIG-RET	69	A7DV
21	HS1P	71	FGAP
23	AF3P	73	BU3P
25	CGAP	75	
27	CCR	77	AC3D
29	A6CR	79	CGBP
31	FG3P	81	A7CR
33	X6	83	
35	PAAVN	85	HS2P
37	G7DV	87	
39	ICR4N	89	
41	ADV	91	
43	A4CR	93	
45	A5DV	95	MCFT3
47	AC1P	97	MCFT1
49	V1		

ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5 I	A6 I	A7 AB
A8 I	A9 AB	A10 I	A11 I	A12 I	A13 AA	A14 I
A15 I	A16 AA	A17 AB	A18 I	A19 AB	A20 AA	A21 AB
A22 AA	A23 I	A24 I	A25 AA	A26 I	A27 I	A28 AA
A29 AA	A30 AA	A31 AB	A32 AB	A33 AA	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A29 Side A, 2A6A18 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112188-A(66126CM)

Figure 10-15. Resolver Processor (Multiplexer) Logic Diagram (Sheet 2)

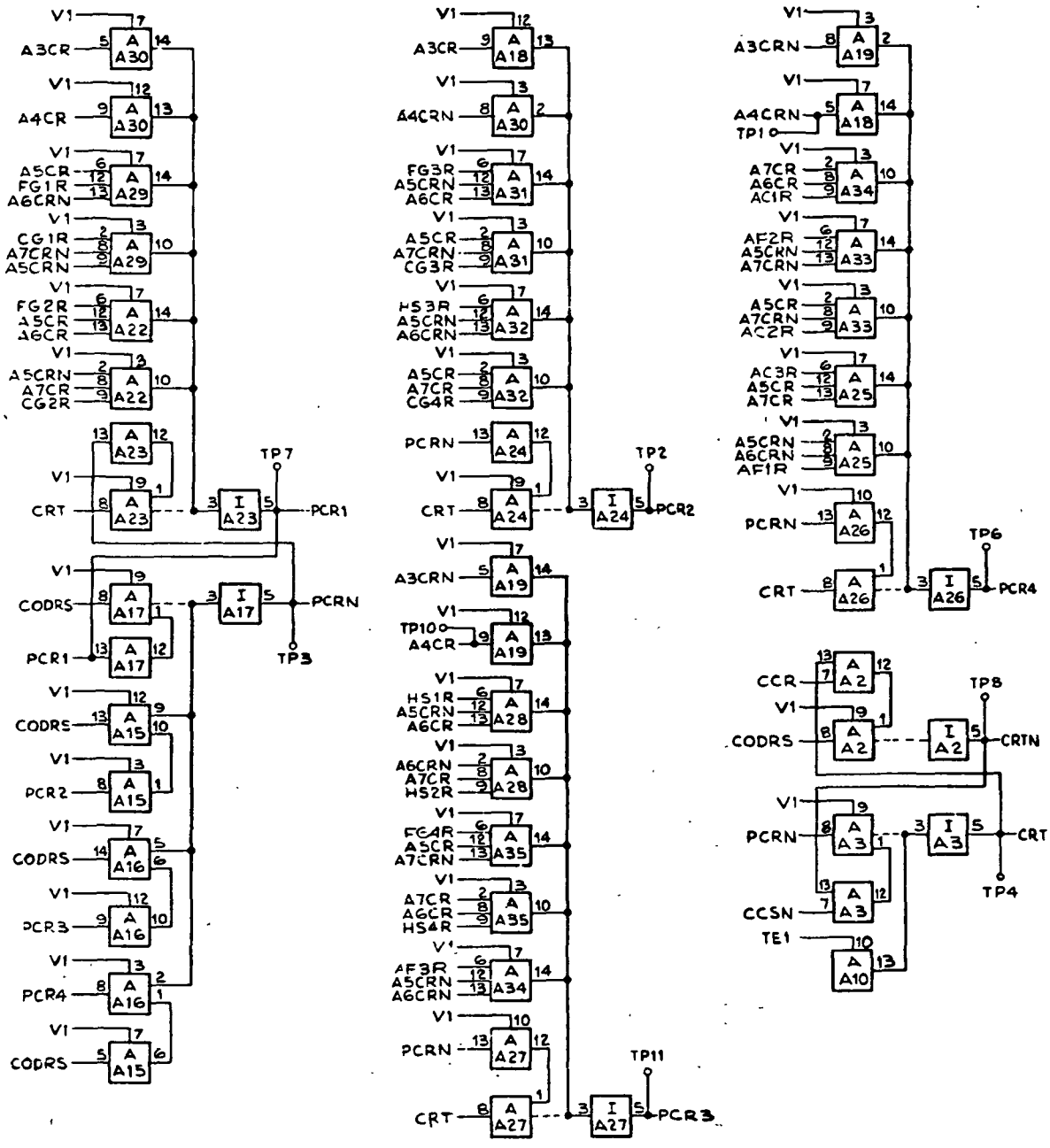
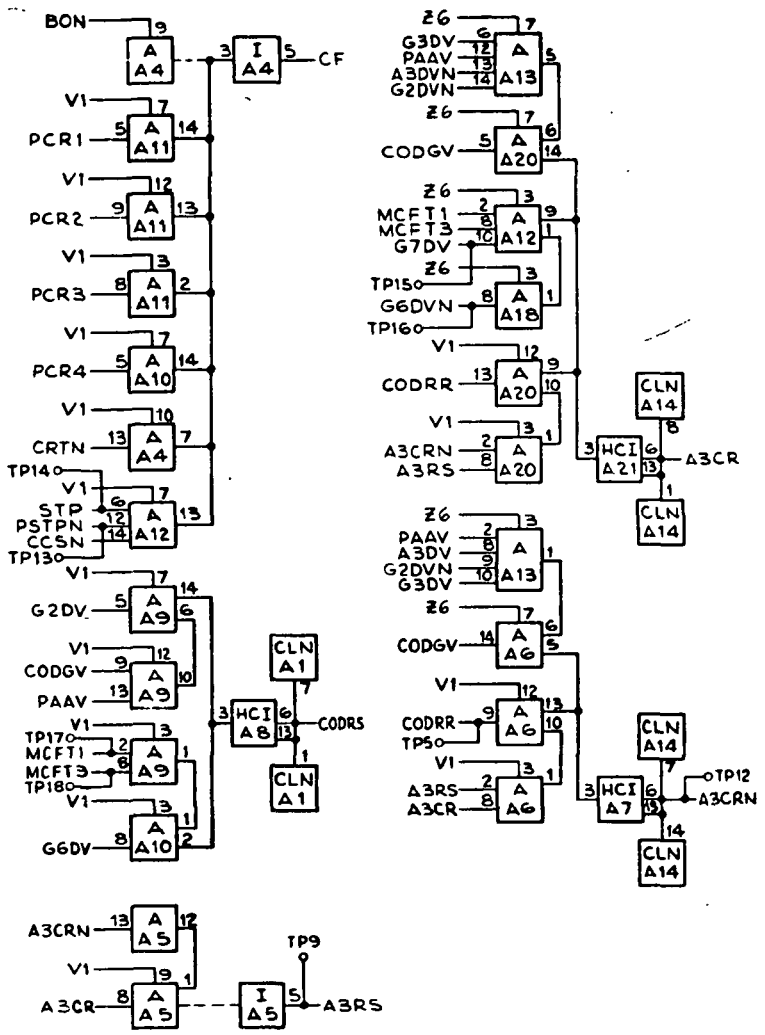


Figure 10-15. Resolver Processor (Multiplexer) Logic Diagram (Sheet 3)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	PSTPN	16	A4CR
2		17	STP
3		18	
4		19	G7DV
5	A3CR	20	A3CRN
6		21	A4CRN
7	G6DVN	22	PAAV
8		23	CODRR
9	G2DV	24	CCR
10	MCFT1	25	PCRN
11	A6CRN	26	MCFT3
12	A6CR	27	A7CR
13	A5CRN	28	CODGV
14	A5CR	29	A7CRN
15	CRT	30	CODRS

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4	A3DV	54	
6	SIG-RET	56	
8	V1	58	
10	V3	60	AC3R
12	Z6	62	AF1R
14	PAAV	64	
16	TEI	66	BON
18	A3CR	68	G2DVN
20		70	HS3R
22		72	CG4R
24		74	G3DV
26	CCSN	76	FG3R
28	FG4R	78	
30	HS4R	80	CG3R
32	HS1R	82	
34	HS2R	84	
36		86	FG1R
38	G6DV	88	CGDRS
40	AF3R	90	CG2R
42	AC1R	92	FG2R
44	AF2R	94	G2DV
46	AC2R	96	CODGV
48	A3DVN	98	CG1R
50	CF		

ULD LOCATIONS

A1 CLN	A2 I	A3 I	A4 I	A5 I	A6 AB	A7 HCI
A8 HCI	A9 AB	A10 AB	A11 AB	A12 AA	A13 AA	A14 CLN
A15 AB	A16 AB	A17 I	A18 AB	A19 AB	A20 AB	A21 HCI
A22 AA	A23 I	A24 I	A25 AA	A26 I	A27 I	A28 AA
A29 AA	A30 AB	A31 AA	A32 AA	A33 AA	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A29 Side B, 2A6A18 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112218-C(66126GM)

Figure 10-15. Resolver Processor (Multiplexer) Logic Diagram (Sheet 4)

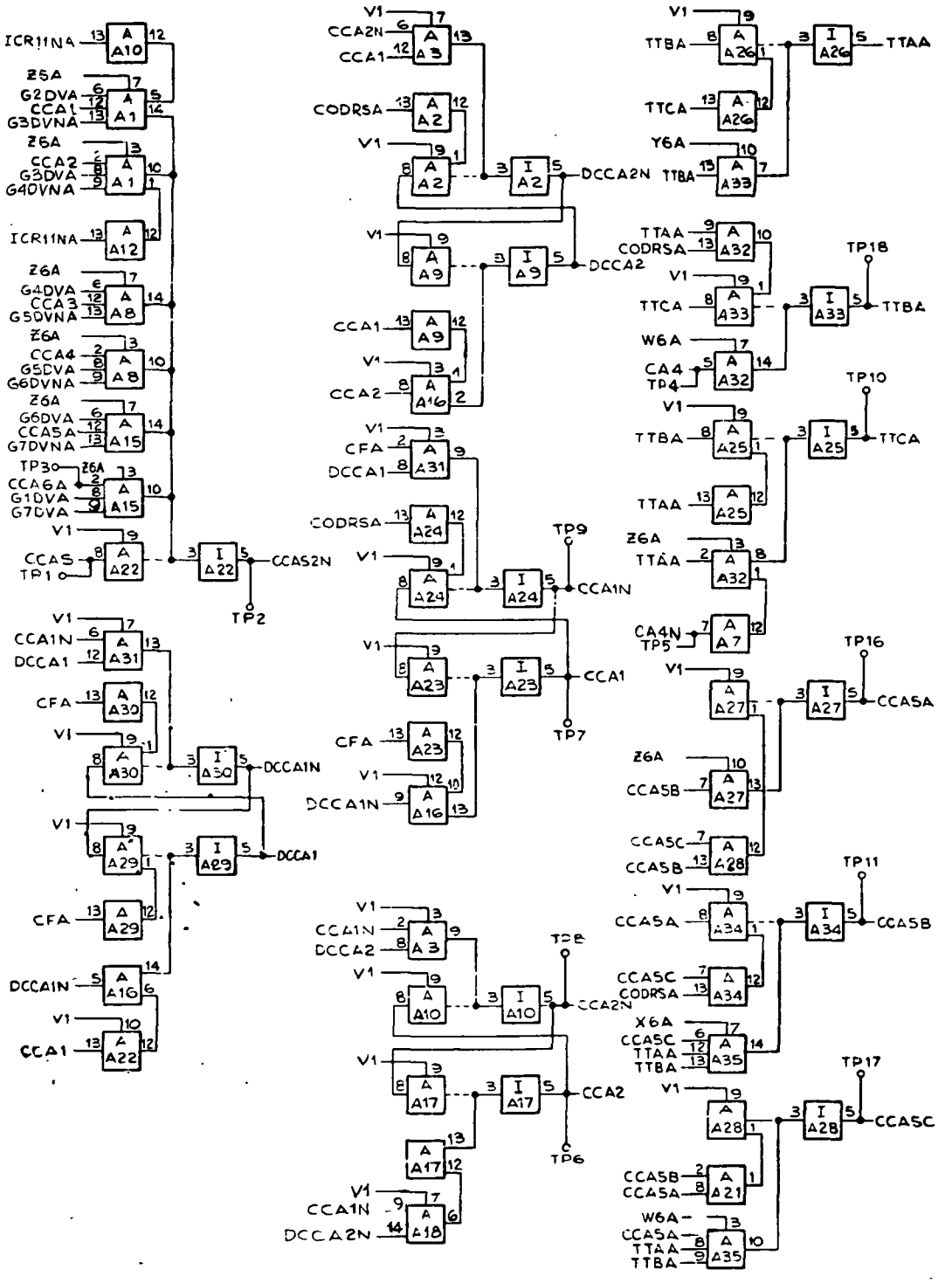
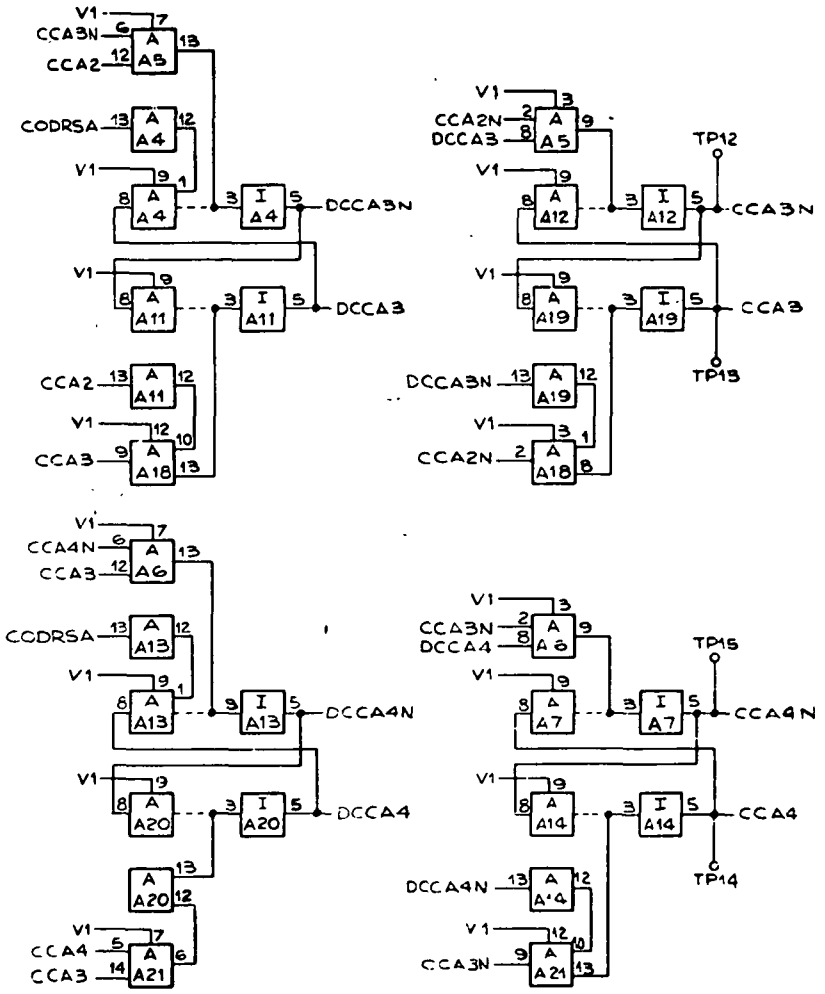


Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 1 of 8)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CCA5	16	CCA6A
2	G4DVNA	17	CCA52N
3	G6DVA	18	G2DVA
4		19	G3DVNA
5	G5DVA	20	G4DVA
6	G3DVA	21	G5DVNA
7		22	Z6A
8	CA4N	23	
9		24	
10		25	Y6A
11	CCA4N	26	CCA4
12		27	
13	CA4	28	X6A
14		29	W6A
15	CCA5A	30	CCA5B

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CFA	51	DCCA2N
3	Z6A	53	
5	G6DVNA	55	X6A
7	V3	57	
9		59	
11	SIG RET	61	DCCA3
13		63	
15	V1	65	DCCA3N
17		67	DCCA4
19		69	
21	G7DVA	71	DCCA4N
23		73	
25	G1DVA	75	TTAA
27		77	
29	DCCA1N	79	
31		81	CODPSA
33	G7DVNA	83	W6A
35		85	
37		87	
39		89	
41	Y6A	91	
43	DCCA2	93	
45	DCCA1	95	
47		97	
49	ICP11NA		

ULD LOCATIONS

A1 AA	A2 I	A3 AA	A4 I	A5 AA	A6 AA	A7 I
A8 AA	A9 I	A10 I	A11 I	A12 I	A13 I	A14 I
A15 AA	A16 AB	A17 I	A18 AB	A19 I	A20 I	A21 AB
A22 I	A23 I	A24 I	A25 I	A26 I	A27 I	A28 I
A29 I	A30 I	A31 AA	A32 AB	A33 I	A34 I	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A30 Side A.
6. This Drawing Derived From IBM DWG NO. 6112288-B(66123RE)

Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 2)

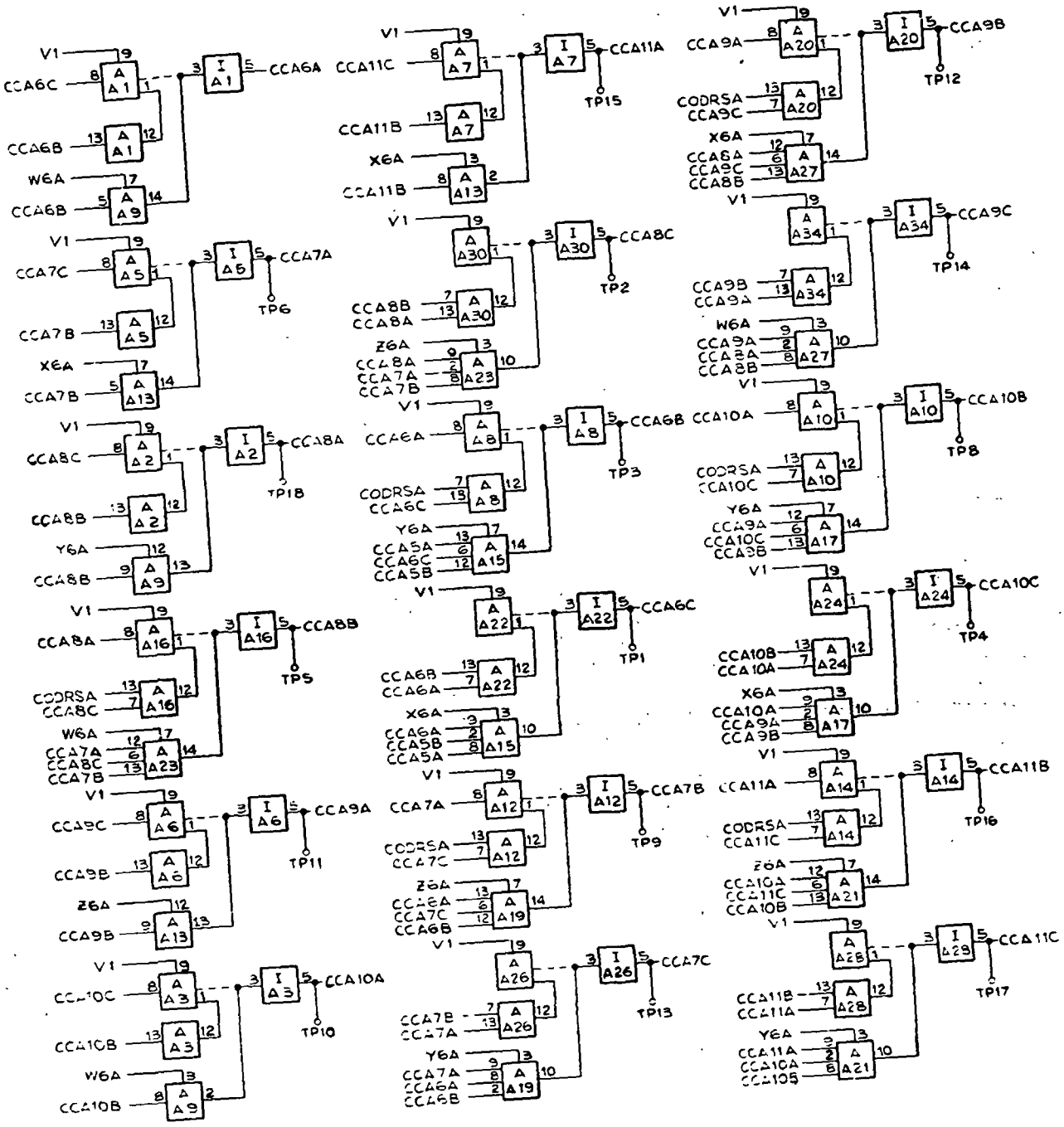
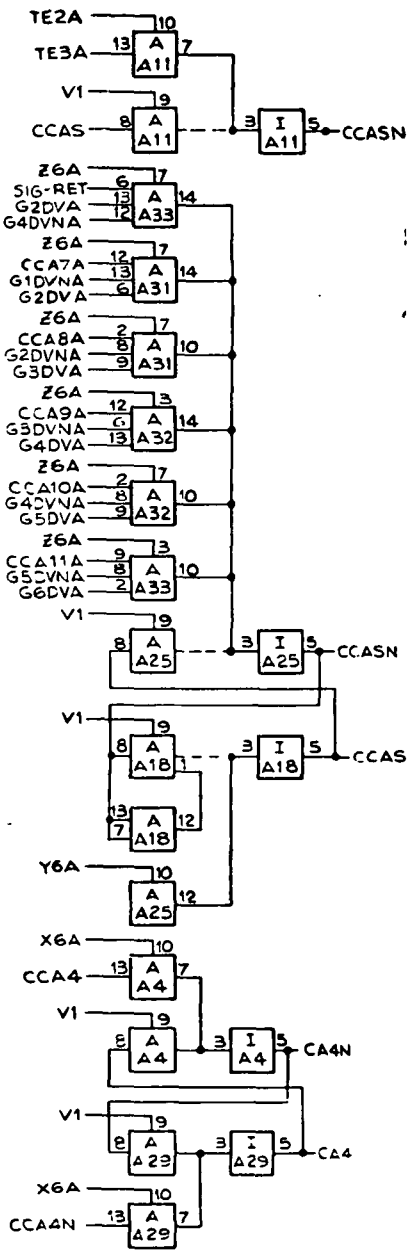


Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 3)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CCAS	16	CCA6A
2	G4DVNA	17	CCASN
3	G6DVA	18	G2DVA
4		19	G3DVNA
5	G5DVA	20	G4DVA
6	G3DVA	21	G5DVNA
7		22	Z6A
8	CA4N	23	
9		24	
10		25	Y6A
11	CCA4N	26	CCA4
12		27	
13	CA4	28	X6A
14		29	W6A
15	CCA5A	30	CCA5B

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4		54	G4DVNA
6		56	G5DVA
8		58	CCAS
10		60	TE2A
12		62	TE3A
14		64	
16	CODPSA	66	
18		68	
20		70	G2DVNA
22		72	G1DVNA
24		74	G3DVA
26		76	
28		78	
30		80	
32		82	
34		84	G3DVNA
36	G6DVA	86	Y6A
38	SIG-RET	88	V3
40	G5DVNA	90	SIG-RET
42		92	
44	G4DVA	94	G2DVA
46	CCAS N	96	
48		98	
50	V1		

ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5 I	A6 I	A7 I
A8 I	A9 AB	A10 I	A11 I	A12 I	A13 AB	A13 I
A15 AA	A16 I	A17 AA	A18 I	A19 AA	A20 I	A21 AA
A22 I	A23 AA	A24 I	A25 I	A26 I	A27 AA	A28 I
A29 I	A30 I	A31 AA	A32 AA	A33 AA	A34 I	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A30 Side B.
6. This Drawing Derived From IBM DWG NO. 6112318-A(66126EJ)

Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 4)

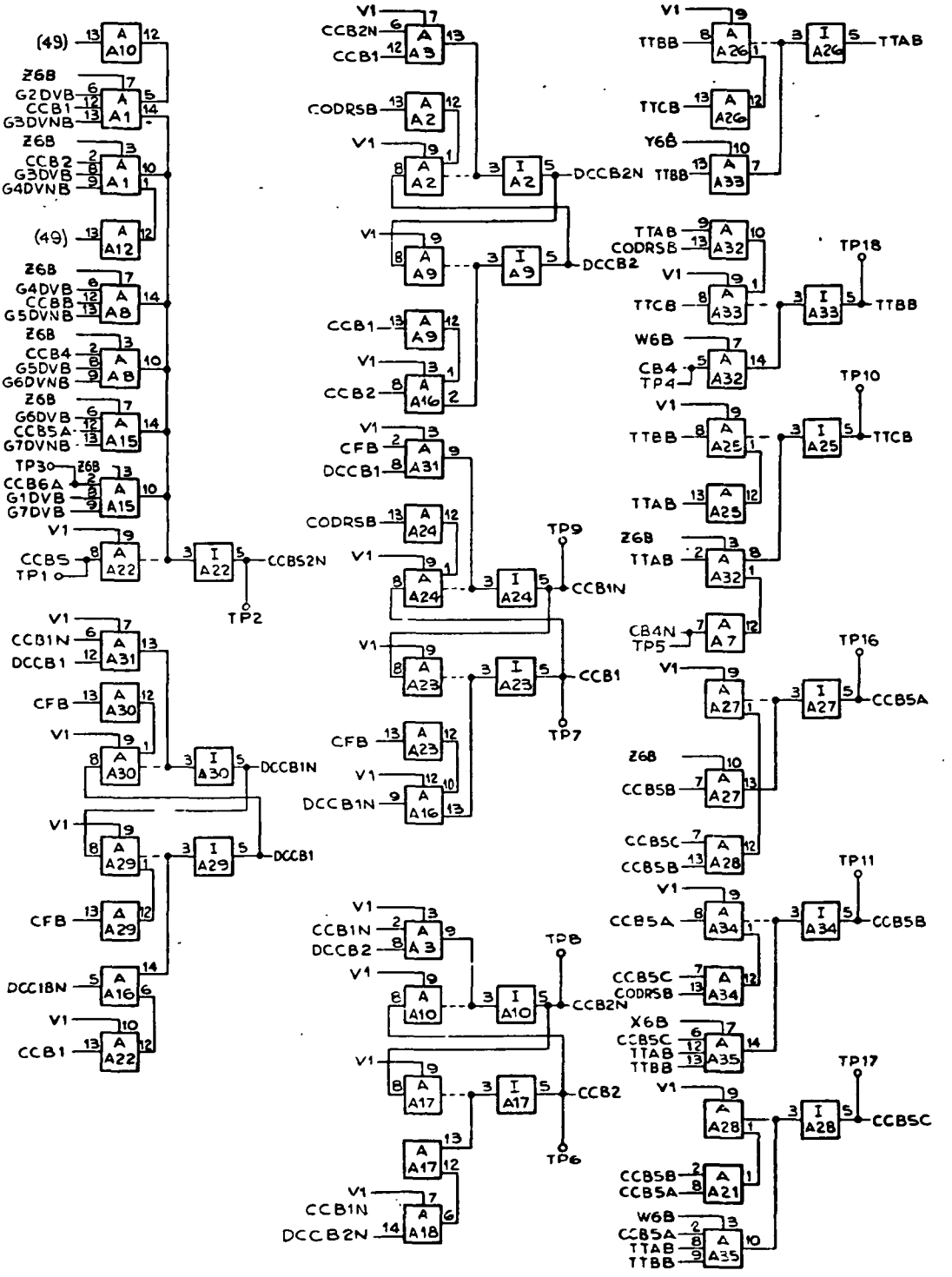
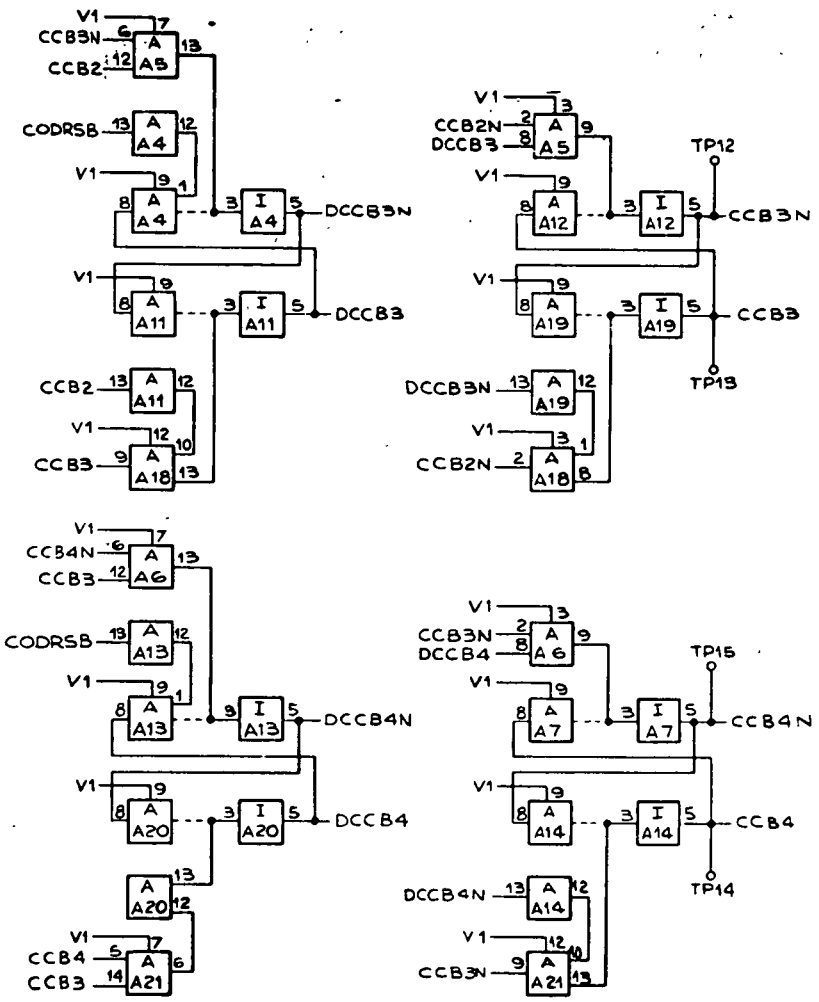


Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 5)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CCB5	16	CCB6A
2	G4DVNB	17	CCB52N
3	G6DVB	18	G2DVB
4		19	G3DVNB
5	G5DVB	20	G4DVB
6	G3DVB	21	G5DVNB
7		22	Z6B
8	CB4N	23	
9		24	
10		25	Y6B
11	CCB4N	26	CCB4
12		27	
13	CB4	28	X6B
14		29	W6B
15	CCB5A	30	CCB5B

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CFB	51	DCCB2N
3	Z6B	53	
5	G6DVNB	55	X6B
7	V3	57	
9		59	
11	SIG RET	61	DCCB3
13		63	
15	V1	65	DCCB3N
17		67	DCCB4
19		69	
21	G7DVB	71	DCCB4N
23		73	
25	G1DVB	75	TTAB
27		77	
29	DCCB1N	79	
31		81	CODRSB
33	G7DVNB	83	W6B
35		85	
37		87	
39		89	
41	Y6B	91	
43	DCCB2	93	
45	DCCB1	95	
47		97	
49			

ULD LOCATIONS

A1 AA	A2 I	A3 AA	A4 I	A5 AA	A6 AA	A7 I
A8 AA	A9 I	A10 I	A11 I	A12 I	A13 I	A14 I
A15 AA	A16 AB	A17 I	A18 AB	A19 I	A20 I	A21 AB
A22 I	A23 I	A24 I	A25 I	A26 I	A27 I	A28 I
A29 I	A30 I	A31 AA	A32 AB	A33 I	A34 I	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A19 Side A.
6. This Drawing Derived From IBM DWG NO. 6112289-B(66123RE)

Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 6)

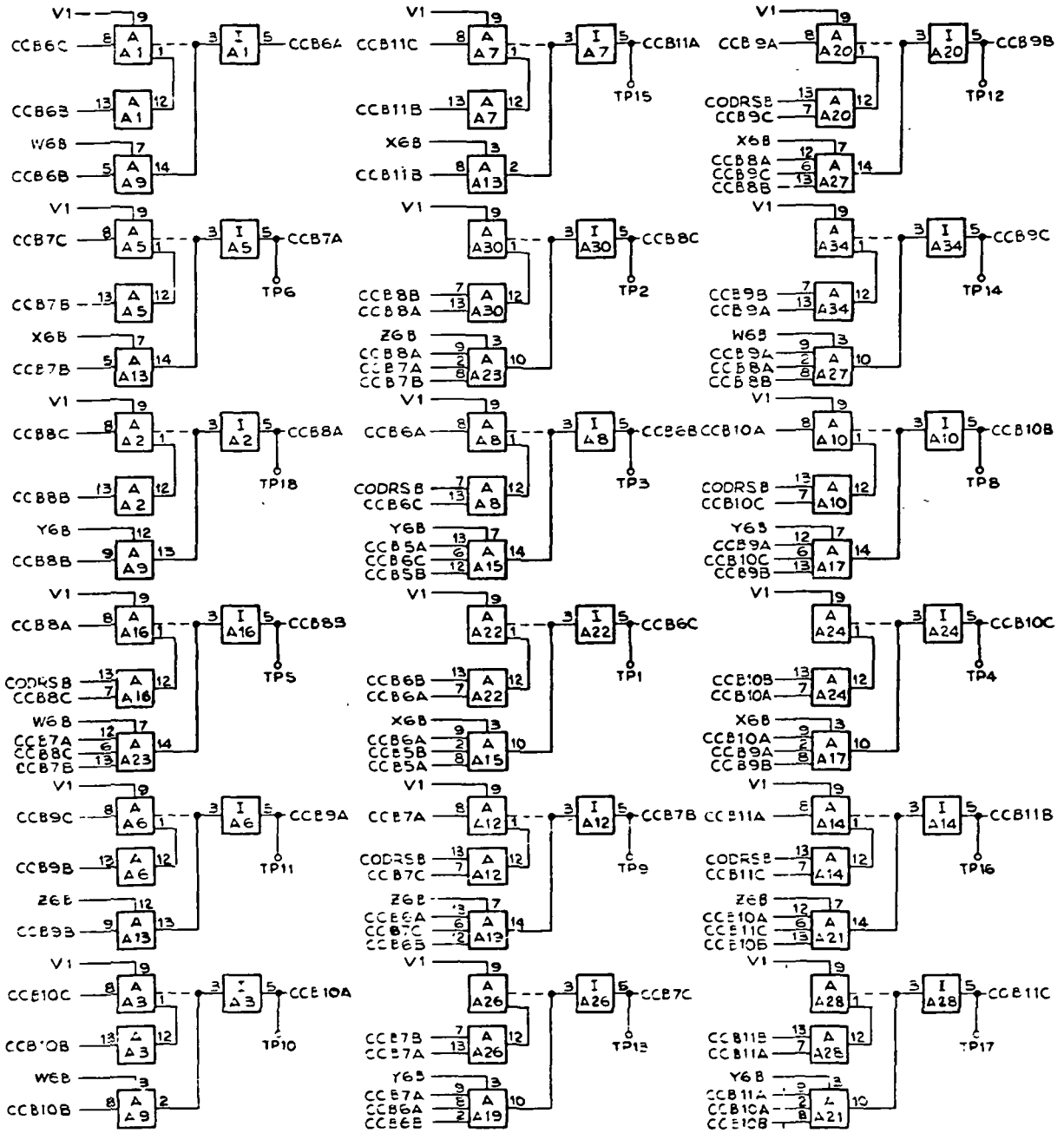
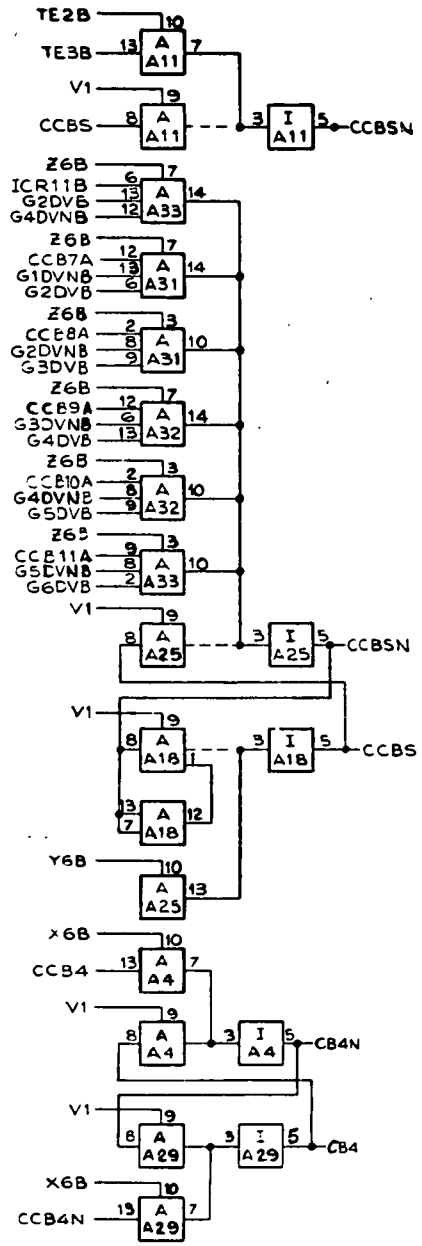


Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 7)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	CCBS	16	CCB6A
2	G4DVNB	17	CCBSN
3	G6DVB	18	G2DVB
4		19	G3DVNB
5	G5DVB	20	G4DVB
6	G3DVB	21	G5DVNB
7		22	Z6B
8	CB4N	23	
9		24	
10		25	Y6B
11	CCB4N	26	CCB4
12		27	
13	CB4	28	X6B
14		29	W6B
15	CCB5A	30	CCB5B

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4		54	G4DVNB
6		56	G5DVB
8		58	CCBS
10		60	TE2B
12		62	TE3B
14		64	
16	CODRSB	66	
18		68	
20		70	G2DVNB
22		72	G1DVNB
24		74	G3DVB
26		76	
28		78	
30		80	
32		82	
34		84	G3DVNB
36	G6DVB	86	Y6B
38	ICR11B	88	
40	G5DVNB	90	SIG-RET
42		92	
44	G4DVB	94	G2DVB
46	CCBSN	96	
48		98	
50	V1		

ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5 I	A6 I	A7 I
A8 I	A9 AB	A10 I	A11 I	A12 I	A13 AE	A14 I
A15 AA	A16 I	A17 AA	A18 I	A19 AA	A20 I	A21 AA
A22 I	A23 AA	A24 I	A25 I	A26 I	A27 AA	A28 I
A29 I	A30 I	A31 AA	A32 AA	A33 AA	A34 I	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A19 Side B.
6. This Drawing Derived From IBM DWG NO. 6112319-A(66126EJ)

Figure 10-16. Resolver Processor (Counters) Logic Diagram (Sheet 8)

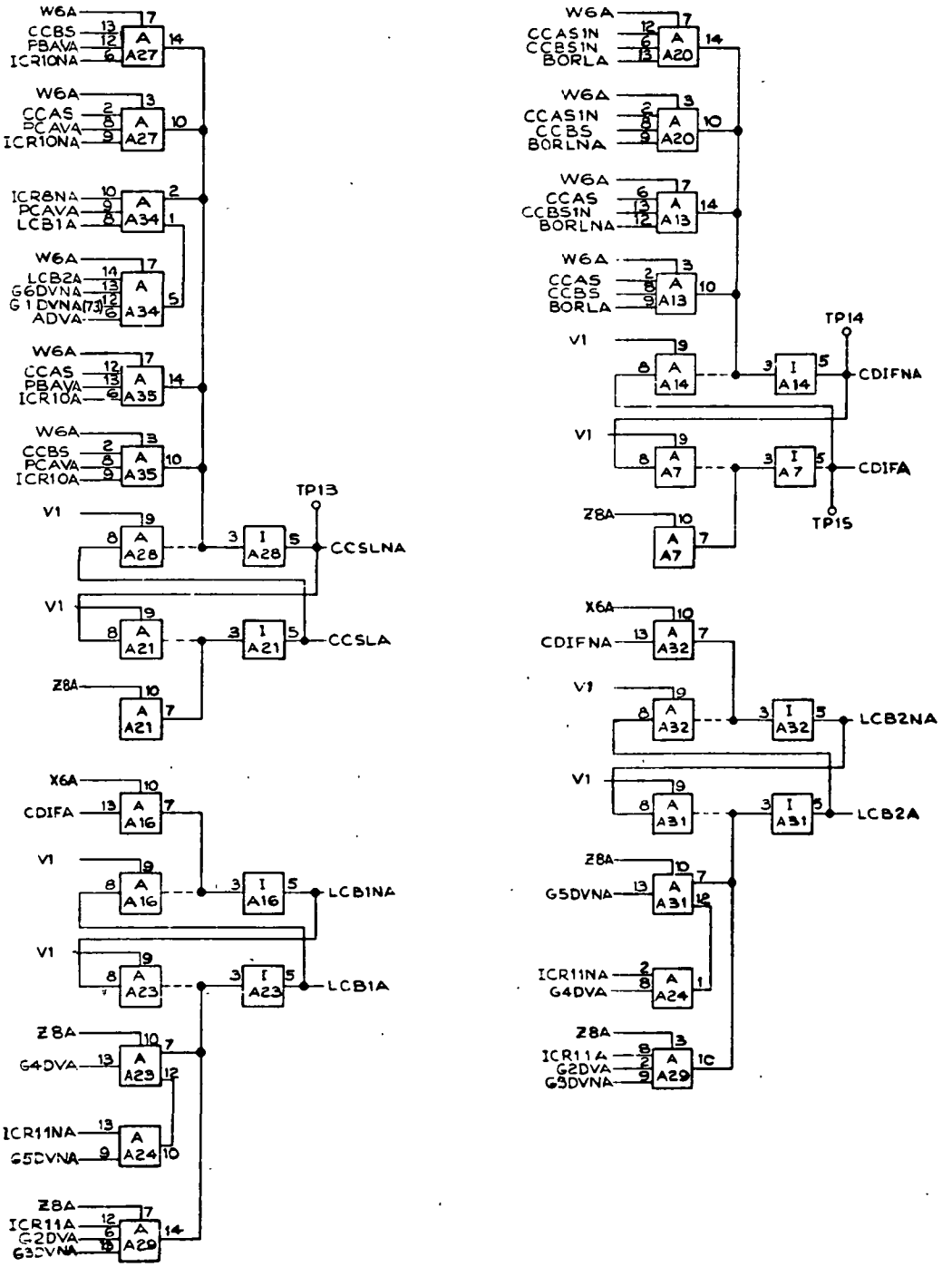
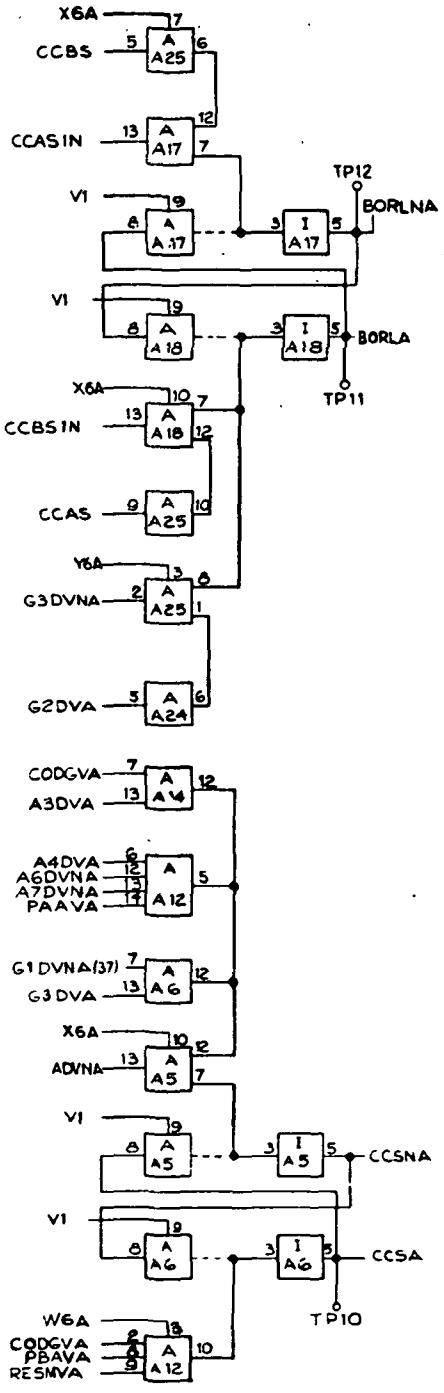


Figure 10-17. Resolver Processor (Subtractor and Limit Check) Logic Diagram (Sheet 1 of 4)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	CCBS
3	SIG- RET	53	CCBSIN
5	G6DVNA	55	X6A
7	ICR11A	57	CCAS
9		59	
11	CCSNA	61	RESMVA
13	Z8A	63	
15	G3DVA	65	
17	LCB1NA	67	A7DVNA
19		69	ICR10NA
21		71	LCB1A
23	ADVNA	73	G1DVNA
25	V1	75	ICR8NA
27	ICR11NA	77	PAAVA
29		79	W6A
31		81	CCSLA
33	LCB2NA	83	G3DVNA
35	Y6A	85	PCAVA
37	G1DVNA	87	A4DVA
39	G5DVNA	89	ICR10A
41	ADVA	91	A3DVA
43	G4DVA	93	G2DVA
45	CCASIN	95	PBAVA
47	LCB2A	97	CODGVA
49	A6DVNA		

ULD LOCATIONS

A1	A2	A3	A4	A5 I	A6 I	A7 I
A8	A9	A10	A11	A12 AA	A13 AA	A14 I
A15	A16 I	A17 :	A18 :	A19	A20 AA	A21 I
A22	A23 I	A24 AB	A25 AB	A26	A27 AA	A28 I
A29 AA	A30	A31 I	A32 I	A33	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A31 Side A.
6. This Drawing Derived From IBM DWG NO. 6112558-A(66123TE)

Figure 10-17. Resolver Processor (Subtractor and Limit Check) Logic Diagram (Sheet 2)

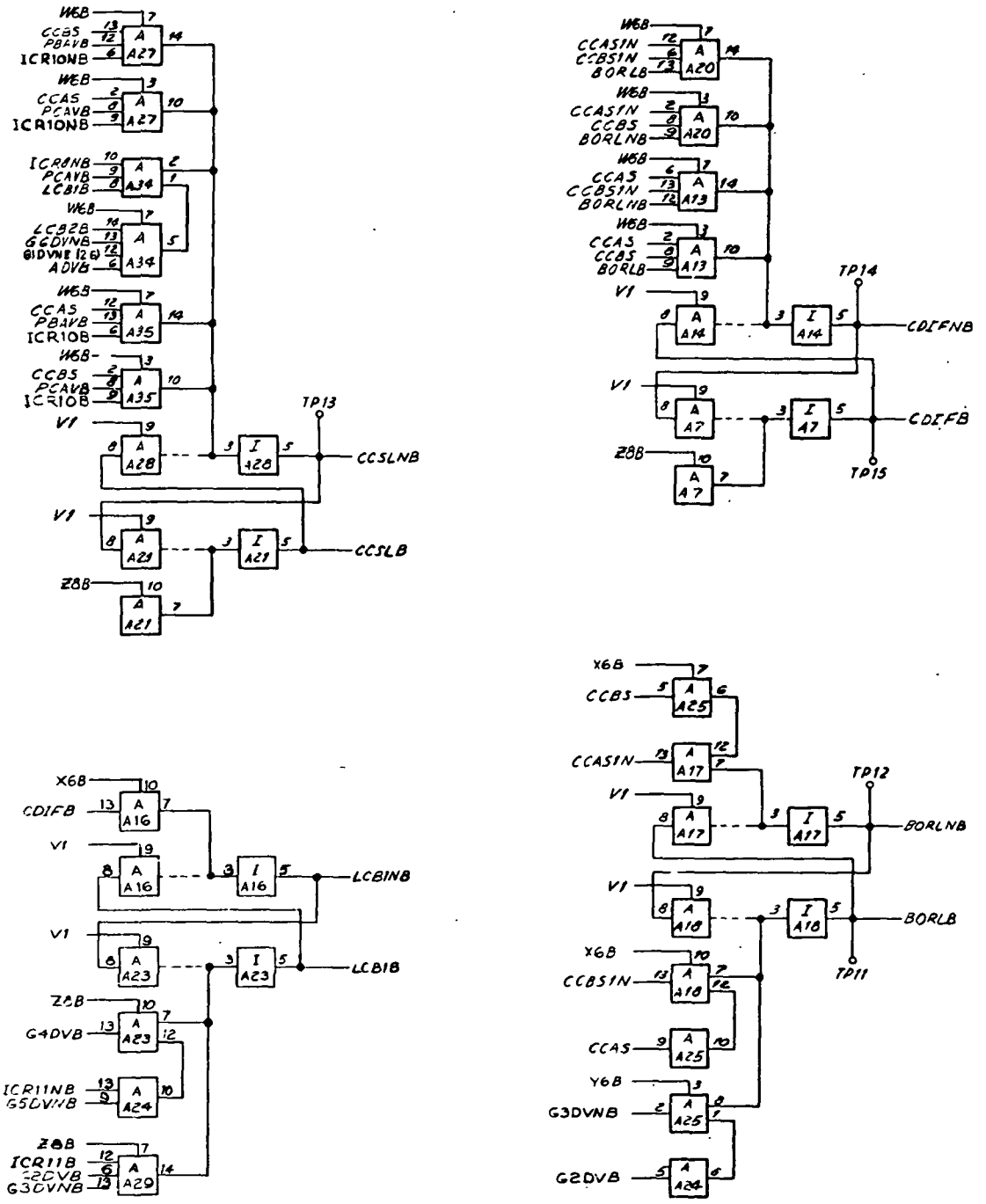
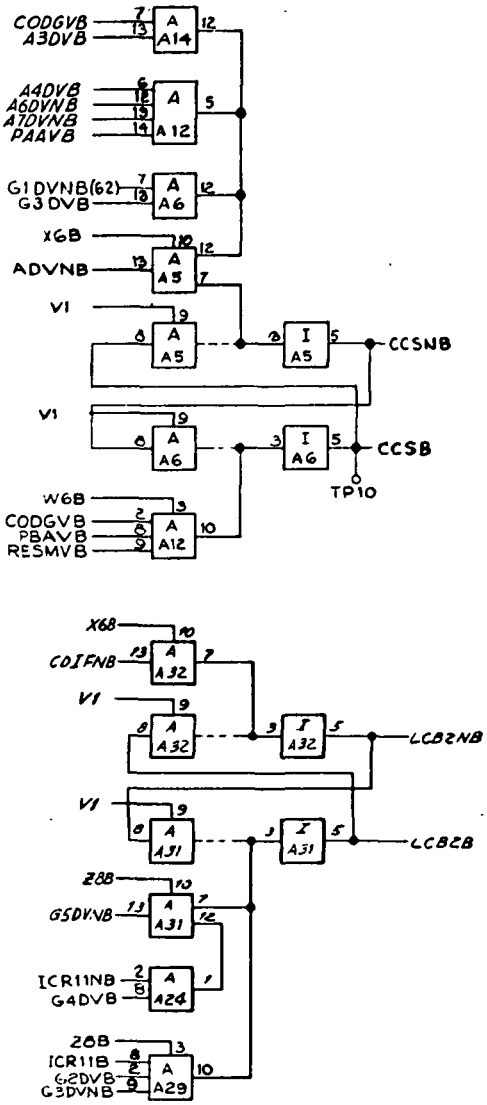


Figure 10-17. Resolver Processor (Subtractor and Limit Check) Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	CODGVB	52	LCB2B
4	PBAVB	54	CCASIN
6	G2DVB	56	G4DVB
8	A3DVB	58	A1DVB
10	ICR10B	60	G5DVNB
12	A4DVB	62	G1DVNB
14	PCAVB	64	YGB
16	G3DVNB	66	LCB2NB
18	CCSLB	68	
20	W6B	70	
22	PAAVB	72	ICR11NB
24	ICR8NB	74	V1
26	G1DVNB	76	ADVNB
28	LCB1B	78	
30	ICR10NB	80	
32	A7DVNB	82	LCB1NB
34		84	G3DVB
36		86	Z8B
38	RESMVB	88	CCSNB
40		90	
42	CCAS	92	ICR11B
44	XGB	94	GGDVNB
46	CCBSIN	96	SIG-RET
48	CCBS	98	V3
50	AGCVNB		

ULD LOCATIONS

A1	A2	A3	A4	A5 I	A6 I	A7 I
A8	A9	A10	A11	A12 AA	A13 AA	A14 I
A15	A16 I	A17 I	A18 I	A19	A20 AA	A21 I
A22	A23 I	A24 AB	A25 AB	A26	A27 AA	A28 I
A29 AA	A30	A31 I	A32 I	A33	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A31 Side B.
6. This Drawing Derived From IBM DWG NO. 6112559-A(66123TE)

Figure 10-17. Resolver Processor (Subtractor and Limit Check) Logic Diagram (Sheet 4)

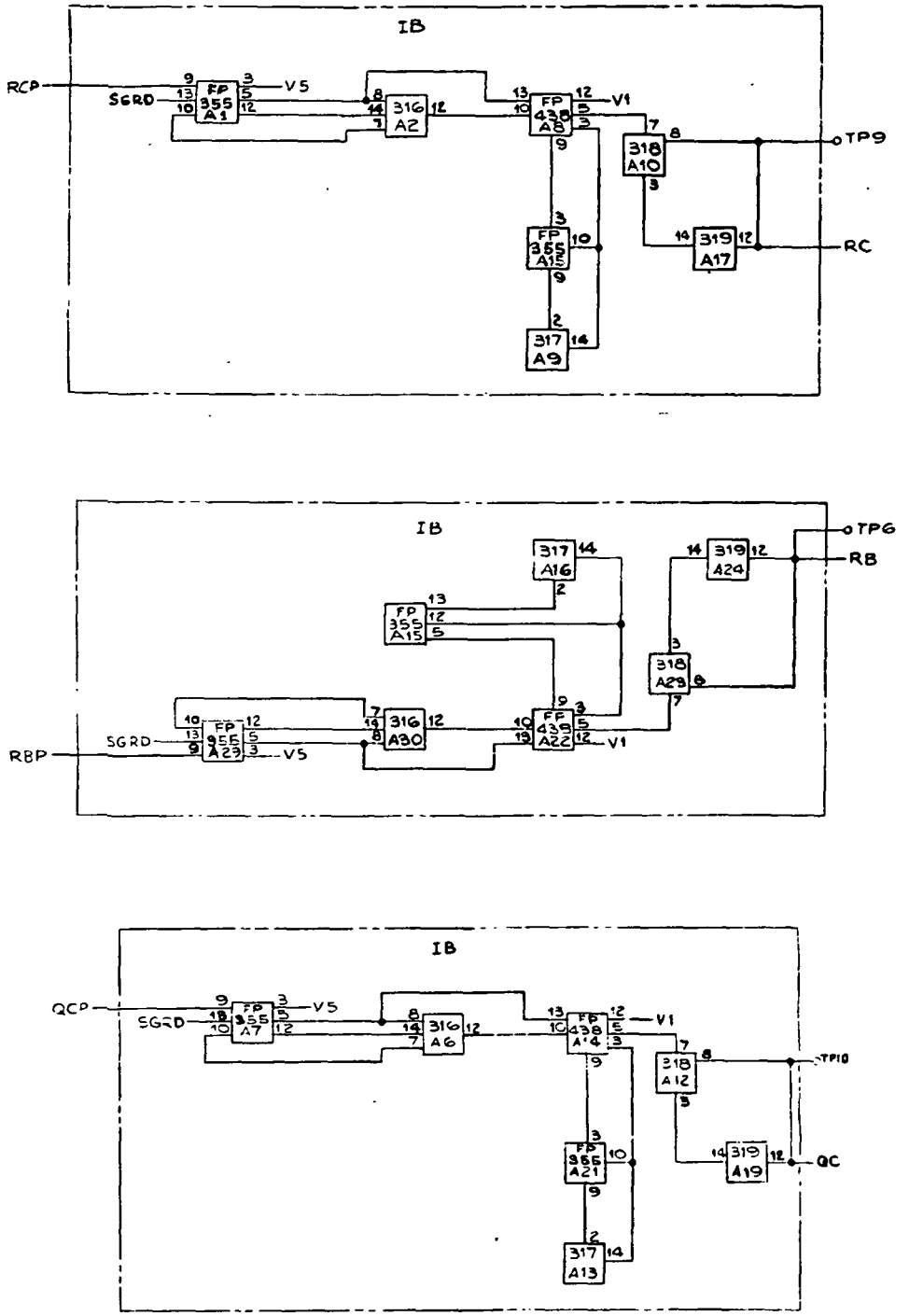
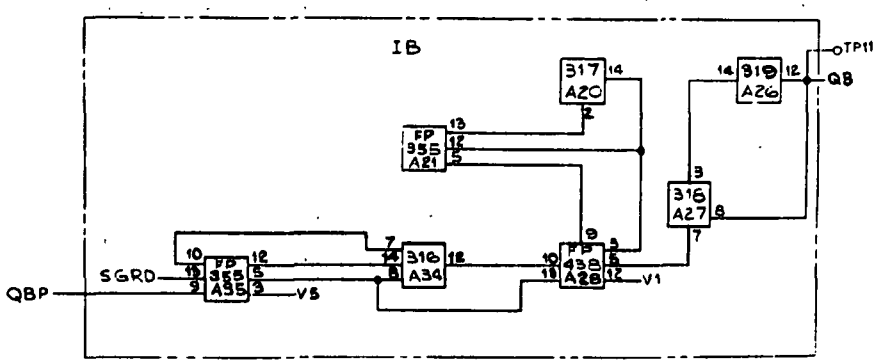


Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 1 of 8)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	QC
3		18	
4		19	
5		20	
6		21	QB
7		22	
8		23	
9		24	
10		25	RB
11		26	
12		27	
13		28	
14		29	RC
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4		54	
6		56	
8		58	
10		60	
12		62	
14		64	
16	QBP	66	
18	QCP	68	
20		70	V7
22		72	
24		74	
26		76	
28		78	
30		80	
32		82	V5
34		84	SGRD
36		86	
38		88	
40		90	
42		92	
44		94	RBP
46	V3	96	RCP
48	SIG RET	98	
50	V1		

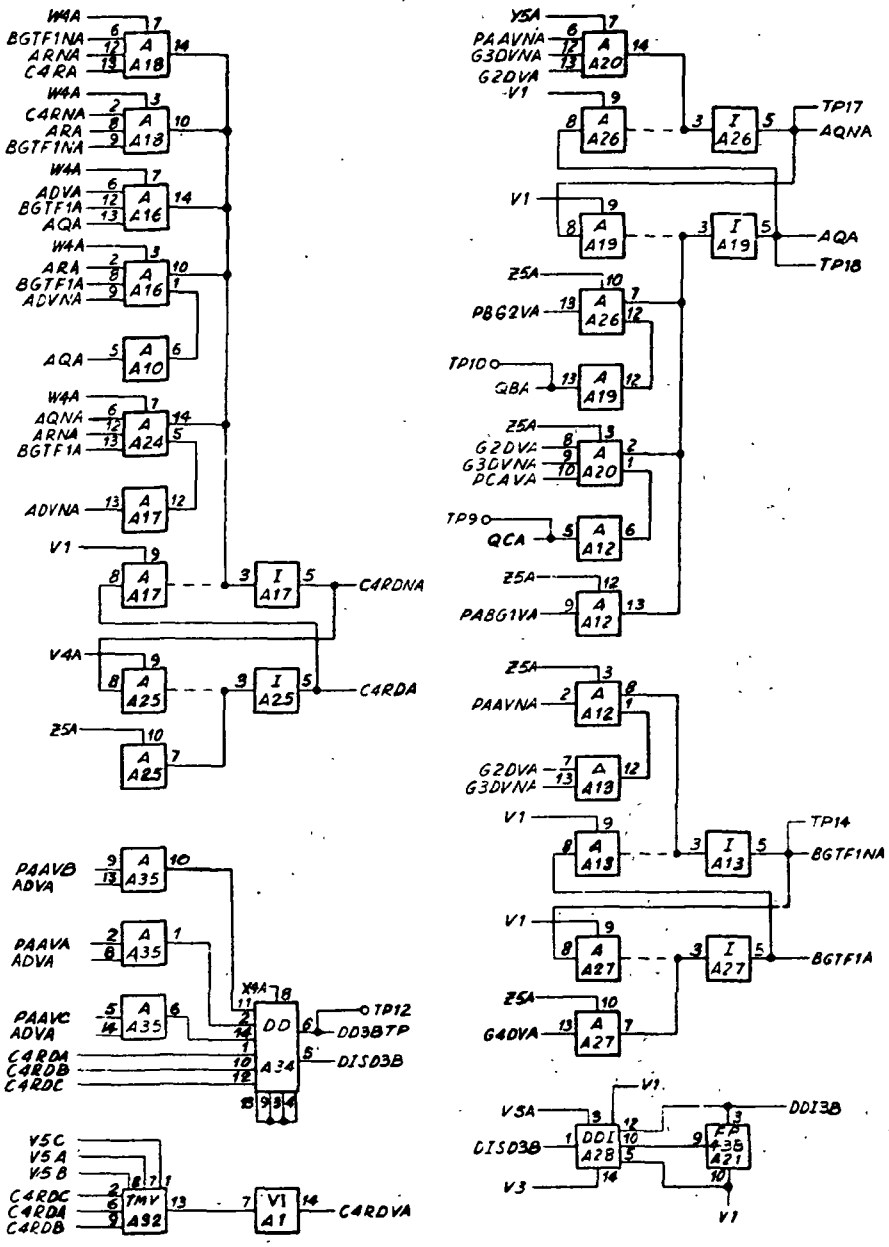
ULD LOCATIONS

A1 FP 355	A2 316	A3	A4	A5	A6 316	A7 FP 355
A8 FP 438	A9 317	A10 318	A11	A12 318	A13 317	A14 FP 438
A15 FP 355	A16 317	A17 319	A18	A19 319	A20 317	A21 FP 355
A22 FP 438	A23 318	A24 319	A25	A26 319	A27 318	A28 FP 438
A29 FP 355	A30 316	A31	A32	A33	A34 316	A35 FP 355

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A24 Side B, 2A4A25 Side B, 2A4A26 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112638-REL(66123BM)

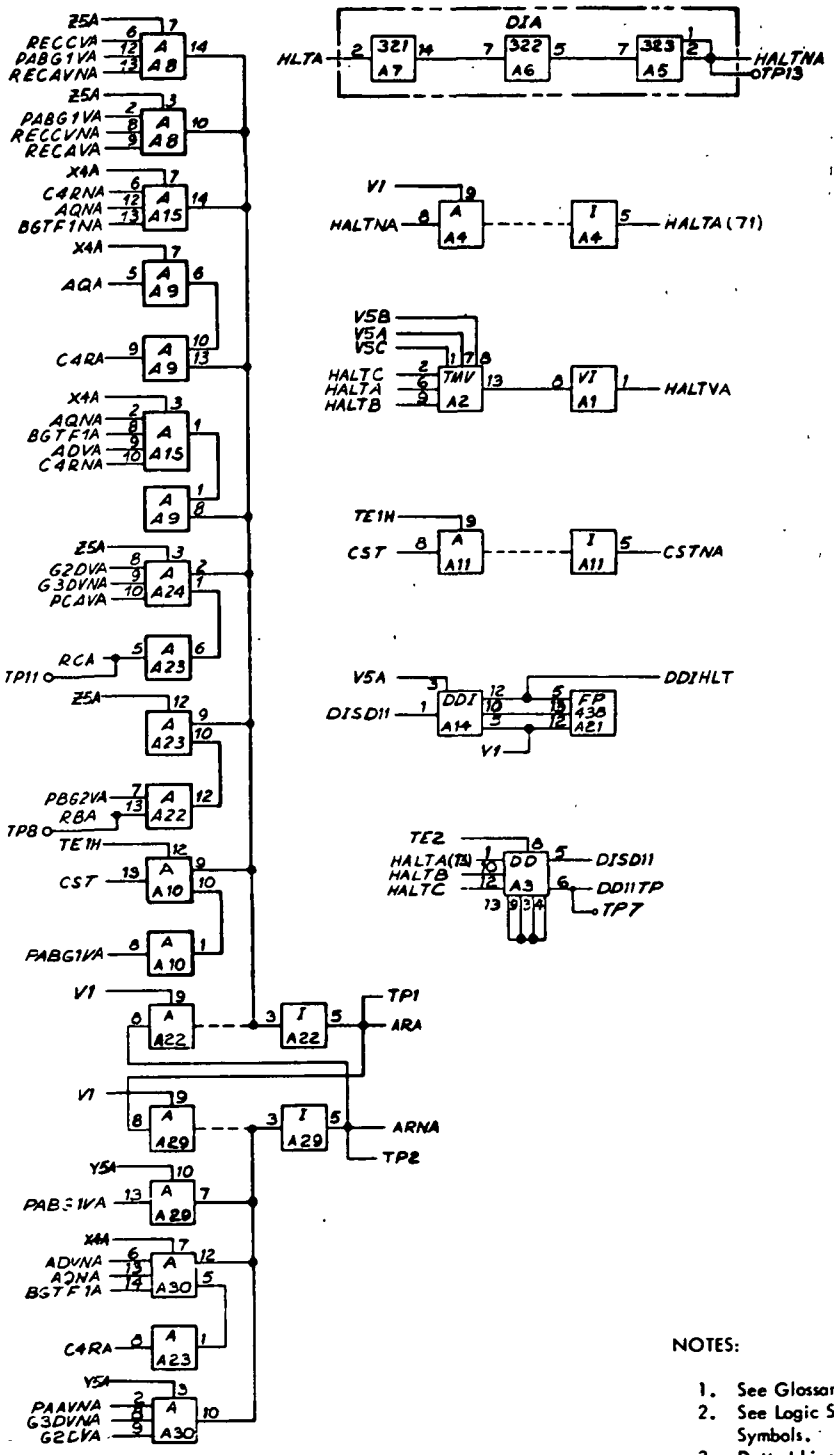
Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 2)



ULD LOCATIONS

A1 V1	A2 TMV	A3 DD	A4 I	A5 323	A6 322	A7 321
A8 AA	A9 AB	A10 AB	A11 I	A12 AB	A13 I	A14 DDI
A15 AA	A16 AA	A17 I	A18 AA	A19 I	A20 AA	A21 FP A38
A22 I	A23 AB	A24 AA	A25 I	A26 I	A27 I	A28 DDI
A29 I	A30 AA	A31	A32 TMV	A33	A34 DD	A35 AB

Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 3)



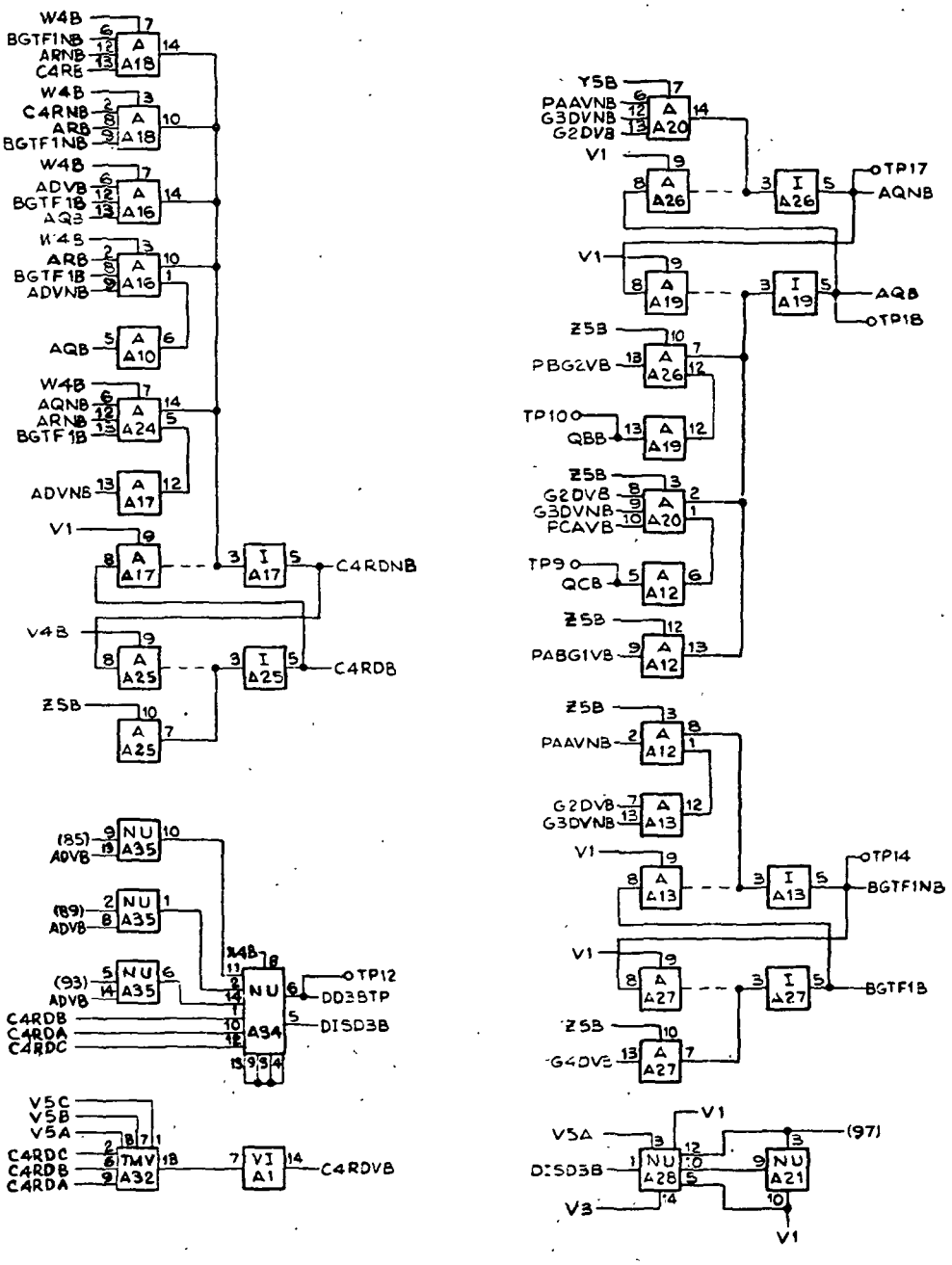
THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	QCA
3		18	
4		19	
5		20	
6		21	QBA
7		22	
8		23	
9		24	
10		25	RBA
11		26	
12		27	
13		28	
14		29	RCA
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	TE2	51	C4RDA
3	V3	53	CST
5	SIG-RET	55	V5A
7	Y5A	57	CSTNA
9	V1	59	V4A
11	TE1H	61	C4RDNA
13	X4A	63	HALTB
15	PAEG1VA	65	HALTC
17	HALTVA	67	G4DVA
19	G3DVNA	69	PBG2VA
21	RECAVA	71	HALTA
23	RECCVNA	73	HALTA
25	ADVA	75	C4RDB
27	C4RNA	77	C4RDC
29	C4RDVA	79	
31	C4RA	81	
33	PAAVNA	83	HLTA
35	G2DVA	85	PAAVB
37	RECCVA	87	W+A
39	ADVNA	89	PAAVA
41	PCAVA	91	Z5A
43	V5C	93	PAAVC
45	V5B	95	DDIHLT
47	RECAVVA	97	DDI3B
49	BGTF1A		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A24 Side A.
6. This Drawing Derived From IBM DWG NO. 6112618-A(66126BR)

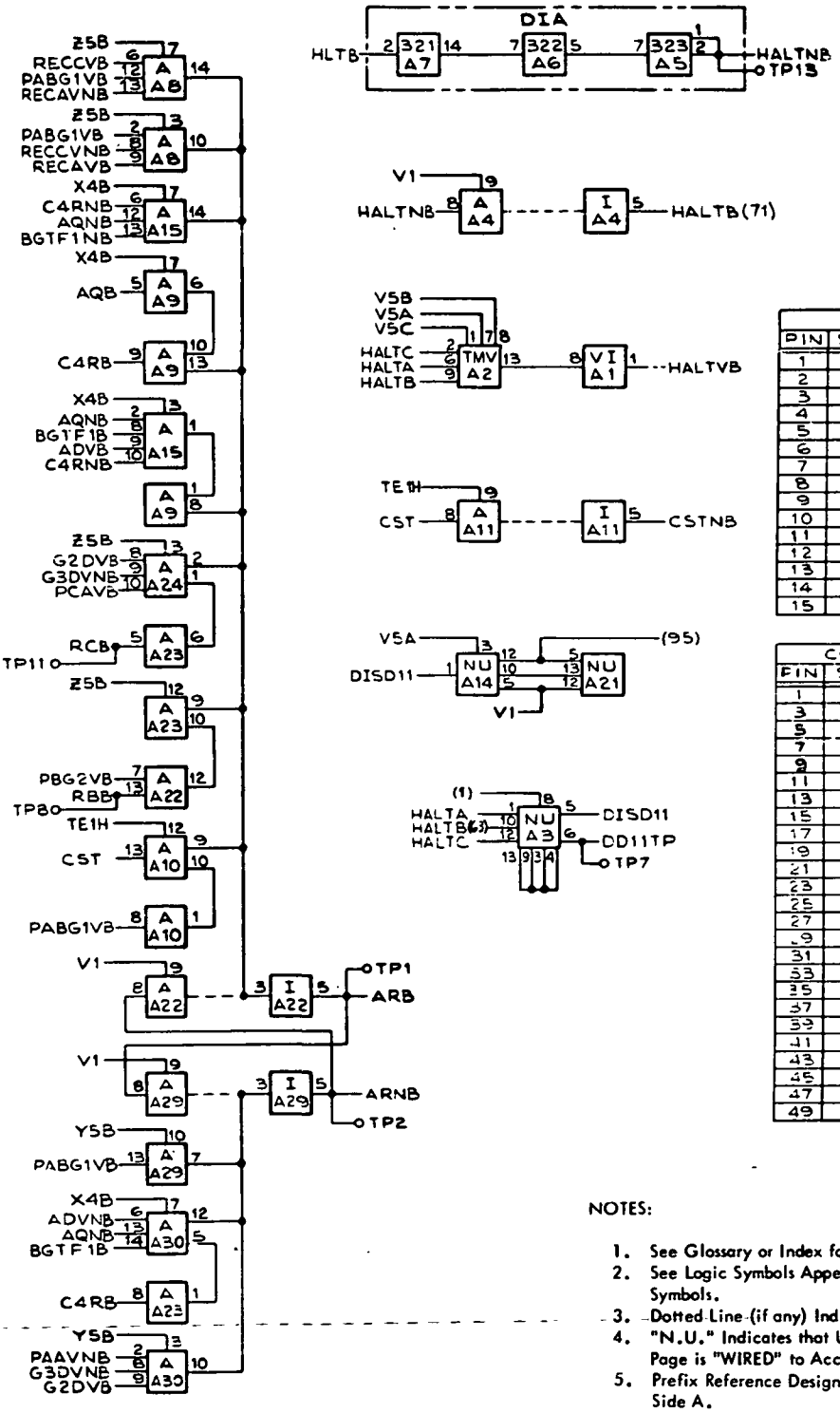
Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 4)



ULD LOCATIONS

A1 VI	A2 TMV	A3	A4 I	A5 323	A6 322	A7 321
A8 AA	A9 AB	A10 AB	A11 I	A12 AB	A13 I	A14
A15 AA	A16 AA	A17 I	A18 AA	A19 I	A20 AA	A21
A22 I	A23 AB	A24 AA	A25 I	A26 I	A27 I	A28
A29 I	A30 AA	A31	A32 TMV	A33	A34	A35

Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 5)



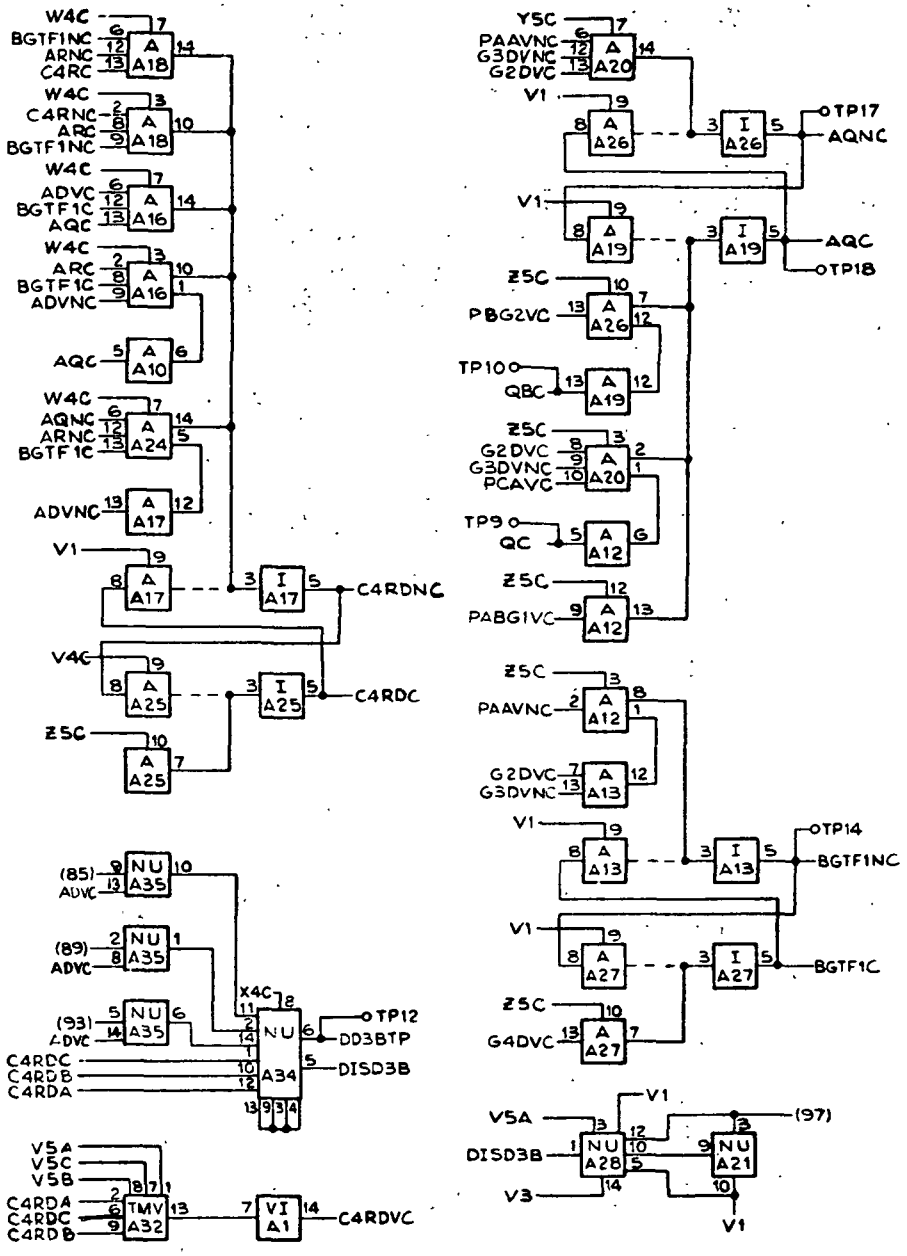
THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	QCB
3		18	
4		19	
5		20	
6		21	QBB
7		22	
8		23	
9		24	
10		25	RBB
11		26	
12		27	
13		28	
14		29	RCB
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1		51	C4RDB
3	V3	53	CST
5	SIG-RET	55	V5B
7	V5B	57	CSTNB
9	V1	59	V4B
11	TE1H	61	C4RDNB
13	V4B	63	HALTB
15	PABG1VB	65	HALTC
17	HALTVB	67	G4DVB
19	G3DVNB	69	PBG2VB
21	RECAVB	71	HALTB
23	RECCVNB	73	HALTA
25	ADVB	75	C4RDA
27	C4RNB	77	G4PDC
29	C4RDVB	79	
31	C4RB	81	
33	PAAVNB	83	HLTB
35	G2DVB	85	
37	RECCVB	87	WJB
39	ADVNB	89	
41	PCAVB	91	Z5B
43	V5C	93	
45	V5A	95	
47	RECAVNB	97	
49	BGTF1B		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A25 Side A.
6. This Drawing Derived From IBM DWG NO. 6112617-A(66126BR)

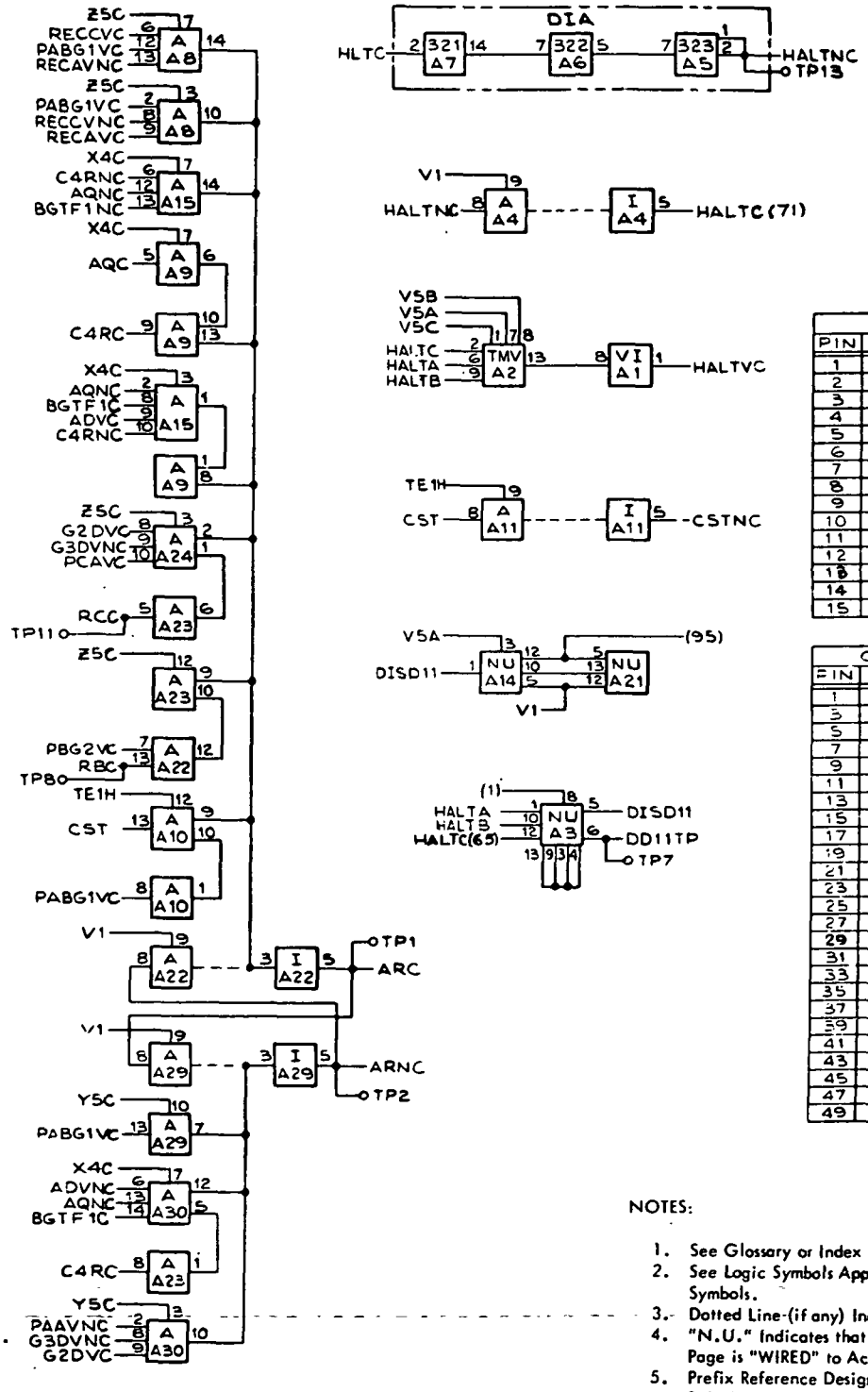
Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 6)



ULD LOCATIONS

A1 VI	A2 TMV	A3	A4 I	A5 323	A6 322	A7 321
A8 AA	A9 AB	A10 AB	A11 I	A12 AB	A13 I	A14
A15 AA	A16 AA	A17	A18 AA	A19 I	A20 AA	A21
A22 I	A23 AB	A24 AA	A25 I	A26 I	A27 I	A28
A29 I	A30 AA	A31	A32 TMV	A33	A34	A35

Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 7)



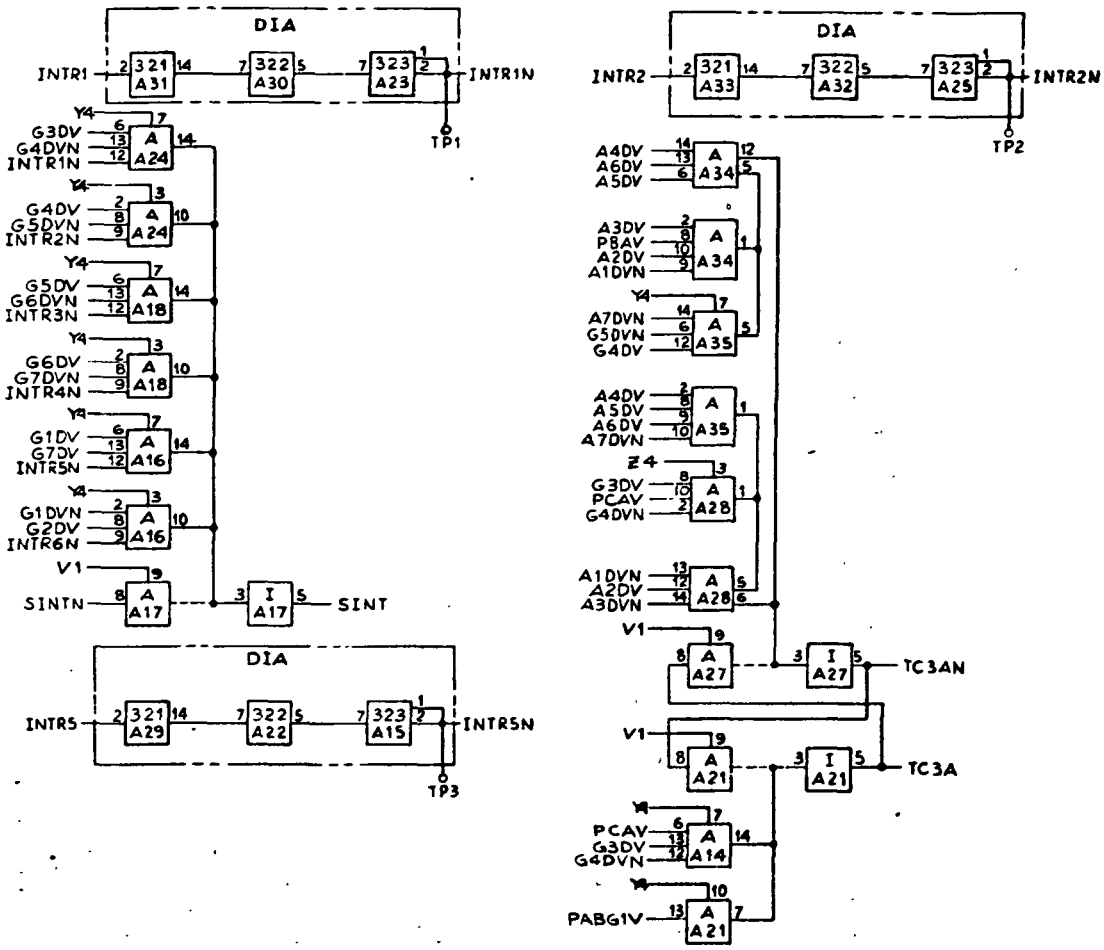
THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	QCC
3		18	
4		19	
5		20	
6		21	QBC
7		22	
8		23	
9		24	
10		25	RBC
11		26	
12		27	
13		28	
14		29	RCC
15		30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1		51	C4RDC
3	V3	53	CST
5	SIG-RET	55	V5C
7	Y5C	57	CSTNC
9	V1	59	V4C
11	TE1H	61	C4RDNC
13	X4C	63	HALTB
15	PAEG1VC	65	HALTC
17	HALTVC	67	G4DVC
19	G3DVNC	69	PBG2VC
21	RECAVC	71	HALTC
23	RECCVNC	73	HALTA
25	ADVC	75	C4RDB
27	C4RNC	77	C4RDA
29	C4RDVC	79	
31	C4RC	81	
33	PAAVNC	83	HLTC
35	G2DVC	85	
37	RECCVC	87	W4C
39	ADVNC	89	
41	PCAVC	91	Z5C
43	V5A	93	
45	V5B	95	
47	RECAVNC	97	
49	BGTF1C		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line-(if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A26 Side A.
6. This Drawing Derived From IBM DWG NO. 6112619-A(66126BR)

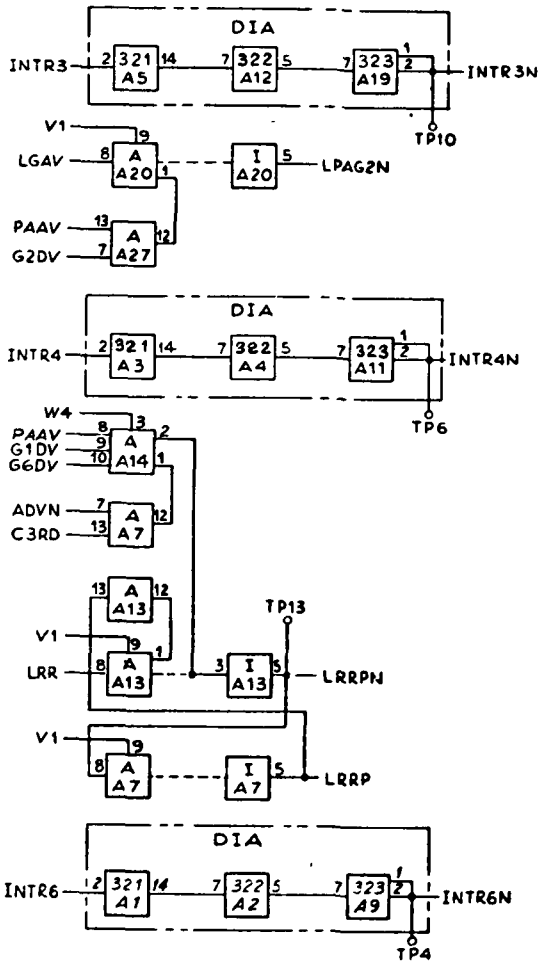
Figure 10-18. Accelerometer Processor Logic Diagram (Sheet 8)



ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
321	322	321	322	321		I
A8	A9	A10	A11	A12	A13	A14
	323		323	322	I	AA
A15	A16	A17	A18	A19	A20	A21
323	AA	I	AA	323	I	I
A22	A23	A24	A25	A26	A27	A28
322	323	AA	323		I	AA
A29	A30	A31	A32	A33	A34	A35
321	322	321	322	321	AA	AA

Figure 10-19. Interrupt Processor Logic Diagram (Sheet 1 of 10)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	G6DVN
2	PCAV	17	G4DVN
3		18	G5DVN
4		19	G5DV
5		20	G6DV
6		21	SINT
7		22	SINTN
8		23	G4DV
9		24	
10		25	G7DVN
11		26	G7DV
12		27	Z4
13		28	G1DVN
14		29	PABG1V
15	G3DV	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	A3DVN	52	
4	A7DVN	54	G7DVN
6	A1DVN	56	G6DVN
8	A6DV	58	LRRP
10	G5DVN	60	LRR
12	A4DV	62	
14	A5DV	64	SINTA
16	A3DV	66	INTR1
18	PAAV	68	G4DV
20	PBAV	70	G7DV
22	G3DV	72	ADVN
24	LGAV	74	C3RD
26	G1DV	76	G1DVN
28	G4DVN	78	V3
30	G5DV	80	SIG-RET
32	PCAV	82	G2DV
34		84	INTR3
36		86	V1
38	A2DV	88	W4
40	TC3A	90	INTR5
42	INTR2	92	Y4
44	PABG1V	94	
46	G6DV	96	INTR6
48	TC3AN	98	INTR4
50	LPA62N		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A18 Side B, 2A4A17 Side B, 2A4A16 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112588-A(66126EJ)

Figure 10-19. Interrupt Processor Logic Diagram (Sheet 2)

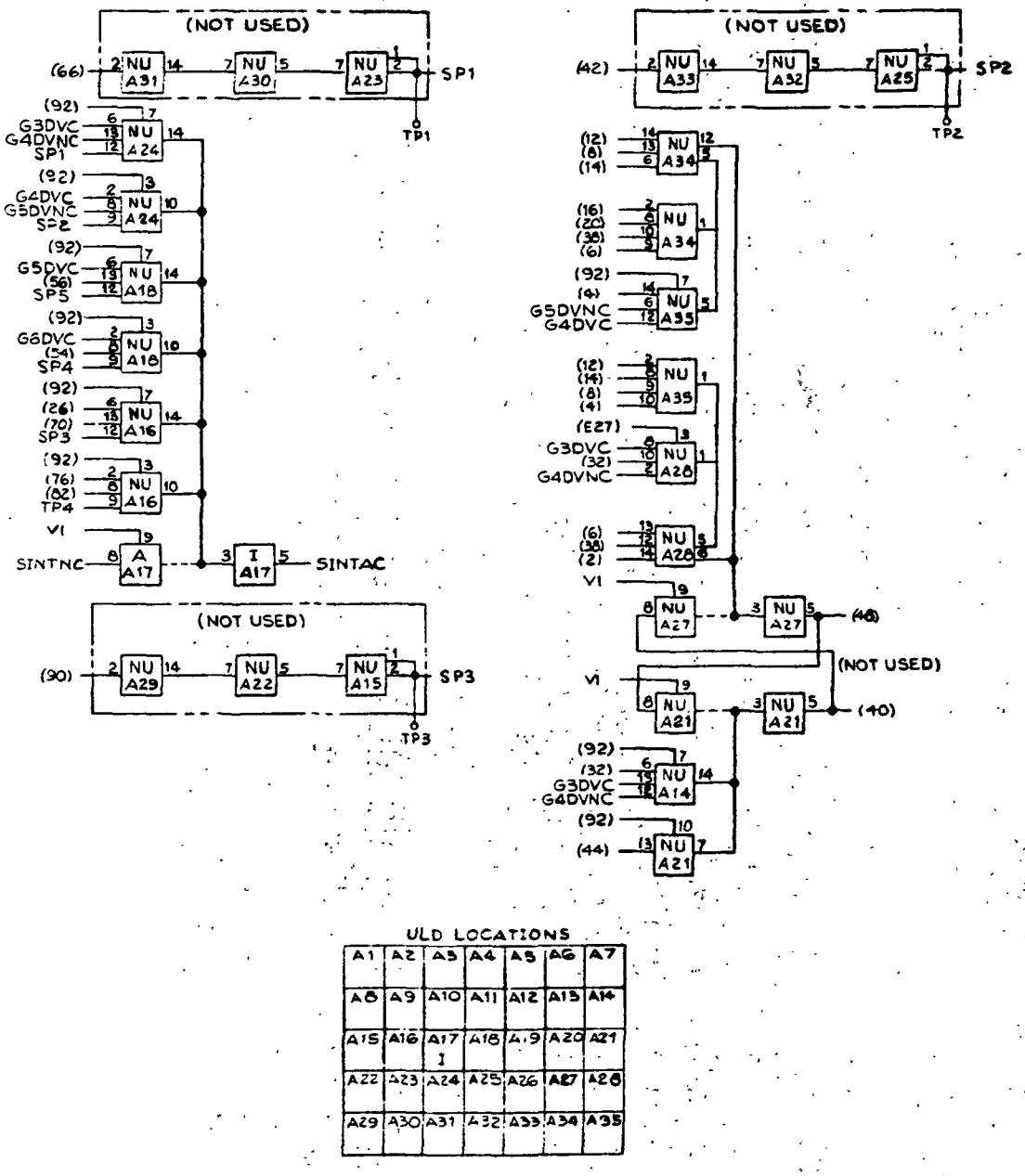
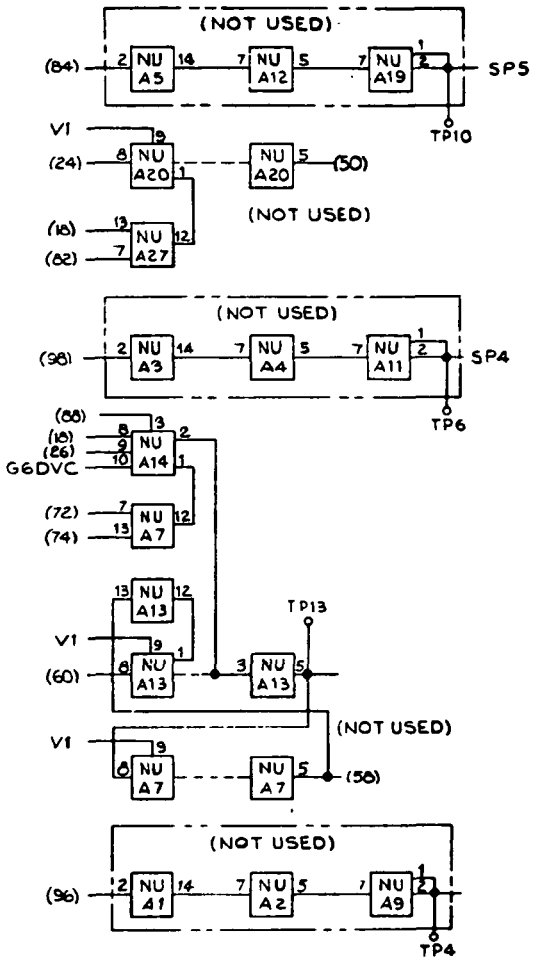


Figure 10-19. Interrupt Processor Logic Diagram (Sheet 3)



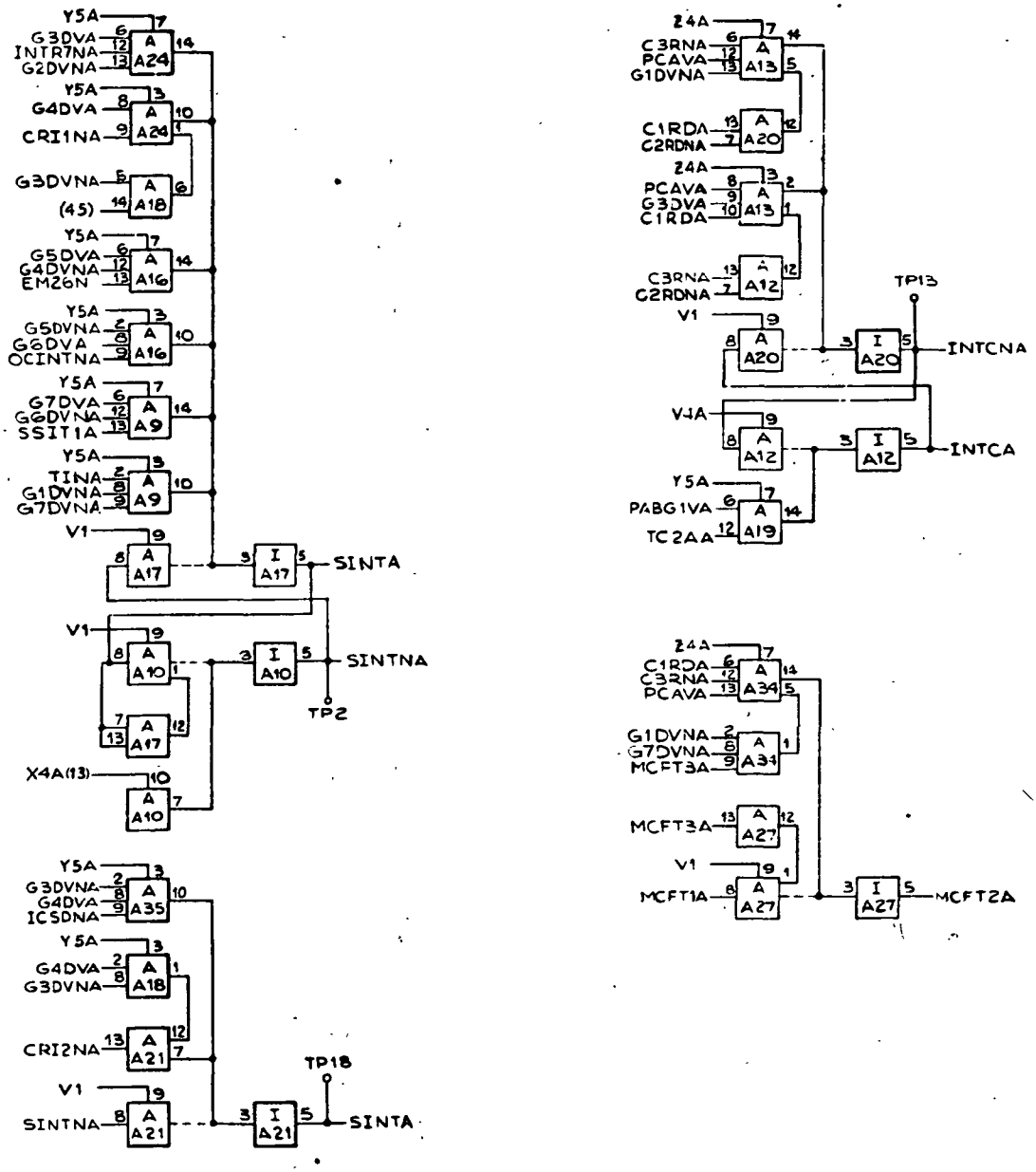
THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	(56)
2	(32)	17	G4DVNC
3		18	G5DVNC
4		19	G5DVC
5		20	G6DVC
6		21	SINTAC
7		22	SINTNC
8		23	G4DVC
9		24	
10		25	(54)
11		26	(70)
12		27	
13		28	(76)
14		29	(44)
15	G3DVC	30	(26)

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	
4		54	
6		56	
8		58	
10	G5DVNC	60	
12		62	
14		64	SINTAC
16		66	
18		68	G4DVC
20		70	
22	G3DVC	72	
24		74	
26		76	
28	G4DVNC	78	V3
30	G5DVC	80	SIG-RET
32		82	
34		84	
36		86	V1
38		88	
40		90	
42		92	
44		94	
46	G6DVC	96	
48		98	
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A16 Side B.
6. This Drawing Derived From IBM DWG NO. 6112719-REL(66123KL)

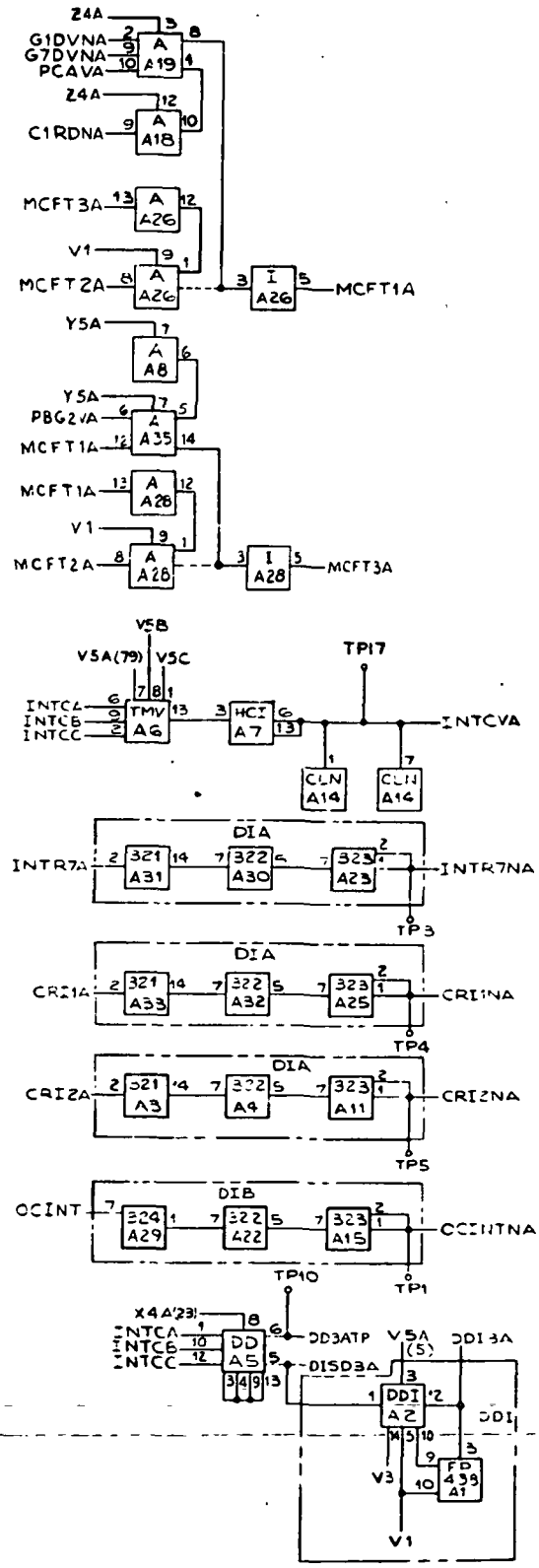
Figure 10-19. Interrupt Processor Logic Diagram (Sheet 4)



ULD LOCATIONS

A1 FP 438	A2 DDI	A3 321	A4 322	A5 DD	A6 TMV	A7 HCI
A8 AB	A9 AA	A10 I	A11 323	A12 I	A13 AA	A14 CLN
A15 323	A16 AA	A17 I	A18 AB	A19 AA	A20 I	A21 I
A22 322	A23 323	A24 AA	A25 323	A26 I	A27 I	A28 I
A29 324	A30 322	A31 321	A32 322	A33 321	A34 AA	A35 AA

Figure 10-19. Interrupt Processor Logic Diagram (Sheet 5)



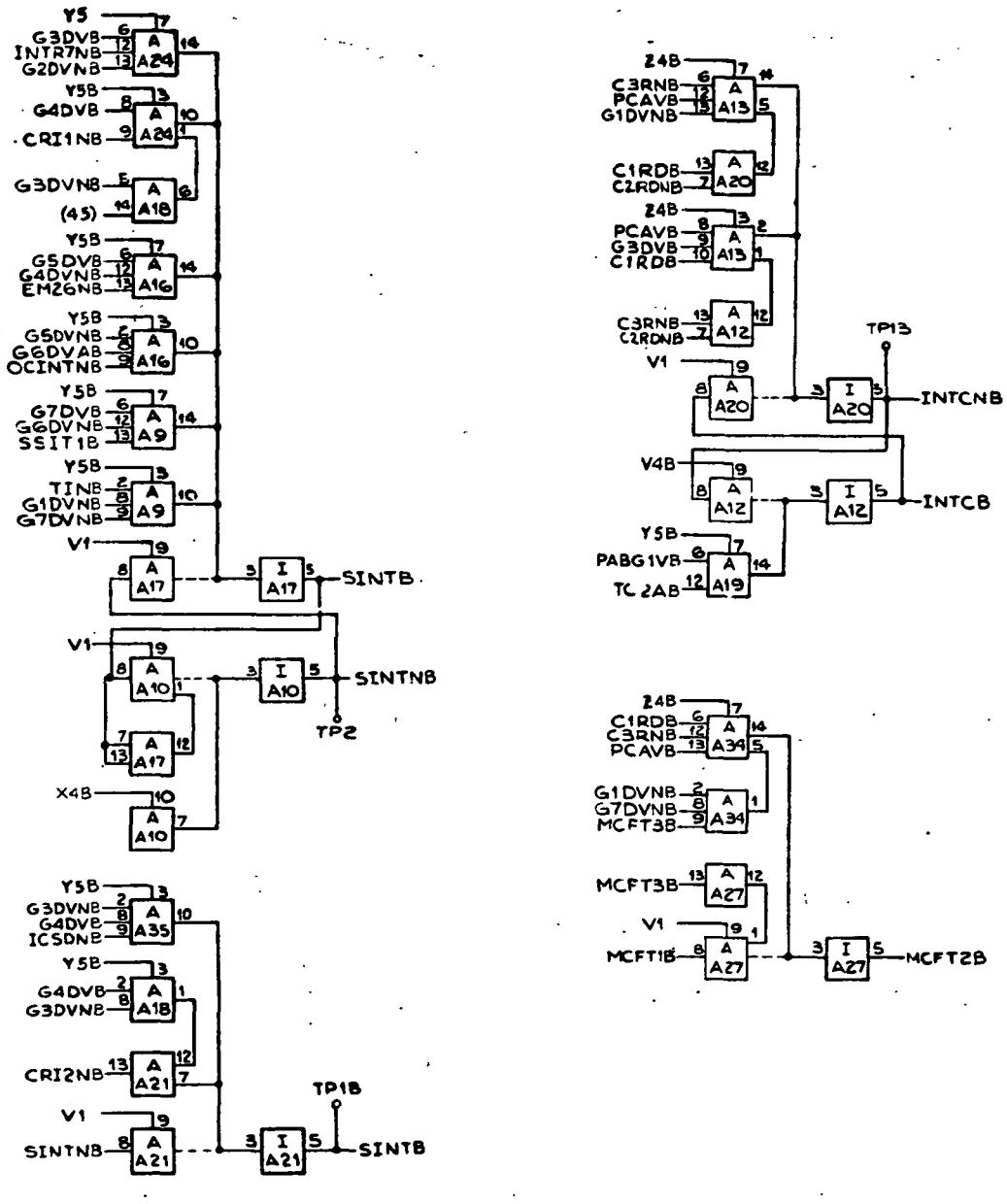
THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	G6DVNA
2	PCAVA	17	G4DVNA
3		18	G5DVNA
4		19	G5DVA
5		20	G6DVA
6		21	SINTA
7		22	SINTNA
8		23	G4DVA
9		24	Y4A
10		25	G7DVNA
11		26	G7DVA
12		27	Z4A
13		28	G1DVNA
14		29	PABG1VA
15	G3DVA	30	

CONNECTOR-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	INTCB
3	SIG-RET	53	INTCA
5	V5A	55	V4A
7	Y5A	57	
9	OCINT	59	INTCC
11	V20	61	CRI1A
13	X4A	63	MCFT3A
15	DDI3A	65	TC2AA
17	TINA	67	MCFT2A
19	G3DVNA	69	PBG2VA
21	V1	71	DISD3A
23	X4A	73	V5C
25	EM26N	75	V5B
27	SSIT1A	77	C3RNA
29	G2DV1IA	79	V5A
31	CRI2A	81	C1RDA
33	INTR7A	83	ICSDNA
35		85	
37		87	
39		89	MCFT1A
41	SIINTA	91	Z4A
43	C1RDNA	93	C2RDNA
45		95	Y4A
47		97	INTCVA
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A18 Side A.
6. This Drawing Derived From IBM DWG NO. 6112578-A(66123NT)

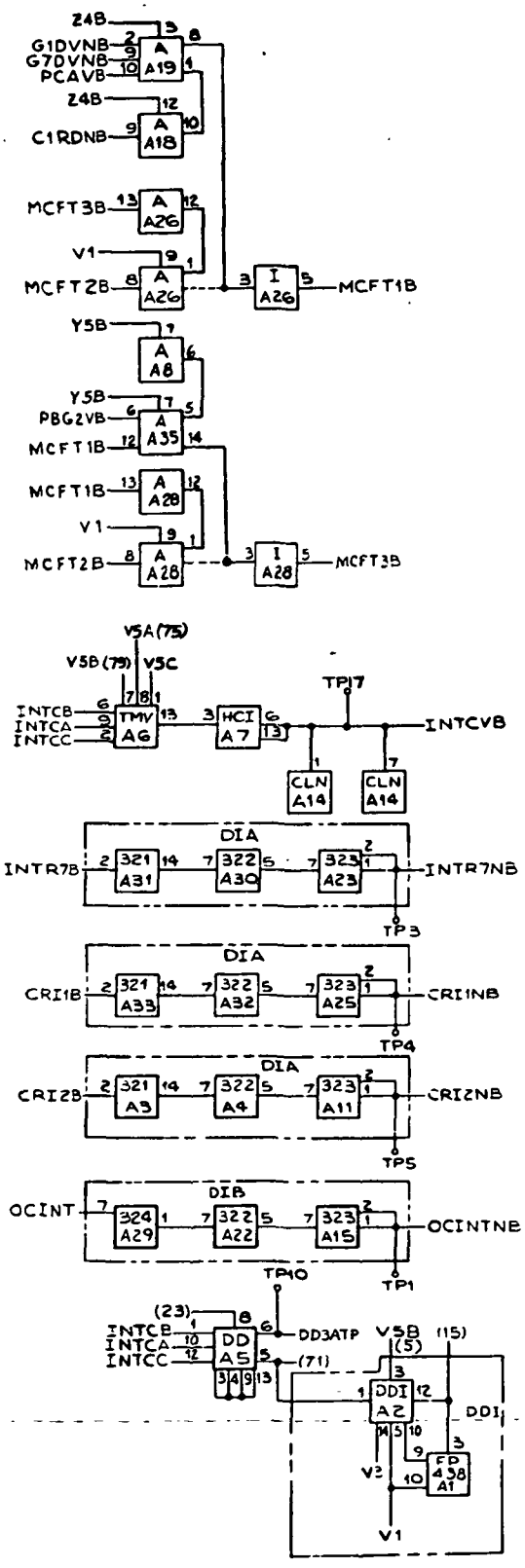
Figure 10-19. Interrupt Processor Logic Diagram (Sheet 6)



ULD LOCATIONS

A1 FP 438	A2 DDI	A3 321	A4 322	A5 DD	A6 TMV	A7 HCI
A8 AB	A9 AA	A10 I	A11 323	A12 I	A13 AA	A14 CLN
A15 323	A16 AA	A17 I	A18 AB	A19 AA	A20 I	A21 I
A22 322	A23 323	A24 AA	A25 323	A26 I	A27 I	A28 I
A29 324	A30 322	A31 321	A32 322	A33 321	A34 AA	A35 AA

Figure 10-19. Interrupt Processor Logic Diagram (Sheet 7)



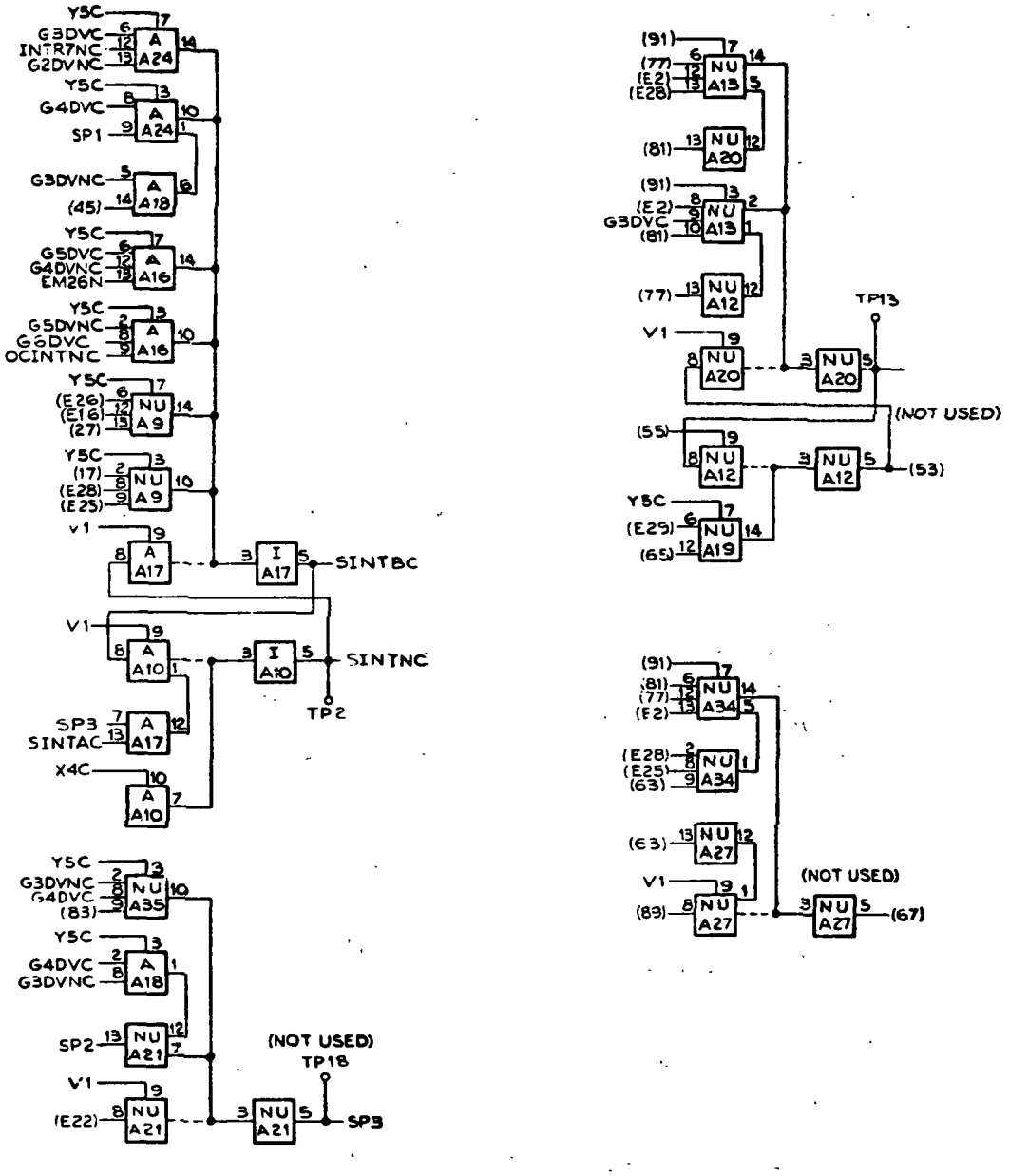
THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	G6DVNB
2	PCAVB	17	G4DVNB
3		18	G5DVNB
4		19	G5DVB
5		20	G6DVB
6		21	SINTB
7		22	SINTNB
8		23	G4DVB
9		24	Y4B
10		25	G7DVNB
11		26	G7DVB
12		27	Z4B
13		28	G1DVNB
14		29	PABG1VB
15	G3DVB	30	

CONNECTOR-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	INTCA
3	SIG-RET	53	INTCB
5	V5B	55	V4B
7	Y5B	57	
9	OCINT	59	INTCC
11	V2O	61	CRI1B
13	X4B	63	MCFT3B
15		65	TC2AB
17	TINB	67	MCFT2B
19	G3DVNB	69	PBG2VB
21	V1	71	
23		73	V5C
25	EM26N	75	V5A
27	SSIT1B	77	C3RNB
29	G2DVNB	79	V5E
31	CRI2B	81	C1RDB
33	INTR7B	83	ICSDNB
35		85	
37		87	
39		89	MCFT1B
41	SINTB	91	Z4B
43	C1RDNB	93	C2RDNB
45		95	Y4B
47		97	INTCVB
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A17 Side A.
6. This Drawing Derived From IBM DWG NO. 6112577-A(66123NT)

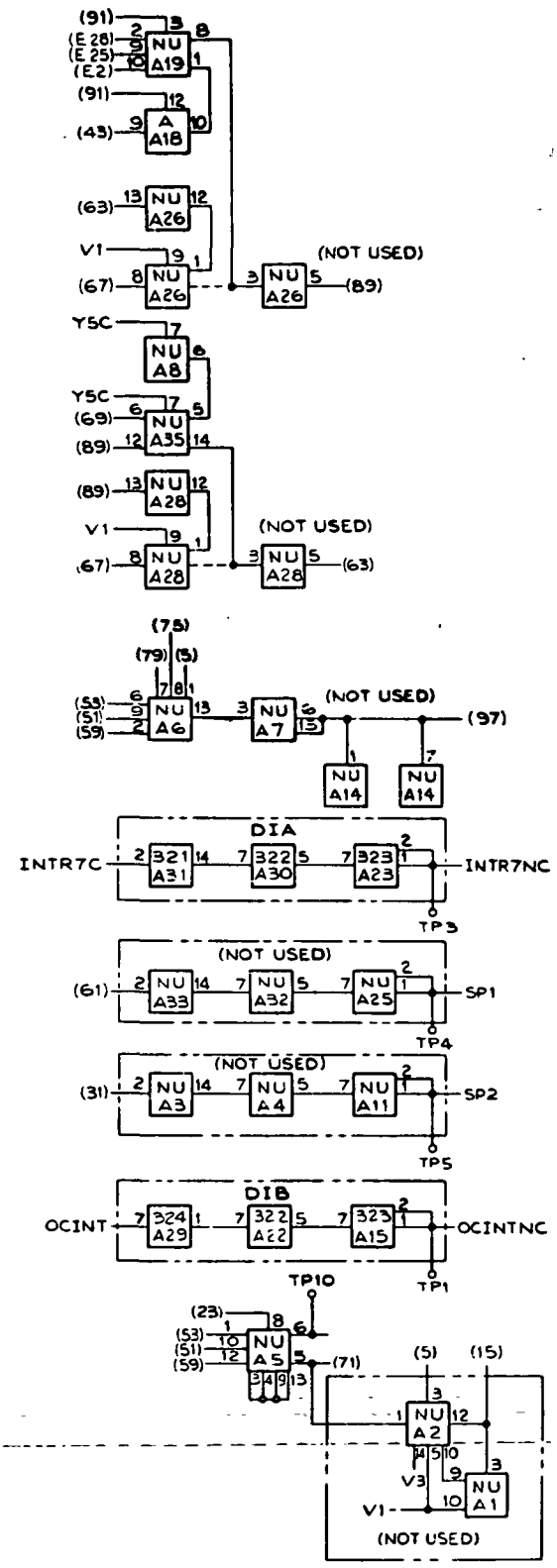
Figure 10-19. Interrupt Processor Logic Diagram (Sheet 8)



ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9	A10 I	A11	A12	A13	A14
A15 323	A16 AA	A17 I	A18 AB	A19	A20	A21
A22 322	A23 323	A24 AA	A25	A26	A27	A28
A29 324	A30 322	A31 321	A32	A33	A34	A35

Figure 10-19. Interrupt Processor Logic Diagram (Sheet 9)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2		17	G4DVNC
3		18	G5DVNC
4		19	G5DVC
5		20	G6DVC
6		21	SINTAC
7		22	SINTNC
8		23	G4DVC
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	
15	G3DVC	30	

CONNECTOR-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5	51	
3	SIG-RET	53	
5		55	
7	Y5C	57	
9	OCINT	59	
11	V20	61	
13	X4C	63	
15		65	
17		67	
19	G3DVNC	69	
21	V1	71	
23		73	
25	EM26N	75	
27		77	
29	G2DVNC	79	
31		81	
33	INTR7C	83	
35		85	
37		87	
39		89	
41	SINTBC	91	
43		93	
45		95	
47		97	
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A16 Side A,
6. This Drawing Derived From IBM DWG NO. 6112739-REL(66123KL)

Figure 10-19. Interrupt Processor Logic Diagram (Sheet 10)

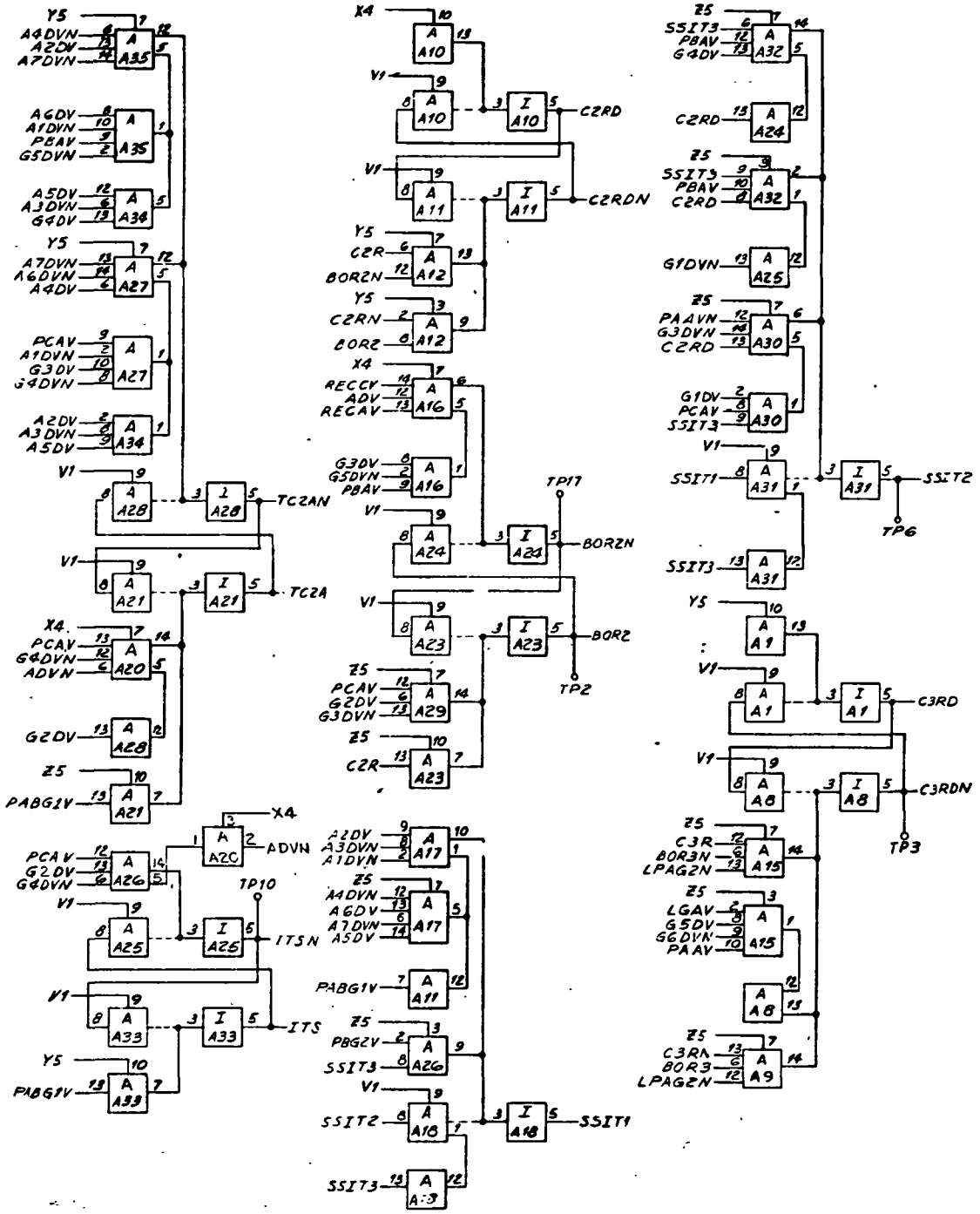
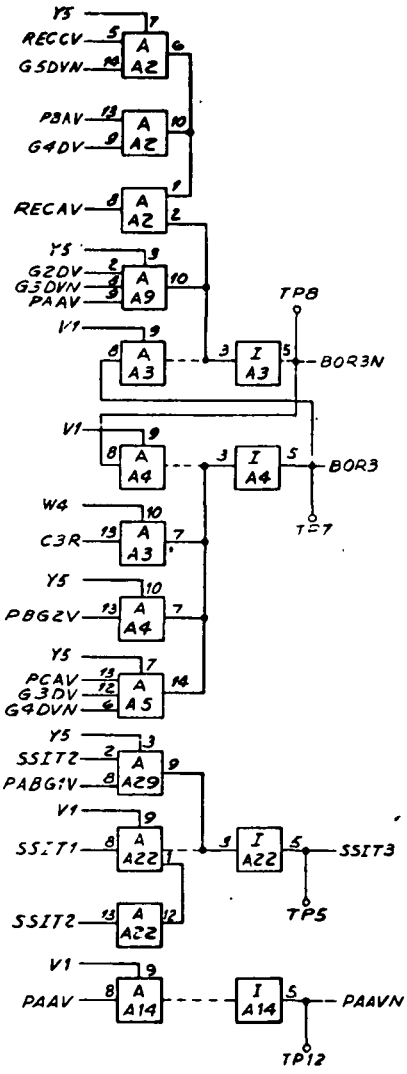
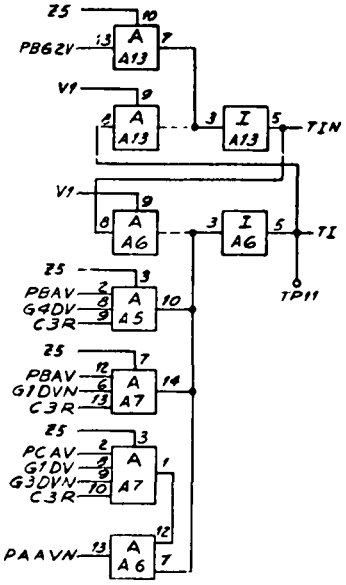


Figure 10-20. Countdown Processors Logic Diagram (Sheet 1 of 4)





CONNECTOR P1115			
PIN	SIGNAL	PIN	SIGNAL
1	A3DVN	51	A6DV
3	A7DVN	53	ADVN
5	G6DVN	55	C3RN
7	PAAV	57	C2RN
9	Y5	59	PBG2V
11	X4	61	G4DVN
13	C3R	63	ITS
15	G2DV	65	C2RDN
17	LPAG2N	67	TIN
19	PCAV	69	C3RD
21	SSIT1	71	W4
23	A6LVN	73	A5DV
25	G1DV	75	G4DV
27	G3DVN	77	V1
29	G5DV	79	PBAV
31	LGAV	81	RECCV
33	A2DV	83	V3
35	A1DVN	85	C2R
37	ADV	87	SIG-RET
39	RECAV	89	G1DVN
41	G5DVN	91	Z5
43	PABG1V	93	A4DVN
45	G3DV	95	TCZA
47	C2RD	97	TCZAN
49	A6DV		

ULD LOCATIONS

A1 I	A2 AB	A3 I	A4 I	A5 AA	A6 I	A7 AA
A8 I	A9 AA	A10 I	A11 I	A12 AA	A13 I	A14 I
A15 AA	A16 AA	A17 AA	A18 I	A19	A20 AA	A21 I
A22 -	A23 I	A24 I	A25 -	A26 AA	A27 AA	A28 I
A29 AA	A30 AA	A31 -	A32 AA	A33 I	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A5 Side A, 2A4A6 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112518-A(66123LM)

Figure 10-20. Countdown Processors Logic Diagram (Sheet 2)

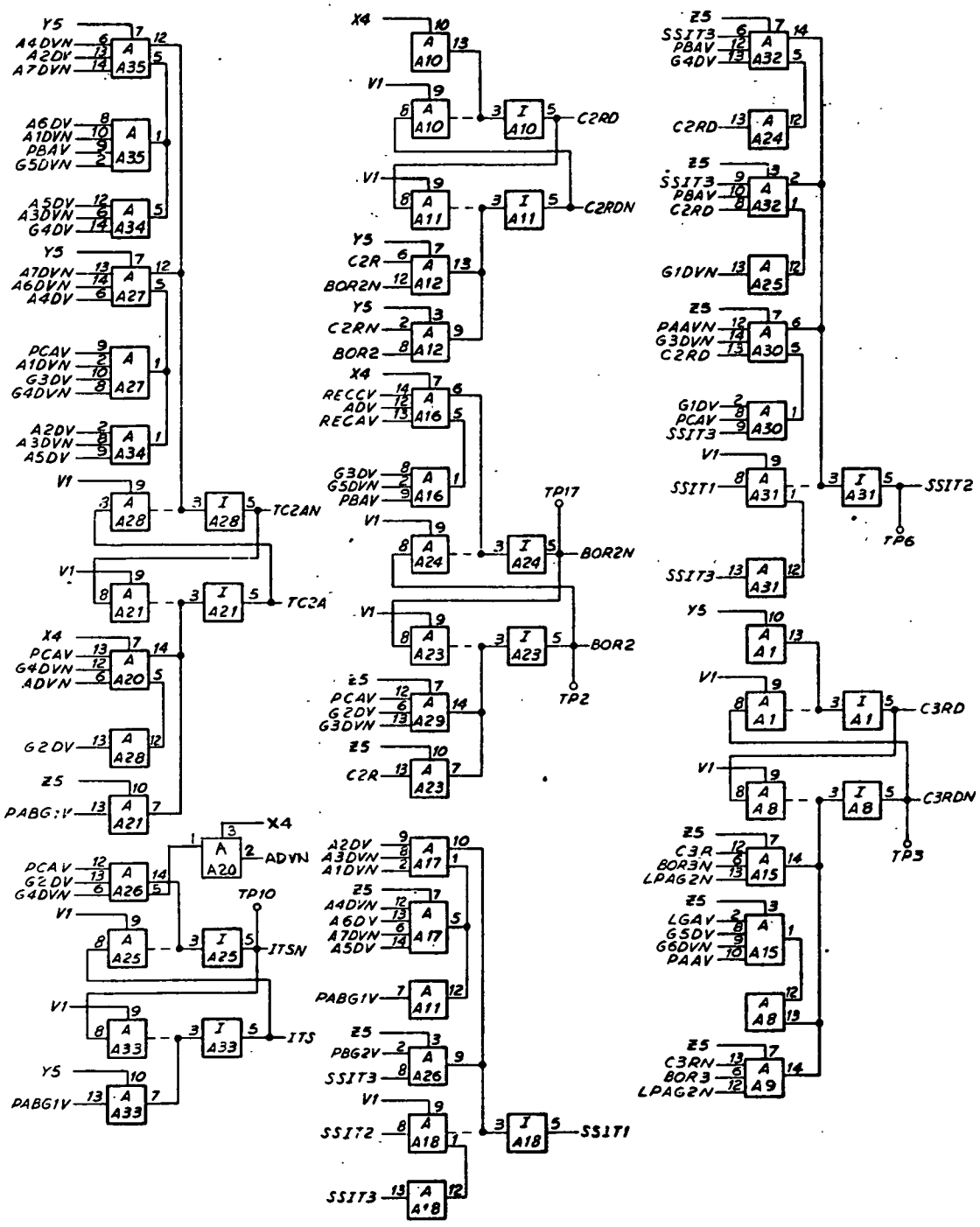
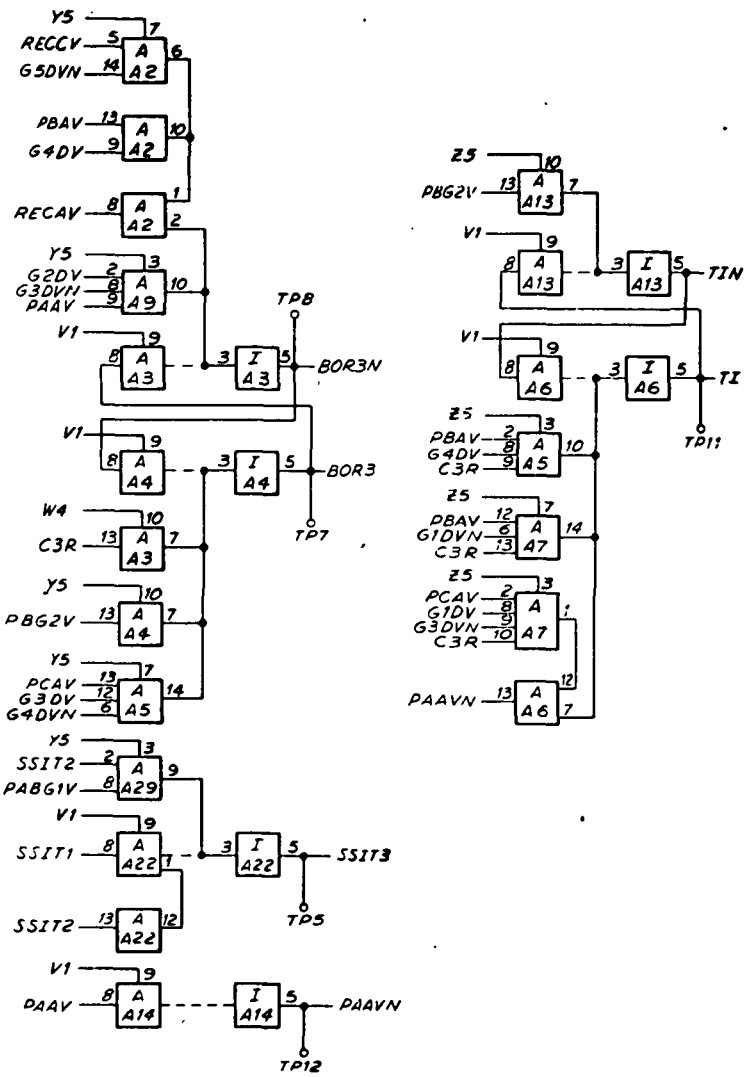


Figure 10-20. Countdown Processors Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	TC2AN	52	C2RD
4	TC2A	54	G3DV
6	A4DVN	56	PABG1V
8	Z5	58	G5DVN
10	G1DVN	60	RECAV
12	SIG-RET	62	ADV
14	C2R	64	A1DVN
16	V3	66	A2DV
18	RECCV	68	LG4V
20	PBAV	70	G5DV
22	V1	72	G3DVN
24	G4DV	74	G1DV
26	A5DV	76	A6DVN
28	W4	78	SSIT1
30	C3RD	80	PCAV
32	TIN	82	LPAG2N
34	C2RDN	84	G2DV
36	TTS	86	C3R
38	G4DVN	88	X4
40	PBG2V	90	Y5
42	C2RN	92	PAAV
44	C3RN	94	G6DVN
46	ADVN	96	A7DVN
48	A4DV	98	A3DVN
50	A6DV		

ULD LOCATIONS

A1 I	A2 AB	A3 I	A4 I	A5 AA	A6 I	A7 AA
A8 I	A9 AA	A10 I	A11 I	A12 AA	A13 I	A14 I
A15 AA	A16 AA	A17 AA	A18 I	A19	A20 AA	A21 I
A22 I	A23 I	A24 I	A25 I	A26 AA	A27 AA	A28 I
A29 AA	A30 AA	A31 I	A32 AA	A33 I	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A5 Side B.
6. This Drawing Derived From IBM DWG NO. 6112519-A(66123LM)

Figure 10-20. Countdown Processors Logic Diagram (Sheet 4)

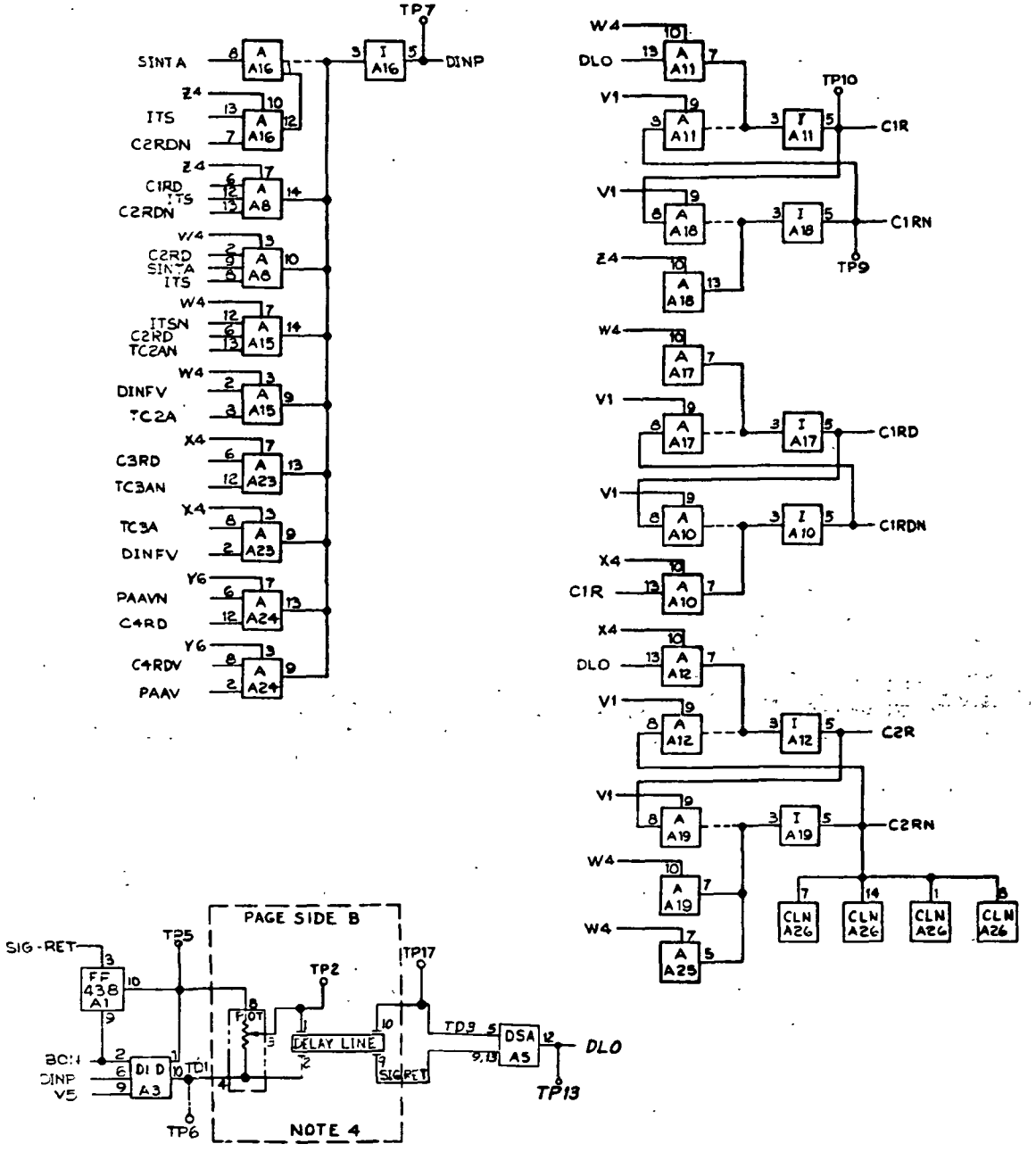
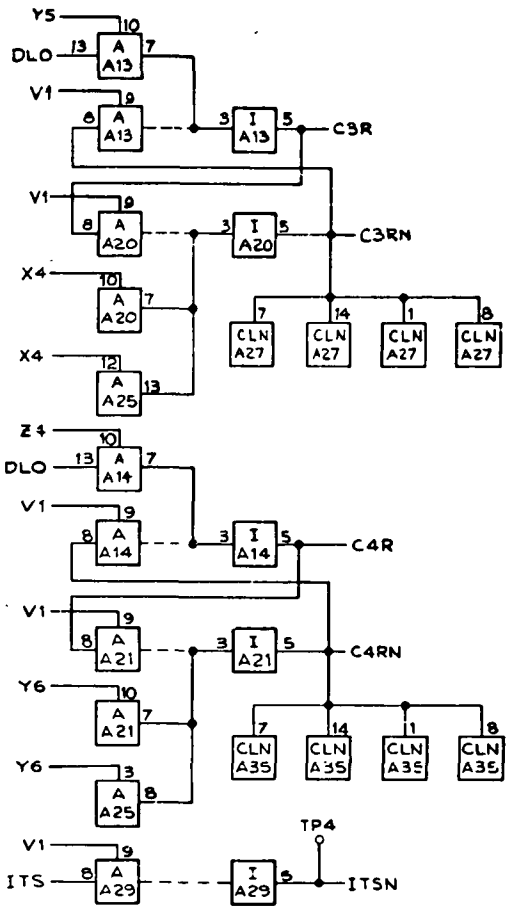


Figure 10-21. Processor Storage Logic Diagram (Sheet 1 of 2)



CONNECTOR-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	BON	51	
3	V1	53	C1RDN
5	V3	55	C3RN
7	Y6	57	C2RN
9	SIG-RET	59	
11	DINFV	61	SINTA
13	X4	63	ITS
15	C3R	65	C2RDN
17		67	
19	PAAV	69	
21		71	
23		73	C3RD
25		75	
27		77	
29	C4RDV	79	V5
31		81	C1RD
33		83	C4RN
35	PAAVN	85	C2R
37		87	W4
39	TC3A	89	C4R
41	C4RD	91	Z4
43		93	Y5
45	TC3AN	95	TC2A
47	C2RD	97	TC2AN
49			

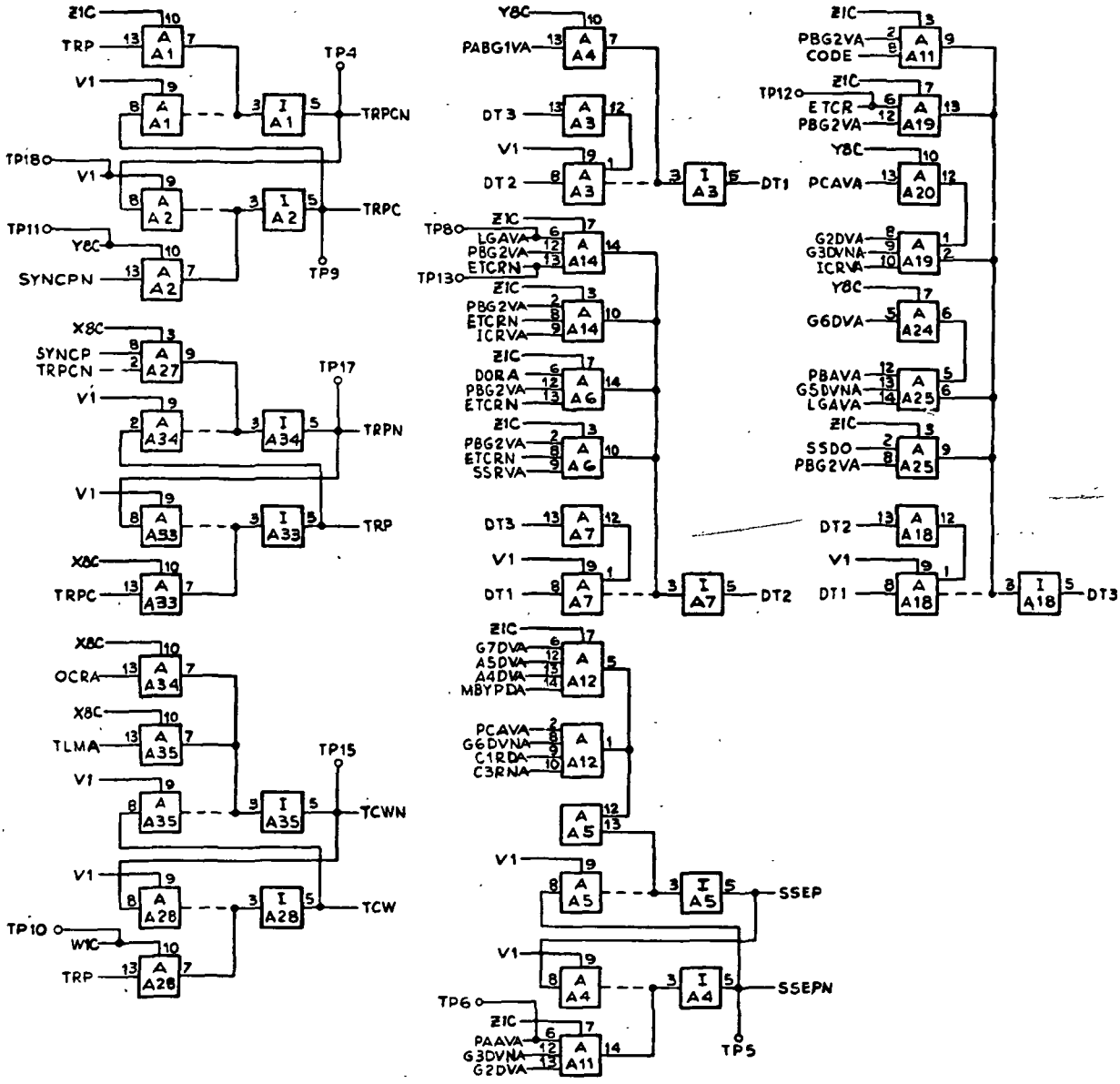
ULD LOCATIONS

A1 FP 438	A2	A3 DLD	A4	A5 DSA	A6	A7
A8 AA	A9	A10 I	A11 I	A12 I	A13 I	A14 I
A15 AA	A16 I	A17 I	A18 I	A19 I	A20 I	A21 I
A22	A23 AA	A24 AA	A25 AB	A26 CLN	A27 CLN	A28
A29 I	A30	A31	A32	A33	A34	A35 CLN

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A12 Side A, 2A4A14 Side A, 2A4A22 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112858-A(66123NE)

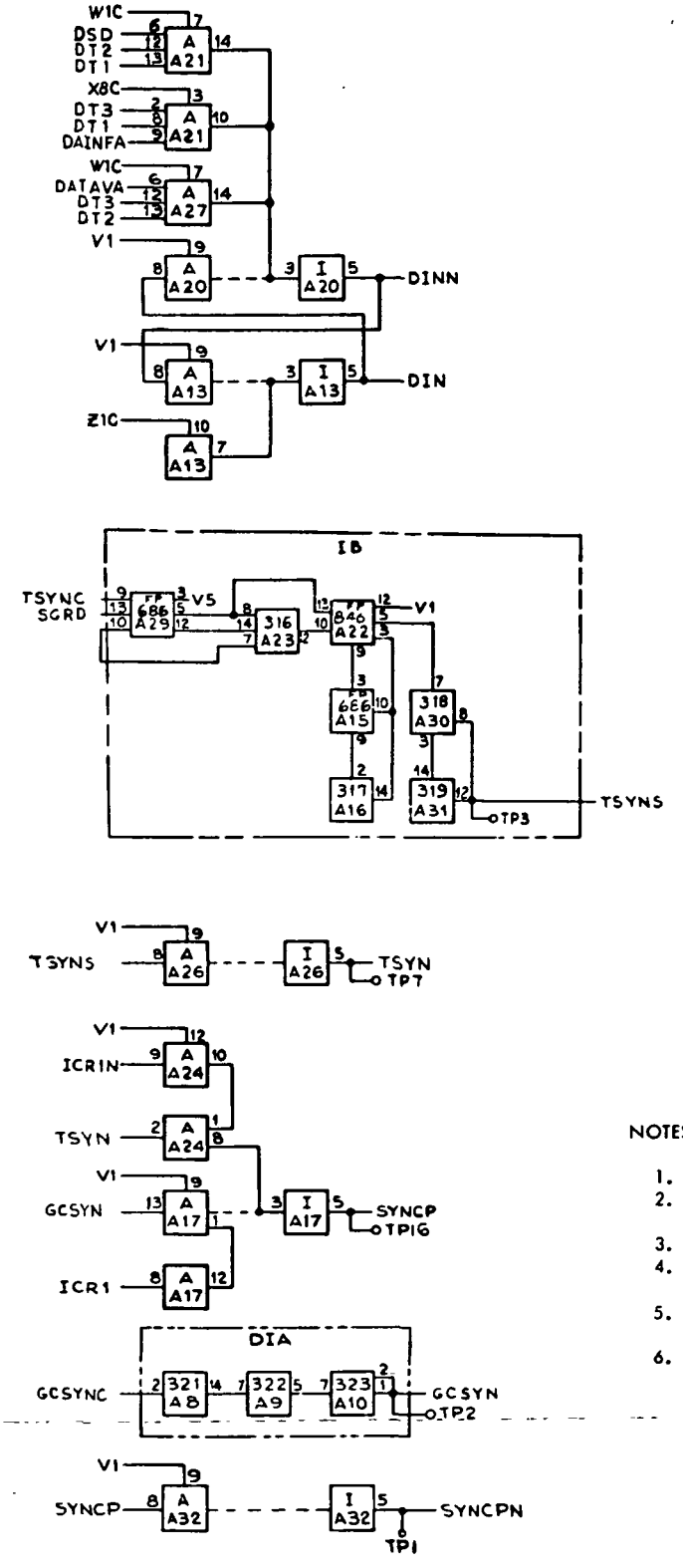
Figure 10-21. Processor Storage Logic Diagram (Sheet 2)



ULD LOCATIONS

A1 I	A2 I	A3 I	A4 I	A5 I	A6 AA	A7 I
A8 321	A9 322	A10 323	A11 AA	A12 AA	A13 I	A14 AA
A15 FP 686	A16 317	A17 I	A18 I	A19 AA	A20 I	A21 AA
A22 FP 846	A23 316	A24 AB	A25 AA	A26 I	A27 AA	A28 I
A29 FP 686	A30 318	A31 319	A32 I	A33 I	A34 I	A35 I

Figure 10-22. Telemetry Control Logic Diagram (Sheet 1 of 8)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	EYCR
2		17	TCWN
3		18	Y8C
4		19	
5		20	TRP
6		21	ETCRN
7		22	W1C
8		23	PAAVA
9		24	V3
10		25	
11		26	SIG RET(TP14)
12		27	
13		28	V1
14		29	LGAVA
15		30	SSEP

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	Z1C	52	DIN
4	DT1	54	A4DVA
6	DSD	56	DINN
8	TLMA	58	V7
10	TCW	60	G3DVNA
12	MBYPDA	62	
14	DATAVA	64	G6DVNA
16	PBG2VA	66	
18	CODE	68	G7DVA
20	SSDO	70	PCAVA
22	DAINFA	72	ICRVA
24	X8C	74	DT2
26	OCRA	76	ICR1
28	TRP	78	PABG1VA
30	V5A	80	
32	DCRA	82	G6DVA
34	SSRVA	84	A5DVA
36		86	ICR1N
38	G2DVA	88	GCSYNC
40	PBAVA	90	SGRD
42		92	TSYNC
44		94	C3RNA
46		96	DT3
48	C1RDA	98	G5DVNA
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A9 Side B.
6. This Drawing Derived From IBM DWG NO. 6112378-B(66126BD)

Figure 10-22. Telemetry Control Logic Diagram (Sheet 2)

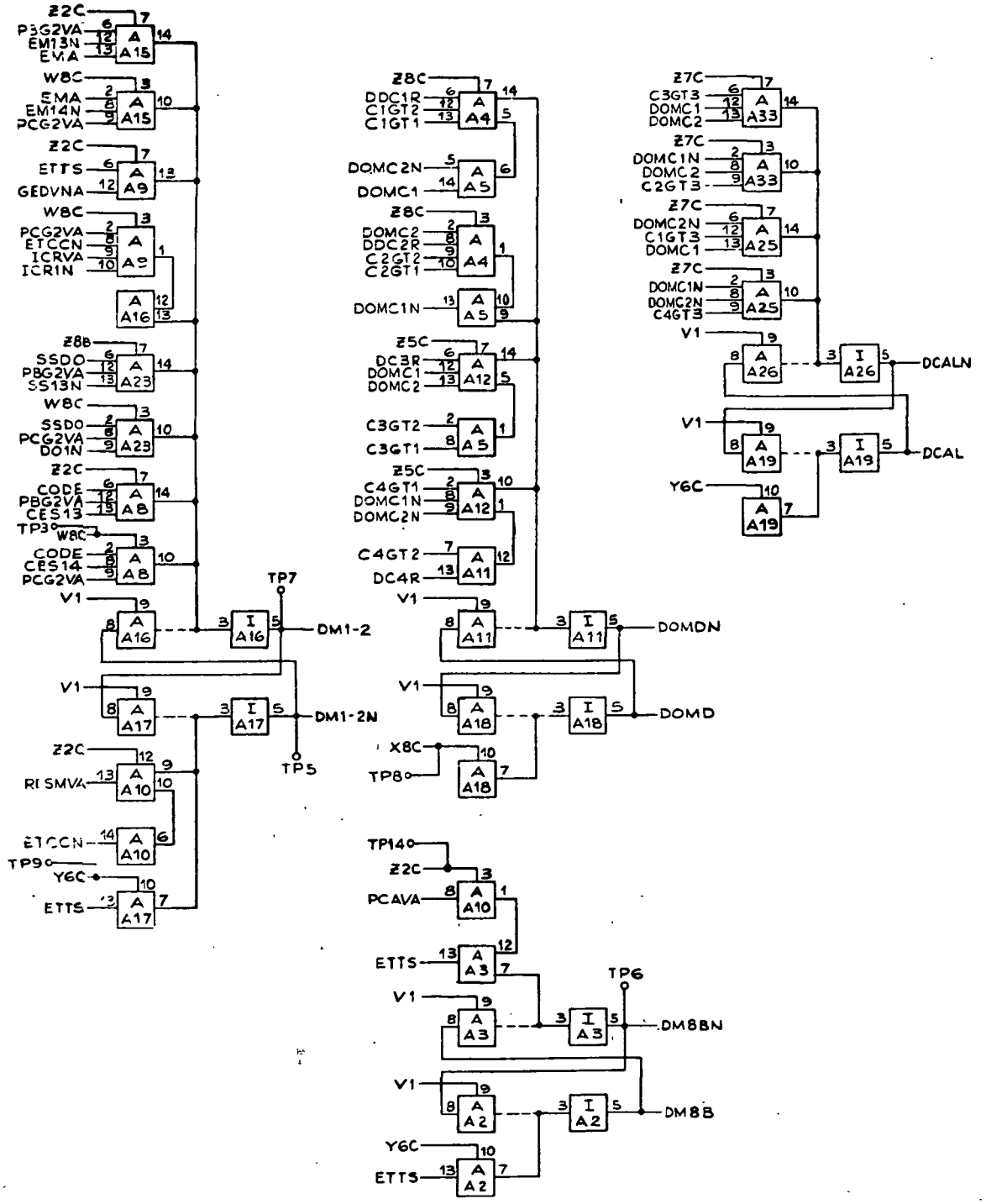
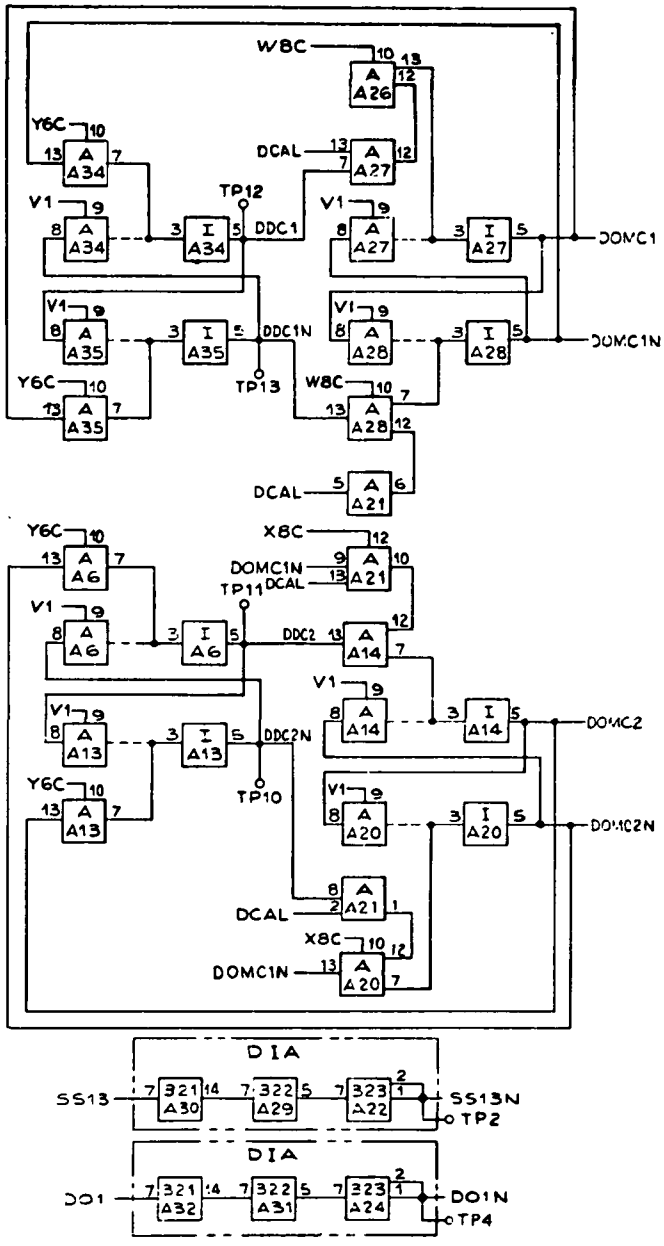


Figure 10-22. Telemetry Control Logic Diagram (Sheet 3)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1	PCG2VA	16	W8C
2	SIG-RET(TP1)	17	X8C
3		18	Y6C
4	V1	19	DM1-2
5		20	G5DVN
6	V3	21	
7		22	
8		23	
9		24	
10		25	
11		26	
12		27	
13		28	
14		29	DM8B
15	Z2C	30	PCAVA

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	C1GT2	51	DOMD
3	C1GT3	53	DO1
5	EM14N	55	DOMC2
7	DOMC1	57	ETTS
9	EM13N	59	C3GT2
11	C2GT3	61	C3GT3
13	DOMC2N	63	DCALN
15	PBG2VA	65	C4GT1
17	CODE	67	ETCCN
19	SSDO	69	PCAVA
21	Z8B	71	ICRVA
23	C2GT2	73	DC3R
25	C2GT1	75	DDC2R
27	SS13	77	DDC1R
29	RESMVA	79	C4GT3
31	EMA	81	DOMC1N
33	CES14	83	DCAL
35	C1GT1	85	Z7C
37	DC4R	87	ICR1N
39	CES13	89	C4GT2
41	Z8C	91	V1
43	C3GT1	93	Z5C
45	DM8B	95	
47	DOMDN	97	G5DVNA
49	V3		

ULD LOCATIONS

A1	A2 I	A3 I	A4 AA	A5 AB	A6 I	A7
A8 AA	A9 AA	A10 AB	A11 I	A12 AA	A13 I	A14 I
A15 AA	A16 I	A17 I	A18 I	A19 I	A20 I	A21 AB
A22 B23	A23 AA	A24 B23	A25 AA	A26 I	A27 I	A28 I
A29 B22	A30 B21	A31 B22	A32 B21	A33 AA	A34 I	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A31 Side A.
6. This Drawing Derived From IBM DWG NO. 6112838-REL(66123CR)

Figure 10-22. Telemetry Control Logic Diagram (Sheet 4)

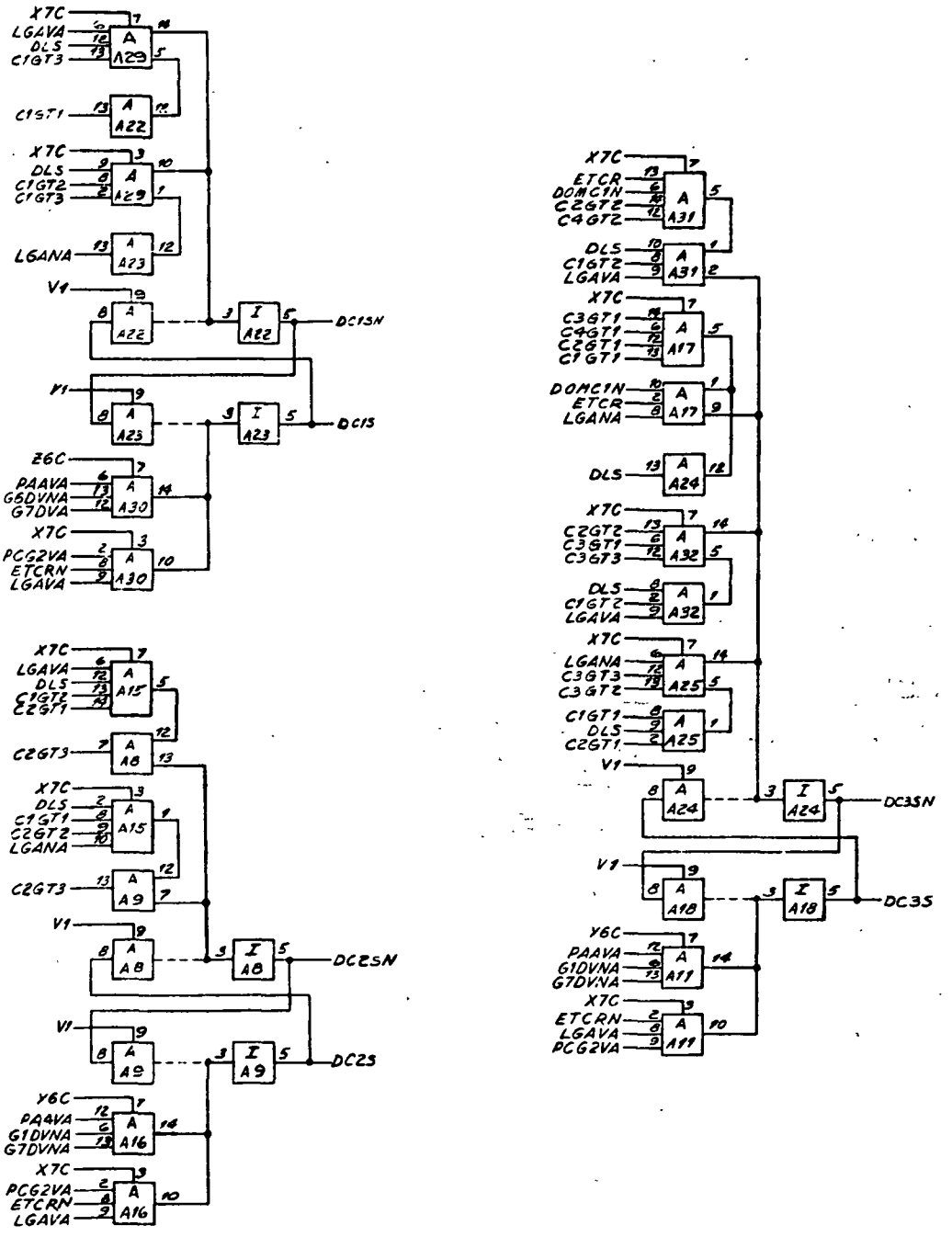
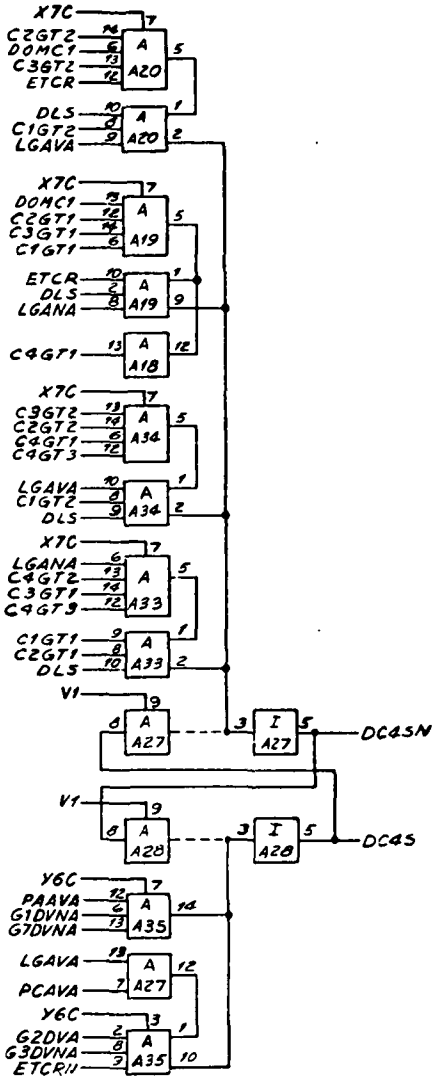


Figure 10-22. Telemetry Control Logic Diagram (Sheet 5)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	SIG-RET	52	C1GT2
4		54	X7C
6	V1	56	LGAVA
8		58	DLS
10	G1DVNA	60	DC3SN
12	V3	62	C2GT2
14	G2DVA	64	C4GT2
16	G3DVNA	66	DOMCIN
18	DC4S	68	C3GT1
20	DC4SN	70	ETCR
22	C3GT2	72	G7DVNA
24		74	DC1S
26		76	G6DVNA
28	Y6C	78	PAAVA
30	PCAVA	80	PCG2VA
32	DOMC1	82	Z6C
34	C4GT3	84	C2GT3
36	LGANA	86	DC2S
38	C4GT1	88	DC2SN
40	C2GT1	90	G7DVA
42	DC3S	92	DC1SN
44		94	C1GT3
46		96	C1GT1
48		98	ETCRN
50	C3GT3		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A8 Side B.
6. This Drawing Derived From IBM DWG NO. 6112348-REL(66123AS)

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8 I	A9 I	A10	A11 AA	A12	A13	A14
A15 AA	A16 AA	A17 AA	A18 I	A19 AA	A20 AA	A21
A22 I	A23 I	A24 I	A25 AA	A26	A27 I	A28 I
A29 AA	A30 AA	A31 AA	A32 AA	A33 AA	A34 AA	A35 AA

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Figure 10-22. Telemetry Control Logic Diagram (Sheet 6)

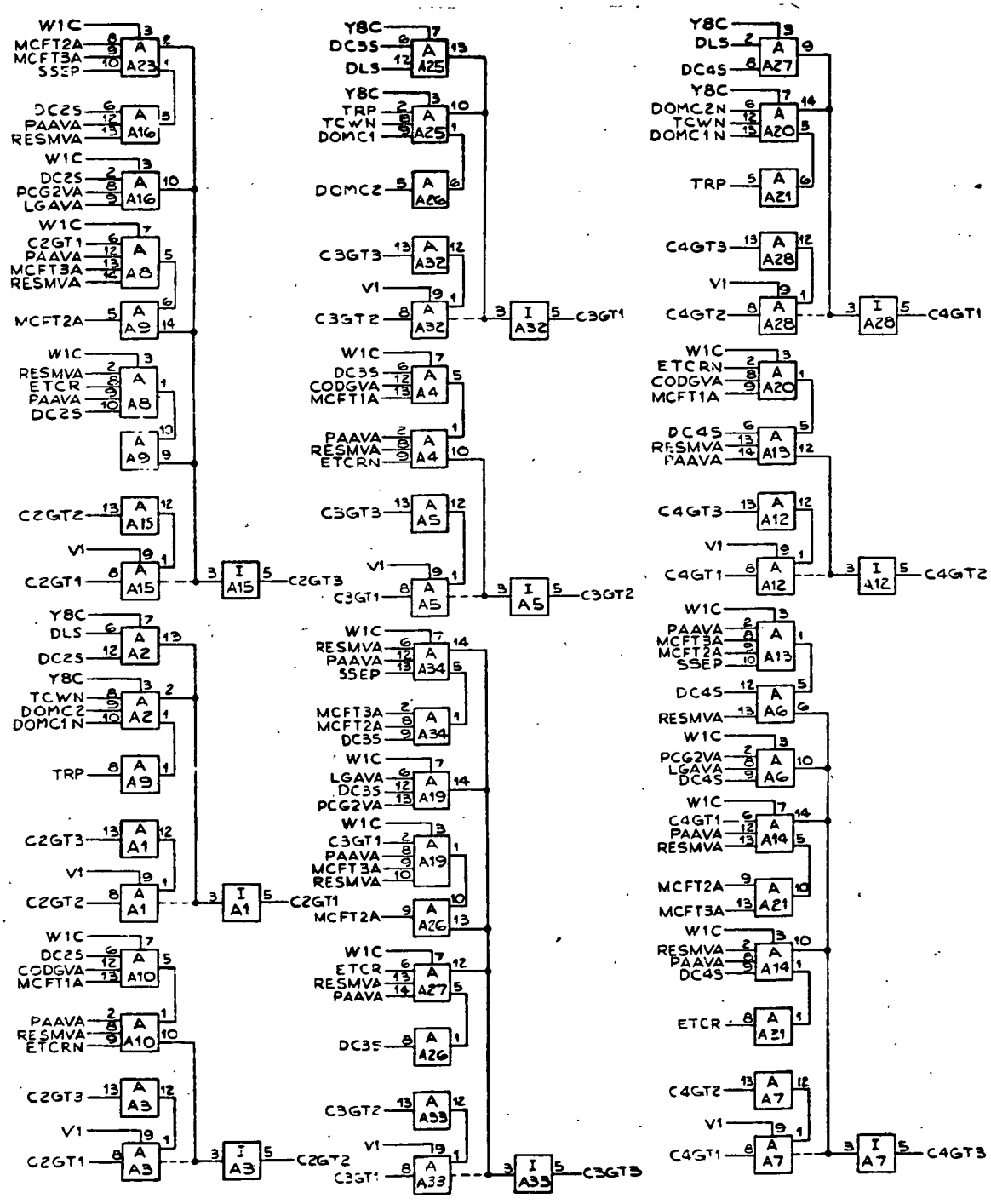
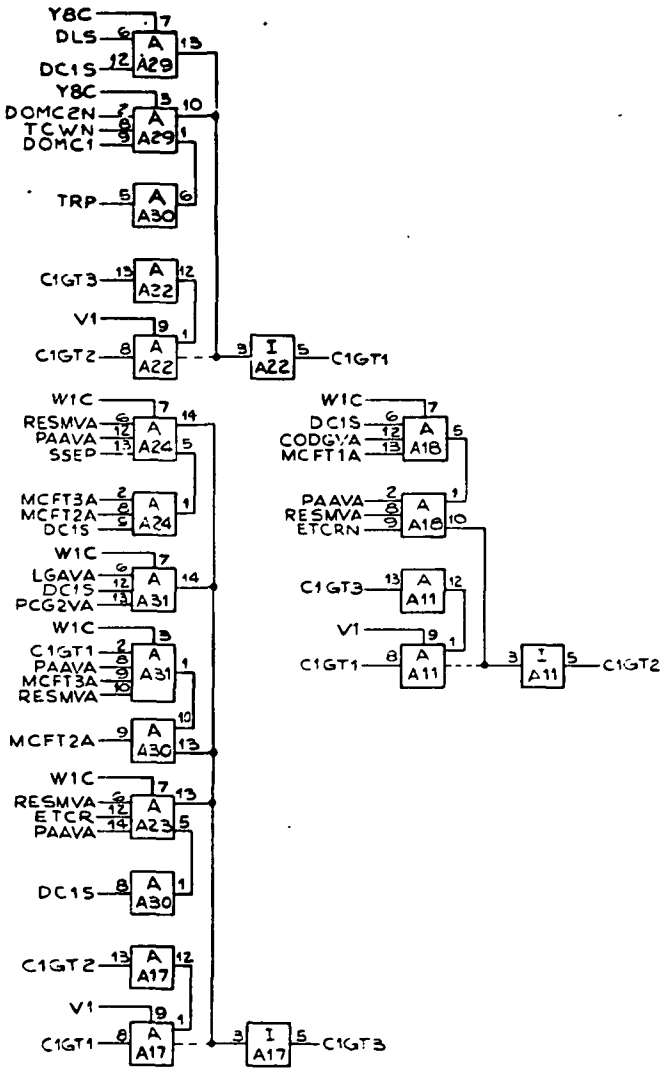


Figure 10-22. Telemetry Control Logic Diagram (Sheet 7)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	ETCR
2		17	TCWN
3		18	Y8C
4		19	
5		20	TRP
6		21	ETCRN
7		22	W1C
8		23	PAAVA
9		24	V3
10		25	
11		26	SIG-RET
12		27	
13		28	V1
14		29	LGAVA
15		30	SSEP

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	C1GT2	51	
3	C1GT3	53	
5	DLS	55	
7	DOMC1	57	DOMC2
9	SIG-RET	59	C3GT2
11	DC1S	61	C3GT3
13	DOMC2N	63	
15	C2GT3	65	TCWN
17	ETCR	67	C4GT1
19	C2GT1	69	DC3S
21	PCG2VA	71	MCFT2A
23	C2GT2	73	MCFT3A
25	DC2S	75	SSEP
27		77	DC4S
29	RESMVA	79	C4GT3
31		81	DOMC1N
33		83	ETCRN
35	C1GT1	85	W1C
37	LGAVA	87	V1
39		89	C4GT2
41	PAAVA	91	Y8C
43	C3GT1	93	CODGVA
45		95	MCFT1A
47		97	
49	V3		

ULD LOCATIONS

A1 I	A2 AA	A3 I	A4 AA	A5 I	A6 AA	A7 I
A8 AA	A9 AB	A10 AA	A11 I	A12 I	A13 AA	A14 AA
A15 I	A16 AA	A17 I	A18 AA	A19 AA	A20 AA	A21 AB
A22 I	A23 AA	A24 AA	A25 AA	A26 AB	A27 AA	A28 I
A29 AA	A30 AB	A31 AA	A32 I	A33 I	A34 AA	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A9 Side A.
6. This Drawing Derived From IBM DWG NO. 6112368-REL(66123CC)

Figure 10-22. Telemetry Control Logic Diagram (Sheet 8)

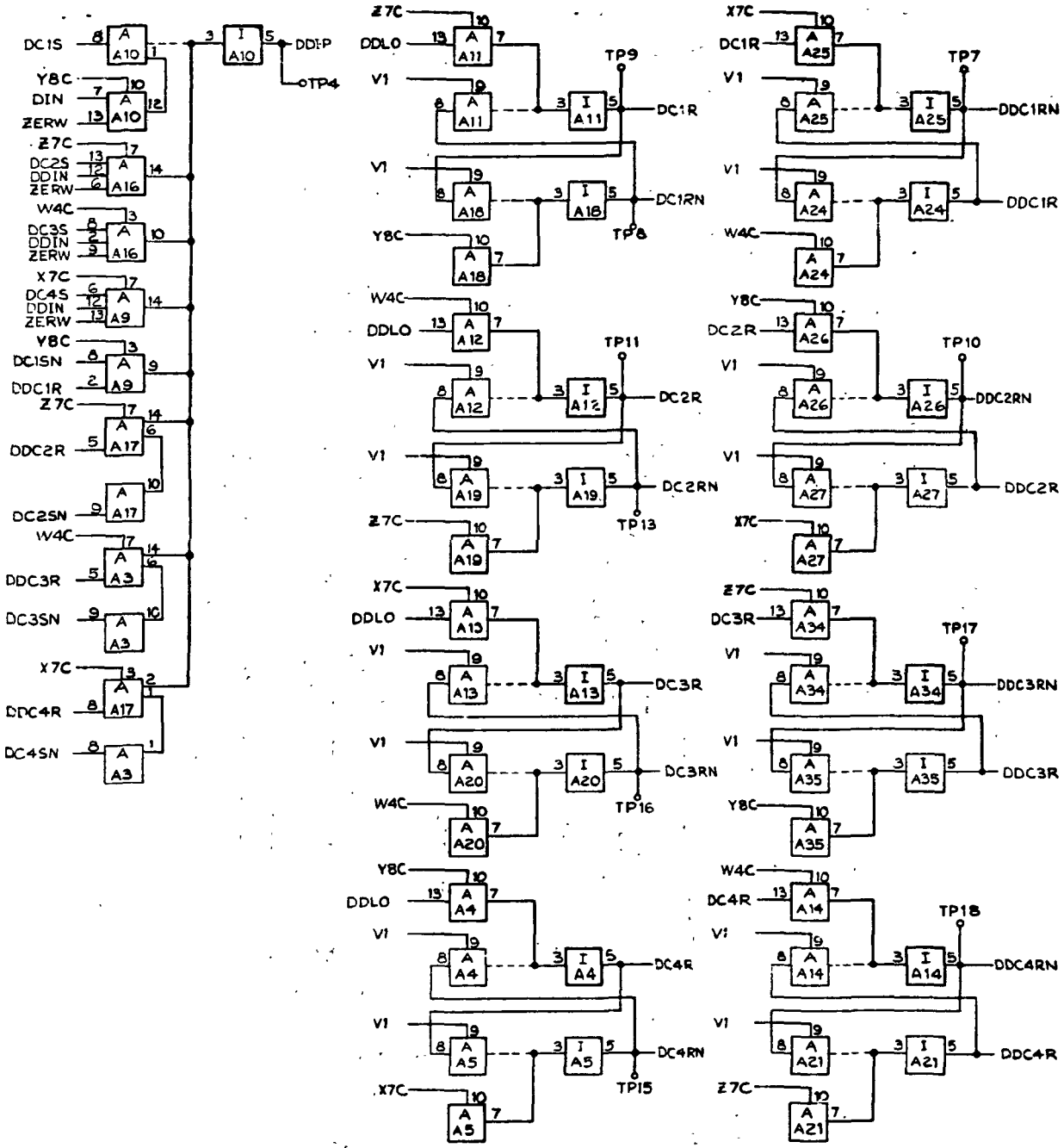
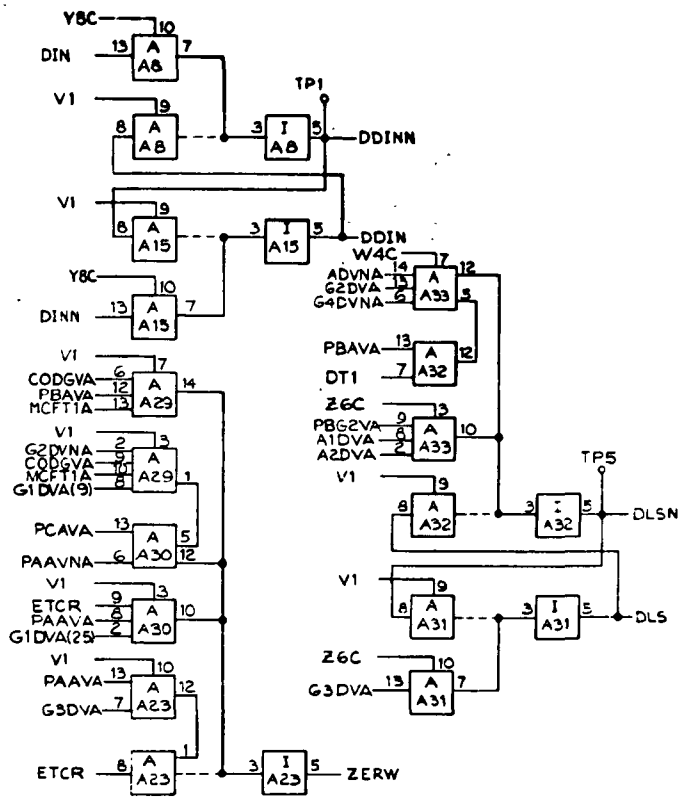
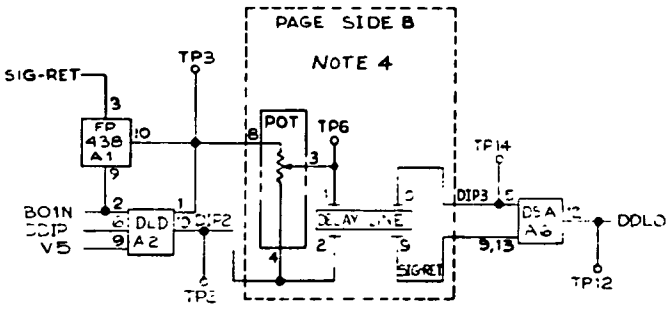


Figure 10-23. Telemetry Storage Logic Diagram (Sheet 1 of 2)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	Z7C	51	ZERW
3	DDIN	53	DDC1R
5	DLS	55	DT1
7	SIG-RET.	57	DDC2R
9	G1DVA	59	A1DVA
11	DC1S	61	A2DVA
13	G2DVNA	63	
15	PBG2VA	65	ADVNA
17	ETCR	67	G2DVA
19	DIN	69	DC3S
21	DINN	71	DDC3R
23	X7C	73	PCAVA
25	G1DVA	75	
27	G4DV11A	77	DC4S
29	PAAVNA	79	V5
31	DC1SN	81	DC3R
33	DC2S	83	Z6C
35	X4C	85	Y8C
37	DC3SN	87	V1
39	PBAVA	89	DDC4R
41	PAAVA	91	BOIN
43	DC4SN	93	CODGVA
45	G3DVA	95	MCFT1A
47	DC2SN	97	DC4R
49	V3		



A1 FP 438	A2 DLD	A3 A5	A4	A5	A6 DSA	A7
A8	A9 AA	A10	A11	A12	A13	A14
A15	A16 AA	A17 AB	A18	A19	A20	A21
A22	A23	A24	A25	A26	A27	A28
A29 AA	A30 AA	A31	A32	A33 AA	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A20 Side A.
6. This Drawing Derived From IBM DWG NO. 6112878-A(66123NE)

Figure 10-23. Telemetry Storage Logic Diagram (Sheet 2)

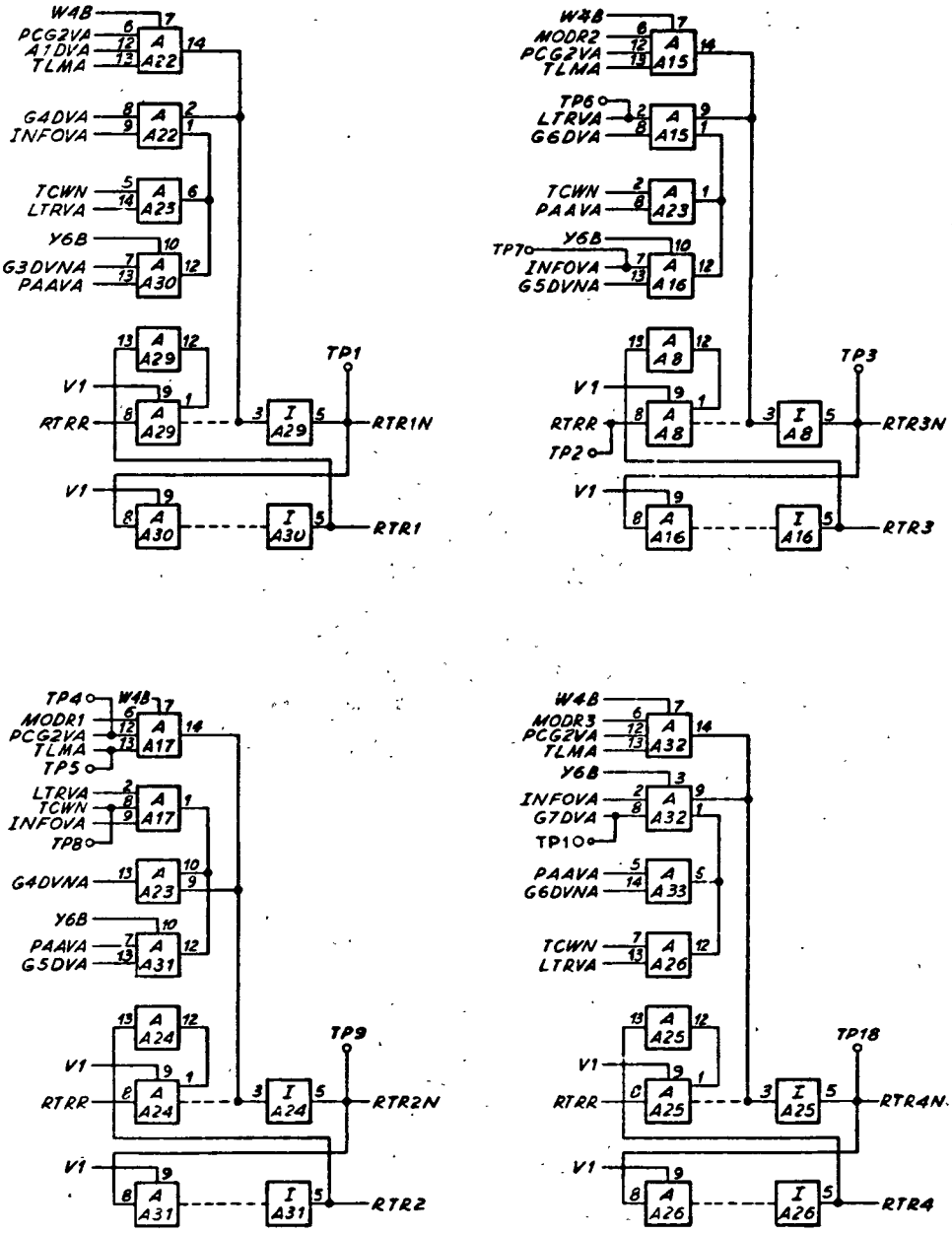
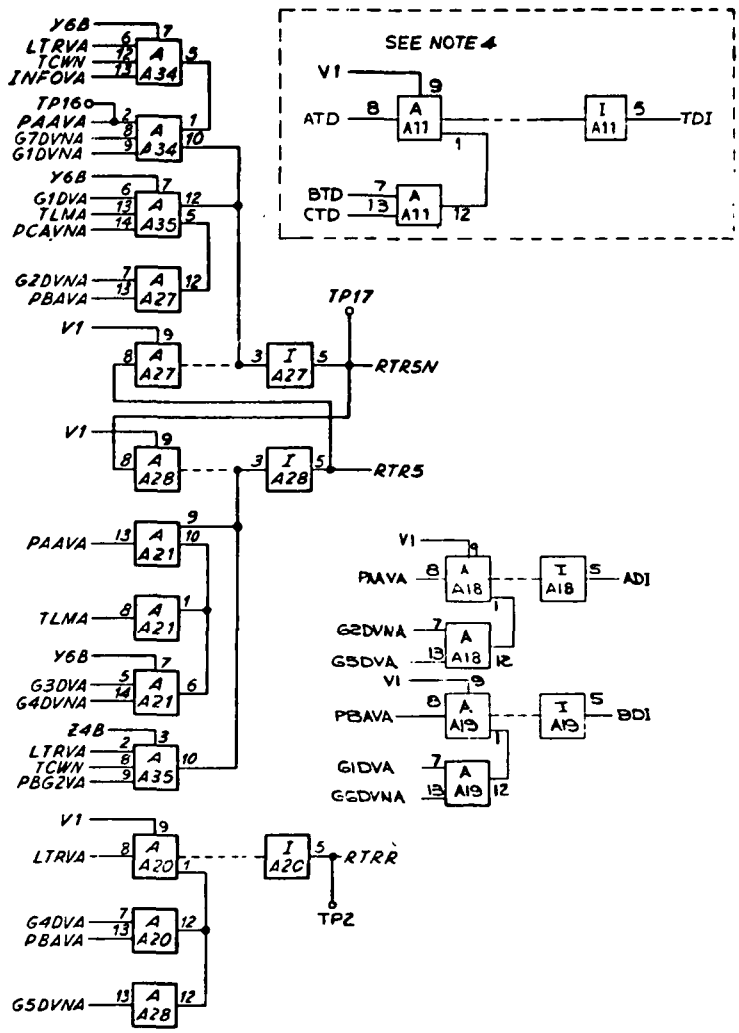


Figure 10-24. Real Time Register Logic Diagram (Sheet 1 of 2)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	G6DVNA
2		17	G4DVNA
3	G6DVA	18	G4DVA
4		19	G7DVNA
5		20	G1DVNA
6		21	G5DVA
7		22	G1DVA
8		23	G7DVA
9		24	G3DVA
10		25	INFOVA
11		26	LTRVA
12		27	PCG2VA
13	G2DVNA	28	TLMA
14	PBAVA	29	PAAVA
15	G5DVNA	30	TCWN

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	RTR5	52	
4		54	
6	V3	56	
8	Y6B	58	
10	SIG-RET	60	
12	V1	62	
14		64	
16	Z4B	66	RTR2
18		68	RTR1
20	G3DVNA	70	PBG2VA
22	BTD	72	MODR1
24	CTD	74	
26	ATD	76	
28	G2DVNA	78	
30		80	
32		82	
34		84	PCAVNA
36		86	MODR2
38		88	W4B
40		90	A1DVA
42	RTR4	92	TDI
44	MODR3	94	BDI
46		96	RTR3
48		98	ADI
50			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8 I	A9	A10	A11	A12	A13	A14
A15 AA	A16 I	A17 AA	A18 I	A19 I	A20 I	A21 AB
A22 AA	A23 AB	A24 I	A25 I	A26 I	A27 I	A28 I
A29	A30 I	A31 I	A32 AA	A33 AB	A34 AA	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A4 Side B.
6. This Drawing Derived From IBM DWG NO. 6112418-B(66126DN)

Figure 10-24. Real Time Register Logic Diagram (Sheet 2)

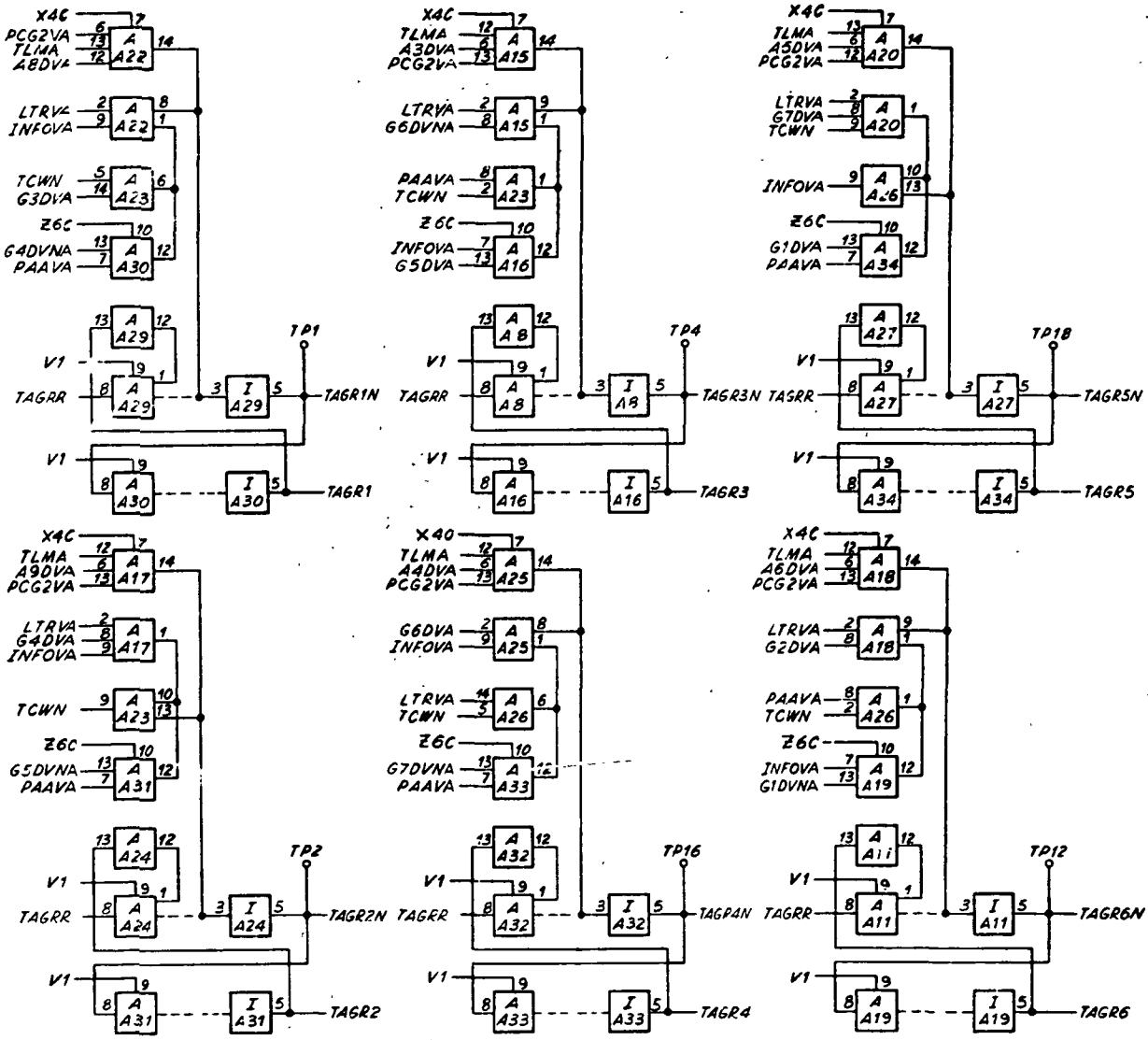
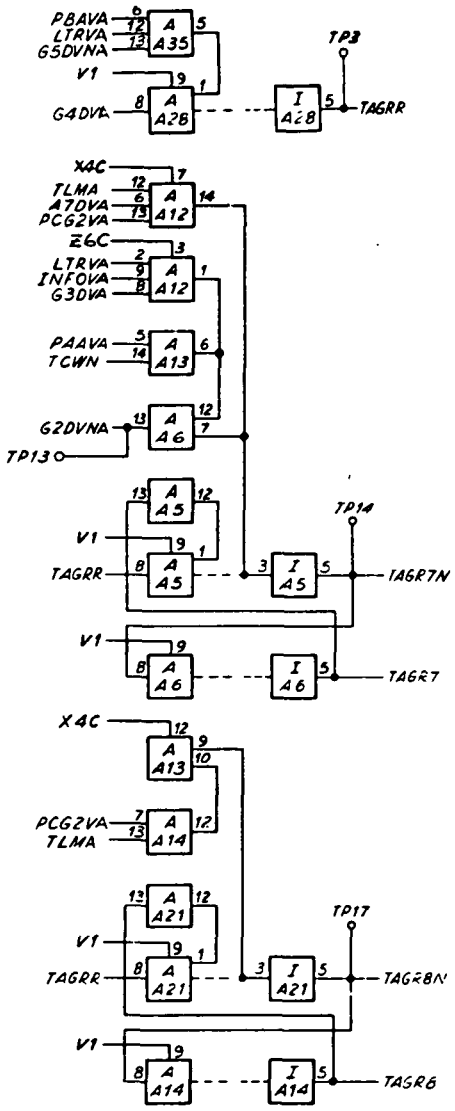


Figure 10-25. Tag Register Logic Diagram (Sheet 1 of 2)



THRU PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	G6DVNA
2		17	G4DVNA
3	G6DVA	18	G4DVA
4		19	G7DVNA
5	+9V	20	G1DVNA
6		21	G5DVA
7		22	G1DVA
8		23	G7DVA
9		24	G3DVA
10		25	INFOVA
11		26	LTRVA
12		27	PCG2VA
13	G2DVNA	28	TLMA
14	PBAVA	29	PAAVA
15	G5DVNA	30	TCWN

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V3	51	G1DVA
3	TAGR3	53	G7DVNA
5	G6DVNA	55	
7	SIG RET	57	
9	A6DVA	59	
11	V1	61	
13	X4C	63	TAGR4
15	A3DVA	65	TCWN
17		67	G4DVA
19	PAAVA	69	G7DVA
21	G3DVA	71	PCG2VA
23		73	A5DVA
25	TAGR1	75	G1DVNA
27	G4DVNA	77	TAGR6
29	G5DVA	79	PRAVA
31		81	LTRVA
33	TAGR2	83	TAGR5
35	G2DVA	85	A7DVA
37	INFOVA	87	TAGR7
39	A3DVA	89	
41	G5DVNA	91	Z6C
43	TLMA	93	
45	G6DVA	95	TAGR8
47	A4DVA	97	
49	A6DVA		

ULD LOCATIONS

A1	A2	A3	A4	A5 I	A6 I	A7
A8 I	A9	A10	A11 I	A12 AA	A13 AB	A14 I
A15 AA	A16 I	A17 AA	A18 AA	A19 I	A20 AA	A21 I
A22 AA	A23 AB	A24 I	A25 AA	A26 AB	A27 I	A28 I
A29 I	A30 I	A31 I	A32 I	A33 I	A34 I	A35 AA

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A4 Side A.
6. This Drawing Derived From IBM DWG NO. 6112388-REL(66123BS)

Figure 10-25. Tag Register Logic Diagram (Sheet 2)

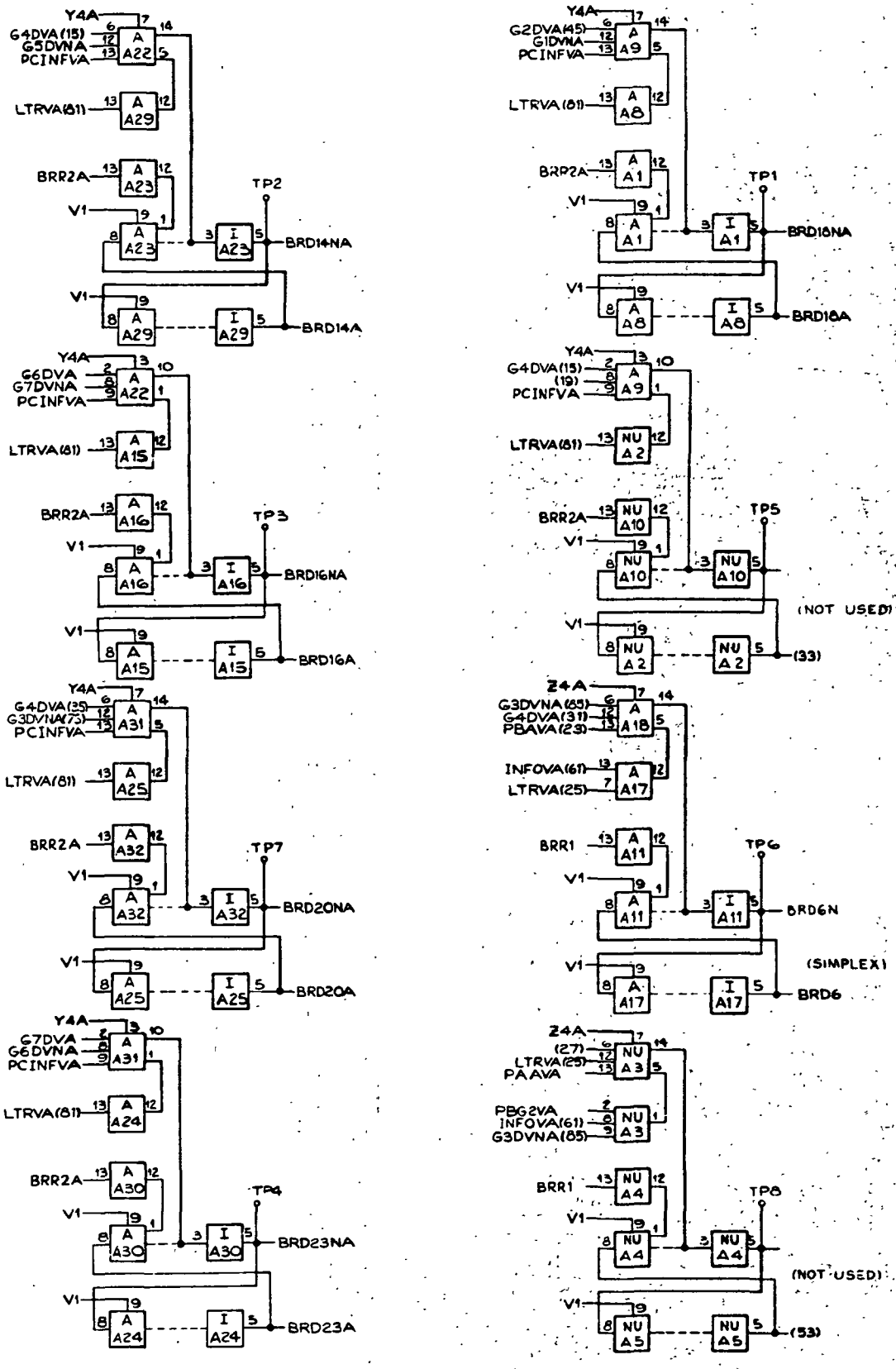
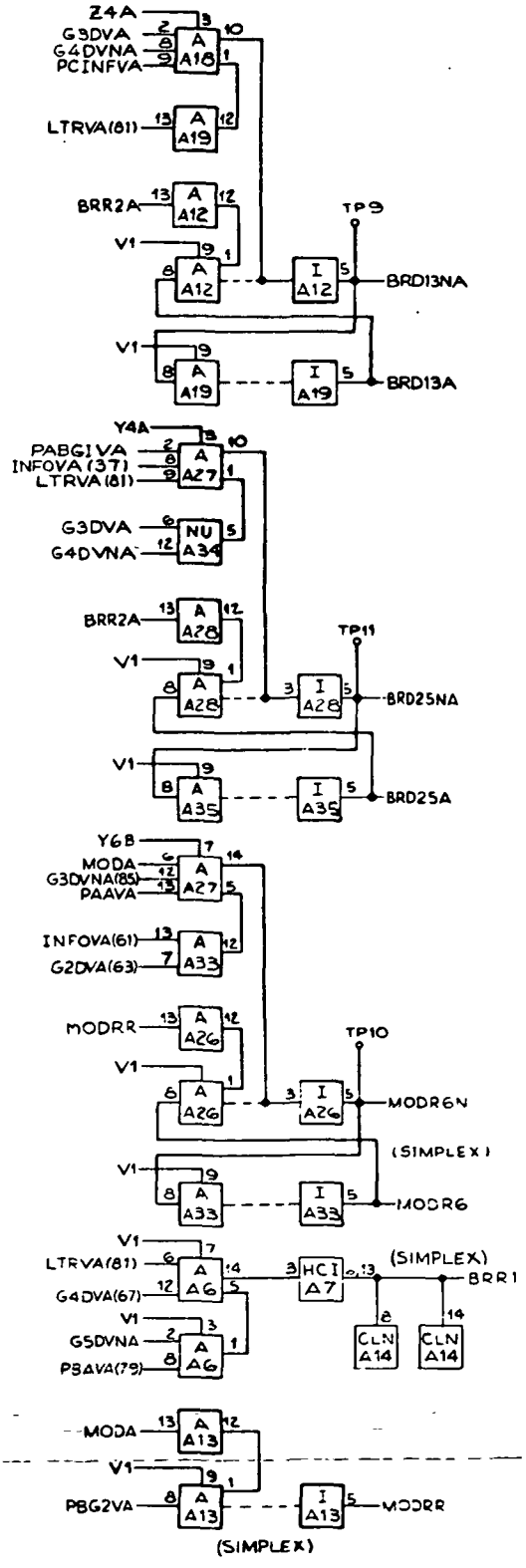
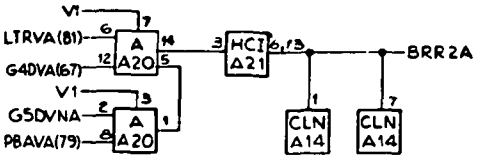


Figure 10-26. Buffer Register Logic Diagram (Sheet 1 of 12)





CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	BRD18A	51	BRD6
3	G7DVNA	53	
5	Y4A	55	G6DVNA
7	Y6B	57	BRD13A
9	G5DVNA	59	MODR6
11	BRD14A	61	INFOVA
13	G6DVA	63	G2DVA
15	G4DVA	65	MODRR
17	BRD16A	67	G4DVA
19		69	PBG2VA
21	BRD23A	71	PABG1VA
23	PBAVA	73	SIG-RET
25	LTRVA	75	G3DVNA
27		77	G4DVNA
29	G7DVA	79	PBAVA
31	G4DVA	81	LTRVA
33		83	G3DVA
35	G4DVA	85	G3DVNA
37	INFOVA	87	MODA
39	PCINFVA	89	PAAVA
41	G1DVNA	91	Z4A
43	V3	93	V1
45	G2DVA	95	BRD25A
47	BRD23A	97	BRR1
49	BRR2A		

ULD LOCATIONS

A1 I	A2	A3	A4	A5	A6 AA	A7 HCI
A8 I	A9 AA	A10	A11 I	A12 I	A13 I	A14 CLN
A15 I	A16 I	A17 I	A18 AA	A19 I	A20 AA	A21 HCI
A22 AA	A23 I	A24 I	A25 I	A26 I	A27 AA	A28 I
A29 I	A30 I	A31 AA	A32 I	A33 I	A34	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A19 Side A.
6. This Drawing Derived From IBM DWG NO. 6112567-A(66123TE)

Figure 10-26. Buffer Register Logic Diagram (Sheet 2)

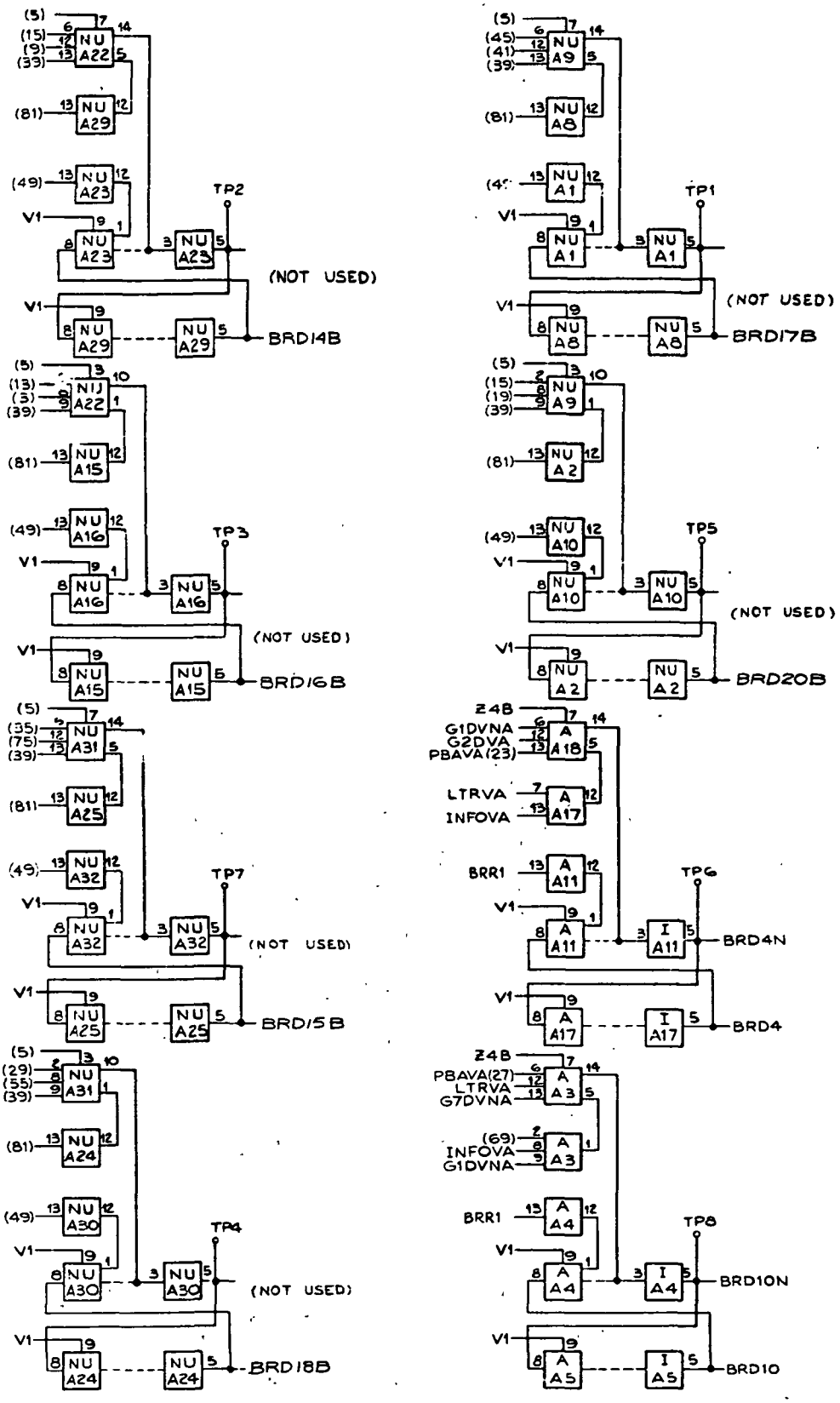
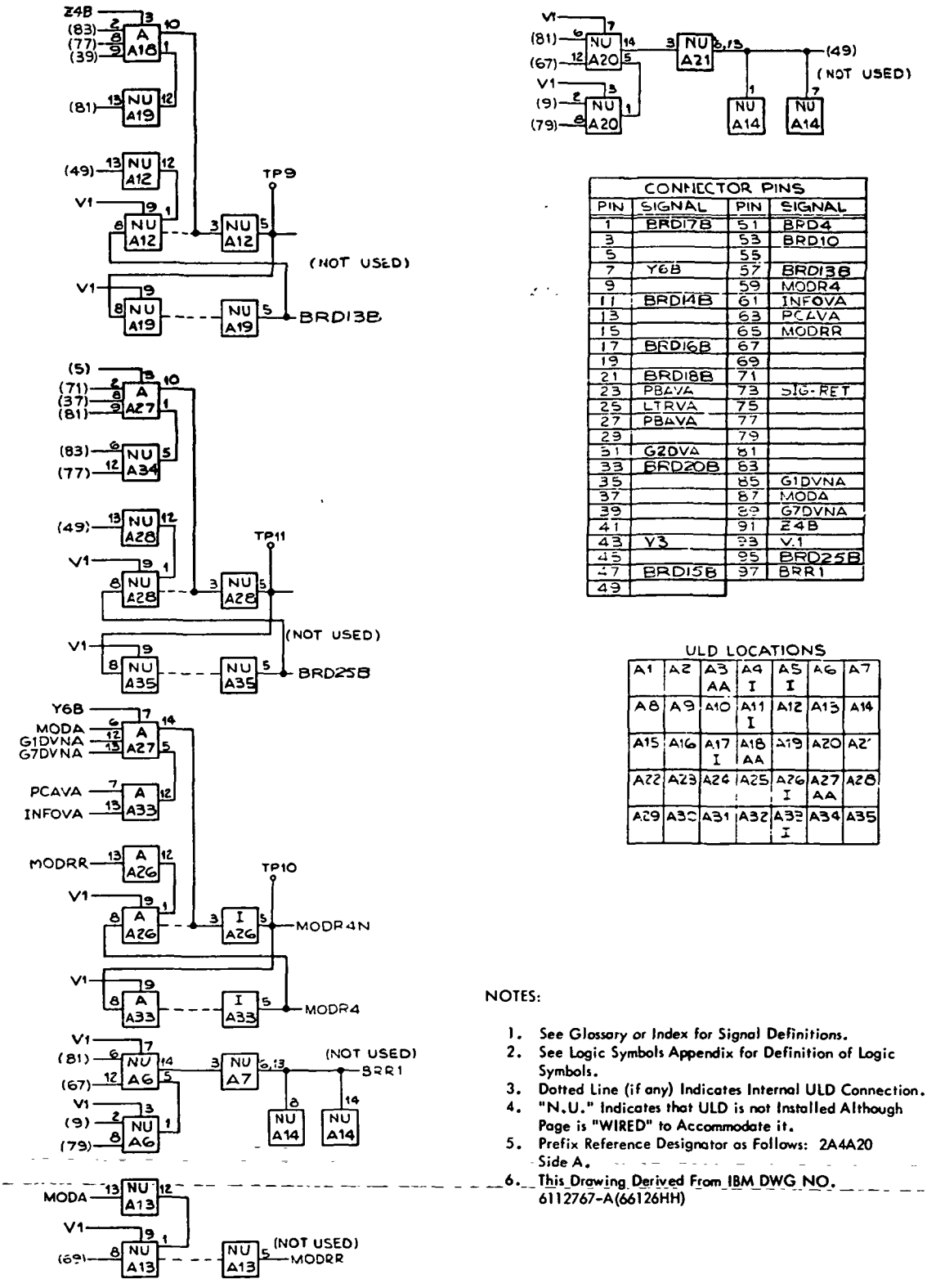


Figure 10-26. Buffer Register Logic Diagram (Sheet 3)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	BRD17B	51	BRD4
3		53	BRD10
5		55	
7	Y6B	57	BRD13B
9		59	MODR4
11	BRD14B	61	INFOVA
13		63	PCAVA
15		65	MODRR
17	BRD16B	67	
19		69	
21	BRD18B	71	
23	PBAVA	73	SIG-RET
25	LTRVA	75	
27	PBAVA	77	
29		79	
31	G2DVA	81	
33	BRD20B	83	
35		85	G1DVNA
37		87	MODA
39		89	G7DVNA
41		91	Z4B
43	V3	93	V1
45		95	BRD25B
47	BRD15B	97	BRR1
49			

ULD LOCATIONS

A1	A2	A3 AA	A4 I	A5 I	A6	A7
A8	A9	A10	A11 I	A12	A13	A14
A15	A16	A17 I	A18 AA	A19	A20	A21
A22	A23	A24	A25	A26 I	A27 AA	A28
A29	A30	A31	A32	A33 I	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A20 Side A.
6. This Drawing Derived From IBM DWG NO. 6112767-A(66126HH)

Figure 10-26. Buffer Register Logic Diagram (Sheet 4)

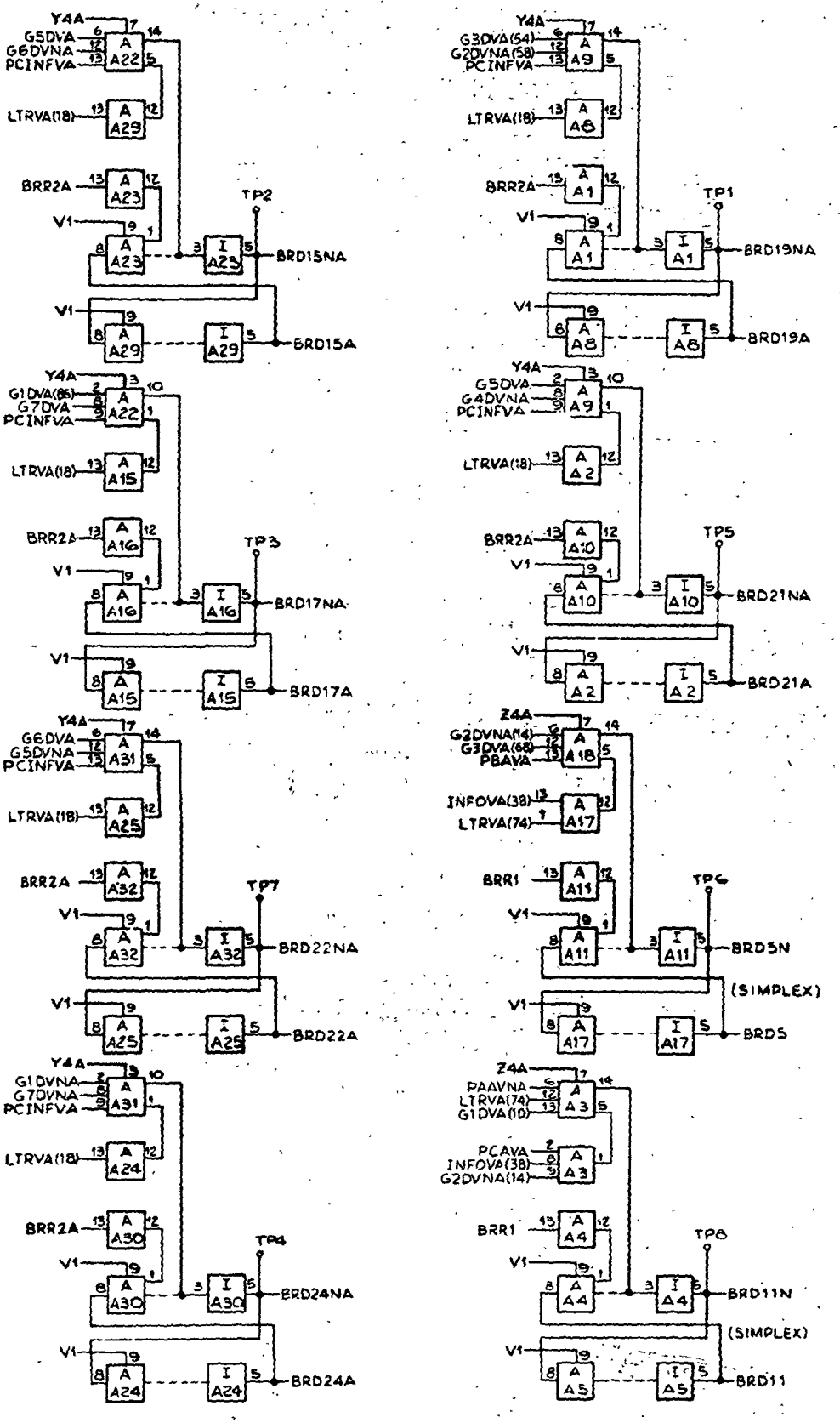
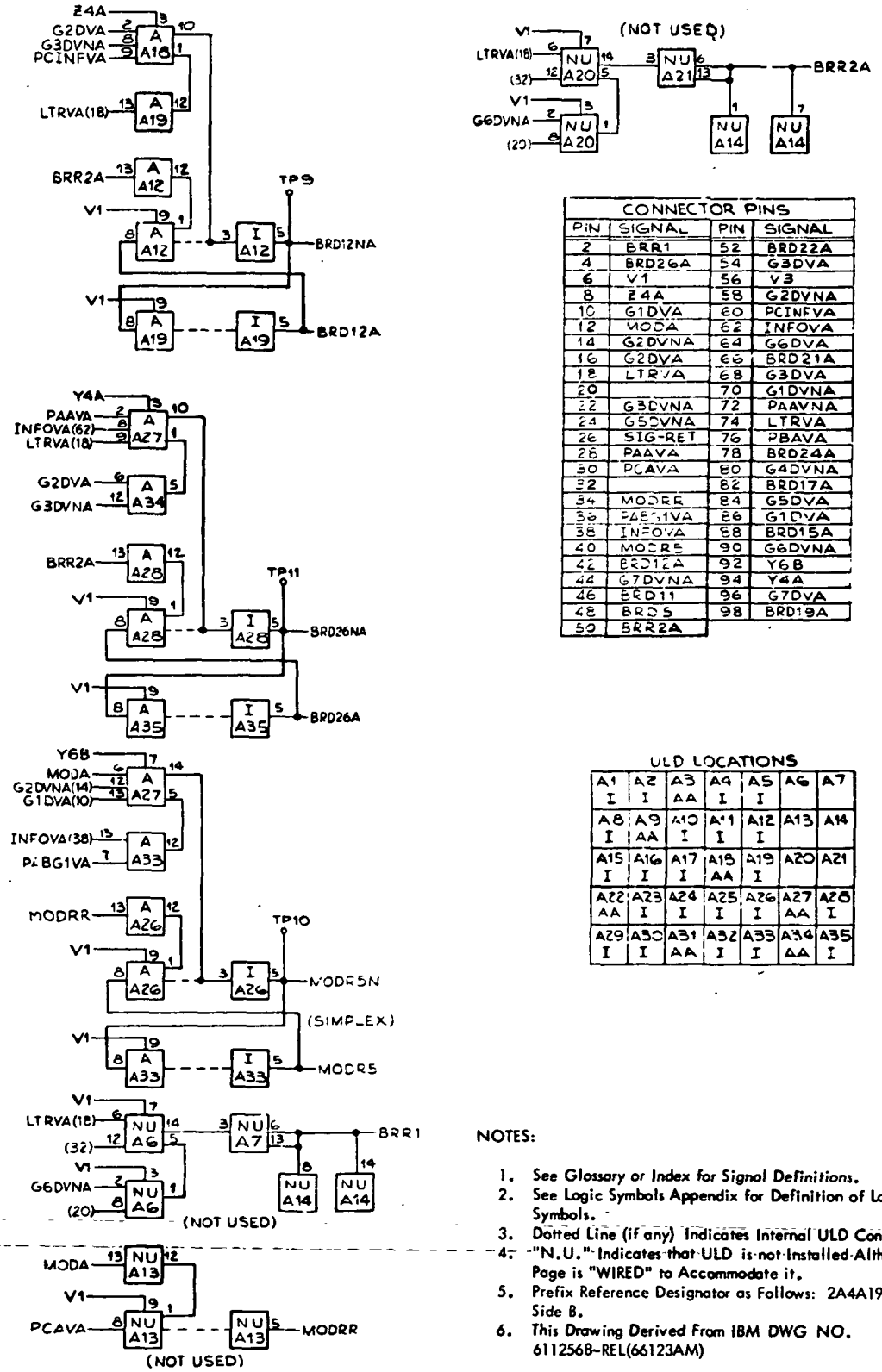


Figure 10-26. Buffer Register Logic Diagram (Sheet 5)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	BRR1	52	BRD22A
4	BRD26A	54	G3DVA
6	V1	56	V3
8	Z4A	58	G2DVNA
10	G1DVA	60	PCINFVA
12	MODA	62	INFOVA
14	G2DVNA	64	G6DVA
16	G2DVA	66	BRD21A
18	LTRVA	68	G3DVA
20		70	G1DVNA
22	G3DVNA	72	PAAVNA
24	G5DVNA	74	LTRVA
26	SIG-RET	76	PBAVA
28	PAAVA	78	BRD24A
30	PCAVA	80	G4DVNA
32		82	BRD17A
34	MODRR	84	G5DVA
36	PABG1VA	86	G1DVA
38	INFOVA	88	BRD15A
40	MODRS	90	G6DVNA
42	BRD12A	92	Y6B
44	G7DVNA	94	Y4A
46	BRD11	96	G7DVA
48	BRD5	98	BRD19A
50	BRR2A		

ULD LOCATIONS

A1 I	A2 I	A3 AA	A4 I	A5 I	A6	A7
A8 I	A9 AA	A10 I	A11 I	A12 I	A13	A14
A15 I	A16 I	A17 I	A18 AA	A19 I	A20	A21
A22 AA	A23 I	A24 I	A25 I	A26 I	A27 AA	A28 I
A29 I	A30 I	A31 AA	A32 I	A33 I	A34 AA	A35 I

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A19 Side B.
6. This Drawing Derived From IBM DWG NO. 6112568-REL(66123AM)

Figure 10-26. Buffer Register Logic Diagram (Sheet 6)

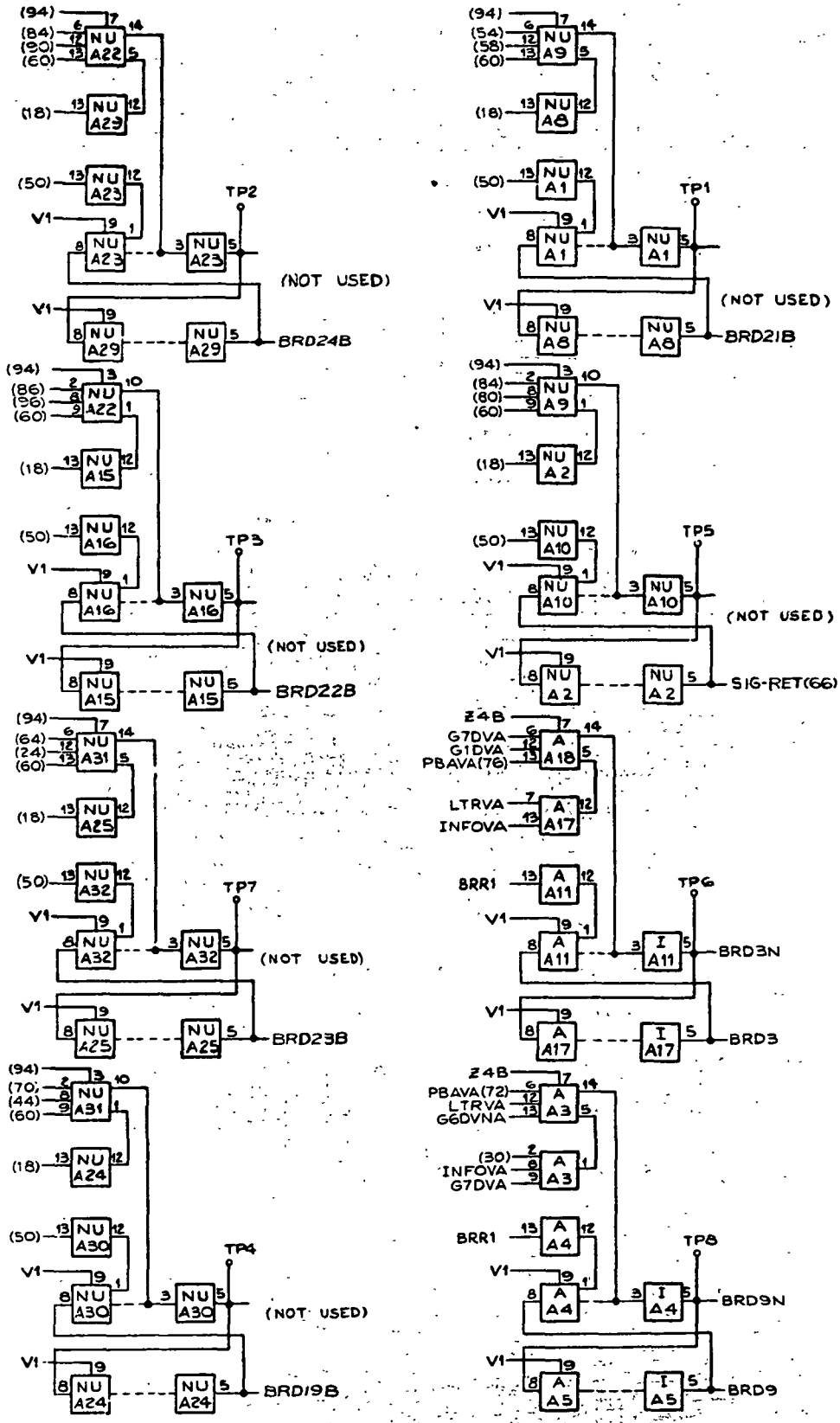
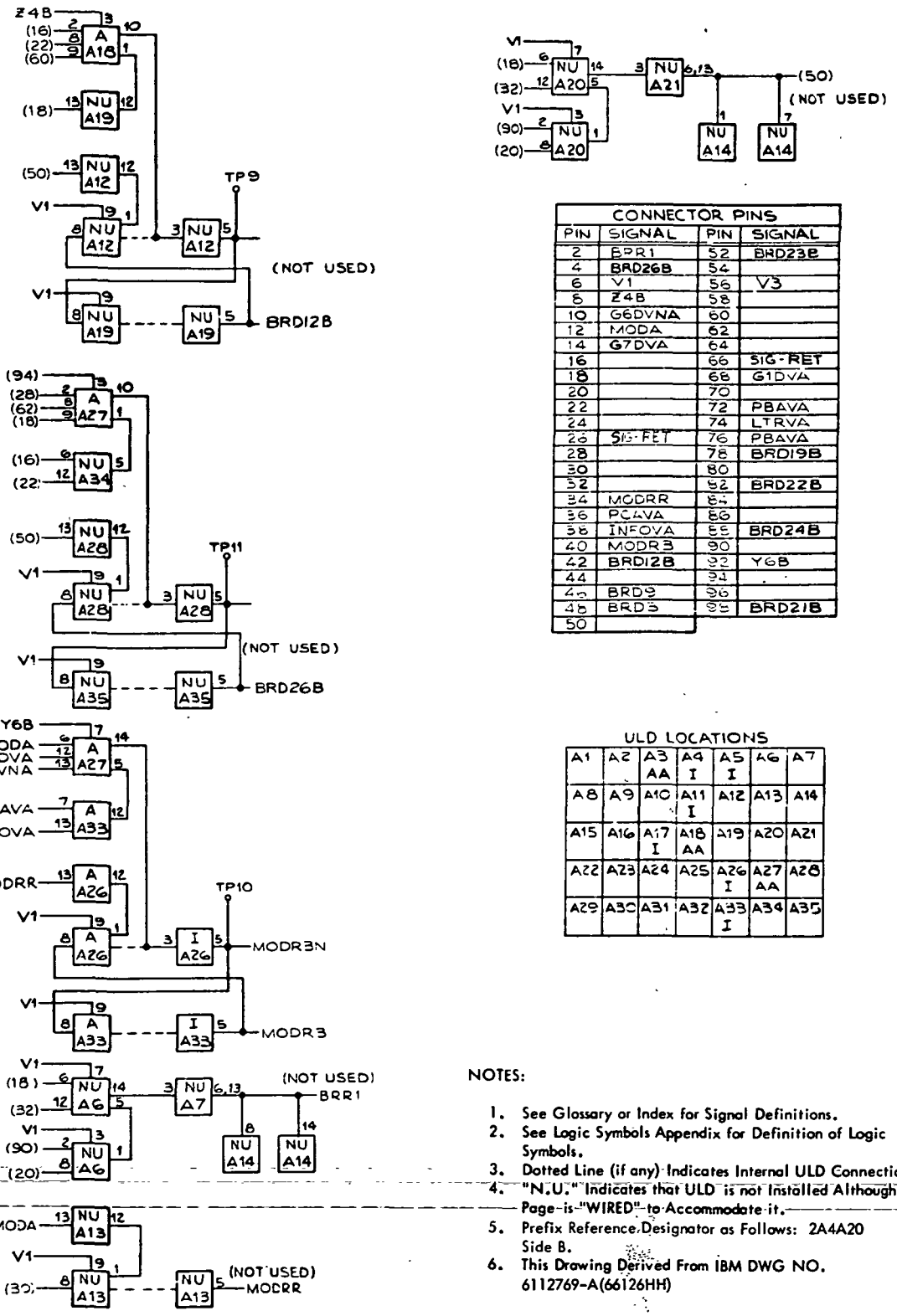


Figure 10-26. Buffer Register Logic Diagram (Sheet 7)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	BRR1	52	BRD23B
4	BRD26B	54	
6	V1	56	V3
8	Z4B	58	
10	G6DVNA	60	
12	MODA	62	
14	G7DVA	64	
16		66	SIG-RET
18		68	G1DVA
20		70	
22		72	PBAVA
24		74	LTRVA
26	SIG-RET	76	PBAVA
28		78	BRD19B
30		80	
32		82	BRD22B
34	MODRR	84	
36	PCAVA	86	
38	INFOVA	88	BRD24B
40	MODR3	90	
42	BRD12B	92	Y6B
44		94	
46	BRD9	96	
48	BRD3	98	BRD21B
50			

ULD LOCATIONS

A1	A2	A3 AA	A4 I	A5 I	A6	A7
A8	A9	A10	A11 I	A12	A13	A14
A15	A16	A17 I	A18 AA	A19	A20	A21
A22	A23	A24	A25	A26 I	A27 AA	A28
A29	A30	A31	A32	A33 I	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A20 Side B.
6. This Drawing Derived From IBM DWG NO. 6112769-A(66126HH)

Figure 10-26. Buffer Register Logic Diagram (Sheet 8)

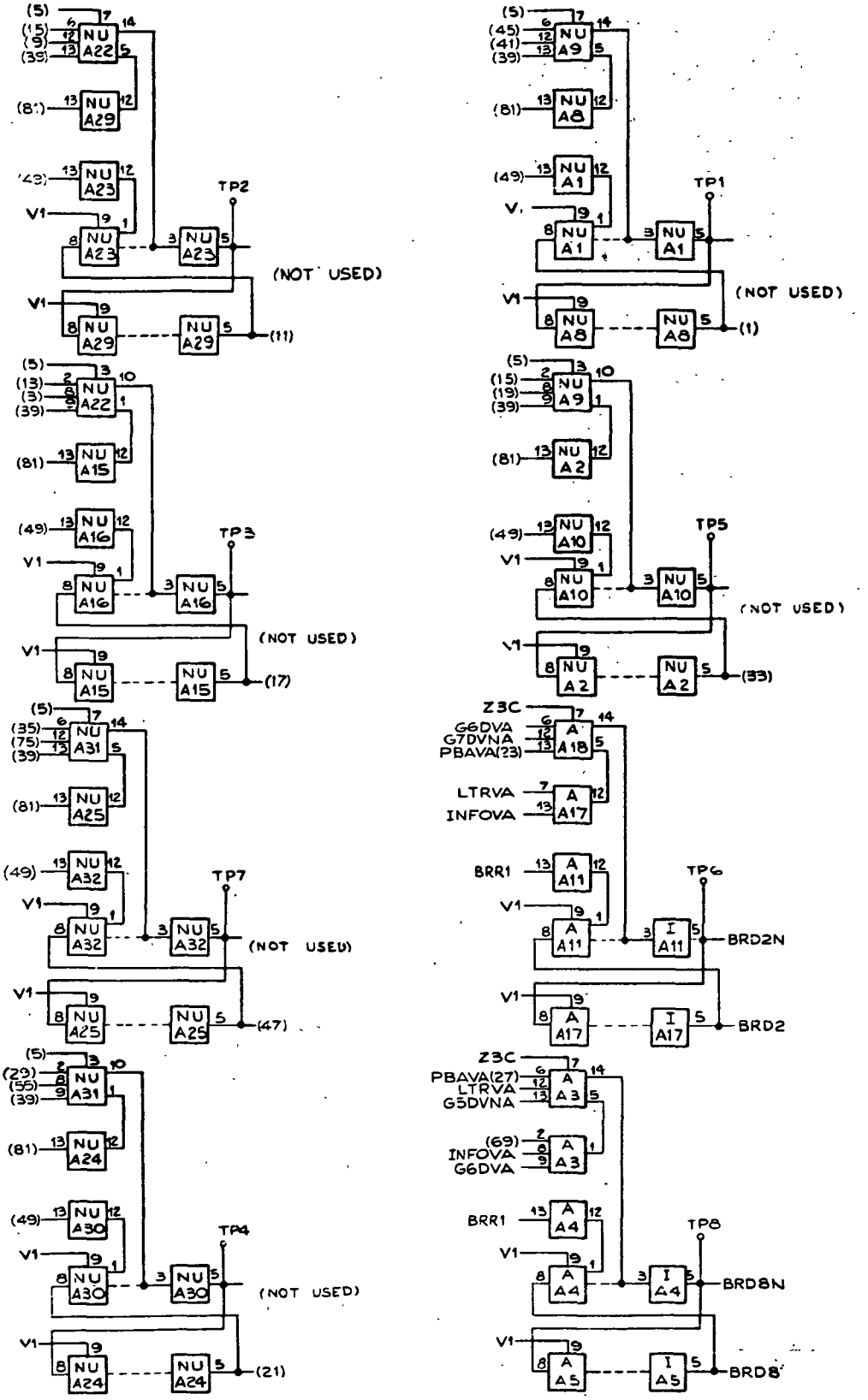
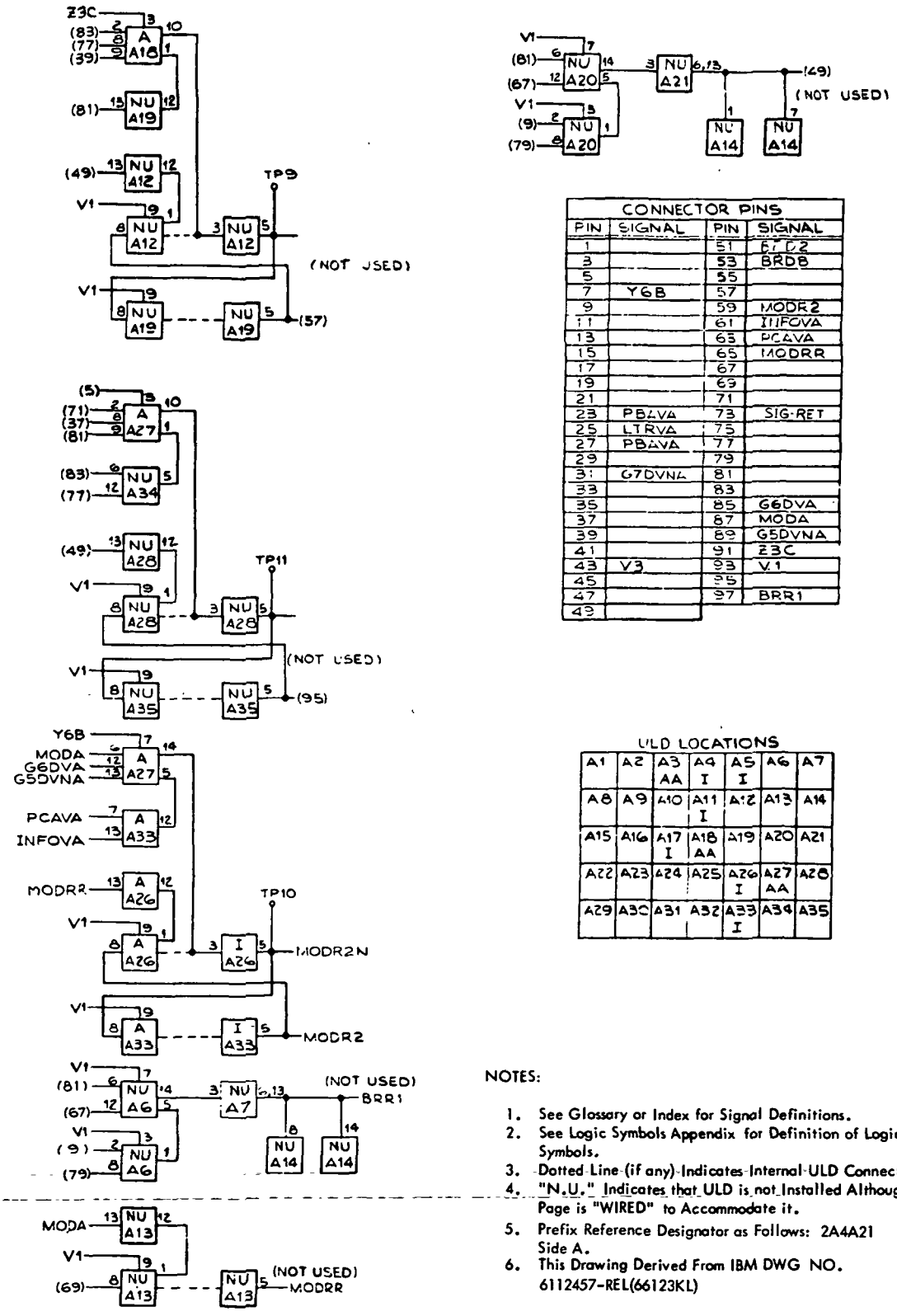


Figure 10-26. Buffer Register Logic Diagram (Sheet 9)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1		51	BRD2
3		53	BRD8
5		55	
7	Y6B	57	
9		59	MODR2
11		61	INFOVA
13		63	PCAVA
15		65	MODRR
17		67	
19		69	
21		71	
23	PBAVA	73	SIG-RET
25	LTRVA	75	
27	PBAVA	77	
29		79	
31	G7DVNA	81	
33		83	
35		85	G6DVA
37		87	MODA
39		89	G5DVNA
41		91	Z3C
43	V3	93	V1
45		95	
47		97	BRR1
49			

ULD LOCATIONS

A1	A2	A3 AA	A4 I	A5 I	A6	A7
A8	A9	A10	A11 I	A12	A13	A14
A15	A16	A17 I	A18 AA	A19	A20	A21
A22	A23	A24	A25	A26 I	A27 AA	A28
A29	A30	A31	A32	A33 I	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A21 Side A.
6. This Drawing Derived From IBM DWG NO. 6112457-REL(66123KL)

Figure 10-26. Buffer Register Logic Diagram (Sheet 10)

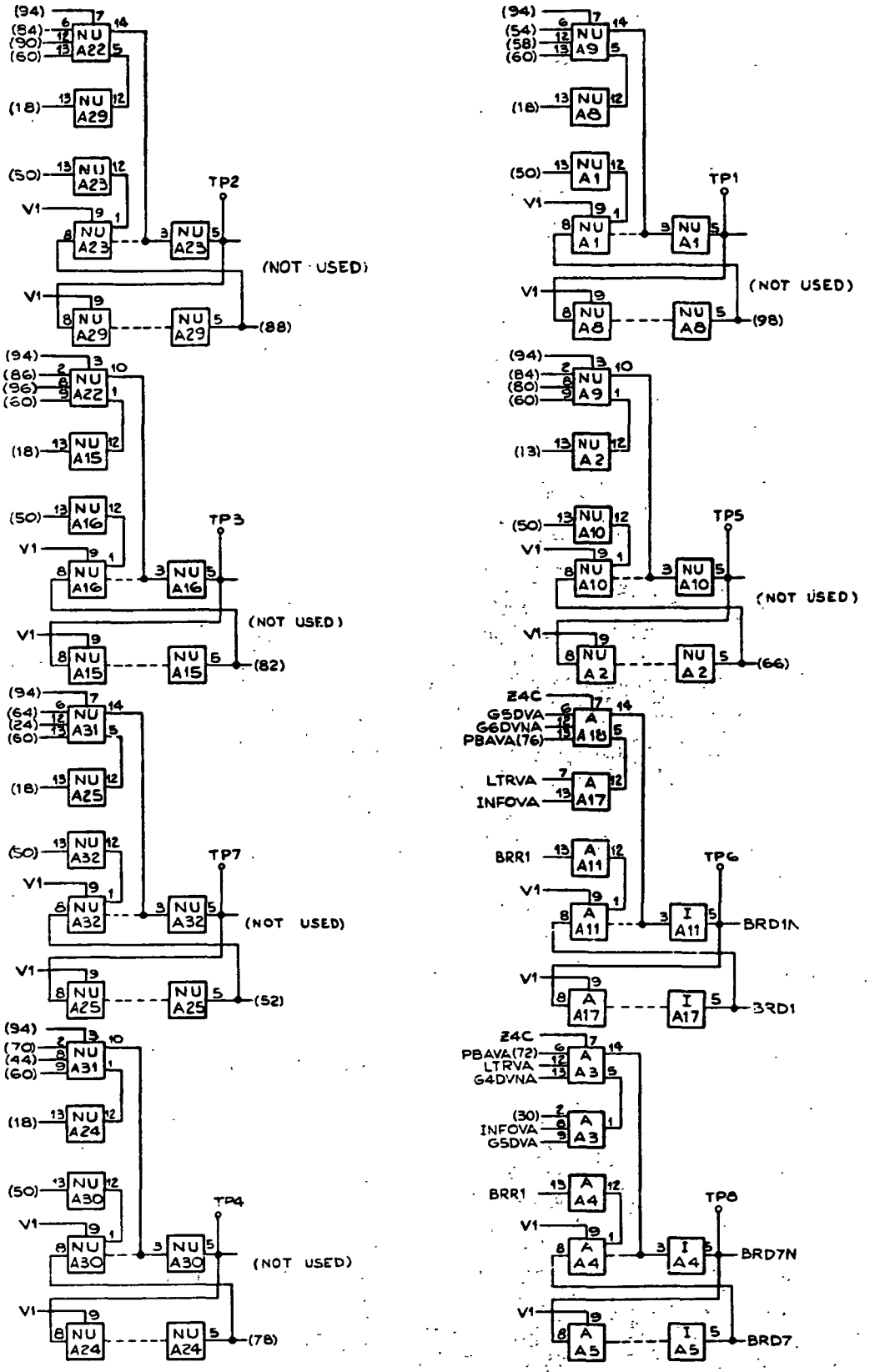
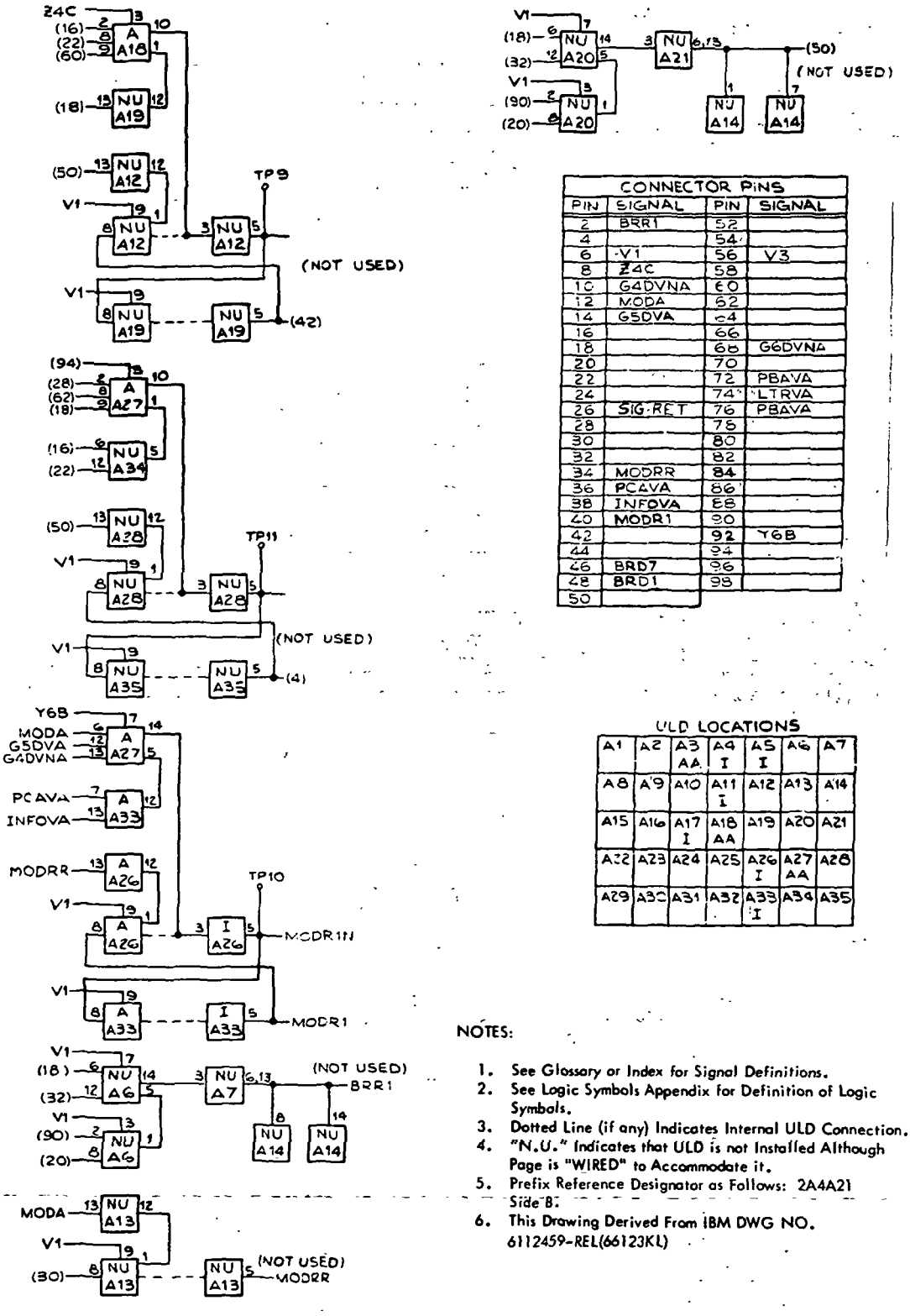


Figure 10-26. Buffer Register Logic Diagram (Sheet 11)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	BRR1	52	
4		54	
6	V1	56	V3
8	Z4C	58	
10	G4DVNA	60	
12	MODA	62	
14	G5DVA	64	
16		66	
18		68	G6DVNA
20		70	
22		72	PBAVA
24		74	LTRVA
26	SIG RET	76	PBAVA
28		78	
30		80	
32		82	
34	MODRR	84	
36	PCAVA	86	
38	INFOVA	88	
40	MODR1	90	
42		92	Y6B
44		94	
46	BRD7	96	
48	BRD1	98	
50			

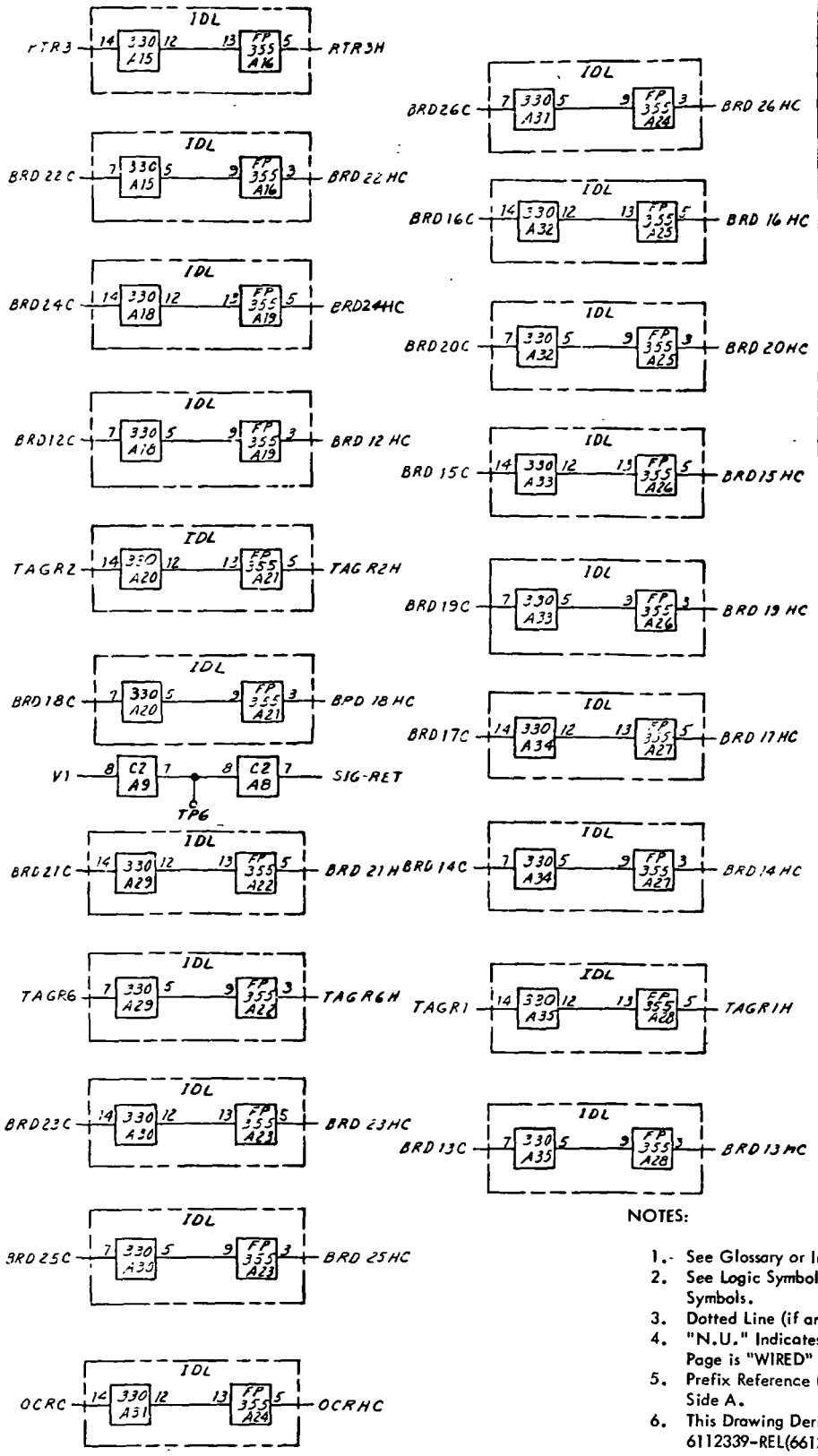
ULD LOCATIONS

A1	A2	A3 AA	A4 I	A5 I	A6	A7
A8	A9	A10	A11 I	A12	A13	A14
A15	A16	A17 I	A18 AA	A19	A20	A21
A22	A23	A24	A25	A26 I	A27 AA	A28
A29	A30	A31	A32	A33 I	A34	A35

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A21 Side B.
6. This Drawing Derived From IBM DWG NO. 6112459-REL(66123KL)

Figure 10-26. Buffer Register Logic Diagram (Sheet 12)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	RTR3H	51	BRD16HC
3	V1	53	BRD16C
5	TAG R6H	55	BRD20C
7	SIG-RET	57	BPD12HC
9		59	BRD24C
11	BRD21C	61	BRD19HC
13	BRD21HC	63	BRD12C
15	TAG R6	65	BRD15HC
17	BRD22HC	67	BRD15C
19	RTR3	69	BRD18HC
21	BRD22C	71	BRD19C
23		73	BRD14HC
25	BRD25HC	75	
27	BRD23C	77	
29	BRD23HC	79	BRD17C
31	BRD25C	81	BRD17HC
33	BRD26HC	83	BRD14C
35	V20C	85	BRD13HC
37		87	TAGR2
39	OCRC	89	BRD18C
41	OCRHC	91	TAGR1
43	BRD26C	93	TAGR1H
45	BRD24HC	95	BRD13C
47		97	TAGR2H
49	BRD20HC		

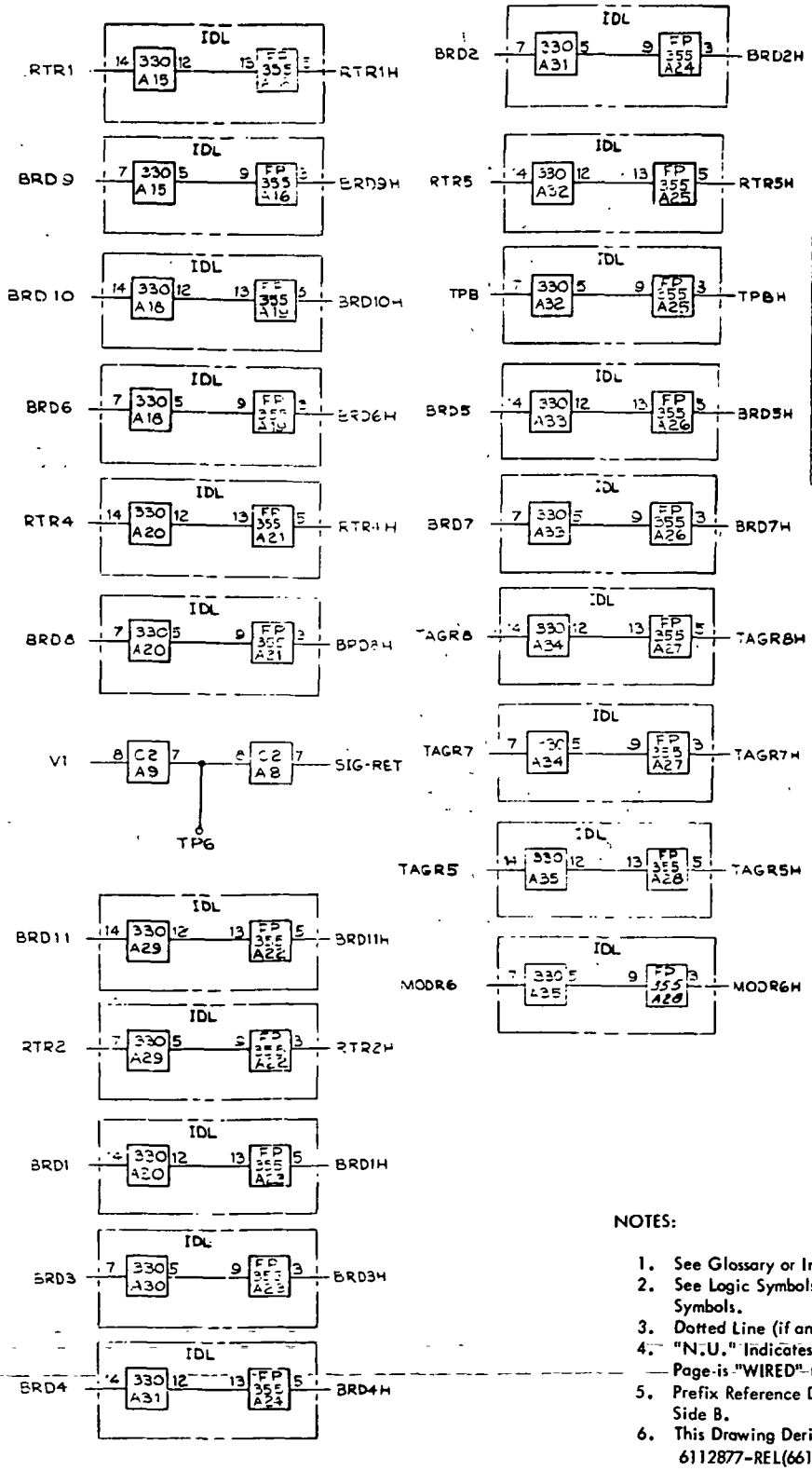
ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8 C2	A9 C2	A10	A11	A12	A13	A14
A15 330	A16 FP 355	A17	A18 330	A19 FP 355	A20 330	A21 FP 355
A22 FP 355	A23 FP 355	A24 FP 355	A25 FP 355	A26 FP 355	A27 FP 355	A28 FP 355
A29 330	A30 330	A31 330	A32 330	A33 330	A34 330	A35 330

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A13 Side A.
6. This Drawing Derived From IBM DWG NO. 6112339-REL(66123CA)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 1 of 10)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	RTR4H	52	
4	MODR6	54	BRD10H
6	TAGR5H	56	BRD2
8	TAGR5	58	BRD4H
10	BRD8	60	BRD4
12	RTR4	62	
14	MODR6H	64	V20C
16	TAGR7	66	BRD2H
18	TAGR8H	68	BRD3
20	TAGR8	70	BRD1H
22		72	BRD1
24		74	BRD3H
26	TAGR7H	76	
28	BRD7	78	BRD9
30	BRD8H	80	RTR1
32	BRD5	82	BRD9H
34	BRD5H	84	RTR2
36	BRD6	86	BRD11H
38	BRD7H	88	BRD11
40	BRD10	90	
42	BRD6H	92	SIG-RET
44	TPB	94	RTR2H
46	RTR5	96	V1
48	RTR5H	98	RTR1H
50	TPBH		

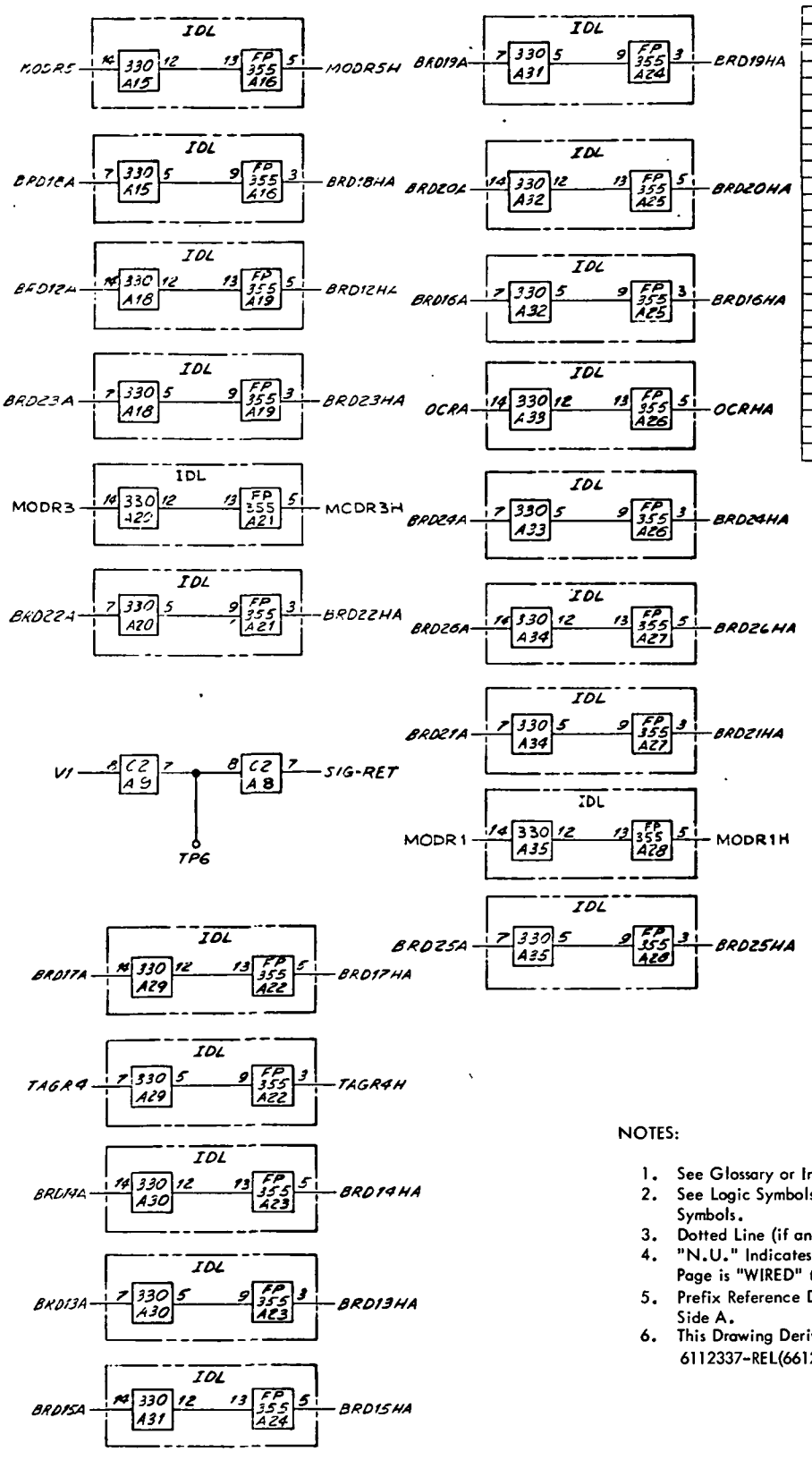
ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8 C2	A9 C2	A10	A11	A12	A13	A14
A15 330	A16 FP 355	A17	A18 330	A19 FP 355	A20 330	A21 FP 355
A22 FP 355	A23 FP 355	A24 FP 355	A25 FP 355	A26 FP 355	A27 FP 355	A28 FP 355
A29 330	A30 330	A31 330	A32 330	A33 330	A34 330	A35 330

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A13 Side B.
6. This Drawing Derived From IBM DWG NO. 6112877-REL(66123FN)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 2)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	MODR5H	51	BRD20HA
3	V1	53	BRD20A
5	TAGR4H	55	BRD16A
7	SIG-RET	57	BRD23HA
9		59	BRD12A
11	BRD17A	61	BRD24HA
13	BRD17HA	63	BRD23A
15	TAGR4	65	OCRHA
17	BRD18HA	67	OCRA
19	MCDR5	69	BRD22HA
21	BRD18A	71	BRD24A
23		73	BRD21HA
25	BRD13HA	75	
27	BRD14A	77	
29	BRD14HA	79	BRD26A
31	BRD13A	81	BRD26HA
33	BRD19HA	83	BRD21A
35	V20A	85	BRD25HA
37		87	MODR3
39	BRD15A	89	BRD22A
41	BRD15HA	91	MODR1
43	BRD19A	93	MODR1H
45	BRD12HA	95	BRD25A
47		97	MODR3H
49	BRD16HA		

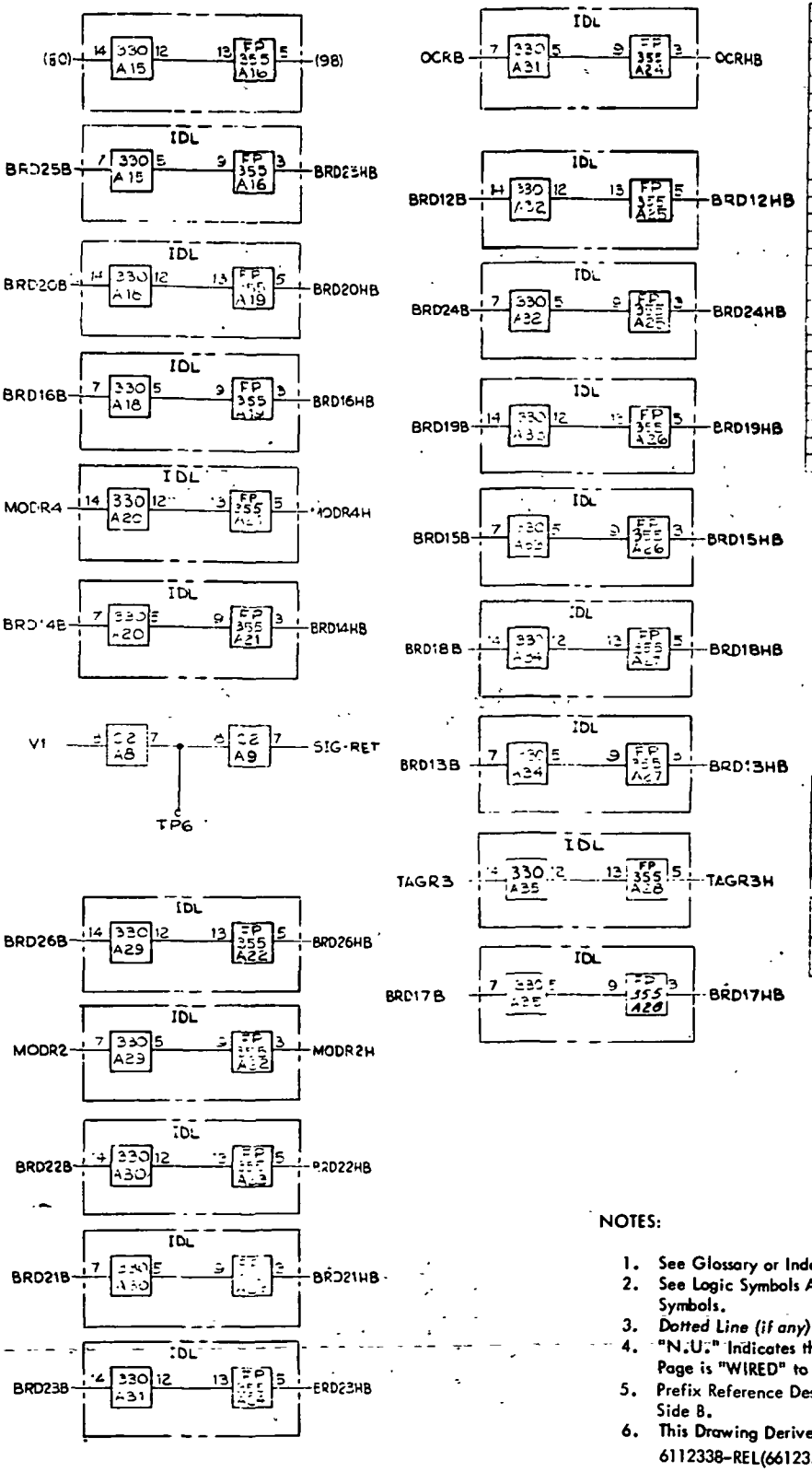
ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8 C2	A9 C2	A10	A11	A12	A13	A14
A15 330	A16 FP 355	A17	A18 330	A19 FP 355	A20 330	A21 FP 355
A22 FP 355	A23 FP 355	A24 FP 355	A25 FP 355	A26 FP 355	A27 FP 355	A28 FP 355
A29 330	A30 330	A31 330	A32 330	A33 330	A34 330	A35 330

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A22 Side A.
6. This Drawing Derived From IBM DWG NO. 6112337-REL(66123FM)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 3)



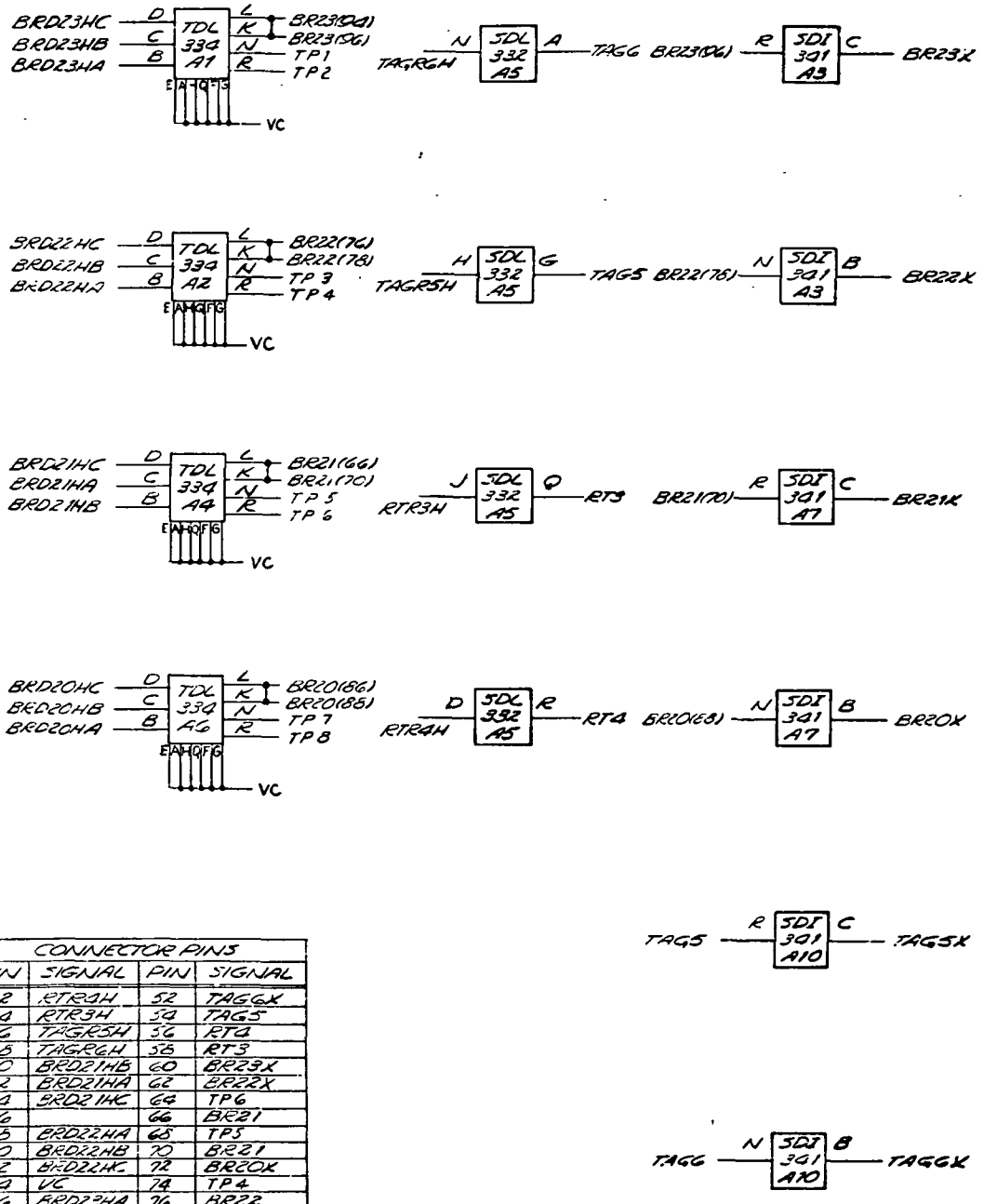
CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	MODR4H	52	
4	BRD17B	54	BRD20HB
6	TAGR3H	56	OCRB
8	TAGR3	58	BRD23HB
10	BRD14B	60	BRD23B
12	MODR4	62	
14	BRD17HB	64	V20B
16	BRD13B	66	OCRHB
18	BRD18HB	68	BRD21B
20	BRD18B	70	BRD22HB
22		72	BRD22B
24		74	BRD21HB
26	BRD13HB	76	
28	BRD15B	78	BRD25B
30	BRD14HB	80	
32	BRD19B	82	BRD25HB
34	BRD19HB	84	MODR2
36	BRD16B	86	BRD26HB
38	BRD15HB	88	BRD26B
40	BRD20B	90	
42	BRD16HB	92	SIG-RET
44	BRD24B	94	MODR2H
46	BRD12B	96	V1
48	BRD12HB	98	
50	BRD24HB		

ULD LOCATIONS						
A1	A2	A3	A4	A5	A6	A7
A8 C2	A9 C2	A10	A11	A12	A13	A14
A15 330	A16 FP 355	A17	A18 330	A19 FP 355	A20 330	A21 FP 355
A22 FP 355	A23 FP 355	A24 FP 355	A25 FP 355	A26 FP 355	A27 FP 355	A28 FP 355
A29 330	A30 330	A31 330	A32 330	A33 330	A34 330	A35 330

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. *Dotted Line (if any) Indicates Internal ULD Connection.*
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A22 Side B.
6. This Drawing Derived From IBM DWG NO. 6112338-REL(66123FM)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 4)

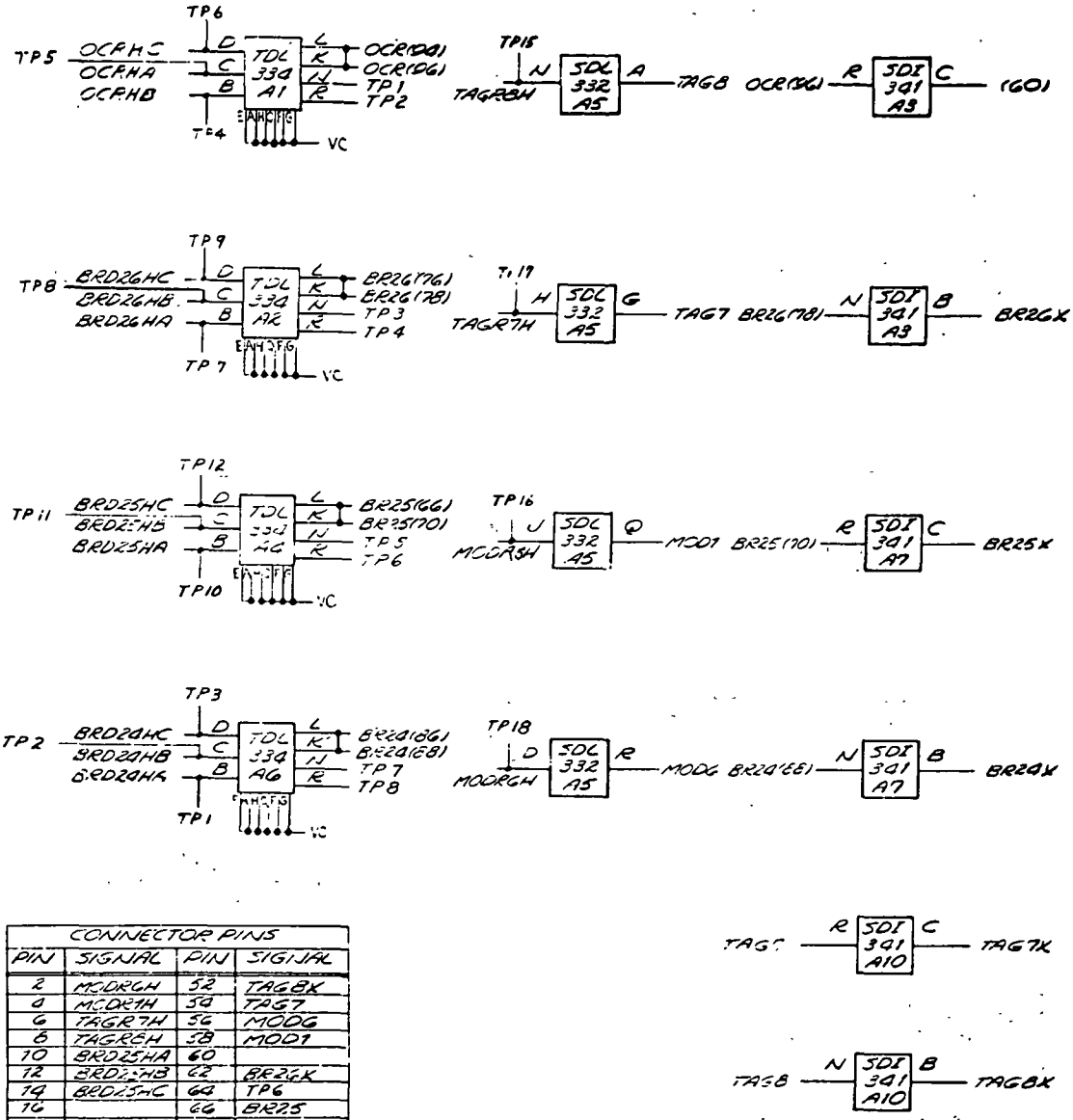


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	RTR3H	52	TAGGX
4	RTR3H	54	TAG5
6	TAGR5H	56	RT4
8	TAGRGH	58	RT3
10	BRD21HB	60	BR23X
12	BRD21HA	62	BR22X
14	BRD21HC	64	TP6
16		66	BR21
18	BRD22HA	68	TP5
20	BRD22HB	70	BR221
22	BRD22HC	72	BR20X
24	VC	74	TP4
26	BRD23HA	76	BR22
28	BRD23HB	78	BR22
30	BRD23HC	80	TP3
32	VC	82	BR21X
34	VEE	84	TP8
36	VEE	86	BR20
38	BRD2CHA	88	BR20
40	BRD2CHB	90	TP7
42	BRD2CHC	92	TP2
44	V7	94	BR23
46	SIG-RET	96	BR23
48	TAGG	98	TP1
50	TAG5X		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A12.
6. This Drawing Derived From IBM DWG NO. 6112747-B(66126BS)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 5)

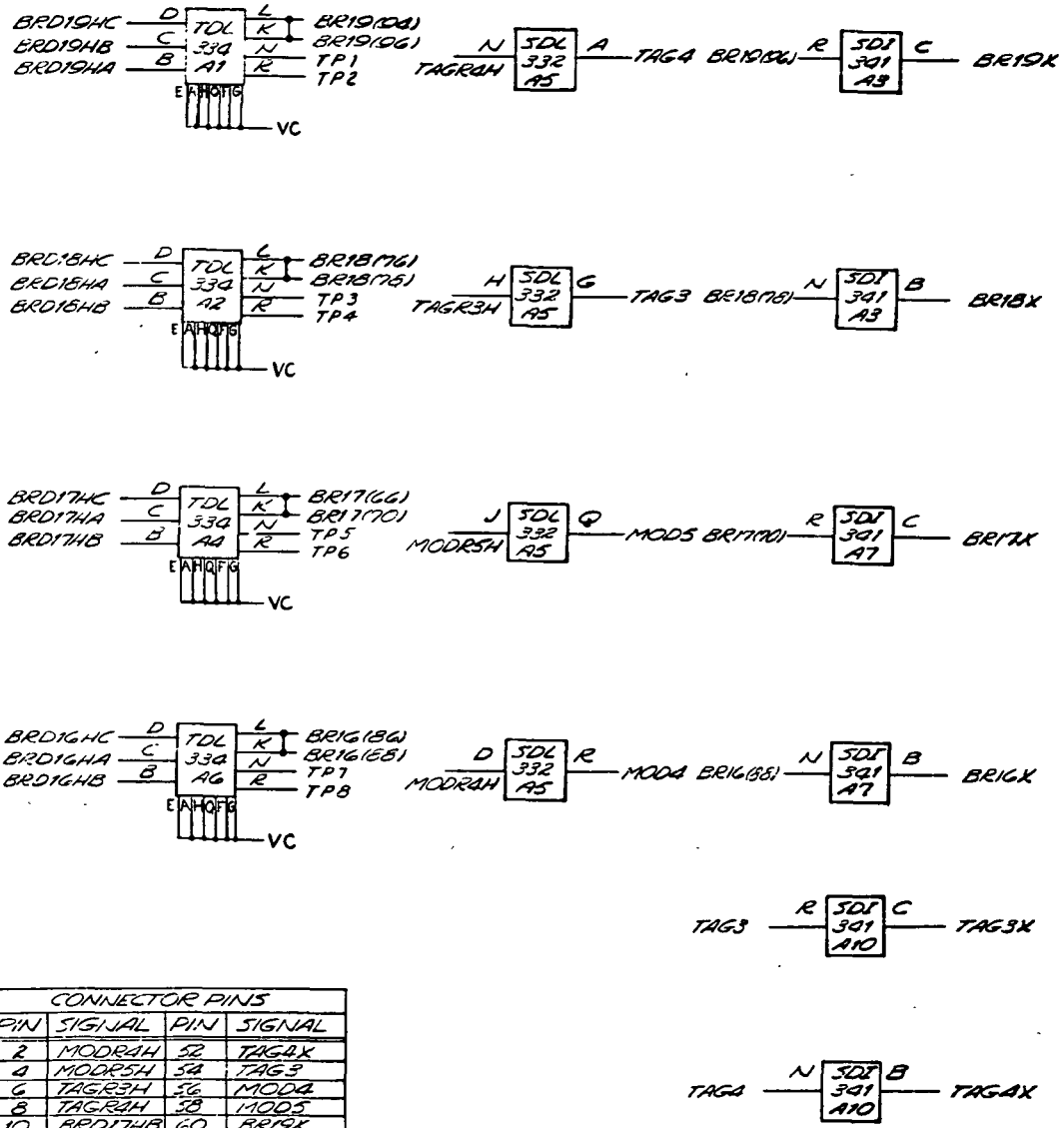


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	MODRGH	52	TAGBX
4	MODRAH	54	TAG7
6	TAGR7H	56	MODG
8	TAGRBH	58	MOD1
10	BRD25HA	60	
12	BRD25HB	62	BR26X
14	BRD25HC	64	TP6
16		66	BR25
18	BRD26HA	68	TP5
20	BRD26HB	70	BR25
22	BRD26HC	72	BR24X
24	VC	74	TP4
26	OCPHB	76	BR26
28	OCRHA	78	BR26
30	OCRHC	80	TP3
32	VC	82	BR32X
34	VEE	84	TP8
36	VEE	86	BR24
38	BRD24HA	88	BR24
40	BRD24HB	90	TP7
42	BRD24HC	92	TP2
44	V7	94	OCR
46	SIG.RET	96	OCR
48	TAGB	98	TP1
50	TAG7X		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix-Reference-Designator as Follows: 2A8A16.
6. This Drawing Derived From IBM DWG NO. 6112748-B(66126BR)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 6)

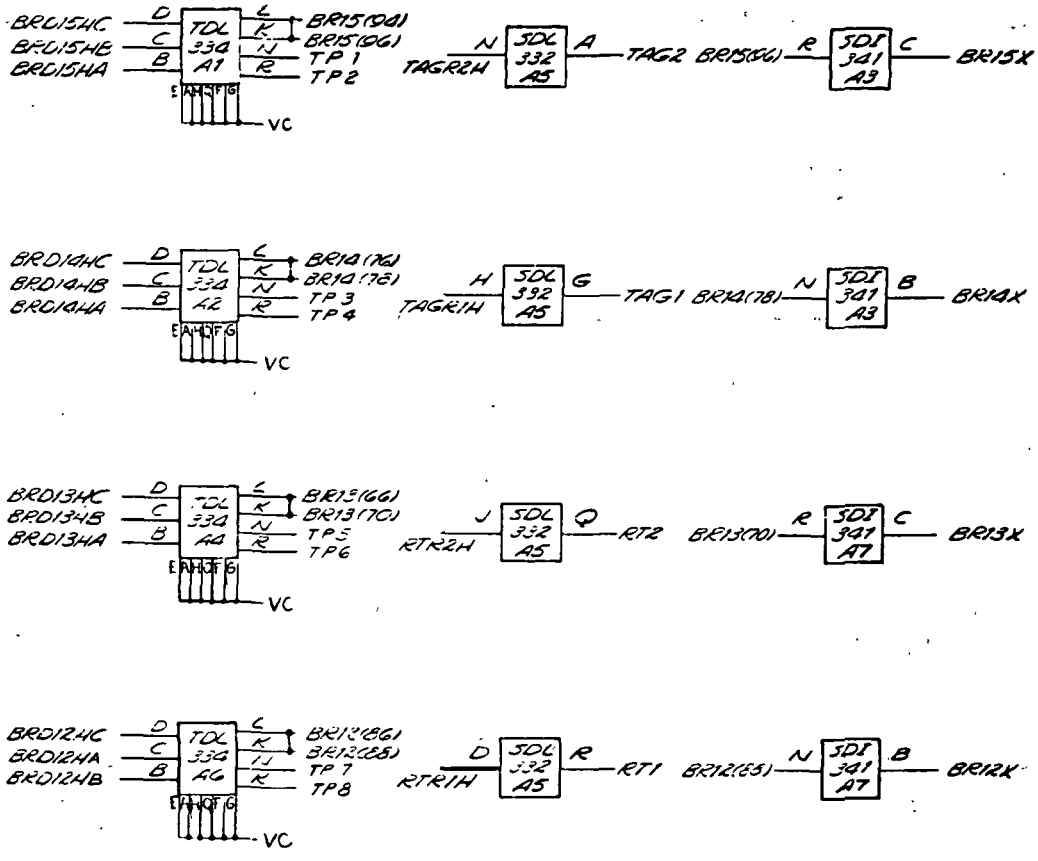


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	MODR4H	52	TAG4X
4	MODR5H	54	TAG3
6	TAGR3H	56	MOD4
8	TAGR4H	58	MOD5
10	BRD17HB	60	BR19X
12	BRD17HA	62	BR18X
14	BRD17HC	64	TP6
16		66	BR17
18	BRD18HB	68	TP5
20	BRD18HA	70	BR17
22	BRD18HC	72	BR16X
24	VC	74	TP4
26	BRD19HA	76	BR18
28	BRD19HB	78	BR18
30	BRD19HC	80	TP3
32	VC	82	BR17X
34	VEE	84	TP8
36	VEE	86	BR16
38	BRD16HB	88	BR16
40	BRD16HA	90	TP7
42	BRD16HC	92	TP2
44	V7	94	BR19
46	SIG.RET	96	BR19
48	TAG4	98	TP1
50	TAG3X		

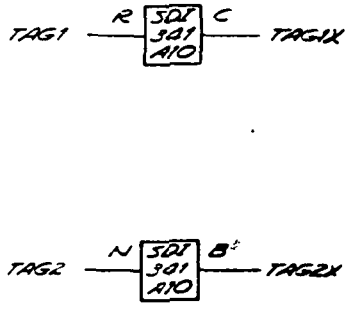
NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A21.
6. This Drawing Derived From IBM DWG NO. 6112749-B(66126BS)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 7)



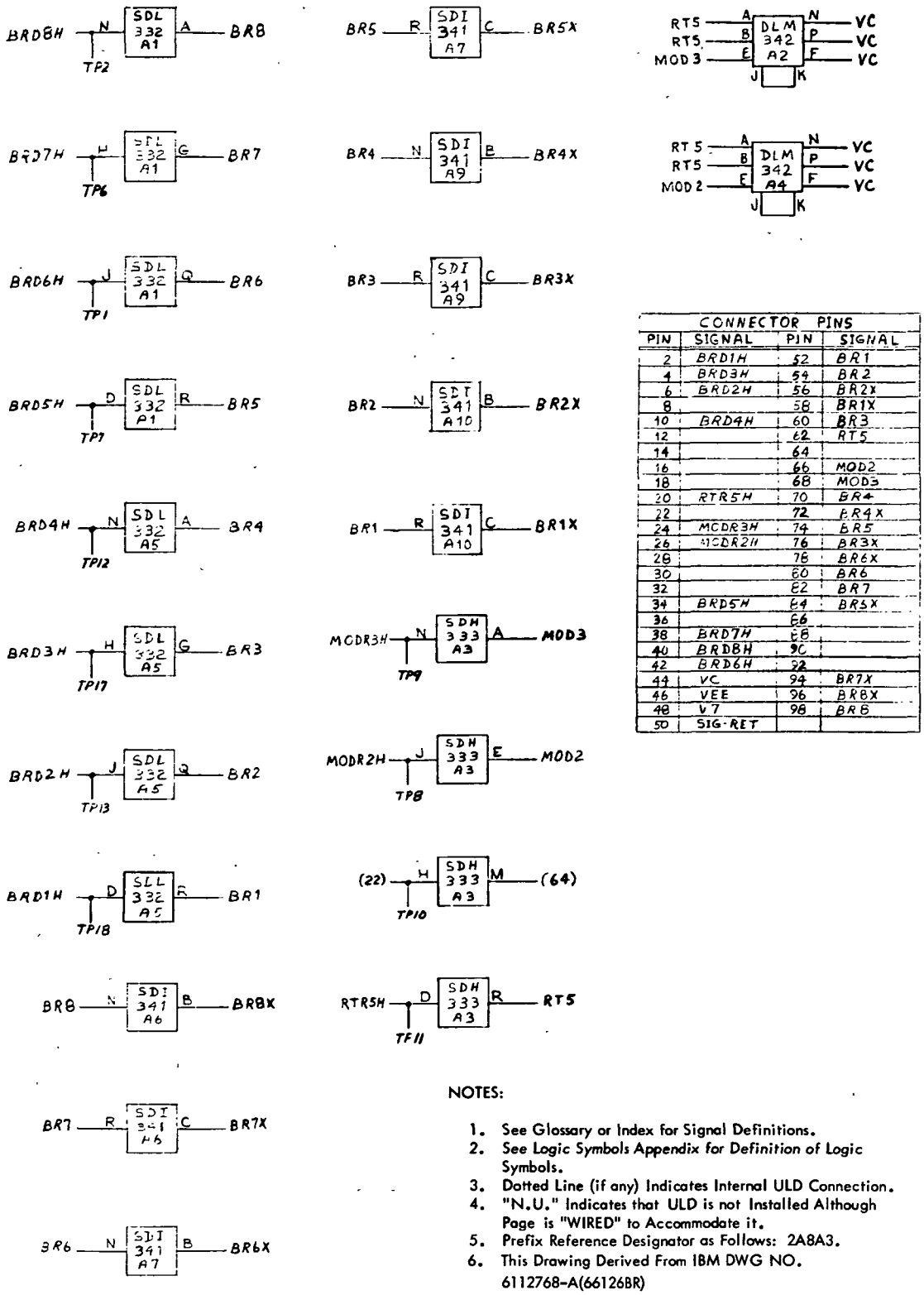
CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	RTR1H	52	TAGR2
4	RTR2H	54	TAG1
6	TAGR1H	56	RT1
8	TAGR2H	58	RT2
10	BRD13H4A	60	BR15X
12	BRD13H4B	62	BR14X
14	BRD13H4C	64	TP6
16		66	BR13
18	BRD14H4A	68	TP5
20	BRD14H4B	70	BR13
22	BRD14H4C	72	BR12X
24	VC	74	TP4
26	BRD15H4A	76	BR14
28	BRD15H4B	78	BR14
30	BRD15H4C	80	TP3
32	VC	82	BR13X
34	VEE	84	TP8
36	VEE	86	BR12
38	BRD12H4B	88	BR12
40	BRD12H4A	90	TP7
42	BRD12H4C	92	TP2
44	V7	94	BR15
46	SIG RET	96	BR15
48	TAG2	98	TP1
50	TAG1X		



NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2ABA25.
6. This Drawing Derived From IBM DWG NO. 6112757-B(66126BS)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 8)

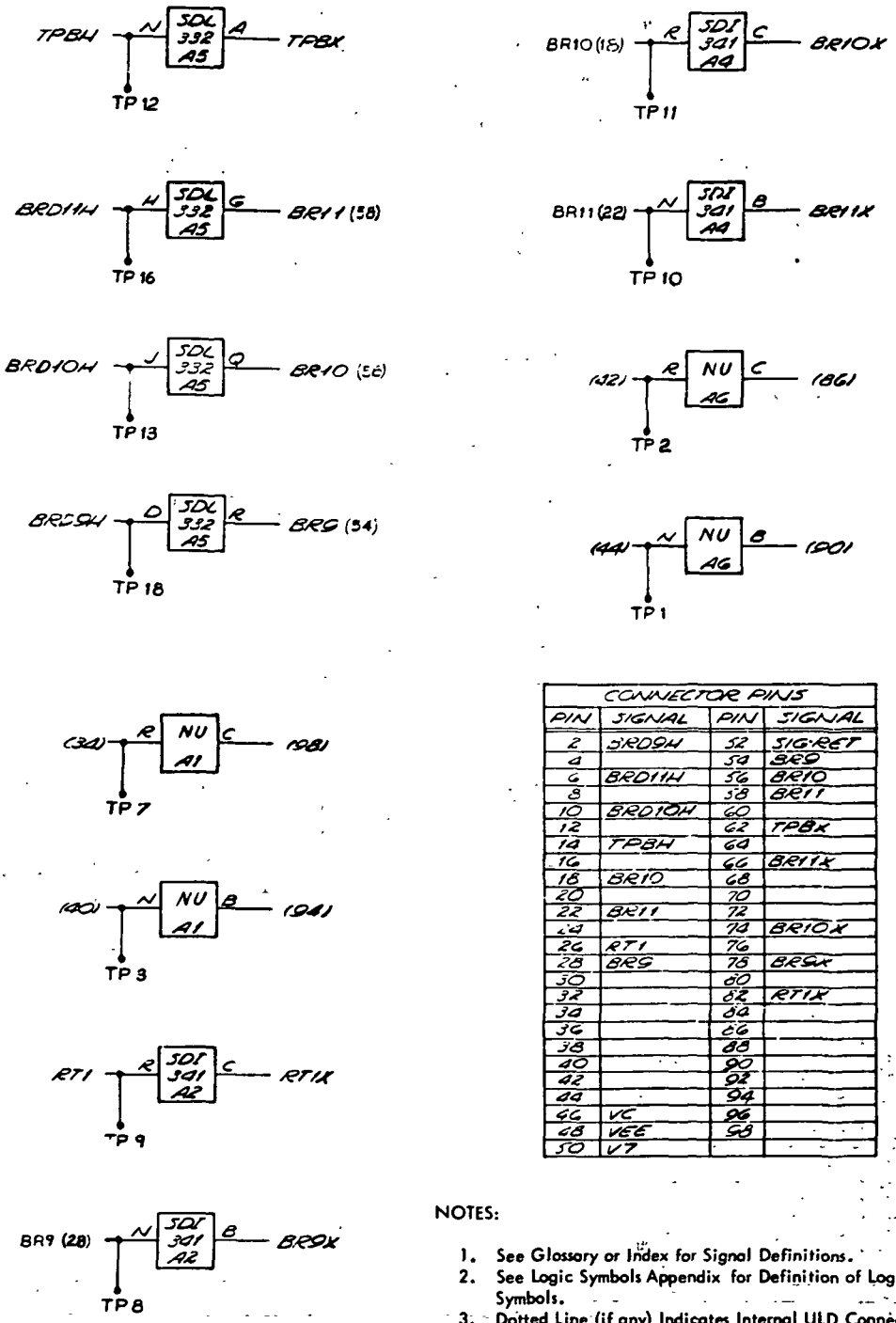


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	BRD1H	52	BR1
4	BRD3H	54	BR2
6	BRD2H	56	BR2X
8		58	BR1X
10	BRD4H	60	BR3
12		62	RT5
14		64	
16		66	MOD2
18		68	MOD3
20	RTR5H	70	BR4
22		72	BR4X
24	MODR3H	74	BR5
26	MODR2H	76	BR3X
28		78	BR6X
30		80	BR6
32		82	BR7
34	BRD5H	84	BR5X
36		86	
38	BRD7H	88	
40	BRD8H	90	
42	BRD6H	92	
44	VC	94	BR7X
46	VEE	96	BR8X
48	V7	98	BR8
50	SIG-RET		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A3.
6. This Drawing Derived From IBM DWG NO. 6112768-A(66126BR)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 9)

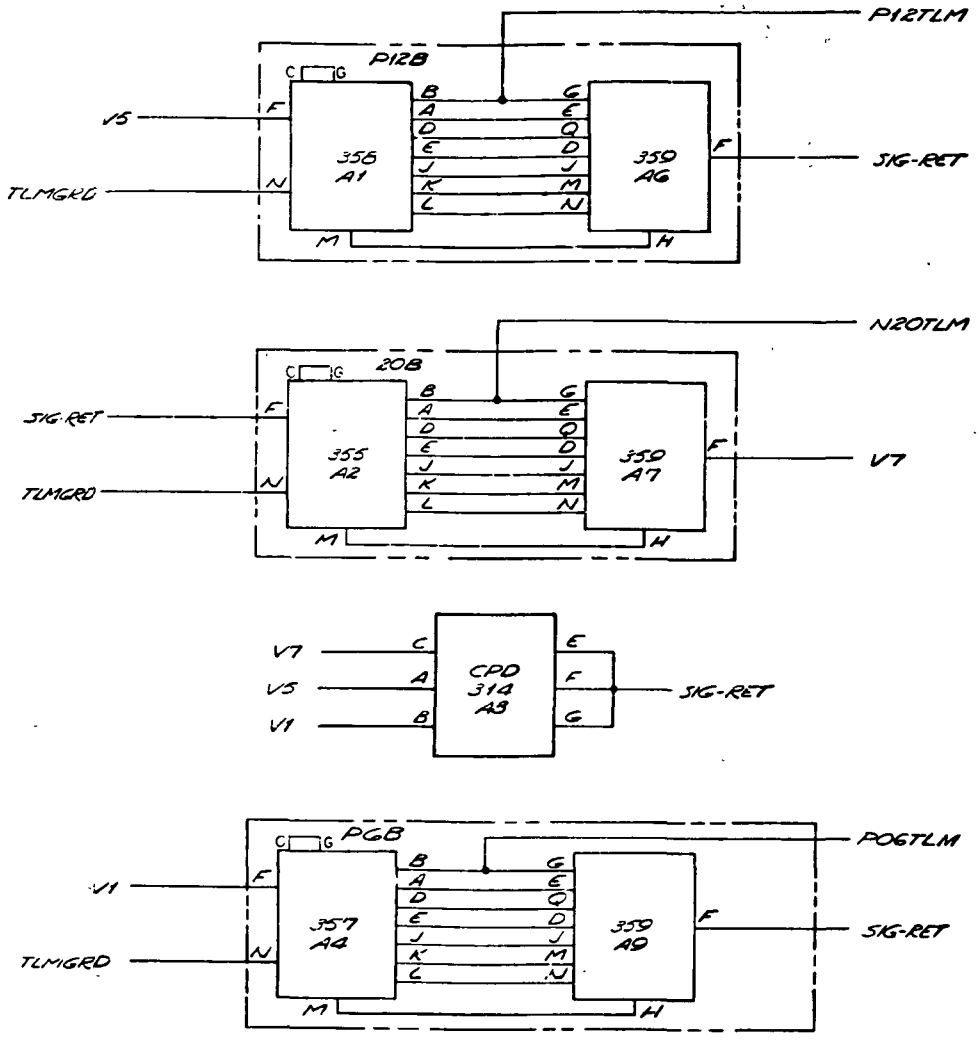


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	BRDSH	52	SIG RET
4		54	BRS
6	BRD11H	56	BR10
8		58	BR11
10	BRD10H	60	
12		62	TPBX
14	TPBH	64	
16		66	BR11X
18	BR10	68	
20		70	
22	BR11	72	
24		74	BR10X
26	RT1	76	
28	BRS	78	BRSX
30		80	
32		82	RT1X
34		84	
36		86	
38		88	
40		90	
42		92	
44		94	
46	VC	96	
48	VEE	98	
50	V7		

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A8A6.
6. This Drawing Derived From IBM DWG NO. 6112758-A(661268D)

Figure 10-27. Telemetry Register Output Drivers Logic Diagram (Sheet 10)

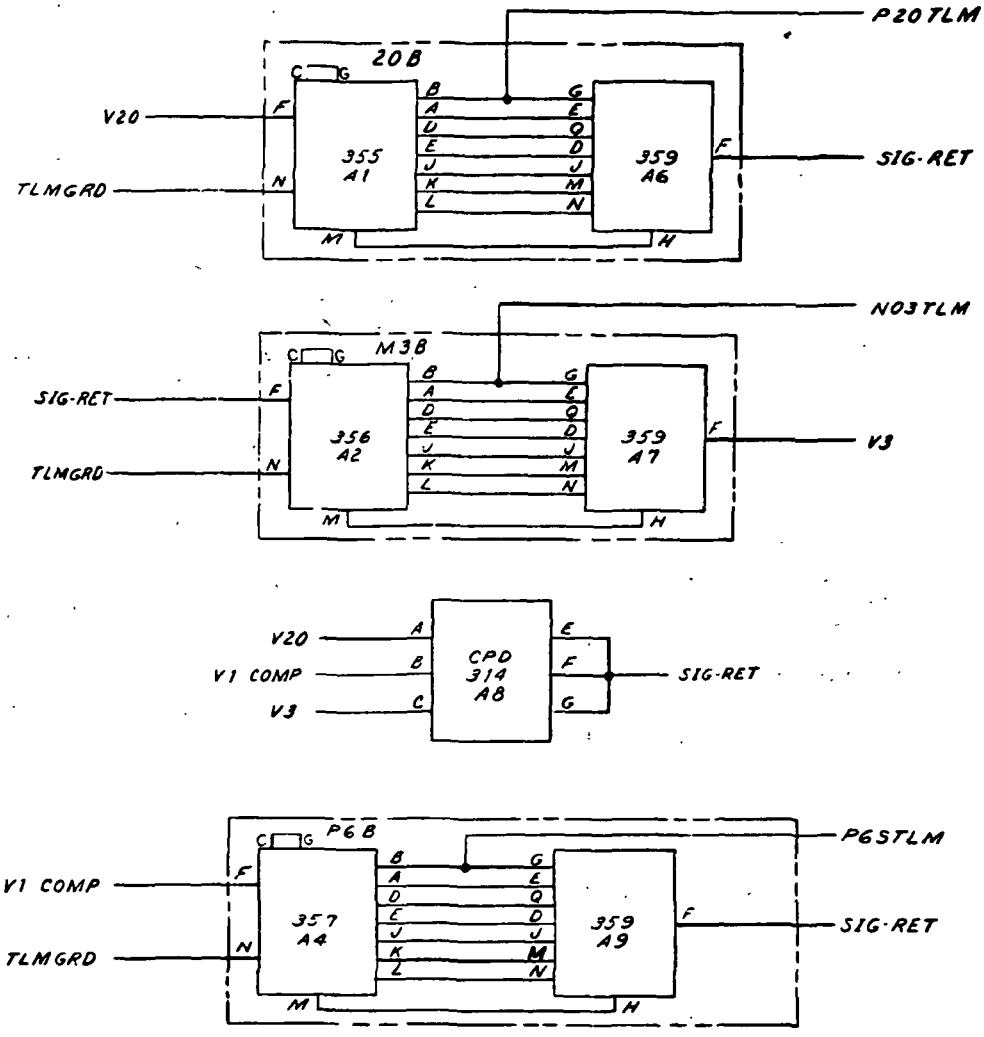


CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	V5
4		54	V7
6		56	V1
8		58	SIG-RET
10		60	SIG-RET
12		62	N20TLM
14		64	
16		66	
18		68	
20		70	
22		72	
24	P06TLM	74	
26		76	
28		78	
30		80	P12TLM
32		82	
34		84	
36		86	
38		88	
40		90	
42		92	
44		94	TLMGRD
46		96	TLMGRD
48		98	
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A25. Side A, 2A6A18 Side A Respectively.
6. This Drawing Derived From IBM DWG NO. 6112718-A(66126BD)

Figure 10-28. Telemetry Buffers Logic Diagram (Sheet 1 of 2)



CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	V20
4		54	V3
6		56	V1 COMP
8		58	SIG-RET
10		60	SIG-RET
12		62	NO3TLM
14		64	
16		66	
18		68	
20		70	
22		72	
24	P6STLM	74	
26		76	
28		78	
30		80	P20TLM
32		82	
34		84	
36		86	
38		88	
40		90	
42		92	
44		94	TLMGRD
46		96	TLMGRD
48		98	
50			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A6A28.
6. This Drawing Derived From IBM DWG NO. 6112717-A(66126BD)

Figure 10-28. Telemetry Buffers Logic Diagram (Sheet 2)

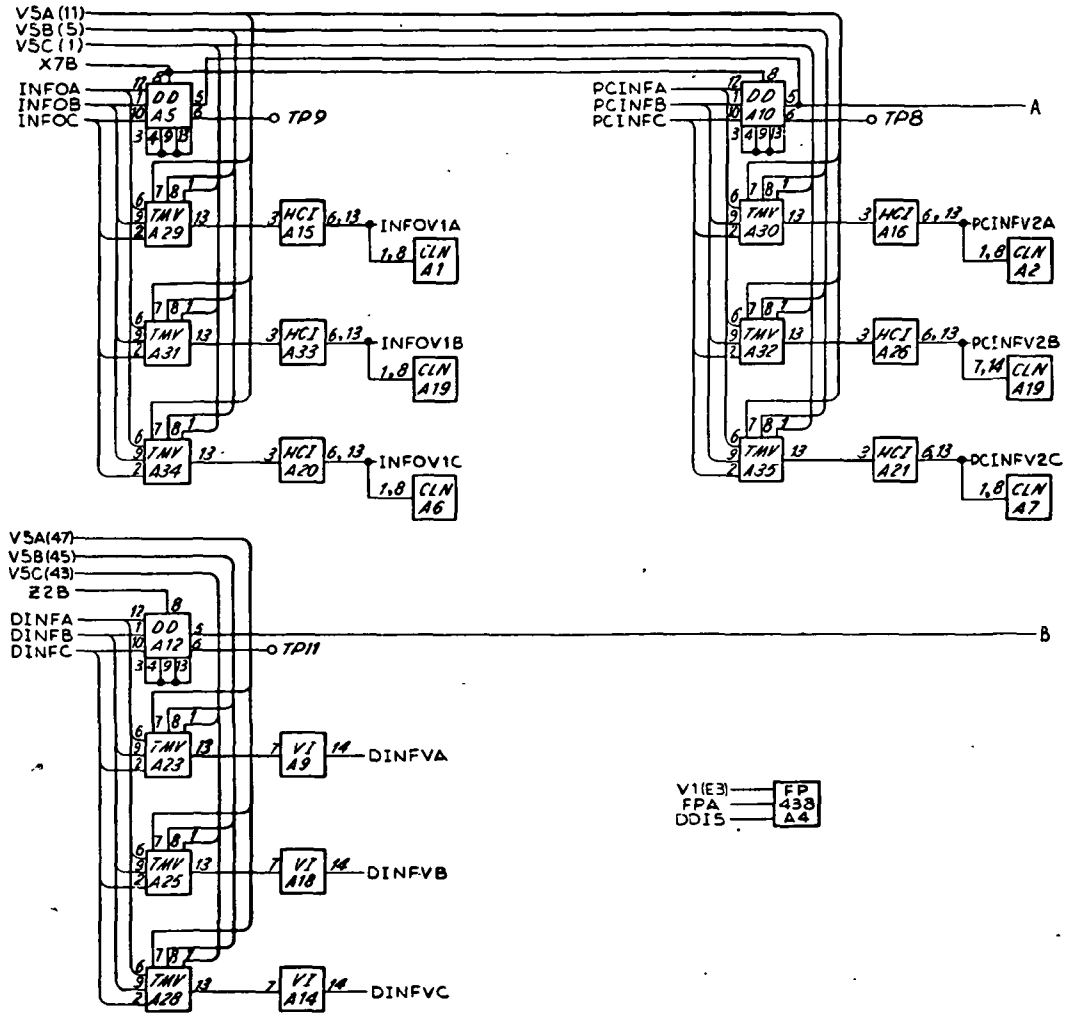
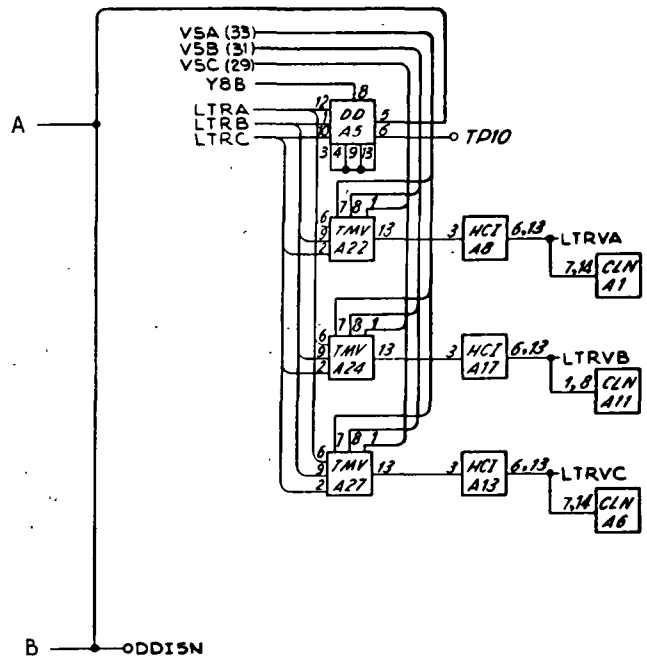


Figure 10-29. Voters Logic Diagram (Sheet 1 of 36)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1A	18	
4	V3A	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DDIS
10	V3	25	DDISN
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDIS
3	INFOB	53	
5	V5B	55	DINFB
7	INFOC	57	DINFC
9	INFOA	59	DINFA
11	V5A	61	
13		63	
15		65	
17		67	INFOV1A
19		69	INFOV1B
21	LTRVA	71	INFOV1C
23	LTRVB	73	
25	LTRVC	75	
27		77	PCINFV2B
29	V5C	79	PCINFV2A
31	V5B	81	PCINFV2C
33	V5A	83	Z2B
35	Y8B	85	
37	LTRB	87	PCINFB
39	LTRC	89	PCINFC
41	LTRA	91	PCINFA
43	V5C	93	DINFVB
45	V5B	95	DINFVA
47	V5A	97	DINFVC
49	X7B		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	FP 23B	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	VI	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A17 Side A.
6. This Drawing Derived From IBM DWG NO. 6112887-REL(66123FN)

Figure 10-29. Voters Logic Diagram (Sheet 2)

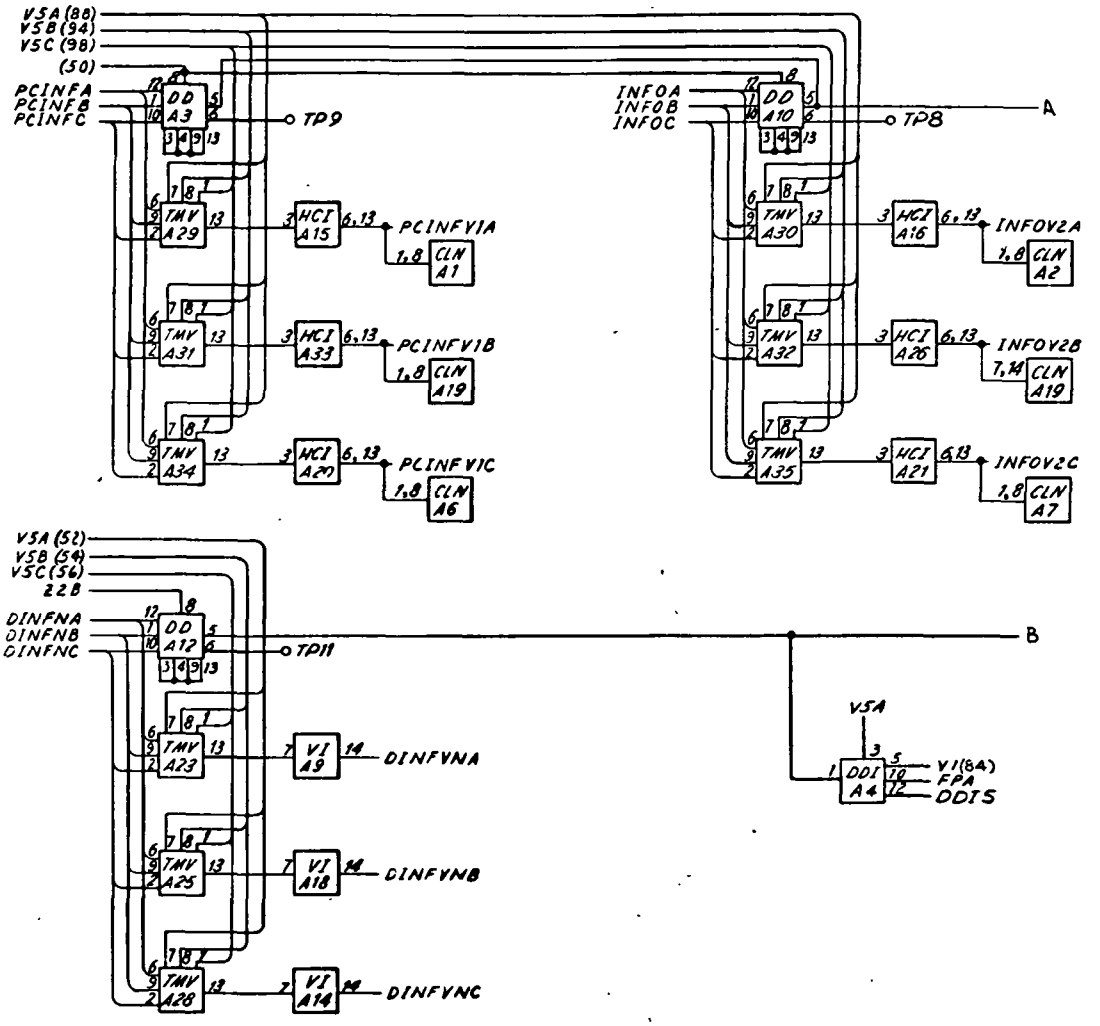
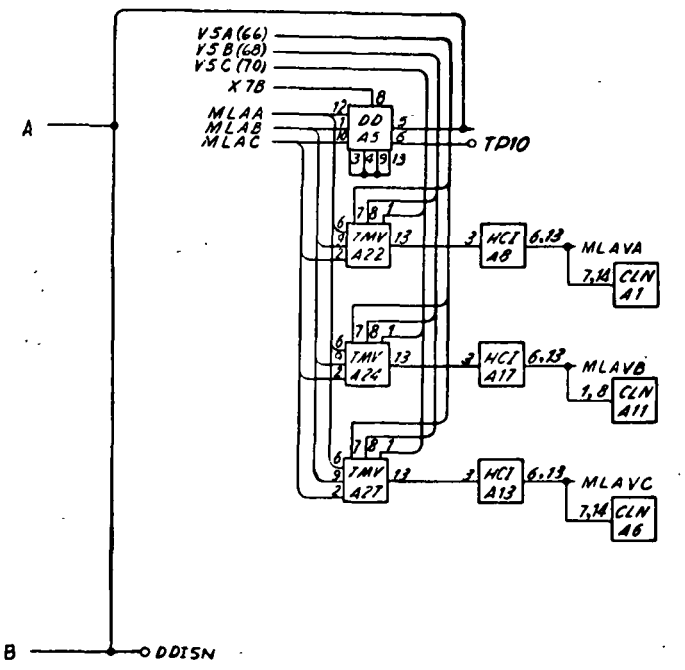


Figure 10-29. Voters Logic Diagram (Sheet 3)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(82)	17	
3	V1(84)	18	
4	V3(86)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DDIS
10	V3(38)	25	DDISN
11		26	
12		27	
13	SIG-RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	DINFVNC	52	VSA
4	DINFVNA	54	VSB
6	DINFVNB	56	VSC
8	INFOA	58	MLAA
10	INFOC	60	MLAC
12	INFOB	62	MLAB
14	SIG-RET	64	X7B
16	Z2F	66	VSA
18	INFOV2C	68	VSB
20	INFOV2A	70	VSC
22	INFOV2B	72	
24	V1	74	MLAVC
26	V3	76	MLAVB
28	PCINFVIC	78	MLAVA
30	PCINFVIB	80	
32	PCINFVIA	82	SIG-RET
34	SIG-RET	84	V1
36	V1	86	V3
38	V3	88	VSA
40	DINFNA	90	PCINFA
42	DINFNC	92	PCINFC
44	DINFNB	94	VSB
46		96	PCINFB
48	VSA	98	VSC
50			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DDI	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	VI	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A17 Side B.
6. This Drawing Derived From IBM DWG NO. 6112917-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 4)

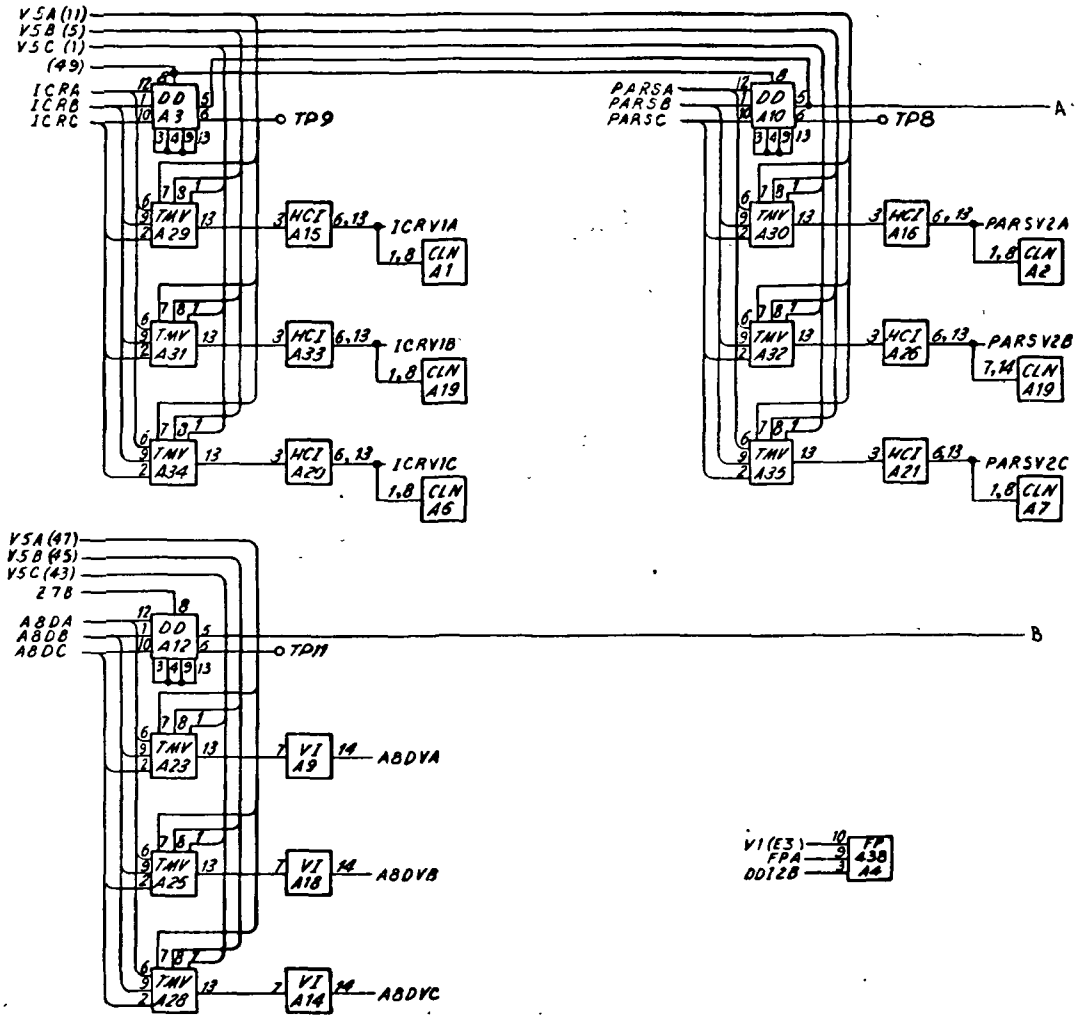
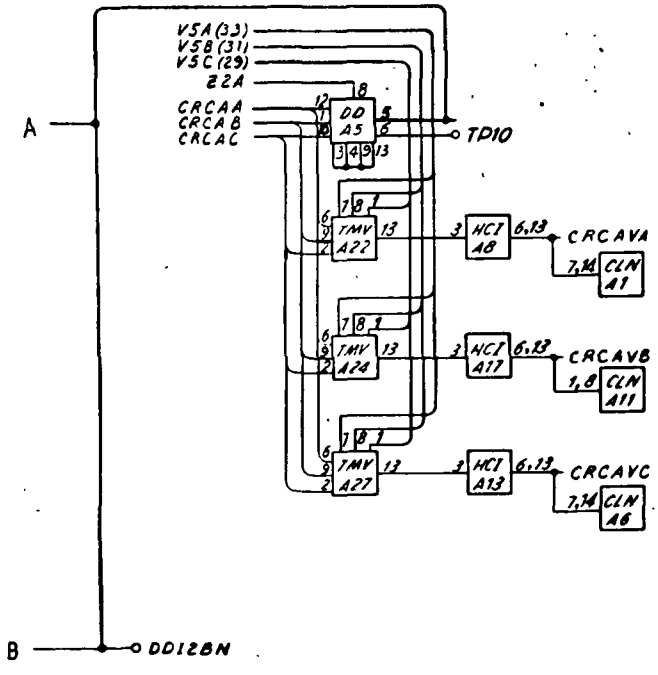


Figure 10-29. Voters Logic Diagram (Sheet 5)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DD12B
10	V3	25	DD12BN
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DD12B
3	ICRB	53	
5	V5B	55	ABDB
7	ICRC	57	ABDC
9	ICRA	59	ABDA
11	V5A	61	
13		63	
15		65	
17		67	ICRV1A
19		69	ICRV1B
21	CRCAVA	71	ICRV1C
23	CRCAVB	73	
25	CRCAVC	75	
27		77	PARSV2B
29	V5C	79	PARSV2A
31	V5B	81	PARSV2C
33	V5A	83	27B
35	22A	85	
37	CRCAB	87	PARSB
39	CRCAC	89	PARSC
41	CRCAA	91	PARSA
43	V5C	93	ABDVB
45	V5B	95	ABDVA
47	V5A	97	ABDVC
49			

ULD LOCATIONS

A1 CLN	A2 CLN	A3 DD	A4 FP A38	A5 DD	A6 CLN	A7 CLN
A8 HCI	A9 V1	A10 DD	A11 CLN	A12 DD	A13 HCI	A14 V1
A15 HCI	A16 HCI	A17 HCI	A18 V1	A19 CLN	A20 HCI	A21 HCI
A22 TMV	A23 TMV	A24 TMV	A25 TMV	A26 HCI	A27 TMV	A28 TMV
A29 TMV	A30 TMV	A31 TMV	A32 TMV	A33 HCI	A34 TMV	A35 TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A4 Side A.
6. This Drawing Derived From IBM DWG NO. 6112888-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 6)

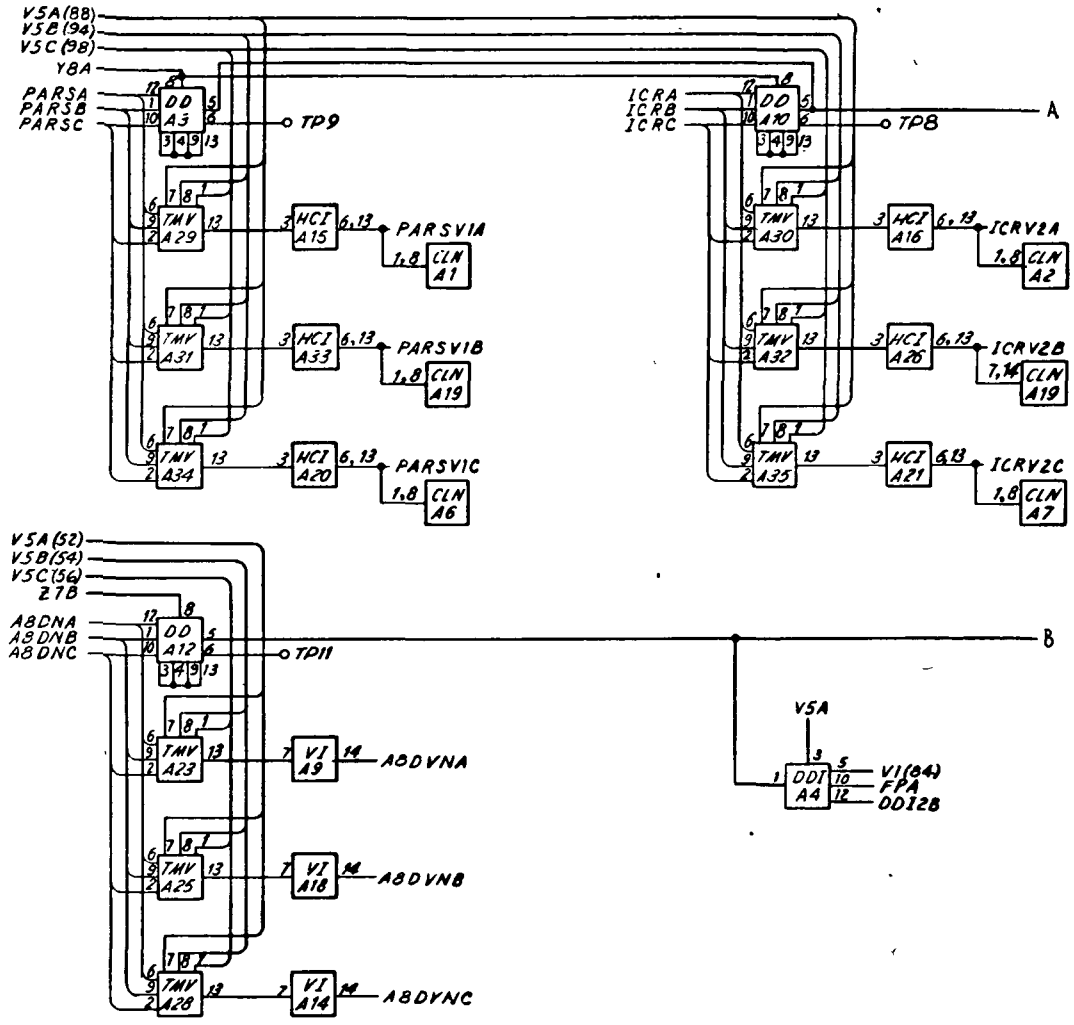
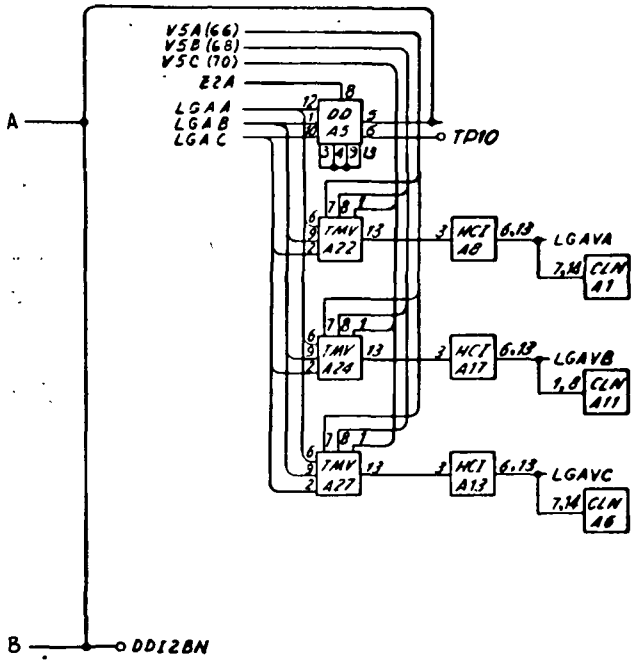


Figure 10-29. Voters Logic Diagram (Sheet 7)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(82)	17	
3	V1(84)	18	
4	V3(86)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DD12C
10	V3(38)	25	DD12BN
11		26	
12		27	
13	SIG-RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	ABDVNC	52	VSA
4	ABDVNA	54	VSB
6	ABDVNB	56	VSC
8	ICRA	58	LGAA
10	ICRC	60	LGAC
12	ICRB	62	LGAB
14	SIG-RET	64	Z2A
16	Z7E	66	VSA
18	ICRV2C	68	VSB
20	ICRV2A	70	VSC
22	ICRV2B	72	
24	V1	74	LGAVC
26	V3	76	LGAVB
28	PARSVIC	78	LGAVA
30	PARSV1B	80	
32	PARSV1A	82	SIG-RET
34	SIG RET	84	V1
36	V1	86	V3
38	V3	88	VSA
40	ABDNA	90	PARSA
42	ABDNC	92	PARSC
44	ABDNB	94	VSB
46		96	PARSB
48	VSA	98	VSC
50	VBA		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DD1	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	VI	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A4 Side B.
6. This Drawing Derived From IBM DWG NO. 6112918-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 8)

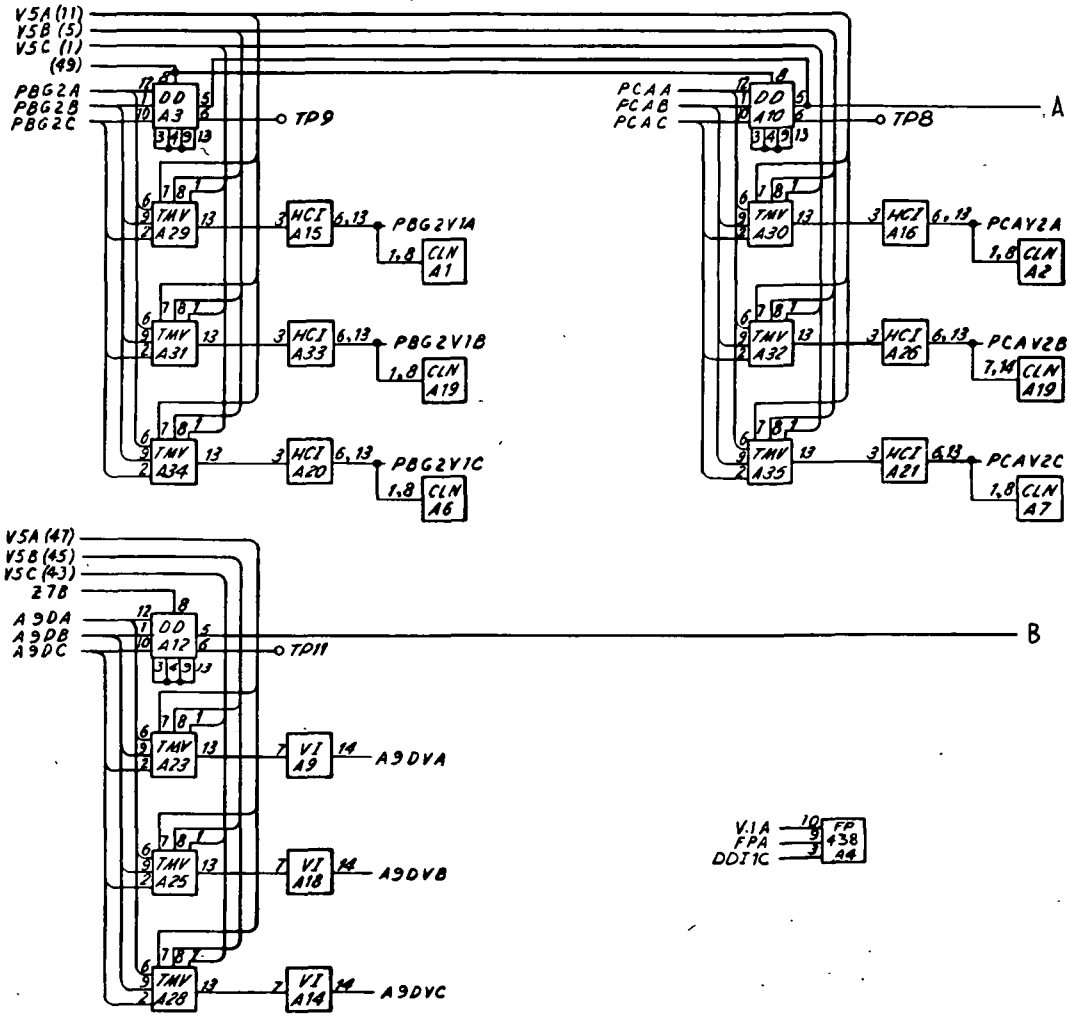
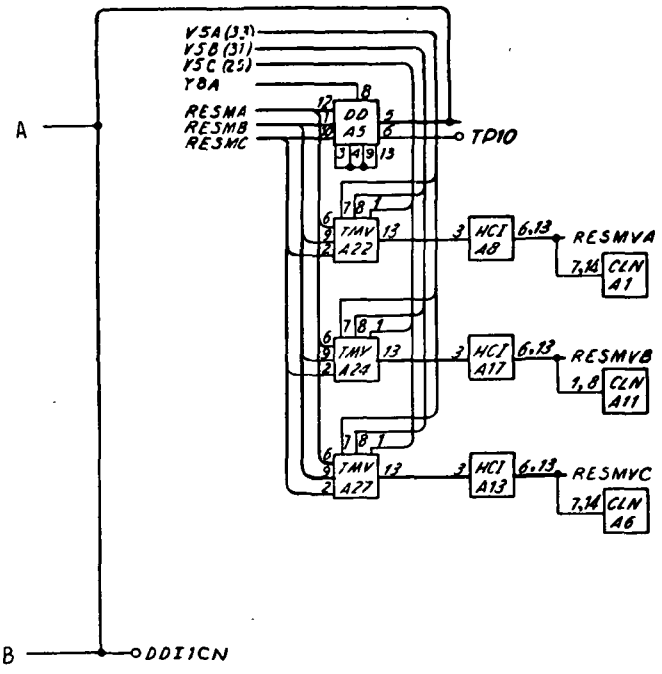


Figure 10-29. Voters Logic Diagram (Sheet 9)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DDI1C
10	V3	25	DDI1CN
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDI1C
3	PBG2B	53	
5	V5B	55	A9DB
7	PBG2C	57	A9DC
9	PBG2A	59	A9DA
11	V5A	61	
13		63	
15		65	
17		67	PBG2V1A
19		69	PBG2V1B
21	RESMVA	71	PBG2V1C
23	RESMVB	73	
25	RESMVC	75	
27		77	PCAV2B
29	V5C	79	PCAV2A
31	V5B	81	PCAV2C
33	V5A	83	27B
35	Y8A	85	
37	RESMB	87	PCAB
39	RESMC	89	PCAC
41	RESMA	91	PCAA
43	V5C	93	A9DVB
45	V5B	95	A9DVA
47	V5A	97	A9DVC
49			

ULD LOCATIONS

A1	A2	A3	A4 FP	A5	A6	A7
CLN	CLN	DD	438	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A9 Side A.
6. This Drawing Derived From IBM DWG NO. 6112889-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 10)

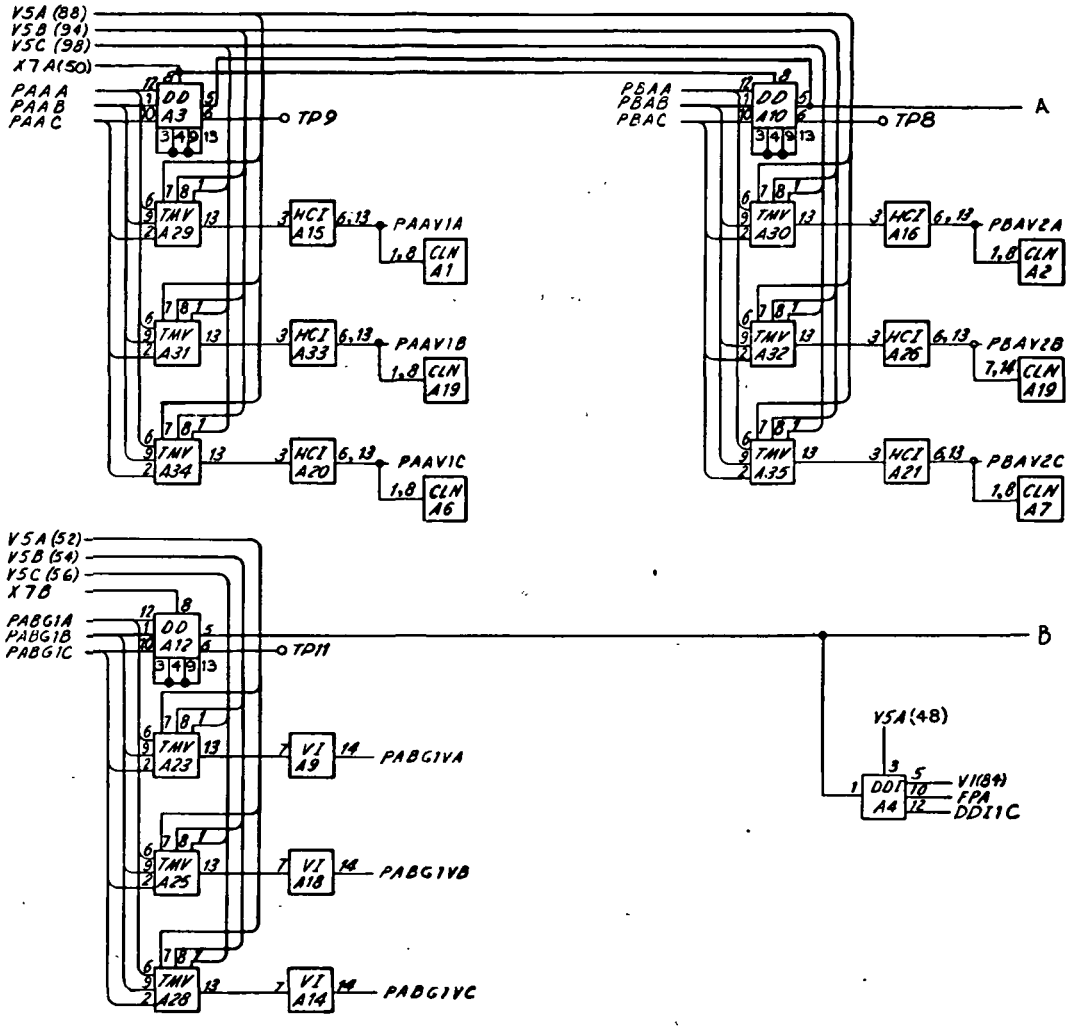
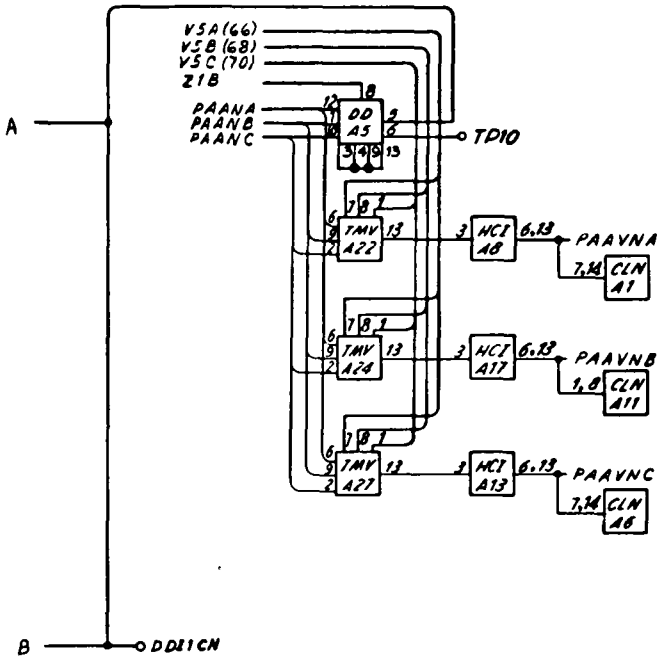


Figure 10-29. Voters Logic Diagram (Sheet 11)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(02)	17	
3	V1(04)	18	
4	V3(06)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DDI1C
10	V3(38)	25	DDI1CN
11		26	
12		27	
13	SIG-RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	PABG1VC	52	VSA
4	PABG1VA	54	VSB
6	PABG1VB	56	VSC
8	PBAA	58	PAANA
10	PBAC	60	PAANC
12	PBAB	62	PAANB
14	SIG-RET	64	Z1B
16	X7B	66	VSA
18	PBAV2C	68	VSB
20	PBAV2A	70	VSC
22	PBAV2B	72	
24	V1	74	PAAVNC
26	V3	76	PAAVNB
28	PAAV1C	78	PAAVNA
30	PAAV1B	80	
32	PAAV1A	82	SIG-RET
34	SIG-RET	84	V1
36	V1	86	V3
38	V3	88	VSA
40	PABG1A	90	PAAA
42	PABG1C	92	PAAC
44	PABG1B	94	VSB
46		96	PAAB
48	VSA	98	VSC
50	X7A		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DD1	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A9 Side B.
6. This Drawing Derived From IBM DWG NO. 6112919-REL(66123FN)

Figure 10-29. Voters Logic Diagram (Sheet 12)

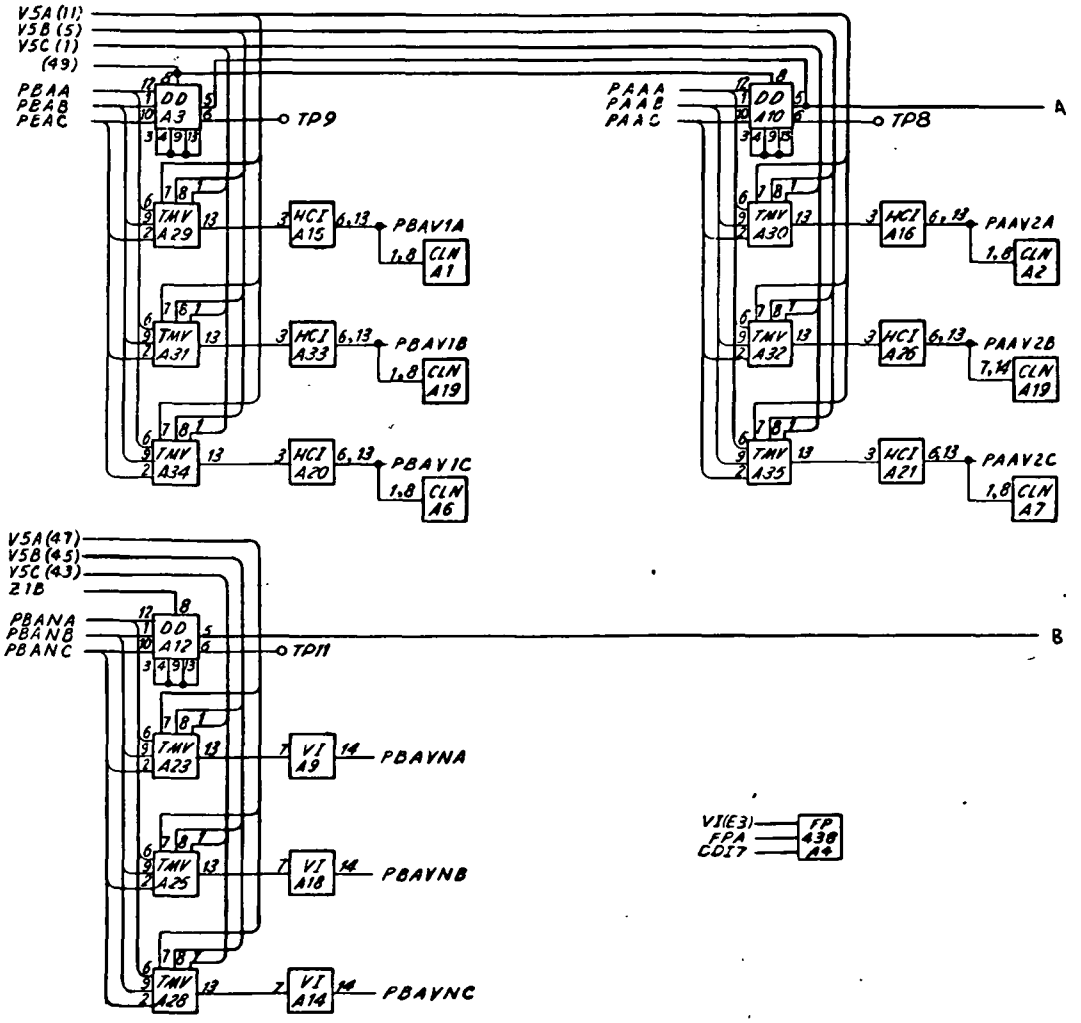
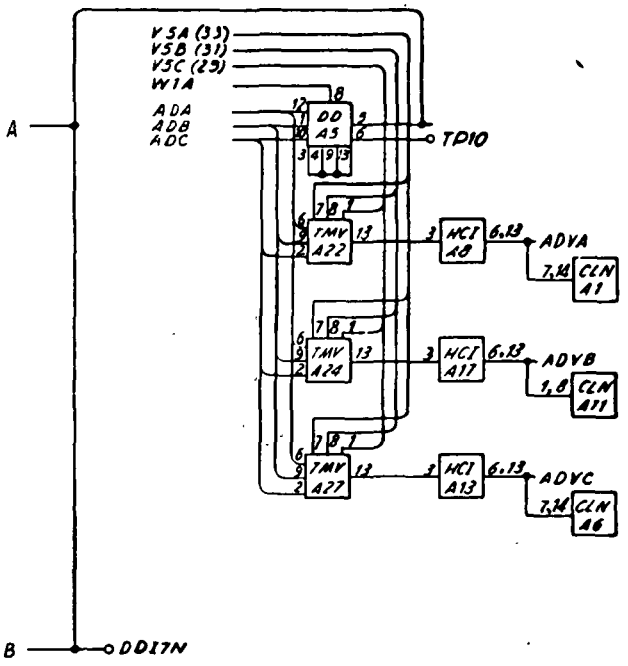


Figure 10-29. Voters Logic Diagram (Sheet 13)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DDI7
10	V3	25	DDI7N
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDI7
3	PBAB	53	
5	V5E	55	PBANB
7	PBAC	57	PBANC
9	PBAA	59	PBANA
11	V5A	61	
13		63	
15		65	
17		67	PBAV1A
19		69	PBAV1B
21	ADVA	71	PBAV1C
23	ADVB	73	
25	ADVC	75	
27		77	PAAV2B
29	V5C	79	PAAV2A
31	V5B	81	PAAV2C
33	V5A	83	Z1B
35	W1A	85	
37	ADB	87	PAAB
39	ADC	89	PAAC
41	ADA	91	PAAA
43	V5C	93	PBAVNB
45	V5B	95	PBAVNA
47	V5A	97	PBAVNC
49			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	A36	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A20-Side A.
6. This Drawing Derived From IBM DWG NO. 6112967-REL(66123FN)

Figure 10-29. Voters Logic Diagram (Sheet 14)

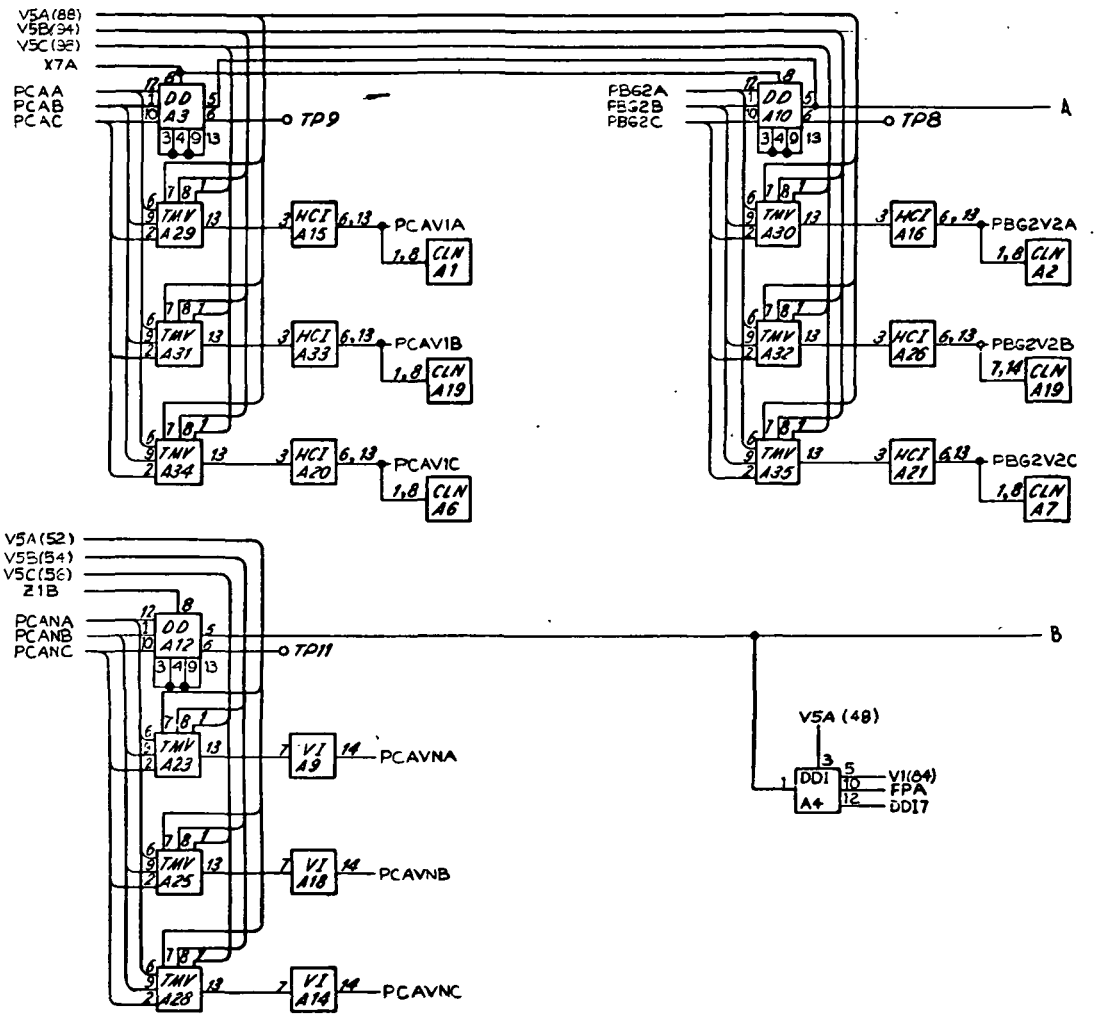
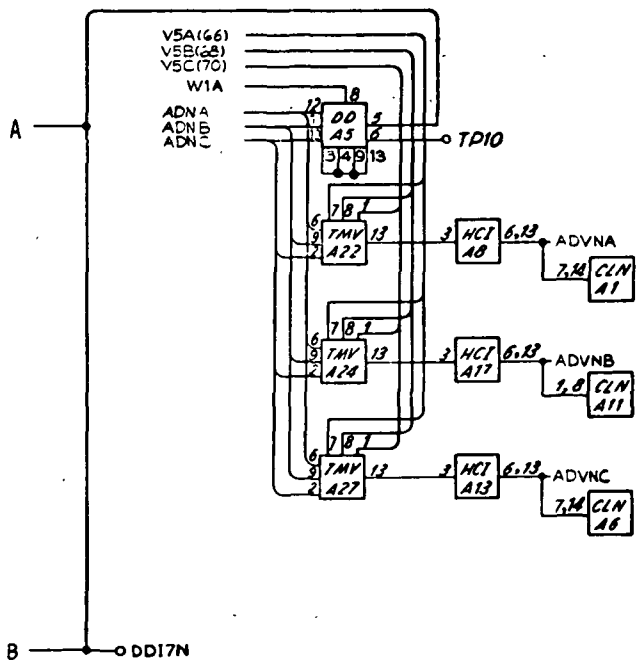


Figure 10-29. Voters Logic Diagram (Sheet 15)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(82)	17	
3	V1(84)	18	
4	V3(86)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DDI7
10	V3(38)	25	DDI7N
11		26	
12		27	
13	SIG-RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	PCAVNC	52	V5A
4	PCAVNA	54	V5B
6	PCAVNB	56	V5C
8	PBG2A	58	ADNA
10	PBG2C	60	ADNC
12	PBG2B	62	ADNB
14	SIG-RET	64	W1A
16	Z1B	66	V5A
18	PBG2V2C	68	V5B
20	PBG2V2A	70	V5C
22	PBG2V2B	72	
24	V1	74	ADVNC
26	V3	76	ADVNB
28	PCAV1C	78	ADVNA
30	PCAV1B	80	
32	PCAV1A	82	SIG-RET
34	SIG-RET	84	V1
36	V1	86	V3
38	V3	88	V5A
40	PCANA	90	PCAA
42	PCANC	92	PCAC
44	PCANB	94	V5B
46		96	PCAB
48	V5A	98	V5C
50	X7A		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DDI	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A20 Side B.
6. This Drawing Derived From IBM DWG NO. 6112969-REL(66123FN)

Figure 10-29. Voters Logic Diagram (Sheet 16)

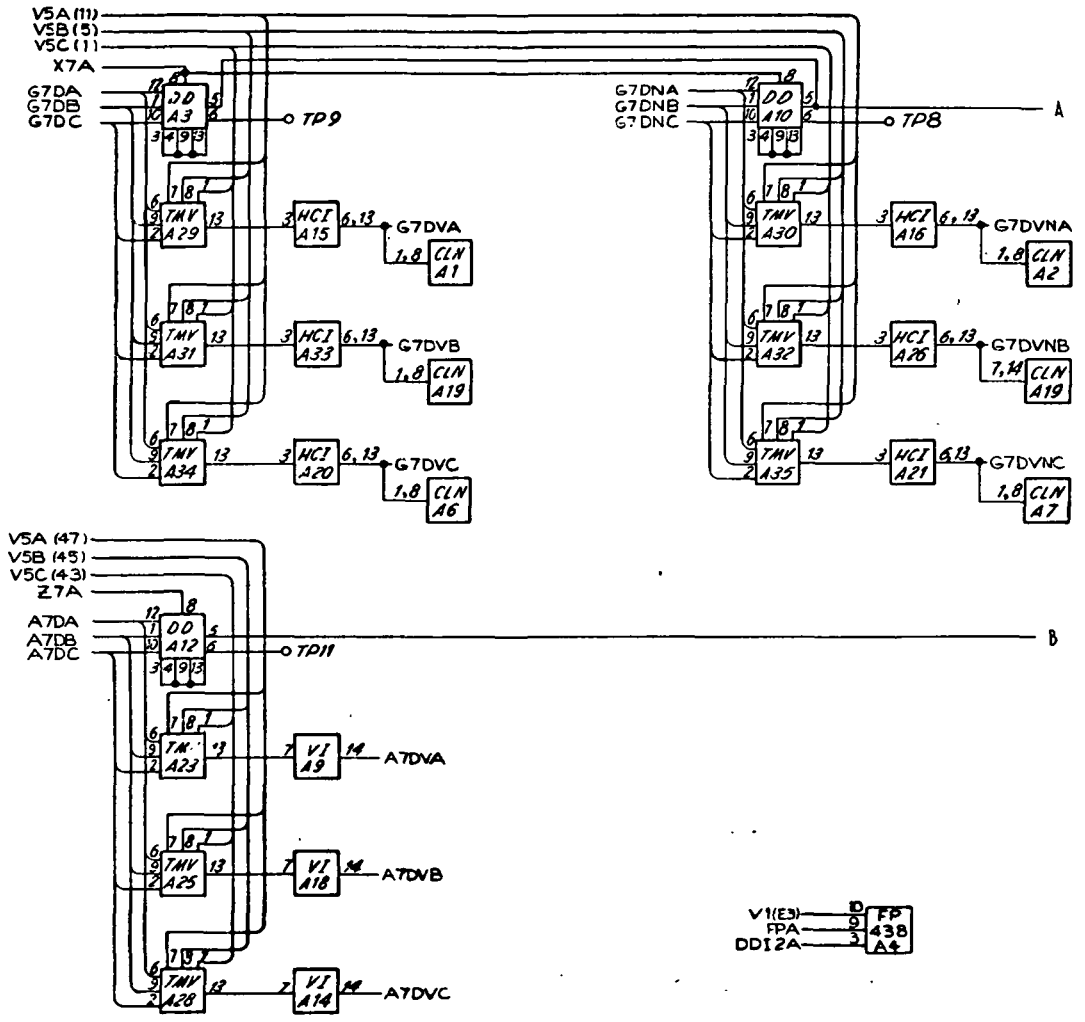
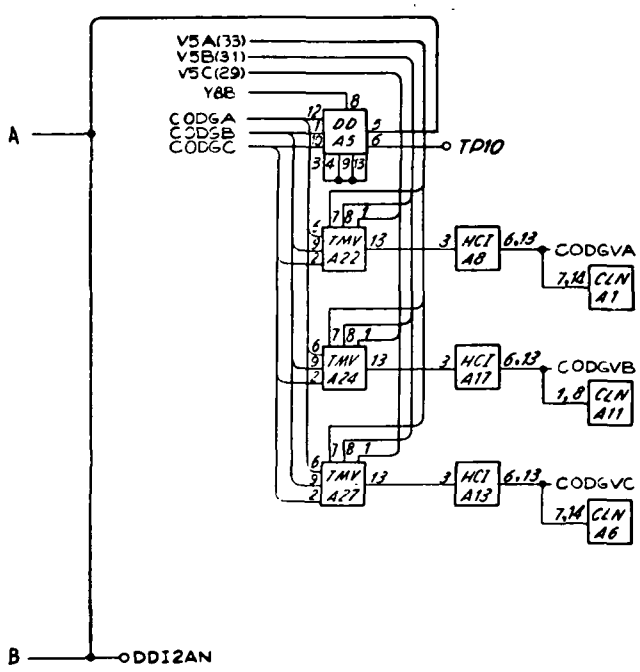


Figure 10-29. Voters Logic Diagram (Sheet 17)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DDI2A
10	V3	25	DDI2AN
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDI2A
3	G7DB	53	
5	V5B	55	A7DB
7	G7DC	57	A7DC
9	G7DA	59	A7DA
11	V5A	61	
13		63	
15		65	
17		67	G7DVA
19		69	G7DVB
21	CODGVA	71	G7DVC
23	CODGVB	73	
25	CODGVC	75	
27		77	G7DVNB
29	V5C	79	G7DVNA
31	V5B	81	G7DVNC
33	V5A	83	Z7A
35	Y8B	85	
37	CODGB	87	G7DNB
39	CODGC	89	G7DNC
41	CODGA	91	G7DNA
43	V5C	93	A7DVB
45	V5B	95	A7DVA
47	V5A	97	A7DVC
49	X7A		

ULD LOCATIONS

A1 CLN	A2 CLN	A3 DD	A4 FD A38	A5 DD	A6 CLN	A7 CLN
A8 HCI	A9 VI	A10 DD	A11 CLN	A12 DD	A13 HCI	A14 VI
A15 HCI	A16 HCI	A17 HCI	A18 VI	A19 CLN	A20 HCI	A21 HCI
A22 TMV	A23 TMV	A24 TMV	A25 TMV	A26 HCI	A27 TMV	A28 TMV
A29 TMV	A30 TMV	A31 TMV	A32 TMV	A33 HCI	A34 TMV	A35 TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A7 Side A.
6. This Drawing Derived From IBM DWG NO. 6112137-REL(66123FM)

Figure 10-29. Voters Logic Diagram (Sheet 18)

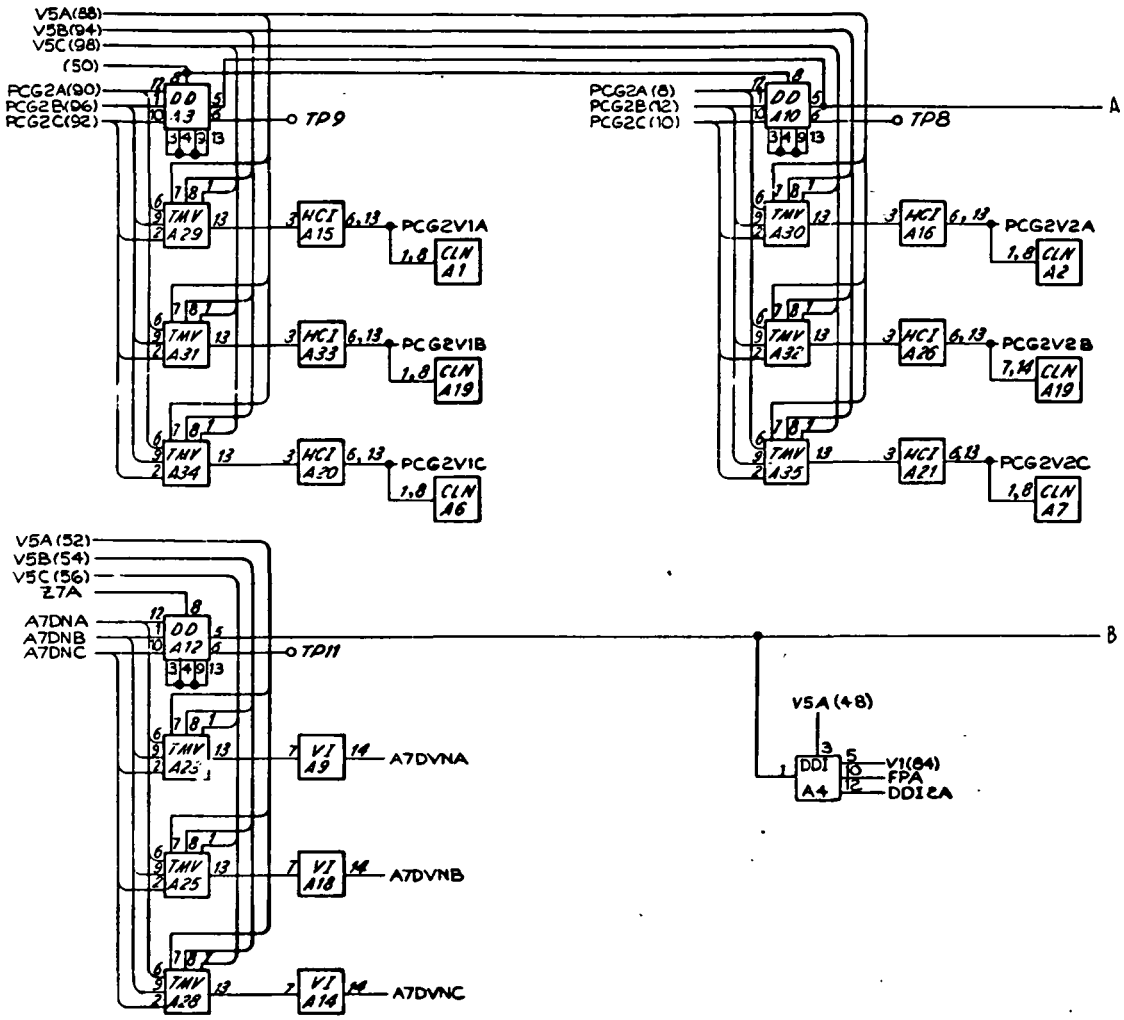
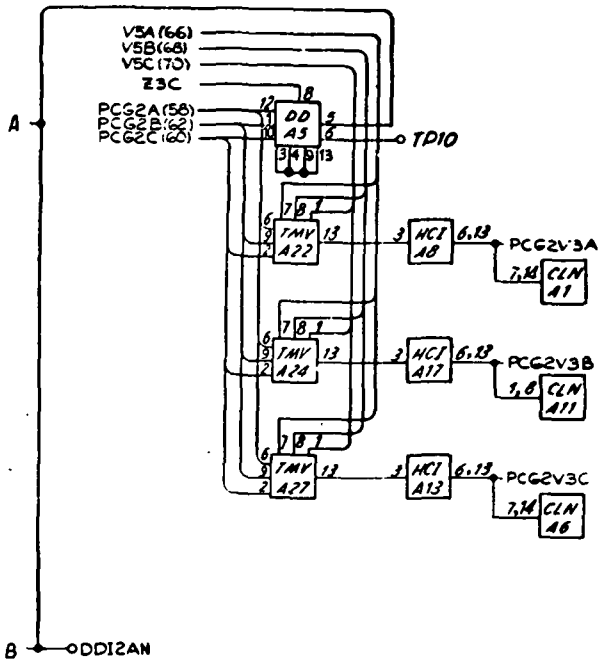


Figure 10-29. Voters Logic Diagram (Sheet 19)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(82)	17	
3	V1(84)	18	
4	V3(86)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DDI2A
10	V3(38)	25	DDI2AN
11		26	
12		27	
13	SIG-RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	A7DVNC	52	V5A
4	A7DVNA	54	V5B
6	A7DVNB	56	V5C
8	PCG2A	58	PCG2A
10	PCG2C	60	PCG2C
12	PCG2B	62	PCG2B
14	SIG-RET	64	Z3C
16	Z7A	66	V5A
18	PCG2V2C	68	V5B
20	PCG2V2A	70	V5C
22	PCG2V2B	72	
24	V1	74	PCG2V3C
26	V3	76	PCG2V3B
28	PCG2V1C	78	PCG2V3A
30	PCG2V1B	80	
32	PCG2V1A	82	SIG-RET
34	SIG-RET	84	V1
36	V1	86	V3
38	V3	88	V5A
40	A7DNA	90	PCG2A
42	A7DNC	92	PCG2C
44	A7DNB	94	V5B
46		96	PCG2B
48	V5A	98	V5C
50			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DDI	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	VI	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A7 Side B.
6. This Drawing Derived From IBM DWG NO. 6112139-REL(66123FM)

Figure 10-29. Voters Logic Diagram (Sheet 20)

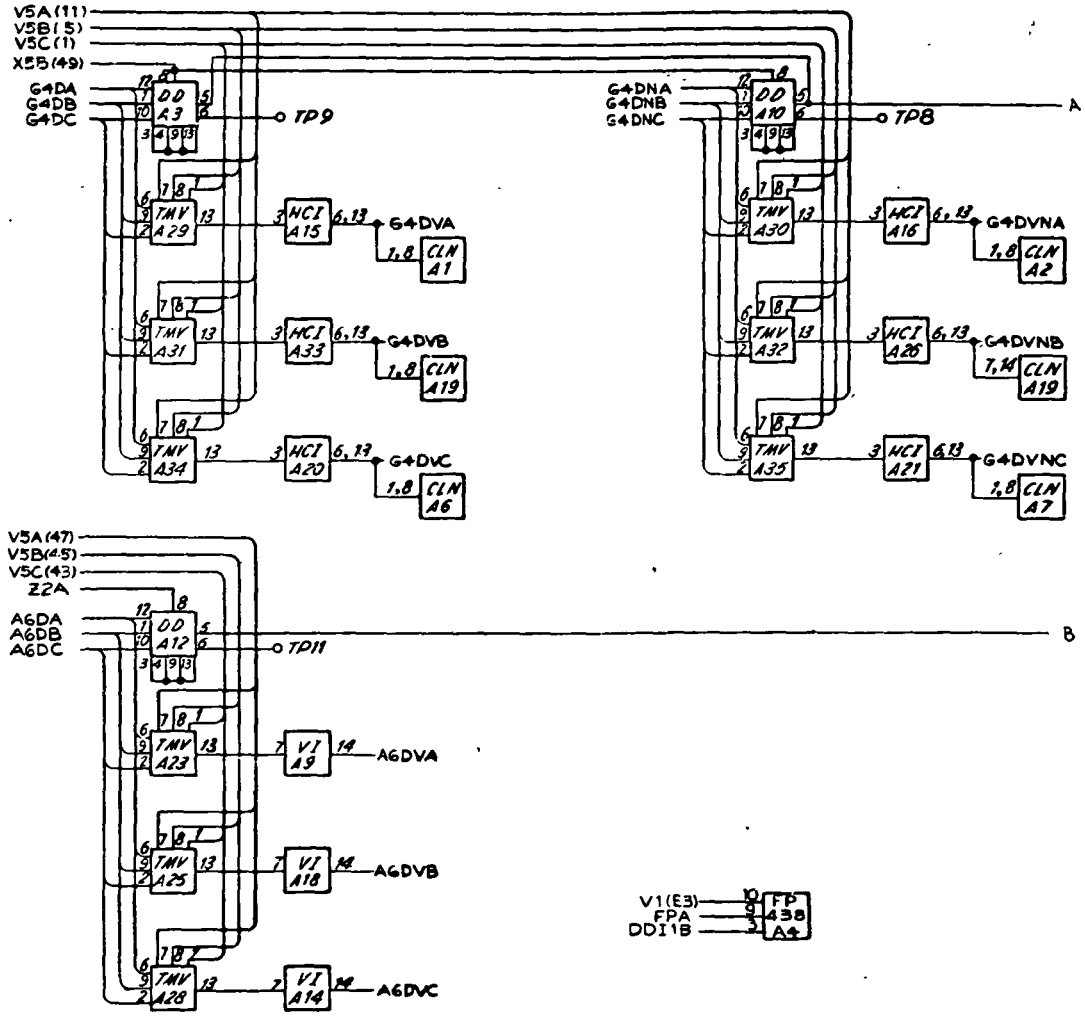
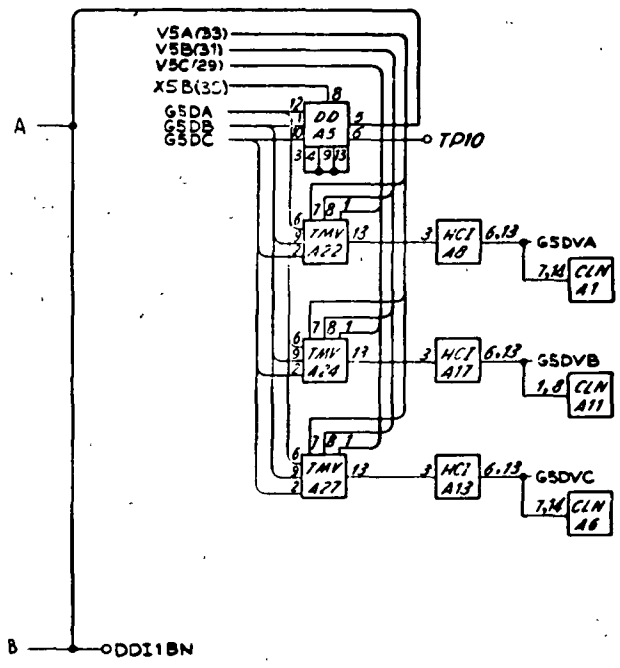


Figure 10-29. Voters Logic Diagram (Sheet 21)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DDI1B
10	V3	25	DDI1BN
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDI1B
3	G4DB	53	
5	V5B	55	A6DB
7	G4DC	57	A6DC
9	G4DA	59	A6DA
11	V5A	61	
13		63	
15		65	
17		67	G4DVA
19		69	G4DVB
21	G5DVA	71	G4DVC
23	G5DVB	73	
25	G5DVC	75	
27		77	G4DVNB
29	V5C	79	G4DVNA
31	V5B	81	G4DVNC
33	V5A	83	ZZA
35	X5B	85	
37	G5DB	87	G4DNB
39	G5DC	89	G4DNC
41	G5DA	91	G4DNA
43	V5C	93	A6DVB
45	V5B	95	A6DVA
47	V5A	97	A6DVC
49	X5B		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	A38	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	VI	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A18 Side A.
6. This Drawing Derived From IBM DWG NO. 6112117-REL(66123FM)

Figure 10-29. Voters Logic Diagram (Sheet 22)

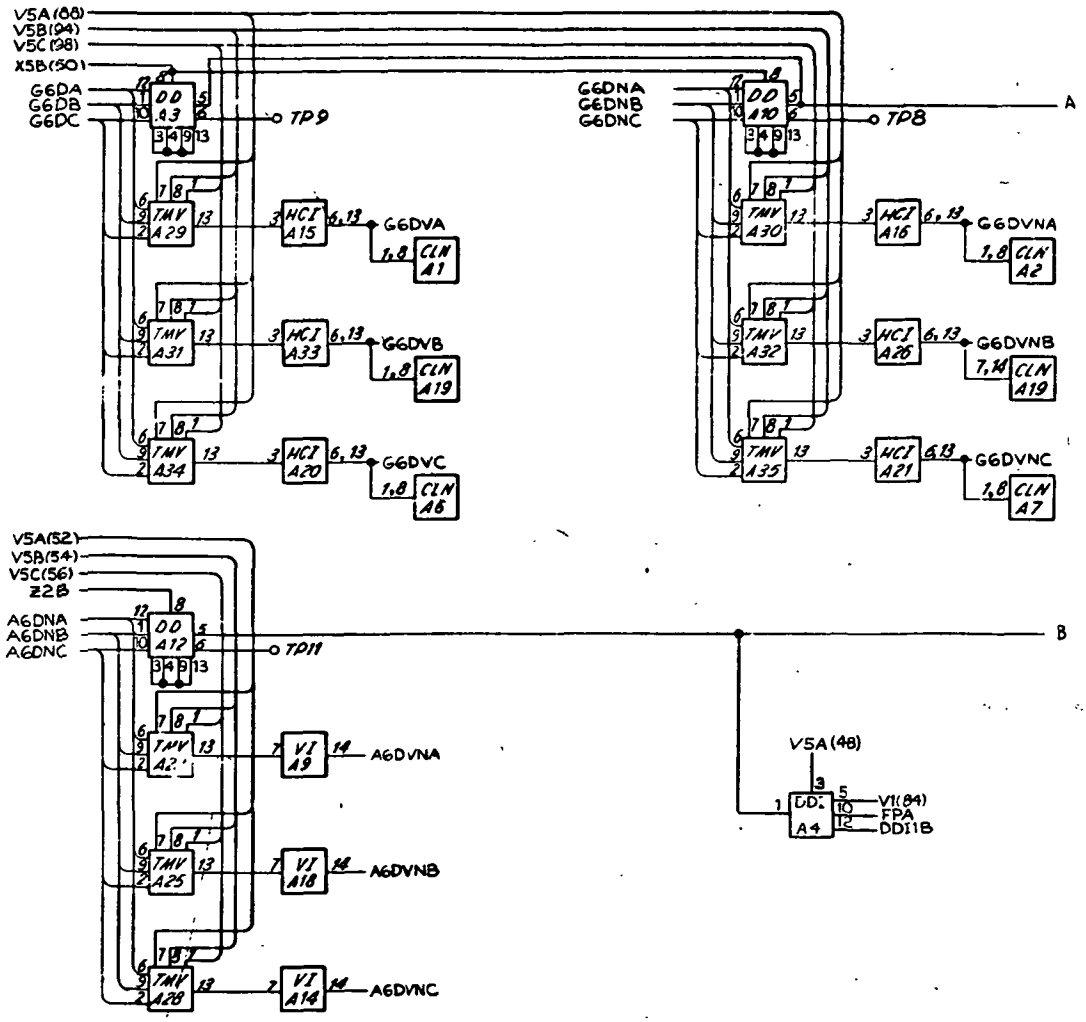
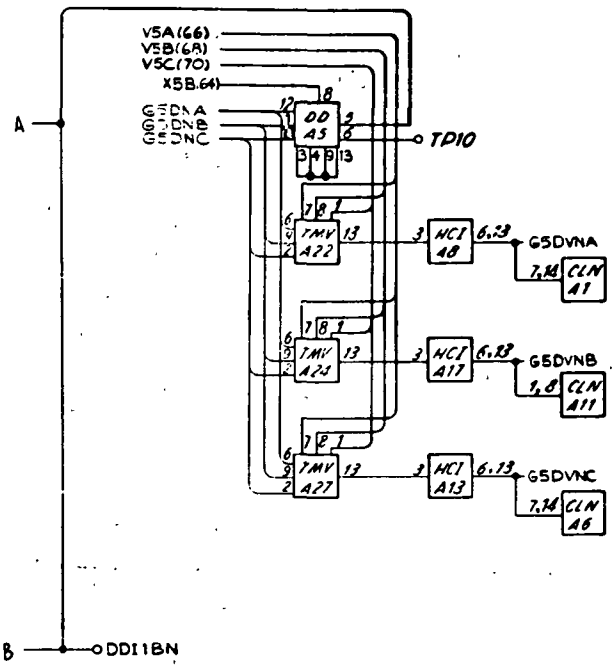


Figure 10-29. Voters Logic Diagram (Sheet 23)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(82)	17	
3	V1(84)	18	
4	V3(86)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DDI1B
10	V3(38)	25	DDI1BN
11		26	
12		27	
13	SIG-RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
[illegible]	A6DVNC	52	V5A
[illegible]	A6DVNA	54	V5B
[illegible]	A6DVNB	56	V5C
[illegible]	G6DVA	58	G5DNA
[illegible]	G6DVNC	60	G5DNC
62	G6DNB	62	G5DVB
64	SIG-RET	64	V5B
[illegible]	Z2B	66	V5A
68	G6DVNC	68	V5B
70	G6DVNA	70	V5C
72	G6DVNB	72	
74	V1	74	G5DVNC
76	V3	76	G5DVNB
78	G6DVC	78	G5DVNA
80	G6DVB	80	
82	G6DVA	82	SIG-RET
84	SIG-RET	84	V1
86	V1	86	V3
88	V3	88	V5A
90	A6DNA	90	G6DA
92	A6DNC	92	G6DC
94	A6DNB	94	V5B
96		96	G6DB
98	V5A	98	V5C
100	X5B		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DDI	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A18 Side B.
6. This Drawing Derived From IBM DWG NO. 6112119-REL(66123FM)

Figure 10-29. Voters Logic Diagram (Sheet 24)

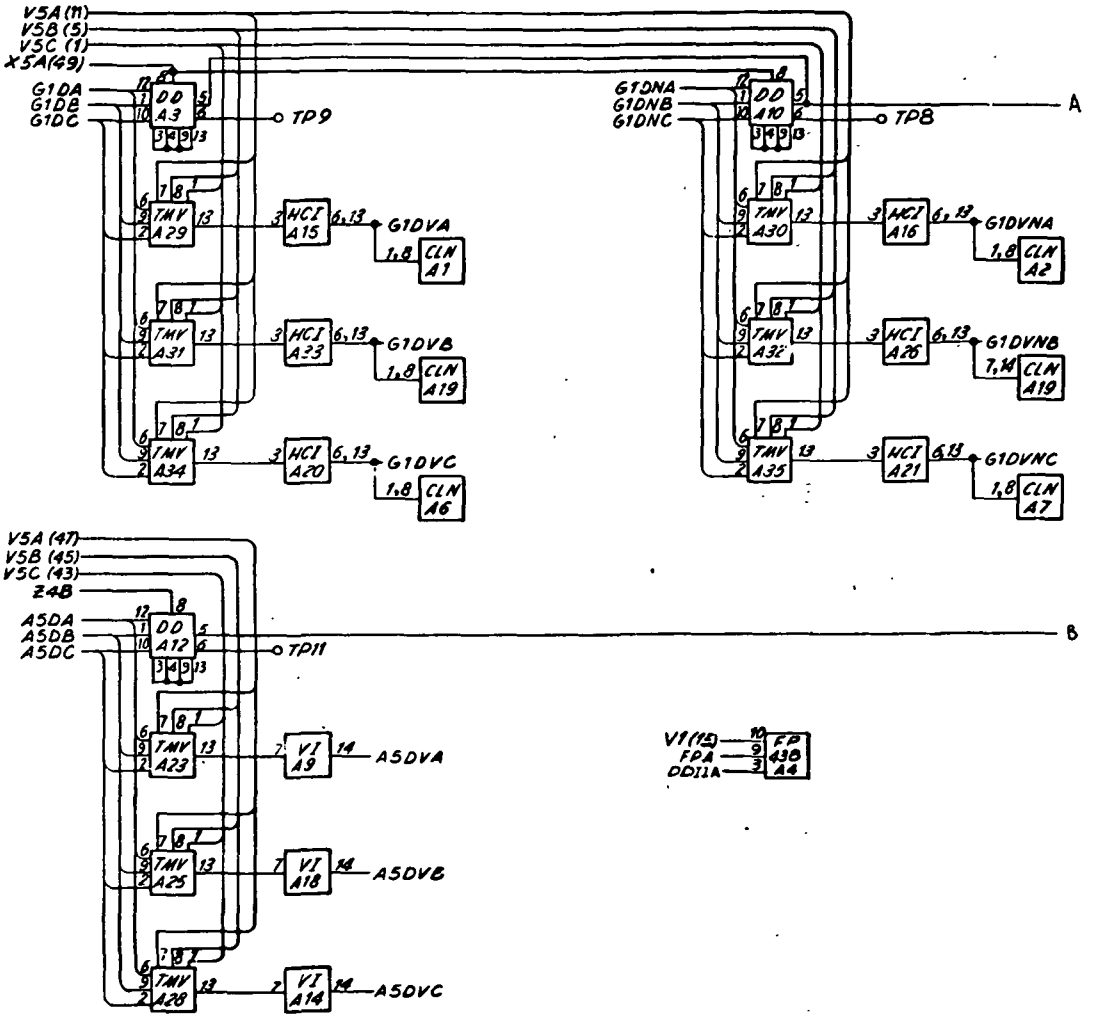
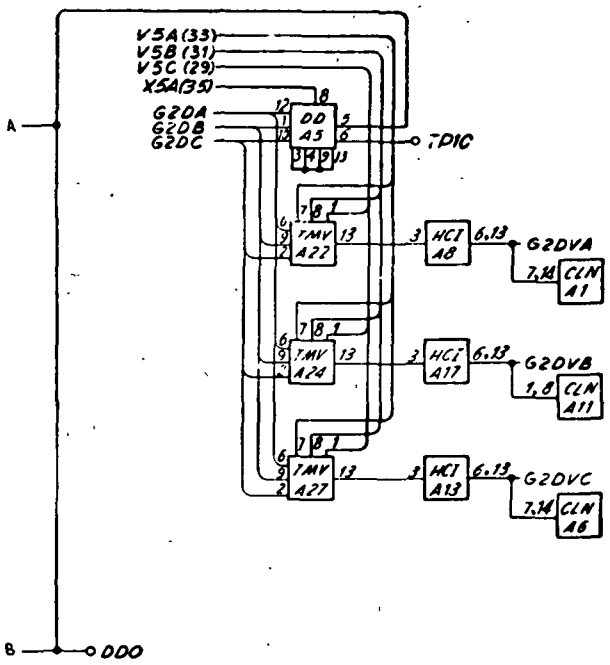


Figure 10-29. Voters Logic Diagram (Sheet 25)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET	17	
3	V1	18	
4	V3	19	
5		20	
6		21	
7		22	
8	SIG-RET	23	FPA
9	V1	24	DDI1A
10	V3	25	DDO
11		26	
12		27	
13	SIG RET	28	
14	V1	29	
15	V3	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDI1A
3	G1DB	53	
5	V5B	55	A5DB
7	G1DC	57	A5DC
9	G1DA	59	A5DA
11	V5A	61	
13		63	
15		65	
17		67	G1DVA
19		69	G1DVB
21	G2DVA	71	G1DVC
23	G2DVB	73	
25	G2DVC	75	
27		77	G1DVNB
29	V5C	79	G1DVNA
31	V5B	81	G1DVNC
33	V5A	83	Z4B
35	X5A	85	
37	G2DE	87	G1DNB
39	G2DC	89	G1DNC
41	G2DA	91	G1DVA
43	V5C	93	A5DB
45	V5B	95	A5DVA
47	V5A	97	A5DVC
49	X5A		

ULD LOCATIONS

A1	A2	A3	A4 FP 439	A5	A6	A7
CLN	CLN	DD		DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A29 Side A.
6. This Drawing Derived From IBM DWG NO. 6112477-REL(66123DM)

Figure 10-29. Voters Logic Diagram (Sheet 26)

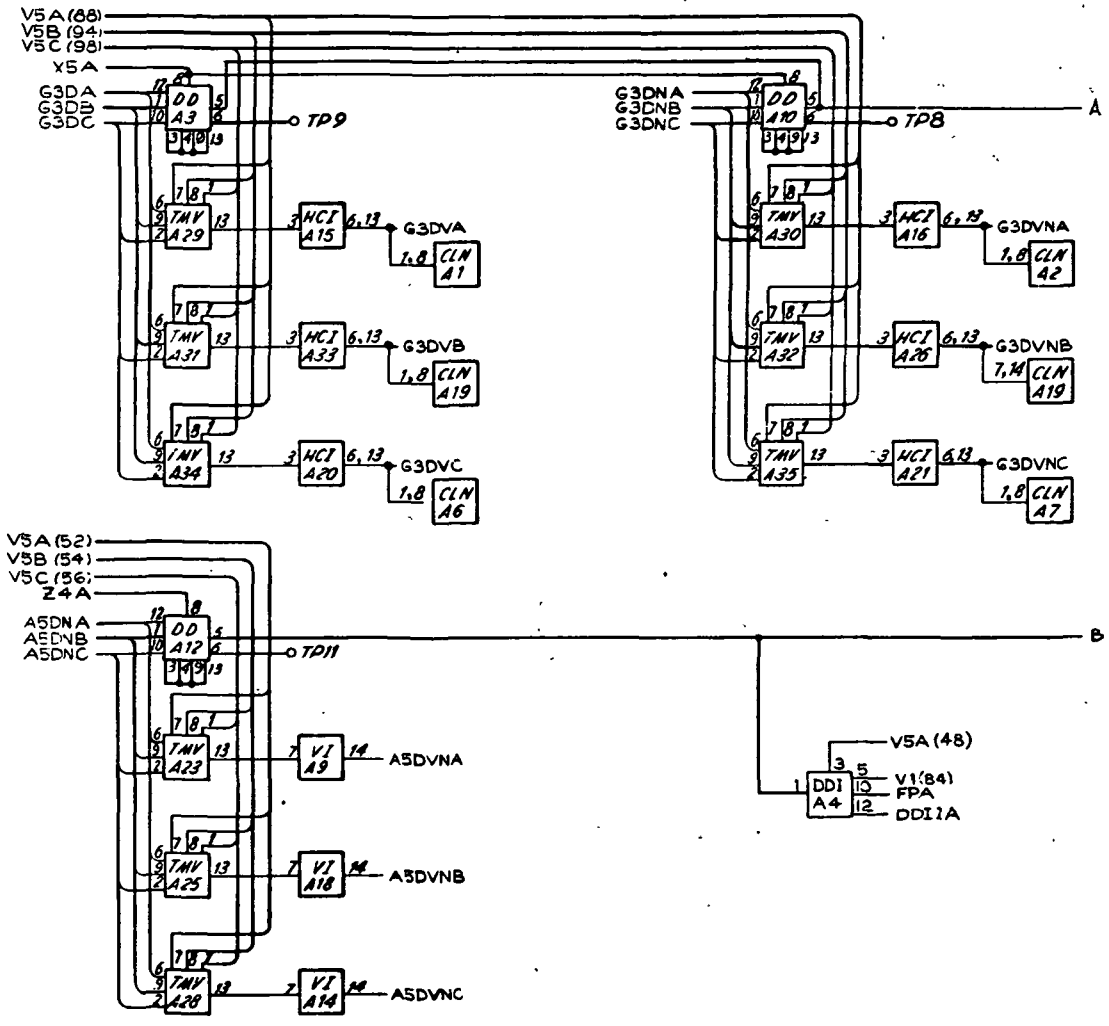
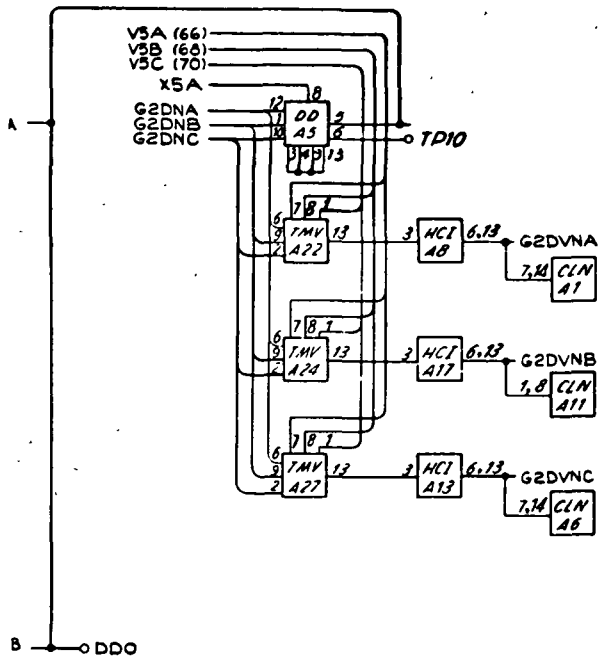


Figure 10-29. Voters Logic Diagram (Sheet 27)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(82)	17	
3	V1(84)	18	
4	V3(86)	19	
5		20	
6		21	
7		22	
8	SIG-RET(34)	23	FPA
9	V1(36)	24	DDI1A
10	V3(38)	25	DDO
11		26	
12		27	
13	SIG RET(14)	28	
14	V1(24)	29	
15	V3(26)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	A5DVNC	52	V5A
4	A5DVNA	54	V5B
6	A5DVNB	56	V5C
8	G3DNA	58	G2DNA
10	G3DNC	60	G2DNC
12	G3DNB	62	G2DNB
14	SIG-RET	64	X5A
16	Z4A	66	V5A
18	G2DVNC	68	V5B
20	G3DVNA	70	V5C
22	G3DVNB	72	
24	V1	74	G2DVNC
26	V3	76	G2DVNB
28	G3DVC	78	G2DVNA
30	G3DVB	80	
32	G3DVA	82	SIG-RET
34	SIG-RET	84	V1
36	V1	86	V3
38	V3	88	V5A
40	A5DNA	90	G3DA
42	A5DNC	92	G3DC
44	A5DNB	94	V5B
[illegible]		96	G3DB
46	V5A	98	VEC
50	X5A		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD	DDI	DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	VI	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U."-Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A29 Side B.
6. This Drawing Derived From IBM DWG NO. 6112479-REL(66123BZ)

Figure 10-29. Voters Logic Diagram (Sheet 28)

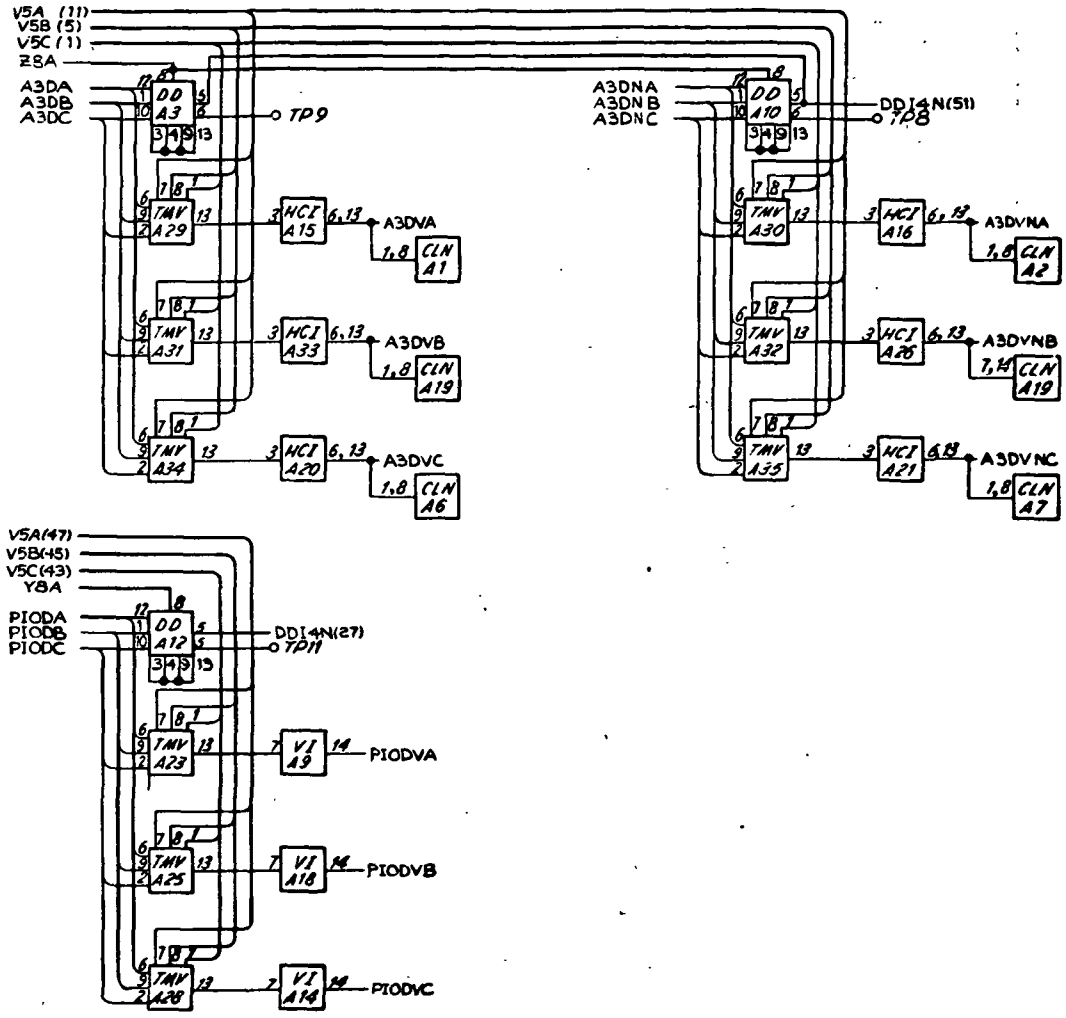
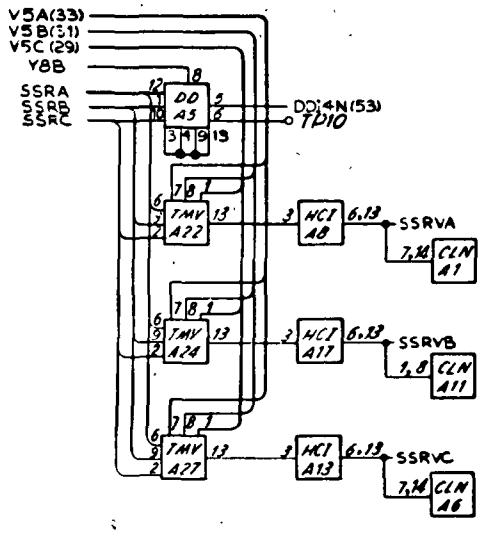


Figure 10-29. Voters Logic Diagram (Sheet 29)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(17)	17	
3	V1(15)	18	
4	V3(13)	19	
5		20	
6		21	
7		22	
8	SIG-RET(65)	23	
9	V1(63)	24	
10	V3(61)	25	
11		26	
12		27	
13	SIG-RET(65)	28	
14	V1(75)	29	
15	V3(73)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1	V5C	51	DDI4N
3	A3DB	53	DDI4N
5	V5B	55	PIODB
7	A3DC	57	PIODC
9	A3DA	59	PIODA
11	V5A	61	V3
13	V3	63	V1
15	V1	65	SIG-RET
17	SIG-RET	67	A3DVA
19		69	A3DVB
21	SSRVA	71	A3DVC
23	SSRVB	73	V3
25	SSRVC	75	V1
27	DDI4N	77	A3DVNB
29	V5C	79	A3DVNA
31	V5B	81	A3DV.C
33	V5A	83	Y8A
35	Y8B	85	SIG-RET
37	SSRB	87	A3DNB
39	SSRC	89	A3DNC
41	SSRA	91	A3DNA
43	V5C	93	PIODVB
45	V5B	95	PIODVA
47	V5A	97	PIODVC
49	28A		

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD		DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	VI	DD	CLN	DD	HCI	VI
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V.'	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A15 Side A.
6. This Drawing Derived From IBM DWG NO. 6112187-REL(66123FM)

Figure 10-29. Voters Logic Diagram (Sheet 30)

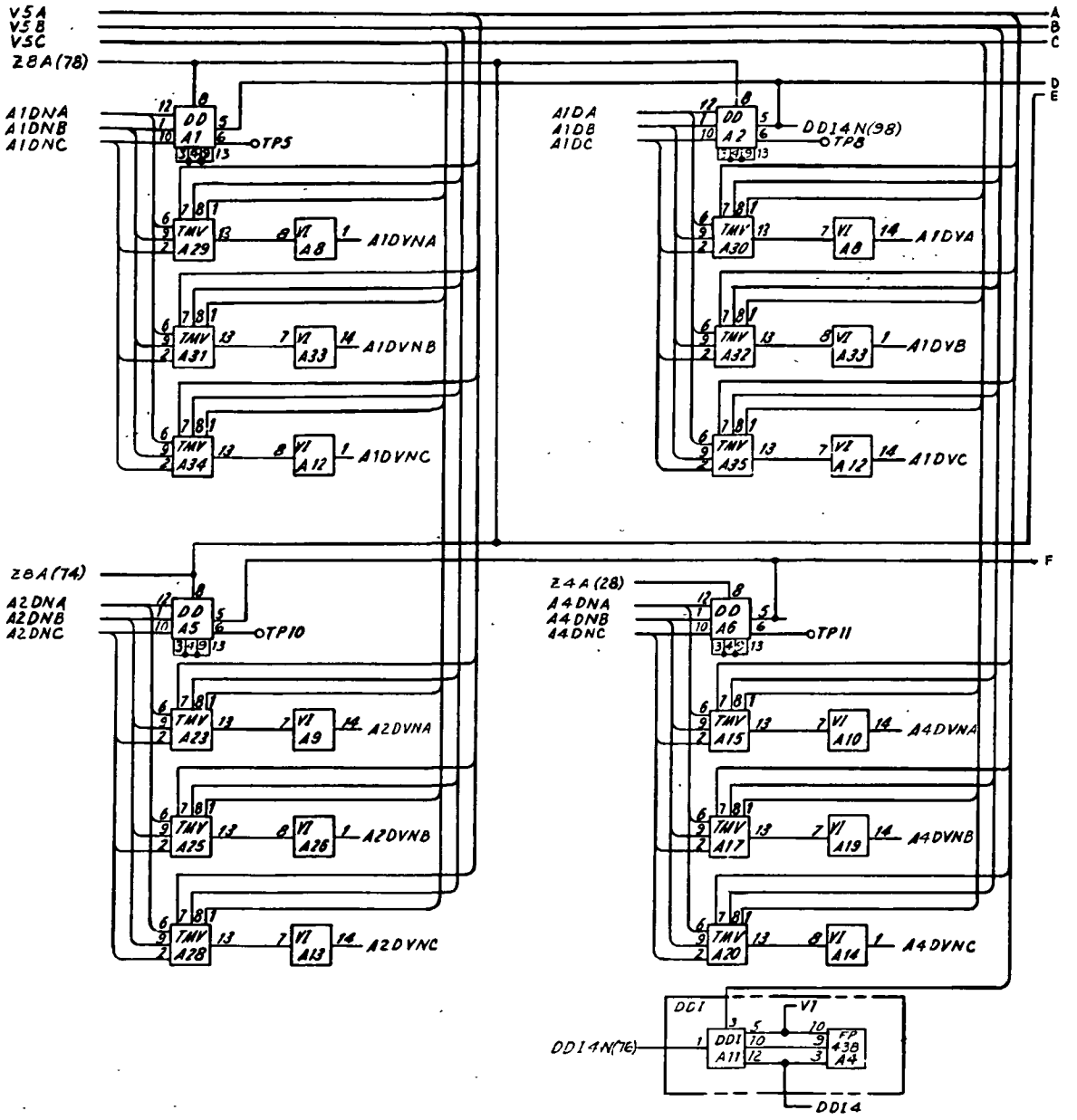
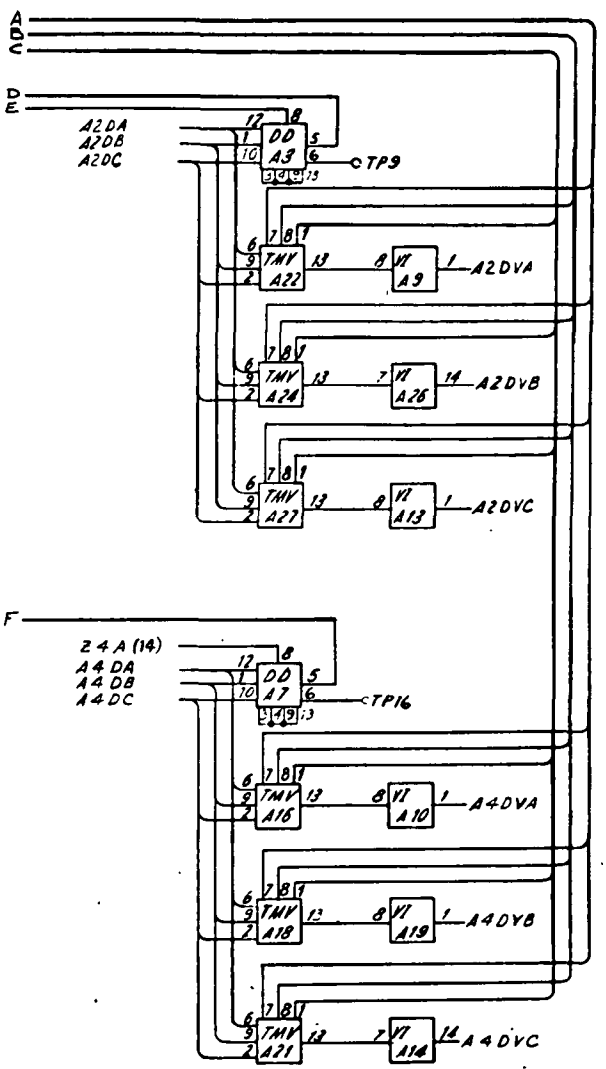


Figure 10-29. Voters Logic Diagram (Sheet 31)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	V5C
2	SIG-RET	17	(2)
3	V1	18	(4)
4	V3	19	(6)
5		20	
6		21	
7		22	
8	SIG-RET	23	V5B
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	V5A

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	A2DNC
4		54	A2DNB
6		56	A1DVB
8	A2DA	58	A1DVC
10	A2DC	60	A1DVA
12	A2DB	62	A2DA
14	Z4A	64	A2DC
16	A2DVA	66	A2DB
18	A2DVC	68	A1DA
20	A2DVB	70	A1DC
22	A2DNA	72	A1DB
24	A4DNA	74	Z3A
26	A2DNB	76	DD24N
28	Z4A	78	Z8A
30	A4DVNC	80	V5A
32	A4DVNA	82	V5B
34	A4DVNB	84	V5C
36	A4DVB	86	A1DVNC
38	A4DVC	88	A1DVNB
40	A4DVA	90	A1DVNA
42	A2DVNB	92	A1DNA
44	A2DVNC	94	A1DNC
46	A2DVNA	96	A1DNB
48	DD14	98	DD14N
50	A2DNA		

A1 DD	A2 DD	A3 DD	A4 438 FP	A5 DD	A6 DD	A7 DD
A8 VI	A9 VI	A10 VI	A11 DD1	A12 VI	A13 VI	A14 VI
A15 TMV	A16 TMV	A17 TMV	A18 TMV	A19 VI	A20 TMV	A21 TMV
A22 TMV	A23 TMV	A24 TMV	A25 TMV	A26 VI	A27 TMV	A28 TMV
A29 TMV	A30 TMV	A31 TMV	A32 TMV	A33 VI	A34 TMV	A35 TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A15 Side B.
6. This Drawing Derived From IBM DWG NO. 6112189-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 32)

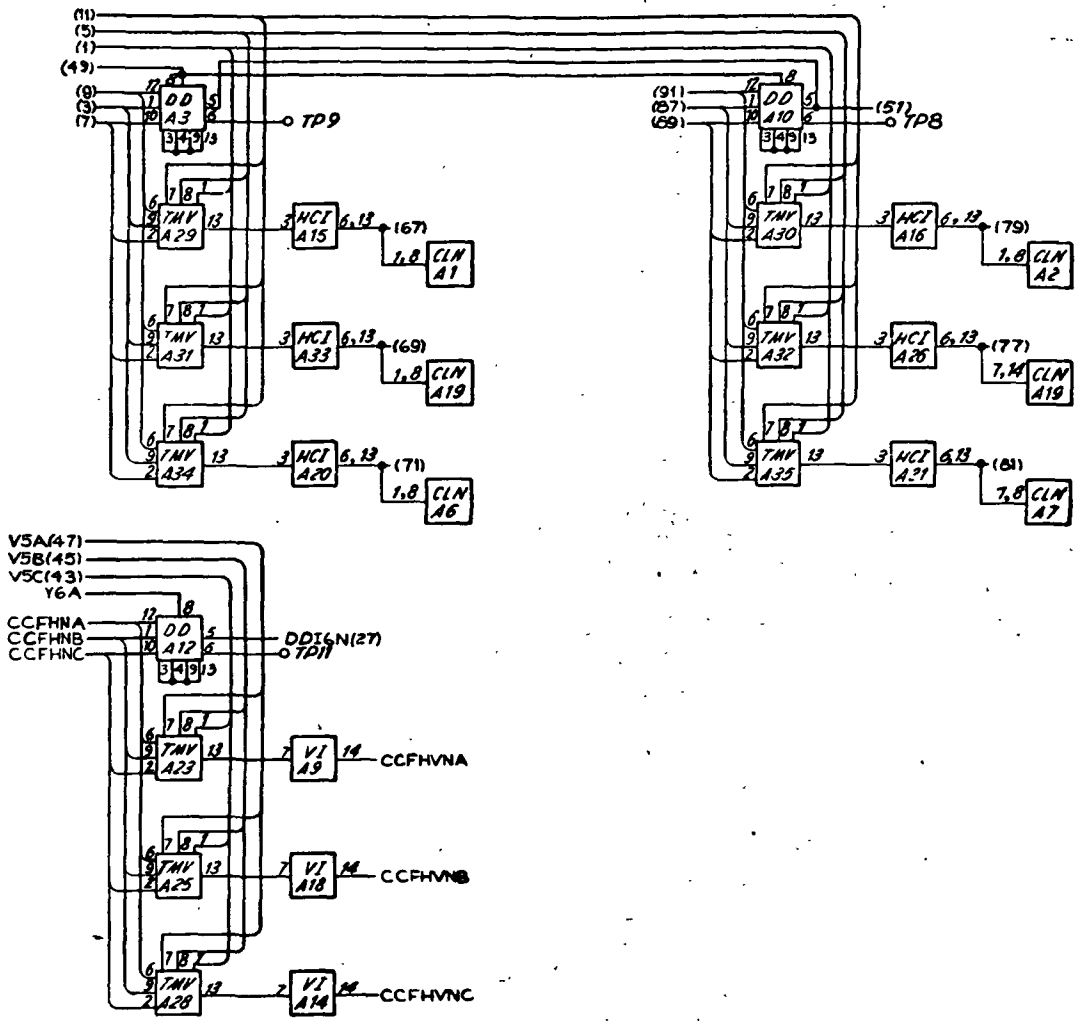
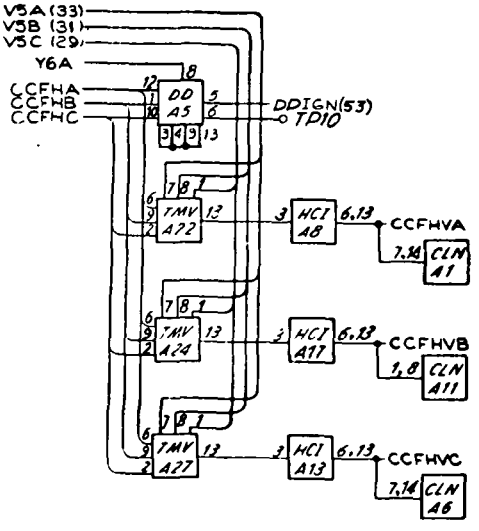


Figure 10-29. Voters Logic Diagram (Sheet 33)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	
2	SIG-RET(17)	17	
3	V1(15)	18	
4	V3(13)	19	
5		20	
6		21	
7		22	
8	SIG-RET(65)	23	
9	V1(63)	24	
10	V3(61)	25	
11		26	
12		27	
13	SIG-RET(85)	28	
14	V1(75)	29	
15	V3(73)	30	

CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
1		51	
3		53	DDIGN
5		55	CCFHNB
7		57	CCFHNC
9		59	CCFHNA
11		61	V3
13	V3	63	V1
15	V1	65	SIG-RET
17	SIG-RET	67	
19		69	
21	CCFHVA	71	
23	CCFHVB	73	V3
25	CCFHVC	75	V1
27	DDIGN	77	
29	V5C	79	
31	V5B	81	
33	V5A	83	Y6A
35	Y6A	85	SIG-RET
37	CCFHB	87	
39	CCFHC	89	
41	CCFHA	91	
43	V5C	93	CCFHVNB
45	V5B	95	CCFHVNA
47	V5A	97	CCFHVNC
49			

ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
CLN	CLN	DD		DD	CLN	CLN
A8	A9	A10	A11	A12	A13	A14
HCI	V1	DD	CLN	DD	HCI	V1
A15	A16	A17	A18	A19	A20	A21
HCI	HCI	HCI	V1	CLN	HCI	HCI
A22	A23	A24	A25	A26	A27	A28
TMV	TMV	TMV	TMV	HCI	TMV	TMV
A29	A30	A31	A32	A33	A34	A35
TMV	TMV	TMV	TMV	HCI	TMV	TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A31 Side A.
6. This Drawing Derived From IBM DWG NO. 6112217-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 34)

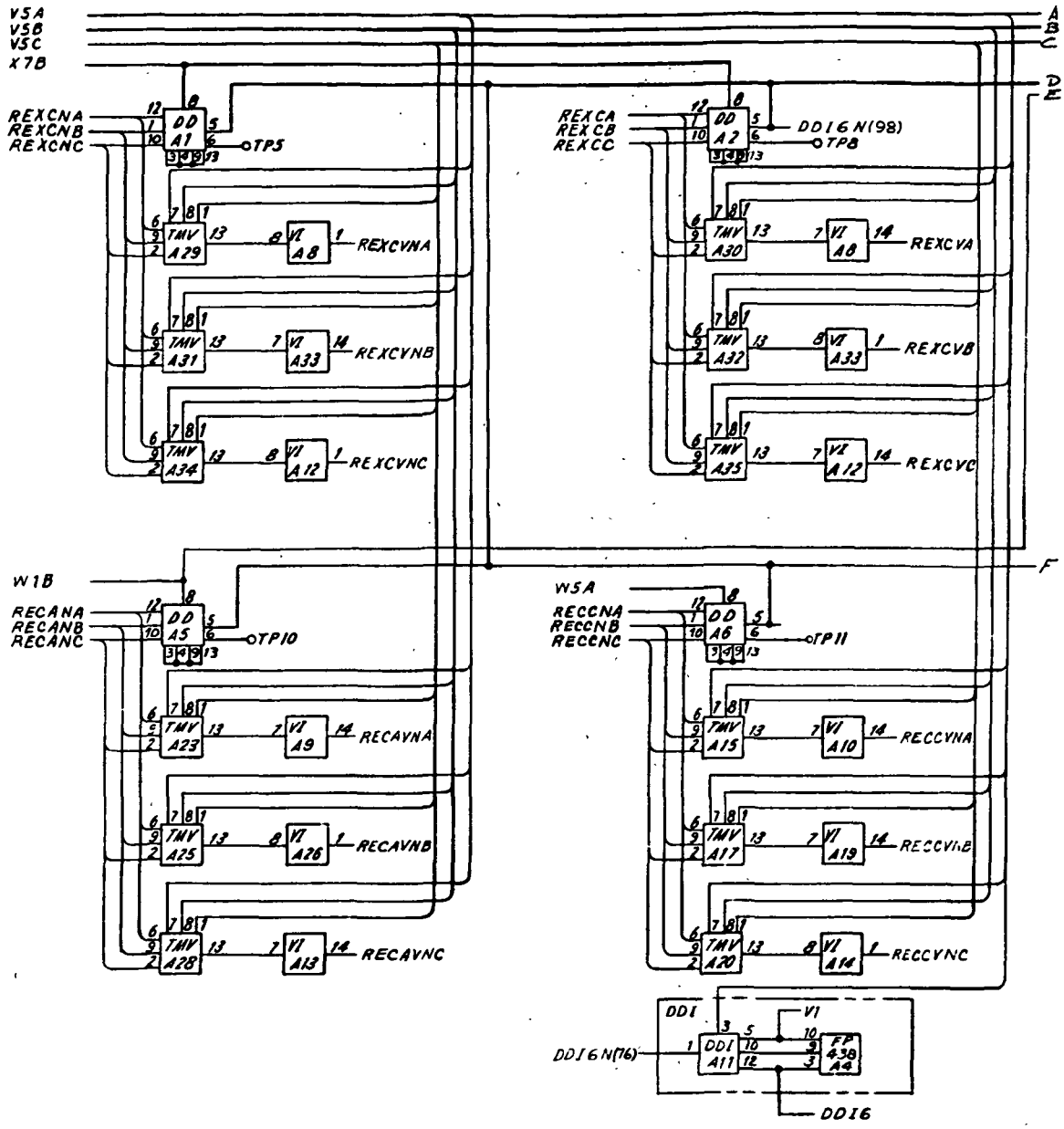
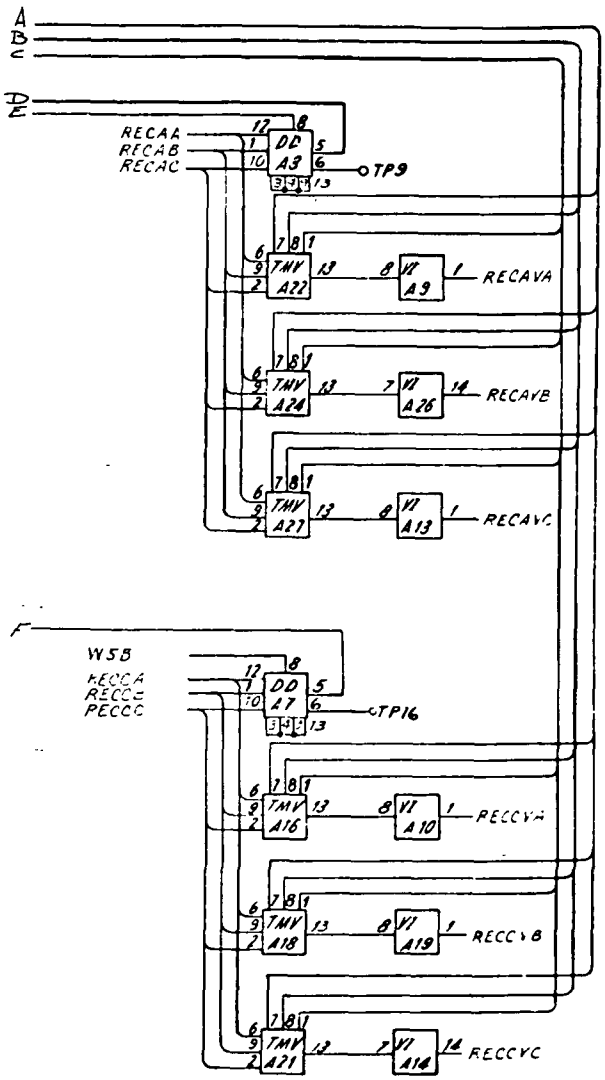


Figure 10-29. Voters Logic Diagram (Sheet 35)



THRU-PINS			
PIN	SIGNAL	PIN	SIGNAL
1		16	V5C
2	SIG-RET	17	(2)
3	V1	18	(4)
4	V3	19	(6)
5		20	
6		21	
7		22	
8	SIG-RET	23	V5B
9	V1	24	
10	V3	25	
11		26	
12		27	
13	SIG-RET	28	
14	V1	29	
15	V3	30	V5A

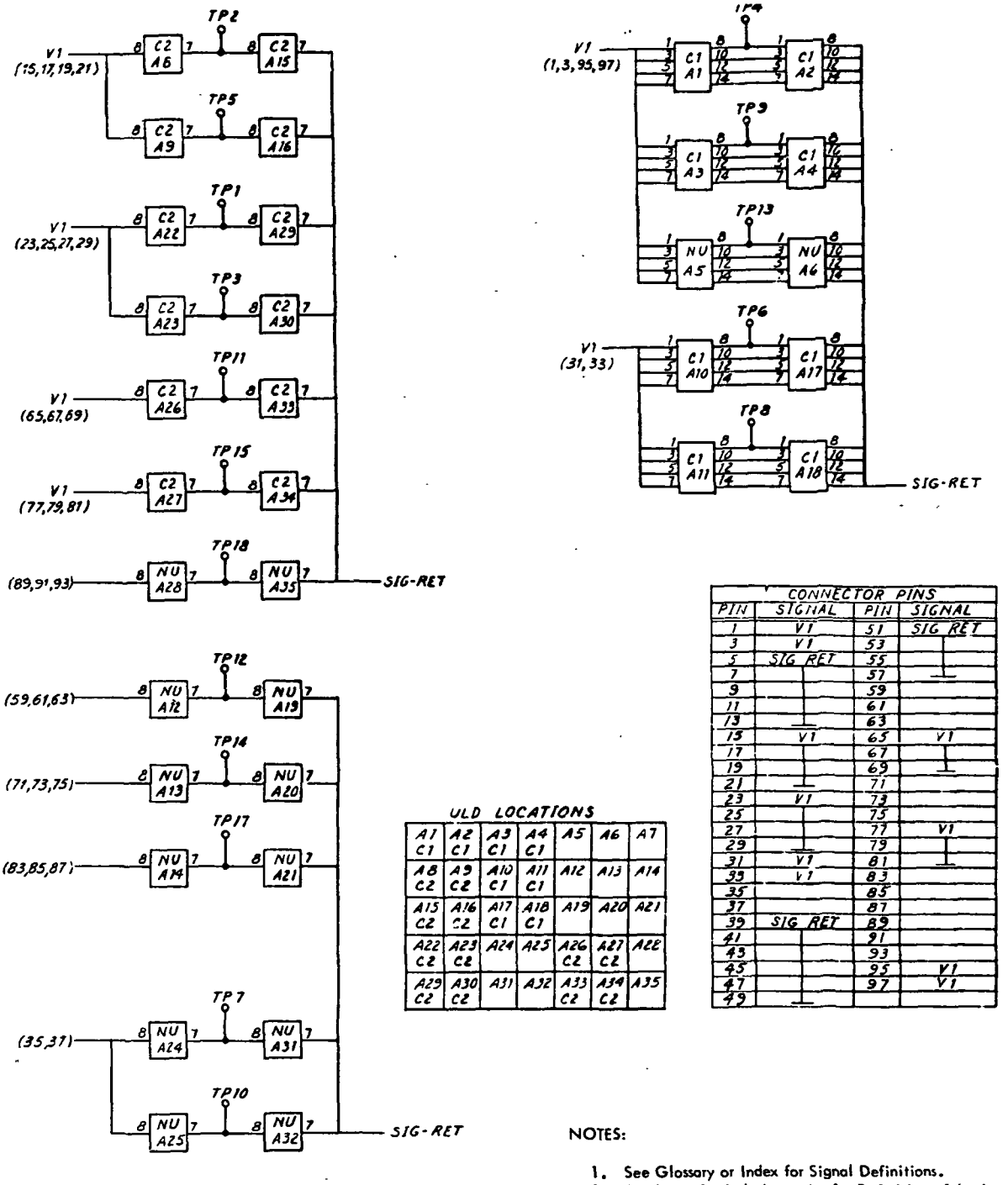
CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2		52	RECAVC
4		54	RECAVB
6		56	RECAVA
8	RECCA	58	RECCVC
10	RECCC	60	RECCVA
12	RECCB	62	RECAM
14	W5B	64	RECAC
16	RECAVA	66	RECAB
18	RECAVC	68	RECAA
20	RECAVB	70	RECCC
22	RECCNA	72	RECCB
24	RECCNC	74	W1B
26	RECCNB	76	DD15A
28	W5A	78	X7B
30	RECCVNC	80	V5A
32	RECCVNA	82	V3C
34	RECCVNB	84	V3C
36	RECCVB	86	RECVCNC
38	RECCVC	88	RECVCNB
40	RECCVA	90	RECXCNA
42	RECAVNB	92	RECXCNA
44	RECAVNC	94	RECXCNC
46	RECAVNA	96	RECXCNB
48	DD16	98	DD15A
50	RECANA		

A1 DD	A2 DD	A3 DD	A4 FF 436	A5 DD	A6 DD	A7 DD
A8 VI	A9 VI	A10 VI	A11 DD1	A12 VI	A13 VI	A14 VI
A15 TMV	A16 TMV	A17 TMV	A18 TMV	A19 VI	A20 TMV	A21 TMV
A22 TMV	A23 TMV	A24 TMV	A25 TMV	A26 VI	A27 TMV	A28 TMV
A29 TMV	A30 TMV	A31 TMV	A32 TMV	A33 VI	A34 TMV	A35 TMV

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A31 Side B.
6. This Drawing Derived From IBM DWG NO. 6112219-REL(66123ET)

Figure 10-29. Voters Logic Diagram (Sheet 36)



ULD LOCATIONS

A1 C1	A2 C1	A3 C1	A4 C1	A5	A6	A7
A8 C2	A9 C2	A10 C1	A11 C1	A12	A13	A14
A15 C2	A16 C2	A17 C1	A18 C1	A19	A20	A21
A22 C2	A23 C2	A24	A25	A26 C2	A27 C2	A28
A29 C2	A30 C2	A31	A32	A33 C2	A34 C2	A35

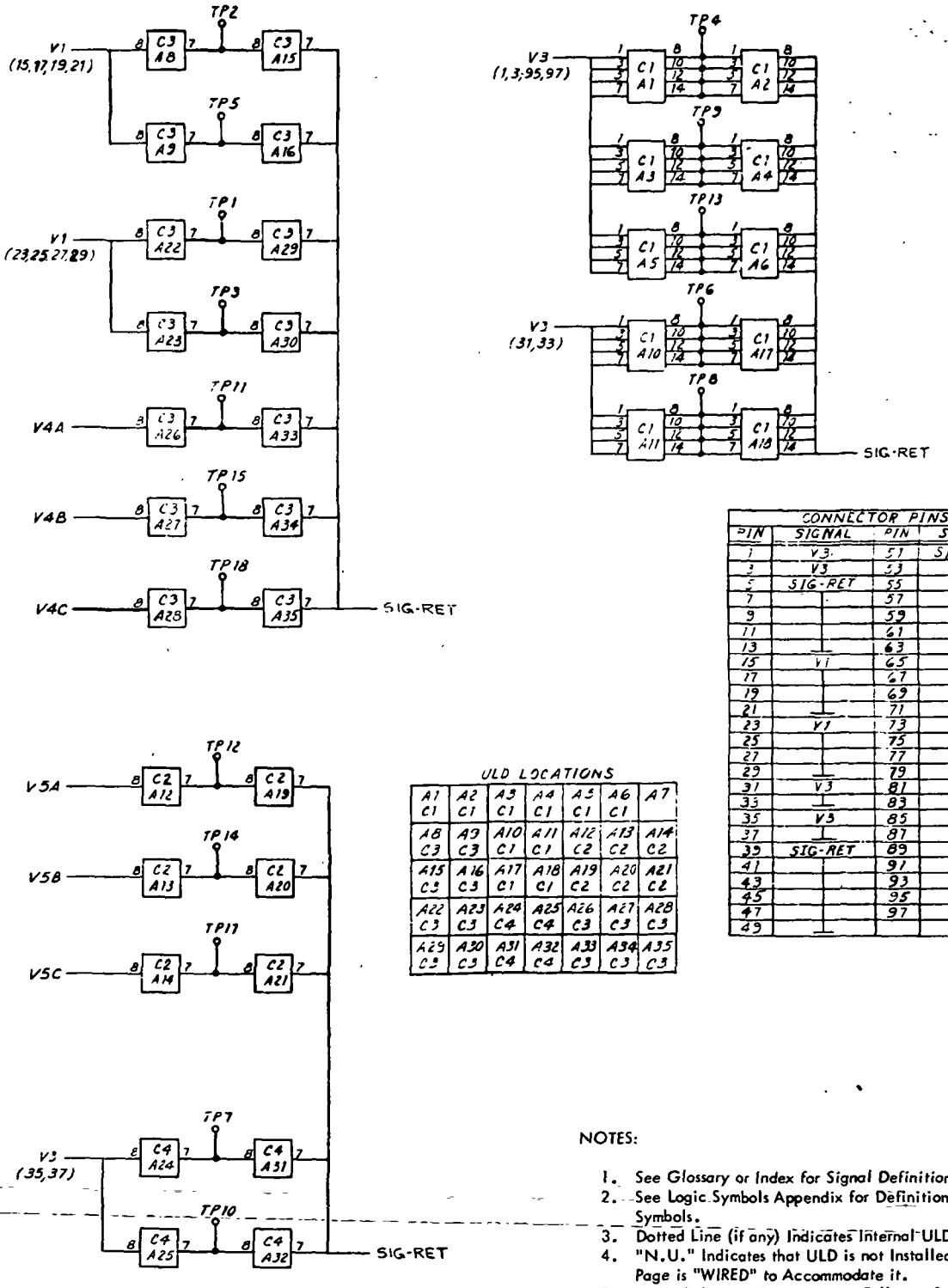
CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
1	V1	51	SIG RET
3	V1	53	
5	SIG RET	55	
7		57	
9		59	
11		61	
13		63	
15	V1	65	V1
17		67	
19		69	
21		71	
23	V1	73	
25		75	
27		77	V1
29		79	
31	V1	81	
33	V1	83	
35		85	
37		87	
39	SIG RET	89	
41		91	
43		93	
45		95	V1
47		97	V1
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A1A13 Side A.
6. This Drawing Derived From IBM DWG NO. 6112947-REL(66123EV)

Figure 10-30. Decoupling Capacitors Logic Diagram (Sheet 1 of 5)



ULD LOCATIONS

A1 C1	A2 C1	A3 C1	A4 C1	A5 C1	A6 C1	A7
A8 C3	A9 C3	A10 C1	A11 C1	A12 C2	A13 C2	A14 C2
A15 C3	A16 C3	A17 C1	A18 C1	A19 C2	A20 C2	A21 C2
A22 C3	A23 C3	A24 C4	A25 C4	A26 C3	A27 C3	A28 C3
A29 C3	A30 C3	A31 C4	A32 C4	A33 C3	A34 C3	A35 C3

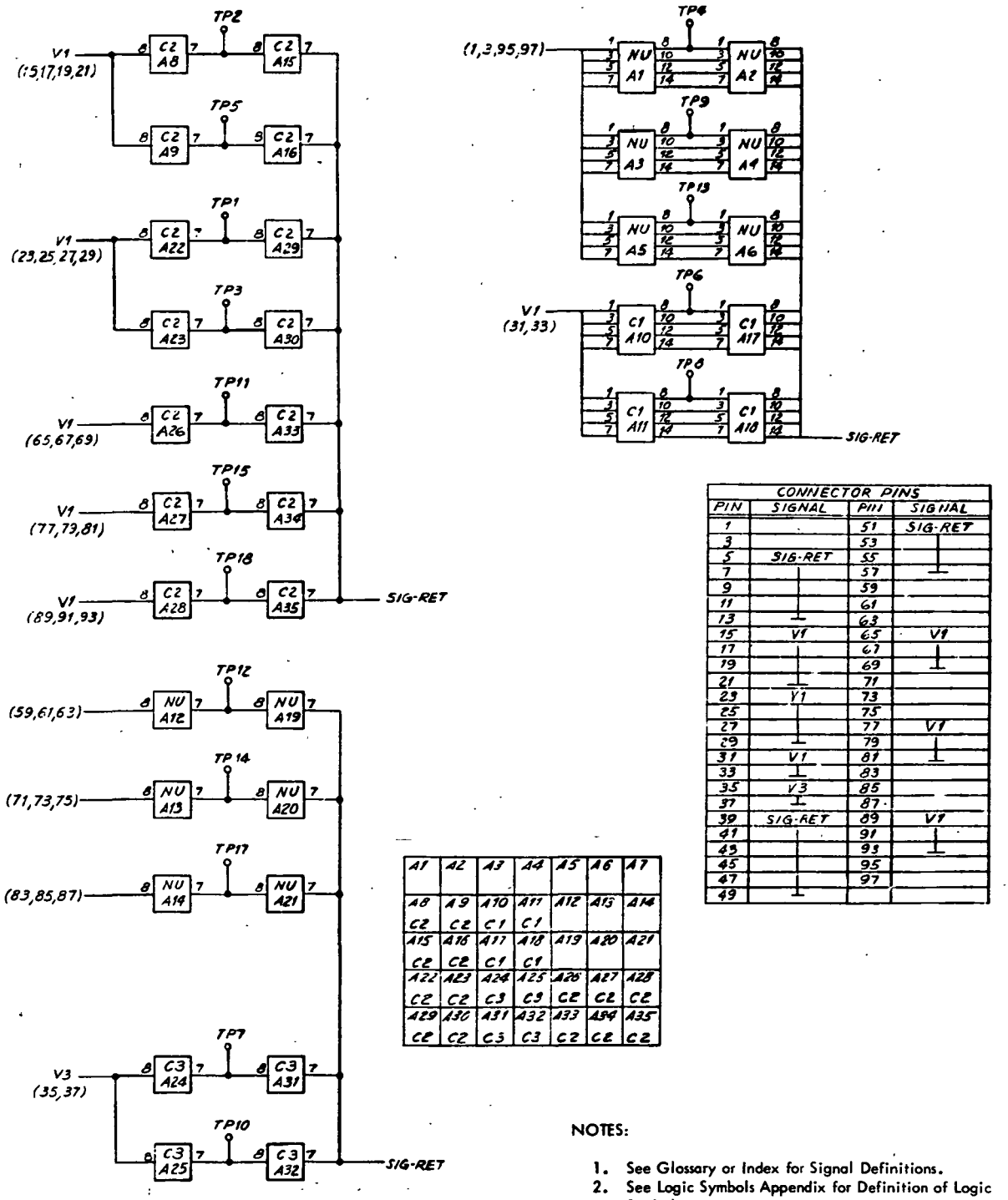
CONNECTOR PINS

PIN	SIGNAL	PIN	SIGNAL
1	V3	51	SIG-RET
3	V3	53	
5	SIG-RET	55	
7		57	
9		59	V5A
11		61	
13		63	
15	V1	65	V4A
17		67	
19		69	
21		71	V5B
23	V1	73	
25		75	
27		77	V4B
29		79	
31	V3	81	
33		83	V5C
35	V3	85	
37		87	
39	SIG-RET	89	V4C
41		91	
43		93	
45		95	V3
47		97	V3
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A25 Side A, 2A3A32 Side A, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112948-REL(66123DJ)

Figure 10-30. Decoupling Capacitors Logic Diagram (Sheet 2)



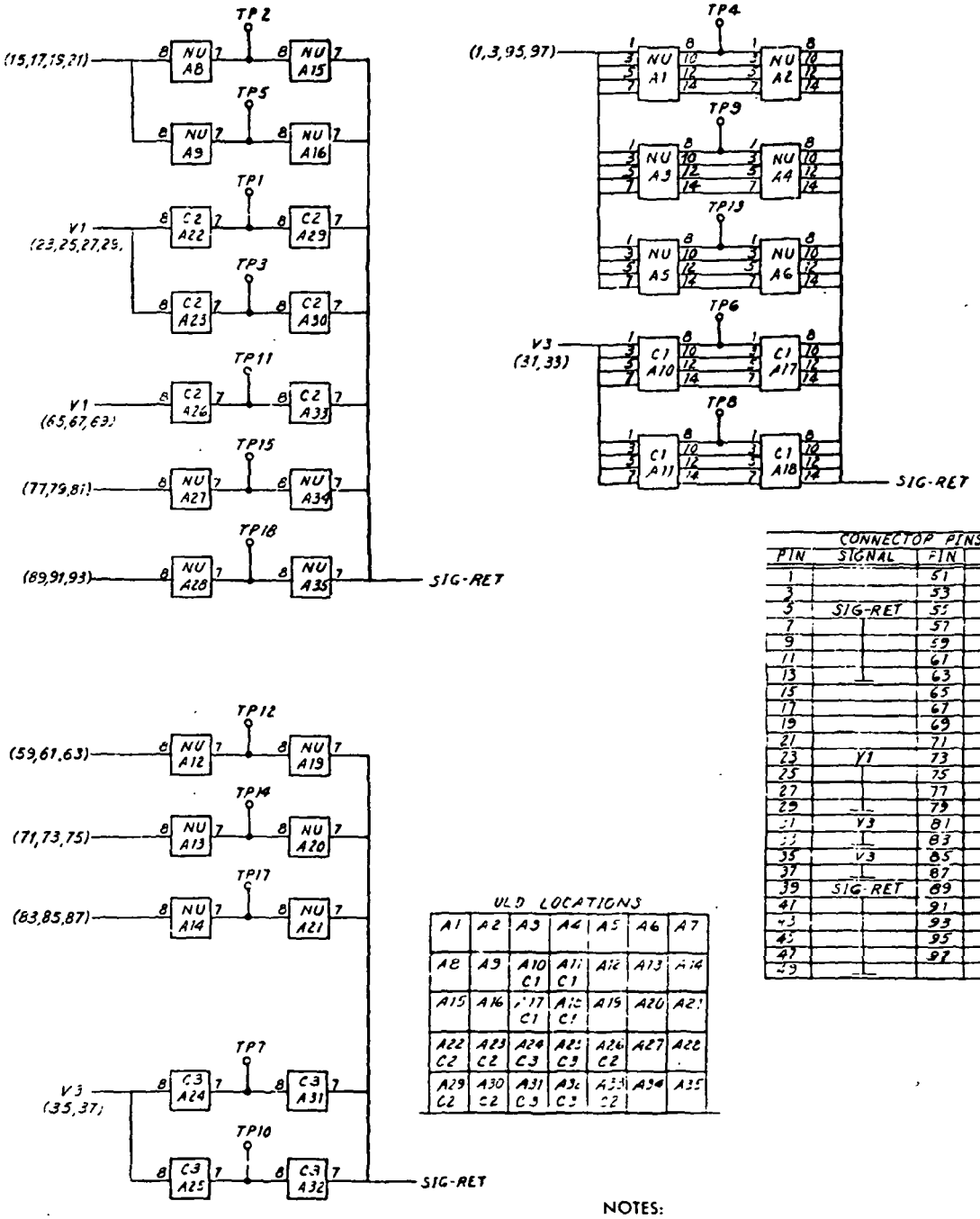
A1	A2	A3	A4	A5	A6	A7
A8 C2	A9 C2	A10 C1	A11 C1	A12	A13	A14
A15 C2	A16 C2	A17 C1	A18 C1	A19	A20	A21
A22 C2	A23 C2	A24 C3	A25 C3	A26 C2	A27 C2	A28 C2
A29 C2	A30 C2	A31 C3	A32 C3	A33 C2	A34 C2	A35 C2

CONNECTOR PINS			
PIN	SIGNAL	P111	SIGNAL
1		51	SIG-RET
3		53	
5	SIG-RET	55	
7		57	
9		59	
11		61	
13		63	
15	V1	65	V1
17		67	
19		69	
21		71	
23	V1	73	
25		75	
27		77	V1
29		79	
31	V1	81	
33		83	
35	V3	85	
37		87	
39	SIG-RET	89	V1
41		91	
43		93	
45		95	
47		97	
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A2A30 Side A.
6. This Drawing Derived From IBM DWG NO. 6112949-REL(66123EV)

Figure 10-30. Decoupling Capacitors Logic Diagram (Sheet 3)



ULD LOCATIONS

A1	A2	A3	A4	A5	A6	A7
A8	A9	A10 C1	A11 C1	A12	A13	A14
A15	A16	A17 C1	A18 C1	A19	A20	A21
A22 C2	A23 C2	A24 C3	A25 C3	A26 C2	A27	A28
A29 C2	A30 C2	A31 C3	A32 C3	A33 C2	A34	A35

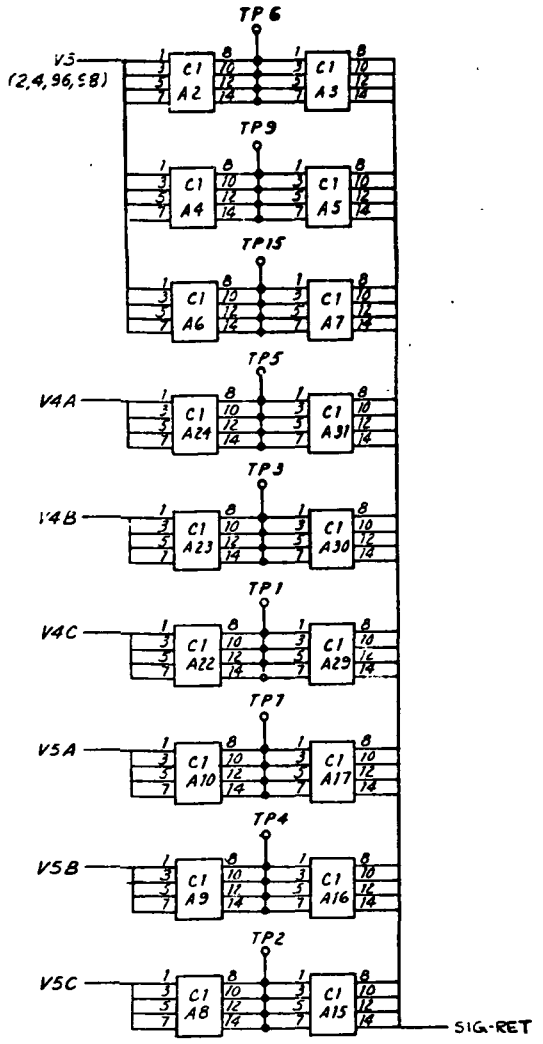
CONNECTOR PINS

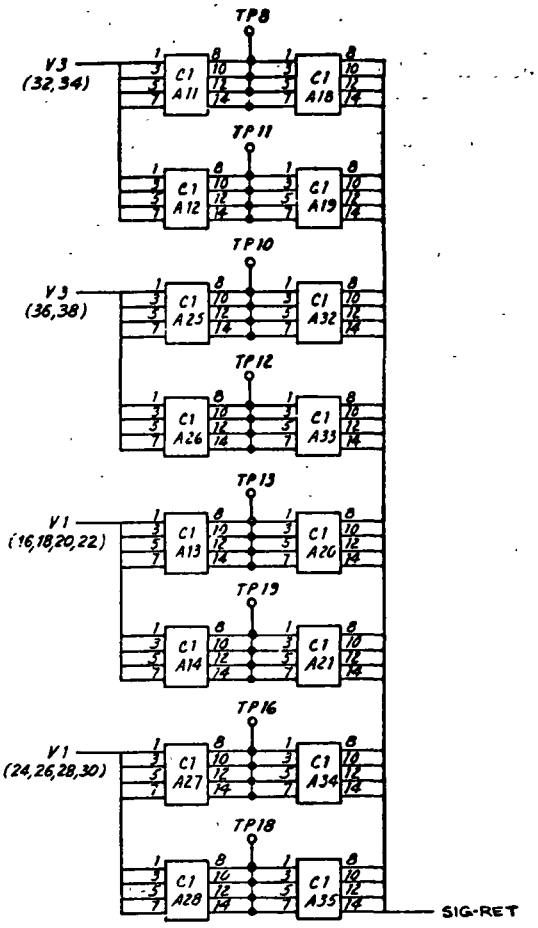
PIN	SIGNAL	PIN	SIGNAL
1		51	SIG-RET
3		53	
5	SIG-RET	55	
7		57	
9		59	
11		61	
13		63	
15		65	V1
17		67	
19		69	
21		71	
23	V1	73	
25		75	
27		77	
29		79	
31	V3	81	
33		83	
35	V3	85	
37		87	
39	SIG-RET	89	
41		91	
43		93	
45		95	
47		97	
49			

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A4A27 Side A.
6. This Drawing Derived From IBM DWG NO. 6112957-REL(66123EV)

Figure 10-30. Decoupling Capacitors Logic Diagram (Sheet 4)





CONNECTOR PINS			
PIN	SIGNAL	PIN	SIGNAL
2	V3	52	SIG RET
4	V3	54	
6	SIG-RET	56	
8		58	
10		60	V5A
12		62	
14		64	
16	V1	66	V4A
18		68	
20		70	
22		72	V5B
24	V1	74	
26		76	
28		78	V4B
30		80	
32	V3	82	
34		84	V5C
36	V3	86	
38		88	
40	SIG-RET	90	V4C
42		92	
44		94	
46		96	V3
48		98	V3
50			

ULD LOCATIONS

A1	A2 C1	A3 C1	A4 C1	A5 C1	A6 C1	A7 C1
A8 C1	A9 C1	A10 C1	A11 C1	A12 C1	A13 C1	A14 C1
A15 C1	A16 C1	A17 C1	A18 C1	A19 C1	A20 C1	A21 C1
A22 C1	A23 C1	A24 C1	A25 C1	A26 C1	A27 C1	A28 C1
A29 C1	A30 C1	A31 C1	A32 C1	A33 C1	A34 C1	A35 C1

NOTES:

1. See Glossary or Index for Signal Definitions.
2. See Logic Symbols Appendix for Definition of Logic Symbols.
3. Dotted Line (if any) Indicates Internal ULD Connection.
4. "N.U." Indicates that ULD is not Installed Although Page is "WIRED" to Accommodate it.
5. Prefix Reference Designator as Follows: 2A3A25 Side B, 2A3A32 Side B, Respectively.
6. This Drawing Derived From IBM DWG NO. 6112958-REL(66123DK)

Figure 10-30. Decoupling Capacitors Logic Diagram (Sheet 5)

SIGNAL	FIGURE NO.	SHEET NO.
500 KCA	10-7	3,4
500 KCB	10-7	5,6
A1D THRU A9D	10-3	1,2
A1DVA,B,C	10-29	31,32
A1DVNA,B,C	10-29	31,32
A2DVA,B,C	10-29	31,32
A2DVNA,B,C	10-29	31,32
A3CR	10-15	3,4
A3DVA,B,C	10-29	29,30
A3DVNA,B,C	10-29	29,30
A3RS	10-15	3,4
A4CR THRU A7CR	10-15	1,2
A4DVA,B,C	10-29	31,32
A4DVNA,B,C	10-29	31,32
A5DVA,B,C	10-29	25,26
A5DVNA,B,C	10-29	27,28
A6DVA,B,C	10-29	21,22
A6DVNA,B,C	10-29	23,24
A7DVA,B,C	10-29	17,18
A7DVNA,B,C	10-29	19,20
A8DVA,B,C	10-29	5,6
A8DVNA,B,C	10-29	7,8
A9DVA,B,C	10-29	9,10
ABD	10-1	5,6
AC1P	10-14	12
AC1R	10-14	12
AC2C	10-14	12
AC2P	10-14	13
AC2R	10-14	12
AC3P	10-14	11
AC3R	10-14	11
ADI	10-24	1,2
AD	10-1	5,6
ADVA,B,C	10-29	13,14
ADVNA,B,C	10-29	15,16
AF1P	10-14	13
AF1R	10-14	13
AF2P	10-14	10
AF2R	10-14	10
AF3C	10-14	10
AF3P	10-14	11
AF3R	10-14	10
AQA	10-18	3,4
AQB	10-18	5,6
AQC	10-18	7,8
ARA	10-18	3,4
ARB	10-18	5,6
ARC	10-18	7,8
ATBP	10-8	1,2
ATBR	10-8	3,4
ATBY	10-8	5,6
BDI	10-24	1,2
BES01,02	10-8	9,10
BGTF1A	10-18	3,4
BGTF1B	10-18	5,6
BGTF1C	10-18	7,8
BOR2,3	10-20	1-4
BORLA	10-17	1,2
BORLB	10-17	3,4
BR01 THRU 08	10-27	9
BR01X THRU 08X	10-27	9
BR09 THRU 11	10-27	10
BR09X THRU 11X	10-27	10
BR12 THRU 15	10-27	8
BR12X THRU 15X	10-27	8
BR16 THRU 19	10-27	7
BR16X THRU 19X	10-27	7
BR20 THRU 23	10-27	5
BR20X THRU 23X	10-27	5
BR24 THRU 26	10-27	6
BR24X THRU 26X	10-27	6
BRD01H THRU 11H	10-27	2
BRD01	10-26	11,12
BRD02	10-26	9,10
BRD03	10-26	7,8
BRD04	10-26	3,4
BRD05	10-26	5,6
BRD06	10-26	1,2
BRD07	10-26	11,12
BRD08	10-26	9,10
BRD09	10-26	7,8
BRD10	10-26	3,4
BRD11	10-26	5,6
BRD12A	10-26	5,6
BRD12B	10-26	3,4
BRD12HA THRU 26HA	10-27	3
BRD12HB THRU 26HB	10-27	4
BRD12HC THRU 26HC	10-27	1
BRD13A	10-26	1,2
BRD13B THRU 18B	10-26	1,2
BRD14A	10-26	1,2
BRD15A	10-26	5,6
BRD16A	10-26	1,2
BRD17A	10-26	5,6
BRD18A	10-26	1,2
BRD19A	10-26	5,6
BRD19B	10-26	3,4
BRD20A	10-26	1,2
BRD20B	10-26	1,2
BRD21A	10-26	5,6
BRD21B THRU 26B	10-26	3,4
BRD22A	10-26	5,6
BRD23A	10-26	1,2
BRD24A	10-26	5,6
BRD25A	10-26	1,2
BRD26A	10-26	5,6
BRR1	10-26	1,2
BRR2A	10-26	1,2
BU1P	10-14	5
BU2C	10-14	1
BU2P	10-14	2
BU3C	10-14	3
BU3P	10-14	5

Figure 10-31. Signal Origin List (Sheet 1 of 7)

SIGNAL	FIGURE NO.	SHEET NO.
BU4C	10-14	7
BU4P	10-14	8
C1GT1,2,3	10-22	7,8
C1RD	10-21	1,2
C1R	10-21	1,2
C2GT1,2,3	10-22	7,8
C2RD	10-20	1-4
C2R	10-21	1,2
C3GT1,2,3	10-22	7,8
C3RD	10-20	1-4
C3R	10-21	1,2
C4GT1,2,3	10-22	7,8
C4RDA	10-18	3,4
C4RDB	10-18	5,6
C4RDC	10-18	7,8
C4RDVA	10-18	3,4
C4RDVB	10-18	5,6
C4RDVC	10-18	7,8
C4R	10-21	1,2
CA4	10-16	3,4
CB4	10-16	7,8
CCA1 THRU CCA4	10-16	1,2
CCA5A,B,C	10-16	1,2
CCA6A THRU 11A	10-16	3,4
CCA6B THRU 11B	10-16	3,4
CCA6C THRU 11C	10-16	3,4
CCAS2N	10-16	1,2
CCAS	10-16	3,4
CCB1 THRU 4	10-16	5,6
CCB5,A,B,C	10-16	5,6
CCB6A THRU 11A	10-16	7,8
CCB6B THRU 11B	10-16	7,8
CCB6C THRU 11C	10-16	7,8
CCBS	10-16	7,8
CCFHC	10-1	7,8
CCFH	10-1	7,8
CCFHVA,B,C	10-29	33,34
CCFHVNA,B,C	10-29	33,34
CCR	10-15	1,2
CCSA	10-17	1,2
CCSB	10-17	3,4
CCSLA	10-17	1,2
CCSLB	10-17	3,4
CDIFA	10-17	1,2
CDIFB	10-17	3,4
CE01A	10-14	3
CE01B	10-14	1
CE02A	10-14	5
CE02B	10-14	2
CE03A	10-14	2
CE03B	10-14	3
CE04A	10-14	6
CE04B	10-14	4
CE05A	10-14	4
CE05B	10-14	6
CE06A	10-14	3
CE06B	10-14	5
CE07A	10-14	8
CE07B	10-14	7
CE08A	10-14	7
CE08B	10-14	8
CE09A	10-14	9
CE09B	10-14	9
CE10A	10-14	2
CE10B	10-14	1
CE11A	10-14	4
CE11B	10-14	7
CE12A	10-14	5
CE12B	10-14	1
CE13A	10-14	8
CE13B	10-14	6
CE14A	10-14	12
CE14B	10-14	13
CE15A	10-14	10
CE15B	10-14	12
CE16A	10-14	10
CE16B	10-14	10
CE17A	10-14	12
CE17B	10-14	11
CE18A	10-14	13
CE18B	10-14	11
CE19A	10-14	11
CE19B	10-14	13
CES01	10-14	1
CES02	10-14	2
CES03	10-14	3
CES04	10-14	4
CES05	10-14	6
CES06	10-14	5
CES07	10-14	7
CES08	10-14	8
CES09	10-14	9
CES10	10-14	2
CES11	10-14	4
CES12	10-14	5
CES13	10-14	8
CES14	10-14	13
CES15	10-14	12
CES16	10-14	10
CES17	10-14	11
CES18	10-14	13
CES19	10-14	11
CF	10-15	3,4
CG1R	10-14	5
CG1 THRU 8	10-8	7,8
CG2R	10-14	1
CG3R	10-14	3
CG4R	10-14	7
CGAP	10-14	9
CGBP	10-14	9
CODE	10-3	9,10
CODG	10-3	15,16
CODGVA,B,C	10-29	17,18

Figure 10-31. Signal Origin List (Sheet 2)

SIGNAL	FIGURE NO.	SHEET NO.
CODRR	10-15	1,2
CODRS	10-15	3,4
CPR1N,2N	10-7	7,8
CPR1,2	10-8	9,10
CR01N,02N	10-11	1-4
CR03NA,04NA	10-11	5,6
CR05N	10-11	7,8
CR06N	10-11	9,10
CR07N	10-11	11,12
CR08N	10-11	13,14
CR09N	10-11	15,16
CR10N	10-11	17,18
CR11N	10-11	19,20
CR12N	10-11	21,22
CR13N	10-11	23,24
CR14N	10-11	25,26
CRCA	10-3	5-8
CRCAVA,B,C	10-29	5,6
CRI1A,2A	10-10	1,2
CRI1NA,2NA	10-19	5,6
CRI1NB,2NB	10-19	7,8
CRT	10-15	3,4
CSP	10-8	1,2
CSRX	10-8	3,4
CSTNA	10-18	3,4
CSTNB	10-18	5,6
CSTNC	10-18	7,8
CSYX	10-8	5,6
DAINF	10-3	1,2
DARAC	10-3	3,4
DARA	10-3	5-8
DARO	10-3	1,2
DATA1NA THRU 4NA	10-12	1,2
DATAA	10-12	1,2
DATAB	10-12	3,4
DATAVA	10-12	1,2
DC1R THRU 4R	10-23	1,2
DC1S THRU 4S	10-22	5,6
DCAL	10-22	3,4
DCCB1 THRU B4	10-16	5,6
DDC1R THRU 4R	10-23	1,2
DDC1	10-22	3,4
DDC2	10-22	3,4
DDCA1 THRU A4	10-16	1,2
DDI1A	10-29	25-28
DDI1BN	10-29	21-24
DDI1B	10-29	21-24
DDI1CN	10-29	9-12
DDI1C	10-29	9-12
DDI2AN	10-29	17-20
DDI2A	10-29	17-20
DDI2BN	10-29	5-8
DDI2B	10-29	5-8
DDI3A	10-19	5,6
DDI3B	10-18	3,4
DDI4N	10-29	29-32
DDI4	10-29	31,32
DDI5N	10-29	1-4
DDI5	10-29	1-4
DDI6N	10-29	33-36
DDI6	10-29	35,36
DDI7N	10-29	13-16
DDI7	10-29	13-16
DDI8	10-12	1,2
DDIHLT	10-18	3,4
DDIN	10-23	1,2
DDIP	10-23	1,2
DDLO	10-23	1,2
DDO	10-29	25-28
DECO	10-8	7,8
DIA	10-3	5-8
DINO1A	10-10	1,2
DINO1N	10-11	7,8
DINO2AA,02BA	10-10	1,2
DINO2AN,02BN	10-11	9,10
DINO3A	10-10	1,2
DINO3N	10-11	11,12
DINO4A	10-10	3,4
DINO4B THRU 08B	10-10	7,8
DINO4C THRU 08C	10-10	9,10
DINO4N	10-11	13,14
DINO5A THRU 07A	10-10	5,6
DINO5N	10-11	15,16
DINO6N	10-11	17,18
DINO7N	10-11	19,20
DINO8A,09A	10-10	3,4
DINO8N	10-11	21,22
DINO9B	10-10	5,6
DINO9C	10-10	7,8
DINO9N	10-11	23,24
DIN10A THRU 24A	10-10	1,2
DIN10N	10-11	25,26
DIN11N,12N	10-11	1-4
DIN13NA,14NA	10-11	5,6
DIN15N	10-11	7,8
DIN16N	10-11	9,10
DIN17N	10-11	11,12
DIN18N	10-11	13,14
DIN19N	10-11	15,16
DIN20N	10-11	17,18
DIN21N	10-11	19,20
DIN22N	10-11	21,22
DIN23N	10-11	23,24
DIN24N	10-11	25,26
DINF	10-3	1,2
DINFVA,B,C	10-29	1,2
DINFVNA,B,C	10-29	3,4
DINP	10-21	1,2
DIN	10-22	1,2
DIS1A THRU 7A	10-10	3,4
DIS1B THRU 7B	10-10	5,6
DIS1C,2C	10-10	9,10
DIS1N	10-11	11,12

Figure 10-31. Signal Origin List (Sheet 3)

SIGNAL	FIGURE NO.	SHEET NO.
DIS2N	10-11	13,14
DIS3C,4C	10-10	7,8
DIS3N	10-11	15,16
DIS4N	10-11	17,18
DIS5C,6C	10-10	9,10
DIS5N	10-11	19,20
DIS6N	10-11	21,22
DIS7C	10-10	7,8
DIS7N	10-11	23,24
DIS8A	10-10	5,6
DIS8B	10-10	7,8
DIS8C	10-10	9,10
DIS8N	10-11	25,26
DISA	10-3	5-8
DISD3A	10-19	5,6
DISD8	10-12	1,2
DLO	10-21	1,2
DLS	10-23	1,2
DM01-02	10-22	3,4
DM02B	10-9	11,12
DM03A	10-9	11,12
DM03B	10-9	1,2
DM04A	10-9	1,2
DM04B	10-9	9,10
DM05A	10-9	11,12
DM05B	10-9	7,8
DM06A	10-9	1,2
DM06B	10-9	3,4
DM07A	10-9	9,10
DM07B	10-9	5,6
DM08A	10-9	7,8
DM08B	10-22	3,4
DM09A	10-9	9,10
DM10A	10-9	7,8
DM11A	10-9	3,4
DM12A	10-9	3,4
DM13A	10-9	5,6
DM14A	10-9	5,6
DO01N	10-22	3,4
DO01,02	10-4	7,8
DO02N	10-9	11,12
DO03N	10-9	1,2
DO03 THRU 05	10-4	6
DO04N	10-9	11,12
DO05N	10-9	1,2
DO06N	10-9	9,10
DO06	10-4	5
DO07N	10-9	7,8
DO07	10-4	6
DO08N	10-9	9,10
DO08 THRU 10	10-4	5
DO09N	10-9	7,8
DO10N,11N	10-9	3,4
DO11 THRU 13	10-4	7,8
DO12N,13N	10-9	5,6
DOMC1	10-22	3,4
DOMC2	10-22	3,4

SIGNAL	FIGURE NO.	SHEET NO.
DOMD	10-22	3,4
DOMS	10-9	13,14
DOR 1H THRU 6H	10-4	1,2
DOR 1 THRU 6	10-4	1,2
DOR 7H THRU 13H	10-4	3,4
DOR 7 THRU 13	10-4	1,2
DOR	10-3	5-8
DOS	10-3	5-8
DPBR	10-2	5,6
DSAN,BN	10-9	13,14
DSD	10-9	13,14
DT1,2,3	10-22	1,2
DTPB	10-13	1,2
ECSA	10-2	5,6
ECSB	10-2	5,6
EM14 THRU EM26	10-2	3,4
EM1 THRU 13	10-2	1,2
EMA	10-3	11,12
EMRG1,2	10-2	1,2
EMRG3,4	10-2	3,4
EMRS1	10-2	1,2
EMRS2	10-2	3,4
ERRS	10-2	5,6
ETCR	10-2	5,6
ETSD	10-2	5,6
ETTS	10-2	5,6
FG1P	10-14	1
FG1R	10-14	1
FG2P	10-14	2
FG2R	10-14	2
FG3P	10-14	3
FG3R	10-14	3
FG4C	10-14	6
FG4P	10-14	4
FG4R	10-14	6
G1D THRU G7D	10-1	5,6
G1DVA,B,C	10-29	25,26
G1DVNA,B,C	10-29	25,26
G2DVA,B,C	10-29	25,26
G2DVNA,B,C	10-29	27,28
G3DVA,B,C	10-29	27,28
G3DVNA,B,C	10-29	27,28
G4DVA,B,C	10-29	21,22
G4DVNA,B,C	10-29	21,22
G5DVA,B,C	10-29	21,22
G5DVNA,B,C	10-29	23,24
G5GC	10-1	5,6
G6DVA,B,C	10-29	23,24
G6DVNA,B,C	10-29	23,24
G7DVA,B,C	10-29	17,18
G7DVNA,B,C	10-29	17,18
GC01N,02N	10-11	1-4
GC03NA,04NA	10-11	5,6
GC05N	10-11	7,8
GC06N	10-11	9,10
GC07N	10-11	11,12

Figure 10-31. Signal Origin List (Sheet 4)

SIGNAL	FIGURE NO.	SHEET NO.
GC08N	10-11	13,14
GC09N	10-11	15,16
GC10N	10-11	17,18
GC11N	10-11	19,20
GC12N	10-11	21,22
GC13N	10-11	23,24
GC14N	10-11	25,26
GCSYNC	10-10	3,4
GCSYN	10-22	1,2
HALTA	10-18	3,4
HALTB	10-18	5,6
HALTC	10-18	7,8
HALTVA	10-18	3,4
HALTVB	10-18	5,6
HALTVC	10-18	7,8
HCA1	10-8	1,2
HCA2	10-8	3,4
HCA3	10-8	5,6
HCB1A	10-8	1,2
HCB2A	10-8	3,4
HCB3A	10-8	5,6
HLTA	10-10	3,4
HLTB	10-10	7,8
HLTC	10-10	9,10
HS1P	10-14	6
HS1R	10-14	6
HS2P	10-14	4
HS2R	10-14	4
HS3P	10-14	7
HS3R	10-14	7
HS4P	10-14	8
HS4R	10-14	8
ICR1	10-6	1,2
ICR2A THRU 6A	10-6	1,2
ICR3B THRU 6B	10-6	3,4
ICR7 THRU 13	10-6	5,6
ICR	10-3	5-8
ICRV1A,B,C	10-29	5,6
ICRV2A,B,C	10-29	7,8
ICSDN	10-11	19,20
ICSD	10-11	21,22
ICS	10-11	19,20
INFLA	10-3	15,16
INFO	10-3	15,16
INFOV1A,B,C	10-29	1,2
INFOV2A,B,C	10-29	3,4
INTCA	10-19	5,6
INTCB	10-19	7,8
INTCVA	10-19	5,6
INTCVB	10-19	7,8
INTR1A	10-10	3,4
INTR1B,2B	10-10	7,8
INTR1C THRU 4C	10-10	9,10
INTR1N THRU 6N	10-19	1,2
INTR2A	10-10	5,6
INTR3A THRU 7A	10-10	3,4
INTR3B THRU 6B	10-10	5,6
INTR5C,6C	10-10	7,8
INTR7B	10-10	7,8
INTR7C	10-10	9,10
INTR7NA	10-19	5,6
INTR7NB	10-19	7,8
INTR7NC	10-19	9,10
ITS	10-20	1-4
L1AA	10-3	11,12
L1AB	10-3	9,10
L1PA THRU L5PA	10-7	3,4
L1PB THRU L5PB	10-7	5,6
L2AA	10-3	11,12
L2AB	10-3	9,10
L3AA	10-3	11,12
L3AB	10-3	9,10
L4AA	10-3	11,12
L4AB	10-3	9,10
L5AA	10-3	11,12
L5AB	10-3	9,10
LCB1A,2A	10-17	1,2
LCB1B,2B	10-17	3,4
LGAC	10-3	3,4
LGA	10-3	5-8
LGAVA,B,C	10-29	7,8
LP	10-7	3,4
LR1A THRU 4A	10-7	3,4
LR1B THRU 4B	10-7	5,6
LR1C THRU 4C	10-7	7,8
LR5 THRU 9	10-7	1,2
LRRA	10-7	3,4
LRRB	10-7	5,6
LRR	10-7	1,2
LTRD	10-3	11,12
LTR	10-3	15,16
LTRVA,B,C	10-29	1,2
MBYPDA	10-12	1,2
MCFT1A THRU 3A	10-19	5,6
MCFT1B THRU 3B	10-19	7,8
ML01-02	10-11	1-4
ML03A	10-11	5,6
ML04A	10-11	5,6
ML05	10-11	7,8
ML06	10-11	9,10
ML07	10-11	11,12
ML08	10-11	13,14
ML09	10-11	15,16
ML10	10-11	17,18
ML11	10-11	19,20
ML12	10-11	21,22
ML13	10-11	23,24
MLA	10-3	15,16
MLAVA,B,C	10-29	3,4
MOD1	10-27	6
MOD2,3	10-27	9
MOD4,5	10-27	7
MOD6	10-27	6

Figure 10-31. Signal Origin List (Sheet 5)

SIGNAL	FIGURE NO.	SHEET NO.
MODA	10-3	9,10
MODR1H	10-27	3
MODR1	10-26	11,12
MODR2H	10-27	4
MODR2	10-26	9,10
MODR3H	10-27	3
MODR3	10-26	7,8
MODR4H	10-27	4
MODR4	10-26	3,4
MODR5H	10-27	3
MODR5	10-26	5,6
MODR6H	10-27	2
MODR6	10-26	1,2
MODRR	10-26	1,2
N03TLM	10-28	2
N20TLM	10-28	1
NCS1A THRU 4A	10-7	3,4
NCS1B THRU 4B	10-7	5,6
NCS1R THRU 4R	10-7	7,8
NCS5 THRU 8	10-7	1,2
NVRO	10-8	7,8
OCINTNA	10-19	5,6
OCINTNB	10-19	7,8
OCINTNC	10-19	9,10
OCRB	10-3	15,16
OCRC	10-3	13,14
OCRHA	10-27	3
OCRHB	10-27	4
OCRHC	10-27	1
OCR	10-27	6
P06TLM	10-28	1
P12TLM	10-28	1
P20TLM	10-28	2
P6STLM	10-28	2
PAA	10-1	7,8
PAAV1A,B,C	10-29	11,12
PAAV2A,B,C	10-29	13,14
PAAVNA,B,C	10-29	11,12
PABG1	10-1	5,6
PABG1VA,B,C	10-29	11,12
PARS	10-3	1,2
PARSV1A,B,C	10-29	7,8
PARSV2A,B,C	10-29	5,6
PBA	10-1	7,8
PBAV1A,B,C	10-29	13,14
PBAV2A,B,C	10-29	11,12
PBAVNA,B,C	10-29	13,14
PBG2	10-1	7,8
PBG2V1A,B,C	10-29	9,10
PBG2V2A,B,C	10-29	15,16
PBGC	10-1	7,8
PBR	10-2	5,6
PCA	10-1	7,8
PCAV1A,B,C	10-29	15,16
PCAV2A,B,C	10-29	9,10
PCAVNA,B,C	10-29	15,16
PCG2	10-1	5,6
PCG2V1A,B,C	10-29	19,20
PCG2V2A,B,C	10-29	19,20
PCG2V3A,B,C	10-29	19,20
PCINF	10-3	15,16
PCINFV1A,B,C	10-29	3,4
PCINFV2A,B,C	10-29	1,2
PCR1 THRU 4	10-15	3,4
PCRN	10-15	3,4
PCS1A THRU 4A	10-7	3,4
PCS1B THRU 4B	10-7	5,6
PCS1R THRU 4R	10-7	7,8
PCS5 THRU 8	10-7	1,2
PIOD	10-3	1,2
PIODVA,B,C	10-29	29,30
PS1A,B,N	10-9	11,12
PS2A,B,N	10-9	1,2
PS3AN,BN	10-9	9,10
PS3	10-9	9,10
PS4AN,BN	10-9	7,8
PS4	10-9	7,8
PS5A,B,N	10-9	3,4
PSTP1 THRU 4	10-15	1,2
PSTPN	10-15	1,2
PVRO	10-8	7,8
QB,QC	10-18	1,2
RB,RC	10-18	1,2
RECA	10-1	7,8
RECAVA,B,C	10-29	35,36
RECAVNA,B,C	10-29	35,36
RECB	10-1	7,8
RECC	10-1	7,8
RECCVA,B,C	10-29	35,36
RECCVNA,B,C	10-29	35,36
RESM	10-1	5,6
RESMVA,B,C	10-29	9,10
REXCC	10-1	7,8
REXC	10-1	7,8
REXCVA,B,C	10-29	35,36
REXCVNA,B,C	10-29	35,36
RT1X	10-27	10
RT1,2	10-27	8
RT3,4	10-27	5
RT5	10-27	9
RTR1H,2H	10-27	2
RTR1 THRU 5	10-24	1,2
RTR3H	10-27	1
RTR4H,5H	10-27	2
RTRR	10-24	1,2
SCA	10-7	7,8
SCB	10-7	7,8
SINTAC	10-19	3,4
SINTBC	10-19	9,10
SINTB	10-19	7,8
SINTNA	10-19	5,6
SINT	10-19	1,2,5,6
SSO1N	10-9	11,12

Figure 10-31. Signal Origin List (Sheet 6)

SIGNAL	FIGURE NO.	SHEET NO.
SS01 THRU 08	10-5	7,8
SS02N	10-9	1,2
SS03N	10-9	11,12
SS04N	10-9	1,2
SS05N	10-9	9,10
SS06N	10-9	7,8
SS07N	10-9	9,10
SS08N	10-9	7,8
SS09N,10N	10-9	3,4
SS09 THRU 13	10-5	7
SS11N,12N	10-9	5,6
SS13N	10-22	3,4
SS14,15	10-5	8
SSA	10-3	5-8
SSDO	10-3	11,12
SSEP	10-22	1,2
SSFB1A	10-10	3,4
SSFB1B	10-10	5,6
SSFB1C,2C	10-10	9,10
SSFB1N	10-11	25,26
SSFB2A	10-10	5,6
SSFB2B	10-10	7,8
SSFB2N,3N	10-11	1-4
SSFB3A	10-10	3,4
SSFB3B	10-10	5,6
SSFB3C	10-10	7,8
SSFB4A	10-10	3,4
SSFB4B THRU 8B	10-10	7,8
SSFB4C THRU 8C	10-10	9,10
SSFB4NA,5NA	10-11	5,6
SSFB5A	10-10	5,6
SSFB6A	10-10	3,4
SSFB6N	10-11	7,8
SSFB7A,8A	10-10	5,6
SSFB7N	10-11	9,10
SSFB8N	10-11	11,12
SSIT1,2,3	10-20	1-4
SSR1H THRU 8H	10-5	1,2
SSR1 THRU 8	10-5	1,2
SSR9H THRU 15H	10-5	3-6
SSR9 THRU 15	10-5	3-6
SSRRA	10-5	1,2
SSRR	10-5	3-6
SSR	10-3	5-8
SSRVA,B,C	10-29	29,30
STP	10-15	1,2
SYNCPN	10-22	1,2
SYNCP	10-22	1,2
TAG1X,2X	10-27	8
TAG1,2	10-27	8
TAG3X,4X	10-27	7
TAG3,4	10-27	7
TAG5X,6X	10-27	5
TAG5,6	10-27	5
TAG7X,8X	10-27	6
TAG7,8	10-27	6
TAGR1H	10-27	1
TAGR1 THRU 8	10-25	1,2
TAGR2H	10-27	1
TAGR3H	10-27	4
TAGR4H	10-27	3
TAGR5H	10-27	2
TAGR6H	10-27	1
TAGR7H,8H	10-27	2
TAGRR	10-25	1,2
TAGS	10-13	1,2
TC2A	10-20	1-4
TC3A	10-19	1,2
TCW	10-22	1,2
TG1N,2N	10-13	1,2
TI	10-20	1-4
TLM	10-3	15,16
TPBH	10-27	2
TPB	10-13	1,2
TPBX	10-27	10
TRPC	10-22	1,2
TRP	10-22	1,2
TS01N	10-11	7,8
TS02N	10-11	9,10
TS03N	10-11	11,12
TS04N	10-11	13,14
TS05N	10-11	15,16
TS06N	10-11	17,18
TS07N	10-11	19,20
TS08N	10-11	21,22
TS09N	10-11	23,24
TS10N	10-11	25,26
TSA	10-3	5-8
TSYN	10-22	1,2
TSYNS	10-22	1,2
TTAA,BA,CA	10-16	1,2
TTAB,BB,CB	10-16	5,6
W1 THRU W8	10-1	1,2
X1 THRU X8	10-1	1,2
Y1 THRU Y8	10-1	3,4
Z1 THRU Z8	10-1	3,4

Figure 10-31. Signal Origin List (Sheet 7)

MIB Reference Designations	Logic Diagram Figure Numbers Panel Assembly Reference Designations							
	2A1	2A2	2A3	2A4	2A5	2A6	2A7	2A8
A1A		10-11						
A1B		10-11						
A2A								
A2B								
A3A		10-11	10-3	10-2	10-14			
A3B	10-4	10-11	10-3	10-13		10-14		10-27
A4A	10-4	10-11	10-29	10-25				
A4B	10-4	10-11	10-29	10-24				
A5A		10-11	10-3	10-20				
A5B		10-12	10-3	10-20				
A6A		10-11		10-20	10-14			
A6B	10-4	10-11				10-14	10-8	10-27
A7A		10-11	10-29	10-2				
A7B		10-11	10-29	10-2				
A8A		10-11	10-1					
A8B		10-22	10-1					
A9A		10-22	10-29		10-14			
A9B	10-4	10-22	10-29				10-8	
A10A								
A10B								
A11A			10-1				10-7	
A11B			10-1			10-14	10-7	
A12A			10-6	10-21	10-14			
A12B	10-4		10-6	10-21				10-27
A13A	10-30							10-27
A13B								10-27
A14A			10-3	10-21				
A14B				10-21				
A15A			10-29		10-14			
A15B			10-29					
A16A			10-3	10-19				
A16B	10-5	10-12	10-3	10-19				10-27
A17A	10-5		10-29	10-19			10-8	
A17B	10-5		10-29	10-19				
A18A	10-5		10-29	10-19	10-14	10-15		
A18B	10-5		10-29	10-19		10-15		
A19A	10-10		10-1	10-26		10-16		
A19B			10-1	10-26		10-16		
A20A		10-23	10-29	10-26				
A20B		10-23	10-29	10-26			10-8	
A21A				10-26	10-14	10-7	10-7	
A21B				10-26				10-27
A22A	10-10	10-9	10-1	10-21				10-27
A22B	10-10	10-9	10-1			10-14		10-27
A23A	10-10		10-6					
A23B	10-10		10-6					
A24A		10-11	10-3	10-18	10-14			
A24B		10-11	10-3	10-18				
A25A			10-30	10-18				
A25B			10-30	10-18		10-28	10-8	10-27
A26A				10-18				
A26B				10-18				
A27A				10-30	10-14			
A27B	10-5		10-3					
A28A								
A28B						10-28	10-8	
A29A			10-29			10-15		
A29B			10-29			10-15		
A30A		10-30	10-1			10-16		
A30B			10-1			10-16		
A31A		10-22	10-29			10-17		
A31B		10-9	10-29			10-17	10-8	
A32A		10-9	10-30				10-7	
A32B		10-9	10-30				10-7	
A33A		10-29	10-1					
A33B		10-9	10-1					

Figure 10-32. Table of Logic Diagrams for Each MIB

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