SATURN V

Laboratory Maintenance Instruction for LTE

Volume III

LVDC Manual Exerciser

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Federal Systems Division
Owego, New York

VOLUME III OF V

Laboratory Maintenance Instructions

SATURN V
LAUNCH VEHICLE DIGITAL COMPUTER AND LAUNCH VEHICLE DATA ADAPTER TEST EQUIPMENT

(International Business Machines Corporation)

Contract NAS 8-11561

VOLUME III

Launch Vehicle Digital Computer Manual Exerciser (IBM Part No. 6902000)

23 OCTOBER 1964

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LIST OF RELATED MANUALS

Equipment	Manufacturer	Manual Title
Power Supply Model M15-50A-0V	Trygon Electronics Corporation	Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-50A-0V.
Power Supply Model M15-15A-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-15A-0V.
Power Supply Model M36-10A-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M36-10A-0V.
Power Supply Model M15-10-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-10-0V.
Power Supply Model M36-5-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M36-5-0V.
Power Supply Model M15-5-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-5-0V.
Power Supply Model M15-30A-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-30A-0V.
Power Supply Model M15-15A-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-15A-0V.
Power Supply Model M15-10-0V		Trygon Electronics, Inc. Instruction and Maintenance Manual, Model M15-10-0V.
Tape Reader Assembly, Model RR-1002B-333	Rheem Electronic Corporation	Rheem Tape Reader, Model RR-1002B, L, R, Operations and Maintenance Manual.
Tape Spooler Assembly, Model RS-500A		Rheem Tape Spooler, Operations and Maintenance Manual.
Automated Logic Diagrams	IBM Corporation	Saturn V LTE – LVDC Manual Exerciser Automated Logic Diagrams.

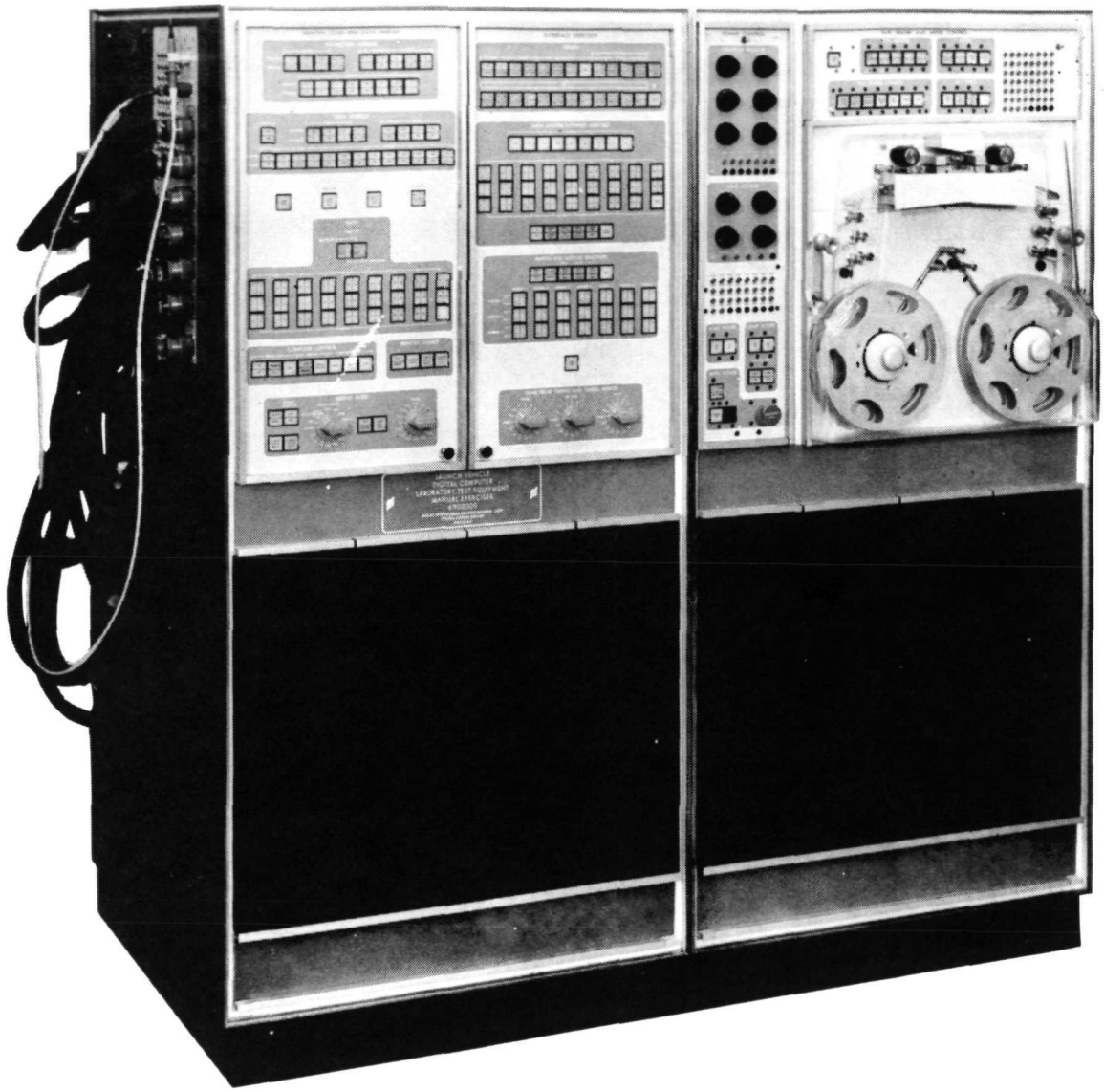


Figure 1-1. Launch Vehicle Digital Computer Manual Exerciser

SECTION I

INTRODUCTION AND DESCRIPTION

1-1. INTRODUCTION.

1-2. PURPOSE OF MANUAL.

1-3. This volume of the manual provides laboratory maintenance instructions for the Saturn V LTE Launch Vehicle Digital Computer Manual Exerciser (hereinafter referred to as the LVDCME), IBM part number 6902000 M1 (see figure 1-1), manufactured by International Business Machines Corporation, Federal Systems Division, Rockville, Maryland.

1-4. Maintenance instructions for those LVDCME assemblies not built or modified by the Federal Systems Division are not included in this manual but are supplied separately. (Refer to the list of related manuals.) Automated Logic Diagrams (ALD's) are not an intregal part of this manual but are referred to (as needed) by their IBM drawing numbers.

1-5. Unusual terms and abbreviations are listed alphabetically in the glossary. A topical index indicates the pages that describe the LVDCME functions and circuits. Both the glossary and the index are located at the back of the volume.

1-6. PURPOSE OF EQUIPMENT.

1-7. The purpose of the LVDCME is to evaluate the Launch Vehicle Digital Computer (LVDC) when the LVDCME is installed in either the ACME or the ASTEC laboratory test equipments (refer to Volume I).

1-8. PART SYMBOLS.

1-9. Symbols for standard electrical and electronic parts conform with military standard MIL-STD-15-1. Nonstandard symbols are defined in the table of part symbols.

1-10. LOGIC SYMBOLS.

1-11. The logic symbols used in this volume and on the ALD's are defined in the table of logic symbols. Also, included with the table is a discussion of the physical layout and interpretation of the ALD's.

1-12. DESCRIPTION.

1-13. CONSTRUCTION.

1-14. The LVDCME (figure 1-1) is comprised of two frames (frame 01 and frame 02) welded together to form a unit 58 inches long, 31 inches deep and 60 inches high that weighs approximately 1912 pounds. Frames 01 and 02 are further divided into modules. The upper module in each of these frames is designated module A; the lower module is designated module B.

1-15. Each module has removable side covers and hinged gate assemblies that provide access to parts within the module. Hinged doors provide access to power supplies and power control relays at the rear of modules 01A and 02A. Each removable side cover and hinged door (except the hinged gate assemblies and the power supply access doors) is electrically interlocked so that power is disconnected whenever a cover is removed or a door is opened. Casters at the bottom of each frame facilitate moving and installation.

1-16. ASSEMBLIES.

1-17. Figure 1-2 shows the assemblies of frames 01 and 02. Figure 1-3 lists the LVDCME assemblies in alphanumeric order by reference designation to provide additional information concerning these assemblies. In frames 01 and 02, reference designators for the assemblies are prefixed by the number of the module in which the assembly is located. For example, the power control panel is located in frame 01 module A and has a partial reference designation 1; the complete reference designation for this panel is therefore 01A1.

1-18. CONTROL PANELS. Each of the four LVDCME control panels is divided into areas that contain associated controls and indicators. The type of controls and/or indicators is designated by the legend at the top of the area. A table in Section III lists all operating controls and indicators with brief descriptions of their functions. The TAPE READER AND MODE CONTROL panel and the POWER CONTROL panel contain test jacks for monitoring critical voltages or signals.

1-19. POWER SUPPLIES. Each of the ten LVDCME power supplies has been slightly modified from the configurations shown in the maintenance manuals for these supplies. One modification is the replacement of the standard input plugs with plugs that fit the power supply receptacles in the LVDCME. Another modification is the removal of internal power supply jumpers to allow remote rather than local sensing of the power supply voltages.

1-20. Each power supply can provide an output that is current and/or voltage regulated. In the LVDCME each current regulation circuit is disabled by placing the CURRENT potentiometer in the full clockwise position.

1-21. The power supplies have external resistor networks that permit the output voltages to be varied plus or minus 1 volt. These resistor networks (consisting of a fixed resistor in series with a potentiometer) are mounted on the POWER CONTROL panel. The potentiometer may be adjusted from the front of the panel.

1-22. GATE ASSEMBLIES. Each of the gate assemblies containing SMS circuit cards and other components is hinged on one edge for ease of accessibility in checkout and maintenance. A fan assembly mounted on each gate assembly provides cooling air for the SMS circuit cards and components.

1-23. STANDARD MODULAR SYSTEM LOGIC.

1-24. SMS CARD PHYSICAL DESCRIPTION. The logic cards used in the LVDCME are called standard modular system (SMS) cards. These pluggable printed circuit cards contain all the components and printed wiring necessary for a particular electronic function. A special program cap on some SMS printed circuit cards gives additional flexibility to this form of packaging, and reduces the number of cards required for field servicing. Each card is identified by a four-character code and a six-, seven-, or nine-digit IBM part number.

1-25. The SMS single card, the kind used in the LVDCME, is made of an epoxy paper laminate material, and is approximately 1/16 inch thick, 4-1/2 inches long, and 2-1/2 inches wide. All of the electronic components and the program cap, if used, are mounted on the front side of the SMS card form. Connections to the components and program cap are made on the back side of the SMS card form by printed wiring patterns that terminate at contacts at the bottom of the card. These contacts, labeled A through R, couple the signals and voltages to the circuit components when the card is inserted into its receptacle. The printed circuit wiring (land pattern) depends on the type of circuit on the card.

1-26. The program cap on the front of some SMS cards comprises two conductor rails which, in the pre-cut state, connect to tabs on the printed circuit land pattern. By cutting the program cap, various jumpering (cap) connections are made to the tabs to allow one SMS card to be used in several circuit configurations.

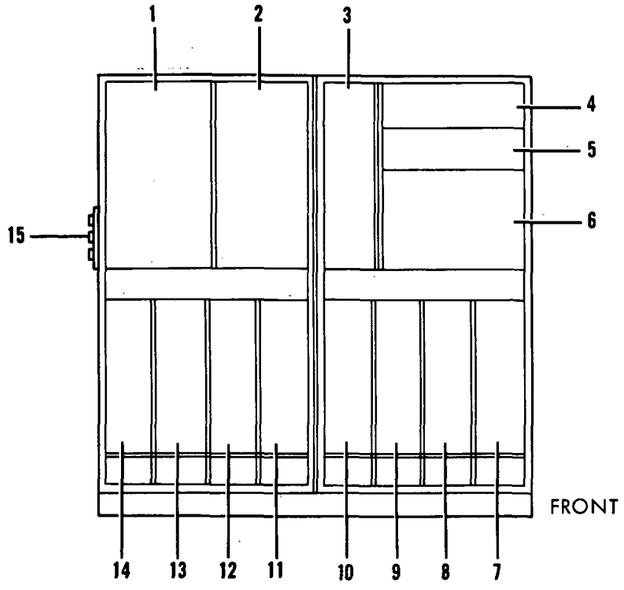
1-27. SMS RECEPTACLE PHYSICAL DESCRIPTION. The pluggable printed circuit cards are inserted into SMS card receptacles (figure 1-4). Although the contacts are all in line on the card insertion side of the receptacle, they pass through the receptacle in a staggered arrangement. This arrangement allows additional room for wire-wrapping or soldering of signal and voltage wires to the terminal pins. The SMS card receptacles used in the LVDCME are the 8-position type, serving as a common receptacle for eight individual SMS cards, and the 1-position type, accommodating one SMS card.

1-28. ELECTRICAL AND MECHANICAL CHARACTERISTICS.

1-29. Figure 1-5 lists the LVDCME electrical and mechanical characteristics.

Legend for Figure 1-2

Item	Name
1	Memory Loader and Data Display Panel Assembly (02A1)
2	Interface Exerciser Panel Assembly (02A2)
3	Power Control Panel Assembly (01A1)
4	Tape Control Panel Assembly (01A2)
5	Tape Reader Assembly (01A3)
6	Tape Spooler Assembly (01A4)
7	Gate Assembly (01B4)
8	Gate Assembly (01B3)
9	Gate Assembly (01B2)
10	Gate Assembly (01B1)
11	Gate Assembly (02B4)
12	Gate Assembly (02B3)
13	Gate Assembly (02B2)
14	Gate Assembly (02B1)
15	Connector Panel Assembly (02A3)
16	Power Sequence Relay Gate Assembly (01A9)
17	Power Supply (02A9)
18	Power Supply (02A10)
19	Computer Power Sequence Relay Gate Assembly (02A8)
20	Power Supply (02A4)
21	Power Supply (02A5)
22	Power Supply (02A6)
23	Power Supply (02A7)
24	Delay Line Gate Assembly (02B8)
25	Gate Assembly (02B7)
26	Gate Assembly (02B6)
27	Gate Assembly (02B5)
28	Module Switching Relay Gate Assembly (01B8)
29	Gate Assembly (01B7)
30	Gate Assembly (01B6)
31	AC Power Gate Assembly (01B5)
32	Power Supply (01A7)
33	Power Supply (01A8)
34	Power Supply (01A6)
35	Power Supply (01A5)



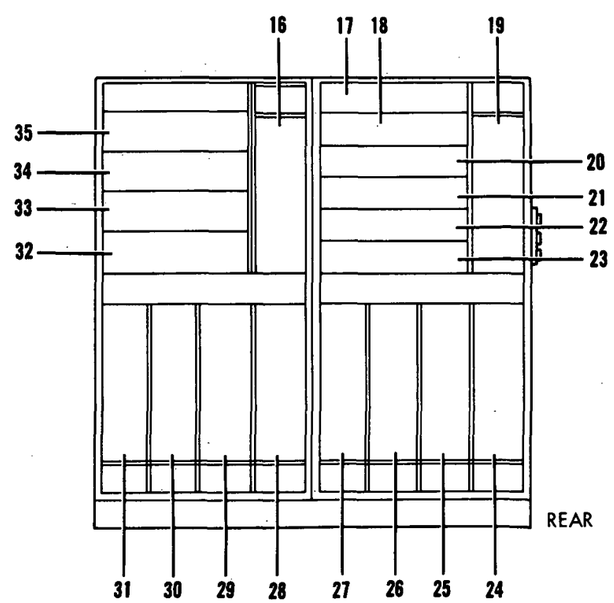


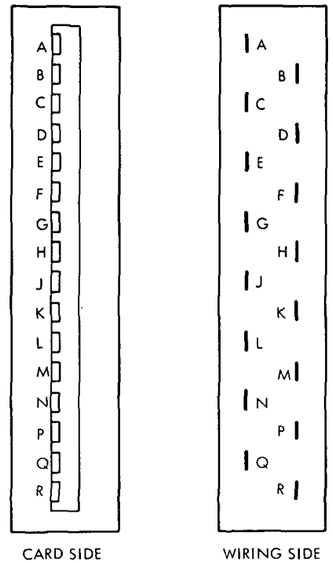
Figure 1-2. Frame 01 and 02 Assemblies

Reference Designation	Index Number Figure 1-2	Name	Part Number or Manufacturers Designation	Manufacturer	Description
01A1	3	Power Control Panel Assembly	6901200	IBM Corporation	Hinged on bottom. Contains power controls and adjustments and voltage monitoring test points for the LVDCME and computer under test.
01A2	4	Tape Control Panel Assembly	6901100	IBM Corporation	Hinged on left side. Contains controls and test points for the tape reader and tape spooler.
01A3	5	Tape Reader Assembly	Model RR-1002B-333 (6901110)	Rheem Electronic Corporation	Mounted on slide mounted rack with assembly 01A4. See maintenance instructions for this item. (Refer to list of related manuals.)
01A4	6	Tape Spooler Assembly	Model RS-500A (6901120)	Rheem Electronic Corporation	Mounted on slide mounted rack with assembly 01A3. See maintenance instructions for this item. (Refer to list of related manuals.)
01A5	35	Power Supply	Model M15-50A-0V (6901013)	Trygon Electronics Incorporated	Provides -12 VDC for LVDCME logic circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
01A6	34	Power Supply	Model M15-15A-0V (6901010)	Trygon Electronics Incorporated	Provides -6 VDC for LVDCME logic circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
01A7	32	Power Supply	Model M36-10A-0V (6901012)	Trygon Electronics Incorporated	Provides -26.5 VDC for LVDCME power sequencing relays. See maintenance instructions for this item. (Refer to list of related manuals.)
01A8	33	Power Supply	Model M15-10-0V (6901011)	Trygon Electronics Incorporated	Provides +12 VDC for LVDCME logic circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
01A9	16	Power Sequence Relay Gate Assembly	6901500	IBM Corporation	Hinged on bottom. Contains voltage sequencing relays used during power-up and power-down operations.
01B1	10	Gate Assembly	6901300	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
01B2	9	Gate Assembly	6901400	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
01B3	8	Gate Assembly	6901430	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
01B4	7	Gate Assembly	6901230	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
01B5	31	AC Power Gate Assembly	6901600	IBM Corporation	Accessible through side panel. Contains AC power control circuits for power supplies and fans.
01B6	30	Gate Assembly	6901630	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
01B7	29	Gate Assembly	6901530	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
01B8	28	Module Switching Relay Gate Assembly	6901220	IBM Corporation	Hinged on top. Contains LVDCME relays used during computer module switching.

Figure 1-3. LVDCME Assemblies (Sheet 1 of 2)

Reference Designation	Index Number Figure 1-2	Name	Part Number or Manufacturers Designation	Manufacturer	Description
02A1	1	Memory Loader and Data Display Panel Assembly	6902100	IBM Corporation	Hinged on left side. Contains controls and indicators needed during memory loading and verification.
02A2	2	Interface Exerciser Panel Assembly	6902150	IBM Corporation	Hinged on right side. Contains error indicators and controls and indicators needed to exercise the computer with the diagnostic program.
02A3	15	Connector Panel Assembly	6902330	IBM Corporation	Contains LVDCME - computer and self check interface connectors.
02A4	20	Power Supply	Model M36-5-0V (6902042)	Trygon Electronics Incorporated	Provides +20 VDC for computer memory circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
02A5	21	Power Supply	Model M15-5-0V (6902041)	Trygon Electronics Incorporated	Provides +12 VDC for computer logic circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
02A6	22	Power Supply	Model M15-30A-0V (6902044)	Trygon Electronics Incorporated	Provides +6 VDC for computer logic circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
02A7	23	Power Supply	Model M15-15A-0V (6902045)	Trygon Electronics Incorporated	Provides -3 VDC for computer logic circuits. See maintenance instructions for this item. (Refer to list of related manuals.)
02A8	19	Computer Power Sequence Relay Gate Assembly	6902230	IBM Corporation	Contains relays that control sequencing of voltages applied to the computer during power-up and power-down operations.
02A9	17	Power Supply	Model M15-10-0V (6902040)	Trygon Electronics Incorporated	Provides +6 volts to computer for module switching. See maintenance instructions for this item. (Refer to list of related manuals.)
02A10	18	Power Supply	Model M15-5-0V (6902041)	Trygon Electronics Incorporated	Provides +12 VDC to computer for module switching. See maintenance instructions for this item. (Refer to list of related manuals.)
02B1	14	Gate Assembly	6902200	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B2	13	Gate Assembly	6902300	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B3	12	Gate Assembly	6902400	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B4	11	Gate Assembly	6902500	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B5	27	Gate Assembly	6902600	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B6	26	Gate Assembly	6902700	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B7	25	Gate Assembly	6902800	IBM Corporation	Hinged on top. Contains LVDCME logic circuits.
02B8	24	Delay Line Gate Assembly	6902900	IBM Corporation	Hinged on top. Contains LVDCME delay lines.

Figure 1-3. LVDCME Assemblies (Sheet 2)



NOTE:

ALL OF THE PIN LETTERS DO NOT APPEAR ON THE RECEPTACLES. THEY ARE SHOWN HERE FOR REFERENCE PURPOSES.

Figure 1-4. Typical SMS Card Receptacle

Input Power	Phase: 3 phase; 5 wire; wye connected; phase sequence is ABC Frequency: 60 ±5 cycles/sec Voltage: 115 ±11.5 VAC (line to neutral) Current: 20 (MIN) to 30 (MAX) amperes/phase
Environment	Ambient Temperature: +60 DEG F to +95 DEG F Relative Humidity: 10% to 80%
Mechanical Packaging	Basic Packaging: IBM SMS family. Cabinet: Two frames mechanically and electrically bonded together Size: Heighth - 60 inches Length - 58 inches Depth - 31 inches Weight: 1912 pounds Logic Chassis Design: Hinged on one edge for ease of accessibility; a blower is mounted on each chassis for cooling of SMS circuit cards and components. Printed Circuit Cards: The basic logic subassembly is SMS cards.

Figure 1-5. Electrical and Mechanical Characteristics

SECTION II

THEORY OF OPERATION

2-1. GENERAL.

2-2. This section contains a functional description of the LVDCME circuits. The functional descriptions contained in this section are as follows:

1. POWER DISTRIBUTION
   - a. AC POWER DISTRIBUTION
   - b. INTERNAL LVDCME POWER DISTRIBUTION
   - c. DC POWER DISTRIBUTION TO COMPUTER INTERFACE
2. LVDCME SUBSIDIARY CIRCUITS
   - a. LVDCME TIMING
   - b. TRANSLATION CIRCUITS
   - c. VOTERS
   - d. DISAGREEMENT ERROR DETECTORS
   - e. EXCLUSIVE OR COMPARATORS
   - f. BINARY COUNTERS
   - g. PARITY DETECTORS
   - h. ERROR TEST AND ERROR RESET CIRCUITS
   - i. INDICATOR LAMP CIRCUITS
3. CHANNEL-MODULE-SWITCHING
4. MEMORY LOADER/DATA DISPLAY
5. INTERFACE EXERCISER
6. SELF CHECK
7. COMPUTER CONTROL

2-3. In describing the functions listed, simplified diagrams and timing charts are presented to familiarize the reader with the equipment. Detailed drawings are provided in Section X; reference to these drawings is made as necessary.

2-4. Negative logic is used throughout the LVDCME. A "1" is represented by a negative voltage level (-6 VDC or -12 VDC) and a "0" is represented by ground potential. An input to an "AND" or an inverter circuit that is floating, is interpreted as a "1". A "0" output prevails when "OR", "AND" or inverter circuit outputs are "ORed" together.

2-5. POWER DISTRIBUTION.

2-6. AC POWER DISTRIBUTION. (See figure 10-4.)

2-7. Primary power (3-phase, 60 cycle AC) is applied to connector 01B11J01. Each phase is applied through circuit breaker 01B5CB4 to movable contacts of relay 01B5K3. Phase A is also connected to the primary of transformer 01B5T1 whose secondary applies 24 volts to receptacle 02A3J23. This voltage is returned externally to the E. O. PWR CONT point (upper left hand corner of drawing) and routed through interlocks, normally closed contacts of POWER OFF switch 01A1S6 and normally closed contacts of relay 01B5K3 to POWER OFF lamps 01A1DS6. This action causes the POWER OFF lamp to light.

2-8. When POWER ON switch 01A1S7 is pressed, relay 01B5K3 picks and holds through its own contacts. The following occurs:

1. POWER OFF lamps 01A1DS6 go out.

2. POWER ON lamps 01A1DS7 light.

3. Primary power is routed through normally open contacts of relay 01B5K3 to fan motors, DC power supplies, and ϕA, ϕB, ϕC, and FAN lamps 01A1DS5.

NOTE

Phases are distributed as follows:

Phase A	-12 V power supply (computer exerciser)
	+12 V power supply (module switching)
	ϕA lamp 01A1DS5
Phase B	All fan motors
	+6 V power supply (module switching)
	+20 V power supply (computer)

NOTE (cont)

+12 V power supply (computer)

+6 V power supply (computer)

-3 V power supply (computer)

ϕB and FAN lamps 01A1DS5

Phase C +12 V power supply (computer exerciser)

-26.5 V power supply (computer exerciser)

-6 V power supply (computer exerciser)

Tape reader

ϕC lamp 01A1DS5

2-9. When POWER OFF switch 01A1S6 is pressed, 24 volts, from the interlocks, is disconnected from the remainder of the circuit, and relay 01B5K3 drops, removing primary power from fans and all AC receptacles. The following occurs:

1. POWER ON lamp 01A1DS7 goes out.

2. ϕA, ϕB, ϕC, and FAN lamps 01A1DS5 lamps go out.

3. POWER OFF lamp 01A1DS6 lights (when POWER OFF switch 01A1S6 is released).

2-10. INTERNAL LVDCME DC POWER DISTRIBUTION. (See figures 10-5 and 10-6.)

2-11. Power distribution paths within the LVDCME are controlled by relays and switches, and the paths vary when the relay and switch contacts are transferred. The subsequent description covers the initial conditions and voltage sequencing during LVDCME power-on and power-off operations.

NOTE

Prefix all abbreviated reference designations with 01A9.

2-12. Initially all relays are de-energized and -26.5 volts is available at contact C of ACME POWER-SEQ ON switch 01A1S4. ACME POWER-SEQ OFF lamps 01A1DS3 are lit, and ACME POWER-SEQ ON lamps 01A1DS4 are not lit. When ACME POWER-SEQ ON switch 01A1S4 is pressed, relay K11 picks, and power supply voltages pick the following relays through normally open contacts of relay K11 (figure 10-6):

Power Supply	K11 Contact	Relay Picked
-12 V	D	K8
+12 V	B	K9
-6 V	C	K16

2-13. Relays K2, K3 and K10 pick through normally open contacts of K9, and relay K13 picks through normally open contacts of relay K10 removing energizing voltage from ACME POWER-SEQ OFF lamps 01A1DS3. All relays picked thus far hold through the interlocks formed by normally open contacts of relays K13, K8, K16, K9 and K10. The ACME POWER-SEQ ON switch 01A1S4 may now be released without affecting the power-on sequencing.

2-14. When relay K13 picks energizing voltage is applied through its normally open contacts to one-second time-delay relay K17. After one second, relay K17 picks and applies a ground to the coil of relay K1. Relay K1 picks and holds through its own contacts and disconnects the ground return for relay K17 causing K17 to drop. Energizing voltage is applied through normally open contacts of relay K1, and normally closed contacts of relays K17 and K14 to relay K12 and ACME POWER-SEQ ON lamps 01A1DS4. When relay K12 picks, a ground level (OPER) is applied to LVDCME logic circuits and the power-on sequence is complete.

2-15. When ACME POWER-SEQ OFF switch 01A1S3 is pressed, the power-off sequence begins. Energizing voltage is applied to relay K14 and one-second time-delay relay K14 through normally closed contacts of relay 02A8K13. Relay K14 picks, holds through its own contacts and provides energizing voltage to relay K4 when switch 01A1S3 is released. When relay K14 picks, relay K12 drops and removes OPER from LVDCME logic circuits. After one second, relay K4 picks and de-energizes relay K11. When relay K11 drops, all relays except K4 drop. (ACME POWER-SEQ ON lamp 01A1DS4 goes out when relay K1 drops; ACME POWER-SEQ OFF lamp 01A1DS3 lights when relay K13 drops.) When the heating element in relay K4 cools, K4 contacts open and the power-off sequence is complete.

2-16. *DC POWER DISTRIBUTION TO THE COMPUTER INTERFACE.* (*See figures* 10-5, 10-7 and 10-8.)

2-17. The subsequent description covers the initial conditions and voltage sequencing of the DC power distribution during computer power-on and power-off operations.

NOTE

Prefix all abbreviated reference designations with 02A8.

2-18. Initially all relays in gate 02A8 are de-energized with the exception of relay K40 which is picked by -26.5 V from the Launch Vehicle Data Adapter Manual Exerciser (LVDAME) or Temperature Modulator interlock. The COMP POWER-SEQ OFF lamps 01A1DS1 are lit, and COMP POWER-SEQ ON lamps 01A1DS2 are not lit. When COMP POWER-SEQ ON switch 01A1S2 is pressed, -26.5 V is applies through normally open relay K40 contacts to relay K36. Relay K36 picks and allows power supply voltages to pick interlock relays K29, K26, K28, K15, K31 and K30 (figures 10-7 and 10-8). Power relays K23, K33 and K39 pick through the interlock formed by the normally open contacts of the interlock relays. Voltages are fed through contacts to the computer interface as follows:

Voltage	Relay	Contacts
+6 V	K33	B and C
+12 V	K33	D
+20 V	K23	A
-3 V	K33	A
+12 V (MS)	K39	A and B
+6 V (MS)	K39	C and D

2-19. The memory interlock relays (K27, K12, K18 and K32) are picked by the power supply voltages. These relays prevent further power sequencing unless each DC power supply voltage (+6, +12, +20 and -3 volts) appears at the interface.

2-20. Relay K13 picks through normally open contacts K32-B and holds through its own contacts. Contacts K13-A by-pass switch 01A1S2 so that all relays energized thus far will remain energized when switch 01A1S2 is released. Contacts K13-B remove the ground return for COMP POWER-SEQ OFF lamps 01A1DS1.

2-21. Interlock relay K37 picks through the interlock formed by relay contacts K32-A, K12-A, K18-A and K27-A. Normally open relay K37 contacts switch power supply sense lines for remote sensing. Interlock relays K35 and K38 pick through normally closed contacts of relay K11 and normally open contacts of relay K37. As normally closed relay K35 contacts open, local sensing lines are disconnected from the power supplies. When relay K37 picks, energizing voltage is applied (through normally closed relay K6 contacts) to one-second time-delay relay K1 and two-second time-delay relay K2. The normally open relay K1 contacts close after 1/5 second and provide a ground return for relay K7 which picks and holds through its own contacts. +20 V is applied to the computer memory through normally closed relay K1 contacts and current limiting resistors R1 and R2. When relay K7 picks, energizing voltage is removed from relay K1 which drops in approximately 4/5 second. Relays K2 and K8 control each other in the same manner that relays K1 and K7 controlled each other except that the total time delay of K2 is two seconds. When relay K2 drops energizing voltage is applied (through normally closed relay K2 contacts and normally open relay K8 contacts) to the coils of relays K14 and K24. Normally open K14-C contacts and normally closed relay K9 contacts shunt current limiting resistors R1 and R2 and allow +20 V to be applied directly to the computer memory. Normally open relay K24-A contacts provide the remote sensing path for the +20 V power supply.

2-22. Relay K19 picks through normally open relay K14 contacts and normally closed relay K17 contacts, and relay K22 picks through contacts of relays K19 and K16. The opening of normally closed K19 contacts disconnect the local sense line for the +20 V power supply. When relay K22 picks, the PWR HLT (power halt) ground level is removed from computer logic circuits, and energizing voltage is applied to COMP POWER-SEQ ON lamps 01A1DS2. This completes the power-on sequence.

2-23. When COMP POWER-SEQ OFF switch 01A1S1 is pressed, the power-off sequence starts. Energizing voltage is applied to relay K16 which picks and holds through its own contacts. When relay K16 picks, contacts K16-B remove energizing voltage from relay K22. The COMP POWER-SEQ ON lamps 01A1DS2 go out, and the PWR HLT ground level is applied to the computer logic circuits. When switch 01A1S1 is pressed, voltage is also applied to one-second time delay relay K20. After one second, relay K20 picks and applies energizing voltage to relay K17, one-second time-delay relay K6 and five-second time-delay relay K5. When relay K17 picks, relay K19 drops and restores local sensing to the +20 V power supply. Open relay contacts K17-A also cause relay K9 to drop.

2-24. When relay K6 picks (after one-second delay), the following relays drop due to the opening of contacts K6-A: K7, K8, K14 and K24. One second after relay K6 picks, relay K5 picks and provides a ground return for relay K11. Relay K11 picks and holds through its own contacts and removes the ground return from relay K5 which drops in approximately four seconds. When relay K11 picks, the energizing voltage for relays K35 and K38 is removed, and the two relays drop. When relays K35 and K38 drop, local sensing is restored to power supplies +12 MS, +6 MS, -3 V, +6 COMP and +12 COMP.

2-25. When relay K14 drops, energizing voltage is applied (through normally closed contacts K14-B) to five-second time-delay relay K4 and two-second time-delay relay K21. After 2/5 second, relay K21 picks; after one second K4 picks. Normally open contacts of relay K21 provide a discharge path for computer memory capacitors. Relay K4 provides a ground return for relay K10 which picks and holds through its own contacts. Relay K10 removes the energizing voltage from relay K4 whose normally open contacts remove the energizing voltage from relay K13. Normally closed contacts K13-A remove the energizing voltage from relays K36 and K16 which, in turn, drop all energized relays except K40.

2-26. Computer power is also sequenced off if ACME POWER-SEQ OFF switch 01A1S3 is pressed. Contacts K13-D (normally open) provide the alternate means of starting the computer power-off sequence.

2-27. LVDCME SUBSIDIARY CIRCUITS.

2-28. Subsidiary circuits are those which are related to more than one LVDCME function. These circuits are necessary to the operation of the LVDCME and are categorized as such only to prevent repetitious explanations.

2-29. LVDCME TIMING.

2-30. The timing circuits provide LVDCME logic with negative timing gates synchronized with the positive computer timing gates. The clock generator receives the voted computer W clock and generates four clocks (NCPW, NCPX, NCPY, and NCPZ). The bit gate generator uses NCPW to generate 14 bit gates (NBG1 through NBG14). Similarly, the phase generator uses NBG1 to generate three phase gates (NPHA, NPHB, and NPHC). Figure 2-1 shows the timing relation between the various timing gates. The sync control circuit maintains synchronization between the outputs of the bit gate and phase

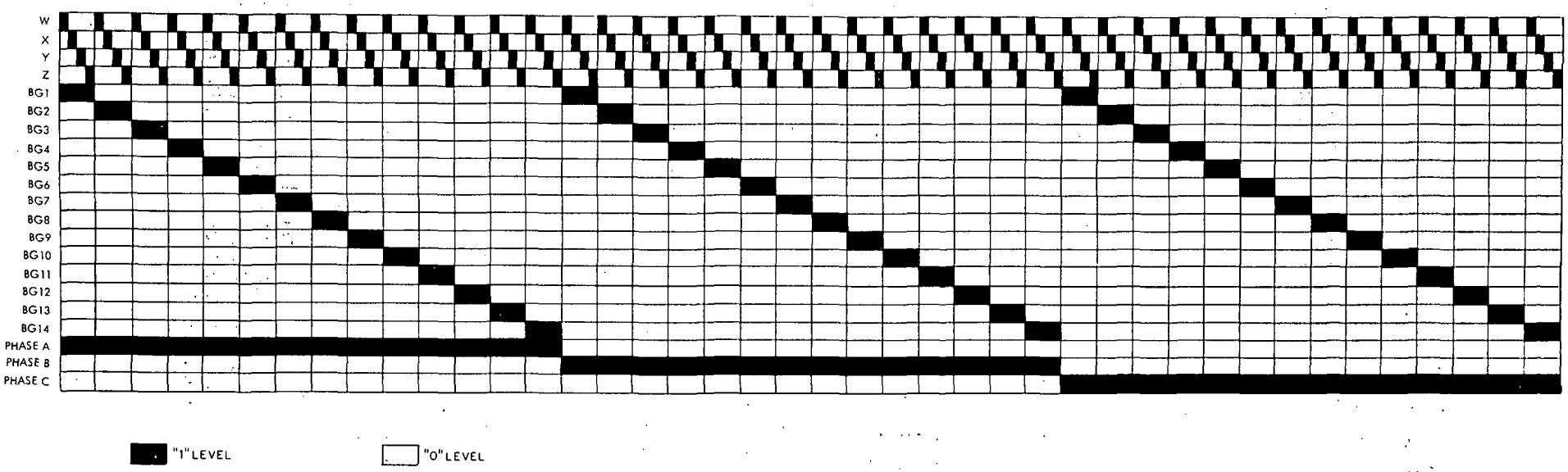


Figure 2-1. LVDCME Timing Gates

generators in the LVDCME and computer. The sync error detectors monitor synchronization between LVDCME and computer phase B and ACME and computer gate 5 and lights a lamp is synchronization is lost.

2-31. CLOCK GENERATOR. The clock generator is shown in simplified form on figure 2-2. The voted W clock (PTGY) is delayed a total of two clock times by DLY 1 and DLY 2. The delayed W clock triggers SS 1 which produces the Y clock pulse (NCPY).

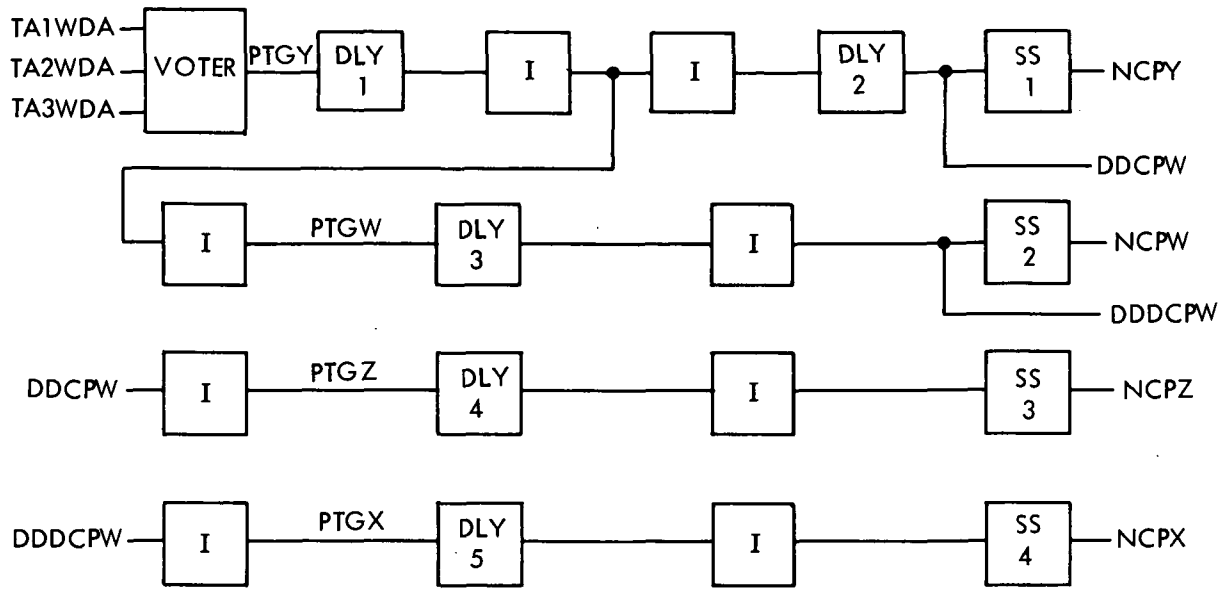


Figure 2-2. Clock Generator

2-32. After being delayed by DLY 1, PTGY is again delayed by DLY 3. (The total delay of DLY 1 and DLY 3 is four clock times.) Single-shot SS 2 is triggered and NCPW is generated. Note that NCPW is generated by the preceding computer W clock.

2-33. The pulse that triggered SS 1 (DDCPW) is inverted and delayed one clock time by DLY 4 to produce NCPZ. Similarly the pulse that triggered SS 2 (DDDCPW) is inverted and delayed one clock time by DLY 5 to produce NCPX.

2-34. BIT GENERATOR. The bit generator consists of a shift register control circuit, a seven-bit shift register, and a bit decoding circuit. The shift register control circuit prevents the contents of the shift register from rippling through when it is stepped.

2-35. Figure 2-3 is a diagram of the shift register control circuit which is comprised of a pair of latches interconnected to form a binary counter. Latch L2 stores the configuration of latch L1 during a Y clock. The outputs of latch L2 are applied to -IO's which subsequently complement latch L1 during the following W clock. Outputs W AND A and W AND A NOT occur during alternate W clocks.

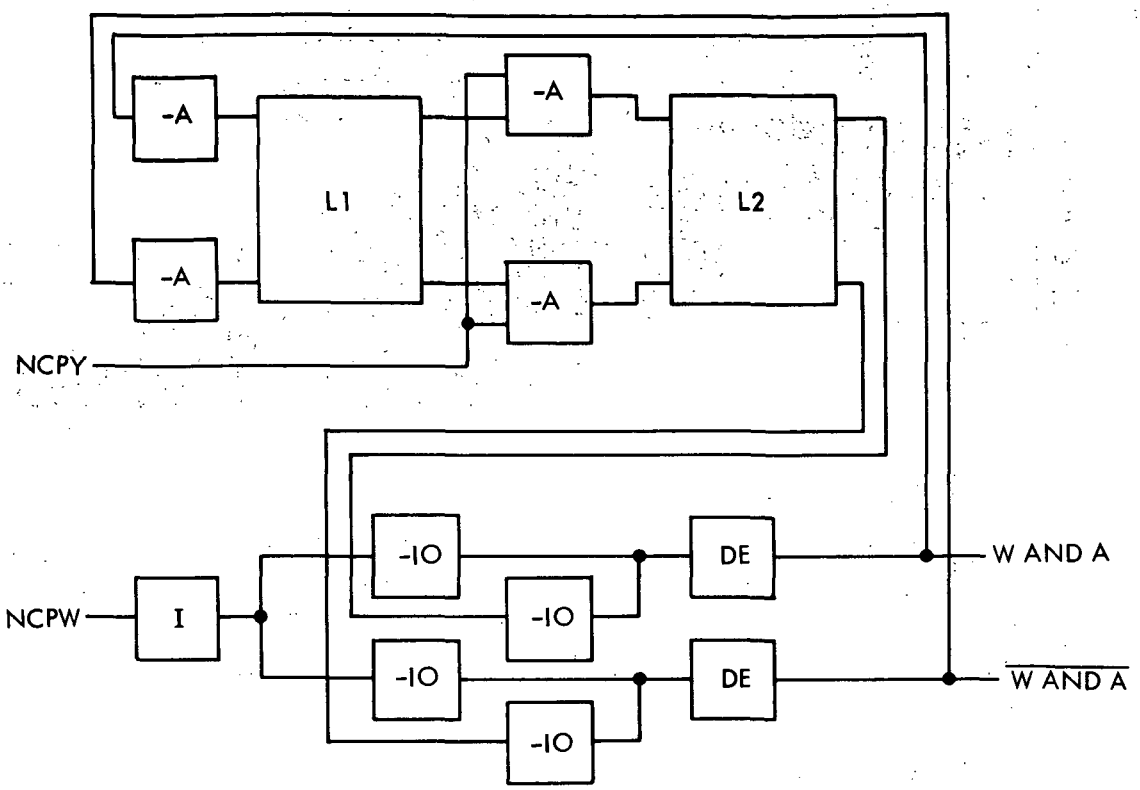


Figure 2-3. Bit-Gate Shift Register Control Circuit

2-36. The bit generator shift register is a latch register that changes configuration every bit time under control of W AND A and W AND A NOT. Seven outputs (G1 through G7) change states as shown on figure 2-4. The bit decoder is a matrix that generates 14 bit gates that correspond to the times that two successive shift register outputs are in opposite states. For instance, NBG1 is generated when G2 = 1 and G1 = 0.

2-37. PHASE GENERATOR. The phase generator (figure 2-5) consists of two tratches that are interconnected so that outputs NPHA, NPHB, and NPHC occur at the same times (respectively) that computer phases PA, PB, and PC occur. The outputs of tratch 1 are changed during Y time of BG14; the outputs of tratch 2 are changed during W time of BG1.

2-38. SYNC CONTROL. The sync control consists of a single-shot that generates a pulse at the beginning of each computer phase B (NPB). This pulse is sent to the bit gate generator where it sets the control circuit and shift register to states that correspond to BG1. The sync pulse is also sent to the phase generator where it sets NPHB to a "1". The sync control therefore maintains synchronization between the computer and LVDCME timing gates once every three phases.

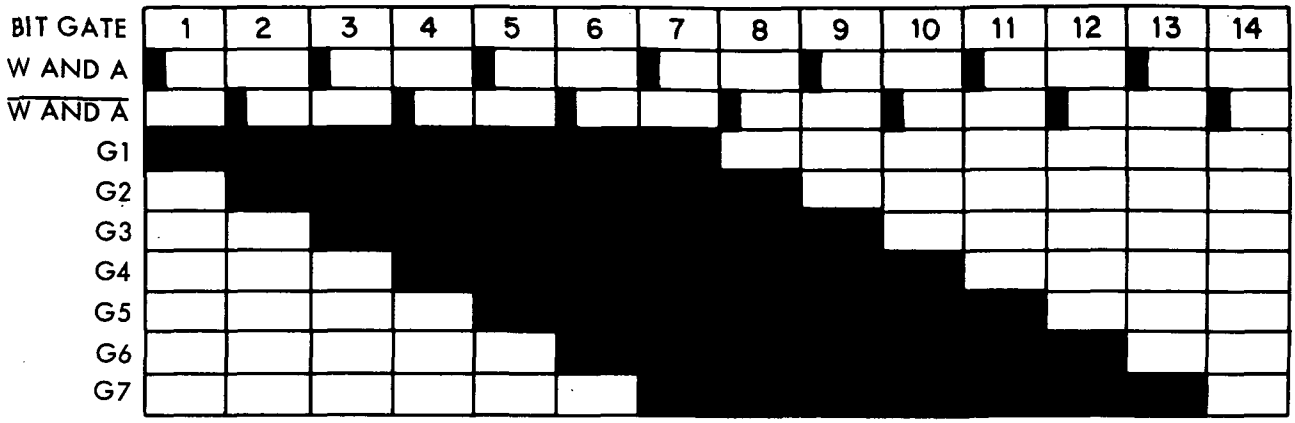


Figure 2-4. Bit-Gate Shift Register Outputs

2-39. PHASE SYNC AND BIT-GATE SYNC ERROR DETECTORS. The phase sync error detector is a single stage comparator that compares NPHB with NPB at Z clock time. Errors are stored in a latch that causes the sync error indicator (SYNC) to light. The bit-gate sync error detector is another single stage comparator that compares G5 and NG5 at Z clock time. Errors are stored in a latch that also causes the sync error indicator to light.

2-40. TRANSLATION CIRCUITS.

2-41. Most computer signals that appear at the computer-LVDCME interface must be translated from positive logic levels to negative logic levels. This is accomplished by translation circuits which change +6 V signals to -6 V signals and leave 0 V signals unchanged. Conversely, LVDCME signals that go to the computer must be translated into positive logic levels for use in the computer. Generally, LVDCME signals are named the same as their computer counterparts except that they are prefixed with T or N to indicate their translated or negative logic nature.

2-42. VOTERS.

2-43. All triple modular redundant (TMR) inputs to the LVDCME go to voters. Each voter provides a single output that corresponds to the majority of inputs to the voter. Figure 2-6 is a simplified diagram of a typical voter in which inputs A1, A2, and A3 are used to generate a single output (NA). If two or more inputs are "1's", NA is a "1"; if two or more inputs are "0's", NA is a "0".

2-44. DISAGREEMENT ERROR DETECTORS.

2-45. All TMR inputs to the LVDCME go to disagreement error detectors. These error detectors continuously sense for disagreement between corresponding signals from the three computer channels. If a disagreement exists, an error signal is generated which subsequently lights a lamp that indicates which signal and channel is at fault.

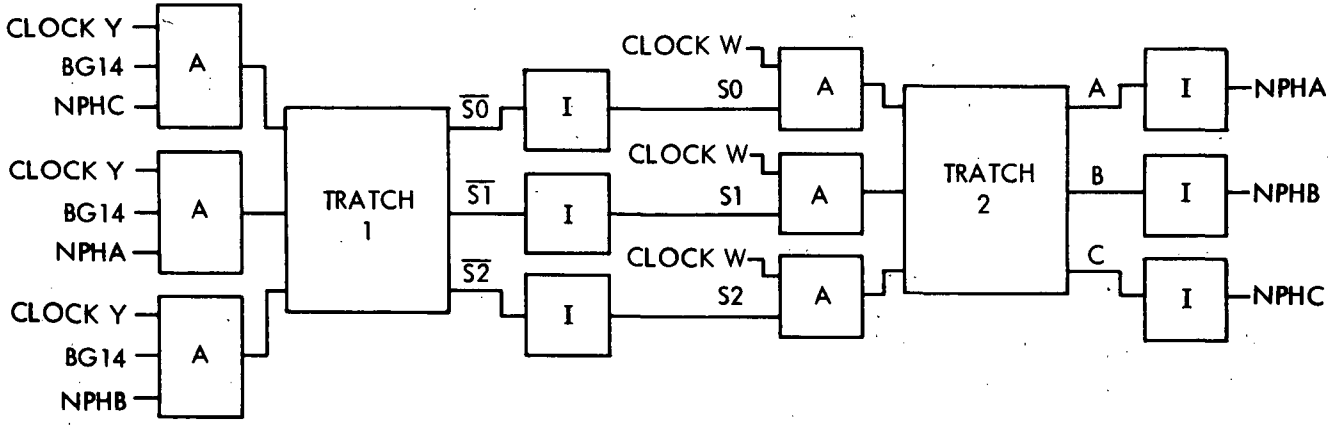


Figure 2-5. Phase Generator

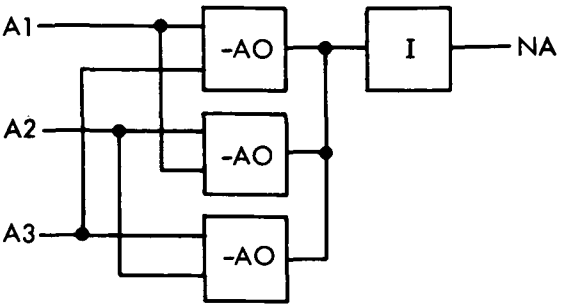


Figure 2-6. Typical LVDCME Voter

2-46. The disagreement error detector works on the principle that if one signal in a TMR trio differs from the other two, it must match the inverses of the other two. Figure 2-7 is a simplified diagram of a typical disagreement error detector in which inputs A1, A2, and A3 (and their inverses) are compared. Each signal is compared (in a -AO) with the inverses of the remaining signals, and the inverse of each signal is compared with the remaining signals. If agreement between A1, A2, and A3 does not exist, a "1" will appear at the disagreement error output that corresponds to the faulty signal.

2-47. EXCLUSIVE OR COMPARATORS.

2-48. The LVDCME contains many exclusive OR comparators that compare corresponding data from two sources. Figure 2-8 shows a typical exclusive OR comparator in which three parallel inputs (X1, X2, and X3) are compared with three other parallel inputs (Y1, Y2, and Y3).

2-49. If a compare exists, the input to each A0 will be unlike, and the output of each A0 will be a "1". This will result in a "1" on the COMPARE line and a "0" on the COMPARE NOT line. If a compare does not exist, at least one of the A0's will have two "1" inputs. This will result in a "0" on the COMPARE line and a "1" on the COMPARE NOT line.

2-50. Two additional A0's are required to compare each additional pair of inputs. A single stage comparator is used to compare serial data from two sources.

2-51. BINARY COUNTERS.

2-52. The LVDCME contains many binary counters which are alternately set or cleared every time the signal they are monitoring changes from a "0" to a "1". Figure 2-9 shows a typical binary counter which is monitoring signal B and controlled by signal A.

2-53. The control latch stores the configuration of the output latch providing A is a "1". The output latch is then alternately set or reset every time B goes from a "0" to a "1". When A is a "0" the configuration of the output latch cannot be changed. The binary counter can be initially set or cleared by routing a signal through an inverter to the output latch set or reset input.

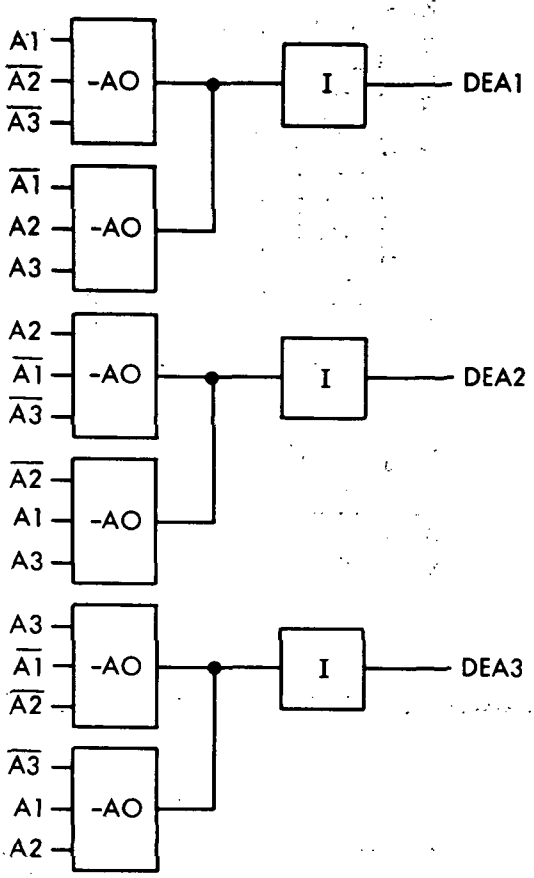


Figure 2-7. Typical LVDCME Disagreement Error Detector

2-54. PARITY DETECTORS.

2-55. The LVDCME contains several parity detectors that are used for parity bit generation and parity error detection. These parity detectors detect the number of "1's" contained in the information feeding them (see figure 2-10).

2-56. When either, none, or 2, or four of the inputs A, B, C, and D are "1's" the outputs of OR circuits 1 and 2 are the same value. Therefore one of the inputs to OR circuit 3 is a "1" and the EVEN and ODD outputs are respectively a "1" and "0". When an odd number of the inputs are "1's" the outputs of OR circuits 1 and 2 are unlike values. Thus the inputs to OR circuit 3 are "0's" and the EVEN and ODD outputs are a "0" and "1" respectively.

2-57. ERROR TEST AND ERROR RESET CIRCUITS.

2-58. The error test and error reset circuits generate four signals (ERR TEST and ERR RST and their inverses). The error latches are all set when ERR TEST is a "1" and are all reset when ERR RST is a "1".

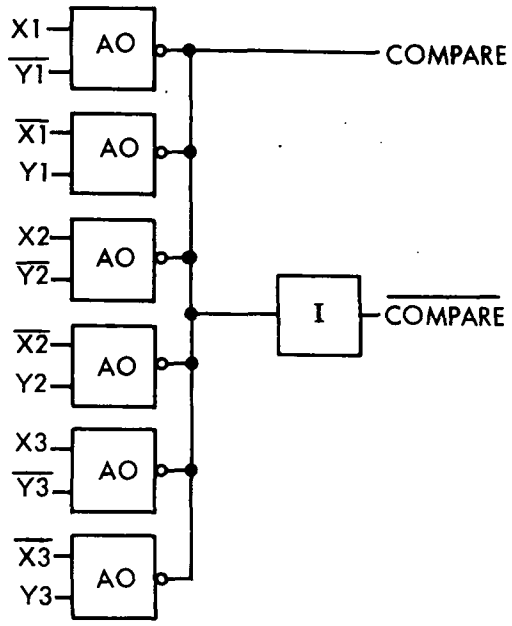


Figure 2-8. Typical Exclusive OR Comparator Circuit

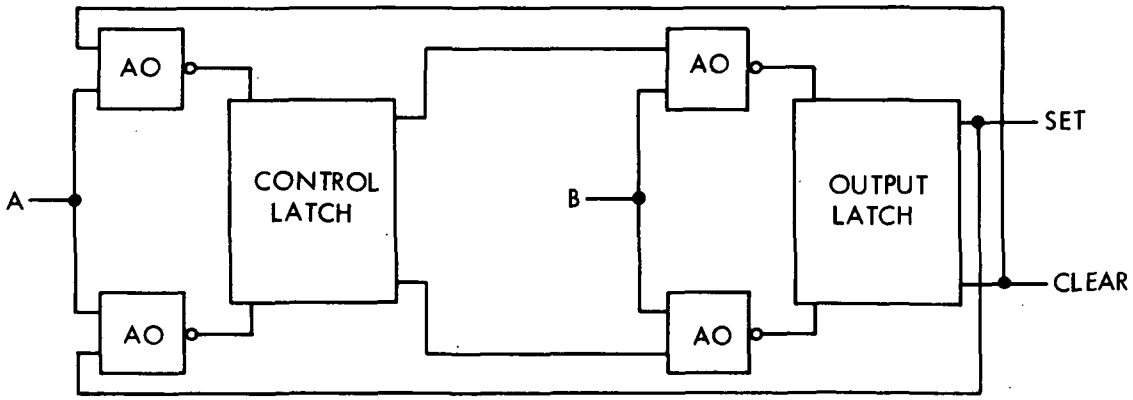


Figure 2-9. Typical Binary Counter

2-59. ERR TEST and ERR TEST NOT are the outputs of a latch which is set when the ERROR DEVICES TEST pushbutton is pressed and the tape reader is stopped. ERR RST and ERR RST NOT are forced to a "1" and a "0" respectively as follows:

1. When the ERROR RESET pushbutton is pressed and the tape reader is stopped.

2. At tape reader clock pulse 2 time in the invert error mode by a tape address of 00110.

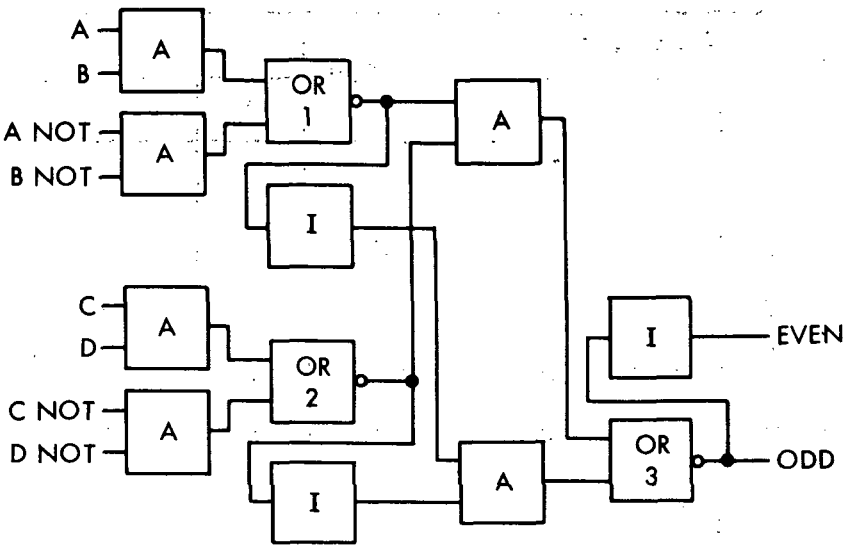


Figure 2-10. Typical Parity Detector

2-60. INDICATOR LAMP CIRCUITS.

2-61. The LVDCME contains many indicator lamps that are associated with either switches or latches. These lamps are all commonly connected to -12 VDC on one side. A lamp associated with a switch is lighted by providing a return path to ground for -12 VDC through the lamp and the normally open or normally closed contacts of the switch.

2-62. A lamp associated with a latch is connected in the collector circuit of an indicator driver. The lamp is lighted by a "1" input into the indicator driver which is fed by the set or reset of a latch.

2-63. The lamps on the MEMORY LOAD AND DATA DISPLAY, TAPE READER AND MODE CONTROL, and INTERFACE EXERCISER panels are lighted when the LAMP TEST pushbuttons on these panels are in the LAMP TEST position. This applies ground to the lamps or to the base of the transistor in the indicator driver.

2-64. CHANNEL-MODULE SWITCHING.

2-65. The channel and module switching feature of the LVDCME is used to force the seven computer modules to operate on only one of their three TMR channels. To select a channel, the LVDCME disables the remaining channels by setting one voter input to "0" and the other voter input to "1". (Refer to manual portion of figure 2-11.)

2-66. Figure 2-12 shows a typical computer voter group and its input circuits. Normally, inputs A1, A2, and A3 and outputs CH1, CH2, and CH3 are alike (all zeroes or all ones); points A, B, and C are connected to +6 MS and points D, E, and F are connected to +12 MS. To select channel 1, input A2 and A3 must be set to "1", input E must be set to "0" and input F must be set to "1". Inputs E and F could be reversed. Outputs CH1, CH2, and CH3 will now correspond to input A1.

MANUAL			CIO CODE	AUTO		
CHANNEL				CHANNEL		
1	2	3		1	2	3
x	0	1	056	x	0	1
x	1	0	062	x	1	0
0	x	1	066	0	x	1
1	x	0	072	1	x	0
0	1	x	076	1	0	x
1	0	x	102	0	1	x
x	x	x (TMR)	022	x	x	x (TMR)
Note: x - denotes selected channel.						

Figure 2-11. Channel Switching Selections

2-67. A voter input may be set to "1" by grounding the corresponding latch-back supply point (A, B, or C). A voter input may be set to "0" by grounding the +12 MS supply point (D, E, or F). The two methods of selecting each channel are listed in figure 2-13. (See figure 2-12.)

2-68. The computer may be operated in any one of the following modes: (1) single channel (channel switching), (2) all channel, or (3) mixed channel (module switching). In single channel operation, the same channel is selected in each of the seven modules; in all channel operation (normal mode when channel-module switching is not used) all channels are selected; in mixed channel operation, any channel in each of the seven modules may be selected.

2-69. The LVDCME circuit that controls channel and module switching is shown in simplified form on figure 2-14. The mode of operation (channel or module switching) is selected by alternate action switch CHANNEL/MODULE (02A2S36).

2-70. CHANNEL SWITCHING. In the manual mode when HALT is activated, and when the CHANNEL/MODULE switch is in the CHANNEL position, the switch contacts allow the three channel selection switches to control computer channel selection. The switch contacts also allow picking of relay 01B8K02 which controls the CHANNEL/MODULE lamp, and puts module selection lamps in a known state (MODULE 1 through 7, CHANNEL 1 $\left(\begin{matrix}\text{CH2=1}\\\text{CH3=0}\end{matrix}\right)$ lamps light.) The logic connected to the channel selection switches maintain channel selection after the switches are released, and provide for the alternate method of selecting each channel (refer to paragraph 2-66). The logic also includes the relay drivers for energizing the 35 channel-module selection relays. The relays that are energized when the channel selection switches are pressed are listed in figure 2-15.

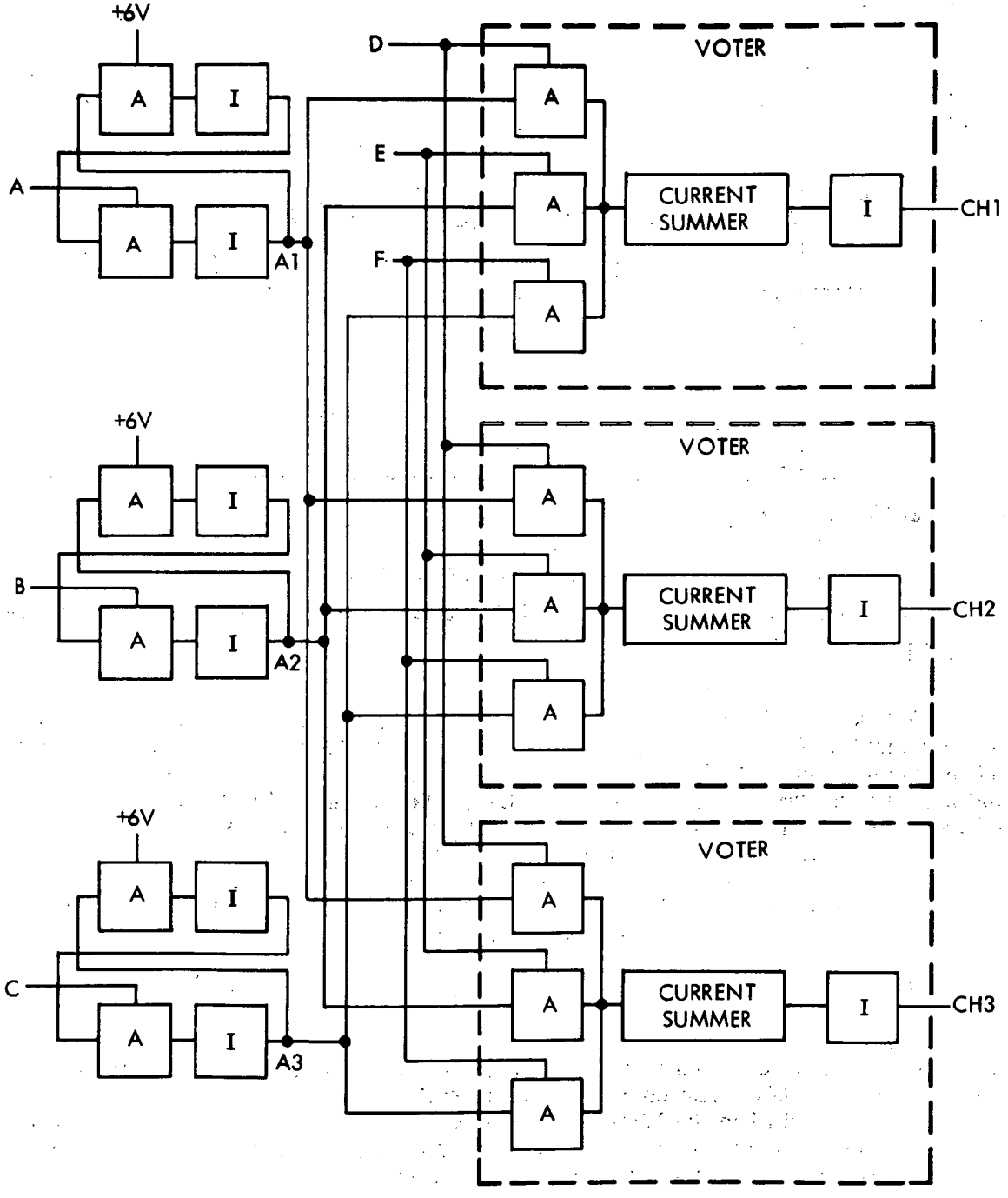


Figure 2-12. Typical Computer Voter Group and Input Circuits

Channel Being Selected	Inputs on Figure 2-12						Configuration of Other Channels
	A	B	C	D	E	F	
CH1	+6 MS	GRD	GRD	+12 MS	+12 MS	GRD	CH2=0 CH3=1
	+6 MS	GRD	GRD	+12 MS	GRD	+12 MS	CH2=1 CH3=0
CH2	GRD	+6 MS	GRD	+12 MS	+12 MS	GRD	CH1=0 CH3=1
	GRD	+6 MS	GRD	GRD	+12 MS	+12 MS	CH1=1 CH3=0
CH3	GRD	GRD	+6 MS	+12 MS	GRD	+12 MS	CH2=0 CH1=1
	GRD	GRD	+6 MS	GRD	+12 MS	+12 MS	CH2=1 CH1=0

Figure 2-13. Channel Selection Methods

Note that there are two ways of selecting each channel and therefore two combinations of energized relays. For example, CHANNEL 1 can be selected when $\begin{pmatrix}\text{CH2=0}\\\text{CH3=1}\end{pmatrix}$ or when $\begin{pmatrix}\text{CH2=1}\\\text{CH3=0}\end{pmatrix}$.

2-71. One set of relay contacts grounds the +12 MS supply points in one channel of all seven computer modules, and applies +12 MS to the remaining two channels. Another set of contacts apply +6 MS to one channel of all modules, and applies GRD to the remaining two channels. Figure 2-13 lists the proper voltage conditions for correct channel selection. An ILLEGAL PATH error will exist if the combinations of energized relays is such that the above conditions are not met. A third set of contacts provide a ground return for one of the six channel indicator lamps. Two more sets of contacts provide paths for energizing 7 of the 42 CHANNEL-MODULE lamps. The lamps that light correspond to the channel indicator lamp that is lit. For instance, if the CH2 $\begin{pmatrix}\text{CH1=0}\\\text{CH3=1}\end{pmatrix}$ lamp is lit, then the CHANNEL 2 $\begin{pmatrix}\text{CH1=0}\\\text{CH3=1}\end{pmatrix}$ lamps for all seven modules are also lit.

2-72. When the ALL switch is pressed, the logic associated with this switch picks and holds relay 01B8K01. The normally open 01B8K01 contacts apply +6 MS to those lines that were grounded when the LVDCME was in the single channel mode. When relay 01B8K01 picks, it removes the GRD from the CHANNEL-MODULE lamps and also removes the ground return from the channel indicator lamps.

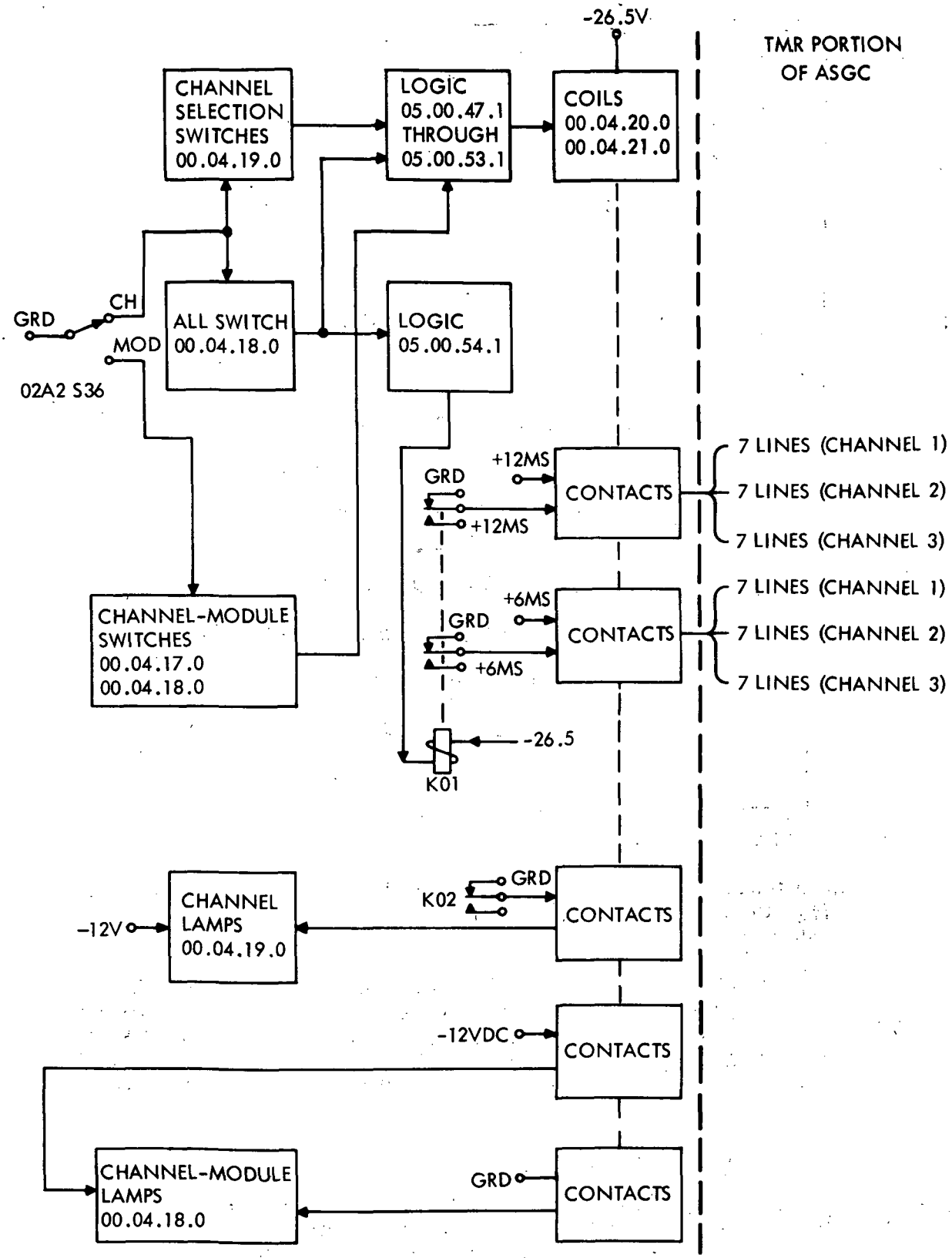


Figure 2-14. Channel/Module Switching Circuits

Switch	Relays Picked (01B8 —)
CH1	K05, K07, K10, K12, K15, K17, K20, K22, K25, K27, K30, K32, K35, and K37; or K05, K06, K10, K11, K15, K16, K20, K21, K25, K26, K30, K31, K35 and K36
CH2	K04, K06, K07, K09, K11, K12, K14, K16, K17, K19, K21, K22, K24, K26, K27, K29, K31, K32, K34, K36, and K37; or K4, K5, K6, K9, K10, K11, K14, K15, K16, K19, K20, K21, K24, K25, K26, K29, K30, K31, K34, K35 and K36
CH3	K03, K06, K07, K08, K11, K12, K13, K16, K17, K18, K21, K22, K23, K26, K27, K28, K31, K32, K33, K36, and K37; or K03, K05, K07, K08, K10, K12, K13, K15, K17, K18, K20, K22, K23, K25, K27, K28, K30, K32, K33, K35 and K37

Figure 2-15. Channel Selection Relay Table

2-73. In the automatic mode, the LVDCME is capable of accepting channel switching commands from the PTC. After a computer HALT is applied, CIO commands select channels as shown in figure 2-11.

2-74. MODULE SWITCHING. When HALT is applied and the CHANNEL/MODULE switch is in the MODULE position, its contacts allow the 21 CHANNEL-MODULE switches to control channel selection in each of the computer modules. Figure 2-16 lists the relays that are picked as each of the CHANNEL-MODULE switches are pressed. Any other combination of relays picked for a particular MODULE selection will cause an ILLEGAL PATH error.

2-75. MEMORY LOADER/DATA DISPLAY.

2-76. The Memory Loader/Data Display contains the circuits necessary to perform the memory load - memory verify and data display functions (see figure 10-30 sheet 3). The majority of these circuits are used in both the memory load - memory verify and data display functions. Consequently although this discussion treats the two functions separately only one circuit description is included.

Channel-Module	Relays Picked	
	Initial	Alternate
CH1 MOD1	K05, K07	K05, K06
CH2 MOD1	K04, K06, K07	K04, K05, K06
CH3 MOD1	K03, K06, K07	K03, K05, K07
CH1 MOD2	K10, K12	K10, K11
CH2 MOD2	K09, K11, K12	K09, K10, K11
CH3 MOD2	K08, K11, K12	K08, K10, K12
CH1 MOD3	K15, K17	K15, K16
CH2 MOD3	K14, K16, K17	K14, K15, K16
CH3 MOD3	K13, K16, K17	K13, K15, K17
CH1 MOD4	K20, K22	K20, K21
CH2 MOD4	K19, K21, K22	K19, K20, K21
CH3 MOD4	K18, K21, K22	K18, K20, K22
CH1 MOD5	K25, K27	K25, K26
CH2 MOD5	K24, K26, K27	K24, K25, K26
CH3 MOD5	K23, K26, K27	K23, K25, K27
CH1 MOD6	K30, K32	K30, K31
CH2 MOD6	K29, K31, K32	K29, K30, K31
CH3 MOD6	K28, K31, K32	K28, K30, K32
CH1 MOD7	K35, K37	K35, K36
CH2 MOD7	K34, K36, K37	K34, K35, K36
CH3 MOD7	K33, K36, K37	K33, K35, K37

Figure 2-16. Relays Picked for Module Selection

2-77. MEMORY LOAD - MEMORY VERIFY.

2-78. The memory load - memory verify function is selected when the ML/DD pushbutton is in the ML position. The computer memory is loaded and/or verified when this function is selected. The contents of the tape reader register and the display registers are displayed by corresponding COMMAND and COMPUTER lamps respectively. These lamps are used in conjunction with the ERROR lamps for failure analysis. The memory load - memory verify function is divided into three operations as follows:

1. Tape reader control.

2. Tape reader register loading.

3. Data transfer.

2-79. TAPE READER CONTROL. The tape reader is controlled by the TAPE READER CONTROL and AUTO/MANUAL pushbuttons. The PWR ON/PWR OFF pushbutton turns the tape reader power on or off. The direction of tape flow is controlled by the FORWARD/REVERSE pushbutton (FORWARD is a clockwise flow and REVERSE is a counterclockwise flow). The INHIBIT READER CONTROL pushbutton turns the tape spooler power on or off (this permits manual indexing of the tape). The tape reader can be operated in the AUTO or MANUAL mode.

2-80. The AUTO mode which is used for reading the tape is selected when the AUTO/MANUAL pushbutton is in the AUTO position. The tape is read in the FORWARD mode; the REVERSE mode is used for tape rewind. The tape reader is started by pressing the START pushbutton and continues to run until the stop pushbutton is pressed, an error is detected, or the last tape word is read (tape address of 00001). When the last tape word is read the tape automatically stops and rewinds to the beginning of the first tape word (tape address of 11111).

2-81. The MANUAL mode which is used for loading the tape on the tape spooler and for initially positioning the tape is selected when the AUTO/MANUAL pushbutton is in the MANUAL position. If the leader portion of the tape (sprocket holes only) is under the tape reader read head, the tape advances to the beginning of the first tape word when the MANUAL ADVANCE TAPE pushbutton is pressed. When the information portion of the tape is under the tape reader read head the tape advances one word every time the MANUAL ADVANCE TAPE pushbutton is pressed.

2-82. TAPE READER REGISTER LOADING. The tape reader register can be loaded with information generated automatically by the tape reader or manually with switches.

2-83. Automatic Tape Reader Register Loading. In the AUTO mode the tape reader register is loaded with information stored on the memory load and verify tape. This tape is comprised of eight channels and a sprocket hole (see figure 2-17). A tape word consists of nine tape characters each of which contains eight bit locations. The value of each bit will be a "1" if a hole is punched in the tape and a "0" if the tape is blank.

2-84. Channel 7 (Sequence Channel) always contains a "0" in tape characters 1 through 8 and a "1" in tape character 9. Channel 8 (Parity Channel) contains a "1" in any tape character that contains an even number of "1's" in channels 1 through 7. SYL1 PB will be a "1" if data bit locations SIGN and B1 through B12 contain an even number of "1's" and SYL0 PB will be a "1" if data bit locations B13 through B25 contain an even number of "1's".

			(PARITY CHANNEL)						Channel 8
			(SEQUENCE CHANNEL)					Always A One	Channel 7
DS1	MM3	OA9	OA3	B3	B9	B15	B21	SYL1 PB	Channel 6
DS2	OP1	OA8	OA2	B4	B10	B16	B22	TAADR 5	Channel 5
DS3	OP2	OA7	OA1	B5	B11	B17	B23	TAADR 4	Channel 4
									Sprocket Holes
DS4	OP3	OA6	SIGN	B6	B12	B18	B24	TAADR 3	Channel 3
MM1	OP4	OA5	B1	B7	B13	B19	B25	TAADR 2	Channel 2
MM2	DUP LEX	OA4	B2	B8	B14	B20	SYL0 PB	TAADR 1	Channel 1
1	2	3	4	5	6	7	8	9	Tape Character

Note: The tape address bits (TAADR 1 through TAADR 5) are used for automatic control of the tape reader and data transfer control circuits.

Figure 2-17. Memory Load and Verify Tape Format

2-85. The tape is read one tape character at a time at a rate of 500 characters per second until a complete tape word is read. The logic value of each bit located in channels 1 through 6 except SYL0 PB and SYL1 PB is stored in a corresponding position of the tape reader register. Parity and sequence checks are performed on each tape character and if an error is detected the tape stops. If any other error is detected the tape stops on tape character 9. When no errors are detected the next word is read. This process is continued until the complete tape is read.

2-86. Manual Tape Reader Register Loading. In the MANUAL mode the tape reader register is loaded with information generated by the DATA ADDRESS, DATA, and TAPE ADDRESS pushbuttons. Pressing a DATA ADDRESS or DATA pushbutton will complement the value stored in the corresponding position of the tape reader register. These positions of the tape reader register are also cleared when the COMMAND DISPLAY RESET pushbutton is pressed. Pressing a TAPE ADDRESS pushbutton will complement the value stored in the corresponding position of the tape reader register providing the ADV CTR/SEL ADR pushbutton is in the SEL ADR position.

2-87. DATA TRANSFER. The data address and data information stored in the tape reader register is serialized at the computer timing rate. This information is then sent to the computer unless:

1. A serial parity error is detected in the AUTO or MANUAL $\overline{\text{REPEAT}}$ mode.

2. The VERIFY ONLY pushbutton is in the VERIFY ONLY position during a load operation.

3. The VERIFY ONLY pushbutton is in the VERIFY ONLY position and the tape address is 00010.

4. An error generated during the previous load or verify operation has not been reset.

5. The data information is not transferred during a verify operation or when a data address compare error occurs.

2-88. The computer after receiving the data address information sends this information back to the Memory Loader. Correct data address transfer is then substantiated by comparing the data address information generated by the Memory Loader with the data address information received from the computer. The current computer sector, syllable, module, duplex, OP code, and operand address bit values contained in the data address information are stored in corresponding display register positions.

2-89. During a load operation (OP code 1011) the data information is sent to the computer and loaded into the memory location specified by the sector, syllable, module, duplex and operand address bit values. During a verify operation (OP code 1111) the data information contained in the memory location specified by the sector, syllable, module, duplex and operand address bit values is sent to the Memory Loader. A correct memory load is verified by comparing the data information generated by the Memory Loader with the data address information received from the computer. The current computer data bit values contained in the data address information are stored in corresponding data display shift register positions.

2-90. Data transfer occurs in either the AUTO or MANUAL mode. These two modes of transferring data are discussed in the following paragraphs.

2-91. Automatic Data Transfer. In the AUTO mode data is continuously sent to the computer as long as the tape is running forward and an error is not detected. Since the data transfer is the same for each tape word, only the transfer of information for one tape word is discussed. Because the tape reader timing rate is much slower than the computer timing rate, six computer operation cycles (cycle 0 through cycle 5) are required to complete one load or verify operation.

2-92. The tape reader register is loaded during cycles 0 and 1. During phase A of cycle 2 the serial parity check is performed. Data address information is sent to the computer on the DIN line (TMR) during cycles 2 and 3. The sector, syllable, and module bit values are transferred during phase B of cycle 2. The OP code and operand address bit values are transferred during phase C of cycle 2 and phase A of cycle 3.

2-93. Data address information is serially transferred from the computer to the Memory Loader on the TRS and HOPC1 lines (TMR) and parallel transferred on the OP1 through OP4 and A1 through A9 lines (TMR). Sector, syllable, duplex and module bit values are serially gated into the sector- syllable - module shift register. This data is then parallel transferred to the sector- syllable-module buffer register and from there

parallel transferred to the sector- syllable-module display register. OP code and operand address bit values are parallel transferred into the address shift register and from there parallel transferred to the instruction display register.

2-94. Correct data address transfer to the computer is substantiated during cycles 2 and 3 by performing two compares. Sector, syllable, duplex and module bit values appearing on the DIN line are compared with corresponding bit values appearing on the TRS line during phase C of cycle 2. OP code and operand address bit values stored in the tape reader register are compared with corresponding bit values received from the computer on the OP1 through OP4 and A1 through A9 lines. Several other compares are performed to substantiate the correct internal transfer of data between the shift, buffer, and display registers.

2-95. Data information is sent to the computer on the DIN line during a load operation. Data bit values 12 through 25 are transferred during phase B of cycle 3 and data bit values SIGN and 1 through 11 are transferred during phase C of cycle 3. During a verify operation data information is received from the computer on the TRS and AI3 lines. The data bit values appearing on the TRS line are serially gated into the data display shift register during phases B and C of cycle 3 and phase A of cycle 4. Data bit values appearing on the AI3 line are serially gated into the data display shift register during phases B and C of cycle 4 and phase A of cycle 5.

2-96. A correct memory load is verified by performing three compares during cycles 3, 4, and 5. The data bit values appearing on the DIN line are compared with the data bit values appearing on the TRS line during phases B and C of cycle 3 and phase A of cycle 4. The data bit values appearing on the DIN line are also compared with the data bit values appearing on the AI3 line during phases B and C of cycle 4 and phase A of cycle 5. The tape reader register data syllable 0 and syllable 1 parity bit values are compared with the parity bit values generated by the computer memory circuits.

2-97. A correct transfer of data into the data display shift register is substantiated by performing one compare. The data bit values appearing on the DIN line are compared with the data bit values appearing on the serial output of the data display shift register.

2-98. Manual Data Transfer. In the manual mode data transfer is controlled by the REPEAT/$\overline{\text{REPEAT}}$ and ADDRESS COMPUTER pushbuttons. When the REPEAT/$\overline{\text{REPEAT}}$ pushbutton is in the $\overline{\text{REPEAT}}$ position data transfer is accomplished every time the ADDRESS COMPUTER pushbutton is pressed. When a load operation is selected the data information is loaded into the computer memory and then the memory load is automatically verified.

2-99. When the REPEAT/$\overline{\text{REPEAT}}$ pushbutton is in the REPEAT position data transfer is accomplished continuously. Load and verify operations are alternately performed as long as the REPEAT mode is maintained.

2-100. The timing for the transfer of data address and data information between the Memory Loader and the computer is the same as in the AUTO mode. The compares performed are also the same as in the AUTO mode. The contents of the display registers are cleared when the COMPTR DISPLAY RESET pushbutton is pressed.

2-101. DATA DISPLAY.

2-102. The data display function is selected in the MANUAL mode when the ML/DD pushbutton is in the DD position. When this function is selected, computer data associated with a data address or instruction address can be monitored. The data display function is divided into two operations as follows:

1. Tape reader register loading.

2. Data selection and storage.

2-103. TAPE READER REGISTER LOADING. The tape reader register is loaded with information generated by the INSTRUCTION ADDRESS or DATA ADDRESS pushbuttons. The instruction address and data address positions of the tape reader register are displayed by corresponding COMMAND lamps. These positions are cleared when the COMMAND DISPLAY RESET pushbutton is actuated. Pressing an INSTRUCTION ADDRESS or DATA ADDRESS pushbutton complements the value stored in the corresponding position of the tape reader register.

2-104. DATA SELECTION AND STORAGE. The data selection and storage operation occurs in either the PRESENT or PAST mode. The PRESENT mode is forced until a computer single step operation is commanded. When this operation is commanded the PAST and PRESENT modes are alternately selected every time the PAST/PRESENT pushbutton is actuated.

2-105. Present Data Selection and Storage. In the PRESENT mode current computer sector, syllable, duplex, and module bit values appearing on the TRS or AI3 lines (TMR) are serially gated into the sector- syllable-module shift register (SSMSR). TRS information is gated into the SSMSR for computer HOP and CDS instructions. AI3 information is gated into the SSMSR for any other computer instruction. The contents of the SSMSR are then parallel transferred into the sector- syllable-module buffer register.

2-106. Current computer OP code and address bit values appearing on the OP1 through OP4 and A1 through A9 lines (TMR) are parallel transferred into the address shift register. The address bit values (A1 through A8) are transferred during phase A and the operand address bit values (OP1 through OP4 and OA1 through OA9) are transferred during phase C.

2-107. The data address and instruction address bit values stored in the tape reader register are then compared with the current computer data address and instruction address bit values. An address compare occurs on an instruction address when the ADDRESS COMPARE pushbutton is in the INS position. When this pushbutton is in the DATA position an address compare occurs on the data address.

2-108. An address compare occurs every time the tape reader register and computer address bit values correspond when the REPEAT/SINGLE pushbutton is in the REPEAT position. When this pushbutton is in the SINGLE position an address compare occurs the first time the tape reader register and computer address bit values correspond after the COMPTR DISPLAY RESET pushbutton is actuated. An address compare also occurs every time an advance operation is commanded in the CST mode.

2-109. When an address compare occurs, the contents of the sector-syllable-module buffer register are parallel transferred to the sector-syllable-module display register. Similarly the address and operand address bit values stored in the address shift register are parallel transferred into the instruction address display and instruction display registers respectively.

2-110. An address compare also serially gates TRS, AI3, MD7, MR1, PR0, HOPC1, SP1, SP2, RTC, MLC, or SSC information selected by the DISPLAY SELECT switch into the data display shift register. AI3-IA information appears in positions sign and 1 through 7. All other information appears in positions sign and 1 through 25.

2-111. The contents of the display registers are displayed by the corresponding COMPUTER lamps. The display registers are cleared when the COMPTR DISPLAY RESET pushbutton is actuated.

2-112. Past Data Selection and Storage. In the PAST mode current computer data appearing on the TRS and AI3 lines (TMR) is serially gated into the corresponding history delay lines. Similarly the associated data and instruction addresses appearing at the serial outputs of the sector-syllable-module shift and address shift registers are gated into the address history delay line. When a computer single step operation is commanded the contents of the delay lines, information generated during the last 13 computer operation cycles, are continuously recirculated.

2-113. During a computer multiply or divide operation current computer data appearing on the MD7, MR1 and PR0 lines (TMR) is serially gated into the corresponding history delay lines. At the completion of the multiply or divide operation the contents of these delay lines, data generated during the development of the result and the partial products/quotients of the multiply or divide operation, are continuously recirculated.

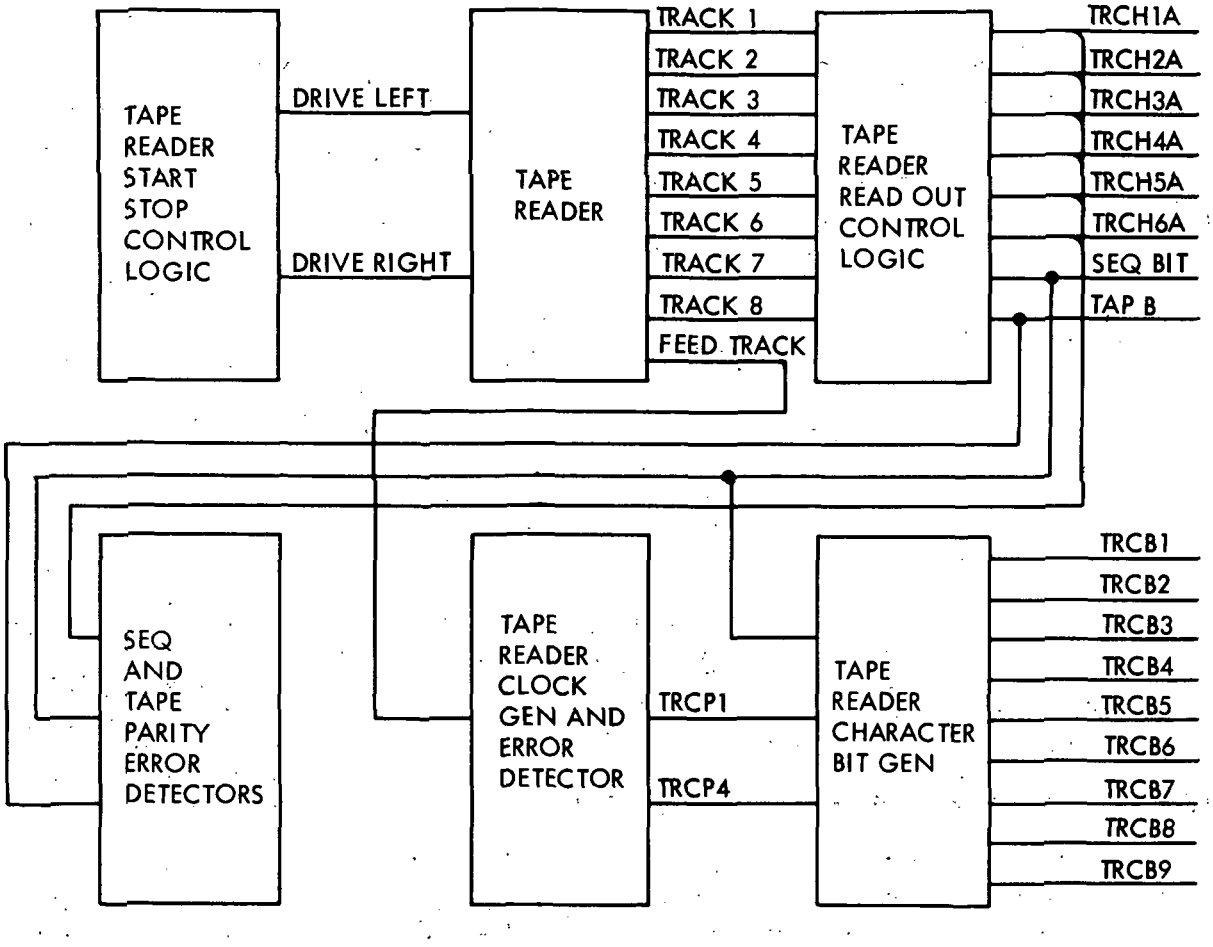
2-114. Desired information is then selected with the DISPLAY SELECT and WORD switches and transferred to the display registers. The information transfer is the same as in the PRESENT mode.

2-115. With the DISPLAY SELECT switch in the TRS or either AI3 position, data and the corresponding instruction and data addresses generated during one of the last 13 computer cycles is transferred into the display registers. With the WORD switch in the T position, current information is transferred. When the WORD switch is in position T-1 through T-12 data generated in one of the 12 computer operation cycles preceding the current operation cycle is selected. The computer operation cycle selected precedes the current one by the number appearing after the T.

2-116. While the DISPLAY SELECT switch is in the MD7, MR1, or PR0 position, data generated during the last multiply/divide operation performed is transferred into the data display shift register. The instruction and data addresses are invalid and therefore their transfer is inhibited. When the WORD switch is in the T position, data generated at the time the result was developed is selected. With the WORD switch in positions T-1 through T-12, data generated at the time one of the partial products/quotients was developed is selected. The partial product/quotient selected corresponds to the number appearing after the T.

2-117. MEMORY LOADER/DATA DISPLAY CIRCUIT DESCRIPTIONS.

2-118. TAPE READER TIMING AND CONTROL CIRCUITS. The tape reader timing and control circuits provide the necessary signals to control the tape reader and to load information into the tape reader register. The breakdown of the tape reader timing and control circuits is shown on figure 2-18.



NOTE: DATA FLOW IS FOR THE AUTO MODE ONLY.

Figure 2-18. Tape Reader Timing and Control Circuits

2-119. Tape Reader Start, Stop Control Logic. Automatic and manual control of the tape reader is accomplished by the tape reader start, stop control logic (see figure 10-30, sheets 13 and 14). The tape is transported in the reverse direction when the DRIVE LEFT signal is a "0" and in the forward direction when the DRIVE RIGHT signal is a "0". When both DRIVE LEFT and DRIVE RIGHT signals are "1's" the tape is stopped.

2-120. DRIVE LEFT and DRIVE RIGHT are two outputs of the run tratch. The three states of this tratch are as follows:

State	RUN	DRIVE LEFT	DRIVE RIGHT
1	"0"	"1"	"1"
2	"1"	"1"	"0"
3	"1"	"0"	"1"

The run tratch is forced to its first state by any one of the following: a STOP signal; a sequence error (SEQ ERR 2) while the tape reader is in the FORWARD AUTO mode; or a tape reader clock pulse error (TRCP ERR). The run tratch is forced to its second and third states by F and R START signals respectively. When the LVDCME is in the SELF CHECK mode and the FREE RUN READER pushbutton is in the FREE RUN READER position the run tratch logic is bypassed. DRIVE LEFT is now forced to a "0" if the REVERSE mode is selected and DRIVE RIGHT is forced to a "0" if the FORWARD mode is selected.

2-121. The STOP signal is the set output of a latch (stop latch) which is set as follows:

1. By pressing the STOP pushbutton.

2. By a tape address of 11111 when the tape reader is in the AUTO REVERSE mode.

3. By an EOP signal which is generated by a tape address of 00001 when the tape reader is in the AUTO FORWARD mode or by a FREE RUN SS signal.

4. By the first sequence bit sensed when the tape reader is in the MANUAL mode and the SKIP FIRST latch is reset.

5. By an error stop reader signal when the tape reader is in the AUTO FORWARD mode and a sequence bit is sensed (SAM ERRS).

The stop latch is reset by an error reset signal or at TRCP4 time. When the direction of tape flow is changed, the SKIP FIRST latch is set by the first and reset by the second sequence bit sensed. This ensures that the tape will advance one word before the stop latch is set.

2-122. The error stop reader (ESR) signal is normally generated by a parity, timing, compare or illegal path error, or by a disagreement or voter error when all three TMR channels are selected. In the self check mode ESR is generated as follows:

1. When voter errors are simultaneously generated by two TMR channels.

2. By a tape address of 00110 in the INVERT ERROR mode when no errors are generated.

3. When the 1 pushbutton is in the 1 position.

2-123. The R START signal is generated as follows:

1. By pressing the MANUAL ADVANCE TAPE pushbutton when the tape reader is in the MANUAL REVERSE mode and the TRCP ERR signal is a "0".

2. By pressing the START pushbutton when the AUTO REVERSE, and ML modes are selected, KWAIN NOT A is a "1", and the error latches are all reset.

3. By an automatic reverse start signal (AUTO R START) generated by an EOP.

The F START signal is generated as follows:

1. By pressing the MANUAL ADVANCE TAPE pushbutton when the tape reader is in the MANUAL FORWARD mode and the TRCP ERR signal is a "0".

2. By pressing the START pushbutton when the AUTO FORWARD, and ML modes are selected, KWAIN NOT A is a "1", and the error latches are all reset.

When the tape reader is in the FREE RUN SS mode the R and F START levels are forced to "0's".

2-124. A KWAIN signal is generated (KWAIN NOT A is a "0") as follows:

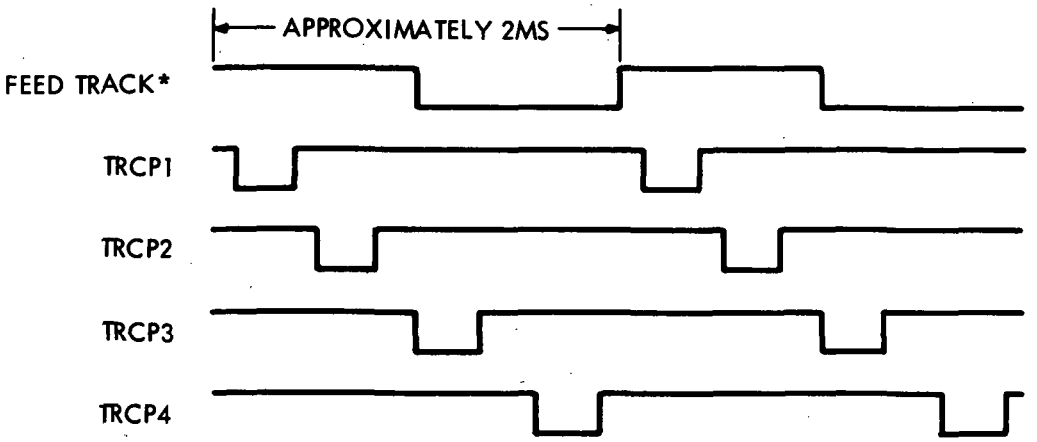
1. During the time prior to the sensing of the first sequence bit when ACME power is turned on.

2. During the time prior to the sensing of the first sequence bit after a sequence error 2 is generated.

3. If the control latches in the tape reader character bit generator stabilize in the wrong configuration when the tape reader stops.

2-125. Tape Reader Clock Generator. The tape reader clock generator generates four timing pulses (TRCP1, TRCP2, TRCP3, and TRCP4) which are used throughout the tape reader control circuitry (see figure 10-30, sheet 7). The tape reader clock generator is triggered as follows:

1. By the tape sprocket holes, when the tape reader is running. (See figure 2-19 for timing.)



*FEED TRACK IS AN UP LEVEL FOR THE SPROCKET HOLE

Figure 2-19. Tape Reader Clock Pulse Timing

2. By pressing any one of the INSTRUCTION ADDRESS, DATA ADDRESS, DATA, or TAPE ADDRESS pushbuttons when the tape reader is stopped and in the MANUAL mode.

3. By a 500 CPS multivibrator oscillator when the tape reader is in the SELF CHECK and FREE RUN SS modes.

2-126. Tape Reader Clock Pulse Error Detector. Tape reader clock pulse errors are stored in a latch which provides outputs TRCP ERR and TRCP ERR NOT (see figure 10-30, sheet 7). A tape reader clock pulse error is generated as follows:

1. If a missing tape reader clock pulse is detected.

2. If an overlap occurs between adjacent tape reader clock pulses.

3. When an INSTRUCTION ADDRESS SECTOR IS1 through IS4 pushbutton is pressed and the tape reader is in the FREE RUN SS mode.

4. If the delay between tape reader clock pulse "1's" exceeds 30 MS when the tape reader is in the AUTO mode and running.

5. For the duration of the time an INSTRUCTION ADDRESS, DATA ADDRESS, DATA, or TAPE ADDRESS pushbutton is pressed when the tape reader is stopped in the MANUAL mode, and the tape reader is not in the FREE RUN SS mode.

2-127. Tape Reader Character Bit Generator. The tape reader character bit generator generates nine bits (TRCB1 through TRCB9). (See figure 10-30, sheet 8.) These nine bits identify a specific tape character of a tape reader word. The tape reader character bits are generated automatically, or manually with switches.

2-128. Automatic generation of the tape reader character bits occurs when the tape reader is in the AUTO FORWARD mode, or the tape reader is in the FREE RUN SS mode. The configuration of 11 control latches determines the tape reader character bit timing. (See figure 2-20.) The outputs of these control latches are applied to AND circuits to produce the tape reader character bits. Automatic generation of TRCB9 is also accomplished whenever a sequence bit is sensed and the tape reader is not in either the FREE RUN SS, or the AUTO FORWARD mode.

2-129. Tape reader character bits are generated manually by the DATA ADDRESS, DATA, or TAPE ADDRESS pushbuttons when the tape reader is stopped and in the MANUAL mode. The tape reader character bit affected will correspond to the tape character containing the information that the pushbutton is simulating. Each tape reader character bit is now generated by one of nine latches. Each latch is set for the duration of the time that one of the group of pushbuttons feeding it is pressed. TRCB9 is forced to a "0" when the ADV CTR/SEL ADR pushbutton is in the ADV CTR position.

2-130. Tape Reader Read Out Control Logic. The tape reader read out control logic converts inputs from the tape reader, or from switches to eight output signals (TRCH1A through TRCH6A, SEQ BIT, and TAP B). (See figure 10-30, sheet 13.)

2-131. In the AUTO mode, tape reader information is sent to the tape reader read out control logic on eight lines (TRACK 1 through TRACK 8). These lines correspond to the eight tape channels (a "0" represents a bit of tape information). The inverses of TRACK 1 through TRACK 6 are sampled at TRCP1 time to determine the logic values of TRCH1A through TRCH6A, respectively. The inverses of TRACK 7 and TRACK 8 respectively determine the logic values of SEQ BIT and TAP B.

2-132. In the MANUAL mode, pressing a DATA ADDRESS, DATA, or TAPE ADDRESS pushbutton will set one of six latches (LACH 1 through LACH 6) which correspond to tape channels 1 through 6. The set outputs of these latches are ANDed with the outputs of a control latch (MANCH latch) to determine the logic values of TRCH1A through TRCH6A. The MANCH latch is set when the tape reader register position that corresponds to the pushbutton pressed contains a "0".

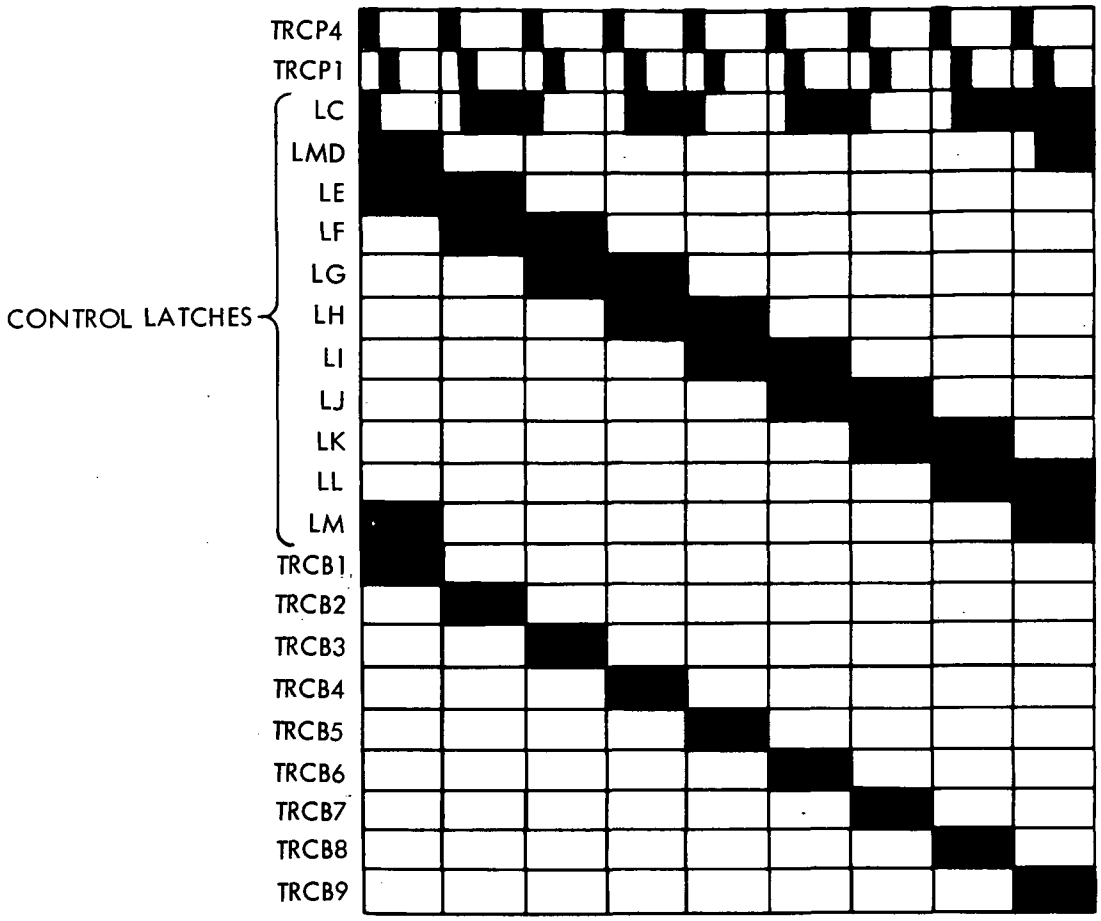


Figure 2-20. Tape Reader Character Bit Generator Timing

2-133. Sequence Error Detectors. Two sequence errors (SE1 and SE2) are generated if an error occurs when the tape reader is running forward (see figure 10-30, sheet 7). SE1 and SE2 are the set outputs of two latches which are set by SEQ BIT and TRCB9 NOT or SEQ BIT NOT and TRCB9 signals.

2-134. Tape Parity Error Detector. The tape parity error detector performs an odd parity check on each tape character when the tape reader is in the AUTO mode and running forward (see figure 10-30, sheet 46). A tape parity error is generated if an even number of "1" bits are detected. Tape parity errors are stored in a latch which produces an output TPE ERR NOT.

2-135. MODE SELECTION CIRCUITS. The mode selection circuits generate eight signals (AUTO, MAN A, DD A, DD NOT A, ML A, ML NOT A, FWD A, and RVS A) which control the mode of operation of the Memory Loader/Data Display and tape reader. (See figure 10-30, sheet 14.) The configuration of these signals can only be changed when the tape reader is stopped.

2-136. Auto and MAN A are the outputs of a latch, which is alternately set or reset when the AUTO/MANUAL pushbutton is pressed. DD A and ML A and their inverses are the outputs of another latch which is alternately set or reset when the ML/DD pushbutton

is pressed and the MANUAL mode is selected. When the AUTO mode is selected DD A is forced to a "0". The AUTO signal is split into three lines, two of which are routed through drivers. This is indicated by the letters A, B, and C following AUTO.

2-137. FWD A and RVS A are the outputs of a binary counter which is complemented every time the FORWARD/REVERSE pushbutton is pressed. When an AUTO R START signal is generated the counter is cleared forcing FWD A and RVS A respectively to a "0" and a "1".

2-138. TAPE READER REGISTER. The tape reader register is a 69 position latch register that stores input information to the Memory Loader/Data Display (see figure 10-30, sheets 9 through 12). The contents of the tape reader register are displayed by corresponding COMMAND display and tape ADDRESS indicator lamps. The tape reader register is cleared except for the tape address positions by pressing the COMMAND DISPLAY RESET pushbutton.

2-139. Tape information or information generated by the DATA ADDRESS, DATA or TAPE ADDRESS pushbuttons is stored in 52 positions of the tape reader register. A specific bit of information is identified by sampling the tape reader channel containing this bit at the corresponding tape reader character bit time. The logic value of this bit is then stored in a latch. Additional control of the latch which stores the logic value of the OP3 bit is provided by two signals (STROP3 and RTOP3). This latch is set by a STROP3 signal and reset by a RTOP3 signal.

2-140. The remaining 17 positions of the tape reader register are used to store the instruction address information. The logic value of two control signals (LAST A and LARE A) determine whether a "1" or "0" is stored in these positions. The latch assigned to the INSTRUCTION ADDRESS pushbutton pressed will set if LAST A is a "1" and reset if LARE A is a "1". LAST A and LARE A are respectively identical to the set and reset outputs or a latch (LACH 7) when the tape reader is in the MANUAL mode. This latch is set when the tape reader register position that corresponds to the pushbutton pressed contains a "0".

2-141. TAPE READER REGISTER PARITY DETECTOR. The tape reader register parity detector generates a parity bit (SERIALIZER PARITY BIT) when the data address, instruction address, and data stored in the tape reader register contains an even number of "1's" (see figure 10-30, sheet 46). Figure 2-21 shows the tape reader register parity detector which consists of four binary counters and a parity detector.

2-142. The configuration of the four binary counters (identified as "A", "B", "C", and "D" for this discussion) is determined by the number of "1's" contained in the information feeding them. In the AUTO mode the configuration of "B" is not changed. "A" which is set at the beginning of each tape word is complemented at tape reader character bit times 1, 2, 3, and 4 if the part of the data address located in these tape characters contains an odd number of "1's". "C" and "D" are respectively set by the presence or cleared by the absence of tape SYL 0 and SYL 1 parity bits.

2-143. In the MANUAL mode the binary counters are initially set when the COMMAND DISPLAY RESET pushbutton is pressed. Each counter is then complemented every time one of the group of pushbuttons feeding it is pressed. "A" is also complemented every time a 755PM signal is generated.

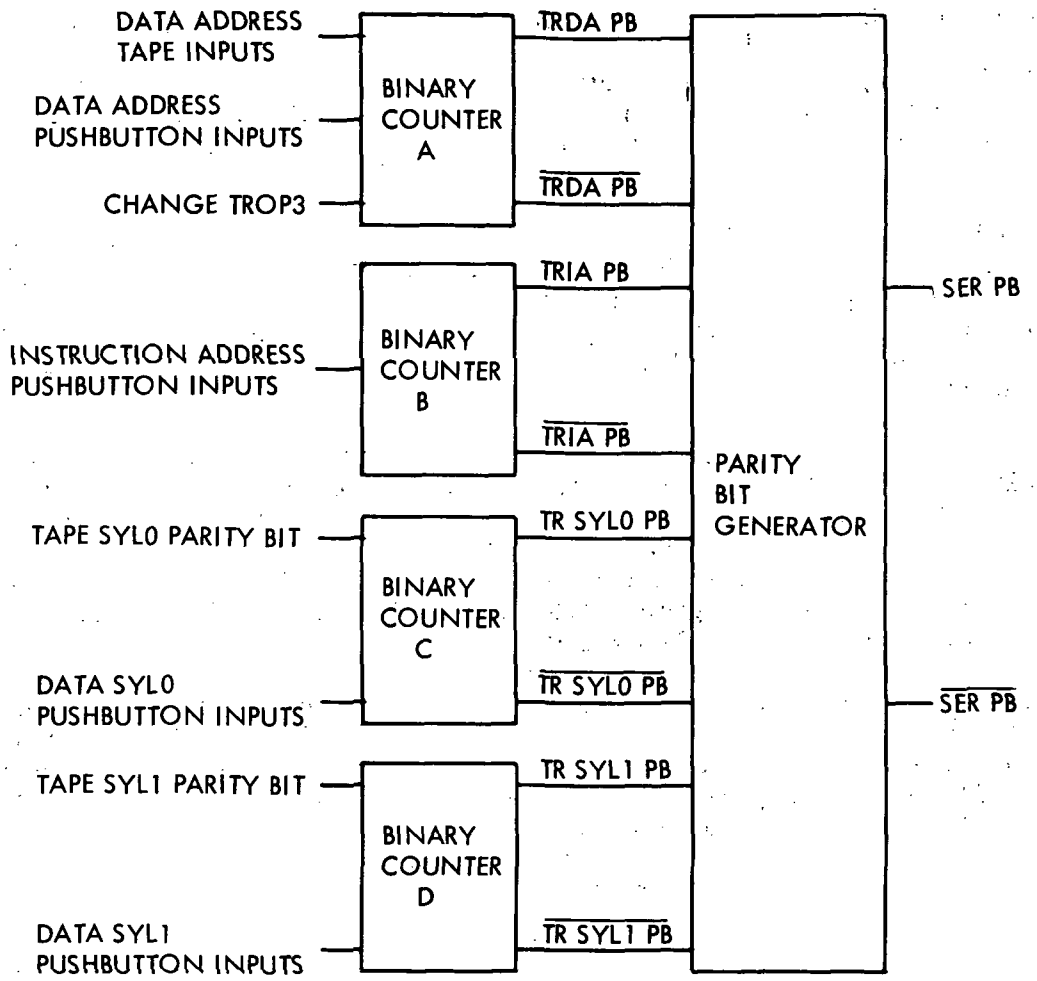


Figure 2-21. Tape Reader Register Parity Detector

2-144. The outputs of the four binary counters are applied to a parity detector which produces outputs SER PB and SER PB NOT. SER PB and SER PB NOT are forced to a "1" and a "0" respectively when none, two, or four of the binary counters are set. Any other condition will force SER PB and SER PB NOT respectively to a "0" and a "1".

2-145. TAPE READER SERIALIZER. The tape reader serializer receives parallel information from the tape reader register and transforms this information into serial data on three lines (see figure 10-30, sheet 16). Data sector and module information appears on the DSMSO line, instruction information appears on the INSSO line, and data information appears on the DTSO line.

2-146. The tape reader register data is gated through the serializer by bit gates. Figure 2-22 shows the order in which bits are transferred on the three serializer output lines.

2-147. The serializer also provides two additional output lines (2BDDTSO and 2BDDTSO NOT). These signals are the outputs of a three-stage shift register which is fed by DTSO and DTSO NOT.

	DSMSO			INSSO			DTSO		
	PHA	PHB	PHC	PHA	PHB	PHC	PHA	PHB	PHC
BG1				TROA3	TROA3	TROA3		TRB25	TRB11
BG2				TROA4	TROA4	TROA4		TRB24	TRB10
BG3				TROA5	TROA5	TROA5		TRB23	TRB9
BG4				TROA6	TROA6	TROA6		TRB22	TRB8
BG5				TROA7	TROA7	TROA7		TRB21	TRB7
BG6	TRDDX	TRDDX	TRDDX	TROA8	TROA8	TROA8		TRB20	TRB6
BG7	TRDM1	TRDM1	TRDM1					TRB19	TRB5
BG8	TRDM2	TRDM2	TRDM2	TROP1	TROP1	TROP1		TRB18	TRB4
BG9	TRDM3	TRDM3	TRDM3	TROP2	TROP2	TROP2		TRB17	TRB3
BG10	TRDS1	TRDS1	TRDS1	TROP3	TROP3	TROP3		TRB16	TRB2
BG11	TRDS2	TRDS2	TRDS2	TROP4	TROP4	TROP4		TRB15	TRB1
BG12	TRDS3	TRDS3	TRDS3	TROA9	TROA9	TROA9		TRB14	TRSIGN
BG13	TRDS4	TRDS4	TRDS4	TROA1	TROA1	TROA1		TRB13	
BG14				TROA2	TROA2	TROA2		TRB12	

Figure 2-22. Tape Reader Serializer Outputs

2-148. SERIAL PARITY ERROR DETECTOR. A serial parity error is generated if the number of "1's" contained in the information appearing on the serializer outputs differs from the number of "1's" contained in the information feeding the tape reader register. (See figure 10-30, sheet 6.) Figure 2-23 is a block diagram of the serial parity error detector.

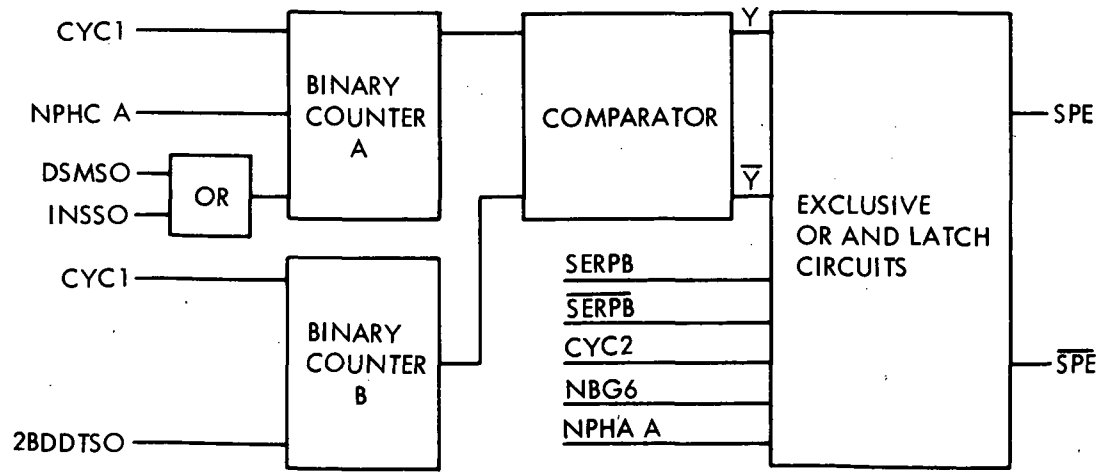


Figure 2-23. Serial Parity Error Detector

2-149. Two binary counters (identified as "A" and "B" for this discussion) are used to count the number of "1's" appearing on the serializer outputs. These counters, which are cleared at bit gate 10 of the preceding cycle 2 time are complemented every bit time whenever their inputs are "1's". Thus at phase A, bit gate 6 of cycle 2 both counters are set when an even number of "1's" appear on the serializer outputs except for two conditions:

1. A tape address of 00101 will cause "A" to be cleared.

2. A TRIA PB NOT will cause "B" to be cleared.

2-150. The outputs of the binary counters are compared and two signals (SPB and SPB NOT) which should correspond to SER PB and SER PB NOT are generated. These signals are applied to an exclusive OR comparator and if they do not correspond at phase A bit gate 6 of cycle 2 a latch is set indicating a serial parity error.

2-151. DATA TRANSFER CONTROL. The data transfer control circuits control the flow of information between the Memory Loader and the Computer. The data transfer control circuits consist of the cycle generator, the DIN control circuit, and the manual mode control circuits (see figure 10-30, sheet 6).

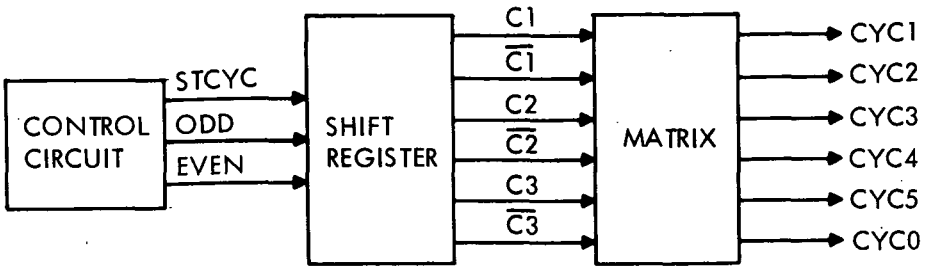
2-152. Cycle Generator. The cycle generator provides additional timing gates for the memory load and memory verification operations. Figure 2-24 shows the cycle generator which consists of a three-stage shift register, a shift control circuit, and a decoding matrix.

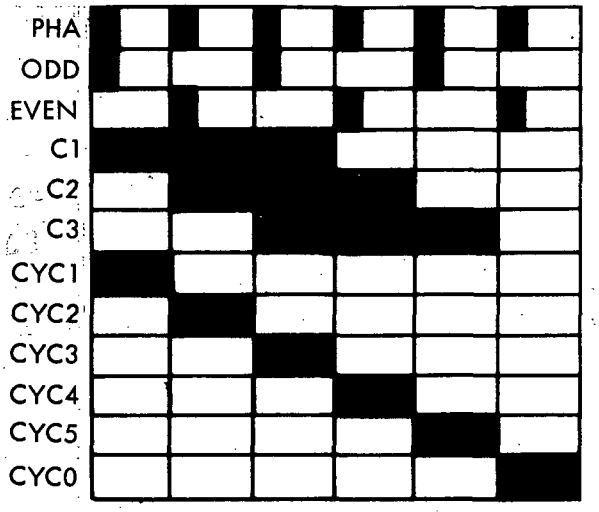
2-153. The shift control circuit provides two shift control gates (ODD and EVEN) that occur during alternate phase A's. Another output from the shift control circuit (STCYC) permits the shift register to step. The shift register provides outputs C1, C1 NOT, C2, C2 NOT, C3, and C3 NOT. These outputs are applied to a matrix which produces the cycle gates as follows:

CYC1 = C1 and C2 NOT
CYC2 = C2 and C3 NOT
CYC3 = C1 and C3
CYC4 = C1 NOT and C2
CYC5 = C2 NOT and C3
CYC0 = C1 NOT and C3 NOT

2-154. In the AUTO mode the cycle generator is started if the error latches are all reset and a transfer inhibit signal is not generated by the first phase A after a sequence bit is read by the tape reader. The cycle generator stops automatically after the last cycle gate (CYC0) is generated. CYC0 is maintained until the next sequence bit is read from the tape.

2-155. In the MANUAL mode the cycle generator is started by the SRPT NOT signal going to a "0". When the Memory Loader is in the REPEAT mode the cycle generator continues to operate as long as this mode is maintained. When the Memory Loader is in REPEAT, the cycle generator operates for a total of 12 cycles. The first six cycles are started by SPRT and the next cycles are started by STROP3, which is generated to enable automatic verification of manually loaded data.





NOTE: RESTING STATE OF CYCLE GENERATOR IS CYC0 = "1"

Figure 2-24. Cycle Generator

2-156. DIN Control Circuit. The DIN control circuit organizes information appearing on the three serializer outputs and sends this information to the computer on the three DIN lines. DSMSO information appears on the DIN lines during phase B of cycle 2. INSSO and DTSSO information appears on the DIN lines when the TATC and TDTTC gates respectively are "1's". When the Memory Loader is in the $\overline{\text{REPEAT}}$ mode a serial parity error forces the DIN lines to "0's".

2-157. The TATC gate is the output of a latch which is set from phase C, bit gate 8 of cycle 2 to phase A, bit gate 8 of cycle 3. The TDTTC gate is the output of a latch which is set from phase B of cycle 3 to phase A of cycle 4 except as follows:

1. When a verify command is generated (TROP3 NOT is a "0").

2. When a serial data compare error occurs (CETRS NOT is a "0") in the $\overline{\text{REPEAT}}$ mode.

2-158. Manual Mode Control Circuits. The manual mode control circuits generate seven signals (DTRPT, DTRPT NOT, SRPT NOT, 755PM, STROP3, and RTOP3). These signals control the memory load and verification operations when the Memory Loader is in the MANUAL mode.

2-159. DTRPT and DTRPT NOT are the outputs of a binary counter which is complemented every time the REPEAT/$\overline{\text{REPEAT}}$ pushbutton is pressed. SRPT NOT is the reset output of a latch which is set in the $\overline{\text{REPEAT}}$ mode from phase C bit gate 10 of cycle 0 to phase A bit gate 2 of cycle 1 every time the ADDRESS COMPTR pushbutton is pressed if the error latches are all reset.

2-160. 755PM, STROP3, and RTROP3 are the outputs of a tratch. The three configurations of this tratch are as follows:

Configuration	755PM	STROP3	RTROP3
1	"0"	"0"	"0"
2	"1"	"1"	"0"
3	"1"	"0"	"1"

The first configuration is forced by every bit gate 12. The tratch is forced to its second configuration at phase A, bit gate 11 of cycle 5 when the tape reader register contains a store command. The third configuration is forced only in the REPEAT mode at phase A, bit gate 10 of cycle 5 when the tape reader register contains a clear and add command.

2-161. TRANSFER CONTROL CIRCUIT. The transfer control circuit controls the transfer of information to the computer. A transfer inhibit signal is generated (TRANS INH NOT is forced to a "0") as follows:

1. For the duration of tape reader character bit 9 when the verify only latch is set and the tape reader register does not contain a clear and add command.

2. By a tape address of 00010 when the verify only latch is set.

3. When the skip first latch is set.

4. Whenever the tape reader is not in the FORWARD AUTO mode.

The verify only latch is alternately set or reset when the VERIFY ONLY pushbutton is pressed and the tape reader is stopped.

2-162. COMPARE ERROR CIRCUITS. (See figure 10-30, sheets 26, 29, 30, 31, 45, and 47.) The compare error circuits compare data generated by the Memory Loader with corresponding data from the computer. Compare errors are stored in 12 latches which provide outputs CETRS, CEHOPC1, CEBR14, CEAI3, CESSMSC, CESSMDR, CEAOC, CEINSDR, CEADRSR, CESSMBR, CESER, and CEPAR and their inverses. These latches are set as follows:

Latch	Set by
CETRS	A non compare of 2BDDTSO and NTRS data at any clock pulse Z when a CTRS signal is generated.
	A CESSMBR, CESSMDR, or CESSMSC error during phase B of cycle 3.
	A CEPAR error.

Latch	Set by
CEHOPC1	A CESSMBR, CESSMDR, or CESSMSC error during phase B of cycle 4.
CEBR14	A non compare of tape reader register syllable 0 or syllable 1 and computer buffer register A or B parity bits at bit gate 6 time of cycle 4.
CEAI3	A non compare of 2BDDTSO and NAI3 data at any clock pulse Z when a CAI3 signal is generated.
CESSMSC	A non compare of DSMSO and NHOPC1 data during cycle 3 at any clock pulse X when a SAM signal is generated. A non compare of DSMSO and NTRS data during cycle 2 at any clock pulse W when a SAM signal is generated.
CESSMDR	A non compare of the data sector-syllable-module tape reader register bits and the corresponding display register bits at phase B bit gate 3 of cycle 3 or 4.
CEAOC	A non compare of the OP code and operand address tape reader register bits and the corresponding computer OP code and operand address bits at phase B bit gate 2 of cycle 3.
CEINSDR	A non compare of the OP code and operand address tape reader register bits and the corresponding display register bits at phase C bit gate 4 of cycle 3.
CEADRSR	A non compare of INSSO data and corresponding address shift register data at any clock pulse X when a CASO signal is generated.
CESSMBR	A non compare of the data sector-syllable-module tape reader register bits and the corresponding buffer register bits at phase B bit gate 3 of cycle 3 or 4.
CESER	A non compare of 2BDDTSO and NTRS data at any clock pulse Z when a CTRS signal is generated. A non compare of 2BDDTSO and NAI3 data at any clock pulse Z when a CAI3 signal is generated.
CEPAR	A non compare of 2BDDTSO data and corresponding display register data at any clock pulse Z when a CAI3 signal is generated.

2-163. COMPARE ERROR CONTROL CIRCUITS. The compare error control circuits generate four signals (CTRS, CAI3, SAM, and CASO) which control the operation of the compare error circuits. The signals are the outputs of four latches and are generated as follows:

CTRS — During a verify operation from phase B bit gate 4 of cycle 3 to phase A bit gate 2 of cycle 4.

CAI3 — During a verify operation from phase B bit gate 4 of cycle 4 to phase A bit gate 2 of cycle 5.

SAM — Every cycle from phase C bit gate 6 to phase A bit gate 1.

CASO — From phase C bit gate 8 clock pulse Y of cycle 3 to phase A bit gate 7 clock pulse Y of cycle 4.

2-164. SECTOR-SYLLABLE-MODULE SHIFT REGISTER. (See figure 10-30, sheet 17.) The sector-syllable-module shift register (SSMSR) receives serial information on the NTRS, NHOPC1, HISTADR, or DSMSO lines. Information shifting through the SSMSR appears on 17 parallel outputs and one serial output. Figure 2-25 is a block diagram of the SSMSR which consists of 24 latches connected in series.

2-165. NTRS information is gated into the SSMSR during the PRESENT mode when a HOP (OP code 0000) or CDS (OP code 1110 and A9 NOT) instruction is received from the computer. NHOPC1 information is gated into the SSMSR during the present mode when any other instruction is received from the computer. In the PAST mode HISTADR information is gated into the SSMSR. When the display serializer output operation (DSO) is selected DSMSO information is gated into the SSMSR.

2-166. Sector, syllable, module, and duplex bit values received on the NTRS, NHOPC1, or DSMSO line appear at the corresponding SSMSR parallel outputs at phase A bit gate 3. Sector, syllable, module, and duplex bit values received on the HISTADR line appear at the corresponding SSMSR parallel outputs from bit gate 7 of phase B to bit gate 6 of phase C. A delayed replica of the input information to the SSMSR appears at the serial output.

2-167. SECTOR-SYLLABLE-MODULE BUFFER REGISTER. (See figure 10-30, sheet 18.) The sector-syllable-module buffer register (SSMBR) is a 17 position latch register that is loaded with information from the SSMSR. The contents of the SSMBR appear on 17 parallel outputs.

2-168. In the PRESENT mode the contents of the SSMSR are transferred into the SSMBR every phase A bit gate 3 unless a KSSMD signal is generated as follows:

1. When a computer single step operation is commanded.
2. During cycle 5 in the ML mode.
3. When a CESSMDR, CESSMBR, or CESSMSC is generated in the ML mode.

In the PAST mode the contents of the SSMSR are transferred into the SSMBR every phase B bit gate 8 when the TRS or AI3 position of the DISPLAY SELECT switch is selected.

2-169. The SSMBR is cleared as follows:

1. Every phase C bit gate 13 unless a KSSMD signal is generated.
2. By a CDRES A signal.
3. Every bit gate 7 in the PAST mode.

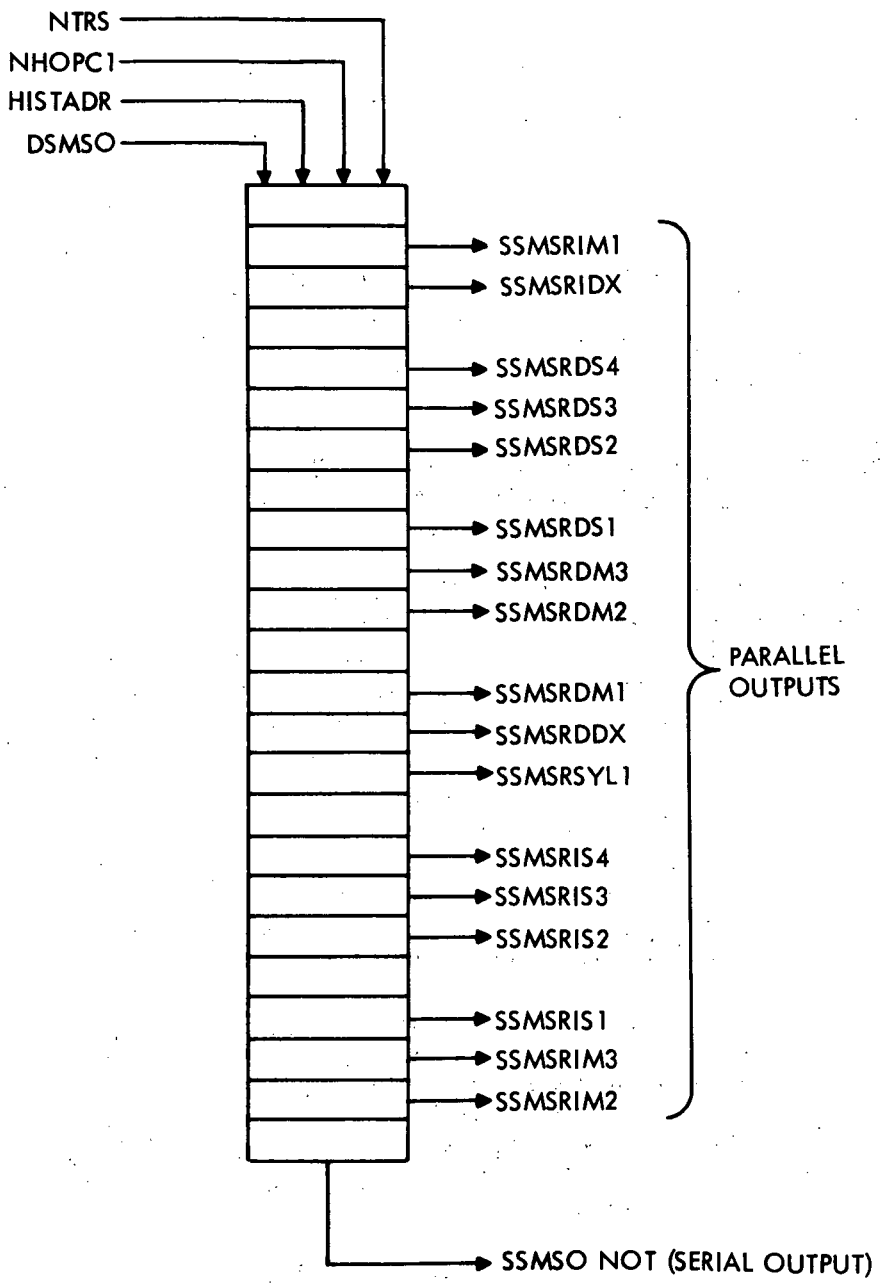


Figure 2-25. Sector-Syllable-Module Shift Register

2-170. SECTOR-SYLLABLE-MODULE DISPLAY REGISTER. (See figure 10-30, sheet 19.) The sector-syllable-module display register (SSMDR) is a 17 position latch register that is loaded with information from the SSMBR. The contents of the SSMDR appear on 13 parallel outputs and are displayed by corresponding COMPUTER display indicator lamps.

2-171. The SSMDR latches are all initially set at phase C bit gate 1 when an address compare occurs or at phase C bit gate 2 when the serializer output is selected. The SSMDR latches are then reset when the corresponding SSMBR latches are reset as follows:

1. At phase C bit gate 2 when an address compare occurs.

2. At phase C bit gate 3 when the serializer output is selected.

3. By a CDRES A signal.

2-172. ADDRESS SHIFT REGISTER. (See figure 10-30, sheet 30.) The address shift register (ADSR) receives serial information on the HISTADR or INSSO line. The ADSR also receives parallel information on the NOP1 through NOP4 and NAI through NA9 lines. Information shifting through the ADSR appears on 13 parallel outputs and one serial output. Figure 2-26 is a block diagram of the ADRSR which consists of 24 latches connected in series.

2-173. HISTADR information is gated into the ADRSR in the PAST mode when the TRS or AI3 position of the DISPLAY SELECT switch is selected. When the display serial output operation is selected INSSO information is gated into the ADRSR.

2-174. INSTRUCTION DISPLAY REGISTER. (See figure 10-30, sheet 31.) The instruction display register (INSDR) is a 13 latch register which receives the parallel inputs from the ADSR to be displayed. The contents of the INSDR is displayed: (1) from bit gate 3 to the following bit gate 2 when in data display mode and an address compare is affected; (2) from bit gate 5 to the following bit gate 4 when in the past history mode; and (3) from bit gate 12 to the following bit gate 11 when the data serial out gate is present.

2-175. INSTRUCTION ADDRESS DISPLAY REGISTER. (See figure 10-30, sheet 32.) The instruction address display register (IADR) is an eight latch register which receives parallel address information from the ADSR for display purposes. The contents of the IADR are displayed (1) during phase B from bit gate 3 to the following bit gate 2 when in the data display mode and an address compare is affected; and (2) during phase C from bit gate 2 to the following bit gate 3 while in the PAST mode.

2-176. DATA DISPLAY SHIFT REGISTER. (See figure 10-30, sheet 27.) The data display shift register (DTDR) is a 35 latch register (figure 2-27) which has 26 parallel lamp outputs (SIGN and 1 through 25) and a serial output (DTDRB25). The register is shifted when data and a shift register clock pulse (DTDRCP1, 2, 3, or 4) are present. DTDRB25 goes to a comparator where it is compared with 2BDDTSO. DTDRB25 is also gated by a compare AI3 (CAI3) level into I/O register 1. The data inputs gated into the DTDR (figure 10-30, sheet 26) are as follows:

1. History delay line serial data is gated into the DTDR by corresponding DISPLAY SELECT rotary switch selection while in the PAST mode.

2. Computer serial data is gated into the DTDR by corresponding DISPLAY SELECT rotary switch selection while not in the PAST mode.

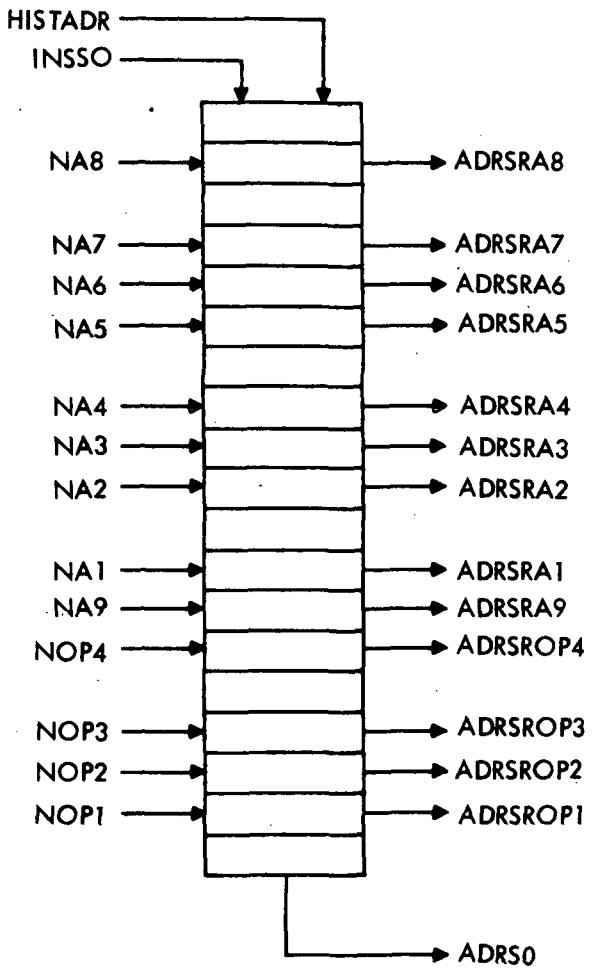


Figure 2-26. Address Shift Register

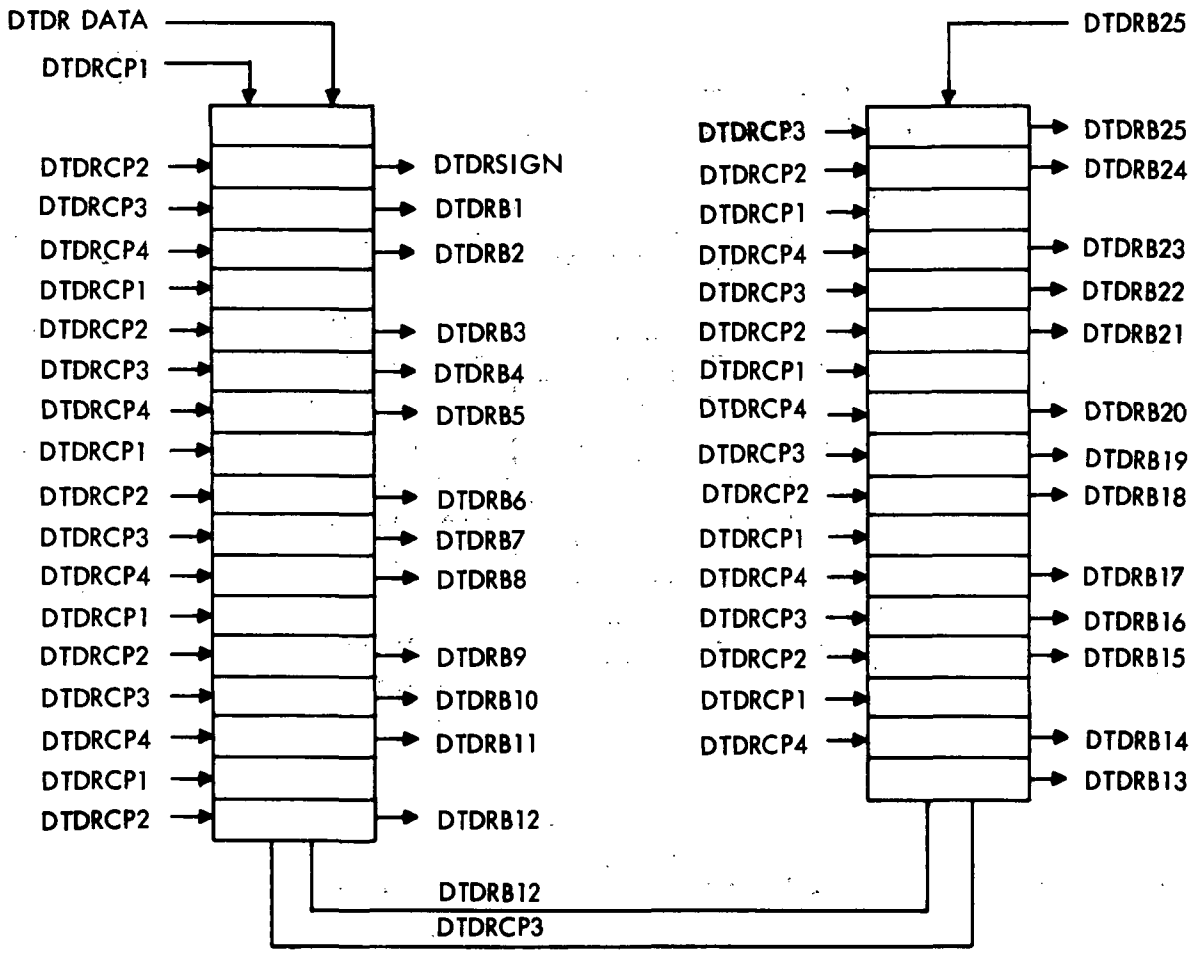


Figure 2-27. Data Display Shift Register

3. TRS or AI3 data is gated into the DTDR by corresponding DISPLAY SELECT rotary switch selection while not in the ML mode and not in the PAST mode. When in the ML mode and not in the PAST mode, TRS and AI3 data is gated into the DTDR by a compare TRS or AI3 level.

4. Switch selector counter, minor loop counter, real time counter and self-check real time counter data is gated into the DTDR by corresponding DISPLAY SELECT rotary switch selection.

5. Spare probe data is gated into the DTDR when not in the PAST mode.

6. History AI3 (instruction address-data) is gated into the DTDR during the PAST mode when the DISPLAY SELECT rotary switch is positioned accordingly.

7. 2BDDTSO data is gated into the DTDR when gating level DSO is present.

In the test program mode, the select serial data gating level is a programmed discrete. (See figure 10-30, sheet 24.)

2-177. MULTIPLY-DIVIDE COUNTER. (Figure 10-30, sheet 25.) The multiply-divide counter is an eight latch, two phase counter (stepped every two phases). The multiply-divide counter outputs form a gating level with the WORD rotary switch positions during a multiply or divide instruction. The gating level allows the data display shift clocks to be present during multiply or divide so that the selected partial product, quotient or result from history is displayed in the data display shift register. In self-check the counter is used to allow recirculation of I/O register 2, during multiply or divide for 14 (two phase) cycles. This is the time required to develop the final product, quotient or result. Counter operation is initiated by a reset to zero at clock pulse X, bit gate 13, phase A, during multiply or divide; the counter is stepped every two phases under control of three latches.

2-178. ADDRESS COMPARE. (See figure 10-30, sheet 28.) A data display can be affected only during an address compare. An address compare level is generated when the address compare latch is set. This latch is set at phase B, bit gate 1 and clock pulse Y when any one of the following conditions prevail:

1. When an instruction address compare operation is in progress and a comparison of sector, syllable, module and address information is made, providing the computer single step function is not used and a display reset is not affected.

2. When a data address compare operation is in progress and a comparison of data address information is made, providing the computer single step function is not used and a display reset is not affected.

3. When in CST mode and a gate advance computer 1 step signal (GAC1SS) is present. The gate is generated by pressing the ADVANCE push-button. A computer single step skip (CST SKIP) can also cause an address compare. A CST SKIP is generated when new address information is manually inserted. This allows the program to advance to the new address before an address compare is generated.

4. When the gate, past history mode, multiply-divide (GPHMMD) is present. (See figure 10-30, sheet 24.)

5. When the past history gate (CPHG) is present.

6. During Memory load and CYC3 or CYC4.

2-179. DATA DISPLAY CONTROLS. The data display controls generate eight signals; PHMA, PHMA NOT, DISSIN, DISRPT, CDRESA, CDRESA NOT, IA COMP and DA COMP. These signals are used to control data display in ML and DD modes, and are generated as follows:

1. Past history mode (PHMA) and past history mode not (PHMA NOT) are outputs of a binary counter. (See figure 10-30, sheet 26.) The counter is complemented each time the PAST/PRESENT switch is pressed while in the CST mode. When not in CST mode, PHMA NOT is forced, which means that present information can be gated into the data display register. PHM is forced in the test program mode with programmed discretes. This allows display data to be shifted to the PTC.

2. Display single (DISSIN) and display repeat (DISRPT) are outputs of a binary counter. (See figure 10-30, sheet 15.) The counter is complemented each time the SINGLE/REPEAT switch is pressed. When in the SINGLE mode, data will be displayed on the first address compare. If the COMPTR DISPLAY RESET switch is pressed while in the SINGLE mode, data will be displayed on the next address compare. In the repeat mode, a new display is generated with each address compare.

3. Computer display reset (CDRESA) is generated by setting a latch. The latch is set manually when the tape reader is not running and when the COMPTR DISPLAY RESET switch (SW CDRES) is pressed while in the DISPRT mode. The latch is set automatically if the self-check "1" function is not activated, during AUTO mode, bit gate 10 and CYC5 if either no compare error (CE) exists or if an address compare is affected. The CDRESA latch is reset to CDRESA NOT at phase A, bit gate 1 time.

4. A data address compare (DA COMP) or instruction address compare (IA COMP) level is generated by actuating the DATA/INS switch. This drops and picks the IA COMP relay which switches a ground level through the relay contacts during the data display mode. This is the DA COMP or IA COMP which allows a data display on either a data address or instruction address compare.

2-180. INTERFACE EXERCISER.

2-181. INPUT/OUTPUT REGISTERS.

2-182. The LVDCME contains two input/output registers: (1) the PIO Memory Register; and (2) the PIO Accumulator Register. These registers provide temporary storage for data transmitted to or from the LVDCME as a result of certain PIO and CIO instructions.

2-183. PIO MEMORY REGISTER. The PIO memory register is a 26-bit shift register that may be loaded in any of the following ways:

1. Serially with AI3 data from the computer.

2. Serially with TRS data from the computer.

3. Serially with PTC accumulator data.

4. Serially with recirculated data.

5. In parallel with data from the I/O REG switches.

6. Serially with data from the DTDR.

2-184. Shifting in the PIO memory register is controlled by a circuit that produces shift clocks SM D, SM A, SM B and SM C that correspond respectively with clocks W, X, Y and Z during shifting operations. Shift clocks are produced whenever serial data is to be read into or out of the PIO memory register.

2-185. Computer AI3 data is loaded into the PIO memory register when PIO bit A8 is a "0" and bit A1 or A2 is a "0". TRS data is loaded when address bit A8 is a "1" and bit A1 or A2 is a "0". PTC accumulator data is loaded as a result of a CIO 002 instruction. Recirculated data is loaded when a read PIO (A1 and A2 are "1's") or CIO 001 is used. Recirculation provides for nondestructive readout of the register.

2-186. Any latch in the PIO memory register may be set by pressing the corresponding I/O REG switch. All latches are simultaneously reset when the PIO RESET switch is pressed. When the PIO RESET switch is pressed, the sign latch is reset and shift clocks are produced. The "0" in the sign position shifts down to the last latch, and since no new data can get into the sign latch while the PIO RESET switch is depressed, the register is cleared.

2-187. During memory verification, the PIO memory register is used to store the serial contents of the DTDR. This permits a comparison between serial data received from the computer (shown in the DATA lamps) and the serial data sent to the computer (shown in the I/O REG #1 lamps). DTDR data is loaded only during cycle 4 of a memory verification operation.

2-188. PIO ACCUMULATOR REGISTER. The PIO accumulator register is a 26-bit shift register which may be used as two separate 13-bit shift registers. When the PIO accumulator is split into two registers, the 13 low-order latches and a serial adder form the switch selector counter (SSC); the 13 high-order latches and a serial adder form the minor loop counter (MLC). In the test program mode, the two halves of the PIO accumulator register are joined together to form a single 26-bit register.

2-189. As a 26-bit register, the PIO accumulator register may be loaded with PTC accumulator data, recirculated data, or parallel data from the I/O REG switches. PTC accumulator data is loaded as a result of a CIO 006 instruction. When a CIO 006 instruction is not present, recirculated data (PIO ABD) is loaded. During self-check, SSC data, which is advanced one bit time from PIO ABD, is re-circulated.

2-190. Shifting in the PIO accumulator register is controlled by a circuit that produces shift clocks SA D, SA A, SA B and SA C that correspond respectively with clocks W, X, Y and Z during shifting operations. Shift clocks are produced whenever serial data is to be read into or out of the register.

2-191. When the LVDCME is in the operational program mode, bits SIGN through 12 of the PIO accumulator register form the MLC, and bits 13 through 25 from the SSC. Data does not shift between the two sections which now operate as two separate binary counters — the MLC and the SSC.

2-192. Minor Loop Counter. The MLC may be loaded with serial data from any of the following sources:

1. AI3 data from the computer.
2. TRS data from the computer.
3. PTC accumulator data.

2-193. Computer AI3 data is loaded into the MLC when PIO address A8 NOT, A7 NOT, A6, A5, A4, A3, A2, A1 NOT is used. PIO address A8, A7 NOT, A6, A5, A4, A3, A2, A1 NOT causes computer TRS data to be loaded. CIO 006 causes PTC accumulator data to be loaded. The MLC may be manually loaded with data from I/O REG #2 switches SIGN through 12.

2-194. When no data is being loaded into the MLC, its count is re-circulated. A serial subtractor subtracts one from the MLC count once every six program cycles. Each time the MLC count becomes zero, an interrupt is generated and sent to the computer and PTC.

2-195. A CIO 021 instruction causes the MLC count to be read into the PTC accumulator. The MLC count is displayed in I/O REG #2 lamps SIGN through 12.

2-196. Switch Selector Counter. The SSC may be loaded with serial data from any of the following sources:

1. AI3 data from the computer.

2. TRS data from the computer.

3. PTC accumulator data.

2-197. Computer AI3 data is loaded into the SSC when PIO address A8 NOT, A7, A6, A5, A4 NOT, A3 NOT, A2, A1 NOT is used. PIO address A8, A7, A6, A5, A4 NOT, A3 NOT, A2, A1 NOT causes computer TRS data to be loaded. CIO 016 causes PTC accumulator data to be loaded. The SSC may be manually loaded with data from I/O REG #2 switches 13 through 25.

2-198. When no data is being loaded into the SSC, its count is re-circulated. A serial subtractor subtracts one from the count once every six program cycles. The first time the SSC count reaches zero, an interrupt is generated and sent to the computer and PTC. The SSC must be reloaded before another interrupt can be generated by the SSC.

2-199. A CIO 025 instruction causes the SSC count to be read into the PTC accumulator. The SSC count is displayed in I/O REG #2 lamps 13 through 25.

2-200. DISAGREEMENT REGISTER.

2-201. The disagreement register is a 13-bit latch register that receives its inputs from the thirteen computer disagreement lines (EP1 through EP13). These inputs are applied to latches in the disagreement register whose outputs light DISAGREEMENT lamps on the INTERFACE EXERCISER panel. When a "1" appears on a computer disagreement line, the corresponding latch sets, and the corresponding lamp lights.

2-202. Once an error is sensed, the corresponding latch remains set until the entire register is reset. The disagreement register may be reset manually with the ERROR RESET pushbutton or automatically with a CIO 026 or a PIO code in which address bits A1, A2 and A9 are "0's" and A5 is a "1".

2-203. INTERFACE EXERCISER ADDRESS REGISTER.

2-204. The interface exerciser address register is a nine-bit latch register that is loaded with PIO address information during a PIO operation. Outputs from this address register are applied to lamp drivers that light the ADDRESS lamps on the INTERFACE

EXERCISER panel. These lamps indicate the states of address lines NA1 through NA9. All latches in the interface exerciser address register are simultaneously reset before a new PIO address is loaded. The register is also reset when the PIO RESET pushbutton is pressed.

2-205. DISAGREEMENT SERIALIZER.

2-206. The outputs from the disagreement register latches, EAM, EBM and the OR'd channel 1, 2 and 3 errors (EA1, EA2 and EA3), are applied to a disagreement serializer. Errors are serialized as follows:

Phase B		Phase C	
*Bit Gate	Error	*Bit Gate	Error
1		1	EP3
2		2	EP4
3		3	EP5
4		4	EP6
5		5	EP7
6		6	EP8
7		7	EP9
8		8	EP10
9		9	EP11
10	EA1	10	EP12
11	EA2	11	EP13
12	EA3	12	EAM
13	EP1	13	EBM
14	EP2	14	TLC

*From Y time of designated bit to Y time of following bit.

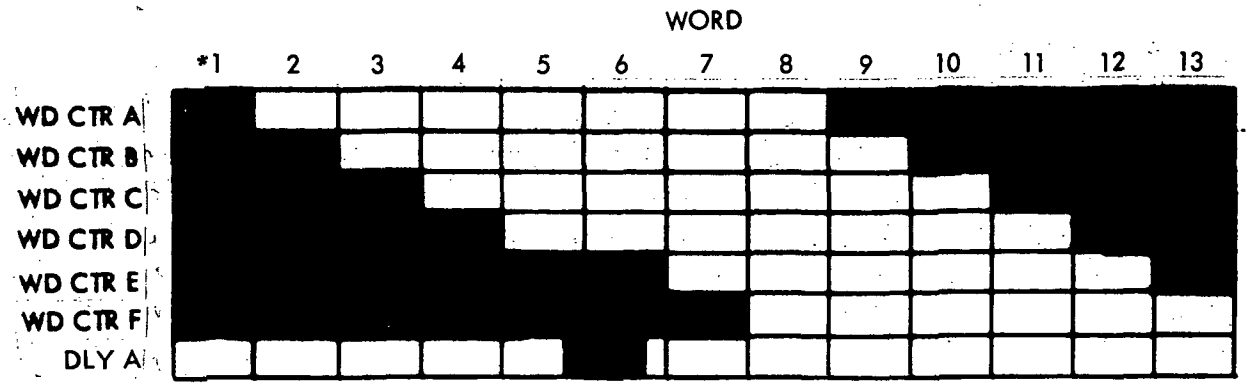
2-207. REAL TIME COUNTER.

2-208. The real time counter (RTC) consists of a serial adder and a delay circuit. The output of the delay circuit is recirculated in the delay circuit through the serial adder. Once every three instruction cycles, the instruction cycle counter (paragraph 2-212) generates a bit which is added (in the serial adder) to the recirculated real-time count. The real time count is therefore increased by one every three instruction cycles.

2-209. Updating of the RTC is inhibited during a CST or HLT operation. During these operations the real-time count is recirculated and remains unchanged. The RTC may be read into the PTC with a CIO 015 instruction.

2-210. AI3/TRS PAST HISTORY WORD COUNTER.

2-11. The AI3/TRS past history word counter consists of a six-bit shift register and a shift control circuit. The shift control circuit produces shifting gates HWC ODD and HWC EVEN. The shifting gates are applied to the shift register which produces outputs as shown on figure 2-28. The output configuration at word 5 is maintained during word 6



Note: DLY A SET FROM BG9, PHASE C, WORD 5
TILL BG3, PHASE C, WORD 6.
*RESET CONDITION FOR COUNTER

Figure 2-28. AI3/TRS Past History Word Counter Outputs

by a circuit that produces DLY A, which inhibits the stepping of the shift control circuit for one word time. Word times are specified by AND'ing outputs as follows:

Word	Specified by
1	WD CTR F and WD CTR A
2	$\overline{\text{WD CTR A}}$ and WD CTR B
3	$\overline{\text{WD CTR B}}$ and WD CTR C
4	$\overline{\text{WD CTR C}}$ and WD CTR D
5	$\overline{\text{WD CTR D}}$ and WD CTR E and $\overline{\text{DLY A}}$
6	$\overline{\text{WD CTR D}}$ and WD CTR E and DLY A
7	$\overline{\text{WD CTR E}}$ and WD CTR F
8	WD CTR F and $\overline{\text{WD CTR A}}$
9	WD CTR A and $\overline{\text{WD CTR B}}$
10	WD CTR B and $\overline{\text{WD CTR C}}$
11	WD CTR C and $\overline{\text{WD CTR D}}$

Word	Specified by
12	WD CTR D and $\overline{\text{WD CTR E}}$
13	WD CTR E and $\overline{\text{WD CTR F}}$

2-212. INSTRUCTION CYCLE COUNTER.

2-213. The instruction cycle counter consists of a six-bit shift register and a shift control circuit. The shift control circuit produces shifting gates PHMDC OD and PHMDC EV. These shifting gates are applied to the shift register which produces outputs as shown on figures 2-29 and 2-30 in the operational and test program mode respectively.

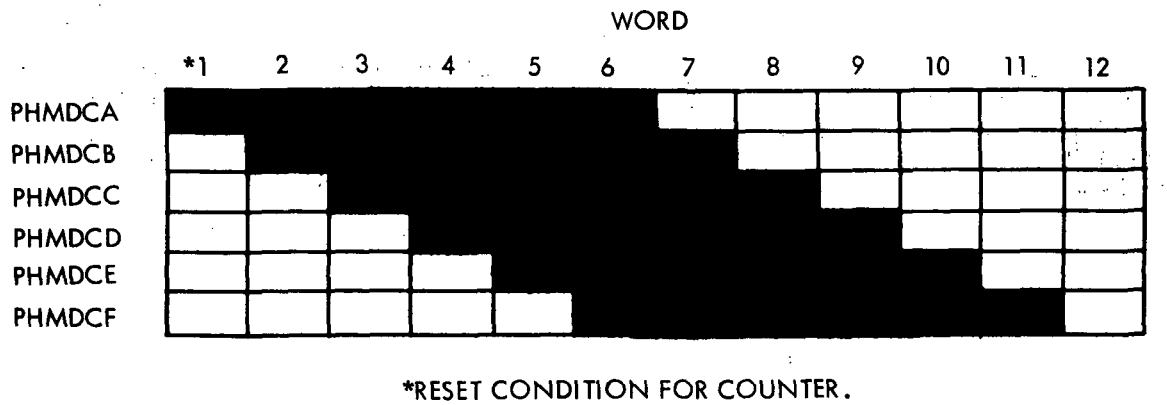


Figure 2-29. Instruction Word Counter Outputs, Operational Program Mode

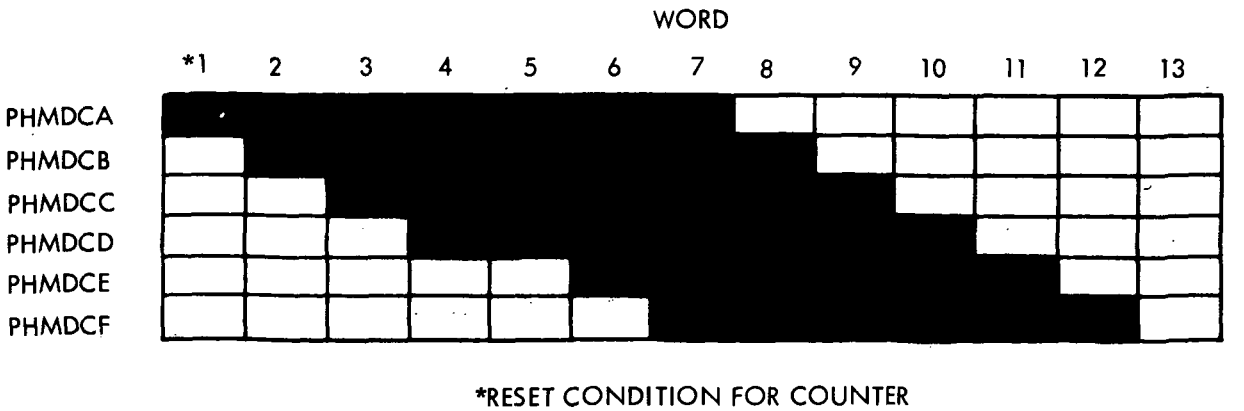


Figure 2-30. Instruction Word Counter Outputs, Test Program Mode

2-214. In the operational program mode, shift register outputs PHMDCA, PHMDCB, and PHMDCE and their inverses are applied to a circuit that produces outputs COUNT 3 and COUNT 6 every three and six instruction cycles, respectively. COUNT 3 occurs during words 1, 4, 7, and 10, and is used to update the real-time count. COUNT 6 occurs during words 1 and 7 and is used to update the minor loop count and the switch selector count.

2-215. In the test program mode, the instruction cycle counter counts 13 instruction cycles. The output configuration (figure 2-30) at word 4 is maintained during word 5 by a circuit that produces PHMDC INH NOT that inhibits the stepping of the shift control circuit for one word time.

2-216. The AND'ed outputs from the shift register are used to control recirculation of ADR, MR1, MD7 and PRO data in the history delay lines. Outputs are also used to synchronize the multiply/divide past history word counter.

2-217. SELF CHECK.

2-218. The LVDCME incorporates a self-check feature which checks the operation of a major portion of the LVDCME. This is accomplished by connecting the interface cable connectors, which normally go to the computer, back to special self-check connector receptacles on the LVDCME. The LVDCME self-check interconnections are listed in figure 2-31.

Cable Part No. *	From	To
6900052	02A3J22	02A3J20
6900053	J18	J17
6900054	J15 and J19	J16
6900055	J14	J13
6900056	J5	J8
6900057	02A3J6	02A3J9
6900058	J7	J10
6900059	J11	J12
6900073	J21	J23
6900085	01A11J32	01A11J25
6900086	J31	J26
6900087	J30	J27

*Jumper plug 6900074 must be connected to 01A11J29.

Figure 2-31. LVDCME Self-Check Cable Interconnection List

2-219. When the LVDCME is operated in the self-check mode, inputs that are normally provided by the computer are simulated by circuits within the LVDCME. These circuits, called simulators, are as follows:

a. Timing simulators (clock generator, bit gate generator, phase generator and buffer oscillator).

b. OP code simulator.

c. Address simulator.

d. Disagreement error simulator.

e. Error simulators (TLC, EAM and EBM).

f. BRA-BRB simulator.

g. CIO codes and discretes simulators.

h. Serial data simulators (SCPRO, SCHOPC1, SCAI3, SCTRA, SCMD7, SCMR1, SCASRTC, SCPIO and SCPTCAI3).

2-220. Some computer signals are simulated (during self-check) by LVDCME circuits that are normally used for computer tests. For instance, HOPC1 data comes from the DTSO output of the serializer. The operations of these circuits have been previously described. However, their special roles during self-check are described in subsequent paragraphs.

2-221. The outputs of the self-check simulators correspond to the translated and inverted computer signals. For instance, SCOP1 (self-check OP1) corresponds to NOP1 which is a translated, inverted and voted computer signal. Computer signals that appear in TMR form are simulated by producing the self-check signal in triplicate.

2-222. TIMING SIMULATORS. (See figure 10-30, sheet 35.) Self-check timing (figure 2-32) is initiated by a crystal controlled oscillator. The oscillator generates a square wave signal (0 VDC to -6 VDC) whose switching rate is 2.048 mc. The oscillator output alternately causes the setting and resetting of a trigger. The trigger set output is an input to a second trigger, and the reset output is an input to a third trigger. The outputs of these two triggers are inverted, and on negative transition cause firing of four single shots. The single shots produce negative pulses 0.4 usec in duration. These negative pulses are the self-check clocks.

2-223. Clock voter errors (fail to "1" and fail to "0") can be induced with the CLOCK and PHASE rotary switches as shown in figure 2-33. When the CLOCK and PHASE rotary switches are in the NONE position, proper generation of computer simulated W, X, Y and Z clocks in triplicate is automatic and continuous.

2-224. SELF-CHECK BIT GENERATOR. (Figure 10-30, sheet 35.) The self-check bit generator consists of a shift register control circuit, a seven bit shift register and a bit decoding circuit.

2-225. The shift register control circuit is composed of a pair of latches interconnected to form a binary counter. The counter alternately produces a self-check odd (SCODD) and a self-check even (SCEVEN) control level at W clock times as shown on part A of figure 2-34.

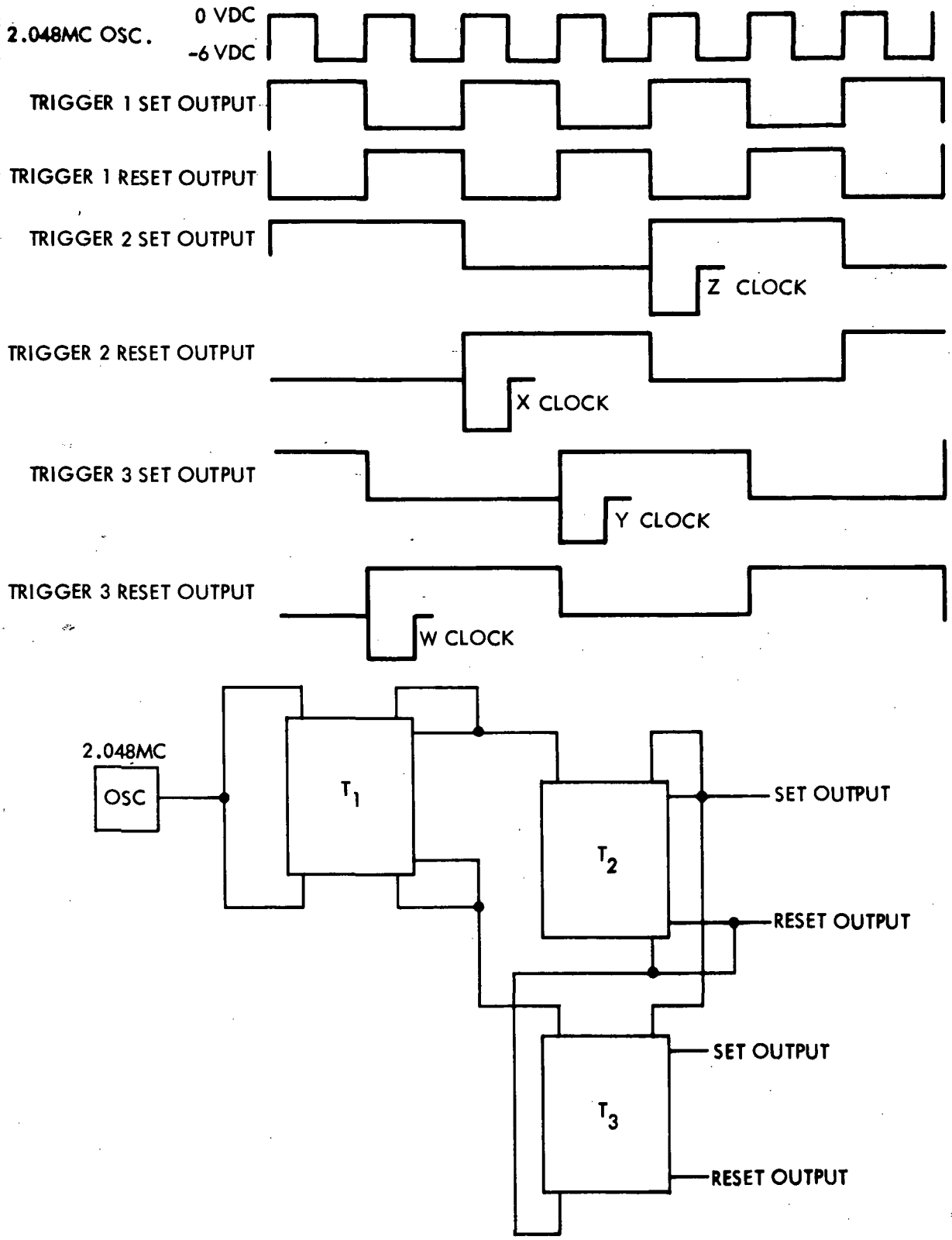


Figure 2-32. Self-Check Clock Generation

Signal	Switch Position			
	Fail To "1"		Fail To "0"	
	CLOCK	PHASE	CLOCK	PHASE
SCA1W	5	1	6	1
SCA2W	5	2	6	2
SCA3W	5	3	6	3
SCA1X	5	4	6	4
SCA2X	5	5	6	5
SCA3X	5	6	6	6
SCA1Y	5	7	6	7
SCA2Y	5	8	6	8
SCA3Y	5	9	6	9
SCA1Z	5	10	6	10
SCA2Z	5	11	6	11
SCA3Z	5	12	6	12
SCB01	7	—	8	—
SCB02	9	—	10	—
SCB03	11	—	12	—

Figure 2-33. Clock and BO Error Simulation

2-226. The SCODD and SCEVEN levels control the shifting of a seven bit shift register and prevent the contents of the register from rippling through when the register is stepped. Seven outputs (SCG1 through SCG7) change states as shown on part B of figure 2-34.

2-227. The self-check bit decoder is a matrix that generates self-check bit gates from the seven bit shift register configuration. The SCG5 (self-check gate 5) output of the shift register is developed into three lines of computer simulated G5 NOT. A G5 voter error (fail to "1") can be induced in self-check by forcing control level(s) CA1G5 and/or CA2G5 and/or CA3G5 to ZERO. This is accomplished during CYC3 and self-check phase C when tape addresses 6 NOT, 5 NOT, 4 NOT, 3, 2 NOT and 1 are programmed. The channel in which the error is induced is determined by TRDM1, TRDM2 and TRDM3 of the tape reader register.

2-228. SELF-CHECK PHASE GENERATION. The self-check phase generator consists of a sync circuit and a four latch cyclic counter. (See figure 2-35.)

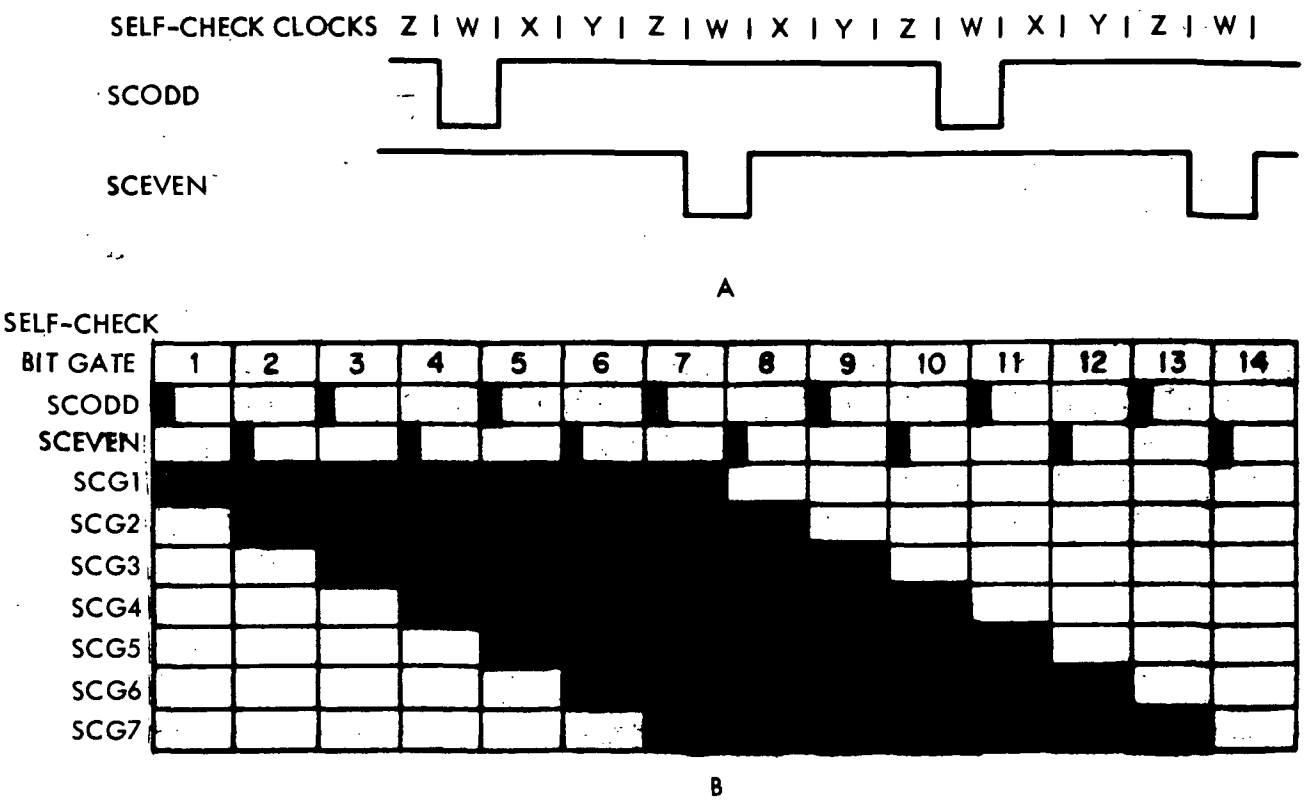


Figure 2-34. Self-Check Bit Generator Control and Shift Register Timing

2-229. The sync circuit produces a phase generator sync signal (APG) when the shift register counter returns to SCG1 at SCODD time.

2-230. The cyclic counter produces three self-check phases — SCPA, SCPB and SCPC. The counter is set up for developing the next phase in the cycle when the shift register counter counts to SCG4. The next phase is then produced with the sync level (APG).

2-231. A phase B voter error (production of a phase B at phase C time) can be induced when the shift register counter counts to SCG5 providing the tape address decoded is TAADR6 NOT, 5 NOT, 4 NOT, 3, 2 NOT, and 1. The channel in which the error is induced is determined by TRDS1, TRDS2 and TRDS3.

2-232. SELF-CHECK BUFFER OSCILLATOR (SCBO1-3). The computer buffer oscillator signal is simulated in the LVDCME during self-check by inverting the output of the 2.048 mc oscillator. The NOT output of the inverter is distributed to three AND circuits, translated, sent out of the LVDCME and returned on three lines via a self-check cable. (See figure 10-30, sheet 25.)

2-233. Buffer oscillator errors (fail to "1" and fail to "0") can be induced with the CLOCK rotary switch as shown in figure 2-33. When the CLOCK rotary switch is in the NONE position, translated buffer oscillator pulses are automatic and continuous.

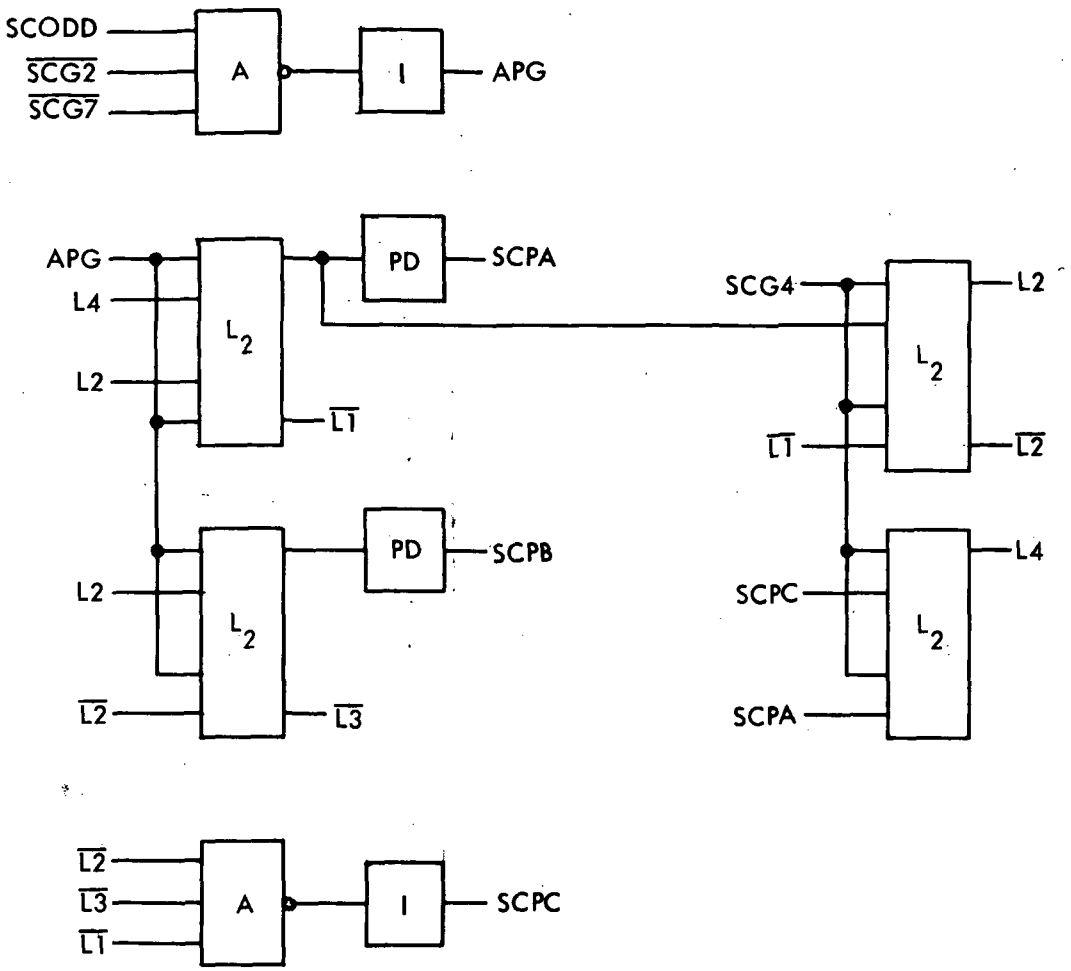


Figure 2-35. Self-Check Phase Generation

2-234. WORD COUNTER. The word counter is a thirteen trigger counter register which counts computer cycles in MEM SIM mode and tape words in the ML mode. The counter is stepped by means of stepping pulses. Each trigger in the chain is complemented when its input goes from "1" to "0". The counter can be stepped as follows: (See figure 10-30, sheet 33.)

a. Manually: When the ADV CTR switch is selected and the tape reader is not running, pressing a TAPE ADDRESS area switch (SWTRCH01 through 05) generates a stepping pulse which advances the word counter by one, within the limits of the pushbutton/lamp being actuated. The counter does not step into a count displayed by another pushbutton/lamp except by pressing that pushbutton/lamp.

b. Automatically:

1. By a word counter stepping pulse while in self-check, MEM SIM mode during each bit gate seven, phase A, and providing that the CST function is not used. In MEM SIM,

a control level (CTR GATE) is provided which allows the counter to be advanced through its entire range. A decoded word counter gives OP code and address information which is part of an inherent program in MEM SIM. The OP codes are decoded from the first five triggers in the word counter. Therefore, every 37_8 cycles, the OP code arrangement is repeated. The instruction addresses are decoded from the first eight bits of the word counter. Therefore, every 377_8 cycles the instruction addresses are repeated.

2. During the ML mode when the tape reader is running, TRCP1 causes the word counter to be advanced each time a sequence bit is sensed. The SEQ BIT causes a control level (CTR GATE) which allows the word counter to be advanced through its entire range.

2-235. OP CODE SIMULATORS (Figure 10-30, sheets 33 and 34). Self-check operation codes in memory load mode are developed from decoded tape reader operation bits (TROP1-4) or from decoded tape address bits (TAADR1-5). During MEM SIM mode, self-check operation codes are decoded from word counter (2^0 through 2^4) bits. In each case, a self-check level (SCOP) controls all operation codes generated. (See timing chart on figure 2-36.)

2-236. A special case simulates a computer function during single step mode. When in single step, the self-check operation code generated is the transfer nonzero (TNZ) instruction (SCOP3=1).

2-237. A voter error, that is, the forcing of all self-check operation code bits in a channel to "1" (fail to a "1"), can be induced with tape address bits 5 and 6 (TAADR5 and TAADR6). The channel in which the error is induced is determined by tape reader operand address bits 1 through 3 (TROA1-3).

2-238. ADDRESS SIMULATORS (Figure 10-30, sheets 33 and 34). Self-check address bits are developed in ML from tape reader operand address bits when self-check level SCOA is present, or in MEM SIM from word counter bits when self-check level SCIA is present, or in MEM SIM from word counter bits when self-check level SCIA is present. (See timing chart on figure 2-36.) A tape reader operand address bit (TROA1-9) becomes the corresponding computer simulated address bit, whereas the word counter counts (2^0 through 2^7) become computer simulated address bits one through eight respectively. 2^0 becomes SCA1, 2^1 becomes SCA2, etc.

2-239. A voter error, that is, the forcing of all self-check operation code bits in a channel to "1" (fail to a "1"), can be induced during cycle 3 when tape address bits TAADR4, TAADR5 NOT, TAADR6 NOT, and INV ERR are decoded. The channel in which the error is induced is determined by tape address bits 1 through 3 (TAADR1-3).

2-240. DISAGREEMENT ERRORS SIMULATION. Computer voter disagreement errors (SCEP1-13) are simulated with the coincidence of a self-check level (signal called HELP) and specific tape reader register bits. The HELP signal is a tape address decode (TAADR1, 2, 3 NOT, 4 NOT, 5 NOT, and 6) at self-check clock Y, self-check bit gate 4, self-check phase A and cycle 3 time. The tape reader register bits used to determine the errors produced are as follows: TROA5 = SCEP1, TROA4 = SCEP2, TROA3 = SCEP3, TROA2 = SCEP4, TROA1 = SCEP5, TRDS1 = SCEP6, TRDS2 = SCEP7, TRDS3 = SCEP8, TRDS4 = SCEP9, TROA9 = SCEP10, TROA8 = SCEP11, TROA7 = SCEP12, and TROA6 = SCEP13.

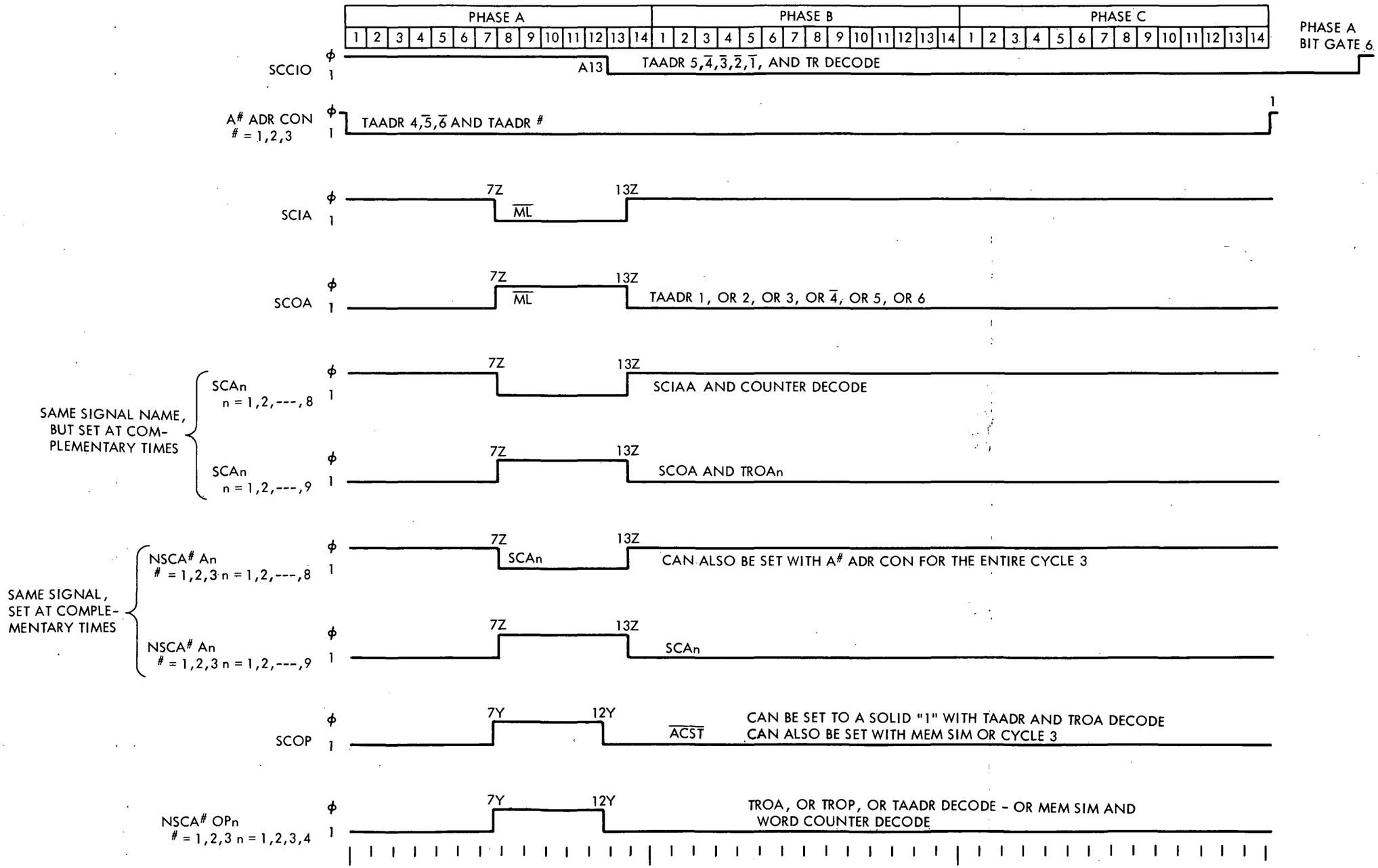


Figure 2-36. Self-Check Operation Code and Address Timing

2-241. ERROR SIMULATORS. Memory module errors (EAM, EBM and TLC) are simulated in self-check with the coincidence of a self-check level signal (LEMMON 1) and specific tape reader register bits. The LEMMON 1 signal is a tape address decode (TAADR1 NOT, 2 NOT, 3, 4 NOT, 5 NOT and 6 NOT). The channel in which the error is induced is determined by tape reader operand address bits (TROA1-3 for EAM-channels 1-3, TROA4-6 for EBM-channels 1-3 and TROA7-9 for TLC-channels 1-3).

2-242. SELF-CHECK BUFFER REGISTER A AND B BIT 14 PARITY (SCBRA14P AND SCBRB14P). Buffer register A and B, bit 14 parities are simulated by the LVDCME as follows (see figure 10-30, sheet 36):

1. When a tape reader data address parity bit (TRDA-PB) is generated during self-check phase A and bit gate 11. It is during this time that a latch is set which allows SCBRA14P and SCBRB14P to be generated.

2. When a store operation is decoded. SCBRA14P and SCBRB14P are generated either (1) when a tape reader syllable "1" parity bit (TRSYL1 PB) is generated during self-check phase A and bit gate 3 through 6, or (2) when a tape reader syllable "0" parity bit (TRSYL0 PB) is generated during phase B or phase C.

3. When a non-store operation is decoded. SCBRA14P and SCBRB14P are generated either (1) when tape reader syllable "0" parity bit is generated during phase B, bit gate 3 through 6, or (2) when tape reader syllable "1" parity bit is generated during phase C, bit gate 3 through 6.

2-243. SCBRA14P can be failed to a constant "1" either during self-check phase B when LEMMON 1 and TRDS1 are programmed or during self-check phase C when LEMMON 1 and TRDS2 are programmed.

2-244. SCBRB14P can be failed to a constant "1" either during self-check phase B when LEMMON 1 and TRDS3 are programmed or during self-check phase C when LEMMON 1 and TRDS4 are programmed.

2-245. LEMMON 1, a self-check control level, is a tape address decode of TAADR1 NOT, 2, 3, 4 NOT, 5 NOT and 6 NOT,

2-246. CIO CODES AND DISCRETES SIMULATORS. Self-check CIO codes in ascending order are developed from tape reader register bits, SIGN and 1 through 25, and TRDS1 through 4 AND'ed with a self-check gate (SCGCIO). (See figure 10-30, sheet 34.) SCGCIO is a latch output, and is present when tape address bits TAADR1 NOT, 2 NOT, 3 NOT, 4 NOT and 5 are decoded during cycle 3, bit gate 13. The gate is removed every phase A, bit gate 6. (See timing chart on figure 2-36.) CIO codes may also be generated by a TIME SEL when conditioned by an interrupt 13. This feature is for self-check of the past history delay line read to the PTC.

2-247. The self-check discretes are developed from corresponding tape reader address bits and a control gate (GATE SC DISCR). GATE SC DISCR is present when tape address bits, TAADR1 NOT, 2 NOT, 3 NOT, 4 NOT and 5 are decoded.

2-248. *SERIAL DATA SIMULATORS. (Figure 2-37)*

2-249. SELF-CHECK SIMULATION OF PRO. (See figure 10-30, sheet 6 and figure 2-38.) The tape reader serializer information used normally to generate data to the computer on the DIN line (see paragraphs 2-156 and 2-157) simulates three lines of PRO during self-check. The sector-syllable-module and instruction serializer information simulates PRO during cycle 2. The data serializer simulates PRO during cycle 3.

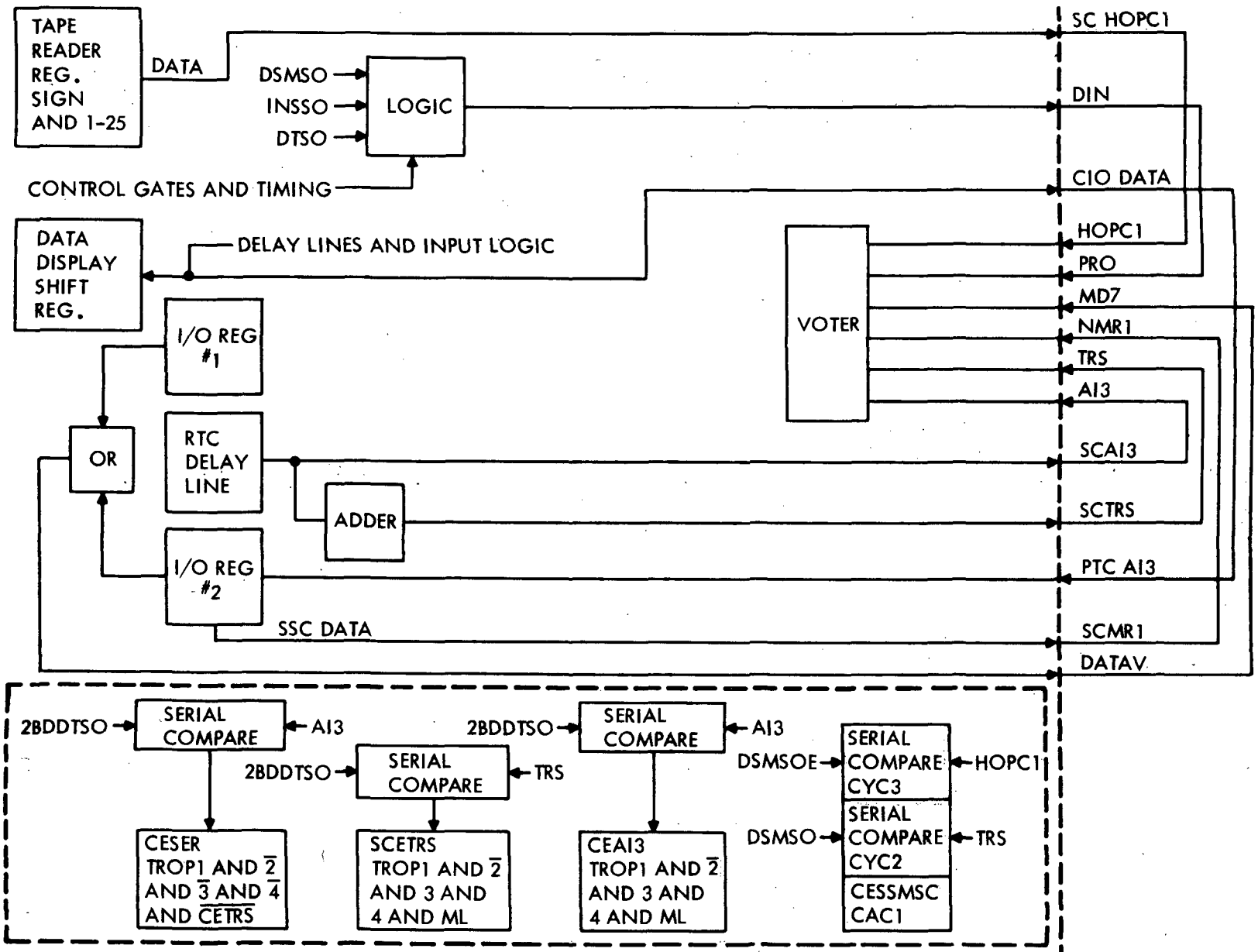


Figure 2-37. Serial Data Simulation and Self-Check Serial Compare Errors

2-250. A voter error (fail to "1") is induced into any channel (A1, or A2, or A3) when a corresponding control level CA1, or CA2, or CA3 is generated. The levels are generated during self-check bit gate 6 through bit gate 11 of self-check phase C, cycle 3 when tape address bits TAADR4 and TAADR5 NOT are decoded. The channel in which an error is induced is determined by corresponding tape address bits 1 through 3 (TAADR1-3).

2-251. SELF-CHECK SIMULATION OF HOPC1. (See figure 2-39 and figure 10-30, sheet 16.) The tape reader data serializer simulates HOPC1 during phase B and phase C. The two bits (needed during EXM-execute-modify instruction) used to simulate HOPC1 during phase A are from the instruction serializer.

2-252. A voter error (fail to "1") is induced into any channel (A1, or A2, or A3) when a corresponding control level CA1DT, or CA2DT or CA3DT is generated. These levels are generated during self-check bit gate 6 through 11 of self-check phase B, cycle 3, when tape address bits TAADR4 and TAADR5 NOT are decoded. The channel in which an error is induced is determined by corresponding tape address bits 1 through 3 (TAADR1-3). A voter error can also be induced in a channel by forcing the other two channels to a "1" with respective control levels (CA1DT, CA2DT and CA3DT) and programming a TROP3.

2-253. SELF-CHECK SIMULATION OF AI3 AND TRS. (See figure 2-40 and figure 10-30, sheet 37.) AI3 and TRS are simulated by gating, shifting and recirculating information into an unused channel of the real-time counter delay line (RTC DLY). PRO information is gated into RTC DLY when the self-check load latch (SCLOAD) is set. SCLOAD is a "1" during CYC2, phase B when address bits 8 and 9 (NA8 and NA9) are programmed. At this time, SSM and INST serializer information is gated into the RTC DLY. SCLOAD is also a "1" during CYC3, phase B when NA7 and NA9 are programmed. At this time, DATA serializer information is gated into RTC DLY. All information is delayed through RTC DLY for a period equal to 2 phases and 13 bits (80.1 usecs). The information is clocked through a latch at clock pulse Y. The information at this point is called transfer register and accumulator simulated information (TASIM). TASIM is delayed for a duration of three clock pulses through a latch. The output of the latch is self-check AI3 (SCAI3).

2-254. In MEM SIM an ADD latch is set at bit gate 2, clock pulse Y, which sets up an "add 1" condition to TASIM. The information obtained as a result of an "add 1" to TASIM is called DATA. DATA is delayed one bit through two latches and becomes SCTRS.

2-255. In ML mode, the ADD latch is reset. There is therefore no addition to TASIM. The information becomes self-check TRS (SCTRS) after a one-bit delay period.

2-256. AI3 and TRS are simulated from shifted SCTRS information when the self-check shift latch (SCSHF) is set. The SCSHF latch is a "1" during CYC1, phase B when NA6 and NA9 are programmed or during CYC2, phase B when NA5 and NA9 are programmed. In each case, the SCTRS format is shifted in the RTC DLY one bit position. That is, bit 25 is shifted into the bit 24 position one cycle later. A shift of two bits is obtained when the SCSHF latch is set and A9, A6 and A5 are programmed. That is, bit 25 is shifted into the bit 23 position one cycle later.

2-257. In MEM SIM mode, when the instruction address as decoded from the word counter equals zero (IA000), RTC DLY is set to zero at phase A, bit gate 10. During phase A, bit gate 10 of the next change in address, DATA from the "add 1" circuit is being recirculated through the delay line. This recirculated data becomes SCAI3 and SCTRS. There is no change in format in recirculated data since it is clocked at the same bit gate one cycle later.

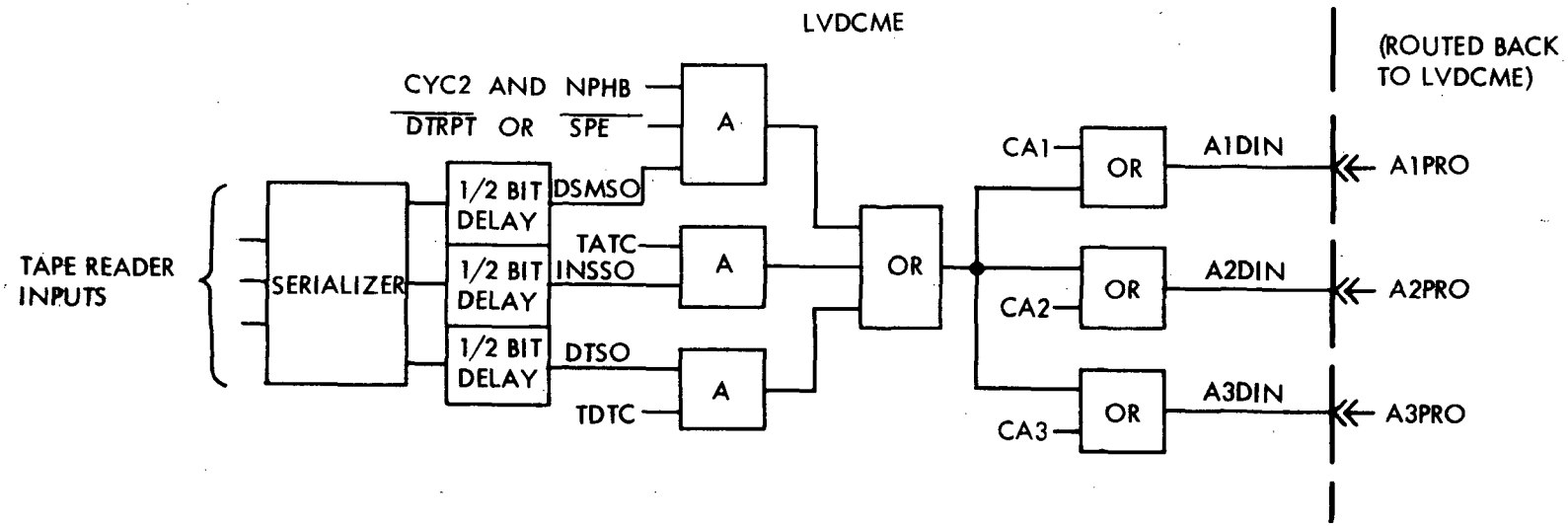


Figure 2-38. Self-Check Simulation of PRO

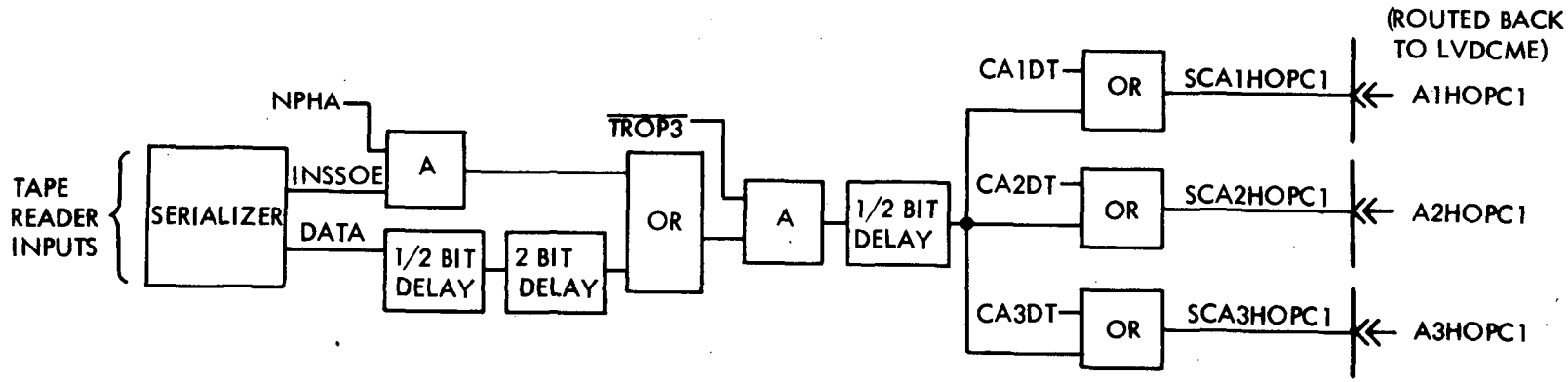


Figure 2-39. Self-Check Simulation of HOPC1

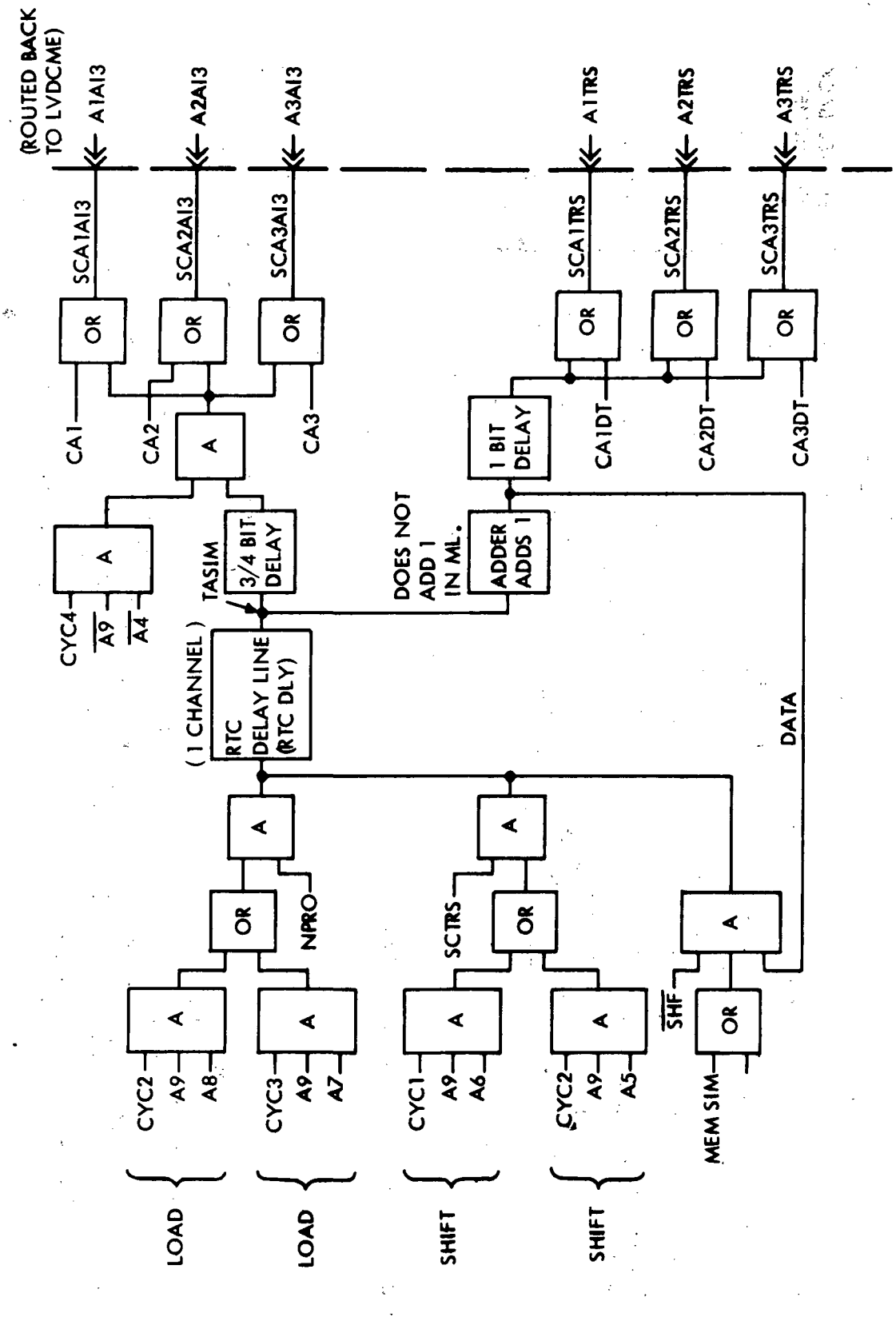


Figure 2-40. Self-Check Simulation of AI3 and TRS

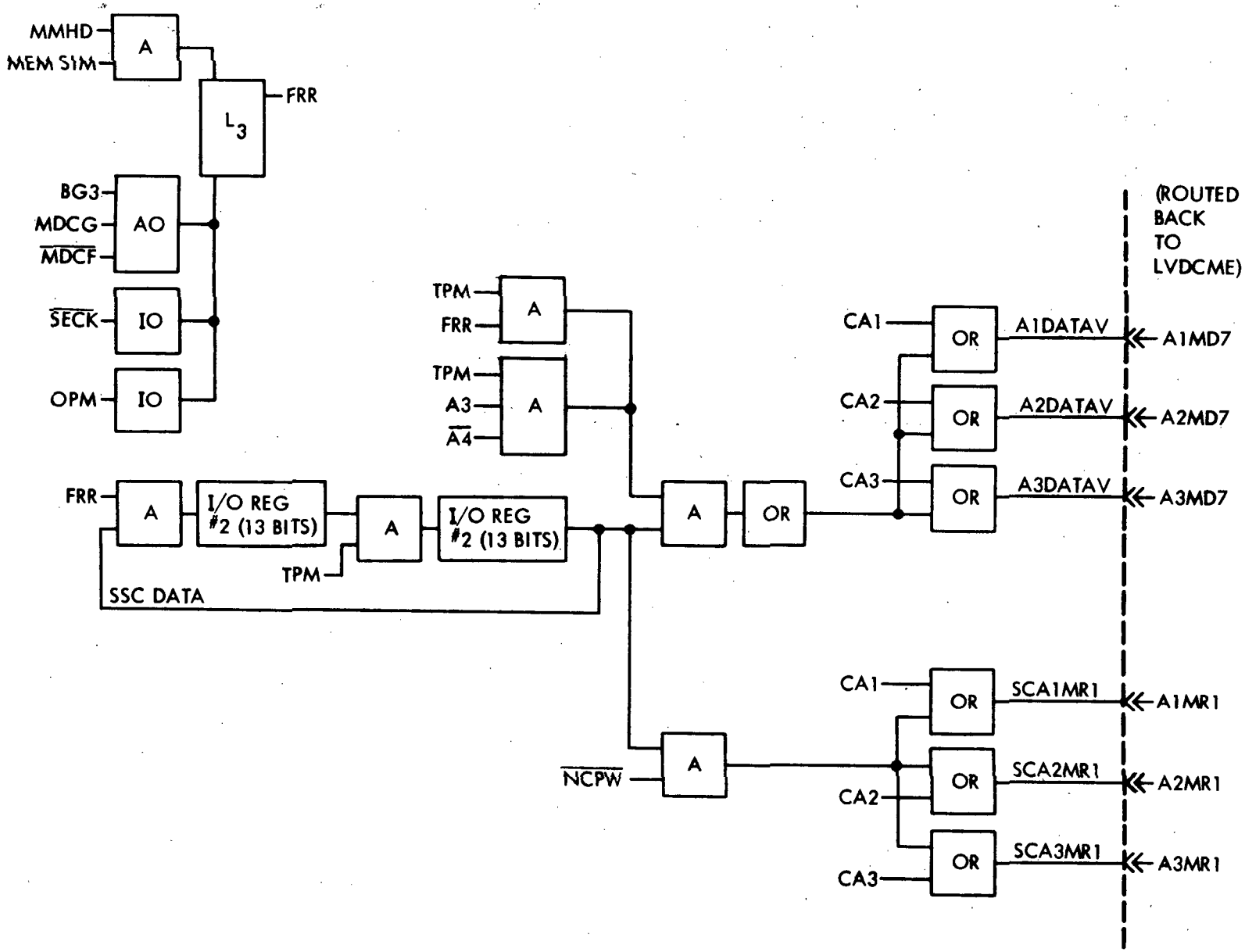


Figure 2-41. Self-Check Simulation of MD7 and MR1

2-258. An AI3 voter error in any channel is induced similarly as in self-check PRO voter error generation. (Refer to paragraph 2-250.)

2-259. A check of the comparators is made during cycle 4, when A9 and A4 are programmed. All SCAI3 channels are forced to a constant "1" without altering the contents of the RTC DLY.

2-260. A TRS voter error in any channel is induced similarly as in self-check HOPC1 voter error generation. (Refer to paragraph 2-252.)

2-261. SELF-CHECK SIMULATION OF MD7 AND MR1.

2-262. The computer MD7 and MR1 data is simulated during self-check by LVDCME circuits that are normally used for computer tests (I/O register 2, and controls). (See figure 10-30, sheets 20, 21, 22 and 23.) The operation of these circuits has been previously described.

2-263. An operation unique only to self-check develops MD7 and MR1 from the three DATA V lines and the three self-check MR1 lines respectively. (See figure 2-41.)

2-264. During MEM SIM and test program mode when a multiply or divide operation is decoded, the free run register latch (FRR) is set. The FRR gate (figure 10-30, sheet 22) allows recirculation of SSC DATA and controls accumulator shift pulses (SA1A-D and SA2A-D) so that SSC data in I/O register 2 is continually being shifted. (See figure 10-30, sheet 21.) The duration of the FRR gate is fourteen counts (two phases) of the multiply-divide counter (9 1/3 computer cycles). (See figure 10-30, sheet 25.) This is the maximum time required to develop partial products, the final product, remainders and the quotient during multiply or divide. Each time the data in the I/O register recirculates, the bit configuration is such that the two low order bits are shifted into the next higher bit positions. The I/O register continues to recirculate once during each count of the multiply-divide counter until the FRR latch is reset. This occurs at bit gate 3 when the multiply-divide counter has gone through a complete count. At this time the I/O register has its original bit configuration.

2-265. The serial output of I/O register 1 (SSC DATA) is gated to three self-check MR1 lines at clock pulse W time and is computer simulated MR1.

2-266. The SSC DATA is also gated to three DATA V lines during test program mode and FRR, or during test program mode when A3 and A4 NOT are programmed. This is computer simulated MD7.

2-267. MR1 and MD7 voter errors (fail to "1") are induced similarly as in self-check PRO voter error generation. (Refer to paragraph 2-250.)

2-268. SELF-CHECK SIMULATION OF REAL TIME COUNTER.

2-269. Self-check real time counter data is simulated from circuits normally used during computer test. (See figure 10-30, sheet 37.) The real time counter is explained in paragraph 2-207.

2-270. Real time counter data is brought back to the LVDCME during self-check, via a self-check cable, and is displayed in the data display register DATA lamps (see figure 10-30, sheet 26) when the DISPLAY SELECT rotary switch is in position 13.

2-271. SELF-CHECK SIMULATION OF PIO. (Figure 10-30, sheet 36.)

2-272. Three channels of self-check PIO are developed when the self-check operation codes (decoded from the tape address bits) generate a PIO operation (SCOP1 NOT, SCOP2, SCOP3 NOT and SCOP4) and the tape reader operation codes (TROP1 through 4) are not decoded as a PIO.

2-273. A voter error (fail to "1") is induced into a channel (A1, or A2, or A3) when the corresponding TRDS1, or 2, or 3 is programmed together with the select data control (SDT). SDT is a decoded TAADR6, TAADR5 NOT and TAADR4 during CYC 3.

2-274. SELF-CHECK SIMULATION OF PTC AI3. (Figure 10-30, sheet 20.)

2-275. PTC AI3 is simulated from LVDCME CIO DATA generated. The LVDCME CIO DATA is generated as follows:

1. SSC DATA gated by a programmed AC CIO 025 (the read SSC code).

2. MLC DATA gated by a programmed AC CIO 021 (the read MLC code).

3. PIO ADRSO gated by a programmed AC CIO 011 (the read PIO ADR code).

4. DTDRB19 gated by a programmed AC CIO 031 (the read phase A information from history code).

5. DTDRB1 gated by a programmed AC CIO 035 (the read phase B and C information from history code).

6. SSMIA gated by a programmed AC CIO 051 (the read SSM and IA information from history code).

7. NSEO gated by a programmed AC CIO 041 (the read disagreement errors code).

8. RTC DATA gated by a programmed AC CIO 015 (the read RTC code)

9. PIOMB25D gated by a programmed AC CIO 001 (the read I/O register 1 code).

10. ADRSO gated by a programmed AC CIO 045 (the read instruction information from history code).

11. AC DISCR OUT 4 (select PRO code), and INTRPT 13(indicates first word from delay line), and LMMH (indicates that the last information was due to a multiply operation).

2-276. SELF-CHECK SERIAL COMPARE ERRORS. (See figure 10-30, sheets 26, 29, 30, 31 and 45.)

2-277. The simulated serial data channeled into the LVDCME via the computer serial data input lines is voted on and compared with the originating serial input data. The simulated serial data is then processed through history, data display and input/output logic as previously described.

2-278. The input serial data is compared with originating serial data in self-check as in normal operation (see paragraphs 2-162 and 2-163). However, there is a unique feature which enables compare in self-check. The enable compare levels are called control address compares (CAC1, 2 and 3) and are always present during normal operation as a

result of a repeated CAD or STO operation decodes. In self-check, the operation codes listed below must be programmed to enable the following compares to take place:

1. Tape reader operation codes (TROP) 1 and 4, or TROP1 NOT, and 2 NOT and 4 = (CAC1), enables SSMSC and AOC compares.

2. TROP2 and 4 or TROP2 NOT and 4 NOT and 1 = (CAC3), enables SSMBR and ADRSR compares.

3. TROP1 and 4 or TROP1 NOT and 2 and 4 NOT = (CAC2), enables SSMDR and INSDR compares.

4. TROP4 NOT and 3 and 2 NOT and 1 NOT enables IADR compare.

5. TROP4 and 3 and 1 enables word serial compare (SER).

6. TROP4 and 3 and 2 enables word parallel compare (PAR).

2-279. Compare errors unique only to self-check are stored in four latches which provide compare error PIO address (CEPIOADR), compare error PIO memory (CEPIOM), compare error PIO accumulator (CEPIOA), and compare error instruction address (CEIADR) outputs and their inverses. These latches are set as follows:

Latch	Set by
CEPIOADR (Figure 10-30, sheet 20)	A non-compare of data serial out (DTSO) and PIO address serial out (PIOADRSO) data at clock pulse W, phase B, CYC 3 when enabling self-check compare level DIEADRCP is generated. DIEADRCP is a programmed TAADR6 NOT, TAADR5 NOT, TAADR4 NOT, TAADR3 NOT, TAADR2 and TAADR1 NOT.
CEPIOM (Figure 10-30, sheet 23)	A non-compare of NMD7 and 2BDDTSO data during ML and clock pulse Z while under control of a self-check enabling level. The enabling level is generated when NA1, NA2 and NA4 NOT are programmed during PIO, phase B, bit gate 6. The enabling level is removed at phase A.
CEPIOA (Figure 10-30, sheet 21)	A non-compare of NMD7 and 2BDDTSO data at Z clock when NA3 and compare enabling level AA are present. AA is generated when NA1, NA2 and NA4 NOT are programmed during PIO, phase B, bit gate 6. The enabling level is removed at phase A, bit gate 6.
CEIADR (Figure 10-30, sheet 32)	A non-compare of address display register and tape reader register data (IADCOMP) during self-check, CYC 3, phase C and bit gate 2 when a compare enabling level is present. The compare enabling level is generated when TROP1 NOT, TROP2 NOT, TROP3 and TROP4 NOT are programmed.

2-280. TAPE READER SELF-CHECK.

2-281. The tape reader manual self-check features include:

1. The FREE RUN READER pushbutton which allows energizing the tape reader transport and tape reader read circuits while bypassing the normal LVDCME tape transport controls (figure 10-30, sheet 14).

2. The FREE RUN SS pushbutton which allows generating an initiating pulse to all the single shots. The tape reader timing clocks are thereby allowed to free-run for check-out purposes. (See figure 10-30, sheet 7.)

3. A one word-at-a-time load feature. This is accomplished each time the START pushbutton is pressed, after the "1" pushbutton has been activated.

2-282. ADDITIONAL SELF-CHECK FEATURES.

2-283. DISPLAY SERIAL OUT. When in the MD mode, the tape reader register and serializer can be checked by using the DISPLAY SERIAL OUT pushbutton. (See paragraph 2-163.) This allows words from the tape serializer to be presented on the data display.

2-284. ERRORS DEVICES TEST. An ERRORS DEVICES TEST pushbutton is used to check the operability of all error latches and all error lamps.

2-285. INVERT ERROR. In the ML mode, an invert error (INV ERR) condition is generated to prevent stopping the tape reader during a known error. The INV ERR latch is set in the self-check mode by a tape address of 01000 and reset by a tape address of 00111. An invert error control pulse generated by a tape address decode of 00100 allows the tape reader to run when an error is encountered.

2-286. PROGRAMS. A wired-in program allows manual check-out of the LVDCME data display and a self-check tape program (the tape is part of the LVDCME) automatically checks approximately 85 percent of the LVDCME. The wired-in program is explained in Section VIII; the self-check tape program is explained in Section VII.

2-287. COMPUTER CONTROL.

2-288. COMPUTER STOP CONTROL.

2-289. The LVDCME stops computer operation when a power halt (PWR HLT) is received from the power sequencing circuits or when a module or channel switching error is detected. Computer operation is also stopped when computer single step (CST) operation is commanded in any of the following ways:

1. The STOP switch is pressed.

2. An address compare is obtained while SINGLE STEP - ON/OFF is ON.

3. A CIO 106 instruction is received from the PTC.

4. Any PIO code is used in the operational program mode.

5. The LVDA single-step signal (DST) is received by the LVDCME.

2-290. COMPUTER SINGLE STEP.

2-291. When a CST operation is commanded, the computer does not read any new instructions. However, if an interrupt, HOP or EXM operation is in process, CST is delayed until the process is completed. The contents of the history delay lines are recirculated during CST unless a multiply or divide is being performed at the time the CST is commanded. In this case, the history multiply-divide delay lines continue to store data until the multiply or divide is completed.

2-292. When the LVDCME is in CST and the ADVANCE pushbutton is pressed, CST is removed from the computer for one word time and then reapplied. This allows the computer to read and perform one instruction. The same restrictions that govern the application of CST (paragraph 2-291) cover the reapplication of CST after the ADVANCE pushbutton is pressed.

2-293. COMPUTER RESTART.

2-294. When computer operation is stopped by a halt signal (NHLT), the program is restarted when the halt signal is removed. When the RESTART - AUTO/MAN/PTC pushbutton is set to MAN/PTC, a computer restart may be initiated by pressing the MANUAL RESTART pushbutton or by issuing a CIO 116 (set HLT) and then a CIO 122 (reset HLT). When the RESTART - AUTO/MAN/PTC switch is set to AUTO, the computer program is automatically restarted whenever an instruction address or data address compare occurs.

2-295. MEMORY CLOCK CONTROL.

2-296. The LVDCME controls the timing of the computer memory clock by means of two signals — A1-2MCN and A1-2MCL. These signals are controlled by the EARLY, NORMAL and LATE pushbuttons. When the EARLY pushbutton is pressed, A1-2MCN becomes a "0" and causes the computer memory clock driver to be strobed early. When the LATE pushbutton is pressed, A1-2MLC becomes a "1" and causes the computer memory clock driver to be strobed late. When the NORMAL pushbutton is pressed, A1-2MCN becomes a "1" and A1-2MCL becomes a "0" and the computer memory clock driver is strobed at the normal time.

2-297. HISTORY STORAGE.

2-298. History storage is accomplished by three 13-word delay lines that store serial AI3, TRS, ADR, MR1, MD7 and PRO data. In normal operation, new data is continually being loaded into the AI3 and TRS delay lines. These delay lines contain data from the last 13 instruction cycles. Whenever the computer program is stopped, history data is recirculated in these delay lines. The AI3 and TRS delay lines therefore store data from the 13 instruction cycles before the computer was stopped. This data may be displayed on the DATA display.

2-299. During multiply-divide operations, new data is being loaded into MR1, MD7 or PRO delay lines. These delay lines contain recirculated multiply-divide information when no new multiply or divide operation is in progress.

2-300. Two types of data are time-shared in each of the delay lines: AI3 and TRS data share the AI3/TRS delay line, ADR and MR1 data share the ADR/MR1 delay line, and MD7 and PRO data share the MD7/PRO delay line. Time sharing is accomplished by interleaving the two types of data in the delay line and then separating the data at the output of the delay line. History data is available on the HISTAI3, HISTTRS, HISTADR, HISTMR1, HISTMD7 and HISTPRO lines.

2-301. OPERATIONAL/TEST PROGRAM MODE SELECTION.

2-302. The LVDCME can be used to exercise a computer which is loaded with either the operational program or a test program. Since computer operation depends on the type of computer program, the LVDCME may be operated in either the operational program mode (OPM) or the test program mode (TPM). OPM and TPM are alternately selected each time the OP/TP switch is pressed. The OP and TP lamps indicate the mode in which the LVDCME is prepared to operate.

SECTION III

INTERFACE AND CONTROLS

3-1. INTERFACE.

3-2. All of the LVDCME interface signals appear at pins of connectors located on the connector panel assembly 02A3 (figure 3-1) and connector panel assembly 01A11 (figure 3-2). Connectors 02A3J1 (SYNC) and 02A3J2 (MARKER) are single UHF type jacks, connectors 02A3J3 (SP1) and 02A3J4 (SP2) are 5-pin connectors, and connectors 02A3J5 through 02A3J23 and 01A11J25 through 01A11J32 are 55-pin connectors.

3-3. The interface signals and connectors are shown on the LVDCME cable diagrams (figures 10-11, 10-18, 10-19, 10-20, 10-22, 10-23, and 10-24).

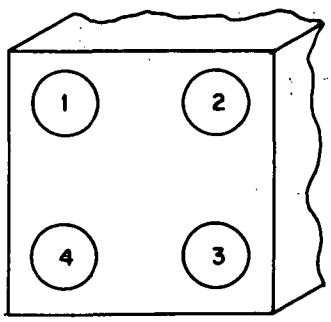
3-4. CONTROLS AND INDICATORS.

3-5. The LVDCME operating controls and indicators are shown on figures 3-3 through 3-6 and are described in figure 3-7. Test points that appear on the control panels are included as indicators in figure 3-7. The location of each control panel on the LVDCME is shown on figure 1-2.

3-6. In addition to the controls and indicators described in figure 3-7, the AC Power Gate Assembly (01B5) at the rear of the LVDCME contains a time totalizing meter (9999 hour) and the circuit breakers for the LVDCME AC input power.

3-7. The controls and indicators on the power supplies (01A5 through 01A8, 02A5, 02A6, 02A7, 02A9, and 02A10) are described in the commercial manuals for these power supplies. (Refer to the list of related manuals.)

3-8. Many of the LVDCME controls and indicators are pushbutton switches which contain four lamp bulbs that light under certain conditions. The four bulbs (1, 2, 3 and 4) are arranged as shown here:



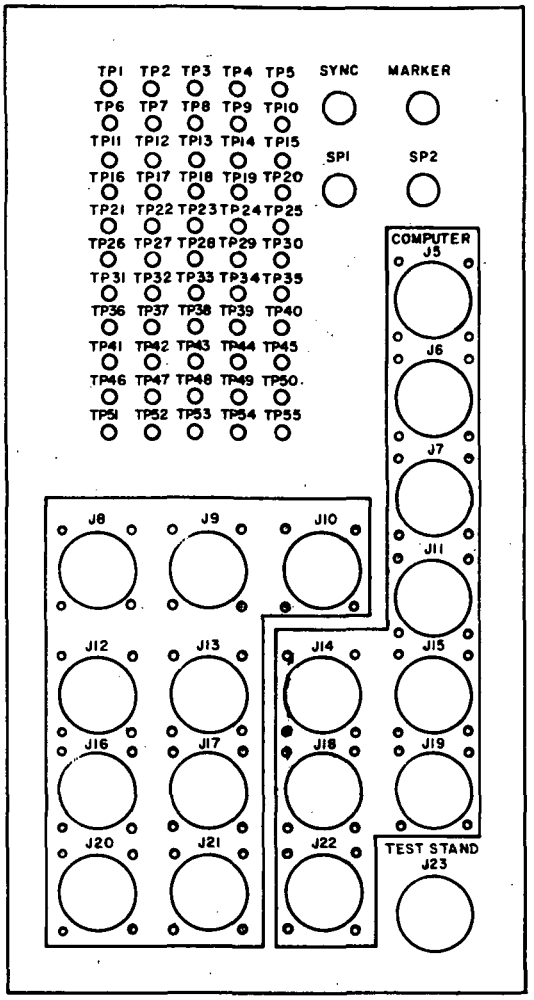


Figure 3-1. Connector Panel Assembly (02A3)

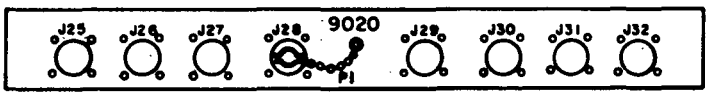


Figure 3-2. Connector Panel Assembly (01A11)

3-9. These bulbs can be wired in many configurations; the following six configurations are used on the LVDCME:

1. Bulbs 1 and 3 or bulbs 1 and 4 constitute one indication.

2. Bulb 1 or bulb 2 constitutes one indication; bulb 3 or bulb 4 constitutes a different indication.

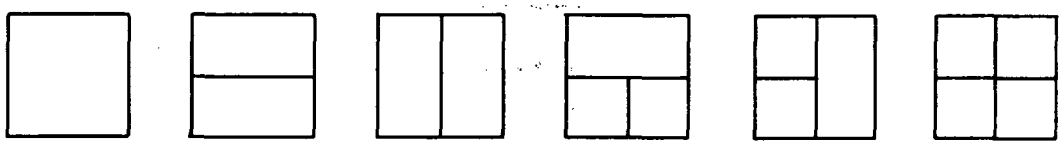
3. Bulb 1 or bulb 4 constitutes one indication; bulb 2 or bulb 3 constitutes a different indication.

4. Bulb 1 or bulb 2 constitutes one indication; bulb 3 constitutes a different indication; and bulb 4 constitutes a different indication.

5. Bulb 2 or bulb 3 constitutes one indication; bulb 1 constitutes a different indication; and bulb 4 constitutes a different indication.

6. Each lamp constitutes a different indication.

3-10. These wiring configurations, listed in paragraph 3-9, correspond to the following patterns on the switch faces:



NOTE

Some indications are located on the faces of switches to which they are not electrically connected. These indications are explained in figure 3-7.

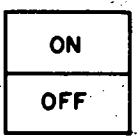
3-11. The following definitions are used in figure 3-7:

1. Momentary pushbutton/lamp. A momentary pushbutton/lamp is a momentary contact pushbutton switch containing lamp bulbs that are lit only while the switch is being pressed. The function controlled by the switch is in the "1" state only while the lamp is lit.

2. Pushbutton/lamp. A pushbutton/lamp is a momentary contact pushbutton switch connected to the LVDCME logic so that its lamp bulbs remain or become lit after the switch face is pressed. The function controlled by the switch is in the "1" state only while the lamp is lit.

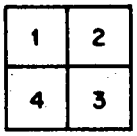
3. Alternate action pushbutton/lamp. An alternate action pushbutton/lamp is a DPDT pushbutton switch (containing lamp bulbs) whose state is changed by pressing the switch face. The lamp bulbs within the switch may be wired in one of the following ways:

a. A bulb (or bulbs) is always lit to indicate the state of the function controlled by the switch. For example, the ON portion of the ON/OFF alternate action pushbutton/lamp shown here is lit only when the function it controls is on.



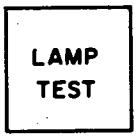
When the ON portion is lit, the OFF portion is not lit, and vice versa.

A second example of this type of wiring occurs when the switch face is partitioned into four areas as shown here:



Only one of the four lamp bulbs is lit at any time. When the switch face is pressed, the next clockwise lamp bulb is lit; a complete cycle occurs if the switch face is pressed four times.

b. Bulbs within the switch are lit only when the function it controls is a "1". For example, the LAMP TEST alternate action pushbutton/lamp shown here is lit only while a lamp test operation is in progress.



When LAMP TEST is pressed while its bulbs are lit, the lamp test operation ceases and the bulbs are turned off. When LAMP TEST is pressed again, another lamp test operation occurs and the bulbs are again lit.

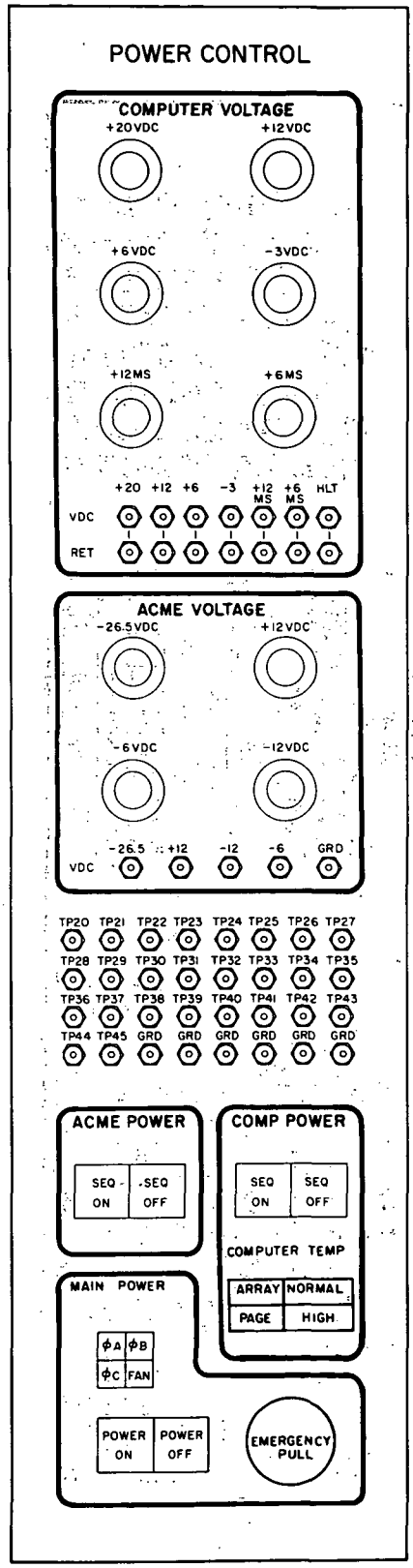


Figure 3-3. Power Control Panel

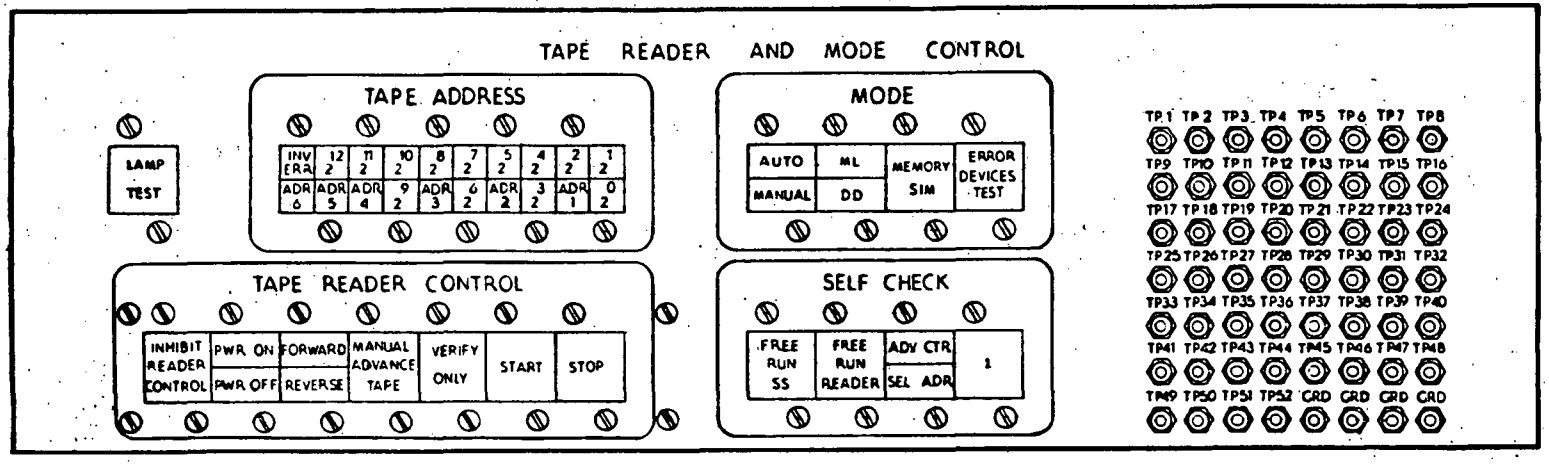


Figure 3-4. Tape Reader and Mode Control Panel

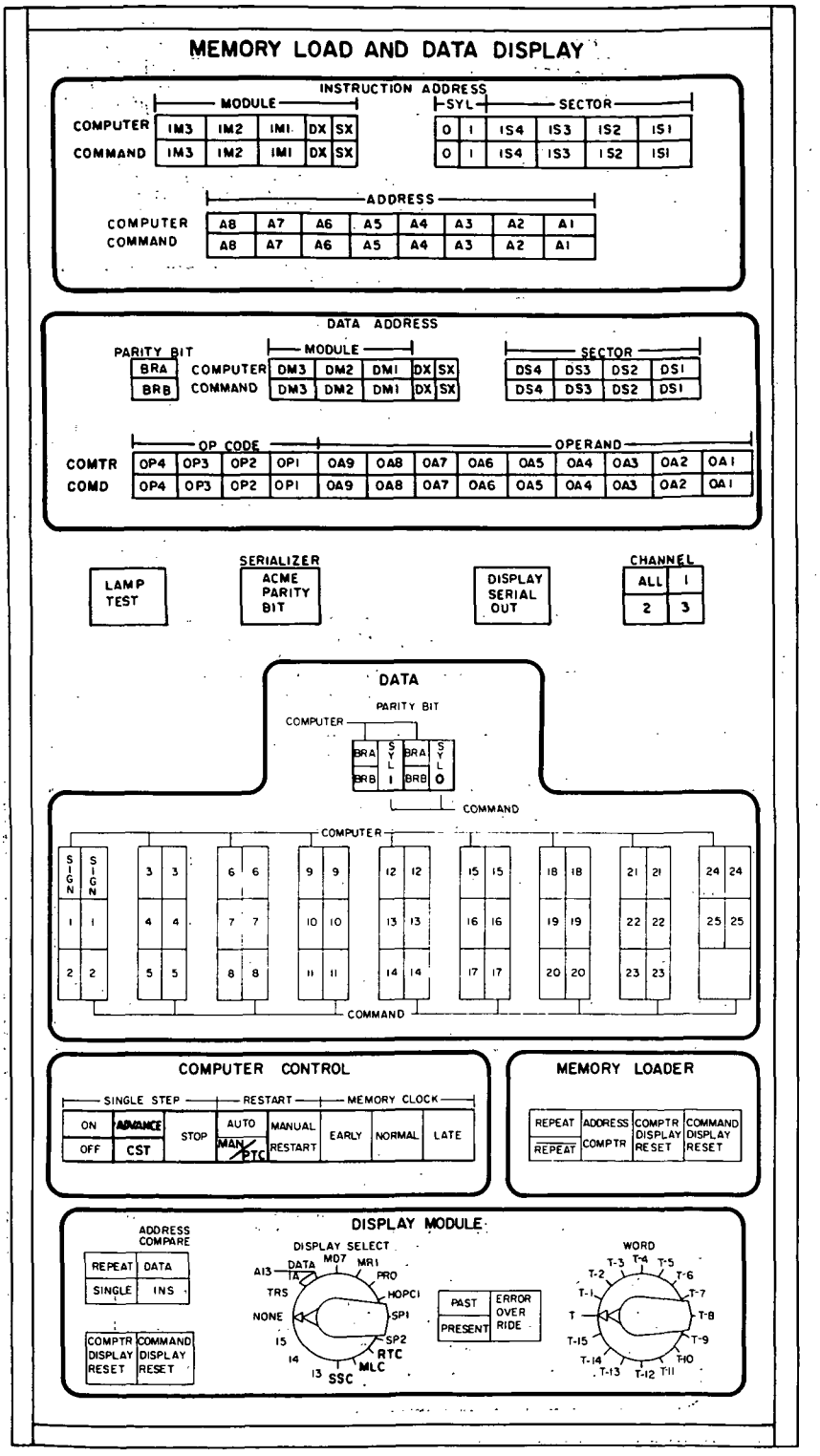


Figure 3-5. Memory Load and Data Display Panel

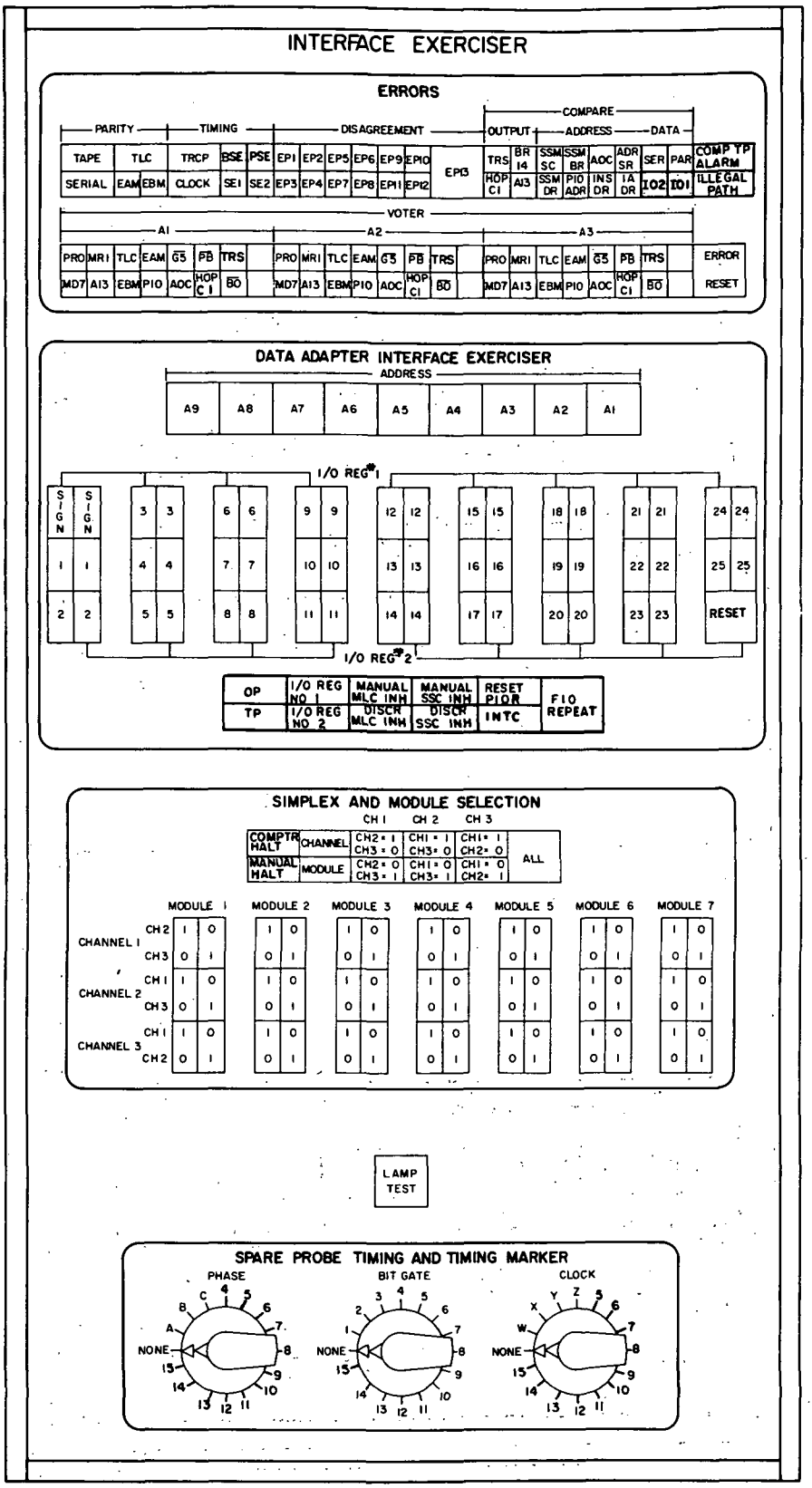


Figure 3-6. Interface Exerciser Panel

Panel	Area	Control/Indicator	Description and Function
POWER CONTROL (figure 3-3)	COMPUTER VOLTAGE	+20 VDC, +12 VDC, +6 VDC, -3 VDC, +12 MS, and +6 MS	Adjustments for varying the corresponding voltages supplied to the computer. (MS stands for module switching.)
		+20, +12, +6, -3, +12 MS, and +6 MS (VDC and RET)	Test jacks for monitoring the outputs of the corresponding power supplies.
		HLT (VDC and RET)	Test jacks for monitoring the power halt (HLT) signal to LVDCME logic.
	ACME VOLTAGE	-26.5 VDC, +12 VDC, -6 VDC and -12 VDC	Adjustments for varying the corresponding voltages supplied to LVDCME circuits.
		-26.5, +12, -12, -6, and GRD	Test jacks for monitoring the outputs of the corresponding LVDCME power supplies. (GRD is the common return for these supplies.)
	None	TP20 through TP45 and GRDs	Test jacks for monitoring the voltages supplied to computer circuits. (Refer to figure 10-9 for voltage at each point.)
	ACME POWER	SEQ ON	Pushbutton/lamp that starts the LVDCME DC power-on sequence and indicates when lit that sequencing is complete.
		SEQ OFF	Pushbutton/lamp that starts the LVDCME DC power-off sequence and indicates when lit that sequencing is complete.

Figure 3-7. Controls and Indicators (Sheet 1 of 15)

Panel	Area	Control/Indicator	Description and Function
POWER CONTROL (figure 3-3)	COMP POWER	SEQ ON	Pushbutton/lamp that starts the computer DC power-on sequence and indicates when lit that sequencing is complete.
		SEQ OFF	Pushbutton/lamp that starts the computer DC power-off sequence and indicates when lit that sequencing is complete.
		ARRAY/PAGE	Lamps that light indicating that either or both computer array (memory) or page temperature is high.
		NORMAL/HIGH	Lamps that light indicating that computer array (memory) or page temperature is normal or high. If NORMAL lamp is lit, ARRAY/PAGE lamps will be out.
	MAIN POWER	ϕA, ϕB, and ϕC	Lamps when lit indicate that the corresponding phase is available to LVDCME circuits.
		FAN	Lamp when lit indicates that power is applied to SMS card gate fans.
		POWER ON	Pushbutton/lamp that starts the LVDCME AC power-on sequence and indicates when lit that sequencing is complete.
		POWER OFF	Pushbutton/lamp that starts the LVDCME AC power-off sequence and indicates when lit that sequencing is complete.
		EMERGENCY PULL	Switch when pulled removes all LVDCME power.

Figure 3-7. Controls and Indicators (Sheet 2)

Panel	Area	Control/Indicator	Description and Function
TAPE READER AND MODE CONTROL (figure 3-4)	None	LAMP TEST	Pushbutton/lamp used to check all indicator lamps on this panel and on the POWER CONTROL panel.
	TAPE ADDRESS	ADR1 through 6 and INV ERR	Pushbutton/lamps that indicate the address bits of the tape word being read. These bits do not indicate actual tape addresses. The decoded bits perform LVDCME functions. ADR1 through 5 can be used to manually insert address bits into the tape reader register.
		2^0 through 2^{12}	Pushbutton/lamps that indicate the tape word count in both AUTO and MANUAL modes and can be used to manually set in the word count. Counts the number of sequence bits in ML mode and counts the number of computer cycles in MEMORY SIM mode.
	MODE	AUTO/MANUAL	Alternate action pushbutton/lamp that allows the tape reader and the memory load portion of the LVDCME to operate in either automatic or manual mode.
		ML/DD	Alternate action pushbutton/lamp that allows the LVDCME to operate in either memory load or data display mode.
		MEMORY SIM	Pushbutton/lamp that allows hard wired program to operate (self-test only). In MEMORY SIM mode, the word counter output decoded, simulates computer OP Codes and Instruction Addresses.
		ERROR DEVICES TEST	Pushbutton that simultaneously sets all error latches. When the ERROR DEVICES TEST button is pressed, all ERRORS lamps on INTERFACE EXERCISER panel light.

Figure 3-7. Controls and Indicators (Sheet 3)

Panel	Area	Control/Indicator	Description and Function
TAPE READER AND MODE CONTROL (figure 3-4)	TAPE READER CONTROL	INHIBIT READER CONTROL	Pushbutton/lamp that inhibits tape reader and spooler operation.
		PWR ON/PWR OFF	Alternate action pushbutton/lamp that applies power to or removes from the tape reader and tape spooler.
		FORWARD/REVERSE	Alternate action pushbutton/lamp that places tape reader in either the forward or reverse mode.
		MANUAL ADVANCE TAPE	Pushbutton/lamp that when in MANUAL mode allows the tape to move the distance of one word (forward or reverse) each time button is pressed.
		VERIFY ONLY	Pushbutton/lamp that causes the LVDCME to ignore the load portions of a tape.
		START	Pushbutton/lamp that starts tape reader and tape spooler operation.
		STOP	Pushbutton/lamp that stops tape reader and tape spooler operation.
	SELF CHECK	FREE RUN SS	Alternate action pushbutton/lamp that free runs the single shots of the LVDCME during self check.
		FREE RUN READER	Alternate action pushbutton/lamp that starts or stops the tape reader and tape spooler during self check. This switch by-passes the RUN tratch.
		ADV CTR/SEL ADR	Alternate action pushbutton/lamp that allows word counter (2^0 through 2^{12}) to be advanced when ADV CTR is lit. When SEL ADR is lit, it allows manual selection of tape address (AR1 through ADR6).

Figure 3-7. Controls and Indicators (Sheet 4)

Panel	Area	Control/Indicator	Description and Function
TAPE READER AND MODE CONTROL (figure 3-4)	SELF CHECK	1	Alternate action pushbutton/lamp that allows tape to be advanced one word at a time during self check.
	None	TP1 through TP52 and GRDs	Test points for monitoring tape reader signals and voltages and special LVDCME signals.
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	INSTRUCTION ADDRESS	MODULE - IM1, IM2, and IM3	Pushbutton/lamps that control the three-bit memory module selection code when reference is made to memory for an instruction. The lower (COMMAND) lamps indicate the module to be used for compare; the upper (COMPUTER) lamps indicate the actual module compared on.
		MODULE - DX/SX	Pushbutton/lamps that alternately select duplex or simplex instruction memory operation each time button is pressed. Lower (COMMAND) lamps indicate commanded instruction memory mode to be used for compare; upper (COMPUTER) lamps indicate actual instruction memory mode compared on.
		SYL-0 1	Pushbutton/lamp that alternately selects either syllable 0 or syllable 1 for instruction word whenever button is pressed. Lower (COMMAND) lamps indicate commanded syllable to be used for compare; upper (COMPUTER) lamps indicate the actual syllable compared on.
		SECTOR - IS1 through IS4	Pushbutton/lamps that control four-bit instruction sector address code. The lower (COMMAND) lamps indicate commanded sector address bits to be used for compare; the upper (COMPUTER) lamps indicate the actual sector address bits compared on.

Figure 3-7. Controls and Indicators (Sheet 5)

Panel	Area	Control/Indicator	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	INSTRUCTION ADDRESS	ADDRESS A1 through A8	Pushbutton/lamps that control the eight-bit instruction address code. The lower (COMMAND) lamps indicate commanded memory instruction address bits to be used for compare; the upper (COMPUTER) lamps indicate the actual memory instruction address bits compared on.
	DATA ADDRESS	PARITY BIT-BRA BRB	Lamps that indicate the existence of instruction word parity bits in buffer registers A and B.
		MODULE - DM1 through DM3	Pushbutton/lamps that control the three-bit memory module selection code when reference is made to memory for data. The lower (COMMAND) lamps indicate the data memory module to be used for compare; the upper (COMPUTER) lamps indicate the actual data memory module compared on.
		DX/SX	Pushbutton/lamps that alternately select duplex or simplex data memory operation each time button is pressed. Lower (COMMAND) lamps indicate commanded data memory mode to be used for compare; upper (COMPUTER) lamps indicate actual data memory mode compared on.
		SECTOR - DS1 through DS4	Pushbutton/lamps that control the four-bit data sector address code. The lower (COMMAND) lamps indicate the commanded data sector address bits to be used for compare; the upper (COMPUTER) lamps indicate the actual data sector address bits compared on.

Figure 3-7. Controls and Indicators (Sheet 6)

Panel	Area	Control/Indicator	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DATA ADDRESS	OP CODE - OP1 through OP4	Pushbutton/lamps that control computer operation code bits (ML mode only). The lower (COMD) lamps indicate the commanded operation code bits to be used for compare; the upper (COMPTR) lamps indicate the actual operation code bits compared on.
		OPERAND - OA1 through OA9	Pushbutton/lamps that control computer operand address code bits. The lower (COMD) lamps indicate the commanded operand address code bits to be used for compare; the upper (COMPTR) lamps indicate the actual operand address code bits compared on.
	None	LAMP TEST	Alternate action pushbutton/lamp used to check all indicator lamps on this panel.
		SERIALIZER-ACME PARITY BIT	Lamp when lit indicates odd parity in the tape reader register.
		DISPLAY SERIAL OUT	Pushbutton/lamp that allows words from the tape serializer to be presented on the data display.
		CHANNEL 1, 2, 3, and ALL	Lamps that indicate channel or channels in use (when channel switching).
	DATA	PARITY BIT-BRA/BRB	Lamps that indicate the existence of buffer registers A and B parity bits.
		PARITY BIT-SYL 0 and SYL 1	Lamps that indicate the existence of data word (COMMAND) parity bits in syllables 0 and 1.

Figure 3-7. Controls and Indicators (Sheet 7)

Panel	Area	Control/Indicator	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DATA	SIGN through 25	Pushbutton/lamps that control the bits of a data word to be loaded into the computer. The lamps at the right side of the pushbuttons indicate the commanded data bits; the lamps at the left side indicate the actual data bits.
	COMPUTER CONTROL	SINGLE STEP-ON OFF	Alternate action pushbutton/lamp that starts or stops single-step computer operation. Upper (ON) lamp when lit indicates the computer is in the single-step mode; lower (OFF) lamp indicates the computer is not in the single-step mode.
		SINGLE STEP-ADVANCE/CST	Pushbutton/lamp that steps the computer program one word when in the single-step mode. Both ADVANCE and CST lamps must be lit for the computer program to be advanced one word.
		SINGLE STEP-STOP	Pushbutton that stops computer operation.
		RESTART-AUTO/MAN/PTC	Alternate action pushbutton/lamp that allows the computer to be restarted automatically or manually. When upper (AUTO) lamp is lit, computer is restarted whenever the computer instruction address matches the instruction address inserted in the INSTRUCTION ADDRESS switches; when lower (MAN/PTC) lamp is lit, computer is restarted whenever MANUAL RESTART (COMPUTER CONTROL) is pressed.
		RESTART-MANUAL RESTART	Refer to AUTO/MANUAL above. If MAN/PTC lamp is lit and MANUAL RESTART is pressed, HLT occurs in 3 MS.

Figure 3-7. Controls and Indicators (Sheet 8)

Panel	Area	Control/Indicator	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	COMPUTER CONTROL	MEMORY CLOCK-EARLY, NORMAL, and LATE	Pushbutton/lamps that cause the memory clock to occur early, normal or late when the corresponding button is pressed. Lamps light to indicate the occurrence of the memory clock.
	MEMORY LOADER	REPEAT/$\overline{\text{REPEAT}}$	Alternate action pushbutton/lamp that causes the selected memory location to be loaded repeatedly (REPEAT) or just once ($\overline{\text{REPEAT}}$). See ADDRESS COMPTR pushbutton.
		ADDRESS COMPTR	Pushbutton/lamp that causes the memory location to be loaded just once in conjunction with $\overline{\text{REPEAT}}$ pushbutton.
		COMPTR DISPLAY RESET	Pushbutton that resets all computer display bits causing all computer display lamps to go out.
		COMMAND DISPLAY RESET	Pushbutton that resets all command display bits causing all command display lamps to go out.
	DISPLAY MODE	REPEAT/SINGLE	Alternate action pushbutton/lamp that causes data to be displayed only during the first pass through the program (SINGLE) or during each program pass (REPEAT).
		ADDRESS COMPARE-DATA/INS	Alternate action pushbutton/lamp that permits data or instruction address comparisons.
		COMPTR DISPLAY RESET	Pushbutton that resets all computer display bits causing computer display lamps to go out.
		COMMAND DISPLAY RESET	Pushbutton that resets all command display bits causing all command display lamps to go out.

Figure 3-7. Controls and Indicators (Sheet 9)

Panel	Area	Control/Indicator	Description and Function
MEMORY LOAD AND DATA DISPLAY (figure 3-5)	DISPLAY MODE	DISPLAY SELECT	Rotary switch that selects data for display as follows: Position — Type of Data NONE — None TRS — Transfer register serial AI3-IA — Instruction address A13-DATA — Accumulator data MD7 — Multiplicand/divisor MR1 — Multiplier/product/quotient PRO — Partial product/remainder HOPC1 — HOP constant SP1 — Input to spare probe 1 SP2 — Input to spare probe 2 TRC — Real time counter MLC — Minor loop counter SSC — Switch select counter 13 — Self check real time counter 14 and 15 — Spares
		PAST/PRESENT	Alternate action switch that permits data display for present or preceding word.
		ERROR OVER RIDE	Pushbutton/lamp that allows all voter errors and all disagreement errors to be ignored.
		WORD	Rotary switch that selects word or partial product from delay lines for display.

Figure 3-7. Controls and Indicators (Sheet 10)

Panel	Area	Control/Indicator	Description and Function
INTERFACE EXERCISER (figure 3-6)	ERRORS	Refer to description and function column	Lamps that light to indicate errors as follows:

	Lamp	Type of Error
PARITY	TAPE	Tape parity
	SERIAL	Serial parity
	TLC	Two simultaneous memory parity
	EAM	Memory module A parity
	EBM	Memory module B parity
TIMING	TRCP	Tape reader clock pulse
	CLOCK	Clock
	BSE	Bit sync
	PSE	Phase sync
	SE1	Tape sequence
	SE2	Tape sequence
DISAGREEMENT	EP1 through EP13	Disagreement
COMPARE	TRS	Transfer register serial output compare
	HOPC1	HOP constant compare
	BR14	Buffer register compare
	AI3	Accumulator data compare
	SSMSC	Sector/syllable/module serial compare
	SSMDR	Sector/syllable/module display register compare
	SSMBR	Sector/syllable/module buffer register compare
	PIO ADR	PIO address compare

Figure 3-7. Controls and Indicators (Sheet 11)

Panel	Area	Control/Indicator	Description and Function
INTERFACE EXERCISER (figure 3-6)	ERRORS	Refer to description and function column	

	Lamp	Type of Error
COMPARE	AOC	Address and operation code compare
	INS DR	Instruction display register compare
	ADRSR	Address shift register compare
	IADR	Instruction address display register compare
	SER	Serial compare
	IO2	I/O register No. 2 serial compare
	PAR	Parallel compare
	IO1	I/O register No. 1 serial compare
	COMPTR ALARM	Computer
	ILLEGAL PATH	Module/channel switching
	*PRO	Partial product/remainder
	*MD7	Multiplicand/divisor
	*MRI	Multiplier/product/quotient
	*AI3	Accumulator
	*TLC	Simultaneous memory
	*EBM	Memory module B
	*EAM	Memory module A
	*PIO	PIO
	*$\overline{G5}$	Bit gate generator
	*AOC	Address and operation code

Figure 3-7. Controls and Indicators (Sheet 12)

Panel	Area	Control/Indicator	Description and Function
INTERFACE EXERCISER (figure 3-6)	ERRORS	Refer to description and function column	Lamp / Type of Error *$\overline{PB}$ — Phase B *HOPC1 — HOP *TRS — Transfer register serial *$\overline{BO}$ — Buffer oscillator *NOTE: These lamps indicate errors in the channel (A1, A2, or A3) shown above the lamp.
		ERROR RESET	Pushbutton that resets all indicators in the ERRORS area.
	DATA ADAPTER INTERFACE EXERCISER	ADDRESS A1 through A9	Lamps that represent the nine bits in the address portion of the PIO instruction.
		I/O REG #1-SIGN through 25	Momentary pushbutton/lamps that allow manual loading of I/O register No. 1 during test program or operational program mode when in single step. When in automatic mode, I/O register No. 1 can be loaded from computer memory or accumulator, or PTC accumulator, or LVDCME data register and can be transferred to PTC or computer.
		I/O REG #2-SIGN through 25	Momentary pushbutton/lamps that allow manual loading of I/O register No. 2 during operational program mode when in single step. When in automatic mode, I/O register No. 2 can be loaded from the computer memory or accumulator or PTC accumulator and can be transferred to PTC.
		RESET	Momentary pushbutton/lamp that resets either I/O REG #1 or I/O REG #2.

Figure 3-7. Controls and Indicators (Sheet 13)

Panel	Area	Control/Indicator	Description and Function
INTERFACE EXERCISER (figure 3-6)	DATA ADAPTER INTERFACE EXERCISER	OP/TP	Alternate action pushbutton/lamp that specifies mode of operation (Operational Program mode or Test Program mode).
		I/O REG No. 1/ I/O REG No. 2	Alternate action pushbutton/lamp that allows manual insertion of data into or the resetting of I/O REG #1 or I/O REG #2.
		MANUAL MLC INH/ DISCR MLC INH	Alternate action pushbutton/lamp that inhibits generation of an interrupt by the Minor Loop Counter during operational program mode (MANUAL MLC INH). The DISCR MLC INH lamp indicates that the inhibiting of the generation of an interrupt by the Minor Loop Counter is being performed by a discrete from the PTC.
		MANUAL SSC INH/ DISCR SSC INH	Alternate action pushbutton/lamp that inhibits generation of an interrupt by the Switch Selector Counter during operational program mode (MANUAL SSC INH). The DISCR SSC IHN lamp indicates that the inhibiting of the generation of an interrupt by the Switch Selector Counter is being performed by a discrete from the PTC.
		RESET PIOR/INTC	Alternate action pushbutton/lamp that allows manual resetting of the PIOR latch without repeating PIO function to computer (RESET PIOR). The INTC lamp indicates computer interrupt.
		PIO REPEAT	Momentary pushbutton that allows manual repeat PIO when information is required from LVDCME during operational program mode.

Figure 3-7. Controls and Indicators (Sheet 14)

Panel	Area	Control/Indicator	Description and Function
INTERFACE EXERCISER (figure 3-6)	SIMPLEX AND MODULE SELECTION	COMPTR HALT/ MANUAL HALT	The COMPTR HALT lamp indicates computer halt. MANUAL HALT is an alternate action pushbutton/lamp that stops computer operation and allows manual channel/ module switching.
		CHANNEL/MODULE	Alternate action pushbutton/lamp that selects either the channel-switching or module switching mode of operation.
		CH 1	Momentary pushbutton/lamp that selects channel 1 by setting channel 2 to a 1 and channel 3 to a 0, or channel 2 to a 0 and channel 3 to a 1.
		CH 2	Momentary pushbutton/lamp that selects channel 2 by setting channel 1 to a 1 and channel 3 to a 0, or channel 1 to a 0 and channel 3 to a 1.
		CH 3	Momentary pushbutton/lamp that selects channel 3 by setting channel 1 to a 1 and channel 2 to a 0, or channel 1 to a 0 and channel 2 to a 1.
		ALL	Pushbutton/lamp that selects all three TMR channels.
		MODULE 1 through 7, CHANNEL 1 through 3	Momentary pushbutton/lamps that select one of three channels in each of seven modules. (Refer to Section II for a detailed description of module and channel switching.)
	None	LAMP TEST	Alternate action pushbutton/lamp used to check all indicator lamps on this panel.
	SPARE PROBE TIMING AND TIMING MARKER	PHASE, BIT GATE, AND CLOCK	Rotary switches that provide spare probe timing gates for the data display.

Figure 3-7. Controls and Indicators (Sheet 15)

SECTION IV

TEST EQUIPMENT AND SPECIAL TOOLS

4-1. SCOPE.

4-2. This section contains the list of standard test equipment and the list and illustrations of the special tools recommended for maintenance of the LVDCME. No special test equipment is required for maintenance of the LVDCME.

4-3. TEST EQUIPMENT.

4-4. Figure 4-1 is the list of standard test equipment recommended for maintenance of the LVDCME. This equipment is not supplied with the LVDCME. Equipment having the same range and accuracy as those listed in figure 4-1 may be substituted for the items listed.

4-5. SPECIAL TOOLS.

4-6. Figure 4-2 is the list of special tools recommended for maintenance of the LVDCME; these special tools are not supplied with the LVDCME. Equivalent tools may be substituted for the items listed.

Name	Model or Type	Vendor
Oscilloscope	585A	Tektronix, Inc.
Plug-in Unit and Adapter	M	Tektronix, Inc.
Differential Voltmeter AC/DC	803-B	John Fluke Mfg. Co., Inc.
Digital Voltmeter	456	Kintel Division, Cohu Electronics, Inc.
AC Converter	452	Kintel Division, Cohu Electronics, Inc.
Digital Readout	473A	Kintel Division, Cohu Electronics, Inc.
Milliammeter (0-15 ma)	901	Weston Instrument Division, Daystrom Inc.
Volt-Ohm-Ammeter	630-A	Triplett Electrical Instrument Co.
Volt-Ohmmeter	269	Simpson Electric Co.
Capacitance Bridge	650-A	General Radio Co.

Figure 4-1. Recommended Standard Test Equipment

Name	Vendor Part No.	Application	Illustration Figure 4-3
SMS Card Puller	IBM 6072429	Facilitates insertion or removal of SMS cards.	Part A
SMS Card Contact Lubricant	IBM 6072430	Insures low contact resistance and reduces wear of the gold-plated SMS card contact surfaces.	Part B
SMS Card Extender	IBM 6072431	Allows access to the components and wiring of an SMS card while the card is connected into the system	Part C
SMS Card Socket Terminal Extractor	IBM 6072432	Used to remove SMS card socket terminals (contacts).	Part D
Soldering Handle	Hexacon P25	Handle for soldering tip.	Part X
Soldering Tip	Hexacon HT248D	Used to remove or install SMS card socket terminals that are soldered to a printed circuit overlay or a voltage chain.	Part F
Hand Wire-Wrap Tool	IBM 6072438	A manual, squeeze-type wire-wrap tool used to wire-wrap SMS card socket terminals.	Part G
Wrapping Bit-22	Keller A-18632	Used with hand wire-wrap tool to wrap AWG22 wire.	Part H
Wrapping Bit-20	Keller A-18633	Used with hand wire-wrap tool to wrap AWG20 wire.	Part I
Wrapping Bit-24	Keller A-26232	Used with hand wire-wrap tool to wrap AWG24 wire.	Part J
Wrapping Bit-26	Keller A-27611	Used with hand wire-wrap tool to wrap AWG26 wire.	Part K
Sleeve - 26	Keller A-17611-2	Used with hand wire-wrap tool to wrap AWG24-26 wire.	Part L
Sleeve - 22, 24	Keller A-18840	Used with hand wire-wrap tool to wrap AWG22 wire.	Part M
Sleeve - 20	Keller A-18285	Used with hand wire-wrap tool to wrap AWG20 wire.	Part N

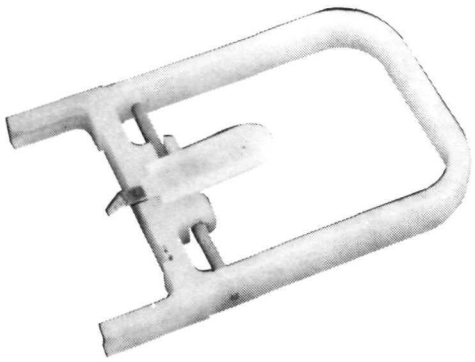
Figure 4-2. List of Recommended Special Tools (Sheet 1 of 3)

Name	Vendor Part No.	Application	Illustration Figure 4-3
Unwrap Tool	IBM 6072437	Used to unwrap both right and left-hand wraps.	Part O
Crimping Tool Kit	Bendix 11-7295	Used to crimp size 12, 16 and 20 type connector contacts.	Part P
Insertion Tool	Bendix 11-6781-16	Used to insert size 16 contacts in Bendix type connectors.	Part Q
Insertion Tool	Bendix 11-8107-20	Used to insert size 20 contacts in Bendix type connectors.	Part R
Contact Removing Tool Kit	Bendix 11-6900	Used to remove size 16 and 20 contacts in Bendix type connectors	Part S
Spanner Wrench	Bendix 11-3544	Used on Bendix type connector spanner nuts.	Part T
Connector Pliers	Bendix 6147-1	Used to hold knurled or serrated surfaces on Bendix type connectors	Part U
Crimping Tool	AMP 59501	Used to crimp AWG22-24 solid or stranded wire.	Part V
Crimping Tool	Berg HT-3-20	Used to crimp AWG20 solid or stranded wire to a slip-on terminal	Part W
Crimping Tool	Berg HT-3-22	Used to crimp AWG22 solid or stranded wire to a slip-on terminal.	Part X
Crimping Tool	Berg HT-3-24	Used to crimp AWG24 solid or stranded wire to a slip-on terminal.	Part Y
Attenuator Probe	Tektronix P-6017	General purpose probe with nine-foot cable terminating at a UHF connector.	Part Z
Current Probe	Tektronix P-6016	Special purpose probe used when monitoring current characteristics.	Part AA
Passive Termination	Tektronix 011-028	Used with the current probe when monitoring current characteristics.	Part AB

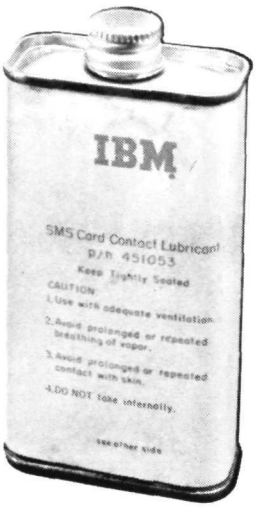
Figure 4-2. List of Recommended Special Tools (Sheet 2)

Name	Vendor Part No.	Application	Illustration Figure 4-3
Tool Case	IBM 6445032	Used for carrying and storing tools.	Part AC
Intercase	IBM 6445698	Used for carrying tools.	Part AD

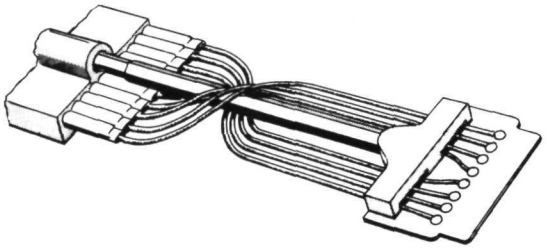
Figure 4-2. List of Recommended Special Tools (Sheet 3)



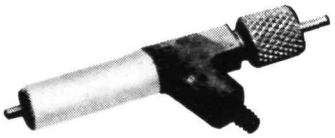
Part A. SMS Card Puller



Part B. SMS Card Contact Lubricant

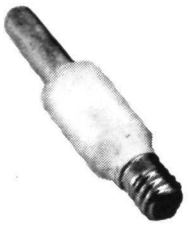


Part C. SMS Card Extender



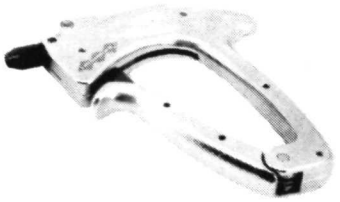
Part D. SMS Card Socket Terminal Extractor

Part E. Soldering Handle



Part F. Soldering Tip

Figure 4-3. Recommended Special Tools (Sheet 1 of 5)



Part G. Hand Wire-Wrap Tool

Part H. Wrapping Bit - 22

Part I. Wrapping Bit - 20

Part J. Wrapping Bit - 24

Part K. Wrapping Bit - 26

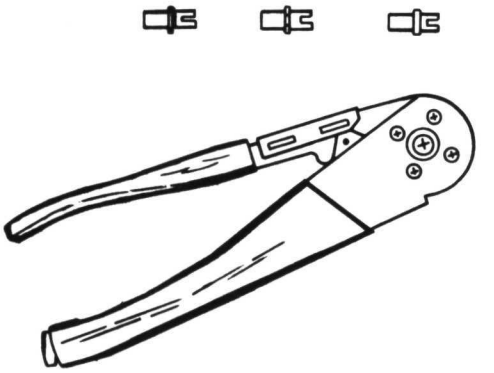
Part L. Sleeve - 26

Figure 4-3. Recommended Special Tools (Sheet 2)

Part M. Sleeve - 22, 24

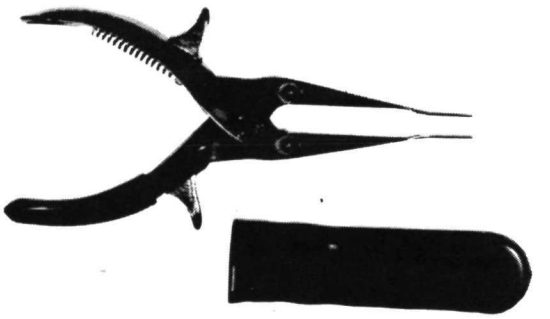
Part N. Sleeve - 20

Part O. Unwrap Tool



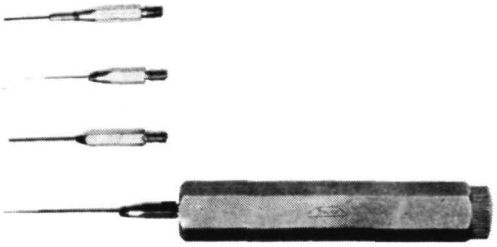
Part P. Crimping Tool Kit

Part Q. Insertion Tool

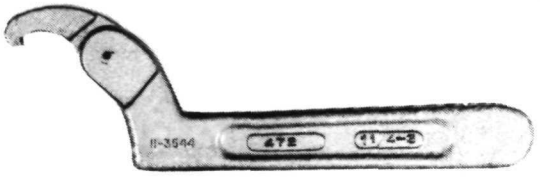


Part R. Insertion Tool

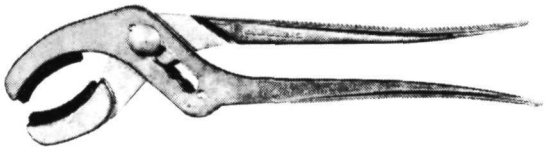
Figure 4-3. Recommended Special Tools (Sheet 3)



Part S. Contact Removing Tool Kit

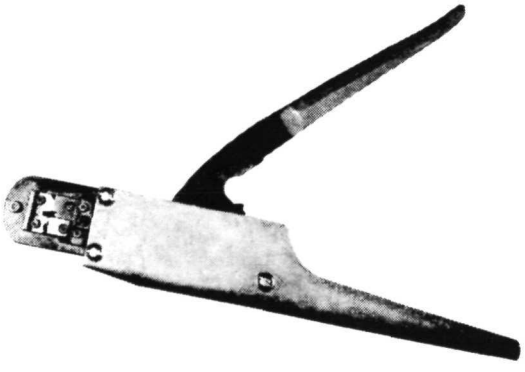


Part T. Spanner Wrench

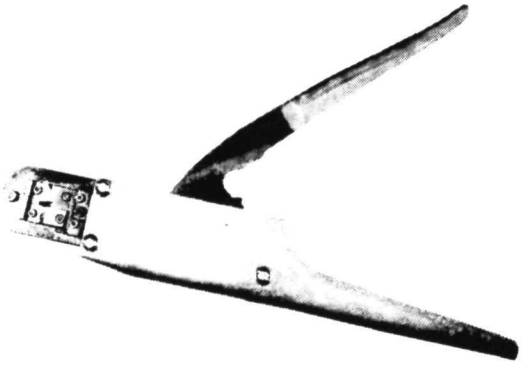


Part U. Connector Pliers

Part V. Crimping Tool

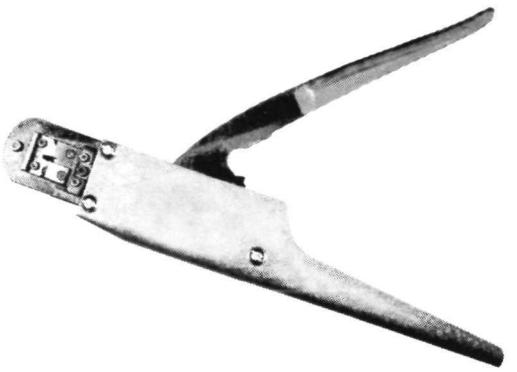


Part W. Crimping Tool



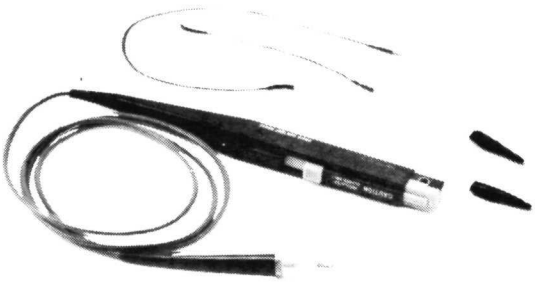
Part X. Crimping Tool

Figure 4-3. Recommended Special Tools (Sheet 4)



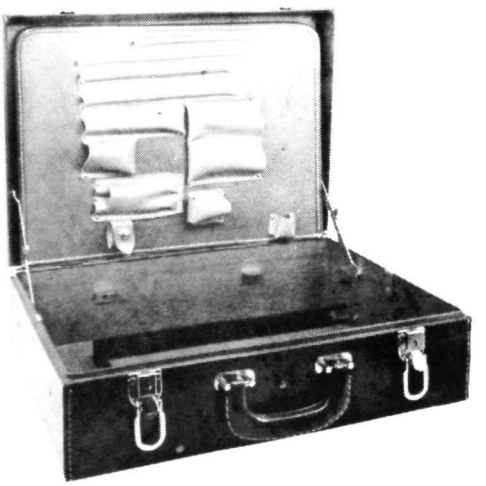
Part Y. Crimping Tool

Part Z. Attenuator Probe



Part AA. Current Probe

Part AB. Passive Termination



Part AC. Tool Case

Part AD. Intercase

Figure 4-3. Recommended Special Tools (Sheet 5)

SECTION V

PREPARATION FOR USE, STORAGE AND SHIPMENT

5-1. PREPARATION FOR USE.

5-2. UNPACKING.

5-3. The LVDCME is not packed for shipment. No unpacking is necessary.

5-4. ASSEMBLY.

5-5. The LVDCME is assembled before shipment. No assembling is necessary.

5-6. INSPECTION.

5-7. The LVDCME should be inspected for evidence of damage during shipment. Loose cables in the shipment should be checked against the following list:

IBM Part No.	IBM Part No.	IBM Part No.
6900035	6900056	6900073
6900052	6900057	6900085
6900053	6900058	6900086
6900054	6900059	6900087
6900055		6900088

5-8. INSTALLATION.

5-9. Refer to Volume I for installation instructions.

5-10. TESTS.

5-11. Before using the LVDCME to test a Computer, perform all calibration checks as described in Section VII.

5-12. PREPARATION FOR STORAGE.

5-13. Prepare the LVDCME for storage as follows:

a. Close all hinged panels and card gates.

b. Install connector dust caps on all connectors.

c. Cover LVDCME with dust cover.

d. Inventory cable assemblies as described in paragraph 5-7, then store cables in a carton near the electronic console.

5-14. PREPARATION FOR SHIPMENT.

5-15. Prepare the LVDCME for shipment as described in steps a, b, and c of paragraph 5-13.

SECTION VI

PREVENTIVE MAINTENANCE

6-1. INSPECTION.

6-2. DAILY INSPECTION.

6-3. There is no recommended daily inspection schedule for the LVDCME. However, if during daily use of the LVDCME exterior damage, obstruction to air flow, or deterioration or discoloration of panel markings is noted, repair the fault as described in Section IX.

6-3. PERIODIC MAINTENANCE.

6-4. Figures 6-1 through 6-4 prescribe the preventive maintenance schedule for the LVDCME. Due to the SMS card design of the LVDCME, preventive maintenance, except for the commercial assemblies, is held at a minimum. Figures 6-1 through 6-4 list the items to be inspected, the location of the item, the frequency at which the item shall be inspected, and the method of inspection and/or maintenance. Commerical manuals are referenced in these figures. Reference should be made to the list of related manuals for the complete title of the referenced manual.

ASSEMBLY LVDCME (6902000) General
REFERENCE MANUAL

PREVENTIVE MAINTENANCE SCHEDULE

ITEM	LOCATION	FREQUENCY	OBSERVE	CLEAN	LUBRICATE	NOTE
Furnace Type Filters	Bottom of Frames 01 and 02.	Monthly	Check for cleanliness.			Replace if deemed necessary.
Muffin Fans	Bottom of each gate assembly in and on top front of Frames 01 and 02.	Monthly	Check for any obvious faults such as noisy operation, wear, cleanliness, etc.			Clean or replace if deemed necessary.

Figure 6-1. LVDCME General Preventive Maintenance

ASSEMBLY Trygon Power Supplies (See below for assembly No's. and models)
REFERENCE MANUAL Trygon Instruction and Maintenance Manual

PREVENTIVE MAINTENANCE SCHEDULE

ITEM	LOCATION	FREQUENCY	OBSERVE	CLEAN	LUBRICATE	NOTE
Fan Motor	See pictorial representation of the inside of a supply in the back of the reference manual.	Monthly			Oil motor shaft at tubes on each end of motor. Use a light oil.	

The above preventive maintenance applies to the following assemblies:

1. Power Supply 01A8 (Trygon Model M15-10-0V)
2. Power Supply 02A4 (Trygon Model M36-5-0V)
3. Power Supply 02A5 (Trygon Model M15-5-0V)
4. Power Supply 02A9 (Trygon Model M15-10-0V)
5. Power Supply 02A10 (Trygon Model M15-5-0V)

Figure 6-2. Power Supplies (Trygon) Preventive Maintenance

ASSEMBLY Tape Reader 6901110 (Rheem Electronics Model RR1002-B-333, P/N 102300)
REFERENCE MANUAL Rheem TRM-306E

PREVENTIVE MAINTENANCE SCHEDULE

ITEM	LOCATION	FREQUENCY	OBSERVE	CLEAN	LUBRICATE	NOTE
Photocell Block	Front panel (See figure 4-7, page 19, No. 10 of reference manual).	Semi-weekly	Check for cleanliness of the glass slide, covering the aperture plate.	Use stiff bristle brush for general cleaning. Use a cotton swab and water, if necessary to remove foreign matter.		
Focusing Lens	Front panel (See figure 4-3, page 13, of reference manual).	Semi-weekly	Check for cleanliness.	Use same materials as above for any necessary cleaning.		
Jam and Drive Rollers	Front panel (See figure 4-1, page 12, of reference manual).	Semi-weekly	Check for wear or indentations on roller surfaces.	If necessary, clean by abrading surfaces with a soft eraser of the "Pink Pearl" type.		
Brake Shoes	Front panel (See figure 4-7, page 19, No. 4, of reference manual).	Semi-monthly	Check for accumulation of foreign matter that might tend to reduce braking force.	Clean with stiff bristle brush.		
Power Supply Voltages	See figures 4-5 and 4-6, pages 17 and 18, of reference manual for location of components and terminals listed under the "observe" column.	Monthly	Check and record all voltages listed below with the same voltmeter. Use the same voltmeter for each monthly test. A change in voltage may be indicative of a gradual component failure. A period of about 30 minutes should be allowed for warm up before the readings are taken. All voltage readings should be ±5%.			
Belt	See figure 4-6, page 18, No. 2, of reference manual.	Monthly	Check for wear or fraying of the belt which might cause slippage or an eventual break.			Replace if deemed necessary.

Voltage	From	To
-56V	C1, -terminal	TP1
-10V	F3, terminal 2	TP1
+4V	C1, +terminal	TP1

Figure 6-3. Tape Reader Assembly (01A3) Preventive Maintenance (Sheet 1 of 2)

ASSEMBLY Tape Reader 6901110 (Rheem Electronics Model RR1002-B-333, P/N 102300)
REFERENCE MANUAL Rheem TRM-306E

PREVENTIVE MAINTENANCE SCHEDULE

ITEM	LOCATION	FREQUENCY	OBSERVE	CLEAN	LUBRICATE	NOTE
Lamp	See figure 4-3, page 13, of reference manual.	*18 Months				Replace lamp and go through necessary adjustments and calibration as outlined in Sections 4.2.2, page 11, and 4.2.3, page 14, of reference manual.
Symmetry of Track Output	See figure 4-5, page 17, of reference manual for location of test points listed under the "Note" column.	When lamp above is replaced or a tape material changes.				Check the output of test points 1 and 2 for 45% on time (refer to Section 4.2.3 on Symmetry Adjustment in reference manual).

*This frequency is good only if the estimated reader on-time per week is ≤ 10 hours. If the reader on time per week (t) is estimated to be >10 hours, use the following formula to establish a different frequency:

$$\text{frequency (in weeks)} = \frac{4,060}{t + 42}$$

Figure 6-3. Tape Reader Assembly (01A3) Preventive Maintenance (Sheet 2)

ASSEMBLY Tape Spooler 6901120 (Rheem Electronics Model RS500A, P/N 102301)
REFERENCE MANUAL Rheem TSM-306A

PREVENTIVE MAINTENANCE SCHEDULE

ITEM	LOCATION	FREQUENCY	OBSERVE	CLEAN	LUBRICATE	NOTE
Warner Brake	See figure 4-7, page 20, of reference manual.	Monthly	See "Note" column first. Then inspect the brake lining and replace when excessively worn.	See "Note" column first. Then clean the brake lining.	See "Note" column first. Then coat both the brake disk and lining with a mixture of Molykote Type Z and one or two drops of light machine oil.	Remove the collar from the rear of each motor shaft, and slide the brake disk off.
Relay K1 Voltage	See figure 4-2, page 15, of reference manual.	Monthly				Check the voltage across the coil of Relay K1 in its operated state (refer to Section 4.2.3 on Relay Voltage Calibration in the reference manual).
Tension of the Tape Sensing Arm	See figure 4-5, page 18, No. 19, of reference manual.	Quarterly				Check the force on the Tape Sensing Arm at the end of the arm (refer to Section 4.2.1, page 12, on Adjustment of Tape Sensing Arm Tension in reference manual).
Gear in Drive Motor, M1	See figure 4-2, page 15, of reference manual.	Semi-Yearly			Apply one or two drops of 80 weight cling oil to each gear.	
Spring in Reel Retainer Housing		Semi-Yearly			Place a small amount of lubricant between the chambered section of the knob and the two locking pins: A small amount of light grade oil is also required on the inside surface of the knob.	

Figure 6-4. Tape Spooler Assembly (01A4) Preventive Maintenance

SECTION VII

CALIBRATION

7-1. GENERAL:

7-2. This section contains the calibration procedure for the LVDCME. The calibration procedure consists of (1) power checks and necessary adjustments, and (2) logic checks and necessary adjustments. The logic checks consist of manual and automatic (programmed) checks.

7-3. The calibration procedure shall be performed monthly. The procedure may be performed at any time for trouble isolation.

7-4. The procedure is presented in such a manner that the entire procedure may be performed in the sequence given, or any one check may be performed by itself.

7-5. The special test equipment specified in the procedure is listed in figure 4-1. The special test equipment shall be calibrated prior to use in accordance with the appropriate commercial manual.

7-6. If a failure occurs as evidenced by indications other than the normal indications listed, refer to the adjustment procedure where applicable or to trouble isolation in Section VIII.

7-7. The following abbreviations are used in the PANEL column of the figures containing the procedures:

Abbreviation	Definition
PC	POWER CONTROL panel
TRMC	TAPE READER AND MODE CONTROL panel
MLDD	MEMORY LOAD AND DATA DISPLAY panel
IE	INTERFACE EXERCISER panel
01A	Right-hand console, upper half
01B	Right-hand console, lower half
02A	Left-hand console, upper half
02B	Left-hand console, lower half

Cable Part Number	From	To
6900052	02A3J22	02A3J20
6900053	J18	J17
6900054	J15	J16
	J19	
6900055	J14	J13
6900056	J05	J08
6900057	J06	J09
6900058	J07	J10
6900059	J11	J12
6900073	J21	J23
6900085	01011J32	01A11J25
6900086	J31	J26
6900087	J30	J27
*6900075		J29

* 6900075 is a jumper plug

Figure 7-1. LVDCME Self-Check Cable Interconnections

7-8. SELF-CHECK CABLE CONNECTIONS.

7-9. The self-check cables shall be connected as listed in figure 7-1 prior to starting the calibration procedure.

7-10. POWER CHECKS.

7-11. PRIMARY POWER CHECKS.

7-12. The LVDCME primary power checks substantiate the following:

1. AC power circuits are functioning properly.

2. Interlocks listed in figure 7-2 are functioning properly.

3. Cooling fans are operational.

4. Power is applied to the ACME (LVDCME), COMP (computer), and MS (module switching) power supplies.

7-13. The LVDCME primary power checks are listed sequentially in figure 7-3.

7-14. SECONDARY POWER CHECKS.

7-15. The LVDCME secondary power checks substantiate the following:

1. LVDCME DC power is properly adjusted.

2. Correct power on sequencing is accomplished.

3. All panel lamps are operational.

7-16. The secondary power checks are listed sequentially in figure 7-4. If any of the measured values are not within the indicated limits, perform the corresponding adjustments in figure 7-19. After an adjustment is performed continue with the next step in figure 7-4.

7-17. COMPUTER POWER CHECKS.

7-18. The computer power checks substantiate that the voltages applied to the computer are adjusted properly and are applied in the correct sequence. Verification is also made that the loss of any computer voltage or the loss of ACME power will cause computer power to be cycled off.

7-19. The computer power checks are listed sequentially in figure 7-5. If any of the measured values are not within the indicated limits, perform the corresponding adjustments in figure 7-20. After an adjustment is performed continue with the next step in figure 7-5.

7-20. LOGIC CHECKS.

7-21. If the calibration is being started here, or if only one group of the logic checks is being performed and power is not on, perform the following steps:

1. Verify that all interlock switches are closed, the EMERGENCY PULL switch is reset (pushed-in), and that all circuit breakers located in end panel 01B11 are ON.

2. Verify that all AC ON and ON switches on the power supplies located at the rear of the LVDCME are at ON position.

3. Press and release MAIN POWER-POWER ON pushbutton/lamp (POWER CONTROL panel) and allow 15 minutes minimum for power supply warm-up. Note that MAIN POWER-POWER ON lamp lights; ϕA, ϕB, ϕC and FAN lamps light; MAIN POWER-POWER OFF lamp goes out; COMP POWER-SEQ OFF lamp lights; and ACME POWER-SEQ OFF lamp lights.

4. Press, hold (five seconds), and release ACME POWER-SEQ ON pushbutton/lamp. Note that ACME POWER-SEQ OFF lamp goes out and ACME POWER-SEQ ON lamp lights after a noticeable delay.

5. Press and release COMP POWER-SEQ ON pushbutton/lamp. Note that COMP POWER-SEQ OFF lamp goes out and COMP POWER-SEQ ON lamp lights after approximately 3 seconds delay.

7-22. The LVDCME must be initialized to insure that certain predetermined conditions exist prior to performing each group of the logic checks. The initialization procedure is contained in figure 7-6.

7-23. TAPE READER REGISTER CHECKS.

7-24. The tape reader register checks substantiate that the tape reader register can be loaded properly in the MANUAL mode. The tape reader register checks are listed sequentially in figure 7-7.

7-25. Each time a pushbutton/lamp is pressed in making a manual selection in the tape reader register, the TIMING TRCP lamp (IE panel) lights, and then goes out when the pushbutton/lamp is released. With each manual selection, if the sum total of lamps lit does not equal an odd number, the SERIALIZER-ACME PARITY BIT lamp shall light.

7-26. TAPE READER CLOCK AND CONTROL CHECKS.

7-27. The tape reader clock and control checks substantiate that the tape reader timing and the tape reader control circuits are functioning properly. The tape reader clock and control checks are listed sequentially in figure 7-8.

7-28. If any of the indicated results cannot be obtained, perform the tape reader clock adjustments in figure 7-21. After the adjustments are performed repeat the checks contained in figure 7-8.

7-29. AUTOMATIC SELF-CHECK AND TAPE READER CONTROLS CHECKS.

7-30. Automatic self-check and tape reader controls checks are accomplished by running the self-check tape. Successful running of the self-check tape substantiates that approximately 85% of the LVDCME logic circuits are functioning properly. The procedure for running the self-check tape is listed in figure 7-9. A listing of the contents of the self-check tape is contained in figure 7-26.

7-31. In the event of a failure, a detailed listing of the tape word instructions performed is contained in figure 7-27. Definitions of the instruction and operation codes used in figure 7-27 are contained in figure 7-28.

7-32. LVDCME SELF-CHECK TIMING CHECKS.

7-33. The LVDCME self-check timing checks substantiate that the self-check timing circuits are functioning properly. The LVDCME self-check timing checks are listed sequentially in figure 7-10.

7-34. If any of the indicated results cannot be obtained, perform the LVDCME self-check timing adjustments contained in figure 7-22. After the adjustments are performed repeat the checks contained in figure 7-10.

7-35. MEMORY TIMING CHECKS.

7-36. The memory timing checks substantiate that the memory timing marginal check circuits are functioning properly. The memory timing checks are listed sequentially in figure 7-11.

7-37. COMPUTER TEMPERATURE SENSING CHECKS.

7-38. The computer temperature sensing checks substantiate that computer power is cycled off if any of the computer temperature sensing circuits are activated. The computer temperature sensing checks are listed sequentially in figure 7-12.

7-39. If any of the indicated results cannot be obtained, perform the computer temperature sensing adjustments contained in figure 7-23. After the adjustments are performed repeat the checks contained in figure 7-12.

7-40. CHANNEL-MODULE SWITCHING CHECKS.

7-41. The channel-module switching checks substantiate that the channel and module switching feature of the LVDCME is functioning properly. The channel-module switching checks are listed sequentially in figure 7-13.

7-42. SINGLE-STEP CHECKS.

7-43. The single-step checks substantiate that the single-step feature of the LVDCME is functioning properly. The single-step checks are listed sequentially in figure 7-14.

7-44. PAST HISTORY MODE CHECKS.

7-45. The past history mode checks substantiate that the history storage feature of the LVDCME is functioning properly. The past history mode checks are listed sequentially in figure 7-15.

7-46. If any of the indicated results cannot be obtained, perform delay lines 1, 2, and 3 adjustments contained in figure 7-24. After the adjustments are performed repeat the checks contained in figure 7-15.

7-47. DATA REGISTER CHECKS.

7-48. The data register checks substantiate that the data registers can be loaded properly. The data register checks are listed sequentially in figure 7-16.

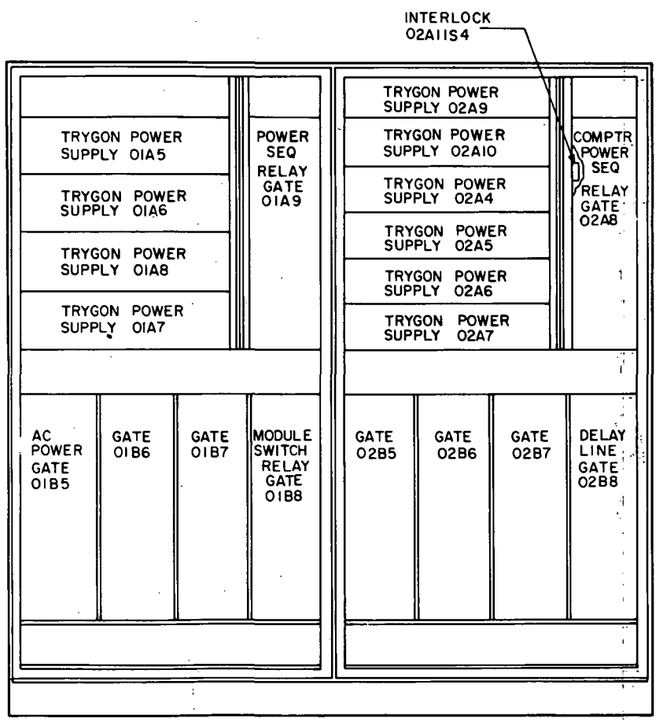
7-49. HALT CHECKS.

7-50. The halt checks substantiate that the halt feature of the LVDCME is functioning properly. The halt checks are listed sequentially in figure 7-17.

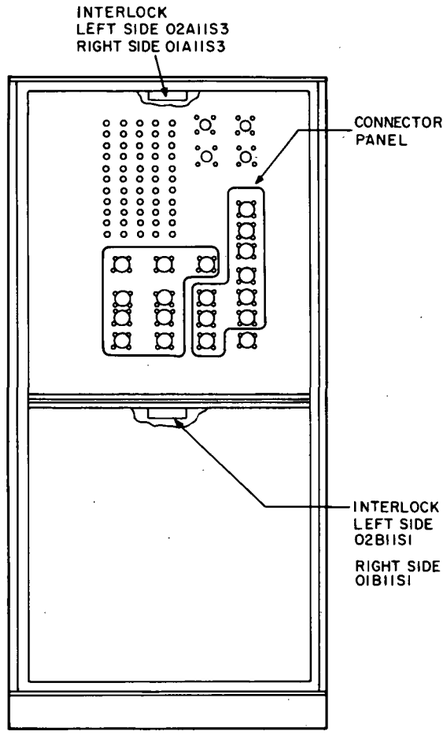
7-51. If any of the indicated results cannot be obtained perform the halt adjustments listed in figure 7-25. After the adjustments are performed repeat the checks contained in figure 7-17.

7-52. INTERRUPT CHECKS.

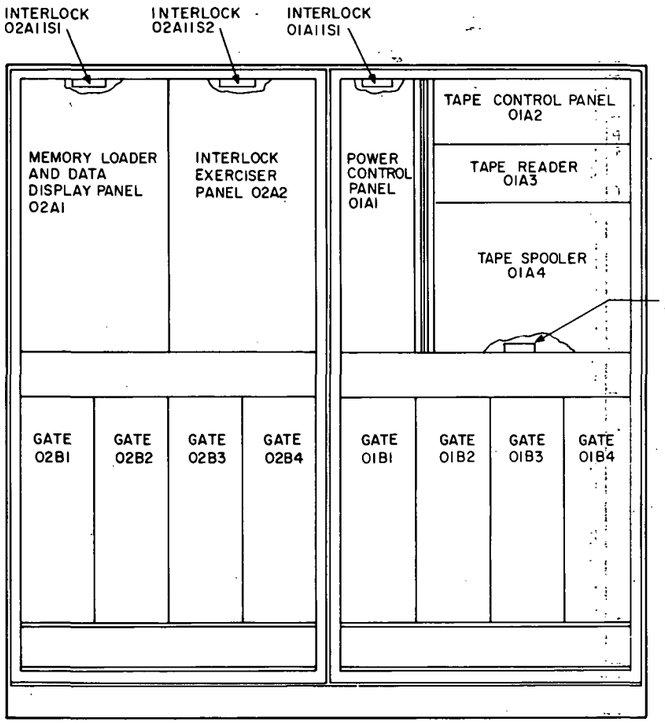
7-53. The interrupt checks substantiate that the LVDCME interrupt circuits are functioning properly. The interrupt checks are listed sequentially in figure 7-18.



REAR VIEW



LEFT END VIEW



FRONT VIEW

Figure 7-2. LVDCME Interlocks Locations

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	02A3 & 9020	Verify that all self check cables are installed except J29 on Panel 9020 install jumper plug	Installed	_____
20	01B5	Connect 3 phase AC power to the unit		
30	01B11	Remove end panel 01B11		
31	01B11	Verify/Set all circuit breakers	ON	_____
32	01B11	Record Elapsed Time (ETI)	Elapsed Time	_____
33	01B11	Install End Panel 01B11		
40	PC	Press EMERGENCY PULL switch to the reset (in) position		
50	PC	POWER OFF Lamp	ON	_____
51	01B11	Remove End Panel 01B11		
60	PC	POWER OFF Lamp	OFF	_____
70	01B11	Install End Panel 01B11		
80	PC	POWER OFF Lamp	ON	_____
90	MLDD	Open Door 02A11 MLDD		
100	PC	POWER OFF Lamp	OFF	_____
110	MLDD	Close Door 02A11 MLDD		
120	PC	POWER OFF Lamp	ON	_____
130	IE	Open Door 02A11 IE		
140	PC	POWER OFF Lamp	OFF	_____
150	IE	Close Door 02A11 IE		
160	PC	POWER OFF Lamp	ON	_____
170	02A11	Remove End Panel 02A11		
180	PC	POWER OFF Lamp	OFF	_____
190	02A11	Install End Panel 02A11		
200	PC	POWER OFF Lamp	ON	_____
210	TR	Open Tape Spooler Drawer 01A11		
220	PC	POWER OFF Lamp	OFF	_____
230	TR	Close Tape Spooler Drawer		
240	PC	POWER OFF Lamp	ON	_____
250	01A11	Remove End Panel 01A11		
260	PC	POWER OFF Lamp	OFF	_____
270	01A11	Install End Panel 01A11		
280	PC	POWER OFF Lamp	ON	_____
290	PC	Open Power Control door 01A11		
300	PC	POWER OFF LAMP	OFF	_____
310	PC	Close Power Control Door		
320	PC	POWER OFF Lamp	ON	_____
330	02B11	Remove End Panel 02B11		
340	PC	POWER OFF Lamp	OFF	_____

A B C D E F G H I J K L M N O P Q R | PAGE 8 | OF | PAGES | NUMBER A- 64-385-9414

X

Figure 7-3. Primary Power Checks (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER			UNIT NO. 6902000	
STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
350	02B11	Install End Panel 02B11		
360	PC	POWER OFF Lamp	ON	_____
370	02A08	Open Computer Power Sequence Relay Gate		

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Figure 7-3. Primary Power Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
380	PC	POWER OFF lamp	OFF	
390	02A08	Close Computer Power Seq. Relay Gate		
400	PC	POWER OFF lamp	ON	
410	PC	Pull EMERGENCY PULL switch		
420	PC	POWER OFF lamp	OFF	
430	PC	Press EMERGENCY PULL switch		
440	PC	POWER OFF lamp	ON	
450	PC	Press and release POWER ON		
460	PC	POWER OFF lamp	OFF	
470	PC	POWER ON lamp	ON	
480	PC	Phase A, B, C and FAN lamps	ON	
490	PC	COMP POWER SEQ OFF lamp	ON	
500	PC	ACME Power Seq. Off lamp	ON	
510	PC	Press and release POWER OFF		
520	PC	All lamps except POWER OFF lamp	OFF	

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Figure 7-3. Primary Power Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
Note		If any of the following measured values do not conform to values in the Normal Indication column, make correpsonding adjustments in Para. 2.1 in the Adjustment Procedure return to the next step in this procedure.		
10	PC	Press and release POWER ON		
20	PC	POWER ON lamp	ON	
30	PC	POWER OFF lamp	OFF	
40	PC	Phase A, B, C, and Fan lamps	ON	
50		Verify 15 minute warm-up ACME and COMPUTER DC voltages are measured using a Diff. DC voltmeter		
60	PC	Measure and record voltage between -26.5 V DC and GND	-26.47 to -26.53 VDC	
70	PC	Measure and record voltage between +12 VDC and GND	+11.98 to +12.05 VDC	
80	PC	Measure and record voltage between -12VDC and GND	-11.98 to -12.10 VDC	
90	PC	Measure and record voltage between -6 VDC and GND	-5.99 to -6.05 VDC	
100	PC	Press (hold 5 seconds) and release ACME POWER SEQ ON		
110	PC	ACME POWER SEQ OFF lamp	OFF	
120	PC	ACME POWER SEQ ON lamp (delayed)	ON	
NOTE		Press and release LAMP TEST on MLDD, IE, or TRMC if ON		
130		All LAMP TEST lamps	OFF	
140	TRMC	PWR ON lamp (press and release if ON)	OFF	
150	PC	COMPUTER TEMP NORMAL lamp	ON	
160	01B3	Open gate 01B3		
170	01B3	Measure and record voltage at gate 01B3 between TB1-7 and TB1-2 (gnd)	-11.82 to -12.12 VDC	
180	01B3	Measure and record voltage at gate 01B3 between TB1-6 and TB1-2(gnd)	-5.88 to -6.065 VDC	
190	01B3	Measure and record voltage at gate 01B3 between TB1-4 and TB1-2 (gnd)	+11.92 to +12.07 VDC	

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Figure 7-4. Secondary Power Checks (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
200	01B3	Close gate 01B3		
210	01B8	Open gate 01B8		
220	01B8	Measure and record voltage at gate 01B8 TB-IE to TB2-1A	-25.69 to -26.53 VDC	
230	01B8	Close gate 01B8		
240	MLDD	Press and release LAMP TEST		
250	MLDD	All lamps in the Instruction Address and Data Address areas	ON	
260	IE	Press and release LAMP TEST		
270	MLDD	All lamps on MLDD panel	ON	
280	IE	All lamps on IE panel except ERROR RESET, PIO REPEAT and RESET.	ON	
290	TRMC	Press and release LAMP TEST		
300	TRMC	All lamps on TRMC panel except ERROR DEVICES TEST	ON	
310	PC	All lamps on PC panel	ON	
320	MLDD	Press and release LAMP TEST		
330	TRMC	Press and release LAMP TEST		
340	IE	Press and release LAMP TEST		
350	PC	Press and release ACME POWER SEQ OFF		
360	PC	ACME POWER SEQ ON lamp	OFF	
370	PC	ACME POWER SEQ OFF lamp	ON	
380	01A9	Open gate 01A9		
390	01A9	Remove relay K 17		
400	PC	Press (hold 5 seconds) and release ACME POWER SEQ ON		
410	PC	ACME POWER SEQ ON lamp	OFF	
420	PC	ACME POWER SEQ OFF lamp	OFF	
430	TRMC	Press and release LAMP TEST		
440	PC	ACME POWER SEQ ON lamp	ON	
450	TRMC	Press and release LAMP TEST		
460	PC	Press and release ACME POWER SEQ OFF		
470	PC	ACME POWER SEQ OFF lamp	ON	
480	01A9	Replace relay K 17		
490	01A9	Close 01A9 gate		

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Figure 7-4. Secondary Power Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
NOTE		If any of the following measured values do not conform to value in the Normal Indication column, make corresponding adjustments in Para. 2.2 in the Adjustment Procedure and return to the next step in this procedure.		
10	PC	Measure and record voltage between +20 VDC and RET	+19.985 to +20.015VDC	
20	PC	Measure and record voltage between +12 VDC and RET	+11.99 to +12.01 VDC	
30	PC	Measure and record voltage between + 6 VDC and RET	+5.99 to +6.01 VDC	
40	PC	Measure and record voltage between -3 VDC and RET	-2.995 to -3.005 VDC	
50	PC	Measure and record voltage between +12 MS and RET	+11.99 to +12.01 VDC	
60	PC	Measure and record voltage between +6 MS and RET	+6.005 to +6.025 VDC	
70	PC	Press (hold 5 seconds) and release ACME POWER SEQ ON		
80	PC	ACME POWER SEQ OFF lamp	OFF	
90	PC	ACME POWER SEQ ON lamp (delayed)	ON	
100	PC	Press and release COMPUTER POWER SEQ ON		
110	PC	COMPUTER POWER SEQ OFF lamp	OFF	
120	PC	COMPUTER POWER SEQ ON lamp (delayed)	ON	
130	02A3	Disconnect self check cable 02A3J8		
140	PC	COMPUTER POWER SEQ ON lamp	OFF	
150	02A3	Reconnect 02A3J8		
160	PC	Press and release COMPUTER POWER SEQ ON		
170	PC	COMPUTER POWER SEQ ON lamp	ON	
180	02A3	Disconnect self check cable 02A3J9		
190	PC	COMPUTER POWER SEQ ON lamp	OFF	
200	02A3	Reconnect cable 02A3J9		
210	PC	Press and release COMPUTER POWER SEQ ON		
220	PC	COMPUTER POWER SEQ ON lamp	ON	

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Figure 7-5. Computer Power Checks (Sheet 1 of 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
230	02A3	Disconnect self check cable 02A3J10		
240	PC	COMPUTER POWER SEQ ON lamp	OFF	
250	02A3	Reconnect cable 02A3J10		
260	PC	Press and release COMPUTER POWER SEQ ON		
270	PC	COMPUTER POWER SEQ ON lamp	ON	
280	02A3	Disconnect self check cable 02A3J12		
290	PC	COMPUTER POWER SEQ ON lamp	OFF	
300	02A3	Reconnect cable 02A3J12		
310	PC	Press and release COMPUTER POWER SEQ ON		
320	PC	COMPUTER POWER SEQ ON lamp	ON	
330	02A3	Disconnect self check cable 02A3J13		
340	PC	COMPUTER POWER SEQ ON lamp	OFF	
350	02A3	Reconnect cable 02A3J13		
355	PC	Press and release COMPUTER POWER SEQ ON		
360	PC	COMPUTER POWER SEQ ON lamp	ON	
370	02A3	Disconnect self check cable 02A3J16		
380	PC	COMPUTER POWER SEQ ON lamp	OFF	
390	02A3	Reconnect cable 02A3J16		
400	PC	Press and release COMPUTER POWER SEQ ON		
410	PC	COMPUTER POWER SEQ ON lamp	ON	
420	02A3	Disconnect self check cable 02A3J17		
430	PC	COMPUTER POWER SEQ ON lamp	OFF	
440	02A3	Reconnect cable 02A3J17		
450	PC	Press and release COMPUTER POWER SEQ ON		
460	PC	COMPUTER POWER SEQ ON lamp	ON	
470	02A3	Disconnect self check cable 02A3J20		
480	PC	COMPUTER POWER SEQ ON lamp	OFF	
490	02A3	Reconnect cable 02A3J20		
500	PC	Press and release COMPUTER POWER SEQ ON		
510	PC	COMPUTER POWER SEQ ON lamp	ON	
520	PC	Measure and record voltage between TP20 and TP36 (Ret)	-2.95 to -3.01 VDC	

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Figure 7-5. Computer Power Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
530	PC	Measure and record voltage between TP 21 and TP 36 (Ret)	-2.97 to -3.00 VDC	
540	PC	Measure and record voltage between TP 22 and TP 36 (Ret)	-2.965 to -3.05 VDC	
550	PC	Measure and record voltage between TP 23 and TP 36 (Ret)	+5.94 to +6.00 VDC	
560	PC	Measure and record voltage between TP 24 and TP 36 (ret)	+5.94 to +6.00 VDC	
570	PC	Measure and record voltage between TP 25 and TP 36 (Ret)	+5.98 to +6.05 VDC	
580	PC	Measure and record voltage between TP 26 and TP 36 (Ret)	+11.94 to +12.00 VDC	
590	PC	Measure and record voltage between TP 27 and TP 36 (Ret)	+11.955 to +12.05 VDC	
600	PC	Measure and record voltage between TP 28 and TP 36 (Ret)	+11.95 to +12 05 VDC	
610	PC	Measure and record voltage between TP 29 and TP 36 (Ret)	+19.98 to +20.09 VDC	
620	PC	Measure and record voltage between TP 30 and TP 36 (Ret)	+19.90 to +20.01 VDC	
630	PC	Measure and record voltage between TP 31 and TP 36 (Ret)	+19.90 to +20.01 VDC	
640	PC	Measure and record voltage between TP 32 and TP 36 (Ret)	+19.87 to +19.99 VDC	
650	PC	Measure and record voltage between TP 33 and TP 36 (Ret)	+19.87 +19.99 VDC	
660	02A	OPEN access panel to Computer Power Supplies		
670	02A7	Record - 3V current	3.0 to 3.8A	
680	02A6	Record - 6V current	10 to 12A	
690	02A5	Record - 12V current	1.4 to 1.8A	
700	02A4	Record +20 V current	0.9 to 1.2A	
EXP		Power Supply Interlock Check		
710	02A7	Turn Power (toggle) switch to OFF on -3V Computer Supply		
720	PC	COMPUTER POWER SEQ ON lamp	OFF	
730	02A7	Turn Power (toggle) switch to ON on -3V Computer Supply		

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Figure 7-5. Computer Power Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
740	PC	Press and release COMPUTER POWER SEQ ON		
750	PC	COMPUTER POWER SEQ ON lamp	ON	
760	02A6	Turn Power (toggle) switch to OFF on +6V Computer Supply		
770	PC	COMPUTER POWER SEQ ON lamp	OFF	
780	02A6	Turn Power (toggle) switch to ON on +6V Computer Supply		
790	PC	Press and release COMPUTER POWER SEQ ON		
800	PC	COMPUTER POWER SEQ ON lamp	ON	
810	02A5	Turn Power (toggle) switch to OFF on +12V Computer Supply		
820	PC	COMPUTER POWER SEQ ON lamp	OFF	
830	02A5	Turn Power (toggle) switch to ON on +12V Computer Supply		
840	PC	Press and release COMPUTER POWER SEQ ON		
850	PC	COMPUTER POWER SEQ ON lamp	ON	
860	02A4	Turn Power (toggle) switch to OFF on +20V Computer Supply		
870	PC	COMPUTER POWER SEQ ON lamp	OFF	
880	02A4	Turn Power (toggle) switch ON on +20 V Computer Supply		
890	PC	Press and release COMPUTER POWER SEQ ON		
900	PC	COMPUTER POWER SEQ ON lamp	ON	
910	TRMC	Press and release LAMP TEST		
920	PC	COMPUTER POWER SEQ OFF lamp	ON	
930	TRMC	Press and release LAMP TEST		
940	PC	COMPUTER POWER SEQ OFF lamp	OFF	
950	PC	Press and release ACME POWER SEQ OFF		
960	PC	COMPUTER POWER SEQ OFF lamp	ON (delayed)	
970	PC	Press and release COMPUTER POWER SEQ ON		
980	PC	COMPUTER POWER SEQ ON lamp	ON (delayed)	

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Figure 7-5. Computer Power Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	IE	LAMP TEST lamp (Press and release if ON)	OFF	
15	MLDD	LAMP TEST lamp (Press and release if ON)	OFF	
20	TRMC	LAMP TEST lamp (Press and release if ON)	OFF	
25	TRMC	MANUAL lamp (Press and release AUTO/MANUAL if OFF)	ON	
30	TRMC	FREE RUN SS lamp (Press and release if ON)	OFF	
35	TRMC	FREE RUN READER lamp (Press and release if ON)	OFF	
40	TRMC	ADV CTR lamp (Press and release if ON)	OFF	
45	TRMC	SEL ADR lamp	ON	
50	TRMC	"1" lamp (Press and release if ON)	OFF	
60	TRMC	POWER ON (Press and release if ON)	OFF	
65	TRMC	POWER OFF lamp	ON	
70	TRMC	Quadrant ADR 1 lamp (Press and release if ON)	OFF	
80	TRMC	Quadrant ADR 2 lamp (Press and release if ON)	OFF	
90	TRMC	Quadrant ADR 3 lamp (Press and release if ON)	OFF	
100	TRMC	Quadrant ADR 4 lamp (Press and release if ON)	OFF	
110	TRMC	Quadrant ADR 5 lamp (Press and release if ON)	OFF	
EXP		If both INV ERR and ADR 6 lamps are OFF, omit steps 120 through 180		
120	TRMC	Press and release ADR 1 lamp	ON	
130	TRMC	Press and release ADR 2 lamp	ON	
140	TRMC	Press and release ADR 3 lamp	ON	
150	TRMC	INV ERR	OFF	
160	TRMC	Press and release ADR 1 lamp	OFF	
170	TRMC	Press and release ADR 2 lamp	OFF	
175	TRMC	ADR 6 lamp	OFF	
180	TRMC	Press and release ADR 3 lamp	OFF	

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Figure 7-6. Initialization Procedure (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
EXP		If all of the word counter lamps 2_0 through 2-12 are OFF, omit steps 190 through 220		
190	TRMC	Press and release ADV CTR/SEL ADR		
191	TRMC	ADV. CTR	ON	
200	TRMC	Continually press and release each word counter until all quadrants in all lamps are off starting with the lowest order lamp in the counter which is on.		
210	TRMC	All word counter lamps	OFF	
220	TRMC	Press and Release ADV CTR/SEL ADR		
230	TRMC	SEL ADR	ON	
240	IE	Position PHASE switch to NONE		
250	IE	Position BIT GATE switch to NONE		
260	IE	Position CLOCK switch to NONE		
270	IE	MANUAL HALT lamp (Press and release if OFF)	ON.	
280	IE	OP lamp (Press and release if ON)	OFF	
285	IE	TP lamp	ON	
290	IE	I/O Reg. No. 1 lamp (Press and release if ON)	OFF	
300	IE	Press and release RESET		
310	IE	All I/O Reg. No. 2 lamps	OFF	
320	IE	Press and release I/O Reg. No. 1 lamp	ON	
330	IE	Press and release RESET		
340	IE	All I/O Reg. No. 1 lamps	OFF	
350	IE	Press and release ERROR RESET		
360	IE	All ERROR lamps (Except COMPTR ALARM)	OFF	
380	MLDD	Position DISPLAY SELECT switch to NONE		
390	MLDD	Position WORD switch to T		
400	MLDD	ERROR OVER RIDE lamp (Press and Releease if ON)	OFF	
410	MLDD	DISPLAY SERIAL OUT lamp (Press and release if ON)	OFF	
420	MLDD	MEMORY LOADER REPEAT lamp (Press and release if ON)	OFF	

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Figure 7-6. Initialization Procedure (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	MLDD	Press and release DS 1		
20	MLDD	COMMAND DS 1 lamp	ON	
30	MLDD	Press and release DS 2		
40	MLDD	COMMAND DS 2 lamp	ON	
50	MLDD	Press and release DS 3		
60	MLDD	COMMAND DS 3 lamp	ON	
70	MLDD	Press and release DS 4		
80	MLDD	COMMAND DS 4 lamp	ON	
90	MLDD	Press and release DM 1		
100	MLDD	COMMAND DM 1 lamp	ON	
110	MLDD	Press and release DM 2		
120	MLDD	COMMAND DM 2 lamp	ON	
130	MLDD	Press and release DATA ADDRESS COMMAND DX/SX		
140	MLDD	DATA ADDRESS COMMAND DX lamp	ON	
150	MLDD	DATA ADDRESS COMMAND SX lamp	OFF	
160	MLDD	Press and release OP 4		
170	MLDD	COMMAND OP 4 lamp	ON	
180	MLDD	Press and release OP 3		
190	MLDD	COMMAND OP3 lamp	ON	
200	MLDD	Press and release OP 2		
210	MLDD	COMMAND OP 2 lamp	ON	
220	MLDD	Press and release OP 1		
230	MLDD	COMMAND OP 1 lamp	ON	
240	MLDD	Press and release DM 3		
250	MLDD	COMMAND DM 3 lamp	ON	
260	MLDD	Press and release DM 2		
270	MLDD	COMMAND DM 2 lamp	OFF	
280	MLDD	Press and release DM 1		
290	MLDD	COMMAND DM 1 lamp	OFF	
300	MLDD	Press and release DS 4		
310	MLDD	COMMAND DS 4 lamp	OFF	
320	MLDD	Press and release DS 3		
330	MLDD	COMMAND DS 3 lamp	OFF	
340	MLDD	Press and release DS 2		
350	MLDD	COMMAND DS 2 lamp	OFF	
360	MLDD	Press and release DS 1		
370	MLDD	COMMAND DS 1 lamp	OFF	
380	MLDD	Press and release 0A4		
390	MLDD	COMMAND 0A4 lamp	ON	

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Figure 7-7. Tape Reader Register Checks (Sheet 1 of 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
400	MLDD	Press and release OA5		
410	MLDD	COMMAND OA5 lamp	ON	
420	MLDD	Press and release OA6		
430	MLDD	COMMAND OA6 lamp	ON	
440	MLDD	Press and release OA7		
450	MLDD	COMMAND OA7 lamp	ON	
460	MLDD	Press and release OA8		
470	MLDD	COMMAND 0A8 lamp	ON	
480	MLDD	Press and release 0A9		
490	MLDD	COMMAND 0A9 lamp	ON	
500	MLDD	Press and release Data Address Command DX/SX		
510	MLDD	Data Address COMMAND DX lamp	OFF	
520	MLDD	Data Address COMMAND SX lamp	ON	
530	MLDD	Press and release OP 4		
540	MLDD	COMMAND OP 4 lamp	OFF	
550	MLDD	Press and releae OP 3		
560	MLDD	COMMAND OP 3 lamp	OFF	
570	MLDD	Press and release OP 2		
580	MLDD	COMMAND OP 2 lamp	OFF	
590	MLDD	Press and release OP 1		
600	MLDD	COMMAND OP 1 lamp	OFF	
610	MLDD	Press and release DM 3		
620	MLDD	COMMAND DM 3 lamp	OFF	
		NOTE: COMMAND SIGN thru DATA 12 switches will cause SYL 1 Parity BIT lamp to go ON & OFF.		
630	MLDD	Press and release DATA 2		
640	MLDD	COMMAND DATA 2 lamp	ON	
650	MLDD	Press and release DATA 1		
660	MLDD	DATA COMMAND 1 lamp	ON	
670	MLDD	Press and releae DATA SIGN		
680	MLDD	DATA COMMAND SIGN lamp	ON	
690	MLDD	Press and release 0A1		
700	MLDD	COMMAND 0A1 lamp	ON	
710	MLDD	Press and release 0A2		
720	MLDD	COMMAND 0A2 lamp	ON	

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Figure 7-7. Tape Reader Register Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MAUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
730	MLDD	Press and release 0A3		
740	MLDD	COMMAND 0A3 lamp	ON	
750	MLDD	Press and release 0A4		
760	MLDD	COMMAND 0A4 lamp	OFF	
770	MLDD	Press and release 0A5		
780	MLDD	COMMAND 0A5 lamp	OFF	
790	MLDD	Press and release 0A6		
800	MLDD	COMMAND 0A6 lamp	OFF	
810	MLDD	Press and release 0A7		
820	MLDD	COMMAND 0A7 lamp	OFF	
830	MLDD	Press and release 0A8		
840	MLDD	COMMAND 0A8 lamp	OFF	
850	MLDD	Press and release 0A9		
860	MLDD	COMMAND 0A9 lamp	OFF	
870	MLDD	Press and release DATA 8		
880	MLDD	DATA COMMAND 8 lamp	ON	
890	MLDD	Press and release DATA 7		
900	MLDD	DATA C OMMAND 7 lamp	ON	
910	MLDD	Press and release DATA 6		
920	MLDD	DATA COMMAND 6 lamp	ON	
930	MLDD	Press and release DATA 5		
940	MLDD	DATA COMMAND 5 lamp	ON	
950	MLDD	Press and release DATA 4		
960	MLDD	DATA COMMAND 4 lamp	ON	
970	MLDD	Press and release DATA 3		
980	MLDD	DATA COMMAND 3 lamp	ON	
990	MLDD	Press and release DATA 2		
1000	MLDD	DATA COMMAND 2 lamp	OFF	
1010	MLDD	Press and release DATA 1		
1020	MLDD	DATA COMMAND 1 lamp	OFF	
1030	MLDD	Press and release D ATA SIGN		
1040	MLDD	DATA COMMAND SIGN lamp	OFF	
1050	MLDD	Press and release 0A1		
1060	MLDD	COMMAND 0A1 lamp	OFF	
1070	MLDD	Press and release 0A2		
1080	MLDD	COMMAND 0A2 lamp	OFF	
1090	MLDD	Press and release 0A3		
1100	MLDD	COMMAND 0A3 lamp	OFF	
		NOTE: COMMAND DATA 13 thru DATA 25 switch will cause SYL 0 PARITY BIT lamp to go ON & OFF		

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Figure 7-7. Tape Reader Register Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
Note		COMMAND DATA 13 through DATA 25 switch will cause SYL0 parity bit lamp to go on and off.		
1110	MLDD	Press and release DATA 14		
1120	MLDD	DATA COMMAND 14 lamp	ON	
1130	MLDD	Press and release DATA 13		
1140	MLDD	DATA COMMAND 13 lamp	ON	
1150	MLDD	Press and release DATA 12		

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Figure 7-7. Tape Reader Register Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1160	MLDD	DATA COMMAND 12 lamp	ON	
1170	MLDD	Press and release DATA 11		
1180	MLDD	DATA COMMAND 11 lamp	ON	
1190	MLDD	Press and release DATA 10		
1200	MLDD	DATA COMMAND 10 lamp	ON	
1210	MLDD	Press and release DATA 9		
1220	MLDD	DATA COMMAND 9 lamp	ON	
1230	MLDD	Press and release DATA 8		
1240	MLDD	DATA COMMAND 8 lamp	OFF	
1250	MLDD	Press and release DATA 7		
1260	MLDD	DATA COMMAND 7 lamp	OFF	
1270	MLDD	Press and release DATA 6		
1280	MLDD	DATA COMMAND 6 lamp	OFF	
1290	MLDD	Press and release DATA 5		
1300	MLDD	DATA COMMAND 5 lamp	OFF	
1310	MLDD	Press and release DATA 4		
1320	MLDD	DATA COMMAND 4 lamp	OFF	
1330	MLDD	Press and release DATA 3		
1340	MLDD	DATA COMMAND 3 lamp	OFF	
1350	MLDD	Press and release DATA 20		
1360	MLDD	DATA COMMAND 20 lamp	ON	
1370	MLDD	Press and release DATA 19		
1380	MLDD	DATA COMMAND 19 lamp	ON	
1390	MLDD	Press and release DATA 18		
1400	MLDD	DATA COMMAND 18 lamp	ON	
1410	MLDD	Press and release DATA 17		
1420	MLDD	DATA COMMAND 17 lamp	ON	
1430	MLDD	Press and release DATA 16		
1440	MLDD	DATA COMMAND 16 lamp	ON	
1450	MLDD	Press and release DATA 15		
1460	MLDD	DATA COMMAND 15 lamp	ON	
1470	MLDD	Press and release DATA 14		
1480	MLDD	DATA COMMAND 14 lamp	OFF	
1490	MLDD	Press and release DATA 13		
1500	MLDD	DATA COMMAND 13 lamp	OFF	
1510	MLDD	Press and release DATA 12		
1520	MLDD	DATA COMMAND 12 lamp	OFF	
1530	MLDD	Press and release DATA 11		
1540	MLDD	DATA COMMAND 11 lamp	OFF	
1550	MLDD	Press and release DATA 10		
1560	MLDD	DATA COMMAND 10 lamp	OFF	

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Figure 7-7. Tape Reader Register Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1570	MLDD	Press and release DATA 9		
1580	MLDD	DATA COMMAND 9 lamp	OFF	
1590	MLDD	Press and release DATA 25		
1600	MLDD	DATA COMMAND 25 lamp	ON	
1610	MLDD	Press and release DATA 24		
1620	MLDD	DATA COMMAND 24 lamp	ON	
1630	MLDD	Press and release DATA 23		
1640	MLDD	DATA COMMAND 23 lamp	ON	
1650	MLDD	Press and release DATA 22		
1660	MLDD	DATA COMMAND 22 lamp	ON	
1670	MLDD	Press and release DATA 21		
1680	MLDD	DATA COMMAND 21 lamp	ON	
1690	TRMC	Press and release ADR 1 lamp	ON	
1700	TRMC	Press and release ADR 2 lamp	ON	
1705	TRMC	ADR 6 lamp	ON	
1710	TRMC	Press and release ADR 3 lamp	ON	
1720	TRMC	Press and release ADR 4 lamp	ON	
1730	TRMC	Press and release ADR 5 lamp	ON	
1740	MLDD	Press and release DATA 20		
1750	MLDD	DATA COMMAND 20 lamp	OFF	
1760	MLDD	Press and release DATA 19		
1770	MLDD	DATA COMMAND 19 lamp	OFF	
1780	MLDD	Press and release DATA 18		
1790	MLDD	DATA COMMAND 18 lamp	OFF	
1800	MLDD	Press and release DATA 17		
1810	MLDD	DATA COMMAND 17 lamp	OFF	
1820	MLDD	Press and release DATA 16		
1830	MLDD	DATA COMMAND 16 lamp	OFF	
1840	MLDD	Press and release DATA 15		
1850	MLDD	DATA COMMAND 15 lamp	OFF	
1860	MLDD	Press and release DATA 25		
1870	MLDD	DATA COMMAND 25 lamp	OFF	
1880	MLDD	Press and release DATA 24		
1890	MLDD	DATA COMMAND 24 lamp	OFF	
1900	MLDD	Press and release DATA 23		
1910	MLDD	DATA COMMAND 23 lamp	OFF	
1920	MLDD	Press and release DATA 22		
1930	MLDD	DATA COMMAND 22 lamp	OFF	
1940	MLDD	Press and release DM 2		
1950	MLDD	COMMAND DM 2 lamp	ON	
1960	MLDD	Press and release DM 1		
1970	MLDD	COMMAND DM 1 lamp	ON	

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Figure 7-7. Tape Reader Register Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1980	MLDD	Press and release DS 4		
1990	MLDD	COMMAND DS 4 lamp	ON	
2000	MLDD	Press and release DS 3		
2010	MLDD	COMMAND DS 3 lamp	ON	
2020	MLDD	Press and release DS 2		
2030	MLDD	COMMAND DS 2 lamp	ON	
2040	MLDD	Press and release DS 1		
2050	MLDD	COMMAND DS 1 lamp	ON	
2060	MLDD	Press and release DATA 21		
2070	MLDD	DATA COMMAND 21 lamp	OFF	
2080	TRMC	Press and release ADR 1 lamp	OFF	
2090	TRMC	Press and release ADR 2 lamp	OFF	
3000	TRMC	Press and release ADR 3 lamp	OFF	
3010	TRMC	Press and release ADR 4 lamp	OFF	
3020	TRMC	Press and release ADR 5 lamp	OFF	
3030	MLDD	Press and release DATA SIGN and DATA 1 through 25		
3040	MLDD	DATA COMMAND SIGN and COMMAND 1 through 25 lamps	ON	
3050	MLDD	Press and release 0A1 through 0A9		
3060	MLDD	COMMAND 0A1 through 0A9 lamps	ON	
3070	MLDD	Press and release OP 4 through OP 1		
3080	MLDD	COMMAND OP 4 through OP 1 lamps	ON	
3090	MLDD	Press and release DM 3		
4000	MLDD	COMMAND DM 3 lamp	ON	
4010	MLDD	Press and release DATA ADDRESS COMMAND DX/SX		
4020	MLDD	COMMAND DX lamp	ON	
4030	MLDD	COMMAND SX lamp	OFF	
4040	MLDD	Press and release COMMAND DISPLAY RESET		
4050	MLDD	DATA ADDRESS COMMAND DX lamp	OFF	
4060	MLDD	DATA ADDRESS COMMAND SX lamp	ON	
4070	MLDD	DATA COMMAND SIGN and COMMAND 1 through 25 lamps	OFF	
4080	MLDD	COMMAND 0A1 through 0A9 lamps	OFF	
4090	MLDD	COMMAND OP1 through OP4 lamps	OFF	
4100	MLDD	COMMAND DS 1 through DS 4 lamps	OFF	
4110	TRMC	Press and release ML/DD		
4120	TRMC	ML lamp	OFF	
4130	TRMC	DD lamp	ON	

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Figure 7-7. Tape Reader Register Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4140	MLDD	DATA lamp on DATA/INS switch (Press and release if ON)	OFF	
4150	MLDD	Press and release IM 3 through IM 1 and DX/SX		
4160	MLDD	COMMAND IM 3 through IM 1 and INSTR. ADDRESS COMMAND DX lamps	ON	
4170	MLDD	Press and release SYL O/I and IS 4 through IS 1		
4180	MLDD	COMMAND SYL 1 and IS 4 through IS 1 lamps	ON	
4190	MLDD	Press and release A8 through A1		
4200	MLDD	COMMAND A8 through A1 lamps	ON	
4210	MLDD	Press and release IM2, IM3, IM1, DX/SX, SLY O/1, IS4 through IS1 and A8 through A1		
4220	MLDD	COMMAND IM2, IM3, IM1, DX, SYL1, IS4 through IS1, and A8 through A1 lamps	OFF	
4230	MLDD	Press and release IM2, IM1, IM3, IS1, through IS4, A8 through A1, DX/SX and SYL O/1		
4240	MLDD	COMMAND IM2, IM1, IM3, IS1 through IS4, A8 through A1, DX and SYL 1 lamps	ON	
4250	MLDD	Press and release the ADDRESS COMPARE DATA/INS switch		
4260	MLDD	DATA lamp	ON	
4270	MLDD	COMMAND IM1 through IM3, IS1 through IS4, A8 through A1, DX and SYL 1 lamps	OFF	
4280	MLDD	Press and release IM3		
4290	MLDD	Verify that COMMAND IM3 lamp remains OFF	OFF	
4300	IE	Verify that TIMING TRCP lamp is ON when IM3 lamp is pressed and go OFF when IM3 is released	ON/OFF	
4310	MLDD	ACME PARITY BIT lamp	ON	
4320	MLDD	Press and release DATA/INS		
4330	MLDD	INS lamp	ON	
4340	MLDD	DATA lamp	OFF	

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Figure 7-7. Tape Reader Register Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	TRMC	Press and release ML/DD		
20	TRMC	ML lamp	ON	
30	TRMC	Press and release PWR ON/PWR OFF		
40	TRMC	PWR OFF lamp	OFF	
50	TRMC	PWR ON lamp	ON	
60	TRMC	Press and release PWR ON/PWR OFF		
70	TRMC	PWR OFF, FORWARD and STOP lamps	ON	
80	TRMC	PWR ON, MANUAL ADVANCE TAPE and REVERSE lamps	OFF	
90	TRMC	Press and release FREE RUN SS		
100	TRMC	FREE RUN SS lamp	ON	
110	IE	Press and release ERROR RESET		
120	IE	Verify TRCP lamp	OFF	
130	MLDD	Press and release IS 1		
140	IE	TRCP lamp	ON	
150	IE	Press and release ERROR RESET		
160	IE	TRCP lamp	OFF	
170	MLDD	Press and release IS 2		
180	IE	TRCP lamp	ON	
190	IE	Press and release ERROR RESET		
200	IE	TRCP lamp	OFF	
210	MLDD	Press and release IS 3		
230	IE	TRCP lamp	ON	
240	IE	Press and release ERROR RESET		
250	IE	TRCP lamp	OFF	
260	MLDD	Press and release IS 4		
280	IE	TRCP lamp	ON	
290	IE	Press and release ERROR RESET		
300	IE	TRCP lamp	OFF	
310	TRMC	Press and release AUTO/MANUAL		
320	TRMC	AUTO lamp	ON	
330	TRMC	MANUAL lamp	OFF	
340	IE	TRCP lamp	ON	
350	IE	Press and hold ERROR RESET		

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Figure 7-8. Tape Reader Check and Controls Check (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
360	IE	TRCP lamp	Flashing	
370	IE	Release ERROR RESET		
380	IE	TRCP lamp	ON	
390	TRMC	Press and release AUTO/MANUAL		
400	TRMC	MANUAL lamp	ON	
410	TRMC	AUTO lamp	OFF	
420	TRMC	Press and release FREE RUN SS		
430	TRMC	FREE RUN SS lamp	OFF	
440	TRMC	MANUAL ADVANCE TAPE lamp	OFF	
450	IE	Press and release ERROR RESET		
460	IE	TRCP lamp	OFF	
470	TRMC	Press and release PWR ON/PWR OFF		
480	TRMC	PWR OFF lamp	OFF	
490	TRMC	PWR ON lamp	ON	
500	TRMC	Photo lamp in Tape Read Head	ON	
510	MLDD	Press and hold IM3		
520	IE	TRCP lamp	ON	
530	MLDD	Release IM3		
540	IE	TRCP lamp	OFF	
550	TRMC	Press and release MANUAL ADVANCE TAPE		
560	TRMC	STOP lamp	OFF	
570	TRMC	Press and release AUTO/MANUAL		
580	TRMC	Press and release ML/DD		
590	TRMC	Press and release MEMORY SIM		
600	TRMC	Display will not change from step 560		
610	TRMC	Press and release FREE RUN SS		
620	TRMC	FREE RUN SS lamp	ON	
630	TRMC	PWR ON lamp	OFF	
640	TRMC	PWR OFF lamp	ON	
650	TRMC	STOP lamp	ON	
660	TRMC	MANUAL ADVANCE TAPE lamp	ON	
670	IE	TRCP lamp may now be either on or off		
680	TRMC	AUTO lamp	ON	
690	TRMC	MANUAL Lamp	OFF	
700	TRMC	Press and release FREE RUN SS		
710	TRMC	FREE RUN SS lamp	OFF	
720	TRMC	MANUAL ADVANCE TAPE lamp	OFF	

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Figure 7-8. Tape Reader Check and Controls Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
730	TRMC	Press and release PWR ON/PWR OFF		
740	TRMC	PWR ON/PWR OFF lamps	Unchanged	
750	TRMC	Press and release PWR ON/PWR OFF		
760	TRMC	PWR ON/PWR OFF lamps	Unchanged	
770	IE	Press and release ERROR RESET		
780	IE	TRCP lamp	OFF	
790	TRMC	PWR OFF lamp	OFF	
800	TRMC	PWR ON lamp	ON	
810	TRMC	START lamp	ON	
820	TRMC	Press and release AUTO/MANUAL		
830	TRMC	AUTO lamp	OFF	
840	TRMC	MANUAL lamp	ON	
850	TRMC	START lamp	OFF	
860	TRMC	Press and release FREE RUN READER		
870	TRMC	FREE RUN READER lamp	ON	
880	TRMC	The Right Capstain wheel is now touching the Right Drive Magnet on Tape Spooler		
890	TRMC	Press and release FORWARD/ REVERSE		
900	TRMC	FORWARD lamp	OFF	
910	TRMC	REVERSE lamp	ON	
920	TRMC	The Left Capstain wheel is now touching the Left Drive Magnet on the Tape Spooler		
930	TRMC	Press and release FREE RUN READER		
940	TRMC	FREE RUN READER lamp	OFF	
950	TRMC	The Left Capstain wheel is no longer touching the Drive Magnet.		
960	TRMC	Press and release FORWARD/ REVERSE		
970	TRMC	REVERSE lamp	OFF	
980	TRMC	FORWARD lamp	ON	
990	TRMC	Press and release PWR ON/PWR OFF		
1000	TRMC	PWR ON lamp	OFF	
1010	TRMC	PWR OFF lamp	ON	

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Figure 7-8. Tape Reader Check and Controls Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	Tape Spooler	Place reel with ACME self test tape on left spooler hub with edge of tape closest to sprocket holes toward the panel. The tape must feed upward off the left side of the reel.		
20		Place empty reel on right spooler hub.		
30		Assure that the tape guide on the front of the photocell block assembly is in its down position.		
40		Strip approximately six feet of tape off the left reel and thread spooler-reader as follows:		
50		Tape goes between the lower side fixed roller and non-rotating pin.		
60		Around the right side of the lower roller on the left tension arm		
70		Around the left side of the middle left fixed roller		
80		Around the right side of the upper roller on the left tension arm.		
90		Around the left side of the upper left fixed roller.		
100		Over the left tension spring on the reader		
110		Over the left roller on the reader		
120		Between the left capstan and pinch roller		
130		Through the slot in the left brake assembly		
140		Under the left pin, spring hold-down device and right pin of the photocell block assembly passing over the photocell under the spring hold-down device.		

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 1 of 15)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
150	Tape Spooler	Through the slot in the right brake assembly. Between the right capstand and pinch roller.		
170		Over the right roller on the reader.		
180		Over the right tenstion spring on the reader.		
190		Around the right side of the upper right fixed roller.		
200		Around the left side of the upper roller on the right tension arm.		
210		Around the right side of the middle right fixed roller.		
220		Around the left side of the lower roller on the right tension arm.		
230		Down between the lower right fixed roller and non-rotating pin.		
240		Down on the right side of the tape reel.		
250		Position the tape so that the leader portion following the punched title is over the photocell and raise the guide on the front of the photocell assembly		
260		Attach the tape to right reel taking up excess tape by rotating reel clockwise until right tension arm is located at the approximate center of its swing.		
270		Adjust tape tension on left side by rotating left reel until tension arm is located at the approximate center of its swing.		
280	TRMC	Press and release ERROR DEVICES TEST SWITCH. Except	All error lamps ILLEGAL PATH ON	
290	MLDD	Press and release COMPUTER DISPLAY RESET		
300	IE	Press and release ERROR RESET	All error lamps OFF	
301	IE	MANUAL MLC INH lamp (Press and release if ON)	OFF	
302	IE	MANUAL SSC INH lamp (Press and release if ON)	OFF	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 2)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
310	TRMC	Press and release PWR ON/PWR OFF	Power On - ON Power Off-OFF	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
320	TRMC	Press and release ADV CTR/SEL ADR	ADV CTR - ON SEL ADR -OFF	
330	IE	Press and release MANUAL HALT	OFF	
340		Allow five minutes for tape reader to warm up before proceeding.		
350	TRMC	Press and release MANUAL ADVANCE TAPE. Tape advances and stops after first tape word	TWC=00001	
360	TRMC	Press and release MANUAL ADVANCE TAPE. Tape advances one tape word	TWC=00002	
370	TRMC	Press and release $2^0, 2^1, 2^2$, ADR1, six times in succession.	TWC=00000	
380	TRMC	Press and release AUTO/MANUAL	Auto - ON Manual - OFF	
390	TRMC	Press and release START Tape runs through automatic tests. In approximately 27 seconds tape stops.		
400	MLDD	COMMAND DS1, OP1, OP2, OP3, OP4, ISX, SYL0, DSX, SIGN, and 1 lamps	ON	
410	MLDD	Parity SYL1 lamp	ON	
420	MLDD	COMPUTER ISX, SYL0, DSX lamps	ON	
430	MLDD	Lamps other than Command and Computer undetermined		
440	IE	Serial Parity error	ON	
450	IE	All other Error lamps	OFF	
460	IE	Lamps other than error undetermined		
470	TRMC	Tape Address	02757	
480	TRMC	Auto, ML, PWR ON, FORWARD, STOP, and ADV CTR lamps	ON	
490	TRMC	Press and release START switch, tape does not advance		
500	IE	Press and release ERROR RESET		
510	IE	Serial Parity Error	OFF	
520	TRMC	Press and release START -		
525	TRMC	Tape advances and stops		

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
530	TRMC	Tape Address	02760	
540	IE	SS MSC and TRS lamps	ON	
550	MLDD	COMPUTER IM1	ON	
		Disregard other lamps		
560	IE	Press and release ERROR RESET		
570	IE	All ERROR lamps	OFF	
580	TRMC	Press and release START.		
585	TRMC	Tape advances and stops.		
590	TRMC	Tape Address	02761	
600	IE	SSMBR and TRS lamps	ON	
610	IE	Press and release ERROR RESET		
620	IE	All ERROR lamps	OFF	
630	TRMC	Press and release START.		
635	TRMC	Tape advances and stops.		
640	TRMC	Tape Address	02762	
650	IE	SSMDR and TRS lamp	ON	
660	MLDD	IM1	ON	
670	IE	Press and release ERROR RESET		
680	IE	All ERROR lamps	OFF	
690	TRMC	Press and release START.		
695	TRMC	Tape advances and stops		
700	TRMC	Tape Address	02763	
710	IE	I/O 1	ON	
720	IE	Press and release ERROR RESET		
730	IE	All ERROR lamps	OFF	
740	TRMC	Press and release START.		
745	TRMC	Tape advances and stops.		
750	TRMC	Tape Address	02764	
760	IE	I/O 2	ON	
770	IE	All other errors	OFF	
780	IE	Press and release ERROR RESET		
790	IE	All ERROR lamps	OFF	
800	TRMC	Press and release START		
805	TRMC	Tape advances and stops.		
810	TRMC	Tape Address	02766	
820	IE	TRS and SER lamps	ON	
830	IE	All other error lamps	OFF	
840	IE	Press and release ERROR RESET		
850	IE	All ERROR lamps	OFF	
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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
860	TRMC	Press and release START.		
865	TRMC	Tape advances and stops		
870	TRMC	Tape Address	02767	
880	IE	AI3 and SER	ON	
890	IE	All other error lamps	OFF	
		Disregard all other lamps.		
900	IE	Press and release ERROR RESET		
910	IE	All ERROR lamps	OFF	
920	TRMC	Press and release START.		
925	TRMC	Tape advances and stops		
930	TRMC	Tape Address	02771	
940	IE	TRS, PAR, SSMBR, and HOPC1 lamps	ON	
950	MLDD	Computer DM1 lamp	ON	
		Disregard all other lamps		
960	IE	Press and release ERROR RESET		
970	IE	All ERROR lamps	OFF	
980	TRMC	Press and release START		
985	TRMC	Tape advances and stops.		
990.	TRMC	Tape Address	02772	
1000	IE	TRS, PAR, SSMBR and HOPC1 lamps	ON	
1010	MLDD	Computer SYL0, ISX and DSX lamps	ON	
1020	IE	Press and release ERROR RESET		
1030	IE	All ERROR lamps	OFF	
1040	TRMC	Press and release START		
1045	TRMC	Tape advances and stops.		
1050	TRMC	Tape Address	02773	
1060	IE	[illegible] SSMDR, SSMBR, HOPC1, TRS and SER lamps	ON	
1070	MLDD	Computer SYL0, ISX and DSX	ON	
1080	MLDD	All other computer SSM Display lamps	OFF	
1090	IE	Press and release ERROR RESET		
		All ERROR lamps	OFF	
1100	TRMC	Press and release START.		
1105	TRMC	Tape advances and stops.		
1110	TRMC	Tape Address	02774	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1120	IE	SSMSC and HOPC1	ON	
1130	MLDD	Computer SYL0, ISX and DSX	ON	
1140	IE	Press and release ERROR RESET		
1150	IE	All error lamps	OFF	
1160	TRMC	Press and release START		
1165	TRMC	Tape advances and stops.		
1170	TRMC	Tape Address	02775	
1180	IE	SSMDR and HOPC1	ON	
1190	IE	All other error lamps	OFF	
1200	IE	Press and release ERROR RESET		
1210	IE	All ERROR lamps	OFF	
1220	TRMC	Press and release START		
1225	TRMC	Tape advances and stops.		
1230	TRMC	Tape Address	02776	
1240	IE	SSMSC and HOPC1	ON	
1250	MLDD	Computer SYL0, ISX and DSX	ON	
1260	IE	Press and release ERROR RESET		
1270	IE	All ERROR lamps	OFF	
1280	TRMC	Press and release START		
1285	TRMC	Tape advances and stops		
1290	TRMC	Tape Address	02777	
1300	IE	IADR	ON	
1310	IE	Press and release ERROR RESET		
1320	IE	All ERROR lamps	OFF	
1330	TRMC	Press and release 1. 1 lamp	ON	
1340	TRMC	Press and release START		
1345	TRMC	Tape advances and stops.		
1350	TRMC	Tape Address	03000	
1360	IE	ALL lamp	ON	
1370	TRMC	Press and release START		
1375	TRMC	Tape advances and stops.		
1380	TRMC	Tape Address	03001	
1390	IE	CH2 = 1, CH3 = 0 lamp	ON	
1400	TRMC	Press and release START		
1405	TRMC	Tape advances and stops.		
1410	TRMC	Tape Address	03002	
1420	IE	CH1 = 0, CH3 = 1 lamp	ON	
1430	TRMC	Press and release START		
1435	TRMC	Tape advances and stops.		
1440	TRMC	Tape Address	03003	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1450	IE	CH1 = 1, CH3 = 0 lamp	ON	
1460	TRMC	Press and release START.		
1465	TRMC	Tape advances and stops.		
1470	TRMC	Tape Address	03004	
1480	IE	CH1 = 1, CH2 = 0 lamp	ON	
1490	TRMC	Press and release START.		
1495	TRMC	Tape advances and stops.		
1500	TRMC	Tape Address	03005	
1510	IE	CH1 = 0, CH2 = 1	ON	
1520	TRMC	Press and release START.		
1525	TRMC	Tape advances and stops.		
1530	TRMC	Tape Address	03006	
1540	IE	CH2 = 0, CH3 = 1 lamp	ON	
1550	TRMC	Press and release START.		
1555	TRMC	Tape advances and stops.		
1560	TRMC	Tape Address	03007	
1570	IE	CH2 = 1, CH3 = 0 lamp	ON	
1580	TRMC	Press and release START		
1585	TRMC	Tape advances and stops		
1590	TRMC	Tape Address	03010	
1600	IE	ALL lamp	ON	
1610	TRMC	Press and release START.		
1615	TRMC	Tape advances and stops.		
1620	TRMC	Tape Address	03011	
1630	IE	BSE	ON	
1640	IE	A3 $\overline{G5}$	ON	
1650	IE	Press and release ERROR RESET		
1660	IE	All ERROR lamps	OFF	
1670	TRMC	Press and release START.		
1675	TRMC	Tape advances and stops.		
1680	TRMC	Tape Address	03012	
1690	IE	BSE	ON	
1700	IE	A2 $\overline{G5}$	ON	
1710	IE	Press and release ERROR RESET		
1720	IE	All ERROR lamps	OFF	
1730	TRMC	Press and release START		
1735	TRMC	Tape advances and stops.		
1740	TRMC	Tape Address	03013	
1750	IE	BSE	ON	
1760	IE	A1 $\overline{G5}$	ON	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1770	IE	Press and release ERROR RESET		
1780	IE	All ERROR LAMPS	OFF	
1790	TRMC	Press and release the 1 lamp	OFF	
1800	TRMC	Press and release START.		
1805	TRMC	Tape advances and stops.		
1810	TRMC	Tape Address	03016	
1820	IE	SE2	ON	
1830	TRMC	Press and release AUTO/MANUAL	Manual ON	
1840	TRMC	Press and release MANUAL ADVANCE TAPE.		
1845	TRMC	Tape advances and stops.		
1850	TRMC	Tape Address	03017	
1860	TRMC	Press and release MANUAL ADVANCE TAPE		
1865	TRMC	Tape advances and stops.		
1866	TRMC	Tape Address	03020	
1867	TRMC	Press and release MANUAL ADVANCE TAPE		
1868	TRMC	Tape advances and stops		
1870	TRMC	Tape Address	03021	
1880	TRMC	Press and release FORWARD/REVERSE		
1890	TRMC	Press and release MANUAL ADVANCE TAPE		
1900	TRMC	Tape goes in reverse and stops		
1910	TRMC	Tape Address	03023	
1920	TRMC	Press and release MANUAL ADVANCE TAPE		
1930	TRMC	Tape goes in reverse and stops		
1940	TRMC	Tape Address	03024	
1950	TRMC	Press and release FORWARD/REVERSE	Forward ON	
1960	TRMC	Press and release MANUAL ADVANCE TAPE		
1970	TRMC	Tape advances and stops.		
1980	TRMC	Tape Address	03026	
1990	TRMC	Press and release MANUAL ADVANCE TAPE		
2000	TRMC	Tape Address	03027	
2010	IE	Press and release ERROR RESET		
2020	IE	ERROR lamp	OFF	
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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2030	TRMC	Press and release AUTO/MANUAL	Auto ON	
2040	TRMC	Press and release START		
2045	TRMC	Tape advances and stops		

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2050	TRMC	Tape Address	03032	
2060	IE	Various A1 and A2 Voter errors	ON	
2070	IE	All A3 voter errors	OFF	
2080	IE	Press and release ERROR RESET		
2090	IE	All error lamps	OFF	
2100	TRMC	Press and release START		
2110	TRMC	Tape advances and stops		
2120	TRMC	Tape Address	03034	
2130	IE	Various A2 and A3 Voter errors	ON	
2140	IE	All A1 voter errors	OFF	
2150	IE	Press and release ERROR RESET		
2160	IE	All errors	OFF	
2170	TRMC	Press and release START		
2180	TRMC	Tape advances and stops		
2190	TRMC	Tape Address	03036	
2200	IE	Various A1 and A3 Voter errors	ON	
2210	IE	All A2 voter errors	OFF	
2220	IE	Press and release ERROR RESET		
2230	IE	All error lamps	OFF	
2240	TRMC	Press and release START		
2250	TRMC	Tape advances and stops		
2260	TRMC	Tape Address	03040	
2270	TRMC	INV ERR	ON	
2280	IE	AOC	ON	
2290	IE	Press and release ERROR RESET		
2300	IE	Error lamp	OFF	
2310	TRMC	Press and release START		
2320	TRMC	Tape advances and stops		
2330	TRMC	Tape Address	03041	
2340	IE	All error lamps	OFF	
2350	TRMC	Press and release AUTO/MANUAL	Manual ON	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2360	TRMC	Press and release ADV CTR/SEL ADR		
2365	TRMC	SEL ADR	ON	
2370	TRMC	Press and release ADR2		
2380	TRMC	ADR 2 and ADR 6 lamps	OFF	
2390	TRMC	Press and release AUTO/MANUAL		
2400	TRMC	AUTO lamp	ON	
2410	MLDD	Press and release ERROR OVER RIDE	ON	
2420	TRMC	Press and release START		
2430	TRMC	Tape runs through automatic tests and stops in approximately 6 seconds		
2440	TRMC	Tape Address	03564	
2450	IE	SERIAL lamp	ON	
2460	IE	Press and release OP/TP		
2470	IE	OP lamp	ON	
2480	IE	Press and release ERROR RESET		
2490	IE	All ERROR lamps	OFF	
2500	TRMC	Press and release START		
2510	TRMC	Tape runs through automatic tests and stops in approximately 1.5 sec		
2520	TRMC	Tape Address	03770	
2530	IE	SERIAL lamp	ON	
2540	MLDD	Press and release ERROR OVER RIDE	OFF	
2550	IE	Press and release OP/TP		
2560	IE	TP lamp	ON	
2570	IE	Press and release ERROR RESET		
2580	IE	All ERROR Lamps	OFF	
2590	TRMC	Press and release VERIFY ONLY	ON	
2600	TRMC	Press and release START		
2610	TRMC	Tape runs to end and rewinds if no errors exist. Tape stops in approximately 24 seconds.		
2620	TRMC	Tape Address	06465	
2630	TRMC	Press and release START nine times. On the ninth operation the tape completes rewinding and stops.		
2640	TRMC	Tape Address	10033	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 12)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2650	TRMC	Press and release FORWARD/ REVERSE		
2660	TRMC	FORWARD lamp	ON	
2670	TRMC	Press and release AUTO/MANUAL		
2680	TRMC	MANUAL lamp	ON	
2690	TRMC	Press and release MANUAL AD- VANCE TAPE.		
2700	TRMC	Tape advances and stops		
2710	TRMC	Press and hold MANUAL ADVANCE TAPE		
2720	TRMC	Tape advances and stops		
2730	TRMC	Release, then press and release MANUAL ADVANCE TAPE		
2740	TRMC	Tape advances and stops		
2750	MLDD	Press and hold IS 4		
2760	TRMC	Press and release MANUAL AD- VANCE TAPE		
2770	TRMC	Tape does not advance		
2780	IE	TRCP lamp	ON	
2790	MLDD	Release IS 4		
2800	IE	TRCP lamp	OFF	
2810	TRMC	Press and release AUTO/MANUAL		
2820	TRMC	AUTO lamp	ON	
2825	TRMC	Press and release VERIFY ONLY		
2826	TRMC	VERIFY ONLY lamp	OFF	
NOTE		Timed steps follow		
2830	TRMC	Press and hold START (see 2870)		
2840	TRMC	Tape advances		
2850	TRMC	Press and release STOP (within 5 sec)		
2860	TRMC	Tape stops		
2870	TRMC	Verify START and STOP lamps were off while tape was running and came on when tape stopped.	OFF/ON	
2880	TRMC	Release START		
2881	TRMC	Press and release FORWARD/ REVERSE		
2882	TRMC	REVERSE lamp	ON	
2883	TRMC	Press and release START		
2884	TRMC	Tape runs in reverse and stops		
2885	TRMC	Press and release FORWARD/ REVERSE		

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 13)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2890	TRMC	Press and release START		
2900	TRMC	Tape advances		
2910	TRMC	Press and release stop (within 10 sec of 2890)		
2920	TRMC	Tape stops		
2930	TRMC	START and STOP lamps	ON	_____
2940	TRMC	Press and release FORWARD/ REVERSE		
2950	TRMC	REVERSE lamp	ON	_____

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 14)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2960	TRMC	Press and release START		
2970	TRMC	Tape rewinds		
2980	TRMC	Press and release STOP(within 5 sec		
2990	TRMC	Tape stops of 2960)		
3000	TRMC	START and STOP lamps	ON	
3010	TRMC	Press and release ML/DD		
3020	TRMC	ML and DD	OFF	
3030	TRMC	Press and release START		
3040	TRMC	Tape does not advance		
3050	TRMC	Press and release ML/DD		
3060	TRMC	ML lamp	ON	
3070	TRMC	Press and release START		
3080	TRMC	Tape rewinds and stops		
3090	TRMC	Press and release FORWARD/ REVERSE		
3100	TRMC	FORWARD lamp	ON	

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Figure 7-9. Automatic Self-Check and Tape Reader Controls Check (Sheet 15)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
NOTE		All lamps used for indications during this check are located in the ERRORS section of the IE Panel.		
05	MLDD	Press and release COMMAND DISPLAY RESET		
06	MLDD	Press and release COMPUTER DISPLAY RESET		
10	IE	Turn CLOCK rotary switch to position No. 7		
20	MLDD	Press and release ADDRESS COMPTR		
30	IE	A1 BO lamp	ON	
40	IE	Press and release ERROR RESET		
50	IE	A1 BO lamps	OFF	
60	IE	Turn CLOCK rotary switch to position No. 8		
70	MLDD	Press and release ADDRESS COMPTR		
80	IE	A1 BO lamp	ON	
90	IE	Press and release ERROR RESET		
100	IE	A1 BO lamp	OFF	
110	IE	Turn CLOCK rotary switch to position No. 9		
120	MLDD	Press and release ADDRESS COMPTR		
130	IE	A2 BO lamp	ON	
140	IE	Press and release ERROR RESET		
150	IE	A2 BO lamp	OFF	
160	IE	Turn CLOCK rotary switch to position No. 10		
170	MLDD	Press and release ADDRESS COMPTR		
180	IE	A2 BO lamp	ON	
190	IE	Press and release ERROR RESET		
200	IE	A2 BO lamp	OFF	
210	IE	Turn CLOCK rotary switch to position No. 11		
220	MLDD	Press and release ADDRESS COMPTR		

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 1 of 7)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
230	IE	A3 BO lamp	ON	
240	IE	Press and release ERROR RESET		
250	IE	A3 BO lamp	OFF	
260	IE	Turn CLOCK rotary switch to position No. 12		

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
270	MLDD	Press and release ADDRESS COMPTR		
280	IE	A3 $\overline{BO}$ lamp	ON	
290	IE	Press and release ERROR RESET		
300	IE	A3 $\overline{BO}$ lamp	OFF	
310	IE	Turn PHASE rotary switch to position A		
320	IE	Turn CLOCK Rotary switch to position 5		
330	MLDD	Press and release ADDRESS COMPTR		
340	IE	TIMING CLOCK lamp	ON	
350	IE	Press and release ERROR RESET		
360	IE	TIMING CLOCK lamp	OFF	
370	IE	Turn PHASE rotary switch to position B		
380	MLDD	Press and release ADDRESS COMPTR		
390	IE	TIMING CLOCK lamp	ON	
400	IE	Press and release ERROR RESET		
410	IE	TIMING CLOCK lamp	OFF	
420	IE	Turn PHASE rotary switch to position C		
430	MLDD	Press and release ADDRESS COMPTR		
440	IE	TIMING CLOCK lamp	ON	
450	IE	Press and release ERROR RESET		
460	IE	TIMING CLOCK lamp	OFF	
470	IE	Turn PHASE rotary switch to position 4		
480	MLDD	Press and release ADDRESS COMPTR		
490	IE	TIMING CLOCK lamp	ON	
500	IE	Press and release ERROR RESET		
510	IE	TIMING CLOCK lamp	OFF	
520	IE	Turn PHASE rotary switch to position 5		
530	MLDD	Press and release ADDRESS COMPTR		
540	IE	TIMING CLOCK lamp	ON	

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
550	IE	Press and release ERROR RESET		
560	IE	TIMING CLOCK lamp	OFF	
570	IE	Turn PHASE rotary switch to position 6		
580	MLDD	Press and release ADDRESS COMPTR		
590	IE	TIMING CLOCK lamp	ON	
600	IE	Press and release ERROR RESET		
610	IE	TIMING CLOCK lamp	OFF	
620	IE	Turn PHASE rotary switch to position 7		
630	MLDD	Press and release ADDRESS COMPTR		
640	IE	TIMING CLOCK lamp	ON	
650	IE	Press and release ERROR RESET		
660	IE	TIMING CLOCK lamp	OFF	
670	IE	Turn PHASE rotary switch to position 8		
680	MLDD	Press and release ADDRESS COMPTR		
690	IE	TIMING CLOCK lamp	ON	
700	IE	Press and release ERROR RESET		
710	IE	TIMING CLOCK lamp	OFF	
720	IE	Turn PHASE rotary switch to position 9		
730	MLDD	Press and release ADDRESS COMPTR		
740	IE	TIMING CLOCK lamp	ON	
750	IE	Press and release ERROR RESET		
760	IE	TIMING CLOCK lamp	OFF	
770	IE	Turn PHASE rotary switch to position 10		
780	MLDD	Press and release ADDRESS COMPTR		
790	IE	TIMING CLOCK lamp	ON	
800	IE	Press and release ERROR RESET		
810	IE	TIMING CLOCK lamp	OFF	
820	IE	Turn PHASE rotary switch to position 11		
830	MLDD	Press and release ADDRESS COMPTR		

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
840	IE	TIMING CLOCK lamp	ON	
850	IE	Press and release ERROR RESET		
860	IE	TIMING CLOCK lamp	OFF	
870	IE	Turn PHASE rotary switch to position 12		
880	MLDD	Press and release ADDRESS COMPTR		
890	IE	TIMING CLOCK lamp	ON	
900	IE	Press and release ERROR RESET		
910	IE	TIMING CLOCK lamp	OFF	
920	IE	Turn PHASE rotary switch (ccw) to position A		
930	IE	Turn CLOCK rotary switch to position 6		
940	MLDD	Press and release ADDRESS COMPTR		
950	IE	TIMING CLOCK lamp	ON	
960	IE	Press and release ERROR RESET		
970	IE	TIMING CLOCK lamp	OFF	
980	IE	Turn PHASE rotary switch to position B		
990	MLDD	Press and release ADDRESS COMPTR		
1000	IE	TIMING CLOCK lamp	ON	
1010	IE	Press and release ERROR RESET		
1020	IE	TIMING CLOCK lamp	OFF	
1030	IE	Turn PHASE rotary switch to position C		
1040	MLDD	Press and release ADDRESS COMPTR		
1050	IE	TIMING CLOCK lamp	ON	
1060	IE	Press and release ERROR RESET		
1070	IE	TIMING CLOCK lamp	OFF	
1080	IE	Turn PHASE rotary switch to position 4		
1090	MLDD	Press and release ADDRESS COMPTR		
1100	IE	TIMING CLOCK lamp	ON	
1110	IE	Press and release ERROR RESET		
1120	IE	TIMING CLOCK lamp	OFF	
1130	IE	Turn PHASE rotary switch to position 5		

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1140	MLDD	Press and release ADDRESS COMPTR		
1150	IE	TIMING CLOCK lamp	ON	
1160	IE	Press and release ERROR RESET		
1170	IE	TIMING CLOCK lamp	OFF	
1180	IE	Turn PHASE rotary switch to position 6		
1190	MLDD	Press and release ADDRESS COMPTR		
1200	IE	TIMING CLOCK lamp	ON	
1210	IE	Press and release ERROR RESET		
1220	IE	TIMING CLOCK lamp	OFF	
1230	IE	Turn PHASE rotary switch to position 7		
1240	MLDD	Press and release ADDRESS COMPTR		
1250	IE	TIMING CLOCK lamp	ON	
1260	IE	Press and release ERROR RESET		
1270	IE	TIMING CLOCK lamp	OFF	
1280	IE	Turn PHASE rotary switch to position 8		
1290	MLDD	Press and release ADDRESS COMPTR		
1300	IE	TIMING CLOCK lamp	ON	
1310	IE	Press and release ERROR RESET		
1320	IE	TIMING CLOCK lamp	OFF	
1330	IE	Turn PHASE rotary switch to position 9		
1340	MLDD	Press and release ADDRESS COMPTR		
1350	IE	TIMING CLOCK lamp	ON	
1360	IE	Press and release ERROR RESET		
1370	IE	TIMING CLOCK lamp	OFF	
1380	IE	Turn PHASE rotary switch to position 10		
1390	MLDD	Press and release ADDRESS COMPTR		
1400	IE	TIMING CLOCK lamp	ON	

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1410	IE	Press and release ERROR RESET		
1420	IE	TIMING CLOCK lamp	OFF	
1430	IE	Turn PHASE rotary switch to position 11		
1440	MLDD	Press and release ADDRESS COMPTR		
1450	IE	TIMING CLOCK lamp	ON	
1460	IE	Press and release ERROR RESET		
1470	IE	TIMING CLOCK lamp	OFF	
1480	IE	Turn PHASE rotary switch to position 12		
1490	MLDD	Press and release ADDRESS COMPTR		
1500	IE	TIMING CLOCK lamp	ON	
1510	IE	Turn CLOCK rotary switch (ccw) to NONE		
1520	IE	Turn PHASE rotary switch to NONE		
1530	IE	Press and release ERROR RESET		
1540	IE	TIMING CLOCK lamp	OFF	

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Figure 7-10. LVDCME Self-Check Timing Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	MLDD	Press and release MEMORY CLOCK EARLY		
20	MLDD	EARLY lamp	ON	
30	MLDD	NORMAL and LATE lamps	OFF	
40	TRMC	Using a digital voltmeter or a John Fluke Model 803B, measure and record voltage between TP 32 and GND.	Less than -1.5 VDC	
50	TRMC	Measure and record voltage between TP 33 and GND	Less than -1.5 VDC	
60	MLDD	Press and release MEMORY CLOCK LATE		
70	MLDD	LATE lamp	ON	
80	MLDD	EARLY and NORMAL lamps	OFF	
90	TRMC	Measure and record voltage between TP 32 and GND	5.0 to 6.2 VDC	
100	TRMC	Measure and record voltage between TP 33 and GND	5.0 to 6.2 VDC	
110	MLDD	Press and release MEMORY CLOCK NORMAL		
120	MLDD	NORMAL lamp	ON	
130	MLDD	EARLY and LATE lamps	OFF	
140	TRMC	Measure and record voltage between TP 32 and GND	Less than -1.5 VDC	
150	TRMC	Measure and record voltage between TP 33 and GND	5.0 to 6.2 VDC	

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Figure 7-11. Memory Timing Checks

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	IE	Turn PHASE rotary switch (CCW) to position 15.		
20	PC	COMP TEMP NORMAL lamp	OFF	
30	PC	COMP TEMP HIGH lamp	ON	
40	PC	COMP TEMP ARRAY lamp	ON	
50	PC	COMP POWER SEQ ON lamp	OFF	
60	PC	COMP POWER SEQ OFF lamp (DELAYED)	ON	
70	IE	Turn PHASE Rotary switch (CW) to NONE position		
80	PC	COMP TEMP NORMAL lamp	ON	
90	PC	COMP TEMP HIGH lamp	OFF	
100	PC	Press and release COMP POWER SEQ ON		
110	PC	COMP POWER SEQ ON lamp	Remains OFF	
115	PC	COMP POWER SEQ OFF lamp	Remains ON	
120	IE	Press and release ERROR RESET		
130	PC	COMP TEMP ARRAY lamp	OFF	
140	PC	Press and release COMP POWER SEQ ON		
145	PC	COMP POWER SEQ OFF lamp	OFF	
150	PC	COMP POWER SEQ ON lamp (delayed)	ON	
160	IE	Turn PHASE rotary switch (CW) to position 14		
165	PC	COMP TEMP NORMAL lamp	OFF	
170	PC	COMP TEMP PAGE lamp	ON	
180	PC	COMP TEMP HIGH lamp	ON	
190	PC	COMP POWER SEQ ON lamp	OFF	
200	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
210	IE	Turn PHASE rotary switch (CCW) to NONE position		
220	PC	COMP TEMP NORMAL lamp	ON	
230	PC	COMP TEMP HIGH lamp	OFF	
240	PC	Press and release COMP POWER SEQ ON		
250	PC	COMP POWER SEQ ON lamp	Remains OFF	
255	PC	COMP POWER SEQ OFF lamp	Remains ON	

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Figure 7-12. Computer Temperature Sensing Checks (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
260	IE	Press and release ERROR RESET		
270	PC	COMP TEMP PAGE lamp	OFF	
280	PC	Press and release COMP POWER SEQ ON		
285	PC	COMP POWER SEQ OFF lamp	OFF	
290	PC	COMP POWER SEQ ON lamp (delayed)	ON	
200	IE	Press and release ERROR RESET		
310	IE	All ERROR lamps	OFF	

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Figure 7-12. Computer Temperature Sensing Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
05	IE	MANUAL HALT lamp (press and release COMPTR HALT/MANUAL HALT if OFF)	ON	
10	IE	CHANNEL lamp (press and release CHANNEL/MODULE if ON)	OFF	
15	IE	MODULE lamp	ON	
20	IE	MODULE, MODULE 1 through 7 CH2=1, CH3=0 lamps	ON	
30	IE	Press and release MODULE 1 through 7 CHANNEL 2 lamps		
40	IE	MODULE 1 through 7 CHANNEL 1 lamps	OFF	
50	IE	MODULE 1 through 7 CHANNEL 2 CH1=0, CH3=1 lamps	ON	
60	IE	Press and release MODULE 1 through 7 CHANNEL 3 lamps		
70	IE	MODULE 1 through 7 CHANNEL 3 CH1=0, CH2=1 lamps	ON	
80	IE	MODULE 1 through 7 CHANNEL 2 lamps	OFF	
90	IE	Press and release MODULE 1 through 7 CHANNEL 1 lamps		
100	IE	MODULE 1 through 7 CHANNEL 1 CH 2 = 0, CH 3 = 1 lamps	ON	
110	IE	MODULE 1 through 7 CHANNEL 3 lamps	OFF	
120	IE	Press and release MODULE 1 through 7 CHANNEL 2 lamps		
130	IE	MODULE 1 through 7 CHANNEL 2 CH 1 = 1, CH 3 = 0 lamps	ON	
140	IE	MODULE 1 through 7 CHANNEL 1 lamps	OFF	
150	IE	Press and release MODULE 1 through 7 CHANNEL 3 lamps		
160	IE	MODULE 1 through 7 CHANNEL 3 CH 1 = 1, CH2 = 0 lamps	ON	
170	IE	MODULE 1 through 7 CHANNEL 2 lamps	OFF	

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Figure 7-13. Channel-Module Switching Checks (Sheet 1 of 10)

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UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
180	IE	Turn CLOCK rotary switch (cw) to position 14		
190	IE	ILLEGAL PATH lamp	ON	
200	IE	Turn CLOCK rotary switch (ccw) to NONE		
210	IE	ILLEGAL PATH lamp	OFF	
220	IE	Press and release CHANNEL/ MODULE		
230	IE	CHANNEL lamp/MODULE lamp	ON/OFF	
240	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
250	IE	MODULE 1 through 7 CHANNEL 1 CH 2 = 1, CH 3 = 0 lamps	ON	
260	IE	MODULE 1 through 7 CHANNEL 3 CH 1 = 1, CH 2 = 0 lamps	OFF	
270	MLDD	CHANNEL 1 lamps	ON	
280	02A03	Measure and reocrd voltage (using a digital voltmeter or equivalent) between TP37 and TP (GND)	5.920 to 6.015 VDC	
290	02A03	Measure and reocrd voltage between TP17 and TP55 (GND)	11.945 to 12.02 VDC	
300	02A03	Using a Simpson voltohmeter, or equivalent, verify 6 VDC (Ref) between the following test points and GND TP 34, 37, 40, 43, 46, 49 and 52	6V (Ref)	
310	02A03	Verify 0.0 VDC at the following test points to GND TP 15, 18, 21, 24, 27, 30, 33, 35, 36, 38, 39, 41, 42, 44, 45, 47, 48, 50, 51, 53 and 54	0 V (Ref)	
320	02A03	Using X1 scale verify continuity between the test points in step 310 to GND	Verify	
330	IE	Press and release CH2		
340	IE	CH2 - CH1 = 0, CH3 = 1 lamp	ON	
350	IE	CH1 - CH2 = 1, CH3 = 0 lamp	OFF	
360	IE	MODULE 1 through 7 CHANNEL 1 lamps	OFF	
370	IE	MODULE 1 through 7 CHANNEL 2 CH1 = 0, CH3 = 1 lamps	ON	
380	MLDD	CHANNEL 2 lamp	ON	

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Figure 7-13. Channel-Module Switching Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
390	02A03	Verify 0 VDC at the following test points to GND TP 13, 16, 19, 22, 25, 28, 31, 34, 37, 40, 43, 46, 49, 52	0 V (Ref)	
400	02A03	Verify continuity between the test points in step 390 and GND	Verify	
410	IE	Press and release CH3		
420	IE	CH3 - CH1 = 0, CH2 = 1 lamp	ON	
430	IE	CH2 - CH1 = 0, CH3 = 1 lamp	OFF	
440	IE	MODULE 1 through 7, CHANNEL 3 CH1 = 0, CH2 = 1 lamps	ON	
450	IE	MODULE 1 through 7 CHANNEL 2 lamps	OFF	
460	MLDD	CHANNEL 3 lamp	ON	
470	MLDD	CHANNEL 2 lamp	OFF	
480	IE	Press and release CH3		
490	IE	CH3 - CH1 = 1, CH2 = 0 lamp	ON	
500	IE	CH3 - CH1 = 0, CH2 = 1 lamp	OFF	
510	IE	MODULE 1 through 7, CHANNEL 3 CH1 = 1, CH2 = 0 lamp	ON	
515	IE	CH1 = 0, CH2 = 1 lamp	OFF	
520	02A03	Verify 0 VDC at the following test points to GND, TP 14, 17, 20, 23, 26, 29, 32, 34, 37, 40, 43, 46, 49, 52	0 V (Ref)	
530	02A03	Verify continuity between the test points in step 520 and GND	Verify	
540	IE	Press and release ALL		
550	IE	CH3 - CH1 = 1, CH2 = 0 lamp	OFF	
560	IE	MODULE 1 through 7, CHANNEL 3 lamps	OFF	
570	MLDD	CHANNEL 3 lamp	OFF	
575	MLDD	CHANNEL ALL lamp	ON	
580	02A03	Verify 6 VDC (Ref) at the following test points to GND. Test Pts. 34 through 54	6 V (Ref)	
590	02A03	Verify 12 VDC (Ref) at the following test points to GND Test points 13 through 33	12 V (Ref)	
600	IE	Turn CLOCK rotary switch (CCW) to position 15		
610	IE	ILLEGAL PATH lamp	ON	
620	IE	Turn CLOCK rotary switch (CW) to NONE		

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Figure 7-13. Channel-Module Switching Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
630	IE	ILLEGAL PATH lamp	OFF	
640	IE	Press and release CH2		
650	IE	CH2 - CH1 = 1, CH3 = 0 lamp	ON	
655	IE	ALL lamp	OFF	
660	IE	MODULE 1 through 7 CHANNEL 2 CH1 = 1, CH3 = 0 lamp	ON	
670	MLDD	CHANNEL 2 lamp	ON	
675	MLDD	CHANNEL ALL lamp	OFF	
680	IE	Press and release LAMP TEST		
690	IE	All lamps	ON	
NOTE		ERROR RESET, RESET and PIO REPEAT do not contain lamps		
695	MLDD	All CHANNEL lamps	ON	
700	IE	Press and release LAMP TEST		
710	IE	All lamps not previously ON	OFF	
720	IE	Press and release CH1		
730	IE	CH1 - CH2 = 0, CH3 = 1 lamp	ON	
740	IE	CH2 - CH1 = 1, CH3 = 0 lamp	OFF	
750	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 0, CH3 = 1 lamps	ON	
760	IE	MODULE 1 through 7, CHANNEL 2 lamps	OFF	
770	MLDD	CHANNEL 1 lamp	ON	
775	MLDD	CHANNEL ALL lamp	OFF	
776	TRMC	Press and release ADR 3		
777	TRMC	ADR 3 lamp/ADR6 lamp	ON/OFF	
778	TRMC	Press and release ADR 3		
779	TRMC	ADR 3 lamp	OFF	
780	TRMC	Press and release ADR 5		
790	TRMC	ADR 5 lamp	ON	
800	MLDD	Press and release DATA 9/9		
810	MLDD	COMMAND 9 lamp	ON	
820	MLDD	Press and release ADDRESS COMPTR		
830	MLDD	CHANNEL ALL lamp	ON	
840	IE	ALL lamp	ON	
850	IE	MODULE 1 through 7 CHANNEL 1 lamps	OFF	
860	MLDD	Press and release DATA 9/9 and 18/18		

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Figure 7-13. Channel-Module Switching Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
870	MLDD	COMMAND 9 lamp	OFF	
875	MLDD	COMMAND 18 lamp	ON	
880	MLDD	Press and release ADDRESS COMPTR		

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Figure 7-13. Channel-Module Switching Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
890	MLDD	CHANNEL 1 lamp	ON	
895	MLDD	ALL lamp	OFF	
900	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
910	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
915	IE	CHANNEL ALL lamp	OFF	
920	MLDD	Press and release DATA 18/18 and 9/9		
930	MLDD	COMMAND 18 lamp	OFF	
935	MLDD	COMMAND 9 lamp	ON	
940	MLDD	Press and release ADDRESS COMPTR		
950	MLDD	CHANNEL ALL lamp	ON	
955	MLDD	CHANNEL 1 lamp	OFF	
960	IE	ALL lamp	ON	
970	IE	MODULE 1 through 7 CHANNEL 1 lamps	OFF	
980	MLDD	Press and release DATA 9/9 and 19/19		
990	MLDD	COMMAND 9 lamp	OFF	
995	MLDD	COMMAND 19 lamp	ON	
1000	MLDD	Press and release ADDRESS COMPTR		
1010	MLDD	CHANNEL 1 lamp	ON	
1015	MLDD	CHANNEL ALL Lamp	OFF	
1020	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
1030	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1035	IE	CHANNEL ALL lamp	OFF	
1040	MLDD	Press and release ADDRESS COMPTR		
1050	MLDD	CHANNEL 2 lamp	ON	
1055	MLDD	CHANNEL 1 lamp	OFF	
1060	IE	CH2 - CH1 = 0, CH3 = 1 lamp	ON	
1070	IE	MODULE 1 through 7, CHANNEL 2 CH1 = 0, CH3 = 1 lamps	ON	
1080	IE	MODULE 1 through 7, CHANNEL 1 lamps	OFF	
1085	IE	CHANNEL 1 lamp	OFF	
1090	MLDD	Press and release DATA 19/19 and 18/18		
1100	MLDD	COMMAND 19 lamp	OFF	
1105	MLDD	COMMAND 18 lamp	ON	

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Figure 7-13. Channel-Module Switching Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1110	MLDD	Press and release Address Computer		
1120	MLDD	CHANNEL 1 lamp	ON	
1125	MLDD	CHANNEL 2 lamp	OFF	
1130	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
1135	IE	CHANNEL 2 lamps	OFF	
1140	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1145	IE	MODULE 1 through 7, CHANNEL 2 lamps	OFF	
1150	MLDD	Press and release DATA 18/18 and 9/9		
1160	MLDD	COMMAND 18 lamp	OFF	
1165	MLDD	COMMAND 9 lamp	ON	
1170	MLDD	Press and release ADDRESS COMPTR		
1180	MLDD	CHANNEL ALL lamp	ON	
1190	IE	ALL lamp	ON	
1193	IE	CH1 lamps	OFF	
1195	IE	MODULE 1 through 7, CHANNEL 1 lamps	OFF	
1197	MLDD	CHANNEL 1 lamp	OFF	
1200	MLDD	Press and release DATA 9/9 and 21/21		
1210	MLDD	COMMAND 9 lamp	OFF	
1215	MLDD	COMMAND 21 lamp	ON	
1220	MLDD	Press and release ADDRESS COMPTR		
1225	MLDD	CHANNEL ALL lamp	OFF	
1230	MLDD	CHANNEL 1 lamp	ON	
1240	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
1245	IE	CHANNEL ALL lamp	OFF	
1246	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1250	MLDD	Press and release ADDRESS COMPTR		
1260	MLDD	CHANNEL 3 lamp	ON	
1265	MLDD	CHANNEL 1 lamp	OFF	
1270	IE	CH3 - CH1 = 1, CH2 = 0 lamp	ON	
1275	IE	MODULE 1 through 7, CHANNEL 3 CH1 = 1, CH2 = 0 lamps	ON	
1277	IE	MODULE 1 through 7, CHANNEL 1 lamps	OFF	
1280	MLDD	Press and release DATA 21/21 and 9/9		
1290	MLDD	COMMAND 21 lamp	OFF	

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Figure 7-13. Channel-Module Switching Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1295	MLDD	COMMAND 9 lamp	ON	
1300	MLDD	Press and release ADDRESS COMPTR		
1310	MLDD	CHANNEL ALL lamp	ON	
1315	MLDD	CH3 lamp	OFF	
1320	IE	ALL lamp	ON	
1325	IE	MODULE 1 through 7, CHANNEL 3 lamps	OFF	
1330	MLDD	Press and release DATA 9/9 and 17/17		
1340	MLDD	COMMAND 9 lamp	OFF	
1345	MLDD	COMMAND 17 lamp	ON	
1350	MLDD	Press and release ADDRESS COMPTR		
1360	MLDD	CHANNEL 1 lamp	ON	
1365	MLDD	CHANNEL ALL lamp	OFF	
1370	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
		MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1375	IE	CH ALL lamp	OFF	
1380	MLDD	Press and release ADDRESS COMPTR		
1390	IE	CH1 - CH2 = 0, CH3 = 1 lamp	ON	
1393	IE	CH1 - CH2 = 1, CH3 = 0 lamp	OFF	
1395	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 0, CH3 = 1 lamps	ON	
1400	MLDD	Press and release DATA 17/17 and 9/9		
1410	MLDD	COMMAND 17 lamp	OFF	
1415	MLDD	COMMAND 9 lamp	ON	
1420	MLDD	Press and release ADDRESS COMPTR		
1430	MLDD	CHANNEL ALL lamp	ON	
1440	IE	ALL lamp	ON	
1445	IE	MODULE 1 through 7, CHANNEL 1 lamps	OFF	
1448	IE	CH1 - CH2 = 0, CH3 = 1 lamp	OFF	
1450	MLDD	Press and release DATA 9/9 and 20/20		
1460	MLDD	COMMAND 9 lamp	OFF	
1465	MLDD	COMMAND 20 lamp	ON	
1470	MLDD	Press and release ADDRESS COMPTR		
1475	MLDD	CHANNEL ALL lamp	OFF	
1480	MLDD	CHANNEL 1 lamp	ON	

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Figure 7-13. Channel-Module Switching Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1490	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
1495	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1500	MLDD	Press and release ADDRESS COMPTR		
1510	MLDD	CHANNEL 2 lamp	ON	
1515	MLDD	CHANNEL 1 lamp	OFF	
1520	IE	CH2 - CH1 = 1, CH3 = 0 lamp	ON	
1523	IE	CH1 - CH2 = 1, CH3 = 0 lamp	OFF	
1525	IE	MODULE 1 through 7, CHANNEL 2 CH1 = 1, CH3 = 0 lamps	ON	
1530	MLDD	Press and release DATA 20/20 and 9/9		
1533	MLDD	COMMAND 20 lamp	OFF	
1536	MLDD	COMMAND 9 lamp	ON	
1540	MLDD	Press and release ADDRESS COMPTR		
1550	MLDD	CHANNEL ALL lamp	ON	
1555	MLDD	CHANNEL 2 lamp	OFF	
1560	IE	ALL lamp	ON	
1563	IE	MODULE 1 through 7, CHANNEL 2 CH1 = 1, CH3 = 0 lamps	OFF	
1566	IE	CH2 - CH1 = 1, CH3 = 0 lamp	OFF	
1570	MLDD	Press and release DATA 9/9 and 22/22		
1580	MLDD	COMMAND 9 lamp	OFF	
1585	MLDD	COMMAND 22 lamp	ON	
1590	MLDD	Press and release ADDRESS COMPTR		
1600	MLDD	CHANNEL 1 lamp	ON	
1605	MLDD	CHANNEL ALL lamp	OFF	
1610	IE	CH1 - CH2 = 1, CH3 = 0 lamp	ON	
1615	IE	ALL lamp	OFF	
1617	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1620	MLDD	Press and release ADDRESS COMPTR		
1630	MLDD	CHANNEL 3 lamp	ON	
1635	MLDD	CHANNEL 1 lamp	OFF	
1640	IE	CH3 - CH1 = 0, CH2 = 1 lamp	ON	
1645	IE	CH1 - CH2 = 1, CH3 = 0 lamp	OFF	
1647	IE	MODULE 1 through 7, CHANNEL 3 CH1 = 0, CH2 = 1 lamps	ON	
1650	IE	Press and release CHANNEL/ MODULE		

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Figure 7-13. Channel-Module Switching Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1660	IE	MODULE lamp	ON	
1665	IE	CHANNEL lamp	OFF	
1670	IE	CH3 - CH1 = 0, CH2 = 1 lamp	OFF	
1674	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1676	MLDD	CHANNEL 3 lamp	OFF	
1680	IE	Press and release LAMP TEST		
1690	IE	CHANNEL lamp	ON	
1700	IE	Press and release LAMP TEST		
1710	IE	CHANNEL lamp	OFF	
1720	IE	Press and release MODULE 1 through 7, CHANNEL 3 lamps		
1730	IE	MODULE 1 through 7, CHANNEL 3 CH1 = 1, CH2 = 0 lamps	ON	
1740	PC	Press and release COMP POWER SEQ OFF		
1750	PC	COMP POWER SEQ ON lamp	OFF	
1760	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
1770	PC	Press and release ACME POWER SEQ OFF		
1780	PC	ACME POWER SEQ ON lamp	OFF	
1790	IE	MODULE 1 through 7, CHANNEL 3 CH1 = 1, CH2 = 0 lamps	OFF	
1800	IE	MODULE 1 through 7, CHANNEL 1 CH2 = 1, CH3 = 0 lamps	ON	
1810	PC	ACME POWER SEQ OFF lamp	ON	
1820	PC	Press and release ACME POWER SEQ ON		
1825	PC	ACME POWER SEQ OFF lamp	OFF	
1830	PC	ACME POWER SEQ ON lamp	ON	
1840	PC	Press and release COMP POWER SEQ ON		
1845	PC	COMP POWER SEQ OFF lamp	OFF	
1850	PC	COMP POWER SEQ ON lamp	ON	
1860	IE	Press and release ERROR RESET		
1870	IE	Press and release COMPTR HALT/ MANUAL HALT		
1880	IE	COMPTR HALT lamp	ON	
		MANUAL HALT lamp	OFF	

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Figure 7-13. Channel-Module Switching Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	TRMC	Press and release MEMORY SIM		
20	TRMC	MEMORY SIM lamp	ON	
30	TRMC	Tape Address Counter	Counting	
40	IE	INTC lamp (If ON perform 41 through 46)		
41	IE	Press and release MANUAL HALT		
42	IE	MANUAL HALT and COMPUTER HALT lamps	ON	
43	IE	INTC lamp	OFF	
44	IE	Press and release MANUAL/ COMPUTER HALT		
45	IE	MANUAL and COMPUTER HALT lamps	OFF	
46	IE	COMPUTER ALARM lamp	ON	
50	MLDD	Press and release A2 and A3		
60	MLDD	COMMAND and COMPUTER A2 and A3 lamps	ON	
70	TRMC	Place Spare Probe (SP2) in TP 28		
80	IE	Turn PHASE switch to C		
90	IE	Turn BIT GATE switch to 6		
100	IE	Turn CLOCK switch to W		
110	MLDD	Turn DISPLAY SELECT switch to SP2		
120	MLDD	Press and release COMPUTER CONTROL ON/OFF		
130	MLDD	ON, ADVANCE and CST lamps	ON	
140	MLDD	Data 22, 23, 24, 25, and OP2 lamps	ON	
150	TRMC	Tape Address counter 2^1 and 2^2 lamps	ON	
NOTE		When Tape Address counter lamps are referenced, lamps 2^8 through 2^{12} may be either ON or OFF. Therefore only lamps 2^0 through 2^7 will be verified.		
160	IE	I/O Reg. No. 1 lamps 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22, and 23	ON	
170	MLDD	Press and release ADVANCE/CST		
180	MLDD	ADVANCE lamp	ON	
190	MLDD	DATA COMPUTER 22, 23, 24, 25, lamps	ON	
200	MLDD	OP2 and OP4 Computer lamps	ON	
210	MLDD	COMPUTER A1, A2 and A3 lamps	ON	
220	IE	I/O Reg. No. 1 lamps 9, 10, 23 and 24	ON	
230	TRMC	Tape Address 2^0, 2^1, and 2^2 lamps	ON	

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Figure 7-14. Single Step Checks (Sheet 1 of 25)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
240	MLDD	Press and release PAST/PRESENT		
250	MLDD	PAST lamp	ON	
251	MLDD	PRESENT lamp	OFF	
255	IE	I/O Reg. No. 1 lamps 9, 10, 23 and 24	ON	
256	MLDD	All Data Computer lamps	OFF	
260	MLDD	ADVANCE lamp	OFF	
265	TRMC	TAPE ADDRESS 2^0, 2^1 and 2^2	ON	

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Figure 7-14. Single Step Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
270	MLDD	COMPUTER A1, A2 and A3 lamps	OFF	
275	MLDD	COMMAND A2 and A3 lamps	ON	
280	MLDD	Press and release ADVANCE/CST		
290	MLDD IE and TRMC	All lamps	No Change	
300	MLDD	Press and release PAST/PRESENT		
310	MLDD	PRESENT lamp	ON	
320	MLDD	ADVANCE lamp	ON	
325	MLDD	PAST Lamp	OFF	
330	MLDD	Press and release A5, 0A8 and 0A9		
340	MLDD	COMMAND A5, 0A8 and 0A9 lamps	ON	
350	MLDD	Press and release ADVANCE/CST		
360	IE	I/O Reg. No. 1 lamps 4, 7, 9, 11, 18, 21, 23, 25	ON	
370	IE	ADDRESS A8 and A9 lamps	ON	
380	MLDD	COMPUTER OP2, OP3, 0A8 and 0A9 lamps	ON	
381	MLDD	COMMAND A2, A3, A5, 0A8, 0A9 lamps	ON	
390	MLDD	COMPUTER A2, A3, A5, and A8 lamp	ON	
391	MLDD	ON, ADVANCE, CST lamps	ON	
400	TRMC	Tape Address 2^1, 2^2, 2^4, and 2^7 lamps	ON	
410	MLDD	Press and release ADVANCE/CST		
420	MLDD	Computer A1, A2, A3, A5, A8, 0A8, 0A9, OP2, OP3, and OP4	ON	
430	MLDD	All DATA COMPUTER lamps	ON	
431	IE	A8 and A9 lamps	ON	
432	IE	I/O Reg. No. 1 lamps 4, 7, 9, 11, 18, 21, 23, and 25	ON	
433	TRMC	Tape Address 2^3, 2^4 and 2^7	ON	
440	MLDD	Press and release ADVANCE/CST		
450	MLDD	DATA COMPUTER 22, 23, 24, and 25 lamps	ON	
460	MLDD	COMPUTER 0A8, 0A9, OP1, OP2, OP4, A1, A4, A5, A8 and DS2 lamps	ON	
470	MLDD	COMMAND 0A8, 0A9, A2, A3 and A5 lamps	ON	
471	MLDD	ON/ADV and CST	ON	

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Figure 7-14. Single Step Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
480	IE	ADDRESS A8 and A9 lamp	ON	
490	IE	I/O Reg. No. 1 lamps 4, 7, 9, 11, 18 21, 23 and 25	ON	
500	TRMC	Tape Address 2^0, 2^3, 2^4, and 2^7 lamps	ON	
510	MLDD	Press and release (4 times) ADVANCE/CST		
520	MLDD	COMPUTER 0A8, 0A9, OP1, OP2, OP3, A2, A3, A4, A5, A8	ON	
521	MLDD	COMMAND A2, A3, A5, 0A8, and 0A9 lamps	ON	
522	MLDD	Computer Data Bits 22, 23, 24, and 25 lamps	ON	
523	MLDD	ADV - ON - CST lamps	ON	
530	IE	I/O Reg. No. 1 lamps 4, 7, 8, 9, 11, 18, 21, 22, 23, and 25	ON	
531	IE	A8 and A9 lamps	ON	
540	TRMC	Tape Address 2^1, 2^2, 2^3, 2^4 and 2^7 lamps	ON	
550	MLDD	Press and release 0A8, 0A9, A3 A5 and A6		
560	MLDD	COMMAND 0A8, 0A9, A3, A5 lamps	OFF	
570	MLDD	COMMAND A6	ON	
580	MLDD	Press and release ADVANCE/CST		
590	MLDD	All DATA COMPUTER lamps	ON	
600	MLDD	COMPUTER and COMMAND A2 and A6 lamps	ON	
601	MLDD	ON- ADV - CST lamp	ON	
610	IE	I/O Reg. No. 1 lamps 7, 8, 9, 21, 22 and 23	ON	
620	TRMC	Tape Address 2^0, 2^1 and 2^5 lamps	ON	
630	MLDD	Press and release A2, A3, A6 and0A9		
640	MLDD	COMMAND A2 and A6 lamps	OFF	
650	MLDD	COMMAND A3 and 0A9 lamps	ON	
670	MLDD	Press and release ADVANCE/CST		
680	MLDD	ADVANCE and CST lamps	OFF	
681	MLDD	ON lamp	ON	
690	TRMC	Tape Address Counter	Counting	
700	MLDD	Press and release 0A9		
710	MLDD	COMMAND 0A9 lamp	OFF	
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Figure 7-14. Single Step Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
730	TRMC	Tape Address 2^0 and 2^2 lamp	ON	
740	MLDD	ADVANCE and CST lamps	ON	
750	MLDD	All DATA COMPUTER lamps	ON	
760	MLDD	COMPUTER A3 lamp	ON	
761	MLDD	COMMAND A3 lamp	ON	
770	IE	I/O Reg. No. 1 lamps 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22 and 23	ON	
780	MLDD	Press and release 0A1 and 0A4		
790	MLDD	COMMAND 0A1 and 0A4 lamps	ON	
800	MLDD	Press and release DATA/INS		
810	MLDD	DATA lamp	ON	
811	MLDD	INS lamp	OFF	
820	MLDD	Press and release ADVANCE/CST		
830	MLDD	DATA COMPUTER lamps 22, 23, 24, and 25	ON	
840	MLDD	COMPUTER 0A1, 0A4, OP2, A2 and A3 lamps	ON	
841	MLDD	COMMAND 0A1, 0A4, A3 lamps	ON	
842	IE	I/O Reg. No. 1 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22, 23 lamps	ON	
850	TRMC	Tape Address 2^1 and 2^2 lamps	ON	
860	MLDD	Press and release A4		
870	MLDD	COMMAND A4 lamp	ON	
880	MLDD	Press and release ADVANCE/CST		
890	MLDD	COMPUTER 0A1, 0A4, OP2, OP4, A1, A2 and A3 lamps	ON	
891	MLDD	COMMAND 0A1, 0A4, A3, and A4 lamps	ON	
892	MLDD	Computer Data Bits 22, 23, 24, and 25 lamps	ON	
900	IE	ADDRESS A1 and A4 lamps and I/O Reg. No. 1 lamps 9, 10, 23, and 24	ON	
910	TRMC	Tape Address 2^0, 2^1 and 2^2 lamps	ON	
920	MLDD	Press and release DATA/INS		
930	MLDD	INS lamp	ON	
940	MLDD	DATA lamp	OFF	
950	MLDD	Press and release 0A1 and 0A4		
960	MLDD	COMMAND 0A1 and 0A4 lamps	OFF	
970	MLDD	Press and release 0A2		
980	MLDD	COMMAND 0A2 lamp	ON	

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Figure 7-14. Single Step Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
990	MLDD	Press and release ADVANCE/CST		
1000	MLDD	COMPUTER A4, 0A2, OP1 and OP 3 lamps	ON	
1001	MLDD	COMMAND 0A2, A3 and A4 lamps	ON	
1002	MLDD	Computer Data Bits 22, 23, 24, 25	ON	
1003	MLDD	ON - CST - ADV lamps	ON	
1004	IE	I/O Reg. No. 1 lamps 9, 10, 23 and 24	ON	
1005	IE	A1 and A4 lamps	ON	
1010	TRMC	Tape Address 2^3 lamp	ON	
1020	MLDD	Press and release A3, A4 and 0A2		
1030	MLDD	COMMAND A3, A4 and 0A2 lamps	OFF	
1040	TRMC	Press and release ADR5		
1050	TRMC	ADR5 lamp	ON	
1060	MLDD	Press and release DS3		
1070	MLDD	COMMAND DS3 lamp	ON	
1080	MLDD	Press and release ADDRESS COMPTR		
1090	MLDD	All DATA COMPUTER lamps	ON	
1100	MLDD	ADVANCE and CST lamps	OFF	
1101	MLDD	ON lamp	ON	
1110	IE	INTC lamp	ON	
1120	TRMC	Tape Address counter	Counting	
1130	MLDD	Press and release DS3 and DS4		
1140	MLDD	COMMAND DS3 lamp	OFF	
1141	MLDD	COMMAND DS4 lamp	ON	
1150	MLDD	Press and release ADDRESS COMPTR		
1160	MLDD	ADVANCE and CST lamps	ON	
1161	MLDD	ON lamp	ON	
1162	MLDD	ALL Data Computer lamps	ON	
1170	IE	INTC lamp	OFF	
1180	TRMC	Tape Address 2^0 lamp	ON	
1190	IE	I/O Reg. No. 1 lamps 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22 and 23	ON	
1200	MLDD	Press and release DS4		
1210	MLDD	COMMAND DS4 lamp	OFF	
1220	MLDD	Press and release SINGLE STEP ON/OFF		
1230	MLDD	ON, ADVANCE and CST lamps	OFF	

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Figure 7-14. Single Step Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1231	MLDD	OFF lamp	ON	
1240	TRMC	Tape Address Counter	Counting	
1250	MLDD	Press and release STOP		
1260	MLDD	ON, ADVANCE and CST lamps	ON	
NOTE		Some Instruction Address and OP lamps will be ON at this time. The Computer Tape Address counter will conform to the COMPUTER lamps in the Instruction Address Register.		
1270	MLDD	Press and release ON/OFF		
1280	MLDD	ON, ADVANCE and CST lamps	OFF	
1281	MLDD	OFF lamp	ON	
1290	TRMC	Tape Address counter	Counting	
1300	MLDD	Press and release ON/OFF		
1310	MLDD	ON, ADVANCE and CST lamps	ON	
1311	MLDD	OFF lamp	OFF	
1312	MLDD	ALL Computer Data Bits	ON	
1313	IE	I/O Reg. No. 1 lamps 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22, 23	ON	
1320	TRMC	Tape Address 2^0 lamp	ON	
1330	MLDD	Press and release (4 times) ADVANCE/CST		
1340	MLDD	COMPUTER A1, A2, A3, OP2 and OP4 lamps	ON	
1341	MLDD	Computer Data Bits 22, 23, 24, 25	ON	
1342	IE	I/O Reg. No. 1 lamps 9, 10, 23, and 24	ON	
1343	TRMC	Tape Address Counter 2^0, 2^1 and 2^2	ON	
1350	MLDD	Press and release DS 3 and 0A9		
1360	MLDD	COMMAND DS3 and 0A9 lamps	ON	
1370	MLDD	Press and release ADVANCE/CST		
1380	MLDD	DATA COMPUTER lamps 22, 23, 24 and 25	ON	
1390	MLDD	COMPUTER A4, 0A9, OP1 and OP3 lamps	ON	
1391	MLDD	COMMAND DS3, 0A9 lamps	ON	
1392	MLDD	Computer Data lamps 22, 23, 24, 25	ON	
1400	IE	INTC lamp	ON	
1401	IE	I/O Reg. No. 1 lamps 9, 10, 23 and 24	ON	

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Figure 7-14. Single Step Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME:

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Figure 7-14. Single Step Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1402	TRMC	2^0 and 2^3 lamps	ON	
1405	MLDD	Press and release 0A9		
1406	MLDD	COMMAND 0A9 lamp	OFF	
1410	MLDD	Press and release DS3 and DS4		
1420	MLDD	COMMAND DS3 lamp	OFF	
1430	MLDD	COMMAND DS4 lamp	ON	
1440	MLDD	Press and release ADDRESS COMPTR		
1450	IE	INTC lamp	OFF	
1460	MLDD	Press and release DS4		
1470	MLDD	COMMAND DS4 lamp	OFF	
1480	PC	Press and release COMPUTER POWER SEQ OFF		
1490	PC	COMPUTER POWER SEQ ON lamp	OFF	
1495	MLDD	ON, ADVANCE and CST lamps	OFF	
1496	IE	Some ERROR lamps may light		
1497	MLDD	OFF lamp	ON	
1500	PC	COMPUTER POWER SEQ OFF lamp (delayed)	ON	
1510	PC	Press and release COMP POWER SEQ ON		
1520	PC	COMP POWER SEQ OFF lamp	OFF	
1530	PC	COMP POWER SEQ ON lamp	ON	
1540	IE	Press and release ERROR RESET		
1541	IE	ALL ERROR lamps OFF with the exception of Computer Alarm which may be ON or OFF		
1550	TRMC	Press and release FREE RUN SS		
1560	TRMC	FREE RUN SS lamp	ON	
1561	TRMC	MEMORY SIM lamp	OFF	
1562	TRMC	ML lamp	ON	
1563	IE	Computer HLT lamp	ON	
1570	TRMC	Press and release MEMORY SIM		
1580	TRMC	MEMORY SIM lamp	ON	
1590	TRMC	ML lamp	OFF	
1600	TRMC	Tape Address Counter	Counting	
1610	IE	Press and release OP/TP		
1620	IE	TP lamp	OFF	
1630	IE	OP lamp	ON	
1640	IE	RESET PIOR lamp	Flashing	
1650	IE	COMPTR HALT lamp	Flashing	
1660	MLDD	CST lamp	Flashing	

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Figure 7-14. Single Step Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1670	TRMC	Press and release FREE RUN SS		
1680	TRMC	FREE RUN SS lamp	OFF	
1690	IE	RESET PIOR lamp	ON	
1700	IE	COMPTR HALT lamp	OFF	
1710	MLDD	CST lamp	ON	
1711	TRMC	Tape Address Counter	Stopped	
1720	IE	Press and release OP/TP		
1730	IE	OP lamp	OFF	
1740	IE	TP lamp	ON	
1750	IE	Press and release RESET PIOR		
1760	IE	RESET PIOR lamp	OFF	
1770	MLDD	CST lamp	OFF	
1780	TRMC	Tape Address Counter	Counting	
1785	MLDD	Press and release COMMAND DISPLAY RESET		
1790	MLDD	Press and release ON/OFF		
1800	MLDD	ON, ADVANCE and CST lamps	ON	
1801	MLDD	ALL Computer Data Bits	ON	
1802	IE	I/O Reg. No. 1 lamps 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22, and 23	ON	
1810	TRMC	Tape ADDRESS 2^0 lamp	ON	
1811	TRMC	Press and release ADR 5		
1812	TRMC	ADR 5 lamp	OFF	
1820	MLDD	Press and release A2 and A3 lamps		
1830	MLDD	COMMAND lamps A2 and A3	ON	
1840	MLDD	Press and release ADVANCE/CST		
1850	MLDD	COMPUTER OP2, A2 and A3 lamps	ON	
1851	MLDD	COMMAND A2 and A3 lamps	ON	
1852	MLDD	Computer Data Bits 22, 23, 24 and 25	ON	
1853	MLDD	ON, ADVANCE and CST lamps	ON	
1854	IE	I/O Reg. No. 1 lamps 4, 5, 6, 7, 8, 9, 18, 19, 20, 21, 22 and 23	ON	
1855	TRMC	Address Counter 2^1, 2^2 lamps	ON	
1860	IE	Press and release OP/TP		
1870	IE	TP lamp	OFF	
1880	IE	OP lamp	ON	
1890	MLDD	Press and release ADVANCE/CST		
1900	IE	RESET PIOR lamp	ON	
1901	IE	I/O Reg. No. 1 lamps 9, 10, 23 and 24	ON	
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Figure 7-14. Single Step Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1910	MLDD	COMPUTER A1, A2, A3, OP2 and OP4 lamps	ON	
1911	MLDD	COMMAND A2 and A3 lamps	ON	
1920	MLDD	DATA COMPUTER lamps 22, 23, 24 and 25	ON	
1921	TRMC	Address Counter 2^0, 2^1, and 2^2	ON	
1930	TRMC	Remove Spare Probe from TP28		
1940	MLDD	Press and release DATA Bit Sign		
1950	MLDD	DATA COMMAND SIGN lamp	ON	
1960	MLDD	Press and release ADDRESS COMPTR		
1970	IE	RESET PIOR lamp	OFF	
1980	MLDD	Press and release (8 times) ADVANCE/CST		
1981	MLDD	ON - ADV - CST lamps	ON	
1982	MLDD	Data Command Sign lamp	ON	
1983	MLDD	Computer A5 lamp	ON	
1984	IE	I/O Reg. No. 1 lamps 7 and 21	ON	
1990	IE	RESET PIOR lamp	ON	
1991	TRMC	Address Counter 2^0 and 2^4	ON	
2000	MLDD	Press and release DATA Bits Sign and 25		
2010	MLDD	DATA COMMAND SIGN lamp	OFF	
2020	MLDD	DATA COMMAND 25 lamp	ON	
2030	TRMC	Press and release ADR 5		
2040	TRMC	ADR 5 lamp	ON	
2060	IE	RESET PIOR lamp	OFF (Dim)	
2070	MLDD	ON, ADVANCE and CST lamps	OFF	
2080	IE	COMPTR HALT lamp	ON	
2090	TRMC	Tape Address Counter	Counting	
2100	MLDD	Press and release DATA 25		
2110	MLDD	DATA COMMAND lamp 25	OFF	
2120	MLDD	Press and release DS1		
2130	MLDD	COMMAND DS1 lamp	ON	
2150	IE	COMPTR HALT lamp	OFF	

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Figure 7-14. Single Step Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2160	TRMC	Tape Address Counter	Stopped	
2170	IE	RESET PIOR lamp	ON	
2180	MLDD	CST lamp	ON	
2190	PC	Press and release COMP POWER SEQ OFF		
2200	PC	COMPUTER POWER SEQ ON lamp	OFF	
2210	IE	RESET PIOR lamp	OFF	
2220	MLDD	CST lamp	OFF	
2230	TRMC	MEMORY SIM lamp	OFF	
2240	TRMC	ML lamp	ON	
2250	IE	Computer HALT lamp	ON	
2260	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
2271	IE	Press and release OP/TP		
2272	IE	OP lamp	OFF	
2273	IE	TP lamp	ON	
2280	PC	Press and release COMPUTER POWER SEQ ON switch		
2290	PC	COMPUTER POWER SEQ OFF lamp	OFF	
		COMPUTER POWER SEQ ON lamp	ON	
2300	IF	Press and release ERROR RESET		
2310	TRMC	Press and release MEMORY SIM		
2320	TRMC	MEMORY SIM lamp	ON	
2330	TRMC	ML lamp	OFF	
2350	MLDD	Press and release Data Bit 23		
2360	MLDD	DATA COMMAND 23 lamp	ON	
2370	MLDD	Press and release Address Computer		
2380	MLDD	CST lamp	ON	
2390	MLDD	Press and release Data Bit 23		
2400	MLDD	DATA COMMAND 23 lamp	OFF	
2410	TRMC	Tape Address Counter	Stopped	
2420	MLDD	Press and release Data Bit 24		
2430	MLDD	DATA COMMAND Bit 24 lamp	ON	
2440	MLDD	Press and release Address Computer		
2450	MLDD	CST lamp	OFF	
2460	TRMC	Address Counter	Counting	
2470	MLDD	Press and release Data Bit 24		
2480	MLDD	DATA COMMAND bit 24 lamp	OFF	

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Figure 7-14. Single Step Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2490	MLDD	Press and release Data Bit 23		
2500	MLDD	DATA COMMAND 23 lamp	ON	
2510	MLDD	Press and release Address Computer		
2520	MLDD	CST lamp	ON	
2540	MLDD	Press and release DATA Bits 23 and 25		
2550	MLDD	DATA COMMAND 23 lamp	OFF	
	MLDD	DATA COMMAND 25 lamp	ON	
2560	MLDD	Press and release Address Computer		
2570	MLDD	CST lamp	OFF	
2580	IE	Computer HALT lamp	ON	
2590	TRMC	Address Counter	Counting	
2600	MLDD	Press and release Data Bit 25		
2610	MLDD	DATA COMMAND 25 lamp	OFF	
2640	MLDD	Press and release Address Computer		
2650	IE	Computer HALT lamp	OFF	
2660	MLDD	Press and release 0A6		
2670	MLDD	0A6 Command lamp	ON	
2680	MLDD	ON, CST and ADVANCE lamps	ON	
2690	IE	A6 lamp	ON	
2700	TRMC	Address Counter	Stopped	
2710	MLDD	Press and release 0A6		
2720	MLDD	0A6 Command lamp	OFF	
2730	MLDD	Press and release Data Bit 25		
2740	MLDD	DATA COMMAND lamp 25	ON	
2750	MLDD	Press and release Address Computer		
2760	MLDD	ON, CST and ADVANCE lamps	OFF	
2770	IE	A6 lamp	OFF	
2775	IE	Computer HALT lamp	ON	
2780	TRMC	Address Counter	Counting	
2790	MLDD	Press and release Data Bit 25		
2800	MLDD	DATA COMMAND 25 lamp	OFF	
2830	MLDD	Press and release Address Computer		

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Figure 7-14. Single Step Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2840	IE	Computer HALT lamp	OFF	
2850	MLDD	Press and release DS1		
2860	MLDD	DS1 Command lamp	OFF	
2870	MLDD	Press and release Data Bit 23		
2880	MLDD	DATA COMMAND 23 lamp	ON	
2890	MLDD	Press and release Address Computer		
2900	MLDD	CST lamp	ON	
2910	TRMC	Tape Address Counter	Stopped	
2920	MLDD	Press and release Data Bit 23		
2930	MLDD	DATA COMMAND 23 lamp	OFF	
2940	IE	Press and release OP/TP		
2950	IE	TP lamp	OFF	
2960	IE	OP lamp	ON	
2970	MLDD	Press and release DS 3		
2975	MLDD	DS3 Command lamp	ON	
2980	MLDD	Press and release Address Computer		
2990	IE	RESET PIOR and INTC lamps	ON	
3000	MLDD	Press and release DS3		
3010	MLDD	DS3 Command lamp	OFF	
3020	MLDD	Press and release Data Bit 24		
3030	MLDD	DATA COMMAND 24 lamp	ON	
3040	MLDD	Press and release Address Computer		
3050	MLDD	Press and release Data Bit 24		
3060	MLDD	DATA COMMAND 24 lamp	OFF	
3070	MLDD	Press and release DS4		
3080	MLDD	DS4 Command lamp	ON	
3090	MLDD	Press and release Address Computer		
3100	IE	INTC lamp	OFF	
3110	MLDD	Press and release DS4		
3120	MLDD	DS4 Command lamp	OFF	
3130	IE	Press and release OP/TP		
3140	IE	OP lamp	OFF	
3150	IE	TP lamp	ON	
3160	IE	Press and release RESET PIOR		
3170	IE	RESET PIOR lamp	OFF	
3180	MLDD	CST lamp	OFF	
3190	TRMC	Address Counter	Counting	
3200	PC	Press and release COMP POWER SEQ OFF		
3210	PC	COMP POWER SEQ ON lamp	OFF	

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Figure 7-14. Single Step Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3220	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
3230	PC	Press and release ACME POWER SEQ OFF		
3240	PC	ACME POWER SEQ ON lamp	OFF	
3250	PC	ACME POWER SEQ OFF lamp	ON	
3260	PC	Press and release Main Power OFF		
3270	PC	POWER ON lamp	OFF	
3280	PC	POWER OFF lamp	ON	
3290	PC	Pull Emergency Pull		
3300	PC	POWER OFF lamp	OFF	
3310	01A	Remove jumper plug from J29 and connect cable from J28 to J29		
3320	PC	Press Emergency Pull		
3330	PC	POWER OFF lamp	ON	
3340	PC	Press and release Main Power ON		
3350	PC	POWER OFF lamp	OFF	
3360	PC	POWER ON lamp	ON	
3370	PC	ACME and COMPUTER POWER SEQ OFF lamps	ON	
3380	PC	Phase A, B, C and Fan lamps	ON	
3390	PC	Press and release ACME POWER SEQ ON		
3400	PC	ACME POWER SEQ OFF lamp	OFF	
3410	PC	ACME POWER SEQ ON lamp	ON	
3420	PC	Press and release COMPUTER POWER SEQ ON		
3430	PC	COMPUTER POWER SEQ OFF lamp	OFF	
3440	PC	COMPUTER POWER SEQ ON lamp	ON	
3450	MLDD	ON lamp	ON	
3460	IE	INTC lamp	ON	
3470	TRMC	DD lamp	ON	
3480	IE	Press and release ERROR RESET		
3490	IE	ERROR lamps	OFF	
3500	TRMC	Press and release MEMORY SIM		
3510	TRMC	DD lamp	OFF	
3520	TRMC	MEMORY SIM lamp	ON	
3530	TRMC	Press and release ADR 5		
3531	TRMC	ADR 5 lamp	ON	
3540	MLDD	Press and release DS 4		
3550	MLDD	COMMAND DS4 lamp	ON	
3551	MLDD	If SINGLE lamp is ON, press and release REPEAT/SINGLE		
3552	MLDD	REPEAT lamp	ON	

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Figure 7-14. Single Step Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3560	MLDD	CST lamp	OFF	
3570	MLDD	Press and release Address Computer		
3580	IE	INTC lamp	OFF	
3590	MLDD	Press and release DS4		
3600	MLDD	DS4 Command lamp	OFF	
3610	MLDD	ON, ADVANCE and CST lamps	ON	
3611	TRMC	Address Counter	Stopped	
3620	MLDD	Press and release ON/OFF		
3630	MLDD	OFF lamp	ON	
3640	MLDD	ON, CST and ADVANCE lamps	OFF	
3650	TRMC	Address Counter	Counting	
3651	TRMC	Place Spare Probe in TP28		
3652	MLDD	ALL Data Computer Bits	ON	
3660	MLDD	Press and release IS3		
3670	MLDD	IS3 Command lamp	ON	
3680	MLDD	CST, ON and ADVANCE lamps	ON	
3690	TRMC	Address Counter	Stopped	
3700	MLDD	Press and release IS3		
3710	MLDD	IS3 Command lamp	OFF	
3720	MLDD	Press and release IS1		
3730	MLDD	IS1 Command lamp	ON	
3740	MLDD	ADVANCE lamp	OFF	
3750	MLDD	CST lamp (Dim)		
3760	MLDD	ALL Data Computer Bits	ON	
3780	TRMC	Address Counter	Counting	
3790	MLDD	Press and release IS 1		
3800	MLDD	IS1 Command lamp	OFF	
3810	MLDD	ON, CST and ADVANCE lamps	ON	
3820	TRMC	Address Counter	Stopped	
3821	TRMC	GND Scope to ACME		
3822	TRMC	Place Scope probe in TP 46	Approx. 0VDC	
3823	TRMC	Place Scope probe in TP 47	Approx. 0VDC	
3830	MLDD	Press and release ON/OFF		
3840	MLDD	OFF lamp	ON	
3850	MLDD	ON, CST and ADVANCE lamps	OFF	
3860	TRMC	Address Counter	Counting	
3870	MLDD	ALL Data Computer bits	ON	
3871	TRMC	Place Scope Probe in TP 46	Approx. -12VDC	
3872	TRMC	Place Scope Probe in TP 47	-12V	
3873	TRMC	Remove Scope probe and GND from TP's	DCO-64-941	

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Figure 7-14. Single Step Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3880	MLDD	Press and release IS4		
3890	MLDD	IS4 Command lamp	ON	

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Figure 7-14. Single Step Checks (Sheet 17)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3900	MLDD	CST lamp	ON	
4000	TRMC	Address Counter	Stopped	
4020	MLDD	Press and release IS4		
4030	MLDD	IS4 Command lamp	OFF	
4040	MLDD	CST lamp	OFF	
4050	MLDD	ALL Computer Data lamps	ON	
4060	TRMC	Address Counter	Counting	
4070	TRMC	Remove Spare Probe from TP 28		
4080	PC	Press and release COMPUTER POWER SEQ OFF		
4090	PC	COMPUTER POWER SEQ ON lamp	OFF	
4100	PC	COMPUTER POWER SEQ OFF lamp (delayed)	ON	
4110	PC	Press and release ACME POWER SEQ OFF		
4120	PC	ACME POWER SEQ ON lamp	OFF	
4130	PC	ACME POWER SEQ OFF lamp	ON	
4140	PC	Press and release POWER OFF		
4150	PC	POWER ON lamp	OFF	
4160	PC	POWER OFF lamp	ON	
4170	PC	Pull Emergency Pull		
4180	PC	POWER OFF lamp	OFF	
4190	01A	Remove cable from J28 to J29 and connect Jumper plug to J29.		
4200	PC	Push Emergency Pull switch		
4210	PC	POWER OFF lamp	ON	
4220	PC	Press and release POWER ON		
4230	PC	POWER OFF lamp	OFF	
4240	PC	POWER ON, Phase A, B, C, FAN, ACME and COMPUTER POWER OFF lamps	ON	
4250	PC	Press and release ACME POWER SEQ ON		
4260	PC	ACME POWER SEQ OFF lamp	OFF	
4270	PC	ACME POWER SEQ ON lamp	ON	
4280	PC	Press and release COMPUTER POWER SEQ ON		
4290	PC	COMPUTER POWER SEQ OFF lamp	OFF	
4300	PC	COMPUTER POWER SEQ ON lamp	ON	

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Figure 7-14. Single Step Checks (Sheet 18)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4310	MLDD	Press and release ERROR OVER RIDE		
4315	MLDD	ERROR OVER RIDE	ON	
4320	MLDD	Press and release COMPUTER DISPLAY RESET and COMMAND DISPLAY RESET		
4325	IE	Press and release ERROR RESET		
4330	IE	All ERROR lamps	OFF	
4335	TRMC	Press and release MEMORY SIM		
4340	TRMC	MEMORY SIM lamp	ON	
4345	TRMC	ML lamp	OFF	
4350	MLDD	Turn DISPLAY SELECT switch to AI3 DATA		
4360	MLDD	Press and release 0A9, A2 and A3		
4370	MLDD	COMPUTER and COMMAND 0A9, COMMAND A2 and A3	ON	
4380	MLDD	Press and release Address Computer		
4390	MLDD	Press and release SYL1		
4400	MLDD	Computer SYL1, OP2, A2 and A3 lamps	ON	

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Figure 7-14. Single Step Checks (Sheet 19)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4410	MLDD	COMMAND SYL1	ON	
4420	MLDD	COMPUTER and COMMAND SYL0	OFF	
4430	MLDD	Data Computer Bits 9, 10, 23 and 24	ON	
4440	MLDD	Press and release A3 and A4		
4450	MLDD	COMMAND A3 lamp	OFF	
4460	MLDD	COMMAND A4 lamp	ON	
4470	MLDD	Press and release SYL1		
4480	MLDD	SYL1 COMPUTER and COMMAND lamps	OFF	
4490	MLDD	SYL0 COMPUTER and COMMAND lamps	ON	
4500	MLDD	A4, OP3, and 0A9 Computer lamps	ON	
4510	MLDD	A3 COMPUTER lamp	OFF	
4520	MLDD	Data computer bits 8, 9, 22, 23 lamps	ON	
4530	MLDD	Press and release A1		
4540	MLDD	COMMAND A1 lamp	ON	
4550	MLDD	Press and release SYL1		
4560	MLDD	SYL1 COMMAND and COMPUTER lamps	ON	
4570	MLDD	SYL0 COMMAND and COMPUTER lamps	OFF	
4580	MLDD	COMPUTER A1 and OP4 lamps	ON	
4590	MLDD	Data Computer 8, 9, 22 and 23 lamps	ON	
4600	MLDD	Press and release A1 and SYL1		
4610	MLDD	Computer and Command A1 and SYL1	OFF	
4620	MLDD	COMPUTER OP4	OFF	
4630	MLDD	Computer and Command SYL0	ON	
4640	MLDD	Data Computer 8, 9, 22 and 23	ON	

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Figure 7-14. Single Step Checks (Sheet 20)

INTERNATIONAL BUSINESS MACHINES

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4650	MLDD	Press and release A7, A2 and A1		
4660	MLDD	COMMAND and COMPUTER A7 and A1 lamps	ON	
4670	MLDD	COMMAND and COMPUTER A2 lamp	OFF	
4680	MLDD	DATA COMPUTER 5, 8, 9, 19, 22 and 23 lamps	ON	
4690	MLDD	COMPUTER OP1, OP3, and OP4 lamps	ON	
4700	MLDD	Press and release COMPUTER CONTROL ON/OFF		
4710	MLDD	OFF lamp	OFF	
4720	MLDD	ON, ADVANCE and CST lamps	ON	
4730	TRMC	Tape Address Counter	Stopped	
4740	MLDD	Press and release A2		
4750	MLDD	COMMAND A2 lamp	ON	
4760	MLDD	Press and release SYL0/1		
4770	MLDD	COMMAND SYL1 lamp	ON	
4780	MLDD	COMMAND SYL0 lamp	OFF	
4790	MLDD	Press and release ADVANCE/CST		
4800	MLDD	COMPUTER OP3, OP4, A2 and SYL1 lamps	ON	
4810	MLDD	Press and release SYL 0/1 and A2		
4820	MLDD	COMMAND SYL1 and A2 lamps	OFF	
4830	MLDD	COMMAND SYL0 lamp	ON	
4840	MLDD	Press and release ADVANCE/CST		
4850	MLDD	COMPUTER SYL1 and A2 lamps	OFF	
4860	MLDD	COMPUTER SYL0, OP1 OP3, and OP4 lamps	ON	
4870	MLDD	DATA COMPUTER 5, 8, 11, 19, 22 and 25 lamps only	ON	
4880	MLDD	Press and release 0A7 and A2		
4890	MLDD	COMMAND 0A7 and A2 lamps	ON	
4900	MLDD	Press and release ADDRESS COMPTR		
4910	MLDD	All DATA COMPUTER lamps	OFF	
4920	MLDD	Press and release ADVANCE/CST		
4930	MLDD	COMPUTER 0A7 and A2 lamps	ON	
4940	MLDD	DATA COMPUTER lamps 11 and 25	ON	
4950	MLDD	COMPUTER OP1 lamp	OFF	

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Figure 7-14. Single Step Checks (Sheet 21)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4960	MLDD	Press and release A1		
4970	MLDD	COMMAND A1 lamp	OFF	
4980	MLDD	Press and release ADVANCE/CST		
4990	MLDD	COMPUTER OP4 lamp	OFF	
5000	MLDD	DATA COMPUTER 5, 8, 10, 19, 22 and 24 lamps only	ON	
5010	MLDD	Press and release A2 and A3		
5020	MLDD	COMMAND A3 lamp	ON	
5030	MLDD	COMMAND A2 lamp	OFF	
5040	MLDD	Press and release ADVANCE/CST		
5050	MLDD	COMPUTER A3 lamp	ON	
5060	MLDD	COMPUTER A2 and OP3 lamps	OFF	
5070	MLDD	DATA COMPUTER 10 and 24 lamps only	ON	
5080	MLDD	Press and release A2 an d A3		
5100	MLDD	COMMAND A2 lamp	ON	
5110	MLDD	COMMAND A3 lamp	OFF	
5120	MLDD	Press and release ADVANCE/CST		
5130	MLDD	COMPUTER OP3 and A2 lamps	ON	
5140	MLDD	COMPUTER A3 lamp	OFF	
5150	MLDD	DATA COMPUTER 5, 8, 10, 19, 22 and 24 lamps only	ON	
5160	MLDD	Press and release DATA SIGN		
5170	MLDD	DATA COMMAND SIGN lamp	ON	
5180	MLDD	Press and release ADDRESS COMPTR		
5190	MLDD	DATA COMMAND and COMPUTER SIGN lamp only	ON	
5200	MLDD	Press and release A2 , A3 and SYL 0/1		
5210	MLDD	COMMAND A3 and SYL1 lamps	ON	
5220	MLDD	COMMAND A2 and SYL0 lamps	OFF	
5230	MLDD	Press and release DATA SIGN		
5240	MLDD	DATA COMMAND SIGN lamp	OFF	
5250	MLDD	Press and release ADVANCE/CST		
5260	MLDD	COMPUTER A3 and SYL1 lamps	ON	
5270	MLDD	COMPUTER A2 and OP3 lamps	OFF	
5280	MLDD	DATA COMPUTER SIGN lamp	OFF	
5290	MLDD	DATA COMPUTER 10 and 24 lamps only	ON	

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Figure 7-14. Single Step Checks (Sheet 22)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
5300	MLDD	Press and release COMPUTER CONTROL ON/OFF		
5310	MLDD	OFF lamp	ON	
5320	MLDD	ON, ADVANCE and CST lamps	OFF	
5330	MLDD	Press and release COMMAND DISPLAY RESET		
5340	MLDD	All COMMAND and COMPUTER lamps	OFF	
5350	MLDD	Press and release A2, A3, A5 and A8		
5360	MLDD	COMMAND and COMPUTER A2, A3 A5, A8 and COMPUTER OP2 and OP3 lamps	ON	
5370	MLDD	DATA COMPUTER 4, 7, 9, 10, 18, 21 23 and 24 lamps only	ON	
5380	MLDD	Press and release COMPUTER CONTROL ON/OFF		
5390	MLDD	OFF lamp	OFF	
5400	MLDD	ON, ADVANCE and CST lamps	ON	
5410	MLDD	Press and release ADVANCE/CST		
5420	MLDD	COMPUTER A1, A2, A3, A5, A8, DS2, OP2, OP3 and OP4	ON	
5430	MLDD	DATA COMPUTER Lamps 4, 7, 9, 10, 11, 18, 21, 23, 24, and 25	ON	
5440	MLDD	Press and release ADVANCE/CST		
5450	MLDD	COMPUTER A4, A5, A8, DS2 and OP1	ON	
5460	MLDD	DATA COMPUTER 4, 7, 8, 18, 21, and 22 lamps only	ON	
5470	MLDD	Press and release PAST/PRESENT		
5480	MLDD	PRESENT and ADVANCE lamps	OFF	
5490	MLDD	PAST lamp	ON	
5500	MLDD	DATA COMPUTER 4, 8, 10, 11, 18, 22 24 and 25 lamps only	ON	
5510	MLDD	Turn WORD to T-1		
5520	MLDD	COMPUTER A1, A2, A3, A5, A8, DS2, OP2, OP3 and OP4 lamps	ON	
5530	MLDD	DATA COMPUTER 4, 7, 9, 10, 11, 18, 21, 23, 24, and 25 lamps only	ON	
5540	MLDD	Press and release PAST/PRESENT		
5550	MLDD	PAST lamp	OFF	

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Figure 7-14. Single Step Checks (Sheet 23)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
5560	MLDD	PRESENT and ADVANCE lamps	ON	
5570	MLDD	DATA COMPUTER 4, 7, 8, 18, 21 and 22 lamps only	ON	
5580	MLDD	Press and release (2 times) COMPUTER CONTROL ON/OFF		
5590	MLDD	COMPUTER and COMMAND A2, A3, A5, A8 and COMPUTER OP2 and OP3 lamps	ON	
5600	MLDD	DATA COMPUTER 4, 7, 9, 10, 18, 21, 23, and 24 lamps only	ON	
5610	MLDD	Press and release 0A1, 0A2, 0A8 and 0A9		
5620	MLDD	COMMAND 0A1, 0A2, 0A8 and 0A9 lamps	ON	
5630	MLDD	Press and release ADVANCE/CST		
5640	MLDD	COMPUTER A1, A2, A3, A5, A8, DS2, 0A1, 0A2, 0A8, 0A9, OP2, OP3 and OP4 lamps	ON	
5650	MLDD	DATA COMPUTER 4, 7, 8, 18, 21 and 22 lamps only	ON	
5660	MLDD	Press and release PAST/PRESENT		
5670	MLDD	PRESENT and ADVANCE lamps	OFF	
5680	MLDD	PAST lamp	ON	
5690	MLDD	DATA COMPUTER 4, 7, 9, 10, 11, 18, 21, 23, 24 and 25 lamps only	ON	
5700	MLDD	Turn WORD to T		
5710	MLDD	COMPUTER A4, A5, A8, DS1, DS2, 0A1, 0A2, 0A8, 0A9 and OP1 lamps	ON	
5720	MLDD	DATA COMPUTER 4, 8, 10, 11, 18, 22, 24 and 25 lamps only	ON	
5730	MLDD	Press and release PAST/PRESENT		
5740	MLDD	PAST lamp	OFF	
5750	MLDD	PRESENT and ADVANCE lamps	ON	
5760	MLDD	DATA COMPUTER 4, 7, 8, 18, 21 and 22 lamps only	ON	
5770	MLDD	Press and release COMPUTER CONTROL ON/OFF		
5780	MLDD	ON, ADVANCE and CST lamps	OFF	
5790	MLDD	OFF lamp	ON	
5800	MLDD	Press and release COMMAND DISPLAY RESET		

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Figure 7-14. Single Step Checks (Sheet 24)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
5810	TRMC	Press and release MEMORY SIM		
5820	TRMC	MEMORY SIM lamp	OFF	
5830	TRMC	ML lamp	ON	

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Figure 7-14. Single Step Checks (Sheet 25)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	IE	TP lamp (Press and release TP/OP if OFF)	ON	
20	MLDD	DISPLAY SERIAL OUT lamp (Press and release if ON)	OFF	
30	TRMC	Press and release MEMORY SIM		
40	TRMC	MEMORY SIM lamp	ON	
50	TRMC	Tape Address Counter	Counting	
60	MLDD	Press and release A5 and A6		
70	MLDD	COMMAND and COMPUTER A5 and A6 lamps	ON	
80	MLDD	Press and release SINGLE STEP ON/OFF		
90	MLDD	ON, ADVANCE and CST lamps	ON	
100	IE	I/O Reg. No. 2 lamps (Press and release if OFF)	ON	
105	IE	Press and release I/O Reg. RESET		
106	IE	All I/O Reg. No. 2 lamps	OFF	
110	IE	Press and release Bit 19		
120	IE	I/O Reg. No. 2 Bit 19 lamp	ON	
121	MLDD	Press and release DATA 12, 13 and 14		
122	MLDD	DATA, COMMAND lamps 12, 13 and 14		
123	MLDD	Press and release ERROR OVER RIDE (if OFF)		
124	MLDD	ERROR OVER RIDE lamp	ON	
125	MLDD	Press and release COMPTR DISPLAY RESET		
126	IE	Press and release ERROR RESET		
127	IE	All ERROR lamps	OFF	
130	MLDD	Press and release ADVANCE/CST (11 times)		

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Figure 7-15. Past History Mode Checks (Sheet 1 of 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
140	MLDD	PRESS and hold PAST/PRESENT		
141	MLDD	PAST LAMP	ON	
142	MLDD	RELEASE PAST/PRESENT		
143	MLDD	PAST LAMP	ON	
144	MLDD	PRESS and hold PAST/PRESENT		
145	MLDD	PAST LAMP	OFF	
146	MLDD	PRESENT LAMP	ON	
147	MLDD	RELEASE PAST/PRESENT		
148	MLDD	PRESENT LAMP	ON	
149	MLDD	PRESS AND RELEASE PAST/ PRESENT		
150	MLDD	PAST LAMP	ON	
160	MLDD	Turn Display Select to AI3 Data		
170	MLDD	Turn WORD switch to T-1		
180	MLDD	DATA lamps 6, 7, 8, 9, 11, 20, 21, 22, 23, 25, and IS4, IS3, IS2, IS1, DM3, DM2, DM1, DX, OP4, OP2, A1, A3, A4, A5 and A6	ON	
190	MLDD	Turn WORD switch to T-2		
200	MLDD	DATA lamps 6, 7, 8, 9, 20, 21, 22 and 23	ON	
210	MLDD	Turn WORD switch to T-3		
220	MLDD	DATA lamps 6, 7, 8, 10, 11, 20, 21, 22, 24 and 25	ON	
230	MLDD	Turn WORD switch to T-4		
240	MLDD	DATA lamps 6, 7, 8, 10, 20, 21, 22 and 24	ON	
250	MLDD	Turn WORD switch to T-5		
260	MLDD	DATA lamps 6, 7, 8, 11, 20, 21, 22 and 25	ON	
270	MLDD	Turn WORD switch to T-6		
280	MLDD	DATA lamps 6, 7, 8, 20, 21 and 22	ON	
290	MLDD	Turn WORD switch to T-7		
300	MLDD	DATA lamps, 6, 7, 9, 10, 11, 20, 21, 23, 24, and 25	ON	
310	MLDD	Turn WORD switch to T-8		
320	MLDD	DATA lamps 6, 7, 9, 10, 20, 21, 23 and 24	ON	

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Figure 7-15. Past History Mode Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
330	MLDD	Turn WORD switch to T-9		
340	MLDD	DATA lamps 6, 7, 9, 11, 20, 21, 23 and 25	ON	
350	MLDD	Turn WORD switch to T-10		
360	MLDD	DATA lamps 6, 7, 9, 20, 21 and 23	ON	
370	MLDD	Turn WORD switch to T-11		
380	MLDD	DATA lamps 6, 7, 10, 11, 20, 21, 24 and 25	ON	
390	MLDD	Turn WORD switch to T-12		
400	MLDD	DATA lamps 6, 7, 10, 20, 21 and 24	ON	
401	MLDD	Turn WORD switch to T-13		
402	MLDD	DATA lamps 6, 7, 8, 10, 20, 21, 22 and 24	ON	
403	MLDD	Turn WORD switch to T-14		
404	MLDD	DATA lamps 6, 7, 8, 10, 20, 21, 22 and 24	ON	
405	MLDD	Turn WORD switch to T-15		
406	MLDD	DATA lamps 6, 7, 8, 10, 20, 21, 22 and 24	ON	
410	MLDD	Turn DISPLAY SELECT to TRS		
420	MLDD	Turn WORD switch (CCW) to T		
430	MLDD	DATA lamps 6, 7, 8, 9, 10, 20, 21, 22, 23, and 24	ON	
440	MLDD	Turn WORD switch to T-1		
450	MLDD	DATA lamps 6, 7, 8, 9, 11, 20, 21, 22, 23 and 25	ON	
460	MLDD	Turn DISPLAY SELECT TO MR1		
470	MLDD	DATA lamp 19	ON	
480	MLDD	Turn DISPLAY SELECT TO MD7		
490	MLDD	DATA lamp 24	ON	
500	MLDD	Turn DISPLAY SELECT to PRO		

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Figure 7-15. Past History Mode Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
520	MLDD	DATA lamps 18, 19 and 20	ON	
530	MLDD	Turn WORD switch to T-2		
540	MLDD	DATA lamps 4, 5 and 6	ON	
550	MLDD	Press and release COMPUTER CONTROL (ON/OFF)		
555	MLDD	PAST lamp	OFF	
560	MLDD	ON, ADVANCE and CST lamps	OFF	
570	MLDD	OFF lamp	ON	
580	MLDD	Press and release A1, A2, A3, A5 and A6		
590	MLDD	COMMAND A5 and A6 lamps	OFF	
600	MLDD	COMMAND A1, A2 and A3 lamps	ON	
610	MLDD	COMPUTER A1, A2 and A3 lamps	ON	
620	MLDD	Press and release COMPUTER CONTROL ON/OFF		
630	MLDD	OFF lamp	OFF	
640	MLDD	ON, ADVANCE and CST lamps	ON	
650	IE	Press and release I/O Reg. Reset		
660	IE	I/O Reg. No. 2 lamps all	OFF	
670	MLDD	Press and release DATA 12, 13 and 14		
680	MLDD	DATA COMMAND lamps all	OFF	
690	MLDD	Press and release ADVANCE/CST (3 times)		
700	MLDD	COMPUTER A4, and A2 lamps	ON	
710	MLDD	Turn DISPLAY SELECT to MD7		
730	MLDD	All DATA lamps	OFF	
740	MLDD	Turn DISPLAY SELECT to MR1		
760	MLDD	All DATA lamps	OFF	
770	MLDD	Turn DISPLAY SELECT to PRO		
790	MLDD	All DATA lamps	OFF	
800	MLDD	Press and release DATA 12, 13 and 14		
810	MLDD	DATA COMMAND lamps 12, 13 and 14	ON	
820	IE	Press and release I/O Reg. 4, 7, 10, 13, 16, 19, 22 and 25		
830	IE	I/O Reg. No. 2 lamps 4, 7, 10, 13, 16, 19, 22 and 25	ON	

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Figure 7-15. Past History Mode Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
980	MLDD	Press and release ADVANCE/CST		
990	MLDD	Verify that lamps OP1, OP2, A2 A3 and A4 are ON If OFF, return to step 980	ON	
1000	MLDD	Press and release PAST/PRESENT		
1010	MLDD	PRESENT lamp	OFF	
1020	MLDD	PAST lamp	ON	
1030	MLDD	Turn DISPLAY SELECT to PRO		
1031	MLDD	Turn WORD to T		
1040	MLDD	DATA lamps 18, 19 and 20	ON	
1050	MLDD	Turn WORD to T-1		
1060	MLDD	DATA lamps 15, 16 and 17	ON	
1070	MLDD	Turn WORD to T-2		
1080	MLDD	DATA lamps 1, 2 and 3	ON	
1210	MLDD	Turn WORD to T		
1220	MLDD	Turn DISPLAY SELECT to MD7		
1230	MLDD	DATA lamps 7, 10, 13, 16, 19, 22 and 25	ON	
1240	MLDD	Turn WORD to T-1		
1250	MLDD	DATA lamps 1, 6, 9, 12, 15, 18, 21 and 24	ON	
1480	MLDD	Turn DISPLAY SELECT to MR1		
1490	MLDD	Turn WORD to T		
1500	MLDD	DATA lamps SIGN, 3, 6, 9, 12, 15, 18 and 21	ON	
1510	MLDD	Turn WORD to T-1		
1520	MLDD	DATA lamps SIGN, 3, 8, 11, 14, 17 20 and 23	ON	
1760	MLDD	Turn WORD to T		

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Figure 7-15. Past History Mode Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1770	MLDD	Press and release PAST/PRESENT		
1780	MLDD	PAST lamp	OFF	
1790	MLDD	PRESENT lamp	ON	
1800	MLDD	Press and release (2 times) ADVANCE/CST		
1810	MLDD	A5 lamp	ON	
1820	MLDD	Press and release PAST/PRESENT		
1830	MLDD	PRESENT lamp	OFF	
1840	MLDD	PAST lamp	ON	
1850	MLDD	Turn WORD to T-1		
1860	MLDD	Turn DISPLAY SELECT to MD7		
1870	MLDD	DATA lamps 1, 6, 9, 12, 15, 18, 21 and 24	ON	
1880	MLDD	Turn DISPLAY SELECT to MR1		
1890	MLDD	DATA lamps SIGN, 3, 8, 11, 14, 17 20 and 23	ON	
1900	MLDD	Turn DISPLAY SELECT to PRO		
1910	MLDD	DATA lamps 15, 16 and 17	ON	
1920	MLDD	Turn WORD to T-8		
1930	MLDD	DATA lamps 1, 2, and 3	ON	
1940	MLDD	Turn DISPLAY SELECT to MR1		
1950	MLDD	DATA lamps 2, 5, 10, 13, 16, 19 22 and 25	ON	
1960	MLDD	Turn DISPLAY SELECT to MD7		
1970	MLDD	DATA lamps SIGN, 3, 6, 9, 12, 15, 20 and 23	ON	
1980	MLDD	Turn DISPLAY SELECT to AI3 DATA		
1990	MLDD	Turn WORD to T		
2000	MLD D	Press and release PAST/PRESENT		
2010	MLDD	PAST LAMP	OFF	
2020	MLDD	PRESENT LAMP	ON	
2030	MLDD	Press ON/OFF		
2031	MLDD	OFF lamp	ON	

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Figure 7-15. Past History Mode Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2040	MLDD	ON, ADVANCE and CST lamps	OFF	
2050	MLDD	Press and release A1, A2, A3, A4 and A5		
2060	MLDD	COMMAND and COMPUTER A5 and A4 lamps	ON	
2070	MLDD	Press and release COMPUTER CONTROL ON/OFF		
2080	MLDD	ON, ADVANCE and CST lamps	ON	
2090	MLDD	Turn DISPLAY SELECT TO MR1		
2100	MLDD	Press and release PAST/PRESENT		
2200	MLDD	PAST lamp	ON	
2300	MLDD	PRESENT lamp	OFF	
2530	MLDD	Turn WORD to T-3		
2540	MLDD	DATA lamps SIGN, 3, 6, 9, 12, 15 18 and 21	ON	
2550	MLDD	Turn WORD to T-4		
2560	MLDD	DATA lamps 1, 4, 7, 10, 13, 16, 19, and 24	ON	
2570	MLDD	Turn WORD to T-5		
2580	MLDD	DATA lamps 2, 5, 8, 11, 14, 17, 22 and 25	ON	
2590	MLDD	Turn WORD to T-6		
2600	MLDD	DATA lamps SIGN, 3, 6, 9, 12, 15, 20 and 23	ON	
2630	MLDD	Turn DISPLAY SELECT to MD7		
2640	MLDD	DATA lamps 2, 5, 8, 11, 14, 19, 22 and 25	ON	
2650	MLDD	Turn WORD to T-7		
2660	MLDD	DATA lamps 1, 4, 7, 10, 13, 16, 21, and 24	ON	

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Figure 7-15. Past History Mode Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2730	MLDD	Press and release PAST/PRESENT		
2740	MLDD	PAST lamp	OFF	
2750	MLDD	PRESENT lamp	ON	
2770	MLDD	Turn WORD to T		
2780	MLDD	Press and release (10 Times) ADVANCE / CST		
2790	MLDD	COMPUTER A2, A3 and A6 lamps	ON	
2791	MLDD	Press and release PAST /PRESENT		
2792	MLDD	PRESENT lamp	OFF	
2793	MLDD	PAST lamp	ON	
2800	MLDD	DATA lamps 7, 10, 13, 16, 19, 22 and 25	ON	
2810	MLDD	Turn DISPLAY SELECT to MR1		
2815	MLDD	Turn WORD to T-1		
2820	MLDD	DATA lamps 4, 7, 10, 13, 16, 19, 22 and 25	ON	
2830	MLDD	Turn DISPLAY SELECT to PRO		
2840	MLDD	DATA lamps 18, 19 and 20	ON	
2850	MLDD	Turn DISPLAY SELECT to AI3 DATA		
2860	MLDD	Press and release COMPUTER CONTROL ON/OFF		
2870	MLDD	ON, ADVANCE and CST lamps	OFF	
2875	MLDD	PAST lamp	OFF	
2876	MLDD	PRESENT lamp	ON	
2880	MLDD	Press and release A5 and A6		
2890	MLDD	COMMAND A5 lamp	OFF	
2900	MLDD	COMMAND A4 and A6 lamps	ON	
2910	MLDD	COMPUTER A4 and A6 lamps	ON	
2930	MLDD	Turn DISPLAY SELECT to PRO		
2940	MLDD	Press and release COMPUTER CONTROL ON/OFF		
2950	MLDD	ON, ADVANCE and CST lamps	ON	
2960	MLDD	Press and release PAST /PRESENT		
2970	MLDD	PAST lamp	ON	
2980	MLDD	PRESENT lamp	OFF	
3030	MLDD	All DATA COMPUTER lamps	OFF	
3040	MLDD	Turn DISPLAY SELECT to MR1		

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Figure 7-15. Past History Mode Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3050	MLDD	All DATA COMPUTER lamps	OFF	
3051	MLDD	Press and release PAST/PRESENT		
3052	MLDD	PAST lamp	OFF	
3053	MLDD	PRESENT lamp	ON	
3060	MLDD	Press and release ADVANCE/CST		
3070	MLDD	COMPUTER A1, A4 and A6 lamps	ON	
3080	MLDD	Turn DISPLAY SELECT to MD7		
3090	MLDD	All DATA COMPUTER lamps	OFF	
3100	MLDD	Turn DISPLAY SELECT to PRO		
3110	MLDD	All DATA COMPUTER lamps	OFF	
3120	MLDD	Turn DISPLAY SELECT to AI3 DATA		
3130	MLDD	Turn WORD to T		
3140	MLDD	Press and release COMPUTER CONTROL ON/OFF		
3150	MLDD	ON, ADVANCE and CST lamps	OFF	
3210	MLDD	Press and release 0A9		
3211	MLDD	Press and release ERROR OVER RIDE		
3212	MLDD	ERROR OVER RIDE lamp	OFF	
3212	MLDD	COMMAND 0A9 lamp	ON	
3214	IE	COMPTR ALARM lamp	OFF	
3240	MLDD	Press and release 0A9		
3250	MLDD	COMMAND 0A9 lamp	OFF	
3260	IE	COMPTR ALARM lamp	ON	
3270	MLDD	Press and release 0A9		
3280	MLDD	COMMAND 0A9 lamp	ON	
3290	MLDD	Press and release COMPTR DISPLAY RESET		
3300	IE	Press and release ERROR RESET		
3310	IE	COMPTR ALARM lamp	OFF	
3320	MLDD	Press and release 0A1		
3330	MLDD	COMMAND 0A1 lamp	ON	
3340	IE	COMPTR ALARM lamp	ON	
3350	MLDD	Press and release 0A1		

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Figure 7-15. Past History Mode Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3360	MLDD	COMMAND 0A1	OFF	
3370	MLDD	Press and release COMPTR DISPLAY RESET		
3380	IE	Press and release ERROR RESET		
3390	IE	COMPTR ALARM lamp	OFF	
3400	MLDD	Press and release 0A2		
3410	MLDD	COMMAND 0A2 lamp	ON	
3420	IE	COMPTR ALARM lamp	ON	
3430	MLDD	Press and release 0A2		
3440	MLDD	COMMAND 0A2 lamp	OFF	
3450	MLDD	Press and release COMPTR DISPLAY RESET		
3460	IE	Press and release ERROR RESET		
3470	IE	COMPTR ALARM lamp	OFF	
3480	IE	MANUAL HALT lamp (Press and release)	ON	
3490	MLDD	Press and release 0A9		
3500	MLDD	COMMAND 0A9 lamp	OFF	
3510	IE	COMPTR ALARM lamp	OFF	
3520	MLDD	Press and release DISPLAY SERIAL OUT		
3530	MLDD	DISPLAY SERIAL OUT lamp	ON	
3540	IE	COMPTR ALARM lamp	ON	
3550	MLDD	Press and release DISPLAY SERIAL OUT		
3560	MLDD	DISPLAY SERIAL OUT lamp	OFF	
3570	IE	Press and release MANUAL HALT lamp		
3571	IE	MANUAL HALT lamp	OFF	
3572	MLDD	Press and release ERROR OVER RIDE		
3573	MLDD	ERROR OVER RIDE lamp	ON	

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Figure 7-15. Past History Mode Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3580	MLDD	Press and release COMPTR DISPLAY RESET		
3590	IE	Press and release ERROR RESET		
3600	IE	COMPTR ALARM lamp	OFF	
3630	IE	Press and release I/O Reg. Reset		
3640	IE	All I/O REG. NO 2 lamps	OFF	
3650	MLDD	Press and release COMMAND DISPLAY RESET		
3660	MLDD	All DATA COMMAND lamps	OFF	
3670	MLDD	Press and release A1, A6, IS4 and DM3		
3680	MLDD	COMMAND and COMPUTER A1, A6, IS4 and DM3	ON	
3690	MLDD	Press and release SINGLE STEP ON/OFF		
3700	MLDD	ON, ADVANCE and CST lamps	ON	
3710	MLDD	Press and release ERROR OVER RIDE		
3720	MLDD	ERROR OVER RIDE lamp	OFF	
3730	IE	Press and release I/O Reg. 4, 7, 10, 13, 16, 19, 22 and 25		
3740	IE	I/O Reg. No. 2 lamps 4, 7, 10, 13, 16, 19, 22 and 25	ON	
3750	MLDD	Press and release DATA COMMAND 12, 13 and 14		
3760	MLDD	DATA COMMAND lamps 12, 13, 14	ON	
3770	MLDD	Press and release A1, A2, A3, A4, IS4 and DM3		
3780	MLDD	COMMAND IS4 and DM3 lamps	OFF	
3790	MLDD	COMMAND lamps A2, A3, A4, and A6	ON	
3800	MLDD	Press and release ADVANCE/CST		
3810	MLDD	COMPUTER Address A2, A3, A4 and A6	ON	
3820	IE	INTC and COMPUTER ALARM lamps	ON	
3830	MLDD	ADVANCE lamp	OFF	
3840	MLDD	Press and release 0A9		
3850	MLDD	COMMAND 0A9	ON	

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Figure 7-15. Past History Mode Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3860	MLDD	ADVANCE lamp	ON	
3880	MLDD	Press and release PAST/PRESENT		
3890	MLDD	PAST lamp	ON	
3900	MLDD	Turn DISPLAY SELECT to AI3 DATA		
3910	MLDD	Turn WORD to T-7		
3920	MLDD	COMPUTER DATA lamps 6, 9, 10, 11, 20, 23, 24, and 25	ON	
3930	MLDD	COMPUTER Address lamps A1, A2, A3, A6, OP2, OP4	ON	
3940	MLDD	Turn DISPLAY SELECT to MD7		
3950	MLDD	COMPUTER DATA lamps 1, 4, 7, 10, 13, 18, 21, and 24	ON	
3960	MLDD	Turn DISPLAY SELECT to MR1		
3970	MLDD	COMPUTER DATA lamps 1, 6, 9, 12, 15, 18, 21, and 24	ON	
3980	MLDD	Turn DISPLAY SELECT to PRO		
3990	MLDD	COMPUTER DATA lamps 15, 16, 17	ON	
4000	MLDD	Press and release ERROR OVER RIDE		
4010	MLDD	ERROR OVER RIDE lamp	ON	
4020	MLDD	Press and release COMPTR DISPLAY RESET		
4030	IE	Press and release ERROR RESET		
4040	IE	COMPTR ALARM lamp	OFF	
4050	MLDD	Press and release COMPUTER CONTROL ON/OFF		
4060	MLDD	ON, ADVANCE and CST lamps	OFF	
4070	TRMC	Press and release MEMORY SIM		
4080	TRMC	MEMORY SIM lamp	OFF	
4090	TRMC	ML lamp	ON	
4100	MLDD	Verify that Address Counter will not step when ADVANCE/CST is depressed	Not Advance	
4110	MLDD	Press and release ERROR OVER RIDE		
4120	MLDD	ERROR OVER FIDE lamp	OFF	
4130	MLDD	Press and release COMMAND DISPLAY RESET		
4140	IE	Press and release DATA ADAPTER INTERFACE EXERCISER-RESET		
4150	IE	All I/O Reg. No. 2 lamps	OFF	

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Figure 7-15. Past History Mode Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
05	IE	Press and release MANUAL HALT		
06	IE	MANUAL HALT lamp	OFF	
10	MLDD	Press and release COMPTR DISPLAY RESET and COMMAND DISPLAY RESET		
20	TRMC	Press and release MEMORY SIM		
30	TRMC	MEMORY SIM lamp	ON	
40	TRMC	ML lamp	OFF	
50	IE	COMPUTER ALARM	ON	
60	IE	INTC lamp	ON	
70	MLDD	Turn DISPLAY SELECT switch to TRS		
80	MLDD	Press and release A1 through A5		
90	MLDD	COMMAND and COMPUTER A1 through A5 lamps	ON	
100	MLDD	COMPUTER OP1, OP2, OP3, OP4 lamps	ON	
110	MLDD	DATA COMPUTER lamps 7, 8, 9, 10, 11, 21, 22, 23, 24 and 25	ON	
120	MLDD	Turn DISPLAY SELECT switch to AI3 DATA		
130	MLDD	Press and release A1, A4, A5 and A6		
140	MLDD	COMMAND and COMPUTER lamps A2, A3 and A6	ON	
150	MLDD	COMPUTER lamp OP2	ON	
160	MLDD	COMPUTER DATA lamps 6, 9, 10, 20, 23 and 24	ON	
170	MLDD	Press and release A2, A3, A4, A5 and A6		
180	MLDD	COMMAND and COMPUTER lamps A4 and A5	ON	
190	MLDD	COMPUTER lamp OP1	ON	
200	MLDD	COMPUTER DATA lamps 7, 8, 21 and 22	ON	
210	MLDD	Turn WORD switch to T-7		
220	MLDD	Press and release A2 and A4		
230	MLDD	COMMAND and COMPUTER lamps A2 and A5	ON	
240	MLDD	COMPUTER lamp OP3	ON	
250	MLDD	COMPUTER DATA lamps 7, 10, 21 and 24	ON	
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Figure 7-16. Data Register Checks (Sheet 1 of 15)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
260	MLDD	Turn WORD switch to T		
270	MLDD	Turn Display Select switch to AI3 IA		
280	MLDD	Press and release A7, A6, A5, A4, A2 and A1		
290	MLDD	COMMAND and COMPUTER lamps A7, A6, A4 and A1	ON	
300	MLDD	COMPUTER lamps OP1, OP3 and OP4	ON	
310	MLDD	Computer Data lamps SIGN, 1 and 3. Lamps 9 through 25 may or may not be lit.	ON	
320	MLDD	Press and hold Repeat/Single		
330	MLDD	SINGLE lamp	ON	
340	MLDD	REPEAT lamp	OFF	
350	MLDD	Release Repeat/Single		
360	MLDD	Single and Repeat lamps	Unchanged	
370	MLDD	Turn Display Select switch to TRS		
380	MLDD	Press and release A2 through A8		
390	MLDD	Press and release 0A8 and 0A9		
400	MLDD	COMMAND lamps A8, A5, A3, A2, A1, 0A8 and 0A9	ON	
410	IE	Lamps A8 and A9	ON	
420	MLDD	Press and hold Computer Display Reset		
430	MLDD	Computer lamps A8, A5, A3, A2, A1, 0A8, 0A9, OP2, OP3 and OP4	ON	
440	MLDD	Computer Data lamps 4, 7, 8, 18, 21 and 22	ON	
450	MLDD	Release Computer Display Reset		
460	MLDD	Lamp status	Unchanged	
470	MLDD	Turn Display Select switch to AI3 DATA		
480	MLDD	Press and release A6		

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Figure 7-16. Data Register Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
490	MLDD	COMMAND lamp A6	ON	
500	MLDD	Press and release Computer Display Reset		
510	MLDD	Computer lamps A8, A6, A5, A3, A2 and A1	ON	
520	MLDD	Computer Data lamps 4, 6, 7, 8, 13, 20, 21 and 22	ON	
530	MLDD	Turn Display Select switch To AI 3 IA		
540	MLDD	Press and release A7 and A6		
550	MLDD	COMMAND lamps A1, A2, A3, A5, A7 and A8	ON	
560	MLDD	Press and release Computer Display Reset		
570	MLDD	Computer lamps A8, A7, A5, A3, A2, A1, OP2, OP3 and OP4	ON	
580	MLDD	Computer Data lamps SIGN, 2, 4, 5 and 6	ON	
585	MLDD	Lamps 9 through 25	ON	
590	MLDD	Press and release A1 through A8, 0A8 and 0A9		
600	MLDD	COMMAND lamps A4 and A6	ON	
610	MLDD	Turn Display Select switch to AI3 DATA		
620	MLDD	Press and hold Repeat/Single		
630	MLDD	REPEAT lamp	ON	
640	MLDD	SINGLE lamp	OFF	
650	MLDD	Computer lamps A4 and A6, OP1 and OP3	ON	
660	MLDD	Computer Data lamps 6, 8, 9, 20, 22 and 23	ON	
670	MLDD	Release Repeat/Single		
680	MLDD	Lamp status	Unchanged	
690	MLDD	Turn Display Select switch to HOPC1		
700	MLDD	Press and release Data 2, 4, 9, 16, and 18		
710	MLDD	Data Command and Computer lamps 2, 4, 9, 16 and 18	ON	
720	MLDD	Computer Data Adr. DS4, DS2 and DX lamps	ON	
730	MLDD	Computer Data Adr. SX lamp	OFF	
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Figure 7-16. Data Register Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
740	MLDD	Press and release REPEAT/SINGLE		
750	MLDD	SINGLE lamp	ON	
760	MLDD	REPEAT lamp	OFF	
770	MLDD	Press and release A8, A5, A4, A3, A2 and A1, 0A9, 0A8, 0A2 and 0A1		
780	MLDD	COMMAND lamps A8, A6, A5, A3, A2, A1, 0A9, 0A8, 0A2 and 0A1	ON	
790	IE	Lamps A1, A2, A8 and A9	ON	
800	MLDD	Press and release COMPUTER DISPLAY RESET		
810	MLDD	COMPUTER DATA lamps SIGN, 5, 12, 14, 24 and 25	ON	
820	MLDD	COMPUTER lamps 0A9, 0A8, 0A2, 0A1, A8, A6, A5, A3, A2, A1, OP2, OP3, and OP4	ON	
830	MLDD	Press and release COMMAND and COMPUTER DISPLAY RESETS		
840	MLDD	All Computer Data lamps	OFF	
850	MLDD	COMMAND and COMPUTER lamps A1 through A8, 0A1 through 0A9, DS1 through DS4 and DX	OFF	
860	MLDD	COMMAND and COMPUTER SX lamp	ON	
870	MLDD	Press and release REPEAT/SINGLE		
880	MLDD	REPEAT lamp	ON	
890	MLDD	SINGLE lamp	OFF	
900	MLDD	Turn DISPLAY SELECT switch to MD7		
910	MLDD	Press and release A2, A3, and A4		
920	MLDD	COMMAND and COMPUTER A2, A3 and A4 lamps	ON	
930	MLDD	COMPUTER lamps OP1 and OP2	ON	
940	MLDD	Press and release ON/OFF		
950	MLDD	ON, ADVANCE and CST lamps	ON	
955	IE	Press and release I/O Reg. No. 2		
956	IE	I/O Reg. No. 2 lamp	ON	
960	IE	Press and release I/O Reg. Bit 25		
970	IE	I/O Reg. No. 2 lamp 25	ON	
980	MLDD	Press and release ON/OFF		
990	MLDD	ON, ADVANCE and CST lamps	OFF	
1000	MLDD	OFF lamp	ON	
1010	MLDD	All Computer Data lamps	OFF	
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Figure 7-16. Data Register Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1020	MLDD	Turn WORD switch to T-1		
1030	MLDD	Computer Data lamp 1	ON	
1040	MLDD	TURN WORD switch to T-2		
1050	MLDD	Computer Data lamp 3	ON	

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Figure 7-16. Data Register Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1060	MLDD	Turn WORD switch to T-3		
1070	MLDD	Computer Data lamp 5	ON	
1080	MLDD	Turn WORD switch to T-4		
1090	MLDD	Computer Dat a lamp 7	ON	
1100	MLDD	Turn WORD switch to T-5		
1110	MLDD	Computer Data lamp 9	ON	
1120	MLDD	Turn WORD switch to T-6		
1130	MLDD	Computer Data lamp 11	ON	
1140	MLDD	Turn WORD switch to T-7		
1150	MLDD	Computer Data lamp 13	ON	
1160	MLDD	Turn WORD switch to T-8		
1170	MLDD	Computer Data lamp 15	ON	
1180	MLDD	Turn WORD switch to T-9		
1190	MLDD	Computer DATA lamp 17	ON	
1200	MLDD	Turn WORD switch to T-10		
1210	MLDD	Computer Data lamp 19	ON	
1220	MLDD	Turn WORD switch to T-11		
1230	MLDD	Computer Data lamp 21	ON	
1240	MLDD	Turn WORD switch to T-12		
1250	MLDD	Computer Data lamp 23	ON	
1260	MLDD	Turn Display Select switch to MR1		
1270	MLDD	Turn WORD switch to T-1		
1280	MLDD	Computer Data lamp 3	ON	
1290	MLDD	Turn WORD switch to T-2		
1300	MLDD	Computer Data lamp 7	ON	
1310	MLDD	Turn WORD switch to T-3		
1320	MLDD	Computer Data lamp 11	ON	
1330	MLDD	Turn WORD switch to T-4		
1340	MLDD	Computer Data lamp 15	ON	
1350	MLDD	Turn WORD switch to T-5		
1360	MLDD	Computer Data lamp 19	ON	
1370	MLDD	Turn WORD switch to T-6		
1380	MLDD	Computer Data lamp 23	ON	
1390	MLDD	Turn WORD switch to T-7		
1400	MLDD	Computer Data lamp 1	ON	
1410	MLDD	Turn WORD switch to T-8		
1420	MLDD	Computer Data lamp 5	ON	
1430	MLDD	Turn WORD switch to T-9		
1440	MLDD	Computer Data lamp 9	ON	
1450	MLDD	Turn WORD switch to T-10		
1460	MLDD	Computer Data lamp 13	ON	

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Figure 7-16. Data Register Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1470	MLDD	Turn WORD switch to T-11		
1480	MLDD	Computer Data lamp 17	ON	
1490	MLDD	Turn WORD switch to T		
1500	MLDD	Computer Data lamp 21	ON	
1510	MLDD	Turn Display Select switch to PRO		
1520	MLDD	Press and release Data Bit 17		
1530	MLDD	Data Command lamp 17 and Data Computer lamp 23	ON	
1540	MLDD	Press and release A2, A3, and A5		
1550	MLDD	COMMAND and COMPUTER lamps A4 and A5	ON	
1560	MLDD	COMPUTER lamps OP1, DM2 and Data Adr. DX	ON	
1570	MLDD	Turn Display Select switch to TRS		
1580	MLDD	Computer Data lamps 7, 8, 21 and 22	ON	
1590	MLDD	Command Data lamp 17	ON	
1600	MLDD	Turn Display Select switch to PRO		
1610	MLDD	Turn WORD switch to T-2		
1620	MLDD	Computer Data lamp 9	ON	
1630	MLDD	Turn Display Select switch to MD7		
1640	MLDD	Turn WORD switch to T		
1650	MLDD	ALL Computer Data lamps	OFF	
1660	MLDD	Turn WORD switch to T-1		
1670	MLDD	Computer Data lamp 4	ON	
1680	MLDD	Turn WORD switch to T-2		
1690	MLDD	Computer Data lamp 6	ON	
1700	MLDD	Turn WORD switch to T-3		
1710	MLDD	Computer Data lamp 8	ON	
1720	MLDD	Turn WORD switch to T-4		
1730	MLDD	Computer Data lamp 10	ON	
1740	MLDD	Turn WORD switch to T-5		
1750	MLDD	Computer Data lamp 12	ON	
1760	MLDD	Turn WORD switch to T-6		
1770	MLDD	Computer Data lamp 14	ON	
1780	MLDD	Turn WORD switch to T-7		
1790	MLDD	Computer Data lamp 16	ON	
1800	MLDD	Turn WORD switch to T-8		
1810	MLDD	Computer Data lamp 18	ON	
1820	MLDD	Turn WORD switch to T		
1830	MLDD	ALL Computer Data lamps	OFF	

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Figure 7-16. Data Register Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1840	MLDD	Turn Display Select switch to MR1		
1850	MLDD	Computer Data lamp 25	ON	
1860	MLDD	Turn WORD switch to T-1		
1870	MLDD	Computer Data lamp 25	ON	
1880	MLDD	Turn WORD switch to T-2		
1890	MLDD	Computer Data lamp 23	ON	
1900	MLDD	Turn WORD switch to T-3		
1910	MLDD	Computer Data lamp 21	ON	
1920	MLDD	Turn WORD switch to T-4		
1930	MLDD	Computer Data lamp 19	ON	
1940	MLDD	Turn WORD switch to T-5		
1950	MLDD	Computer Data lamp 17	ON	
1960	MLDD	Turn WORD switch to T-6		
1970	MLDD	Computer Data lamp 15	ON	
1980	MLDD	Turn WORD switch to T-7		
1990	MLDD	Computer Data lamp 13	ON	
2000	MLDD	Turn WORD switch to T-8		
2010	MLDD	Computer Data lamp 11	ON	
2020	MLDD	Turn WORD switch to T-13		
2030	MLDD	Computer Data lamp 13	ON	
2040	MLDD	Turn Display Select switch to PRO		
2050	MLDD	Turn WORD switch to T-3		
2060	MLDD	ALL Computer Data lamps	OFF	
2070	MLDD	Turn WORD switch to T-4		
2080	MLDD	Computer Data lamp 23	ON	
2090	MLDD	Press and release A5, A3, A2		
2100	MLDD	COMMAND and COMPUTER A2, A3, and A4 lamps	ON	
2110	MLDD	COMPUTER OP1 and OP2	ON	
2120	MLDD	Computer Data lamp 20	ON	
2130	MLDD	Turn WORD switch to T-3		
2140	MLDD	ALL Computer Data lamps	OFF	
2150	MLDD	Turn WORD switch to T-2		
2160	MLDD	Computer Data lamp 6	ON	
2170	MLDD	Turn WORD switch to T-1		
2180	MLDD	Computer Data lamp 20	ON	
2190	MLDD	Press and release Data Bit 17		
2200	MLDD	COMMAND Data lamp 17	OFF	
2210	MLDD	Computer Data lamp 20	OFF	
2220	MLDD	Turn Display Select switch to SSC		
2230	MLDD	Computer Data lamp 25	ON	

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Figure 7-16. Data Register Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2240	MLDD	Turn Display Select switch to MLC		
2250	MLDD	Computer Data lamp 12	ON	
2260	MLDD	Turn Display Select to NONE		
2270	MLDD	Turn WORD switch to T		
2280	MLDD	Press and release COMMAND and COMPUTER Display Reset		
2320	MLDD	COMMAND and COMPUTER A8 through A1, OP4 through OP1, 0A9 through 0A1 and All DATA lamps	OFF	
2321	TRMC	Press and release ADR5		
2322	TRMC	ADR5 lamp	ON	
2323	MLDD	Press and release DS4		
2324	MLDD	DS4 Command lamp	ON	
2325	MLDD	Press and release Address Computer		
2326	IE	INTC lamp	OFF	
2327	MLDD	Press and release DS4		
2328	MLDD	DS4 lamp	OFF	
2329	TRMC	Press and release ADR5		
2330	TRMC	ADR5 lamp	OFF	
EXP		Check Real Time Counter		
2340	MLDD	Turn DISPLAY SELECT to RTC		
2341	MLDD	Press and release A4		
2350	MLDD	COMMAND and COMPUTER A4 and COMPUTER OP1 and OP3	ON	
2360	MLDD	Press and release ON/OFF		
2370	MLDD	ON, ADVANCE and CST lamps	ON	
2380	IE	Press and release OP/TP		
2390	IE	OP lamp	ON	
2400	IE	TP lamp	OFF	
2410	MLDD	Press and release COMPTR DISPLAY RESET		
2411	MLDD	COMPUTER A4, OP1 and OP3	OFF	
2420	IE	Press and release ERROR RESET		
2430	IE	All ERROR lamps	OFF	
2450	IE	Press and release MANUAL SSC INH and MLC INH (if OFF)		
2460	IE	MANUAL MLC INH and MANUAL SSC INH lamps	ON	
2470	MLDD	Record DATA Register	Record	
2480	MLDD	Press and release ADVANCE/CST		
2490	MLDD	COMPUTER OP1, OP3, OP4, A1, A4, and COMMAND A4 lamps	ON	

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Figure 7-16. Data Register Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2500	MLDD	Record DATA Register	Record	
2510	MLDD	If DATA as recorded in step 2500 does not differ from DATA in step 2470, omit steps 2520 through 2550		
2520	MLDD	Press and release (3 times) ADVANCE/CST		
2530	MLDD	COMPUTER OP1, OP3, and OP4 lamps	OFF	
2540	MLDD	COMPUTER A3, A4 and COMMAND A4 lamps	ON	
2550	MLDD	If DATA Register increased by 1 Bit omit steps 2560 through 2690		
2560	MLDD	Press and release ADVANCE/CST		
2570	MLDD	COMPUTER OP3, A2, A4 and COMMAND A4 lamps	ON	
2580	MLDD	Record DATA Register	Record	
2590	MLDD	If DATA as recorded in step 2580 does not differ from DATA in step 2500, omit steps 2600 through 2630		
2600	MLDD	Press and release (2 times) ADVANCE/CST		
2610	MLDD	COMPUTER OP1, OP3 and OP4 lamps	OFF	
2620	MLDD	COMPUTER A3, A4 and COMMAND A4 lamps	ON	
2630	MLDD	If DATA Register increased by 1 Bit, omit steps 2640 through 2690		
2640	MLDD	Press and release ADVANCE/CST		
2650	MLDD	COMPUTER OP3, OP4, A1, A2, A4, and COMMAND A4 lamps	ON	
2660	MLDD	Verify DATA Register increased by 1 Bit	Verify	
2670	MLDD	Press and release (2 times) ADVANCE/CST		
2680	MLDD	COMPUTER OP1, OP2, A2, A3, A4, and COMMAND A4 lamp	ON	
2690	MLDD	Verify DATA Register increased by 1 Bit	Verify	

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Figure 7-16. Data Register Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2700	TRMC	Press and release MEMORY SIM		
2710	TRMC	MEMORY SIM lamp	OFF	
2720	TRMC	ML lamp	ON	
2730	MLDD	OFF lamp	ON	
2740	MLDD	ON, ADVANCE and CST lamps	OFF	
2750	MLDD	Turn DISPLAY SELECT to NONE		
2760	IE	Press and release OP/TP		
2770	IE	OP lamp	OFF	
2780	IE	TP lamp	ON	
2790	IE	Press and release MANUAL SSC INH and MANUAL MLC INH		
2800	IE	MANUAL MLC INH and MANUAL SSC INH lamps	OFF	
EXP		DISCRETES		
2810	IE	TP lamp (Press and release TP/OP if OFF)	ON	
2820	MLDD	DISPLAY SERIAL OUT lamp (Press and release if ON)	OFF	
2830	TRMC	Press and release MEMORY SIM		
2840	TRMC	MEMORY SIM lamp	ON	
2850	TRMC	Tape Address Counter	Counting	
2860	MLDD	Press and release A5 and A6		
2870	MLDD	COMMAND and COMPUTER A5 and A6 lamps	ON	
2875	MLDD	Press and release MANUAL RE-START		
2876	IE	INTC lamp	OFF	
2880	MLDD	Press and release SINGLE STEP ON/OFF		
2890	MLDD	ON, ADVANCE and CST lamps	ON	
2900	IE	I/O Reg. No. 2 lamps (press and release if OFF)	ON	
2905	IE	Press and release I/O Reg. RESET		
2906	IE	I/O Reg. No. 2 lamps	OFF	
2910	IE	Press and release Bit 19		
2920	IE	I/O Reg. No. 2 Bit 19 lamp	ON	
2921	MLDD	Press and release DATA 12, 13 and 14		
2922	MLDD	DATA COMMAND lamps 12, 13 and 14	ON	
2923	MLDD	Press and release ERROR OVER RIDE		
2924	MLDD	ERROR OVER RIDE lamp	ON	

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Figure 7-16. Data Register Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2925	MLDD	Press and release COMPTR DISPLAY RESET		
2926	IE	Press and release ERROR RESET		
2927	IE	All ERROR lamps	OFF	
2930	MLDD	Press and release ADVANCE/CST (11 times)		
2940	MLDD	Press and release A5 and A6		
2950	MLDD	COMMAND A5 and A6 lamps	OFF	
2960	MLDD	COMPUTER A2, A3, A4, A5, and A6 lamps	ON	
2970	TRMC	Press and release TAPE ADDRESS ADR 5		
2980	TRMC	TAPE ADDRESS ADR 5 lamp	ON	
3000	MLDD	Press and release DATA 1, 12 and 14		
3010	MLDD	COMMAND DATA 1 and 13 lamps	ON	
3020	MLDD	COMMAND DATA 12 and 14 lamps	OFF	
3030	MLDD	Press and release A2		
3040	MLDD	COMMAND A2 lamp	ON	
3050	MLDD	DISPLAY MODE PAST lamp	ON	
3060	MLDD	DISPLAY MODE PRESENT lamp	OFF	
3070	MLDD	Disregard ALL COMPUTER DISPLAY lamps		
3080	MLDD	Turn WORD switch to T-1		
3090	IE	I/O Reg. No. 1 lamps 3, 4, 5, 6, 17, 18, 19, and 20	ON	
3100	MLDD	Turn WORD switch to T-2		
3110	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	
3120	MLDD	Press and release A2		
3130	MLDD	COMMAND A2 lamp	OFF	
3140	IE	Press and release I/O Reg. No. 1/2		
3150	IE	I/O Reg. No. 1 lamp	ON	
3160	IE	I/O Reg. No. 2 lamp	OFF	
3170	IE	Press and release I/O Reg. RESET		
3180	IE	ALL I/O Reg. No. 1 lamps	OFF	
3190	MLDD	Press and release A2		
3200	MLDD	COMMAND A2 lamp	ON	
3210	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	

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Figure 7-16. Data Register Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3220	TRMC	Press and release TAPE ADDRESS ADR1		
3230	TRMC	ADR 1 lamp	ON	
3240	IE	Press and release I/O Reg. Reset		
3250	IE	ALL I/O Reg. No. 1 lamps	OFF	
3260	TRMC	Press and release TAPE ADDRESS ADR1		
3270	TRMC	ADR1 lamp	OFF	
3280	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21, and 22	ON	
3290	TRMC	Press and release TAPE ADDRESS ADR2		
3300	TRMC	ADR2 lamp	ON	
3310	IE	Press and release I/O Reg. Reset		
3320	IE	ALL I/O Reg. No. 1 lamps	OFF	
3330	TRMC	Press and release TAPE ADDRESS ADR2		
3340	TRMC	ADR2 lamp	OFF	
3350	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	
3360	TRMC	Press and release TAPE ADDRESS ADR3		
3370	TRMC	ADR3 lamp	ON	
3380	IE	Press and release I/O Reg. reset		
3390	IE	ALL I/O Reg. No. 1 lamps	OFF	
3400	TRMC	Press and release TAPE ADDRESS ADR3		
3410	TRMC	ADR3 lamp	OFF	
3420	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	
3430	TRMC	Press and release TAPE ADDRESS ADR 4		
3440	TRMC	ADR 4 lamp	ON	
3450	IE	Press and release I/O Reg. Reset		
3460	IE	ALL I/O Reg. No. 1 lamps	OFF	
3470	TRMC	Press and release TAPE ADDRESS ADR 4		
	TRMC	ADR4 lamp	OFF	
	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	

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Figure 7-16. Data Register Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3480	TRMC	Press and release TAPE ADDRESS ADR 5		
3490	TRMC	ADR5 lamp	OFF	
3500	IE	Press and release I/O Reg. Reset		
3510	IE	ALL I/O Reg. No. 1 lamps	OFF	
3520	TRMC	Press and release TAPE ADDRESS ADR5		
3530	TRMC	ADR5 lamp	ON	
3540	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	
3550	IE	Press and release OP/TP		
3560	IE	OP lamp	ON	
3570	IE	TP lamp	OFF	
3580	IE	Press and release I/O Reg. Reset		
3590	IE	ALL I/O Reg. No. 1 lamps	OFF	
3600	IE	Press and release OP/TP		
3610	IE	OP lamp	OFF	
3620	IE	TP lamp	ON	
3630	IE	I/O Reg. No. 1 lamps 3, 4, 5, 7, 8, 17, 18, 19, 21 and 22	ON	
3640	MLDD	Press and release A2 and A1		
3650	MLDD	COMMAND A2 lamp	OFF	
3660	MLDD	COMMAND A1 lamp	ON	
3670	MLDD	Turn WORD switch (ccw) to T		
3680	IE	I/O Reg. No. 1 lamps 3, 4, 5, 6, 7, 17 18, 19, 20 and 21	ON	
3690	MLDD	Turn WORD switch to T-1		
3700	IE	I/O Reg. No. 1 lamps 3, 4, 5, 6, 8, 17, 18, 19, 20 and 22	ON	
3710	TRMC	Press and release TAPE ADDRESS ADR1		
3720	TRMC	ADR 1 lamp	ON	
3730	IE	Press and release I/O Reg. Reset		
3740	IE	ALL I/O Reg. No. 1 lamps	OFF	
3750	MLDD	Press and release A1 and A3		
3760	MLDD	COMMAND A1	OFF	
3770	MLDD	COMMAND A3	ON	
3780	IE	ALL I/O Reg. No. 1 lamps	OFF	
3790	MLDD	Press and release A3 and A4		
3800	MLDD	COMMAND A3	OFF	
3810	MLDD	COMMAND A4	ON	

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Figure 7-16. Data Register Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3820	IE	ALL I/O Reg. No. 1 lamps	OFF	
3830	MLDD	Press and release A4 and A5		
3840	MLDD	COMMAND A4	OFF	
3850	MLDD	COMMAND A5	ON	
3860	IE	ALL I/O Reg. No. 1 lamps	OFF	
3870	MLDD	Press and release A5 and A6		
3880	MLDD	COMMAND A5 lamp	OFF	
3890	MLDD	COMMAND A6 lamp	ON	
3900	IE	ALL I/O Reg. No. 1 lamps	OFF	
3910	TRMC	Press and release TAPE ADDRESS ADR1		
3920	TRMC	ADR1 lamp	OFF	
3930	IE	I/O Reg. No. 1 18 lamp	ON	
3940	MLDD	Press and release A6 and A5		
3950	MLDD	COMMAND A6 lamp	OFF	
3960	MLDD	COMMAND A5 lamp	ON	
3970	IE	I/O Reg. No. 1 18 lamp	ON	
3980	MLDD	Press and release A5 and A4		
3990	MLDD	COMMAND A5 lamp	OFF	
4000	MLDD	COMMAND A4 lamp	ON	
4010	IE	I/O Reg. No. 1 11, 12, and 13 lamps	ON	
4020	IE	Press and release I/O Reset		
4030	MLDD	Press and release COMMAND DISPLAY RESET		
4040	MLDD	PAST lamp (press and release if ON)	OFF	
4050	MLDD	Turn WORD to T		
4060	TRMC	MEMORY SIM (press and release if ON)	OFF	

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Figure 7-16. Data Register Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	IE	TP Lamp (Press and release if OFF)	ON	
20	IE	MANUAL HALT lamp (Press and release if ON)	OFF	
30	IE	COMPTR HALT lamp	ON	
40	MLDD	COMPUTER CONTROL, AUTO lamp	OFF	
50	MLDD	COMPUTER CONTROL, MAN/PTC lamp	ON	
60	TRMC	Press and release MEMORY SIM		
70	TRMC	MEMORY SIM lamp	ON	
75	TRMC	Tape Address Counter	Counting	
80	TRMC	ML lamp	OFF	
90	IE	COMPTR HALT lamp	OFF	
100	IE	Press and release MANUAL HALT/ COMPTR HALT		
110	IE	COMPTR HALT and MANUAL HALT lamps	ON	
120	IE	CHANNEL lamp (Press and release CHANNEL/MODULE if OFF)	ON	
130	IE	Press and release ALL		
140	IE	ALL lamp	ON	
145	IE	Press and release COMPTR HALT/ MANUAL HALT		
150	IE	MANUAL HALT and COMPTR HALT lamps	OFF	
160	IE	Turn CLOCK switch (ccw) to 15		
170	IE	ILLEGAL PATH lamp	ON	
180	IE	COMPTR HALT lamp	ON	
190	IE	Turn CLOCK switch (cw) to NONE		
200	IE	ILLEGAL PATH lamp	OFF	
210	IE	COMPTR HALT lamp	OFF	
211	TRMC	MANUAL lamp (Press and release if OFF)	ON	
212	TRMC	AUTO lamp	OFF	
213	IE	Press and release ERROR RESET		
214	TRMC	Press and release PWR ON/PWR OFF		
215	TRMC	PWR OFF lamp	OFF	
216	TRMC	PWR ON lamp	ON	
217	IE	Press and release COMPTR HALT/ MANUAL HALT		
218	IE	COMPTR HALT and MANUAL HALT lamps	ON	

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Figure 7-17. Halt Checks (Sheet 1 of 11)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
219	TRMC	Press and release MANUAL ADVANCE TAPE		
220	IE	MANUAL HALT and COMPTR HALT lamps	OFF	
221	IE	Press and release MANUAL HALT		
222	IE	MANUAL HALT lamp remains	OFF	
225	PC	Press and release COMP, POWER SEQ OFF		
230	PC	COMP POWER SEQ ON lamp	OFF	
240	TRMC	ML lamp	ON	
250	IE	COMPTR HALT lamp	ON	
260	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
270	PC	Press and release ACME POWER SEQ OFF		
280	PC	ACME POWER SEQ ON lamp	OFF	
290	PC	ACME POWER SEQ OFF lamp (delayed)	ON	
300	PC	Press and release MAIN POWER OFF		
310	PC	POWER ON lamp	OFF	
320	PC	POWER OFF lamp	ON	
330	9020	Remove jumper plug from J29		
340	PC	POWER OFF lamp	OFF	
350	9020	Connect cable 9020J29 to J29		
360	PC	POWER OFF lamp	ON	
370	PC	Press and release MAIN POWER PANEL ON		
380	PC	POWER OFF lamp	OFF	
390	PC	POWER ON lamp	ON	
395	PC	ACME and COMP SEQ OFF lamps	ON	
400	PC	Press and release ACME SEQ ON		
410	PC	ACME POWER SEQ OFF lamp	OFF	
420	PC	ACME POWER SEQ ON lamp	ON	
430	PC	Press and release COMP POWER SEQ ON		
440	PC	COMP POWER SEQ OFF lamp	OFF	
450	PC	COMP POWER SEQ ON lamp	ON (delayed)	

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Figure 7-17. Halt Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
Note		If neither INV ERR or ADR6 lamps are lit on the TRMC panel, omit steps 460 through 540		
460	TRMC	Press and release ADR 1		
465	TRMC	ADR 1 lamp	ON	
470	TRMC	Press and release ADR 2		
475	TRMC	ADR 2 and ADR 6 lamps	ON	
480	TRMC	Press and release ADR 3		
485	TRMC	ADR 3 lamp	ON	
490	TRMC	INV ERR lamp	OFF	
500	TRMC	Press and release ADR 1		
510	TRMC	ADR 1 lamp	OFF	
515	TRMC	Press and release ADR 2		
520	TRMC	ADR 2 and ADR 6 lamps	OFF	
530	TRMC	Press and release ADR 3		
540	TRMC	ADR 3 lamp	OFF	
550	IE	Press and release ERROR RESET		
560	IE	All ERROR lamps (except COMPTR ALARM which may be either OFF or ON)	OFF	
570	TRMC	DD lamp	ON	
580	IE	Press and release MANUAL HALT/ COMPTR HALT		
590	IE	MANUAL HALT lamp	ON	
600	IE	COMPTR HALT lamp	OFF	
610	IE	Press and release MANUAL HALT/ COMPTR HALT		
620	IE	MANUAL HALT lamp	OFF	
630	TRMC	Press and release ADR 5		
640	TRMC	ADR 5 lamp	ON	
645	IE	COMPTR HALT lamp	OFF	
650	MLDD	Press and release IS 2		
660	MLDD	COMMAND IS 2 lamp	ON	
670	IE	COMPTR HALT lamp	ON	
740	TRMC	Press and release ADR 1		
750	TRMC	ADR 1 lamp	ON	
760	IE	COMPTR HALT lamp	OFF	
770	TRMC	Press and release ADR 1		
780	TRMC	ADR 1 lamp	OFF	
790	IE	COMPTR HALT Lamp	ON	

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Figure 7-17. Halt Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
800	TRMC	Press and release ADR 2		
810	TRMC	ADR 2 lamp	ON	
820	IE	COMPTR HALT lamp	OFF	
830	TRMC	Press and release ADR 2		
840	TRMC	ADR 2 lamp	OFF	
850	IE	COMPTR HALT lamp	ON	
860	TRMC	Press and release ADR 3		
870	TRMC	ADR 3 lamp	ON	
880	IE	COMPTR HALT lamp	OFF	
890	TRMC	Press and release ADR 3		
900	TRMC	ADR 3 lamp	OFF	
910	IE	COMPTR HALT lamp	ON	
920	TRMC	Press and release ADR 4		
930	TRMC	ADR 4 lamp	ON	
940	IE	COMPTR HALT lamp	OFF	
950	TRMC	Press and release ADR 4		
960	TRMC	ADR 4 lamp	OFF	
970	IE	COMPTR HALT lamp	ON	
1010	PC	Press and release COMP POWER SEQ OFF		
1015	IE	COMPTR HALT lamp	OFF	
1020	PC	COMP POWER SEQ ON lamp	OFF	
1030	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
1040	PC	Press and release ACME POWER SEQ OFF		
1050	PC	ACME POWER SEQ ON lamp	OFF	
1060	PC	ACME POWER SEQ OFF lamp (delayed)	ON	
1070	PC	Press and release MAIN POWER OFF		
1080	PC	POWER ON lamp	OFF	
1090	PC	POWER OFF lamp	ON	
1100	01A	Remove cable 9020J29 from J29		
1110	PC	POWER OFF lamp	OFF	
1120	01A	Connect jumper plug (P1) to J29		
1130	PC	POWER OFF lamp	ON	
1140	PC	Press and release MAIN POWER ON		
1150	PC	POWER OFF lamp	OFF	

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Figure 7-17. Halt Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1160	PC	POWER ON lamp	ON	
1170	PC	Phase A, B, C, and FAN lamps	ON	
1175	PC	ACME and COMP SEQ OFF lamps	ON	
1180	PC	Press and release ACME POWER SEQ ON		
1190	PC	ACME POWER SEQ OFF lamp	OFF	
1200	PC	ACME POWER SEQ ON lamp (delayed)	ON	
1210	PC	Press and release COMP POWER SEQ ON		
1220	PC	COMP POWER SEQ OFF lamp	OFF	
1230	PC	COMP POWER SEQ ON lamp (delayed)	ON	
1235	PC	NORMAL lamp	ON	
1240	IE	Press and release ERROR RESET		
Note		If neither INV ERR or ADR6 lamps are lit on the TRMC panel, omit steps 1250 through 1330.		
1250	TRMC	Press and release ADR 1		
1255	TRMC	ADR 1 lamp	ON	
1260	TRMC	Press and release ADR 2		
1265	TRMC	ADR 2 and ADR 6 lamps	ON	
1270	TRMC	Press and release ADR 3		
1275	TRMC	ADR 3 lamp	ON	
1280	TRMC	INV ERR lamp	OFF	
1285	TRMC	Press and release ADR 1		
1290	TRMC	ADR 1 lamp	OFF	
1300	TRMC	Press and release ADR 2		
1310	TRMC	ADR 2 and ADR 6 lamps	OFF	
1320	TRMC	Press and release ADR 3		
1330	TRMC	ADR 3 lamp	OFF	
1450	TRMC	MANUAL lamp (Press and release if OFF)	ON	
1460	TRMC	AUTO lamp	OFF	
1470	IE	Press and release ERROR RESET		
1475	IE	ERROR lamps (COMPTR ALARM may be ON or OFF at this time)	OFF	

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Figure 7-17. Halt Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1630	TRMC	Press and release ML/DD		
1640	TRMC	ML lamp	OFF	
1650	TRMC	DD lamp	ON	
1660	IE	COMPTR HALT lamp	OFF	
1670	TRMC	Press and release FREE RUN SS		
1680	TRMC	FREE RUN SS lamp	ON	
1690	IE	COMPTR HALT lamp	Flashes	
1695	TRMC	PWR ON lamp	OFF	
1696	TRMC	PWR OFF lamp	ON	
1700	TRMC	Press and release FREE RUN SS		
1710	TRMC	FREE RUN SS lamp	OFF	
1715	MLDD	Press and release COMMAND DISPLAY RESET		
1720	IE	COMPTR HALT lamp	OFF	
1730	TRMC	Press and release MEMORY SIM		
1740	TRMC	MEMORY SIM lamp	ON	
1750	TRMC	DD lamp	OFF	
1755	TRMC	Tape Address Counter	Counting	
1760	TRMC	Press and release ADR 5		
1770	TRMC	ADR 5 lamp	ON	
1780	MLDD	Press and release DATA Bit 25		
1790	MLDD	DATA COMMAND 25 lamp	ON	
1800	MLDD	Press and release ADDRESS COMPTR		
1810	IE	COMPTR HALT lamp	ON	
1820	MLDD	Press and release DATA Bit 25		

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Figure 7-17. Halt Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1830	MLDD	DATA COMMAND 25 lamp	OFF	
1840	MLDD	Press and release DS1		
1850	MLDD	COMMAND DS1 lamp	ON	
1860	MLDD	Press and release ADDRESS CMPTR		
1870	IE	COMPTR HALT lamp	OFF	
1880	MLDD	Press and release DS1		
1890	MLDD	COMMAND DS1 lamp	OFF	
1900	TRMC	Press and release ADR5		
1910	TRMC	ADR5 lamp	OFF	
1920	MLDD	Press and release COMPUTER CONTROL SS ON/OFF		
1930	MLDD	ON, ADVANCE and CST lamps	ON	
1940	MLDD	Press and hold AUTO/MAN/PTC		
1950	MLDD	MAN/PTC lamp	OFF	
1960	MLDD	AUTO lamp	ON	
1970	MLDD	Release AUTO/MAN/PTC		
1975	MLDD	ADVANCE/CST lamp	ON	
1980	MLDD	Press and release MANUAL RESTART		
1985	MLDD	ADVANCE/CST lamps	ON	
1990	MLDD	Press and hold AUTO/MAN/PTC		
2000	MLDD	AUTO lamp	OFF	
2010	MLDD	MAN/PTC lamp	ON	
2020	MLDD	ON, ADVANCE and CST lamps	OFF	
2030	MLDD	Release AUTO/MAN/PTC		
2040	MLDD	Press and release COMPUTER CONTROL SS ON/OFF		
2050	MLDD	ON, ADVANCE and CST lamps	ON	
2060	MLDD	Press and release MANUAL RESTART		
2070	MLDD	ON, ADVANCE and CST lamps	OFF	
2080	MLDD	Turn DISPLAY SELECT to SP2		
2090	IE	Turn PHASE switch to B		
2100	IE	Turn BIT GATE switch to 2		
2110	IE	Turn CLOCK switch to W		
2120	02B4	Open gate 02B4		
2130	02B4	Connect spare probe to A07A		
2135	02A3	Connect other end of spare probe to SP2		
2140	MLDD	All DATA lamps	OFF	

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Figure 7-17. Halt Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2144	TRMC	Press and release PWR ON/PWR OFF (If PWR ON is ON)		
2145	TRMC	PWR OFF lamp	ON	
2146	TRMC	PWR ON lamp	OFF	
2150	MLDD	Press and release DATA Bits 15, 16 and 17		
2160	MLDD	DATA COMMAND 15, 16, and 17 lamps	ON	
2190	MLDD	DATA COMPUTER lamps 15, 16 and 17	ON	
2195	MLDD	DATA COMPUTER lamp 14	OFF	
2200	IE	Turn CLOCK to X		
2210	MLDD	DATA COMPUTER lamps 15, 16 and 17 remain	ON	
2220	IE	Turn CLOCK to Y		
2230	MLDD	DATA COMPUTER lamps 15, 16 and 17 remain	ON	
2240	IE	Turn CLOCK to Z		
2250	MLDD	DATA COMPUTER lamp 15	OFF	
2260	MLDD	DATA COMPUTER lamps 16, 17 and 18	ON	
2270	IE	Turn CLOCK to Y		
2280	MLDD	DATA COMPUTER lamp 18	OFF	
2290	MLDD	DATA COMPUTER lamps 15, 16 and 17	ON	
2300	IE	Turn BIT GATE to 3		
2310	MLDD	DATA COMPUTER lamp 15	OFF	
2320	MLDD	DATA COMPUTER lamps 16, 17 and 18	ON	
2330	IE	Turn BIT GATE to 4		
2340	MLDD	DATA COMPUTER lamp 16	OFF	
2350	MLDD	DATA COMPUTER lamps 17, 18 and 19	ON	
2360	IE	Turn BIT GATE to 5		
2370	MLDD	DATA COMPUTER lamp 17	OFF	
2380	MLDD	DATA COMPUTER lamps 18, 19 and 20	ON	

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Figure 7-17. Halt Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2390	IE	Turn BIT GATE to 6		
2400	MLDD	DATA COMPUTER lamp 18	OFF	
2410	MLDD	DATA COMPUTER lamps 19, 20 and 21	ON	
2420	IE	Turn BIT GATE to 7		
2430	MLDD	DATA COMPUTER lamp 19	OFF	
2440	MLDD	DATA COMPUTER lamps 20, 21 and 22	ON	
2450	IE	Turn BIT GATE to 8		
2460	MLDD	DATA COMPUTER lamp 20	OFF	
2470	MLDD	DATA COMPUTER lamps 21, 22 and 23	ON	
2480	IE	Turn BIT GATE to 9		
2490	MLDD	DATA COMPUTER lamp 21	OFF	
2500	MLDD	DATA COMPUTER lamps 22, 23 and 24	ON	
2510	IE	Turn BIT GATE to 10		
2520	MLDD	DATA COMPUTER lamp 22	OFF	
2530	MLDD	DATA COMPUTER lamps 23, 24 and 25	ON	
2540	IE	Turn BIT GATE to 11		
2550	MLDD	DATA COMPUTER lamp 23	OFF	
2560	IE	Turn BIT GATE to 12		
2570	MLDD	DATA COMPUTER lamp 24	OFF	
2580	IE	Turn BIT GATE to 13		
2590	MLDD	All DATA COMPUTER lamps	OFF	
2600	IE	Turn BIT GATE to 14		
2610	MLDD	All DATA COMPUTER lamps remain	OFF	
2620	MLDD	Press and release DATA Bits 15, 16 and 17		
2630	MLDD	DATA COMMAND lamps 15, 16 and 17	OFF	
2640	02B4	Disconnect spare probe		
2650	02B4	Close gate 02B4		
2660	02A3	Disconnect spare probe from SP2 and connect to SP1		
2670	MLDD	Turn DISPLAY SELECT to SP1		

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Figure 7-17. Halt Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2670	TRMC	Connect spare probe to TP29		
2680	IE	Turn BIT GATE to 12		
2690	MLDD	Press and release A2, A3, A5 and A7		
2700	MLDD	COMMAND and COMPUTER lamps A2, A3, A5 and A7	ON	
2710	MLDD	Press and release COMPUTER CONTROL AUTO/MAN/PTC		
2720	MLDD	AUTO lamp	ON	
2730	MLDD	MAN/PTC lamp	OFF	
2740	MLDD	DATA COMPUTER lamps SIGN, 1, 2 and 3	ON	
2750	IE	Turn PHASE to C		
2760	IE	Turn BIT GATE to 11		
2770	MLDD	DATA COMPUTER lamps SIGN through 16	ON	
2780	MLDD	Press and release 0A8 and 0A9		
2790	MLDD	COMMAND and COMPUTER lamps 0A8 and 0A9	ON	
2800	MLDD	DATA COMPUTER lamps 9 through 16	ON	
2805	MLDD	DATA COMPUTER lamps 7 and 8	OFF	
2810	MLDD	Turn DISPLAY SELECT to HOPC1		
2820	MLDD	DATA COMPUTER lamps 9 through 16	OFF	
2830	MLDD	Turn DISPLAY SELECT to SP1		
2840	MLDD	DATA COMPUTER lamps 9 through 16	ON	
2850	IE	Turn BIT GATE to NONE		
2860	MLDD	DATA COMPUTER lamps 9 through 16	OFF	
2870	MLDD	DATA COMPUTER lamps SIGN through 6	ON	
2880	IE	Turn BIT GATE to 11		
2890	MLDD	DATA COMPUTER lamps SIGN through 6	OFF	
2900	MLDD	DATA COMPUTER lamps 9 through 16	ON	
2910	IE	Turn PHASE to NONE		
2920	MLDD	DATA COMPUTER lamps 9 through 16	OFF	
2930	MLDD	Press and release 0A8 and 0A9		

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Figure 7-17. Halt Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2940	MLDD	COMMAND and COMPUTER lamps 0A8 and 0A9	OFF	
2950	MLDD	Press and release A1, A5 and A7		
2960	MLDD	COMMAND and COMPUTER lamps A5 and A7	OFF	
2970	MLDD	COMMAND and COMPUTER lamps A1, A2 and A3	ON	
2980	IE	Turn PHASE to A		
2990	IE	Turn BIT GATE to 1		
3000	MLDD	DATA COMPUTER lamps 11 through 20	ON	
3005	MLDD	Press and release AUTO/MAN/PTC		
3006	MLDD	AUTO lamp	OFF	
3007	MLDD	MAN/PTC lamp	ON	
3008	MLDD	DATA COMPUTER lamps 11 through 20	OFF	
3010	IE	Turn CLOCK to NONE		
3020	MLDD	DATA COMPUTER lamps 11 through 20	OFF	
3030	IE	Turn PHASE and BIT GATE to NONE		
3040	MLDD	Press and release A1		
3050	MLDD	COMMAND and COMPUTER lamps A1	OFF	
3060	MLDD	Turn DISPLAY SELECT to NONE		
3070	TRMC	Disconnect spare probe from TP29		
3120	PC	Press and release COMPUTER SEQ OFF		
3130	PC	COMPUTER SEQ ON lamp	OFF	
3140	PC	COMPUTER SEQ OFF lamp (delayed)	ON	
3150	PC	Press and release ACME SEQ OFF		
3160	PC	ACME SEQ ON lamp	OFF	
3170	PC	ACME SEQ OFF lamp (delayed)	ON	
3200	PC	Press and release ACME SEQ ON		
3210	PC	ACME SEQ ON lamp	ON	
3220	PC	ACME SEQ OFF lamp	OFF	
3230	PC	Press and release COMPUTER SEQ ON		
3240	PC	COMPUTER SEQ ON lamp	ON	
3250	PC	COMPUTER SEQ OFF lamp	OFF	

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Figure 7-17. Halt Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
05		Perform operations in the Initialization portion of this procedure.		
10	IE	If MANUAL HALT lamp is on, press and release MANUAL HALT/COMPTR HALT		
		MANUAL HALT lamp	OFF	
15	IE	COMPTR HALT lamp	ON	
20	MLDD	Rotate DISPLAY SELECT switch to position 14		
30	TRMC	Press and release MEMORY SIM lamp	ON	
40	TRMC	ML lamp	OFF	
50	IE	INTC lamp, if OFF go to Step 130.		
55	IE	Press and release MANUAL HALT/ COMPTR HALT		
60	IE	MANUAL HALT lamp	ON	
70	IE	COMPTR HALT lamp	ON	
80	IE	INTC lamp	OFF	
90	IE	Press and release MANUAL HALT/ COMPTR HALT		
100	IE	MANUAL HALT lamp	OFF	
110	IE	COMPUTER HALT lamp	OFF	
120	IE	INTC lamp	OFF	
130	MLDD	DATA lamps (COMPTR and COMMAND)	OFF	
140	MLDD	DATA lamp (Press and release if ON)	OFF	
150	MLDD	INS lamp	ON	
160	MLDD	Press and release Instruction Address A1 and A4		
170	MLDD	COMMAND and COMPUTER A1 and A4 lamps	ON	
180	01B4	Open gate and remove SMS Card A22		
190	IE	MANUAL MLC INH lamp (Press and release MANUAL MLC INH if OFF)	ON	
200	IE	MANUAL SSC INH lamp (Press and release MANUAL SSC INH if OFF)	ON	

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Figure 7-18. Interrupt Checks (Sheet 1 of 20)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
210	IE	Press and release COMPTR HALT/ MANUAL HALT		
220	IE	COMPTR HALT/MANUAL HALT lamps	ON	
230	IE	Press and release OP/TP		
240	IE	OP lamp	ON	
250	IE	TP lamp	OFF	
260	TRMC	Press and release Tape Address ADR 5		
270	TRMC	ADR5 lamp	ON	
280	MLDD	Press and release Data 23		
290	MLDD	DATA COMMAND 23 lamp	ON	
300	MLDD	Press and release REPEAT/$\overline{\text{REPEAT}}$		
310	MLDD	REPEAT lamp	ON	
320	MLDD	$\overline{\text{REPEAT}}$ lamp	OFF	
330	MLDD	CST lamp	ON	
340	MLDD	DATA COMPUTER lamps 11 and 25	Flashing	
350	TRMC	Press and release Tape Address ADR 5		
360	TRMC	ADR 5 lamp	OFF	
370	MLDD	Press and release Data 23		
380	MLDD	DATA COMMAND 23 lamp	OFF	
390	MLDD	DATA COMPUTER lamps 11 and 25	OFF	
400	IE	Press and release OP/TP		
410	IE	OP lamp	OFF	
420	IE	TP lamp	ON	
430	01B4	Replace SMS Card in Pos. A22 and close gate 01B4		
440	IE	Press and release COMPTR HALT/ MANUAL HALT		
450	IE	COMPTR HALT/MANUAL HALT lamps	OFF	
460	IE	Press and release REPEAT/$\overline{\text{REPEAT}}$		
470	IE	REPEAT lamp	OFF	
480	IE	$\overline{\text{REPEAT}}$ lamp	ON	

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Figure 7-18. Interrupt Checks (Sheet 2)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
490	MLDD	Press and release A3, A5, IS1, IS2, IS3,		
500	MLDD	COMMAND and COMPUTER A1, A3, A4, A5, IS1, IS2 and IS3 lamps	ON	
510	MLDD	DATA ADDRESS COMPUTER ~~DX~~, DM1, DM2, OP2 and OP4 lamps	ON	
520	MLDD	Press and release 0A4		
530	MLDD	COMMAND and COMPUTER 0A4 lamp	ON	
540	MLDD	DATA COMPTR lamp 12	ON	
550	MLDD	Press and release 0A1 DATA ADDRESS (COMMAND and COMPTR)	ON	
560	MLDD	DATA COMPTR lamp 12	OFF	
570	MLDD	Press and release 0A1 DATA ADDRESS (COMMAND and COMPTR)	OFF	
580	MLDD	DATA COMPTR lamp 12	ON	
590	MLDD	Press and release DATA ADDRESS 0A9 (COMMAND and COMPTR lamp)	ON	
600	MLDD	DATA COMPTR lamp 12	OFF	
610	MLDD	Press and release DATA ADDRESS 0A9 (COMMAND and COMPTR lamp)	OFF	
620	MLDD	DATA COMPTR lamp 12	ON	
630	MLDD	Press and release IS1, IS2, IS3 and A1		
640	MLDD	COMMAND and COMPUTER IS1, IS2, IS3 and A1 lamps	OFF	
650	MLDD	COMMAND and COMPUTER A3, A4, A5 and 0A4 lamps	ON	
660	MLDD	DATA COMPTR lamp 12	OFF	
670	MLDD	Press and release IS1, IS2, IS3 and A1		

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Figure 7-18. Interrupt Checks (Sheet 3)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
680	MLDD	COMMAND and COMPUTER IS1, IS2, IS3, A1, A3, A4, A5 and 0A4 lamps	ON	
690	MLDD	COMPUTER DX, DM1, DM2, OP2 and OP4 lamps	ON	
700	MLDD	DATA COMPTR lamp 12	ON	
710	IE	Press and release OP/TP		
720	IE	OP lamp	ON	
730	IE	TP lamp	OFF	
740	MLDD	DATA COMPTR lamp 12	OFF	
750	IE	RESET PIOR lamp	ON	
760	MLDD	CST lamp	ON	
770	IE	Press and release OP/TP		
780	IE	OP lamp	OFF	
790	IE	TP lamp	ON	
800	IE	Press and release RESET PIOR		
810	IE	RESET PIOR lamp	OFF	
820	MLDD	CST lamp	OFF	
830	MLDD	DATA COMPTR lamp 12	ON	
840	MLDD	Press and release 0A4		
850	MLDD	COMMAND and COMPTR 0A4 lamp	OFF	
860	MLDD	DATA COMPTR lamp 12	OFF	
870	MLDD	Press and release 0A3		
880	MLDD	COMMAND and COMPTR 0A3 lamp	ON	
890	MLDD	DATA COMPTR 11 and 25 lamps	ON	
900	MLDD	Press and release 0A1		
910	MLDD	COMMAND and COMPTR 0A1 lamp	ON	
920	MLDD	DATA COMPTR 11 and 25 lamps	OFF	
930	MLDD	Press and release 0A1		
940	MLDD	COMMAND and COMPTR 0A1 lamp	OFF	
950	MLDD	DATA COMPTR 11 and 25 lamps	ON	
960	MLDD	Press and release 0A3		
970	MLDD	COMMAND and COMPTR 0A3 lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 4)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
980	MLDD	DATA COMPTR 11 and 25 lamps	OFF	
990	MLDD	Press and release 0A1		
1000	MLDD	COMMAND and COMPUTER 0A1 lamp	ON	
1010	MLDD	Press and release 0A6		
1020	MLDD	COMMAND 0A6 lamp	ON	
1030	MLDD	ON, ADVANCE and CST lamps	OFF	
1040	MLDD	Press and release 0A6		
1050	MLDD	COMMAND 0A6 lamp	OFF	
1060	MLDD	Press and release 0A1		
1070	MLDD	COMMAND and COMPUTER 0A1 lamp	OFF	
1080	MLDD	Press and release A2, A3, A8, IS1, IS2, and IS3		
1090	MLDD	COMMAND and COMPUTER IS1, IS2, IS3, and A3 lamps	OFF	
1100	MLDD	DATA ADDRESS COMPUTER DX, DM1, DM2, and OP2 lamps	OFF	
1110	MLDD	COMPUTER OP3, and OP4 lamps	ON	
1120	MLDD	COMMAND and COMPUTER A1, A2, A4, A5 and A8 lamps	ON	
1130	MLDD	Press and release SINGLE STEP ON/OFF		
1140	MLDD	ON, ADVANCE and CST lamps	ON	
1150	MLDD	OFF lamp	OFF	
1160	MLDD	Press and release A1 and A3		
1170	MLDD	COMPTR A1, A2, A4, A5, and A8 lamps	ON	
1180	MLDD	COMMAND A1 lamp	OFF	
1190	MLDD	COMMAND A2, A3, A4, A5 and A8 lamps	ON	
1200	02A3 MLDD	If the Spare Probe is connected to SP1, rotate display select to position SP1; if Spare Probe is connected to SP2, rotate display select to SP2 position.		
1210	E	Rotate phase select switch to position B.		

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Figure 7-18. Interrupt Checks (Sheet 5)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1220	IE	Turn BIT GATE to 5		
1230	TRMC	Connect Spare Probe to TP30		
1240	IE	Turn CLOCK to Y		
1250	MLDD	Press and release 0A8		
1260	MLDD	COMMAND 0A8 lamp	ON	
1270	MLDD	Press and release REPEAT/SINGLE		
1280	MLDD	Press and release ADVANCE/CST		
1290	MLDD	ADVANCE and CST lamps	OFF	
1300	MLDD	ON lamp	ON	
1310	IE	INTC lamp	ON	
1320	MLDD	DATA COMPUTER SIGN through 12 lamps	ON	
1330	MLDD	COMMAND and COMPTR A2, A3, A4, A5 and A8 lamps	ON	
1340	MLDD	REPEAT lamp	OFF	
1350	MLDD	SINGLE lamp	ON	
1360	MLDD	Press and release REPEAT/SINGLE		
1370	MLDD	REPEAT lamp	ON	
1380	MLDD	SINGLE lamp	OFF	
1390	MLDD	DATA COMPUTER SIGN through 25 lamps	ON	
1400	MLDD	Press and release A4, A5 and A6		
1410	MLDD	COMMAND A2, A3, A6 and A8 lamps	ON	
1420	MLDD	COMPTR A2, A3, A6 and A8 lamps	ON	
1430	MLDD	Press and release 0A8		
1440	MLDD	COMMAND and COMPTR 0A8 lamp	OFF	
1450	MLDD	Press and release 0A9		
1460	MLDD	COMMAND 0A9 lamp	ON	
1470	MLDD	ADVANCE and CST lamps	ON	
1480	MLDD	Press and release 0A9		
1490	MLDD	COMMAND 0A9 lamp	OFF	
1500	MLDD	Press and release A2, A8 and A7		
1510	MLDD	COMMAND A2 and A8 lamps	OFF	

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Figure 7-18. Interrupt Checks (Sheet 6)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: 'LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1520	MLDD	COMMAND A7 lamp	ON	
1530	MLDD	Press and release ADVANCE/CST		
1540	MLDD	COMPTR and COMMAND A3, A6 and A7 lamps	ON	
1550	MLDD	Press and release 0A5, 0A4, and 0A2		
1560	MLDD	COMMAND 0A5, 0A4, and 0A2 lamps	ON	
1570	IE	Turn BIT GATE to 2		
1580	MLDD	Press and release ADVANCE/CST (2 times)		
1590	MLDD	COMPUTER 0A5, 0A4 and 0A2 lamps	ON	
1600	MLDD	DATA COMPUTER 22, 23, 24, and 25 lamps	ON	
1610	IE	INTC lamp	OFF	
1620	MLDD	Press and release 0A5 and 0A4		
1630	MLDD	COMMAND 0A5 and 0A4 lamps	OFF	
1640	MLDD	Press and release SINGLE STEP ON/OFF		
1650	MLDD	ON, ADVANCE and CST lamps	OFF	
1660	MLDD	OFF lamp	ON	
1670	MLDD	COMPTR 0A5 and 0A4 lamps	OFF	
1680	MLDD	Press and release 0A8		
1690	MLDD	COMMAND and COMPTR 0A8 lamp	ON	
1700	MLDD	Press and release 0A2		
1710	MLDD	COMMAND and COMPTR 0A2 lamp	OFF	
1720	IE	INTC lamp	ON	
1730	MLDD	Press and release 0A8		
1740	MLDD	COMMAND and COMPTR 0A8 lamp	OFF	
1750	MLDD	Press and release MANUAL RE-START		
1760	IE	INTC lamp	OFF	
1770	IE	MANUAL MLC INH lamp (if OFF press and release MANUAL MLC INH)	ON	

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Figure 7-18. Interrupt Checks (Sheet 7)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
1780	IE	MANUAL SSC INH lamp (if OFF press and release MANUAL SSC INH)	ON	
1790	MLDD	Press and release COMMAND DISPLAY RESET and COMPTR DISPLAY RESET		
1800	MLDD	COMMAND and COMPTR ADR lamps	OFF	
1810	IE	INTC lamp	ON	
1820	MLDD	Turn DISPLAY SELECT to position 14		
1830	MLDD	ALL DATA COMPTR lamps	OFF	
1840	MLDD	Press and release MANUAL RESTART		
1850	IE	INTC lamp	OFF	
1860	MLDD	Press and release ON/OFF		
1870	MLDD	ON, ADVANCE and CST lamps	ON	
1880	MLDD	OFF lamp	OFF	
1890	IE	Press and release OP/TP		
1900	IE	OP lamp	ON	
1910	IE	TP lamp	OFF	
1920	TRMC	Press and release ADR 3		
1930	TRMC	ADR 3 lamp	ON	
1940	MLDD	Press and release 0A1, 0A2 and 0A3		
1950	MLDD	COMMAND 0A1, 0A2 and 0A3 lamps	ON	
1960	MLDD	Press and release ADVANCE/CST		
1970	MLDD	All DATA lamps except 10 (DATA LAMP 10 may be on)	OFF	
1980	MLDD	COMPTR 0A1, 0A2, 0A3 and A2 lamps	ON	
1990	IE	INTC lamp	OFF	
2000	IE	EAM lamp	ON	
2010	IE	Press and release OP/TP		
2020	IE	OP lamp	OFF	
2030	IE	TP lamp	ON	
2035	IE	Press and release RESET PIOR		
2036	IE	RESET PIOR lamp	OFF	
2040	IE	INTC lamp	ON	
2050	MLDD	DATA COMPTR SIGN through 25 lamps	ON	
2060	MLDD	ADVANCE/CST lamps	OFF	
2070	IE	Press and release MANUAL MLC INH		
2075	IE	MANUAL MLC INH lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 8)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2090	IE	Press and release MANUAL SSC INH		
2100	IE	MANUAL SSC INH lamp	OFF	
2110	MLDD	Press and release 0A1, 0A2 and 0A3		
2120	MLDD	COMMAND and COMPTR 0A1, 0A2 and 0A3 lamps	OFF	
2130	TRMC	Press and release ADR 3		
2140	IE	Press and release ERROR RESET		
2150	IE	EAM lamp	OFF	
2160	IE	INTC lamp	OFF	
2170	MLDD	DATA COMPUTER SIGN through 25 lamps	OFF	
2180	MLDD	ADVANCE/CST lamps	ON	
2190	TRMC	Press and release ADR 5		
2200	TRMC	ADR 5 lamp	ON	
2210	MLDD	Press and release DS3		
2220	MLDD	DS 3 lamp	ON	
2230	MLDD	Press and release ADVANCE/CST		
2240	MLDD	ADVANCE and CST lamps	OFF	
2250	MLDD	ON lamp	ON	
2260	IE	INTC lamp	ON	
2270	TRMC	Press and release ADR 5		
2280	TRMC	ADR 5 lamp	OFF	
2290	MLDD	Press and release DS 3 lamp		
2300	MLDD	DS 3 lamp	OFF	
2310	MLDD	Press and release 0A1, 0A2, 0A4, 0A5		
2320	MLDD	COMMAND and COMPUTER 0A1, 0A2, 0A4 and 0A5 lamps	ON	
2330	IE	INTC lamp	ON	
2340	MLDD	Press and release 0A2		
2350	MLDD	COMMAND and COMPUTER 0A2 lamp	OFF	
2360	MLDD	Press and release 0A1		
2370	MLDD	COMMAND and COMPUTER 0A1 lamp	OFF	
2380	IE	INTC lamp	ON	

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Figure 7-18. Interrupt Checks (Sheet 9)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2390	MLDD	Press and release 0A3		
2400	MLDD	COMMAND and COMPUTER 0A3 lamp	ON	
2410	MLDD	Press and release 0A2		
2420	MLDD	COMMAND and COMPUTER 0A2 lamp	ON	
2430	IE	INTC lamp	ON	
2440	MLDD	Press and release 0A4		
2450	MLDD	COMMAND and COMPUTER 0A4 lamp	OFF	
2460	MLDD	Press and release 0A3		
2470	MLDD	COMMAND and COMPUTER 0A3 lamp	OFF	
2480	IE	INTC lamp	ON	
2490	MLDD	Press and release 0A5		
2500	MLDD	COMMAND and COMPUTER 0A5 lamp	OFF	
2510	MLDD	Press and release 0A4		
2520	MLDD	COMMAND and COMPUTER 0A4 lamp	ON	
2530	IE	INTC lamp	ON	
2540	MLDD	Press and release 0A6		
2550	MLDD	COMMAND and COMPUTER 0A6 lamp	ON	
2560	MLDD	Press and release 0A5		
2570	MLDD	COMMAND and COMPUTER 0A5 lamp	ON	
2580	IE	INTC lamp	ON	
2590	MLDD	Press and release 0A7		
2600	MLDD	COMMAND and COMPUTER 0A7 lamp	ON	
2610	MLDD	Press and release 0A6		
2620	MLDD	COMMAND and COMPUTER 0A6 lamp	OFF	
2630	IE	INTC lamp	ON	
2640	MLDD	Press and release COMMAND DISPLAY RESET		
2650	MLDD	COMMAND and COMPUTER lamps	OFF	
2660	MLDD	Press and release 0A9		
2670	MLDD	COMMAND 0A9 lamp	ON	
2680	MLDD	ADVANCE/CST lamps	ON	
2690	IE	INTC lamp	ON	
2700	MLDD	Press and release 0A9		
2710	MLDD	COMMAND 0A9 lamp	OFF	
2720	MLDD	Press and release 0A2, 0A4 and 0A5		

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Figure 7-18. Interrupt Checks (Sheet 10)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
2730	MLDD	COMMAND 0A2, 0A4 and 0A5 lamps	ON	
2740	MLDD	Press and release ADVANCE/CST		
2750	MLDD	COMPUTER 0A2, 0A4 and 0A5 lamps	ON	
2760	MLDD	Press and release 0A2, 0A4 and 0A5		
2770	MLDD	COMMAND 0A2, 0A4 and 0A5 lamps	OFF	
2780	IE	INTC lamp	ON	
2790	TRMC	Press and release ADR 5		
2800	TRMC	ADR 5 lamp	ON	
2810	MLDD	Press and release DS 4		
2820	MLDD	COMMAND DS 4 lamp	ON	
2830	MLDD	Press and release ADVANCE/CST		
2840	MLDD	COMPUTER 0A2, 0A4, and 0A5 lamps	OFF	
2850	IE	INTC lamp	OFF	
2860	TRMC	Press and release ADR 5		
2870	TRMC	ADR 5 lamp	OFF	
2880	MLDD	Press and release DS 4		
2890	MLDD	COMMAND DS 4 lamp	OFF	
2900	TRMC	Press and release ADR1, ADR2		
2910	TRMC	ADR1, ADR2 and ADR6 lamps	ON	
2920	MLDD	Press and release 0A5		
2930	MLDD	COMMAND 0A5 lamp	ON	
2940	MLDD	Press and release ADVANCE/CST		
2950	IE	INTC lamp (if ALL lamp is ON)	ON	
2960	IE	Press and release MANUAL HALT/ COMPTR HALT		
2970	IE	MANUAL HALT and COMPTR HALT lamps	ON	
2980	IE	CHANNEL lamp (if OFF press and release)	ON	
2990	IE	MODULE lamp	OFF	
3000	IE	Press and release ALL		
3010	IE	ALL lamp	ON	
3012	IE	Press and release MANUAL HALT		
3013	MLDD	Press and release ON/OFF		
3014	MLDD	Press and release ADVANCE		
3015	MLDD	Press and release ON/OFF		
3020	IE	INTC lamp	ON	

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Figure 7-18. Interrupt Checks (Sheet 11)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3030	MLDD	ON, ADVANCE and CST lamps	OFF	
3040	MLDD	Press and release MANUAL RE-START		
3060	MLDD	Press and release SINGLE STEP ON/OFF		
3070	MLDD	ON, ADVANCE and CST lamps	ON	
3090	IE	INTC lamp	OFF	
3100	IE	Press and release MANUAL HALT/ COMPTR HALT		
3110	IE	MANUAL HALT and COMPTR HALT lamps	ON	
3120	IE	Press and release CHANNEL 1 (CH2=1, CH3=0, CH2=0, CH3=1)		
3130	IE	ALL lamp	OFF	
3140	IE	CHANNEL 1 (CH2=1, CH3=0) lamp	OFF	
3150	IE	CHANNEL 1 (CH2=0, CH3=1) lamp	ON	
3160	IE	Press and release MANUAL HALT/ COMPTR HALT		
3170	IE	MANUAL HALT and COMPTR HALT lamps	OFF	
3180	MLDD	Press and release 0A5		
3190	MLDD	COMMAND and COMPUTER 0A5 lamp	OFF	
3200	TRMC	Press and release ADR 3 lamp	ON	
3210	TRMC	Press and release ADR1, ADR2 and ADR3		
3220	TRMC	ADR1, ADR2, ADR3 and ADR6 lamps	OFF	
3230	MLDD	Press and release A2 and A3		
3240	MLDD	COMMAND and COMPUTER A2 and A3 lamps	ON	
3250	MLDD	Press and release ON/OFF		
3260	MLDD	ON lamp	ON	
3270	MLDD	OFF lamp	OFF	
3280	MLDD	Press and release 0A9		
3290	MLDD	COMMAND 0A9 lamp	ON	
3300	MLDD	Press and release COMPTR DIS-PLAY RESET		
3310	IE	Press and release ERROR RESET		
3320	IE	COMPTR ALARM lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 12)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3330	MLDD	Turn DISPLAY SELECT to 14		
3340	MLDD	Press and release 0A9		
3350	MLDD	COMMAND 0A9 lamp	OFF	
3360	MLDD	Press and release A1, A3, and A5		
3370	MLDD	COMMAND A3 lamp	OFF	
3380	MLDD	COMMAND A1, A2 and A5 lamps	ON	
Note:		DATA COMPUTER 10 lamp will flash ON and then go OFF when step 3390 is exercised		
3390	MLDD	Press and release ON/OFF		
3400	MLDD	DATA COMPUTER lamp 10	ON/OFF	
3410	MLDD	ON, ADVANCE and CST lamps	OFF	
3420	MLDD	OFF lamp	ON	
3430	MLDD	COMPUTER A1, A2 and A5 lamps	ON	
3440	IE	COMPTR ALARM lamp	ON	
3450	IE	INTC lamp	ON	
3460	MLDD	Press and release MANUAL RESTART		
3470	IE	INTC lamp	OFF	
3480	MLDD	Press and release COMMAND DISPLAY RESET		
3490	MLDD	All COMMAND and COMPUTER lamps	OFF	
3500	IE	Press and release MANUAL MLC INH		
3510	IE	MANUAL MLC INH lamp	ON	
3520	IE	Press and release MANUAL SSC INH		
3530	IE	MANUAL SSC INH lamp	ON	
3540	MLDD	Press and release A2 and A3		
3550	MLDD	COMMAND and COMPUTER A2 and A3 lamps	ON	
3560	MLDD	Press and release ON/OFF		
3570	MLDD	ON, ADVANCE and CST lamps	ON	
3580	MLDD	OFF lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 13)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3590	MLDD	Press and release 0A9		
3600	MLDD	COMMAND 0A9 lamp	ON	
3610	MLDD	Press and release COMPUTER DISPLAY RESET		
3620	IE	Press and release ERROR RESET		
3630	IE	COMPUTER ALARM lamp	OFF	
3640	MLDD	Press and release 0A9		
3650	MLDD	COMMAND 0A9 lamp	OFF	
3660	IE	Press and release OP/TP		
3670	IE	OP lamp	ON	
3680	IE	TP lamp	OFF	
3690	MLDD	Press and release ADVANCE/CST		
3700	IE	RESET PIOR lamp	ON	
3710	IE	Press and release RESET PIOR		
3720	IE	RESET PIOR lamp	OFF	
Note:		DATA COMPUTER 10 lamp (may be ON or OFF)		
3730	IE	Press and release OP/TP		
3740	IE	OP lamp	OFF	
3750	IE	TP lamp	ON	
3760	MLDD	Press and release ON/OFF		
3770	MLDD	ON, ADVANCE and CST lamps	OFF	
3780	MLDD	OFF lamp	ON	
3790	MLDD	DATA COMPTR SIGN through 25 lamps	OFF	
3800	MLDD	Press and release MANUAL RESTART		
3810	IE	INTC lamp	OFF	
3820	MLDD	Press and release COMMAND DISPLAY RESET		
3830	MLDD	All COMMAND lamps	OFF	
3840	MLDD	Press and release ERROR OVER RIDE		
3850	MLDD	ERROR OVER RIDE lamp	ON	
3860	MLDD	Press and release A2 and A3		
3870	MLDD	COMMAND and COMPUTER A2 and A3 lamps	ON	

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Figure 7-18. Interrupt Checks (Sheet 14)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
3880	MLDD	Press and release ON/OFF		
3890	MLDD	ON, ADVANCE and CST lamps	ON	
3900	MLDD	OFF lamp	OFF	
3910	MLDD	Press and release 0A9		
3920	MLDD	COMMAND 0A9 lamp	ON	
3930	MLDD	Press and release COMPTR DISPLAY RESET		
3940	IE	Press and release ERROR RESET		
3950	IE	COMPTR ALARM lamp	OFF	
3960	MLDD	Turn DISPLAY SELECT to 14		
3970	MLDD	Press and release 0A9		
3980	MLDD	COMMAND 0A9 lamp	OFF	
3990	MLDD	Press and release A1, A3, and A5		
4000	MLDD	COMMAND A3 lamp	OFF	
4010	MLDD	COMMAND A1, A2 and A5 lamps	ON	
4020	MLDD	Press and release ON/OFF		
4030	MLDD	ON, ADVANCE and CST lamps	OFF	
4040	MLDD	OFF lamp	ON	
4050	MLDD	COMPUTER A1, A2 and A5 lamps	ON	
4060	IE	INTC lamp	OFF	
4070	MLDD	Press and release ERROR OVER RIDE		
4080	MLDD	ERROR OVER RIDE lamp	OFF	
4090	IE	INTC lamp	ON	
4100	MLDD	Press and release MANUAL RESTART		
4110	IE	INTC lamp	OFF	
4120	MLDD	Press and release COMMAND DISPLAY RESET		
4130	MLDD	All COMMAND lamps	OFF	
4140	MLDD	Press and release A1, A2 and A3		
4150	MLDD	COMMAND and COMPUTER A1, A2 and A3 lamps	ON	
4160	MLDD	Press and release ON/OFF		
4170	MLDD	ON, ADVANCE and CST lamps	ON	
4180	MLDD	OFF lamp	OFF	
4190	MLDD	Press and release REPEAT/SINGLE		
4200	MLDD	REPEAT lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 15)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4210	MLDD	SINGLE lamp	ON	
4220	IE	MANUAL MLC INH lamp (Press and release if OFF)	ON	
4230	IE	MANUAL SSC INH lamp (Press and release if OFF)	ON	
4235	MLDD	Press and release A1, A2 and A3		
4236	MLDD	COMMAND and COMPUTER A1, A2 and A3 lamps	ON	
4240	IE	Press and release OP/TP		
4250	IE	OP lamp	ON	
4260	IE	TP lamp	OFF	
4270	IE	Press and release MANUAL HALT/ COMPUTER HALT		
4280	MLDD	ON, ADVANCE and CST lamps	OFF	
4290	MLDD	Press and release COMPUTER DISPLAY RESET		
4300	MLDD	DATA COMPUTER 8 and 22 lamps	ON	
4310	IE	RESET PIOR lamp	ON (Dim)	
4315	MLDD	Press and release REPEAT/SINGLE		
4320	MLDD	REPEAT lamp	ON	
4330	MLDD	SINGLE lamp	OFF	
4340	IE	Press and release OP/TP		
4350	IE	OP lamp	OFF	
4360	IE	TP lamp	ON	
4370	IE	Press and release MANUAL HALT/ COMPUTER HALT		
4380	IE	MANUAL HALT and COMPUTER HALT lamps	OFF	
4390	IE	INTC lamp	ON	
4400	MLDD	Press and release MANUAL RESTART		
4410	IE	INTC lamp	OFF	
4420	MLDD	Press and release COMMAND DISPLAY RESET		
4430	MLDD	All COMMAND lamps	OFF	
4440	MLDD	Press and release ON/OFF		
4450	MLDD	ON, ADVANCE and CST lamps	ON	
4460	IE	Press and release I/O Reg. RESET		
4470	IE	Press and release I/O Reg. No. 2		
4480	IE	I/O Reg. No. 2 lamp	ON	
4490	IE	Press and release I/O Reg. RESET		

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Figure 7-18. Interrupt Checks (Sheet 16)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4500	IE	All I/O Reg. lamps	OFF	
4510	IE	Press and release I/O Reg. Bit 12		
4520	IE	I/O Reg. No. 2 lamp	ON	
4530	IE	Press and release MANUAL MLC INH		
4540	IE	MANUAL MLC INH lamp	OFF	
4550	IE	Press and release OP/TP		
4560	IE	OP lamp	ON	
4570	IE	TP lamp	OFF	
4580	MLDD	Press and release ADVANCE/CST until INTC lamp goes ON and I/O Reg. No. 2 lamp 12 goes OFF		
4590	IE	INTC lamp	ON	
4600	IE	I/O Reg. No. 2 lamp 12	OFF	
4610	MLDD	Press and release COMPUTER DISPLAY RESET		
4620	IE	Press and release OP/TP		
4630	IE	OP lamp	OFF	
4640	IE	TP lamp	ON	
4650	MLDD	Press and release MANUAL RESTART		
4660	IE	INTC lamp	OFF	
4665	MLDD	Press and release A1, A2 and A3		
4666	MLDD	COMMAND and COMPUTER lamps A1, A2 and A3	OFF	
4670	TRMC	Press and release ADR 5		
4680	TRMC	ADR 5 lamp	ON	
4690	MLDD	Press and release A2		
4700	MLDD	COMMAND A2 lamp	ON	
4710	IE	DISCR MLC INH lamp	ON	
4720	IE	Press and release OP/TP		
4730	IE	OP lamp	ON	
4740	IE	TP lamp	OFF	
4750	IE	INTC lamp	OFF	
4760	IE	Press and release OP/TP		
4770	IE	OP lamp	OFF	
4780	IE	TP lamp	ON	
4790	MLDD	Press and release MANUAL RESTART		
4800	IE	RESET PIOR lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 17)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
4810	MLDD	CST lamp	OFF	
4820	MLDD	Press and release A2		
4830	MLDD	COMMAND A2 lamp	OFF	
4840	IE	DISCR MLC INH lamp	OFF	
4850	IE	Press and release MANUAL SSC INH		
4860	IE	MANUAL SSC INH lamp	OFF	
4870	IE	Press and release MANUAL MLC INH		
4880	IE	MANUAL MLC INH lamp	ON	
4890	MLDD	Press and release A1		
4900	MLDD	COMMAND A1 lamp	ON	
4910	IE	DISCR SSC INH lamp	ON	
4920	MLDD	Press and release ON/OFF		
4930	MLDD	ON and CST lamps	ON	
4940	IE	Press and release I/O Reg. No. 25		
4950	IE	I/O Reg. No. 2 lamp 25	ON	
4960	MLDD	Press and release ON/OFF		
4970	MLDD	ON and CST lamps	OFF	
4980	MLDD	OFF lamp	ON	
4990	IE	Press and release OP/TP		
5000	IE	OP and RESET PIOR lamps	ON	
5010	IE	TP and INTC lamps I/O Reg. No. 2 lamp 25	OFF	
5020	IE	Press and release OP/TP		
5030	IE	OP lamp	OFF	
5040	IE	TP lamp	ON	
5050	MLDD	Press and release MANUAL RESTART		
5060	MLDD	CST lamp	OFF	
5070	IE	RESET PIOR lamp	OFF	
5080	MLDD	Press and release A1		
5090	MLDD	COMMAND A1 lamp	OFF	

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Figure 7-18. Interrupt Checks (Sheet 18)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
5100	TRMC	Press and release ADR 5		
5110	TRMC	ADR 5 lamp	OFF	
5120	IE	DISCR SSC INH lamp	OFF	
5130	MLDD	Press and release ON/OFF		
5140	MLDD	ON, ADVANCE and CST lamps	ON	
5150	IE	Press and release I/O Reg. No. 2 RESET		
5155	IE	Press and release RESET PIOR		
5160	IE	Press and release OP/TP		
5170	IE	OP lamp	ON	
5180	IE	TP lamp	OFF	
5190	MLDD	Press and release ON/OFF		
5200	MLDD	ON and ADVANCE lamps	OFF	
5210	MLDD	CST lamps	ON	
5220	IE	RESET PIOR and INTC lamps	ON	
5230	IE	Press and release OP/TP		
5240	IE	OP lamp	OFF	
5250	IE	TP lamp	ON	
5260	MLDD	Press and release COMPTR DISPLAY RESET		
5270	MLDD	Press and release COMMAND DISPLAY RESET		
5280	MLDD	Press and release MANUAL RESTART		
5290	MLDD	Press and release ON/OFF		
5300	PC	Press and release COMPUTER POWER SEQ OFF		
5310	PC	COMPUTER POWER SEQ ON lamp	OFF	
5320	PC	COMPUTER POWER SEQ OFF lamp (delayed)	ON	
5330	PC	Press and release ACME POWER SEQ OFF		
5340	PC	ACME POWER SEQ ON lamp	OFF	
5350	PC	ACME POWER SEQ OFF lamp (delayed)	ON	
5360	PC	Press and release MAIN POWER OFF		

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Figure 7-18. Interrupt Checks (Sheet 19)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO. 6902000

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
5370	PC	MAIN POWER ON, PHASE 1, 2, 3, and FAN lamps	OFF	
5380	PC	MAIN POWER OFF lamp	ON	
5390	PC	Pull EMERGENCY PULL		
5400	PC	MAIN POWER OFF, ACME POWER SEQ OFF and COMPUTER POWER SEQ OFF lamps	OFF	
5410	01B	Open side panel 01B and record ETI	ETI hrs	
5420	01B	Close side panel 01B		

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Figure 7-18. Interrupt Checks (Sheet 20)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	PC	Connect a digital voltmeter (DVM) between test points -26.5 VDC and GRD.		
20	PC	Turn -26.5 VDC adjustment full CCW		
30	DVM	Record voltage	-25.185 to -25.815 VDC	
40	PC	Turn -26.5 VDC adjustment full CW		
50	DVM	Record voltage	-27.185 to -27.815 VDC	
60	PC	Set the -26.5 VDC adjustment so that -26.5 VDC is read on the DVM.	-26.47 to -26.53 VDC	
70	PC	Disconnect lead from -26.5 VDC TP and connect to -12 VDC.		
80	PC	Turn -12 VDC adjustment full CCW		
90	DVM	Record voltage	-10.81 to -11.19 VDC	
100	PC	Turn -12 VDC adjustment full CW		
110	DVM	Record voltage	-12.81 to -13.19 VDC	
120	PC	Set -12 VDC adjustment so that -12 VDC is read on the DVM. Record.	-11.98 to -12.1 VDC	
130	PC	Disconnect lead from -12 VDC TP and connect to 12 VDC		
140	PC	Turn 12 VDC adjustment full CCW		
150	DVM	Record voltage	10.79 to 11.21 VDC	
160	PC	Turn 12 VDC adjustment full CW		
170	DVM	Record voltage	12.79 to 13.21 VDC	
180	PC	Set 12 VDC adjustment so that 12 VDC is read on the DVM. Record.	11.98 to 12.05 VDC	
190	PC	Disconnect lead from 12 VDC TP and connect to -6 VDC		
200	PC	Turn -6 VDC adjustment full CCW		
210	DVM	Record voltage	-4.89 to -5.11 VDC	
220	PC	Turn -6 VDC adjustment full CW		

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Figure 7-19. Secondary Power Adjustments (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
230	DVM	Record voltage	-6.89 to -7.11 VDC	
240	PC	Set -6 VDC adjustment so that -6 VDC is read on the DVM. Record.	-5.985 to -6.05 VDC	
250	PC	Disconnect test leads from -6 VDC and GRD test points.		

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Figure 7-19. Secondary Power Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
10	PC	Connect a digital voltmeter (DVM) between the +20 VDC and RET jacks		
20	PC	Turn +20 VDC adjustment full CCW		
30	DVM	Record voltage	18.71 to 19.29 VDC	
40	PC	Turn +20 VDC adjustment full CW		
50	DVM	Record voltage	20.71 to 21.29 VDC	
60	PC	Set +20 VDC adjustment so that 20 VDC is read on the DVM Record	19.985 to 20.015 VDC	
70	PC	Disconnect meter leads from +20 VDC and RET jacks and connect to +12 VDC and RET jacks		
80	PC	Turn +12 VDC adjustment full CCW		
90	DVM	Record voltage	10.79 to 11.21 VDC	
100	PC	Turn +12 VDC adjustment full CW		
110	DVM	Record voltage	12.79 to 13.21 VDC	
120	PC	Set +12 VDC adjustment so that 12 VDC is read on the DVM. Record	11.99 to 12.01 VDC	
130	PC	Disconnect meter leads from +12 VDC and RET jacks and connect to +6 VDC and RET jacks.		
140	PC	Turn +6 VDC adjustment full CCW		
150	DVM	Record voltage	4.89 to 5.11 VDC	
160	PC	Turn +6 VDC adjustment full CW		
170	DVM	Record voltage	6.89 to 7.11 VDC	
180	PC	Set +6 VDC adjustment so that 6 VDC is read on the DVM. Record	5.99 to 6.01 VDC	
190	PC	Disconnect meter leads from +6 VDC and RET jacks and connect to -3 VDC and RET jacks.		

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Figure 7-20. Computer Power Adjustments (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
200	PC	Turn -3 VDC adjustment full CCW		
210	DVM	Record voltage	-1.9 to -2.1 VDC	
220	PC	Turn -3 VDC adjustment full CW		
230	DVM	Record voltage	-3.9 to -4.1 VDC	
240	PC	Set -3 VDC adjustment so that -3 VDC is read on the DVM. Record.	-2.995 to -3.005 VDC	
250	PC	Disconnect meter leads from -3 VDC and RET jacks and connect to +12 MS VDC and RET jacks.		
260	PC	Turn +12 MS adjustment full CCW		
270	DVM	Record voltage	10.79 to 11.21 VDC	
280	PC	Turn +12 MS adjustment full CW		
290	DVM	Record voltage	12.79 to 13.21 VDC	
300	PC	Set +12 MS adjustment so that 12 VDC is read on the DVM. Record.	11.99 to 12.01 VDC	
310	PC	Disconnect meter leads from +12MS VDC and RET jacks and connect to +6 MS VDC and RET jacks.		
320	PC	Turn +6 MS adjustment full CCW		
330	DVM	Record voltage	4.85 to 5.15 VDC	
340	PC	Turn +6 MS adjustment full CW		
350	DVM	Record voltage	6.85 to 7.15 VDC	
360	PC	Set +6 MS adjustment so that 6 VDC is read on the DVM. Record	6.005 to 6.025 VDC	
370	PC	Disconnect meter leads from +6 MS VDC and RET jacks.		

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Figure 7-20. Computer Power Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
Note		The overvoltage limits of all power supplies are checked and actual cut out voltage recorded.		
380		Overvoltage limits -26.5 VDC ACME Power Supply	36 VDC Min.	
390		Overvoltage limits 12 VDC ACME Power Supply	15 to 16 VDC	
400		Overvoltage limits 12 VDC ACME Power Supply	15 to 16 VDC	
410		Overvoltage limits -6 VDC ACME Power Supply	8 to 9 VDC	
420		Overvoltage limits 12 MS Power Supply	15 to 16 VDC	
430		Overvoltage limit 6 MS Power Supply	8 to 9 VDC	
440		Overvoltage limit 12 VDC COMPUTER Power Supply	15 to 16 VDC	
450		Overvoltage limit 6 VDC COMPUTER Power Supply	8 to 9 VDC	
460		Overvoltage limit 20 VDC COMPUTER Power Supply	22 to 23 VDC	
470		Overvoltage limits -3 VDC COMPUTER Power Supply	4 to 5 VDC	

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Figure 7-20. Computer Power Adjustments (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
10	TRMC	Press and Release FREE RUN SS FREE RUN SS lamp	ON	
20	TRMC	Connect Oscilloscope input A to TP1		
30	01B3	Adjust potentiometer on card A05 for mean up level of 1100 Usec	942-1275 Usec	
40	01B3	Adjust potentiometer on card A09 for a mean down level of 900 Usec	753-1062 Usec	
50	TRMC	Connect oscilloscope input A to TP2		
60	01B3	Adjust potentiometer on card A07 to obtain a mean down level of 175 Usec	140-200 Usec	
70	TRMC	Connect Oscilloscope input A to TP3		
80	01B3	Adjust potentiometer on Card A10 for a mean down level duration of 200 Usec	140-265 Usec	
90	TRMC	Connect Oscilloscope input A to TP4		
100	01B3	Adjust potentiometer on card A11 to obtain a mean down level duration of 375 Usec.	300-450 Usec	
110	TRMC	Connect Oscilloscope input A to TP5		
120	01B3	Adjust potentiometer on A13 to obtain a mean down level duration of 250 Usec	140-342 Usec	
130	TRMC	Connect Oscilloscope input A to TP6		
140	01B3	Adjust potentiometer on card B06 for a mean up level duration of 100 Msec.	90-120 Msec	
150	01B3	Adjust potentiometer on card B05 for a mean down level duration of 100 Msec.	90-120 Msec	
160	TRMC	Connect oscilloscope input A to TP17		
170	01B3	Adjust potentiometer on card F19 for a mean down level duration of 500 Usec	140-1100 Usec.	
180	01B3	Connect oscilloscope input A to B04H		
190	01B3	Adjust potentiometer on card D12 for a mean down level duration of 750 Nsec	140-1000 Nsec	

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Figure 7-21. Tape Reader Clock Adjustments (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
200	TRMC	Connect oscilloscope input A and Scope Sync input to TP1. Connect oscilloscope input B to TP2 Sync. external -		
210	01B3	Adjust potentiometer on card A06 for a mean delay duration between start of down levels of two waveshapes of 175 Usec.	140-200 Usec.	
220	TRMC	Connect oscilloscope input A and Scope Sync to TP2. Connect oscilloscope input B to TP3.		
230	01B3	Adjust potentiometer on card A08 for a mean delay duration between start of down levels of two waveshapes of 250 Usec.	210-280 Usec.	
240	TRMC	Connect oscilloscope input A and Scope Sync to TP4. Connect oscilloscope input B to TP5.		
250	01B3	Adjust potentiometer on card A12 for a mean delay duration between start of down levels of two waveshapes of 525 Usec.	460-600 Usec.	
260	TRMC	Connect oscilloscope input A and Scope Sync to TP6. Connect oscilloscope input B to TP7. Sync Ext. +		
270	01B3	Adjust potentiometer on card B17 for a mean delay duration between start of the two waveshapes' up levels of 40 Msec.	30 to 50 Msec.	
280	TRMC	Connect oscilloscope input B to TP17 Leave oscilloscope input A and Sync input in TP6		
290	01B3	Adjust potentiometer on card F18 for a mean delay duration from the up level start of waveshape A to the down level start of waveshape B of 150 Msec.	130-170 Msec.	

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Figure 7-21. Tape Reader Clock Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
NOTE		Use M Type Preamp in Type 585 Scope		
10	02A3	Connect Scope Probe No. 1 to TP7		
20	02B2	Connect Scope Probe No. 2 to D-23-A Set scope sync to EXT. plus and connect "A" signal out" of Preamp to Trigger input of Scope. Horizontal Display to "A Del'd by B".		
30	Scope	Input No. 2 mean value is coincident with Input No. 1 (leading edge)	± 50 NS	
40	02B2	Adjust SMS card in B25		
50	02A3	Connect scope probe No. 1 to TP1		
60	02B3	Connect scope probe No. 2 to D-23-P		
70	Scope	Input No. 2 mean value is coincident with Input No. 1 (leading edge)	± 50 NS	
80	02B2	Adjust SMS card in C24		
90	02A3	Connect scope probe No. 1 to TP10		
100	02B2	Connect scope probe No. 2 to D-23-D		
110	Scope	Input No. 2 mean value is coincident with Input No. 1 (leading edge)	± 50 NS	
120	02B2	Adjust SMS card B26		
130	02A3	Connect scope probe No. 1 to TP4		
140	02B2	Connect scope probe No. 2 to D-22-A		
150	Scope	Input No. 2 mean value is coincident with No. 1 (leading edge)	± 50 NS	
160	02B2	Adjust SMS card B-24		
170	02B2	Connect scope probe No. 2 to A-17-P		
180	TRMC	Press and release Free Run Single Shot.		
185	TRMC	Free Run Single Shot lamp	ON	
190	02B2	Adjust SMS card A-17 for a mean down level of 650 NS	± 50 NS	
200	02B2	Connect scope probe No. 2 to A-18-P		
210	02B2	Adjust SMS card A-18 for a mean down level of 650 NS	± 50 NS	
220	02B2	Connect scope probe No. 2 to A-19-P		
230	02B2	Adjust SMS card A-19 for a mean down level of 650 NS	± 50 NS	
240	02B2	Connect scope probe No. 2 to A-20-P		
250	02B2	Adjust SMS card A-20 for a mean down level of 650 NS		

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Figure 7-22. LVDCME Self-Check Timing Adjustments (Sheet 1 of 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
260	02A3	Remove scope probe No. 1 from TP4		
270	02B2	Remove scope probe No. 2 from A-20 P		
280	MLDD	Press and release Repeat/$\overline{\text{Repeat}}$		
290	MLDD	$\overline{\text{REPEAT}}$ lamp	OFF	
300	MLDD	REPEAT lamp	ON	
310	TRMC	Press and release Free Run Single Shot		
320	TRMC	Free Run Single Shot lamp	OFF	
330	IE	Turn Clock Rotary switch to Position 7		
340	IE	A1-$\overline{\text{BO}}$ lamp	ON	
350	02B4	Connect Scope external sync to B-05-B		
360	02B2	Connect scope probe No. 1 to B-05-R		
370	02B2	Connect scope probe No. 2 to B-05-Q		
380	02B2	With Scope Triggering source on neg. Ext. observe 2 u sec (approx.) Pos. pulse. Adjust the leading edge of the pos. going pulse on probe No. 2 with respect to the leading edge of the pos. pulse on probe No. 1 to 400 NS mean time by using the left hand pot on B05 facing the card side of the gate	± 50 NS	

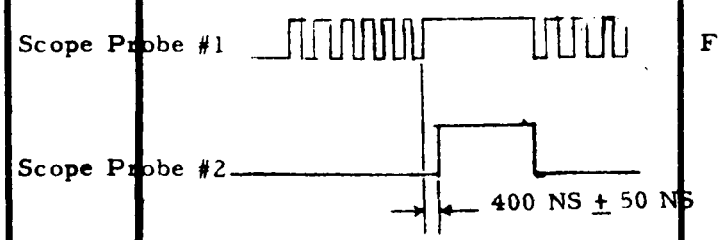

Figure 1

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Figure 7-22. LVDCME Self-Check Timing Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
390	IE	Turn the Clock Rotary switch to position 8		
400	02B2	Adjust the pos. going pulse on probe No. 2 with respect to the leading edge of the pos. pulse on probe No. 1 to 400 NS mean time by using the right pot on B05 facing the card side of gate (see Figure 1)	± 50 NS	
410	IE	Turn Clock Rotary switch to position 9		
420	02B2	Connect scope probe No. 1 to B06R Connect scope probe No. 2 to B06Q Adjust the positive going pulse on probe No. 2 with respec t to the leading edge of the positive pulse on probe No. 1 to 400 NS mean time by using the left hand pot on B06 facing the card side of the gate. (see fig. 1)	± 50 NS	
430	IE	Turn Clock Rotary switch to position 10.		
440	02B2	With the probes positioned as immediately above on BO6 adjust the positive going pulse on probe No. 2 with respect to the leading edge of the positive pulse on probe No. 1 to 400 NS using the right hand pot on BO6 facing the card side of the gate (see figure 1)	± 50 NS	
450	IE	Turn Clock Rotary switch to position 11		
460	02B2	Connect scope probe No. 1 to BO7R Connect scope probe No. 2 to BO7Q Adjust the positive going pulse on probe No. 2 with respect to the leading edge of the positive pulse on probe No. 1 to 400 NS mean time by using the left hand pot on BO7 facing the card side of the gate (See figure 1)	± 50 NS	

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Figure 7-22. LVDCME Self-Check Timing Adjustments (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
470	IE	Turn Clock Rotary switch to position 12		
480	02B2	With the scope probes position as immediately above on BO7 adjust the positive going pulse on probe No. 2 with respect to the leading edge of the positive pulse on probe No. 1 to 400 NS using the right hand pot. on BO7 facing the card side of the gate. (See figure 1)	± 50 NS	
490	MLDD	Press Repeat/$\overline{\text{Repeat}}$ switch.		
495	MLDD	$\overline{\text{Repeat}}$ lamp	ON	
500	02B4	Remove Scope Sync from B-05-B		
510	02B2	Remove Scope probes from Gate 02B2		
520	IE	Turn Clock Rotary switch to position NONE		
530	01B6	Connect scope probe No. 1 to A20-P Sync Scope Int. Neg.		
540	01B6	Adjust A-20 for a mean down level time of 400 NS	± 20 NS	
550	01B6	Connect Scope probe No. 1 to A21-P		
560	01B6	Adjust A21 for a mean down level time of 400 NS	± 20 NS	
570	01B6	Connect Scope probe No. 1 to A22-P		
580	01B6	Adjust A22 for a mean down level time of 400 NS	± 20 NS	
590	01B6	Connect Scope probe No. 1 to A23-P		
600	01B6	Adjust A23 for a mean down level time of 400 NS	± 20 NS	
610	02B2	Connect Scope Probe No. 1 to A21-P		
620	02B2	Adjust A21 for a mean down level time of 400 NS	± 20 NS	

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Figure 7-22. LVDCME Self-Check Timing Adjustments (Sheet 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
630	02B2	Connect Scope probe No. 1 to A22-P		
640	02B2	Adjust A22 for a mean down level time of 400 NS	± 20 NS	
650	02B2	Connect Scope probe No. 1 to A23-P		
660	02B2	Adjust A23 for a mean down level time of 400 NS	± 20 NS	
670	02B2	Connect Scope probe No. 1 to A24-P		
680	02B2	Adjust A24 for a mean down level time of 400 NS	± 20 NS	
690	02B7	Connect Scope probe No. 1 to B26-P		
700	02B7	Adjust B26 for a mean down level time of 400 NS	± 20 NS	

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Figure 7-22. LVDCME Self-Check Timing Adjustments (Sheet 5)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
10	PC	Press and release COMP POWER SEQ OFF		
20	PC	COMP POWER SEQ ON lamp	OFF	
30	PC	COMP POWER SEQ OFF lamp (delayed)	ON	
40	01B7	Open gate 01B7		
50	PC	If COMPUTER TEMP NORMAL lamp is ON, omit steps 60 through 65	ON	
60	01B7 & PC	If the HIGH and ARRAY lamps are ON adjust the left hand potentiometer in location 01B7E07 in a CW direction until the NORMAL lamp lights.		
61	01B7 &PC	If the HIGH and PAGE lamps are ON adjust the right hand potentiometer in location 01B7E07 in a CW direction until the NORMAL lamp lights.		
63	IE	Press and release ERROR RESET		
65	PC	PAGE and ARRAY lamps	OFF	
70	01B7	Adjust the left hand potentiometer located at 01B7E07 in a CCW direction until the COMPUTER TEMP HIGH lamp lights		
80	PC	COMPUTER TEMP HIGH lamp	ON	
90	PC	COMPUTER TEMP NORMAL lamp	OFF	
95	PC	ARRAY lamp	ON	
100	01B7	Adjust the potentiometer in a CW direction until the COMPUTER TEMP HIGH lamp just extinguishes		
110	PC	COMPUTER TEMP HIGH lamp	OFF	
120	PC	COMPUTER TEMP NORMAL and ARRAY lamps	ON	
130	01B7	Adjust the right hand potentiometer in location 01B7E07 in a CCW direction until the COMPUTER TEMP HIGH lamp lights		
140	PC	COMPUTER TEMP HIGH, PAGE and ARRAY lamps	ON	
150	PC	COMPUTER TEMP NORMAL lamp	OFF	

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Figure 7-23. Computer Temperature Sensing Adjustment (Sheet 1 of 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
160	01B7	Adjust the potentiometer in a CW direction until the COMPUTER TEMP HIGH lamp just extinguishes.		
170	PC	COMPUTER TEMP HIGH lamp	OFF	
180	PC	COMPUTER TEMP NORMAL, HIGH and PAGE lamps	ON	
190	IE	Press and release ERROR RESET		
200	PC	COMPUTER TEMP ARRAY and PAGE lamps	OFF	
210	PC	Press and release COMP POWER SEQ ON		
220	PC	COMP POWER SEQ OFF lamp	OFF	
230	PC	COMP POWER SEQ ON lamp	ON	
240	IE	Turn PHASE switch CCW to 15		
250	PC	COMPUTER TEMP HIGH and ARRAY lamps	ON	
260	PC	COMPUTER TEMP NORMAL lamp	OFF	
270	PC	COMP POWER SEQ ON lamp	OFF	
280	PC	COMP POWER SEQ OFF lamp	ON (delayed)	
290	IE	Turn PHASE switch CW to NONE		
300	PC	COMPUTER TEMP HIGH lamp	OFF	
310	PC	COMPUTER TEMP NORMAL lamp	ON	
320	PC	Press and release COMP POWER SEQ ON		
330	PC	COMP POWER SEQ OFF lamp remains	ON	
340	IE	Press and release ERROR RESET		
350	PC	COMPUTER TEMP ARRAY lamp	OFF	
360	PC	Press and release COMP POWER SEQ ON		
370	PC	COMP POWER SEQ OFF lamp	OFF	
380	PC	COMP POWER SEQ ON lamp	ON	
390	IE	Turn PHASE switch CW to 14		
400	PC	COMPUTER TEMP PAGE and HIGH lamps	ON	
410	PC	COMPUTER TEMP NORMAL lamp	OFF	
420	PC	COMP POWER SEQ ON lamp	OFF	
430	PC	COMP POWER SEQ OFF lamp	ON (delayed)	
440	IE	Turn PHASE switch CCW to NONE		

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Figure 7-23. Computer Temperature Sensing Adjustment (Sheet 2)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
450	PC	COMPUTER TEMP HIGH lamp	OFF	
460	PC	COMPUTER TEMP NORMAL lamp	ON	
470	PC	Press and release COMP POWER SEQ ON		
480	PC	COMP POWER SEQ OFF lamp remains	ON	
490	IE	Press and release ERROR RESET		
500	PC	COMPUTER TEMP PAGE lamp	OFF	
510	PC	Press and release COMP POWER SEQ ON		
520	PC	COMP POWER SEQ OFF lamp	OFF	
530	PC	COMP POWER SEQ ON lamp	ON	
540	01B7	Close gate 01B7		

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Figure 7-23. Computer Temperature Sensing Adjustment (Sheet 3)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
10	MLDD	Press and release ERROR OVER RIDE ERROR OVER RIDE indicator lamp	ON	
20	TRMC	Press and release MEMORY SIM MEMORY SIM indicator lamp	ON	
30	IE	Press and release COMP HALT/MAN HALT MANUAL HALT indicator lamp	OFF	
40	MLDD	Press and release SINGLE STEP ON/OFF ON, CST, and ADVANCE indicator lamps	ON	
50	IE	Press and release I/O Reg. No. 1/ Reg. No. 2 I/O Reg. No. 2 indicator lamp	ON	
60	IE	Press and release I/O Reg. 19 I/O Reg. No. 2 Bit 19 lamp All other lamps undetermined	ON	
70	MLDD	Press and release A4 and A5 A4 and A5 COMMAND indicator lamps	ON	
80	MLDD	Press and release DATA 12, 13, 14 DATA COMMAND 12, 13, and 14 indicator lamps	ON	
90	MLDD	Press and release SINGLE STEP ON/OFF OFF indicator lamp	ON	
100	02A3	Using a scope with a Type M preamp, connect input probe #2 to TIMING MARKER.		
110	02A3	Connect "Trigger input, time base B" of scope to SYNC.		
120	SCOPE	Switch TRIGGER SOURCE, TIME BASE B to EXT AC, Switch HORIZONTAL DISPLAY to "A DELAYED BY B", Control knob STABILITY, TIME BASE A turned maximum clockwise. Switch TIME/CM OR DELAY/TIME, TIME BASE B to "0.2 Milli sec.". Switch TIME/CM, TIME BASE A to "5 MICRO SEC. " On preamp, switch MODE, chan A to NORMAL, DC		

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Figure 7-24. Delay Lines 1, 2, and 3 Adjustments (Sheet 1 of 4)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
120	cont'd	Switch V/CM of all four channels to "0.1"		
130	02B8	Connect scope input 1 to B08G.		
140	02B8	Connect scope input 3 to B16Q		
150	02B8	Connect scope input 4 to B08F		
160	IE	Switch PHASE to C		
170	IE	Switch BIT GATE to 6		
180	IE	Switch CLOCK PULSE to X		
190	SCOPE	Adjust STABILITY, TRIGGERING LEVEL of TIME BASE B, INTENSITY, FOCUS and ASTIGMATISM for a clear, stable display. Use scope mask, if necessary. Rotate DELAY TIME MULTIPLIER to approximately "0.25" Observe pulse on trace B. Adjust DELAY TIME MULTIPLIER until pulse appears in center of display. There should be four pulses on trace 1. The fourth pulse should be opposite pulse on trace 2. Now rotate DELAY TIME MULTIPLIER to approximately 5.60 (to 13th pulse on channel B of scope). Adjust this control to bring pulse on trace 2 to center of display. On preamp, turn Mode, Channel 1 OFF; Mode channel C to INVERT DC. Now verify that the pattern of pulses are the same as trace A was earlier, but that the pulse on trace B DOES NOT align itself with the fourth pulse. The fourth pulse on trace C should, in fact LEAD the pulse on trace B by approximately 2.4 MICRO sec. Turn on "5X MULTIPLIER".		

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Figure 7-24. Delay Lines 1, 2, and 3 Adjustments (Sheet 2)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
200	02B8	Just under blower fan on this gate locate four holes labled DL1, DL2, DL3, DL4. With screwdriver, CAREFULLY adjust DL3 until the separation of pulses above (step 190) is approximately 2.40 Micro secs.	+0.1 usec	
210	SCOPE	Rotate Mode, channel D to NORM DC Using VERTICAL POS, adjust channel D. Adjust so base line of channel D pulses are coincident. The start of the negative pulse of trace 4 should appear in CENTER of 4th pulse of trace C. Repeat step 200 until this agrees	2.4 usec	
215	SCOPE	Turn 5X MULTIPLIER OFF		
220	02B8	Connect scope input 1 to B07G		
230	02B8	Connect scope input 3 to B15Q		
240	IE	Turn PHASE to B		
250	IE	Turn BIT GATE to 8		
260	SCOPE	Repeat step 190. The pulse on trace 2 should be aligned with SECOND pulse from LEFT on trace 1. Data pattern will be different from step 190.		
270	02B8	Adjust DL2 for separation of pulses described in steps 200 and 210 agrees		
280	02B8	Connect scope input 1 to B06G		
290	IE	Turn PHASE to A		
300	IE	Turn BIT GATE to 12		
310	SCOPE	Repeat step 190. The pulse on trace 2 should be aligned with the pulse on trace 1. Different data pattern than for previous delay lines.		
320	02B8	Adjust DL1 for separation of pulses described in steps 200 and 210 agrees		

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Figure 7-24. Delay Lines 1, 2, and 3 Adjustments (Sheet 3)

INTERNATIONAL BUSINESS MACHINES—

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	NORMAL INDICATION	DATA
330	SCOPE	Remove scope probes and close gate 02B8		
340	MLDD	Press and release COMPUTER CONTROL ON		
		ON, CST, and ADVANCE indicator lamps	ON	
350	MLDD	Press and release PAST/PRESENT		
		PAST indicator lamp	ON	
360	MLDD	Switch DISPLAY SELECT to TRS		
370	MLDD	Switch WORD to T-1		
380	MLDD	DATA COMPUTER lamps 7, 9, 10, 11, 21, 23, 24, 25 only	ON	
390	MLDD	OP1 COMPUTER lamp	OFF	
		OP2, OP3 and OP4 lamps	ON	
400	MLDD	A5, A3, A2, A1 COMPUTER lamps	ON	
		A8, A7, A6 and A4 lamps	OFF	
410	MLDD	Display select to AI3 Data		
420	MLDD	Computer Data 7, 9, 10, 11, 21, 23, 24, and 25 lamps	ON	
430	MLDD	Display select to MD7		
440	MLDD	Computer Data Bit 24 lamp	ON	
450	MLDD	Display select to MR1		
460	MLDD	Computer Data Bit 19 lamp	ON	
470	MLDD	Display select to PRO		
480	MLDD	Computer Data Bits 18, 19 and 20	ON	

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Figure 7-24. Delay Lines 1, 2, and 3 Adjustments (Sheet 4)

INTERNATIONAL BUSINESS MACHINES-

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
10	TRMC	If neither INV ERR or ADR 6 lamps are ON, delete steps 20 through 60		
20	TRMC	Press and release ADR 1	ON	
21	TRMC	ADR 1 lamp		
25	TRMC	Press and release ADR 2		
26	TRMC	ADR 2 and ADR 6 lamps	ON	
30	TRMC	Press and release ADR 3		
31	TRMC	ADR 3 lamp	ON	
35	TRMC	INV ERR lamp	OFF	
40	TRMC	Press and release ADR 1		
41	TRMC	ADR 1 lamp	OFF	
45	TRMC	Press and release ADR 2		
50	TRMC	ADR 2 and ADR 6 lamps	OFF	
55	TRMC	Press and release ADR 3		
60	TRMC	ADR 3 lamp	OFF	
70	IE	Press and release ERROR RESET		
90	TRMC	Press and release ML/DD		
100	TRMC	ML lamp	OFF	
110	TRMC	DD lamp	ON	
120	IE	COMPTR HALT lamp	OFF	
130	IE	Press and release COMPTR HALT/ MANUAL HALT		
140	IE	MANUAL HALT and COMPTR HALT lamps	ON	
NOTE		TP 30 will be at 20 VDC level when COMPTR HALT and MANUAL HALT lamps are OFF.		
150	PC	Connect Sync probe of Oscilloscope to TP 30		
160	SCOPE	Adjust Sync controls to Sync EXT + Horiz. Swp 2MS/CM		
170	TRMC	Connect Oscilloscope probe to monitor TP29 (A1-3HALTV)		
180	IE	While monitoring the oscilloscope, press and release COMPTR HALT		
190	SCOPE	Verify (A1-3HALTV) starts at +6 VDC and drops to 0VDC 9 ms after start of sweep	8 to 10 ms	
200		If A1-3 HALTV dropr to 0VDC within 8 to 10 ms omit steps 210 through 270		
205	IE	MANUAL HALT and COMPTR HALT lamps	OFF	

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Figure 7-25. Halt Adjustments (Sheet 1 of 2)

INTERNATIONAL BUSINESS MACHINES–

UNIT NAME: LVDC MANUAL EXERCISER | UNIT NO.

STEP	PANEL	OPERATION	TOLERANCE	DATA
210	TRMC	Press and release FREE RUN SS		
220	TRMC	FREE RUN SS lamp	ON	
230	01B3	Open gate 01B3		
240	01B3	Adjust potentiometer at 01B3 A15 while observing scope trace. Set 50% point of trailing edge of A1-3HALTV 9 ms from start of sweep	8 to 10 ms	
250	01B3	Close gate 01B3		
260	TRMC	Press and release FREE RUN SS		
270	TRMS	FREE RUN SS LAMP	OFF	
280	TRMC	Press and release MEMORY SIM		
290	TRMC	MEMORY SIM lamp	ON	
300	01B7	Open gate 01B7		
310	PC and TRMC	Remove scope probes from TP 29 (TRMC) and TP30 (PC)		
320	01B7	Connect Sync probe to 01B7 C14P		
330	01B7	Connect oscilloscope probe to monitor 01B7 C14B		
333	MLDD	Press and release AUTO/MAN/PTC		
335	MLDD	AUTO lamp	ON	
337	MLDD	MAN/PTC lamp	OFF	
338	MLDD	Turn DISPLAY SELECT to TRS		
340	SCOPE	Adjust Sync controls to Sync EXT-		
350	01B7	Adjust the potentiometer at 01B7 C14 for 3 ms between the 50% point of the leading (negative) edge and the 50% point of the trailing edge (positive) of the pulse	2.5 to 3.5 ms	
360	01B7	Disconnect scope probes from 01B7 C14 B		
370	01B7	Close gate 01B7		
380	TRMC	Press and release MEMORY SIM		
390	TRMC	MEMORY SIM lamp	OFF	
400	TRMC	Press and release ML/DD		
410	TRMC	ML lamp	ON	
420	TRMC	DD lamp	OFF	
430	MLDD	Press and release AUTO/MAN/PTC		
440	MLDD	MAN/PTC lamp	ON	
450	MLDD	AUTO lamp	OFF	
460	MLDD	Turn DISPLAY SELECT to NONE		

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Figure 7-25. Halt Adjustments (Sheet 2)

Tape Word	Word Count
0000000000000C0140	00000
000C000000000C0177	00000
0000000000000C0147	00001
C000000400000C0204	00002
0000000000000C0140	00003
4000000000000C0140	00004
2000000000000C0140	00005
1000000000000C0140	00006
0400000000000C0140	00007
0200000000000C0140	00010
0100000000000C0140	00011
0040000000000C0140	00012
0001000000000C0140	00013
0000400000000C0140	00014
0000200000000C0140	00015
0000100000000C0140	00016
0000040000000C0140	00017
0000020000000C0140	00020
0000010000000C0140	00021
0000004000000C0140	00022
0000002000000C0140	00023
0000001000000C0140	00024
0000050000000C0140	00025
0020000000000C0161	00026
0010000000000C0162	00027
0004000000000C0140	00030
0002000000000C0170	00031
0000000400000C0100	00032
0000000200000C0100	00033
0000000100000C0100	00034
0000000040000C0100	00035
0000000020000C0100	00036
0000000010000C0100	00037
0000000004000C0100	00040
0000000002000C0100	00041
0000000001000C0100	00042
0000000000400C0100	00043
0000000000200C0100	00044
0000000000100C0100	00045
0000000000040C0100	00046
0000000000020C0040	00047
0000000000010C0040	00050
0000000000004C0040	00051
0000000000002C0040	00052
0000000000001C0040	00053
0000000000000C0040	00054
0000000000000C0040	00055
0000000000000C0040	00056
0000000000000C0040	00057
0000000000000C0040	00060
0000000000000C0040	00061
000C000000000C0440	00062
C000000000000C0240	00063
4000000000000C0240	00064
4000400000000C0140	00065
4000000000000C0140	00066
C000000000000C0140	00067
C000000000000C0240	00070
4000000000000C0240	00071
C000000000000C0150	00072
0000000400000C0140	00073
0000000000000C0146	00074

Figure 7-26. Self-Check Tape Listing (Sheet 1 of 27)

Tape Word	Word Count	Tape Word	Word Count
0000000000000C100	00075	000000300000000172	00144
0000000000000146	00076	C00000777777777632	00145
C00C000000200C140	00077	000000044000000160	00146
000C000000000C146	00100	000000700000000172	00147
C000000000000C0040	00101	000C00300000000172	00150
C0C0000000000000146	00102	C0C0000477777777632	00151
0000000000000000143	00103	000000700000000172	00152
4000000000000000145	00104	00C050077777777600	00153
0000000000000C0146	00105	C000000000000C0172	00154
0000000000000CC145	00106	000050000000000140	00155
0000000000000000146	00107	000003777777777632	00156
000C000000000C0147	00110	000000700000000172	00157
0000000000000000144	00111	C000000044000000160	00160
0000000000000C0172	00112	C00C003777777777632	00161
0000000000000C0142	00113	C0C0007777777777632	00162
C000777000000000140	00114	000020000000C000172	00163
0000000000000C00142	00115	000000300000C000172	00164
000077600000000172	00116	00C000020020000160	00165
C000000400007761O2	00117	000000777777777632	00166
000000100000000172	00120	C000003777777777632	00167
C0000000000001042	00121	000000000000000172	00170
000C000000000C0C172	00122	00C000044000000160	00171
C000000000000000142	00123	00C050077777777600	00172
000000077777777600	00124	000000000000C000172	00173
C000000000000000150	00125	000050000000000140	00174
000C000000000CC0242	00126	C000000200200000160	00175
C0000000000000000146	00127	C000003C000000C0172	00176
0000400000000C0172	00130	C00C007000000000172	00177
000C000000000000142	00131	C000500777777777600	00200
000000000000C00146	00132	000000000000000172	00201
0000000000000000147	00133	C000000440000C0160	00202
C000500777777777600	00134	C0C050000000000140	00203
0000000000000000172	00135	000000000000C00C172	00204
000050000000000140	00136	000000040020000160	00205
C000000440000000160	00137	C00C003000000000172	00206
C000003777777777632	00140	C00C50077777777600	00207
000000777777777632	00141	000001300000000172	00210
000001377777777632	00142	C000003000000C0C172	00211
0000000000000C0172	00143		

Figure 7-26. Self-Check Tape Listing (Sheet 2)

Tape Word	Word Count	Tape Word	Word Count
0000500000000C00140	00212	C0000030000C000272	00261
0000000000000000172	00213	00C0000000000000146	00262
C0000004400000C160	00214	CC00007000000000272	00263
0000500777777777600	00215	0000000000000000146	00264
0000000000000000172	00216	0000003400000C00132	00265
0000000400200000160	00217	0000000000000000146	00266
0000007000000000172	00220	0000007400000000132	00267
0000000440000000160	00221	0000000000000000146	00270
0000000002000000120	00222	0000500000000000240	00271
0000007000000C00172	00223	0000000000000000172	00272
0000000440000000160	00224	0000003000000000172	00273
0000000001000000120	00225	0000000000000C00146	00274
0000007000000000172	00226	C000000000000000147	00275
0000003000000000140	00227	0000500000000000140	00276
0000001000000C00172	00230	70045007000000C100	00277
0000002000000000172	00231	0000000000000000172	00300
0000000002000000120	00232	0000003000000C00172	00301
0000000200200000160	00233	0001600000000C00140	00302
0000000200000000120	00234	0000000000000000172	00303
0000003000000000172	00235	0000003400000010032	00304
0000500525252500	00236	0000600000000000140	00305
0000200000000C00172	00237	C000600700000C00100	00306
0000003525252532	00240	0000000000000000172	00307
0000000440000000160	00241	0000003400000000132	00310
0000003525252532	00242	0000500000000000140	00311
0000007525252532	00243	0000000000000C00172	00312
0000000002000C00120	00244	0000000000000C00157	00313
0000000200200000160	00245	0012000000000700040	00314
0000000201000000160	00246	0022000000000700040	00315
0000003000000C00172	00247	0024000700000000125	00316
0000000000000000172	00250	0006000700000C00134	00317
0000000440000000160	00251	0014000700000C00126	00320
0000500000000C00140	00252	0000500000000017140	00321
00C0000000000000172	00253	0030000000000000140	00322
0000000201000000160	00254	00C2000000000C00170	00323
0000003000025252?2	00255	0000500000000000140	00324
0000000002000000120	00256	0012377000000000140	00325
0000000200200000160	00257	C012400000000C00140	00326
0000000000CCCC0150	00260		

Figure 7-26. Self-Check Tape Listing (Sheet 3)

Tape Word	Word Count	Tape Word	Word Count
C000000000000000150	00327	0000000000000000146	00376
0012776000000000157	00330	0012100000000000150	00377
0000000000000C00146	00331	0000000000000000C146	00400
0000500000000C00140	00332	C012200000000000150	00401
0012775000000000157	00333	0000000000000000146	00402
0000000000000000146	00334	0012400000000C00150	00403
0000500000000C000140	00335	0000000000000000146	00404
0012773000000000157	00336	0002000000000000171	00405
0000000000000000146	00337	0000000000000000146	00406
0000500000000C00140	00340	0002000000000000172	00407
0012767000000000157	00341	0000000000000000146	00410
0000000000000000146	00342	0002000000000000174	00411
0000500000000000140	00343	0000000000000000146	00412
0012757000000C00157	00344	0006000000000000170	00413
00C0000000000000146	00345	0000000000000000146	00414
0000500000000000140	00346	0002000000000000160	00415
0012737000000000157	00347	0000000000000C000146	00416
0000000000000000146	00350	0030000000000000173	00417
0000500000000000140	00351	0000000000000000146	00420
0012677000000000157	00352	0030000000000000161	00421
0000000000000000146	00353	C000000000000000146	00422
0000500000000000140	00354	0030000000000000162	00423
0012577000000000157	00355	0000000000000000146	00424
0000000000000C00146	00356	0000000000000000147	00425
0000500000000000140	00357	0000000200000200020	00426
0012377000000000157	00360	0000003000000000172	00427
0000000000000000146	00361	0000125200000200020	00430
0000500000000C00140	00362	0000003000252C0172	00431
0012001000000000150	00363	0000400200000200020	00432
0000000000000000146	00364	0000003000001000172	00433
0012002000000000150	00365	0000252200000200020	00434
0000000000000000146	00366	0000003000524000172	00435
0012004000000C000150	00367	0000000000000000150	00436
0C00000000000C00146	00370	0030000200000200020	00437
0012010000000000150	00371	0000000000000000146	00440
0000C000000000000146	00372	C000000000000000147	00441
0012020000000000150	00373	0C00C030000000000172	00442
C0C0000000000C000146	00374	0000000000000000C150	00443
C012040000000000150	00375		

Figure 7-26. Self-Check Tape Listing (Sheet 4)

Tape Word	Word Count	Tape Word	Word Count
0006000200002C0020	00444	0000000C0000000146	00513
0000000000000000146	00445	0000500000000C0140	00514
0000000000000000147	00446	C0227370000000C157	00515
0000003000000000172	00447	0000000000000000146	00516
0000001200000000120	00450	0000500000000C0140	00517
0000003000000C000172	00451	C0226770000000C157	00520
0012200000000000140	00452	0000000000000C0C146	00521
0000000000000000150	00453	0000500000000000140	00522
0020000000000C000160	00454	0022577000000C0C157	00523
0000000000000000146	00455	0000000000000000146	00524
0012000000000000176	00456	0000500000000000140	00525
0000000000000000146	00457	0022377000000000157	00526
0012577000000000157	00460	0000000000000000146	00527
0000000000000000146	00461	0000500000000000140	00530
0000000000000000147	00462	0022001000000000150	00531
0000500000000000140	00463	0000000000000000146	00532
0000001000000000172	00464	0022002000000000150	00533
0000000220000000160	00465	0000000000000000146	00534
0000003000100000232	00466	0022004000000000150	00535
0000000200000000120	00467	0000000000000000146	00536
0000003000000000172	00470	0022010000000000150	00537
0000000000000000172	00471	0000000000000000146	00540
0026000000000000140	00472	0022020000000000150	00541
0022777000000000157	00473	0000000000000000146	00542
0000000000000000150	00474	0022040000000000150	00543
0000500000000000140	00475	0000000000000000146	00544
0022776000000000157	00476	0022100000000000150	00545
0000000000000000146	00477	0000000000000000146	00546
0000500000000000140	00500	0022200000000000150	00547
0022775000000000157	00501	0000000000000000146	00550
0000000000000000146	00502	0022400000000000150	00551
0000500000000000140	00503	0000000000000000146	00552
0022773000000000157	00504	0010000000000000166	00553
0000000000000000146	00505	0000000000000000146	00554
0000500000000000140	00506	0014000000000000162	00555
0022767000000000157	00507	0000000000000000146	00556
0000000000000000146	00510	0010000000000000160	00557
0000500000000000140	00511	0000000000000000146	00560
0022757000000000157	00512		

Figure 7-26. Self-Check Tape Listing (Sheet 5)

Tape Word	Word Count	Tape Word	Word Count
0010000000000163	00561	0004040000000C150	00630
00C0000000000146	00562	0000000000000C146	00631
0010000000000172	00563	0004100C000000150	00632
0000000000000146	00564	C00C0000000000146	00633
0022000000000173	00565	0004200000000150	00634
0000000000000146	00566	0C00000000000C146	00635
0022000000000161	00567	0000000000000147	00636
0000000000000146	00570	0000500022000C340	00637
0022000000000170	00571	2130000022000C340	00640
0000000000000146	00572	0000500000020C040	00641
0000000000000147	00573	0030000000000C140	00642
0004377000000C00140	00574	0000500040400C140	00643
0000000000000C0150	00575	0630440101000C140	00644
0004776000000C0157	00576	0000000000000C150	00645
0000000000000146	00577	0000500000000C0140	00646
0004775000000C00157	00600	0031500000400C100	00647
0000000000000C0146	00601	000C00000000000146	00650
0004773000000C00157	00602	0000000000000C172	00651
0000000000000C146	00603	0000003000400C0132	00652
0004767000000000157	00604	00C0000000000000146	00653
0000000000000000146	00605	0000500010000C00100	00654
0004757000000C000157	00606	C0300000100000C100	00655
0000000000000C0146	00607	0000000000000000146	00656
C0047370000000C0157	00610	4030000000000C140	00657
0000000000000000146	00611	0000000000000000146	00660
0004677000000000157	00612	0000500000000C0140	00661
00C0000000000C0146	00613	0030500010000C0C200	00662
0004577000000000157	00614	00C0000000000C0146	00663
0000000000000000146	00615	0000C000000000C172	00664
0004001000000000150	00616	0000003000000000172	00665
0000000000000000146	00617	0000000000000000146	00666
0004002000000000150	00620	4034000000000000140	00667
0000000000000C0146	00621	00C0000000000C0C146	00670
0004004000000C00150	00622	C0000030000000C0172	00671
0000000000000000146	00623	C0000000000000C146	00672
00C4010000000C0C150	00624	C0000000000000C0147	00673
0000000000000C0146	00625	0000500000000000140	00674
0004020000000C0C150	00626	0000000C0000000172	00675
0000000000000C0146	00627		

Figure 7-26. Self-Check Tape Listing (Sheet 6)

Tape Word	Word Count	Tape Word	Word Count
0000500440000000140	00676	0012440000000000140	00745
0000000200002000020	00677	0000000000000000146	00746
0000003000000002372	00700	0012440000000000140	00747
0000500000000000240	00701	0000000000000000146	00750
0000000200004000020	00702	0012440000000000140	00751
0000003000100000132	00703	0000000000000000146	00752
0000000200000000120	00704	0012000000000000140	00753
0000003000000000172	00705	0000000000000000146	00754
0000400200006000060	00706	0012440000000000140	00755
0000003000101000032	00707	0000000000000000146	00756
0000500000000000140	00710	0012440000000000140	00757
0000000000000000172	00711	0000000000000000146	00760
0000500777400376400	00712	0012440000000000140	00761
7753000777400376400	00713	0000000000000000146	00762
0000500000000000240	00714	0000000000000000147	00763
0000000000000000150	00715	0000500777400376400	00764
0012000000000000140	00716	7763000777400376400	00765
0000000000000000146	00717	0000000000000000150	00766
0012440000000000140	00720	0000500000000000240	00767
0000000000000000146	00721	0112000002000002000	00770
0012440000000000140	00722	0000000000000000146	00771
0000000000000000146	00723	0122000002000002000	00772
0012440000000000140	00724	0000000000000000146	00773
0000000000000000146	00725	0052440004000004000	00774
0012440000000000140	00726	0000000000000000146	00775
0000000000000000146	00727	0062000004000004000	00776
0012440000000000140	00730	0000000000000000146	00777
0000000000000000146	00731	4012440010000001000	01000
0012440000000000140	00732	0000000000000000146	01001
0000000000000000146	00733	4022000010000001000	01002
0000500000400000100	00734	0000000000000000146	01003
0012000000000000140	00735	2012440020000002000	01004
0000000000000000146	00736	0000000000000000146	01005
0012440000000000140	00737	2022000020000002000	01006
0000000000000000146	00740	0000000000000000146	01007
0012440000000000140	00741	1012440040000004000	01010
0000000000000000146	00742	0000000000000000146	01011
0012440000000000140	00743	1022000040000004000	01012
0000000000000000146	00744		

Figure 7-26. Self-Check Tape Listing (Sheet 7)

Tape Word	Word Count	Tape Word	Word Count
000C000000000000146	01013	2022000020000002000	01062
C41244010000010000	01014	0000000000000000146	01063
C0000000000000C146	01015	101244004000004000	01064
C42200010000010000	01016	C0000000000000000146	01065
0000C00000000000146	01017	102200004000004000	01066
0000500200400000140	01020	0000000000000000146	01067
0013000200400200040	01021	041244010000010000	01070
0000000000000000146	01022	0000000000000000146	01071
0023000200400200040	01023	C42200010000010000	01072
0000000000000000146	01024	C0000000000000000146	01073
0000500200000200000	01025	021244040010000140	01074
0013000200400200400	01026	0000000000000000146	01075
C0000000000000C146	01027	022244040100000140	01076
0023000200400200040	01030	0000000000000000146	01077
C0C0000000000000146	01031	021200040100C00140	01100
0000500000400200000	01032	0000000000000000146	01101
0013000200400200040	01033	0000500000000000240	01102
0000000000000000146	01034	0022000000000C00140	01103
0023000200400200040	01035	0000000000000C00146	01104
0000000000000C00146	01036	0022440000000000140	01105
0000500001000001000	01037	0000000000000000146	01106
021200040100000140	01040	0022440000000000140	01107
C0000000000000C146	01041	0000000000000000146	01110
022200040100C00140	01042	0022440000000000140	01111
0000000000000000146	01043	000C000000000000146	01112
011244000200C0C200	01044	0022440000000000140	01113
0000000000000000146	01045	0000000000000000146	01114
012200000200000200	01046	0022440000000000140	01115
0000000000000000146	01047	0000000000000000146	01116
0052440004000004000	01050	0022440000000000140	01117
0000000000000000146	01051	0000000000000C00146	01120
0062000004000004000	01052	0000500000400C00100	01121
0000000000000000146	01053	0022000000000000140	01122
401244001000001000	01054	0000000000000000146	01123
0000000000000000146	01055	0022440000000000140	01124
402200001000001000	01056	0000000000000000146	01125
0000000000000000146	01057	0022440000000000140	01126
201244002000002000	01060	0000000000000000146	01127
0000000000000000146	01061		

Figure 7-26. Self-Check Tape Listing (Sheet 8)

Tape Word	Word Count
0022440000000C00140	01130
0000000000000000146	01131
0022440000000000140	01132
0000000000000000146	01133
0022440000000000140	01134
0000000000000000146	01135
0022440000000000140	01136
0000000000000000146	01137
0022440000000000140	01140
0000000000000000146	01141
0022440000000000140	01142
0000000000000C00146	01143
0022440000000000140	01144
0000000000000000146	01145
0000500401000000140	01146
0212000000000000140	01147
0000000000000000146	01150
0222000000000000140	01151
0000000000000000146	01152
0212000000000000140	01153
0000000000000000146	01154
0212000401000000240	01155
0000000000000C00146	01156
0222000401000000240	01157
0000000000000000146	01160
0000500000000000140	01161
0000000000000C00147	01162
0004000000000000140	01163
0000003000000000172	01164
0000500000000000240	01165
0004000000000000140	01166
0000003000000000272	01167
0000500000000C000140	01170
0000003000000000272	01171
0000500400000000100	01172
0004000000000000140	01173
0000003400000000132	01174
0004600000000000176	01175
0000003012000000172	01176

Tape Word	Word Count
0004600000000000140	01177
0000003500000000172	01200
0004600000000000175	01201
0000003500000000172	01202
0004600000000000174	01203
0000003500000000172	01204
0004600000000000172	01205
0000003500000000172	01206
0004600000000000166	01207
0000003500000000172	01210
0000500500000000140	01211
0004400000000000176	01212
0000003500000000172	01213
0004200000000000176	01214
0000003500000000172	01215
0000000200020000020	01216
0000003000000000172	01217
0000000200040000160	01220
0000003000000000172	01221
0000500000000000140	01222
0026600720000000140	01223
0000000200000000120	01224
0000000000000000150	01225
0000500000000000140	01226
0026600700000000100	01227
0000000000000000146	01230
0000003720000000172	01231
0000000000000000146	01232
0000500000000000140	01233
0026900730000000100	01234
0000000000000000146	01235
0000003730000000132	01236
0000000000000000146	01237
0000500000000000140	01240
0026610720000000140	01241
0000000000000000146	01242
0000000000000000147	01243
0000003720000000172	01244

Figure 7-26. Self-Check Tape Listing (Sheet 9)

Tape Word	Word Count	Tape Word	Word Count
0000000200000000120	01245	0000003000000000172	01314
0000500000000000140	01246	0000C000000000150	01315
0000000000000000150	01247	0000500001000001000	01316
0026700720000000140	01250	0234000001000001000	01317
0000000000000000146	01251	0000000000000000146	01320
0000000200000000120	01252	0000000200040000160	01321
0000500000000000140	01253	0000000000000000147	01322
0026600000000000140	01254	0000003000020000072	01323
0000000000000000146	01255	0000500000000000140	01324
0000000200020000020	01256	0016600017000000140	01325
0000000000000000147	01257	0000000000000000150	01326
0000003000000001672	01260	0000500000000000140	01327
0000000000000000150	01261	0016600000000000140	01330
0000500000000000140	01262	0000000000000000146	01331
0026600000000000140	01263	0000500000000000140	01332
0000000000000000146	01264	0016600037000000040	01333
0000000200040000160	01265	0000000000000000146	01334
0000000000000000147	01266	0000000000000000147	01335
0000003016400000172	01267	0000600000000000140	01336
0000000000000000150	01270	0000000200004000020	01337
0000500000000000140	01271	0000003000000010072	01340
0026600000000000140	01272	0000500000000000140	01341
0000000000000000146	01273	0000000000000000172	01342
0000000200000000120	01274	0000000400000000233	01343
0000000000000000147	01275	0000000400000000133	01344
0000003000000000172	01276	0200000000000000240	01345
0000000000000000150	01277	0000000000000000277	01346
0000500001000001000	01300	0000000000000000263	01347
0034000000000000140	01301	0000000000000000271	01350
0000000000000000146	01302	0000000000000000272	01351
0000000200040000160	01303	0001000400000000204	01352
0000000000000000147	01304	4000000400000000104	01353
0000003000000000172	01305	2000000000000000244	01354
0000000000000000150	01306	1200000400000000104	01355
0000500000000000140	01307	0600000000000000244	01356
0026700720000000140	01310	7401000400000000200	01357
0000000000000000146	01311	6000000000000000144	01360
0000000200040000160	01312	1600000000000000144	01361
0000000000000000147	01313		

Figure 7-26. Self-Check Tape Listing (Sheet 10)

Tape Word	Word Count	Tape Word	Word Count
0001000400000000233	01362	C000010000000000143	01431
0001000000000000240	01363	C000000000000000146	01432
C001000000000000273	01364	0000004000000000143	01433
0001000400000000100	01365	0000000000000000146	01434
C001000400000000133	01366	C000002000000000143	01435
0000000000000000150	01367	0000000000000000146	01436
1401000400000000204	01370	0000001000000000143	01437
0000000000000000146	01371	C000300000000000146	01440
6201000400000000204	01372	4000030000000000143	01441
0000000000000000146	01373	0000000000000000146	01442
3400000000000000144	01374	2000000000000000143	01443
0000000000000000146	01375	C000000000000000146	01444
5400000000000000144	01376	1000000000000000143	01445
0000000000000000146	01377	0000000000000000146	01446
4000000400000000204	01400	0400000000000000143	01447
0000000000000000146	01401	0000000000000000146	01450
2000000400000000204	01402	0000400000000000143	01451
0000000000000000146	01403	C000000000000000146	01452
6600000000000000144	01404	0000200000000000143	01453
0000000000000000146	01405	0000000000000000146	01454
7200000000000000144	01406	0000100000000000143	01455
0000000000000000146	01407	0000000000000000146	01456
1200000400000000204	01410	0000040000000000143	01457
0000000000000000146	01411	0000000000000000146	01460
0600000400000000204	01412	C000000000000100060	01461
0000000000000000146	01413	0000000000000000140	01462
0000000000000000244	01414	0000000000000000140	01463
0000000000000000146	01415	0000000000000000140	01464
0000000000400000120	01416	0000000000000000140	01465
0000000000000000140	01417	0000000000000000147	01466
0000000000000000140	01420	0000020000000000143	01467
0000000000000000140	01421	0000000000000000150	01470
0000000000000000140	01422	C000000000400000120	01471
C000000000000000147	01423	0000000000000000140	01472
0000000000000000143	01424	0000000000000000140	01473
0000000000000000143	01425	0000000000000000140	01474
0000000000000000150	01426	0000000000000000140	01475
0000020000000000143	01427	0000000000000000146	01476
0000000000000000146	01430		

Figure 7-26. Self-Check Tape Listing (Sheet 11)

Tape Word	Word Count	Tape Word	Word Count
000050006140000140	01477	700000077777777614	01546
000000000000CC172	01500	C000000000000CC0146	01547
000000044000000160	01501	70C0003077401770l0	01550
000050006140143140	01502	C000C000000000C146	01551
000000000000000147	01503	700000477777777615	01552
700000430600143150	01504	000C000000000C00146	01553
000050077777777600	01505	7000C03061401770S0	01554
000000000000000172	01506	C000C000000000C0146	01555
000000044000000160	01507	700000077777777612	01556
000050037740143100	01510	000000000000C000146	01557
700020077777777613	01511	70C0003077401770l0	01560
000000000000000146	01512	C000000000000000146	01561
700000337740143110	01513	700000477777777616	01562
000000000000000146	01514	0000000000000000146	01563
700020077777777614	01515	70CC003061401770S0	01564
000000000000000146	01516	C000000000000C00146	01565
700000337740177010	01517	700000077777777611	01566
000000000000000146	01520	C000000000000000146	01567
700020077777777615	01521	70CC003077401770l0	01570
000000000000000146	01522	C000000000000CC0146	01571
700000337740143110	01523	C000S0077777777600	01572
000000000000C00146	01524	70C050430600177053	01573
700020077777777612	01525	CCC000000000000C146	01574
000000000000000146	01526	70CC000000000CC0150	01575
700000337740177010	01527	700C003306001770S0	01576
000000000000000146	01530	000000000000000C146	01577
700020077777777616	01531	C00C50077777777600	01600
000000000000000146	01532	70C050430600177054	01601
700000337740143110	01533	00CC000000000C0146	01602
000000000000000C146	01534	700C00000000000C150	01603
7000200777777777611	01535	700000337600177010	01604
000000000000000C146	01536	0000000000000000146	01605
700000337740177010	01537	000050077777777600	01606
000000000000000146	01540	700050430600177055	01607
000050006140177040	01541	C0C000000000000C146	01610
700000077777777613	01542	70CCC00000000000150	01611
000000000000000C146	01543	70C0003306001770S0	01612
700000306140177050	01544	C000000000000C00146	01613
C000000000000000146	01545		

Figure 7-26. Self-Check Tape Listing (Sheet 12)

Tape Word	Word Count	Tape Word	Word Count
0000500777777777600	01614	7000500777777777610	01663
7000504306001770 52	01615	7000000777777777611	01664
0060000000000000146	01616	0000000000000000146	01665
7000000000000000150	01617	0000500061400000140	01666
7000003376001770 10	01620	7000500777777777610	01667
0000000000000000146	01621	0000000440000000160	01670
0000500777777777600	01622	0000000000000000172	01671
7000504306001770 56	01623	7000000777777777613	01672
0000000000000000146	01624	0000000000000000146	01673
7000000000000000150	01625	7000000777777777614	01674
7000003306001770 50	01626	0000000000000000146	01675
0000000000000000146	01627	7000000777777777615	01676
0000500777777777600	01630	0000000000000000146	01677
7000504306001770 51	01631	7000000777777777612	01700
0000000000000000146	01632	0000000000000000146	01701
7000000000000000150	01633	7000000777777777616	01702
7000003376001770 10	01634	0000000000000000146	01703
0000000000000000146	01635	7000000777777777611	01704
0000500061400000140	01636	0000000000000000146	01705
7000500777777777610	01637	0000500000000000140	01706
7000000777777777613	01640	7000500777777777510	01707
0000000000000000146	01641	0000000440000000160	01710
0000500061400000140	01642	4000000000000000150	01711
7000500777777777610	01643	0000000000000000146	01712
7000000777777777614	01644	7000003377777777550	01713
0000000000000000146	01645	0000000000000000146	01714
0000500061400000140	01646	2000000000000000150	01715
7000500777777777610	01647	0000000000000000146	01716
7000000777777777615	01650	7000003377777777550	01717
0000000000000000146	01651	0000000000000000146	01720
0000500061400000140	01652	1000000000000000150	01721
7000500777777777610	01653	0000000000000000146	01722
7000000777777777612	01654	7000003377777777550	01723
0000000000000000146	01655	0000000000000000146	01724
0000500061400000140	01656	3000000000000000150	01725
7000500777777777610	01657	0000000000000000146	01726
7000000777777777616	01660	7000003000000000150	01727
0000000000000000146	01661	0000000000000000146	01730
0000500061400000140	01662		

Figure 7-26. Self-Check Tape Listing (Sheet 13)

Tape Word	Word Count	Tape Word	Word Count
0000000200000000120	01731	0000000440000000160	02000
5000000000000000150	01732	7000500306001770 57	02001
0000000000000000146	01733	0000000000000000172	02002
7000003000000000150	01734	0000000000000000144	02003
0000000000000000146	01735	0000003376001770 32	02004
0000000200000000120	01736	0000000000000000143	02005
6000000000000000150	01737	0000000240000000160	02006
0000000000000000146	01740	0000500400000000100	02007
7000003000000000150	01741	0000000000000000173	02010
0000000000000000146	01742	0000000000000000144	02011
0000000440000000160	01743	0000003000000000172	02012
7000004377401431 13	01744	0000000000000000143	02013
0000000000000000146	01745	0000000000000000170	02014
7000004377401431 14	01746	0000000000000000144	02015
0000000000000000146	01747	0000003000000000172	02016
7000004377401431 15	01750	0000000000000000143	02017
0000000000000000146	01751	0000000000000000176	02020
7000004377401431 12	01752	0000000000000000144	02021
0000000000000000146	01753	0000003000000000172	02022
7000004377401431 16	01754	0000000000000000143	02023
0000000000000000146	01755	0000000000000000162	02024
7000004377401431 11	01756	0000000000000000144	02025
0000000000000000146	01757	0000003000000000172	02026
0000000000000000147	01760	0000000000000000143	02027
0000000000000000144	01761	0000010000000000142	02030
0000500777777777600	01762	0000010000000000147	02031
0000000000000000172	01763	0000500777777777600	02032
0000000440000000160	01764	0000000000000000172	02033
0000000000000000143	01765	0000000440000000160	02034
7000000776001770 57	01766	7000004777777776 13	02035
7000000776001770 57	01767	0000010000000000163	02036
0000500000000000140	01770	0000000000000000144	02037
0000000240000000160	01771	0000010000000000143	02040
0000000000000000150	01772	0000000000000000144	02041
0000000000000000147	01773	0000000000000000145	02042
0000000000000000147	01774	0000000000000000146	02043
0000000000000000143	01775	0000777000000000154	02044
0000500777777777600	01776	0000000000000000164	02045
0000000000000000172	01777		

Figure 7-26. Self-Check Tape Listing (Sheet 14)

Tape Word	Word Count	Tape Word	Word Count
0000000000000000143	02046	0212000401000000140	02115
0000000000000000144	02047	0000003000000000172	02116
0000000400000000204	02050	0000500000000000140	02117
0000000000000000150	02051	0022000000000000146	02120
0000600400000000114	02052	0030777000000000154	02121
0000000000000000146	02053	0000500000000000140	02122
0000000000000000147	02054	0012000000000000147	02123
0000000000000000172	02055	0000000000000000143	02124
0000003400000000132	02056	0000600000000000160	02125
0000000000000000150	02057	0000000000000000144	02126
0000500000000000140	02060	0000000000000000150	02127
0000600000000000154	02061	7030000000000000140	02130
0000000000000000146	02062	0000000000000000145	02131
0000000000000000147	02063	0000000000000000146	02132
0000000000000000172	02064	7030000000000000140	02133
0000003400000000132	02065	0000000000000000143	02134
0000000000000000150	02066	0000000000000000146	02135
0000000000000000147	02067	7030000000000000140	02136
0000000000000000147	02070	0000000000000000157	02137
0000000000000000143	02071	0000000000000000146	02140
0000500000000000140	02072	7030000000000000140	02141
0030001000000000150	02073	0000000000000000167	02142
0000000000000000147	02074	0000000000000000146	02143
0000000000000000144	02075	0000000000000000147	02144
0030777000000000151	02076	0000000000000000144	02145
0000500000000000140	02077	0000000000000000145	02146
0030777000000000152	02100	0000001000000000160	02147
0000500000000000140	02101	0000000000000000146	02150
0030777000000000154	02102	0000001000000000160	02151
0000500000000000140	02103	0000000000000000140	02152
0030001000000000140	02104	0000001000000000160	02153
0002011000000000170	02105	0000777000000000154	02154
0000007000000000160	02106	0000001000000000160	02155
0000000000000000143	02107	0000000000000000164	02156
0000007000000000160	02110	0000001000000000160	02157
0000000000000000144	02111	0000001000000000143	02160
0000500000000000140	02112	0000000000000000172	02161
0000000000000000172	02113	0000000000000000142	02162
0000500401000000140	02114		

Figure 7-26. Self-Check Tape Listing (Sheet 15)

Tape Word	Word Count	Tape Word	Word Count
0000001000000000142	02163	0000000000000000146	02232
0000000000000000147	02164	0000003000000000175	02233
0000001000000000142	02165	0000000000000000146	02234
0000500777777777600	02166	0000004000000000175	02235
0000000000000000172	02167	0000000000000000146	02236
0000000440000000160	02170	0000005000000000175	02237
7000000777777777613	02171	0000000000000000146	02240
0000001000000000142	02172	0000002000000000175	02241
0000000000000000163	02173	0000000000000000146	02242
0000001000000000142	02174	0000006000000000175	02243
0000500000000000140	02175	0000000000000000146	02244
0000000000000000172	02176	0000001000000000175	02245
0000000040000000120	02177	0000000000000000146	02246
0000001000000000144	02200	0000003000000000176	02247
0000000000000000150	02201	0000000000000000146	02250
0000000000000000143	02202	0000004000000000176	02251
0000003000000000167	02203	0000000000000000146	02252
0000000000000000146	02204	0000005000000000176	02253
0000004000000000167	02205	0000000000000000146	02254
0000000000000000146	02206	0000002000000000176	02255
0000005000000000167	02207	0000000000000000146	02256
0000000000000000146	02210	0000006000000000176	02257
0000002000000000167	02211	0000000000000000146	02260
0000000000000000146	02212	0000001000000000176	02261
0000006000000000167	02213	0000000000000000146	02262
0000000000000000146	02214	0000000000000000144	02263
0000001000000000167	02215	0000001400000000204	02264
0000000000000000146	02216	0000000000000000140	02265
0000003000000000173	02217	0000001400000000204	02266
0000000000000000146	02220	0000000000000000140	02267
0000004000000000173	02221	0000001400000000204	02270
0000000000000000146	02222	0000000000000000140	02271
0000005000000000173	02223	0000001400000000204	02272
0000000000000000146	02224	0000000000000000140	02273
0000002000000000173	02225	0000001400000000204	02274
0000000000000000146	02226	0000000000000000140	02275
0000006000000000173	02227	0000001400000000204	02276
0000000000000000146	02230	0000000000000000140	02277
0000001000000000173	02231		

Figure 7-26. Self-Check Tape Listing (Sheet 16)

Tape Word	Word Count	Tape Word	Word Count
0000010400000000204	02300	0000000000000000146	02347
0000000000000000140	02301	0000776000000000155	02350
0000010400000000204	02302	0000000000000000146	02351
0000000000000000140	02303	0000776000000000152	02352
0000010400000000204	02304	0000000000000000146	02353
0000000000000000140	02305	0000776000000000156	02354
0000010400000000204	02306	0000000000000000146	02355
0000000000000000140	02307	0000776000000000151	02356
0000010400000000204	02310	0000000000000000146	02357
0000000000000000140	02311	0000773000000000153	02360
0000010400000000204	02312	0000000000000000146	02361
0000000000000000140	02313	0000773000000000154	02362
0000300400000000204	02314	0000000000000000146	02363
0000000000000000146	02315	0000773000000000155	02364
0000400400000000204	02316	0000000000000000146	02365
0000000000000000146	02317	0000773000000000152	02366
0000500400000000204	02320	0000000000000000146	02367
0000000000000000146	02321	0000773000000000156	02370
0000200400000000204	02322	0000000000000000146	02371
0000000000000000146	02323	0000773000000000151	02372
0000600400000000204	02324	0000000000000000146	02373
0000000000000000146	02325	0000767000000000153	02374
0000100400000000204	02326	0000000000000000146	02375
0000000000000000146	02327	0000767000000000154	02376
0000775000000000153	02330	0000000000000000146	02377
0000000000000000146	02331	0000767000000000155	02400
0000775000000000154	02332	0000000000000000146	02401
0000000000000000146	02333	0000767000000000152	02402
0000775000000000155	02334	0000000000000000146	02403
0000000000000000146	02335	0000767000000000156	02404
0000775000000000152	02336	0000000000000000146	02405
0000000000000000146	02337	0000767000000000151	02406
0000775000000000156	02340	0000000000000000146	02407
0000000000000000146	02341	0000757000000000153	02410
0000775000000000151	02342	0000000000000000146	02411
0000000000000000146	02343	0000757000000000154	02412
0000776000000000153	02344	0000000000000000146	02413
0000000000000000146	02345	0000757000000000155	02414
0000776000000000154	02346		

Figure 7-26. Self-Check Tape Listing (Sheet 17)

Tape Word	Word Count	Tape Word	Word Count
0000000000000000146	02415	0000577000000000156	02464
0000757000000000152	02416	0000000000000000146	02465
0000000000000000146	02417	0000577000000000151	02466
0000757000000000156	02420	0000000000000000146	02467
0000000000000000146	02421	0000377000000000153	02470
0000757000000000151	02422	0000000000000000146	02471
0000000000000000146	02423	0000377000000000154	02472
0000737000000000153	02424	0000000000000000146	02473
0000000000000000146	02425	0000377000000000155	02474
0000737000000000154	02426	0000000000000000146	02475
0000000000000000146	02427	0000377000000000152	02476
0000737000000000155	02430	0000000000000000146	02477
0000000000000000146	02431	0000377000000000156	02500
0000737000000000152	02432	0000000000000000146	02501
0000000000000000146	02433	0000377000000000151	02502
0000737000000000156	02434	0000000000000000146	02503
0000000000000000146	02435	0000000000000000147	02504
0000737000000000151	02436	0000000240000000160	02505
0000000000000000146	02437	0000500000000000140	02506
0000677000000000153	02440	0000000000000000143	02507
0000000000000000146	02441	7004600000000000150	02510
0000677000000000154	02442	0000000000000000147	02511
0000000000000000146	02443	7000003000000000150	02512
0000677000000000155	02444	0000000000000000147	02513
0000000000000000146	02445	0000500200000000100	02514
0000677000000000152	02446	0000000000000000144	02515
0000000000000000146	02447	0000000000000000172	02516
0000677000000000156	02450	0000000440000000160	02517
0000000000000000146	02451	0000500000000000140	02520
0000677000000000151	02452	0004604000000000172	02521
0000000000000000146	02453	0000003500000000172	02522
0000577000000000153	02454	0000500000000000140	02523
0000000000000000146	02455	0000000000000000143	02524
0000577000000000154	02456	7004004000000000150	02525
0000000000000000146	02457	0000000000000000147	02526
0000577000000000155	02460	0000000000000000144	02527
0000000000000000146	02461	0000003000000000172	02530
0000577000000000152	02462	0004004000000000172	02531
0000000000000000146	02463		

Figure 7-26. Self-Check Tape Listing (Sheet 18)

Tape Word	Word Count	Tape Word	Word Count
000000300000000172	02532	000020300000000172	02601
000050060000000240	02533	C00000000000000143	02602
000000000000C00172	02534	0004C10000000C00150	02603
C00000044000000160	02535	000000000000000147	02604
000050000000000140	02536	C00000000000000144	02605
000000000000000143	02537	000000300000000172	02606
700440000000000150	02540	000000000C000000150	02607
000000000000000147	02541	000000000000100060	02610
700000360000000150	02542	000000000000000140	02611
000000000000000147	02543	000000000000000140	02612
000400000000000140	02544	000C000000000C00140	02613
700000300000000150	02545	000000000000000140	02614
C00000000000000147	02546	000000000000000147	02615
700420400000000150	02547	000000000000000143	02616
000000000000000147	02550	700420000000000150	02617
700000360000C00150	02551	C00000000000000147	02620
000C000000000C00147	02552	C00000000000000144	02621
000440000000000172	02553	000020300000000172	02622
700000300000000150	02554	000000000000000143	02623
000000000400000130	02555	C00401400000000150	02624
000000000000000140	02556	000000000000000147	02625
000000000000000140	02557	000000000000C00144	02626
000000000000000140	02560	00C000300000000172	02627
000000000000000140	02561	000000000000000150	02630
C00000000000000147	02562	000000000040000120	02631
000401400000000140	02563	000030000000000140	02632
000000000000000144	02564	000000000000000140	02633
000000300000000172	02565	000000000C000000140	02634
000477700000000157	02566	000000000C000000140	02635
000020350000000172	02567	C00000000000000147	02636
000000000000000143	02570	000000024000000160	02637
000401400000000150	02571	000000020001000020	02640
000000000000000147	02572	C00003000000020072	02641
000000000000000144	02573	000000020000000120	02642
000020300000020072	02574	00C000300000000172	02643
000000000000000143	02575	C00000000000000150	02644
000400400000000150	02576	000050040000000100	02645
000000000000000147	02577	C00000000000000143	02646
000000000000000144	02600		

Figure 7-26. Self-Check Tape Listing (Sheet 19)

Tape Word	Word Count	Tape Word	Word Count
C0040010000000160	02647	00005000000000C140	02716
0000000000000C00146	02650	C0043004000000C100	02717
C0000000000C00147	02651	C0000000000000C172	02720
C0000000000000000144	02652	C000003000000C0C172	02721
0000003000000C0C172	02653	C0005000000000240	02722
0000000C0000000143	02654	0000060000000000140	02723
0000000000000000164	02655	0000000000000C0C172	02724
C00050077777777600	02656	0000003000000C0C272	02725
0000000000000000172	02657	0000460000000C0C140	02726
C0000004400000C160	02660	0000000000000000172	02727
70000C0477777777614	02661	0000003000000001072	02730
0000500000000CCC140	02662	00C0400400000000100	02731
C0000000000000000144	02663	0000000C0000000172	02732
0000000240000000160	02664	000000300000000001072	02733
C0C0000000C00000150	02665	C0006100000C000172	02734
0340000000000C0145	02666	0000003400000000132	02735
0000000000000000146	02667	00005000C002000040	02736
0200000000000C0C145	02670	0016010000020000040	02737
0000000000000C0C146	02671	C0164000000200C040	02740
0100000000000000145	02672	0000500000000000140	02741
0000000000000000146	02673	0000000000000000172	02742
0040000000000C00145	02674	0000000000000000150	02743
0000000000000C0C146	02675	0000000000000C000140	02744,02745
4000000000000000145	02676	0000000000000000146	02746
0000000000000000146	02677	0000000000000000140	02747
2000000000000C00145	02700	0000000000000000146	02750
C0000000000000C0146	02701	C0005004000000C100	02751
1000000000000000145	02702	0000000000000000146	02752
0000000000000C0C146	02703	C0000000000000C172	02753
0200500400000000105	02704	C0000000000000000147	02754
0000000000000000146	02705	C0000030000000000172	02755
0000000000000000147	02706	0000500400000000100	02756
0000000000000000172	02707	4036000600000000040	02757
0000003400000000132	02710	4030000200000000100	02760
0000000000000000172	02711	4012000000000000140	02761
7400000000000000144	02712	4022000000000000140	02762
4000000000000000147	02713	0000003770000000172	02763
0000777000000000155	02714	000000777000000C172	02764
4000000000000C00165	02715		

Figure 7-26. Self-Check Tape Listing (Sheet 20)

Tape Word	Word Count	Tape Word	Word Count
0000500000000000140	02765	0000000000000000146	03041
0026000400000000100	02766	0000000000000000166	03042
0026410000000000140	02767	0000777000000000156	03043
0000500401000000140	02770	0000000000000000142	03044
0216000400000000100	02771	0000000000000000143	03045
0216400400000000100	02772	0000000000000000147	03046
0236000400000000100	02773	0000500000000000140	03047
0206000400000000134	02774	0000000400000000204	03050
0214000400000000126	02775	0030000000000000151	03051
0202000000000000170	02776	0000000000000000154	03052
0004000400000000117	02777	0000000000000000150	03053
0000000000400000120	03000	0030000000000000157	03054
0000000000000020060	03001	0000000000000000146	03055
0000000000000020060	03002	0000500000000000140	03056
0000000000000010060	03003	0000000000000000147	03057
0000000000000004060	03004	0030000000000000152	03060
0000000000000002060	03005	0000000000000000151	03061
0000000000000100060	03006	0000000000000000150	03062
0000000000000040060	03007	0030000000000000157	03063
0000000004000000120	03010	0000000000000000146	03064
0300000000000000145	03011	0000500000000000140	03065
0240000000000000145	03012	0000000000000000147	03066
0140000000000000145	03013	0030000000000000154	03067
0000500000000000140	03014	0000000000000000150	03070
0000000000000000172	03015	0030000000000000157	03071
0000000040000000120	03016	0000000000000000146	03072
0000000000000000140	03016A	0000500000000000140	03073
0000000000000000140	03017	0030776000000000156	03074
0000000000000000140	03020	0000000000000000146	03075
0000000000000000140	03021	0030776000000000155	03076
0000000000000000150	03030	0000000000000000146	03077
0000000400000000203	03031	0030776000000000153	03100
4000000000000000152	03032	0000000000000000146	03101
0000000000000000140	03033	0030775000000000156	03102
2000000000000000154	03034	0000000000000000146	03103
0000000000000000140	03035	0030775000000000155	03104
1000000000000000151	03036	0000000000000000146	03105
0000000000000000147	03037	0030775000000000153	03106
0002070000000000150	03040		

Figure 7-26. Self-Check Tape Listing (Sheet 21)

Tape Word	Word Count	Tape Word	Word Count
0000000000000000146	03107	C03037700000000155	03156
0030773000000000156	03110	C0000000000000000146	03157
0000000000000000146	03111	0030377000000000153	03160
0030773000000000155	03112	0000000000000000146	03161
0000000000000000146	03113	C0000000000000000147	03162
0030773000000000153	03114	C0000000000000000143	03163
0000000000000000146	03115	0002001000000000170	03164
0030767000000000156	03116	0002002000000000170	03165
0000000000000000146	03117	0002004000000000170	03166
0030767000000000155	03120	0030001000000000163	03167
0000000000000000146	03121	C0300020000000000163	03170
0030767000000000153	03122	0030004000000000163	03171
0000000000000000146	03123	0000500000000000140	03172
0030757000000000156	03124	0036006000000000160	03173
0000000000000000146	03125	0036005000000000160	03174
0030757000000000155	03126	0036003000000000160	03175
0000000000000000146	03127	0000500070000007000	03176
0030757000000000153	03130	7012000070000007011	03177
0000000000000000146	03131	0000000000000000150	03200
0030737000000000156	03132	0012000000000000140	03201
0000000000000000146	03133	0000000000000000146	03202
0030737000000000155	03134	0000000000000000147	03203
0000000000000000146	03135	7012000070000007012	03204
0030737000000000153	03136	0000000000000000150	03205
0000000000000000146	03137	0012000000000000140	03206
0030677000000000156	03140	0000000000000000146	03207
0000000000000000146	03131	0000000000000000147	03210
0030677000000000155	03142	7012000070000007014	03211
0000000000000000146	03143	0000000000000000150	03212
0030677000000000153	03144	0012000000000000140	03213
0000000000000000146	03145	0000000000000000146	03214
0030577000000000156	03146	0000500376400376400	03215
0000000000000000146	03147	0000000000000000147	03216
0030577000000000155	03150	7553000376401476560	03217
0000000000000000146	03151	0000000000000000150	03220
0030577000000000153	03152	0012000000000000140	03221
0000000000000000146	03153	0000000000000000146	03222
0030377000000000156	03154	0000000000000000147	03223
0000000000000000146	03155		

Figure 7-26. Self-Check Tape Listing (Sheet 22)

Tape Word	Word Count	Tape Word	Word Count
7553000376401476 55	03224	700440000000000153	03273
0000000000000000150	03225	70000030774000110	03274
0012000000000000140	03226	403000000000000140	03275
0000000000000000146	03227	0000000000000000146	03276
0000000000000000147	03230	0000000000000000147	03277
7553000376401476 53	03231	700420400000000151	03300
0000000000000000150	03232	70000030614000C150	03301
0012000000000000140	03233	403000000000000140	03302
0000000000000000146	03234	0000000000000000146	03303
00005C006140000140	03235	0000000000000000147	03304
0000000000000000172	03236	700420000000000152	03305
0000000440000000160	03237	70000030614000C150	03306
0000500000000000140	03240	403000000000000140	03307
0000000000000000147	03241	00C0000000000000146	03310
700440000000000151	03242	0000000000000000147	03311
70000030614000C150	03243	700420000000000154	03312
403000000000000140	03244	70000030614000C150	03313
0000000000000000146	03245	403000000000000140	03314
0000000000000000147	03246	0000000000000000146	03315
700440000000000152	03247	0000000000000000147	03316
70000030614000C150	03250	700420000000000156	03317
403000000000000140	03251	70000030774000011O	03320
0000000000000000146	03252	403000000000000140	03321
0000000000000000147	03253	0000000000000000146	03322
700440000000000154	03254	0000000000000000147	03323
70000030614000C150	03255	700420400000000155	03324
403000000000000140	03256	70000030774000C110	03325
0000000000000000146	03257	403000000000000C140	03326
0000000000000000147	03260	00C0000000000000146	03327
700440000000000156	03261	0000000000000000147	03330
70000030774000110	03262	700420400000000153	03331
403000000000000140	03263	70C0003077400C0110	03332
00C0000000000000146	03264	403000000000000C140	03333
0000000000000000147	03265	0000000000000000146	03334
700440000000000155	03266	400000000000000150	03335
70000030774000011O	03267	0000000000430000120	03336
403000000000000140	03270	00C0000000000000140	03337
0000C0000000000146	03271	0000000000000000140	03340
0000000000000000147	03272		

Figure 7-26. Self-Check Tape Listing (Sheet 23)

Tape Word	Word Count	Tape Word	Word Count
0000000000000000140	03341	0000000000000000147	03410
0000000000000000140	03342	7000007000004020010	03411
0000000004001000020	03343	0000000000010000120	03412
4030000000000000140	03344	0000001000000000143	03413
0000000000000000146	03345	0000000004001000020	03414
0000000000000000147	03346	0000000000000000147	03415
7000007000000060150	03347	7000007000100200l0	03416
2000000000000000150	03350	0000000000100000120	03417
0000000004001000020	03351	4000000000000000143	03420
4030000000000000140	03352	0000000004001000020	03421
0000000000000000146	03353	0000000000000000147	03422
0000000000000000147	03354	7000007000200200l0	03423
7000007000000120150	03355	0000000000100000120	03424
1000000000000000150	03356	2000000000000000143	03425
0000000004001000020	03357	0000000004001000020	03426
4030000000000000140	03360	0000000000000000147	03427
0000000000000000146	03361	7000007000400200l0	03430
0000000000000000147	03362	0000000000100000120	03431
7000007000000220150	03363	1000000000000000143	03432
0000020000000000143	03364	0000000004001000020	03433
0000000004001000020	03365	0000000000000000147	03434
0000000000000000147	03366	7000007001000200l0	03435
7000007000000420150	03367	0000000000100000120	03436
0000000000100000120	03370	0400000000000000143	03437
0000000004001000020	03371	0000000004001000020	03440
0000000000000000147	03372	0000000000000000147	03441
7000007000000200150	03373	7000007002000200l0	03442
0000010000000000143	03374	0000000000100000120	03443
0000000004001000020	03375	0000400000000000143	03444
0000000000000000147	03376	0000000004001000020	03445
7000007000001020150	03377	0000000000000000147	03446
0000000000100000120	03400	7000007004000200l0	03447
0000004000000000143	03401	0000000000100000120	03450
0000000004001000020	03402	0000200000000000143	03451
0000000000000000147	03403	0000000004001000020	03452
7000007000020200150	03404	0000000000000000147	03453
0000000000100000120	03405	7000007010000200l0	03454
0000002000000000143	03406	0000000000100000120	03455
0000000004001000020	03407		

Figure 7-26. Self-Check Tape Listing (Sheet 24)

Tape Word	Word Count	Tape Word	Word Count
C0001000000000143	03456	0000020000000C0172	03525
0000000040010000020	03457	0000000040010000020	03526
0000000000000C147	03460	0000007000000020072	03527
7000007020C0020010	03461	C0001111000000C204	03530
0000000000100C0120	03462	0000000040010000020	03531
0000040000000C0143	03463	0000007700000C6132	03532
0000000040010000020	03464	0000000000000C0150	03533
00C0000000000C0147	03465	4030000000000C0140	03534
700000704000020010	03466	0000000000000C0146	03535
0000000000100C0120	03467	C0000000000000C147	03536
0000000000000C0147	03470	C0002114000000C204	03537
C0000000000000C0144	03471	0000000040010000020	03540
0000007400000000204	03472	00C0007700001 2C132	03541
C0000000400100C020	03473	C0000000000000C150	03542
0000007100000 20032	03474	4030000C0000000140	03543
0000000000100C0120	03475	0000000000000C0146	03544
0000070400000C0204	03476	0000000C0000C00147	03545
0000000040010000020	03477	0000411400000 0C204	03546
0000007200000020032	03500	0000000040010000020	03547
0000000000100C0120	03501	0000007700002 20132	03550
0000700400000000204	03502	C0000000000000150	03551
0000000040010000020	03503	4030000000000C0140	03552
0000007400000 20032	03504	0000000000000C0146	03553
C0000114000000C204	03505	C0000000000000147	03554
0000C2000000C00140	03506	C0005000000000C140	03555
0000000040010000020	03507	0000000240000C0160	03556
0000007700000 20032	03510	0000500000000C0240	03557
0000000000000C0172	03511	0000076000000C0172	03560
0000000040010000020	03512	0000007000000C0172	03561
0000007700000020032	03513	0000062000000C0172	03562
0000420000000C0172	03514	0000007000000000172	03563
0000000040010000020	03515	0000000000000C00040	03564
C0000077000020032	03516	0000500000020C0040	03565
C0000210000000C172	03517	C0U0076000000000172	03566
0000000040010C00020	03520	0000000201000C0160	03567
0000022000000000172	03522	0000030000200 0072	03570
0000007700000 20032	03521	0000500000000C0140	03571
0000000040010C00020	03523	0000076000000C0172	03572
0000CC7700000 20032	03524		

Figure 7-26. Self-Check Tape Listing (Sheet 25)

Tape Word	Word Count	Tape Word	Word Count
0000000201000C0160	03573	000007600000000140	03642
0000003000000000172	03574	0000000201000000160	03643
0000500000020000040	03575	0000003000020000072	03644
0000076000000000172	03576	0000500400000000100	03645
0000000201000000160	03577	0000000000000000172	03646
0000000201000000160	03600	0000500000000000140	03647
0000003000020000072	03601	0000203400000000132	03650
0000500000000000240	03602	0000000000000000143	03651
0000000000000000172	03603	0004010000000000150	03652
0000000440000000160	03604	0000000000000000147	03653
0000000201000000160	03605	0000C0000000000144	03654
0000003000000000272	03606	0000003000000000172	03655
0000500000020000040	03607	0000700400000000204	03656
0000000000000000172	03610	0000000000000000172	03657
0000000440000000160	03611	0000000000000000143	03660
0000000201000000160	03612	0004C1400000000150	03661
0000003000020000072	03613	0000000000000000144	03662
0000500000000000140	03614	0000000000000000147	03663
0000176000000000172	03615	0000003000000000172	03664
0000000201000000160	03616	0000000000010000120	03665
0000003000020000072	03617	0000000240000000172	03666
0000036000000000172	03620	0000500000020000040	03667
0000000201000000160	03621	0000062000000000172	03670
0000003000020000072	03622	0000500000000000140	03671
0000056000000000172	03623	0000000200200000160	03672
0000000201000000160	03624	0000003000020000072	03673
0000003000020000072	03625	0000062000000000172	03674
0000066000000000172	03626	0000000200200000160	03675
0000000201000000160	03627	0000003000000000172	03676
0000003000020000072	03630	0000500000020000040	03677
0000072000000000172	03631	0000000000000000172	03700
0000000201000000160	03632	0000000200200000160	03701
0000003000020000072	03633	0000003000000000172	03702
0000074000000000172	03634	0000000402000000160	03703
0000000201000000160	03635	0000000200200000160	03704
0000003000020000072	03636	0000003000000000172	03705
0000077000000000172	03637	0000000000000000172	03706
0000000201000000160	03640	0000000402000000160	03707
0000003000020000072	03641		

Figure 7-26. Self-Check Tape Listing (Sheet 26)

Tape Word	Word Count	Tape Word	Word Count
0000000200200000160	03710	0000000200200000160	03757
0000003000020000072	03711	0000003000000000172	03760
0000500000000000240	03712	0000000040000000120	03761
0000000402000000160	03713	0000062000000000172	03762
0000000200200000160	03714	0000000000000000172	03763
0000003000020000072	03715	0000000201000000160	03764
0000000000000000172	03716	0000003000000000172	03765
0000000400000000120	03717	0000000000000000172	03766
0000000200200000160	03720	0000500000000000140	03767
0000003000020000072	03721	0000000000000000040	03770
0000500000000000140	03722	7716000000000000140	03771
0000162000000000172	03723	7726000000000000140	03772
0000000200200000160	03724	7732000000000000140	03773
0000003000020000072	03725	7734000000000000140	03774
0000022000000000172	03726	0036000000000000150	03775
0000000200200000160	03727	7736000000000000140	03776
0000003000020000072	03730	0000000000000000146	03777
0000042000000000172	03731	0036000000000000147	04000
0000000200200000160	03732	7736000000000000142	04001
0000003000020000072	03733	0036000000000000150	04002
0000072000000000172	03734	7736000400000000203	04003
0000000200200000160	03735	0000000000000000146	04004
0000003000020000072	03736	0036000000000000144	04005
0000066000000000172	03737	7736000000000000140	04006
0000000200200000160	03740	0000000000000000146	04007
0000003000020000072	03741	0036000000000000152	04010
0000060000000000172	03742	0000000000000000146	04011
0000000200200000160	03743	0036000000000000162	04012
0000003000020000072	03744	0000000000000000146	04013
0000063000020000072	03745	7736000400000000203	04014
0000000200200000160	03746	0000000000000000146	04015
0000003000020000072	03747	0036000000000000147	04016
0000062000000000140	03750	0036000000000000146	04017
0000000200200000160	03751	0000010000000000141	04020
0000003000020000072	03752		
0000062000000000172	03753		
0000500000000010040	03754		
0000076000000000172	03755		
0000000000000000172	03756		

Figure 7-26. Self-Check Tape Listing (Sheet 27)

Tape Word Count	Operation	Indication
00001	RIE	
00002	RT6	
00003		CHECKS SERIALIZER AND SERIAL PARITY ERROR IN THE FOLLOWING CHECKS THE INDICATED COMMAND LAMPS WILL LIGHT
00004		DS1
00005		DS2
00006		DS3
00007		DS4
00010		DM1
00011		DM2
00012		DM3
00013		DDX
00014		CA9
00015		CA8
00016		CA7
00017		CA6
00020		CA5
00021		CA4
00022		CA3
00023		CA2
00024		CA1
00025	LDLC3	CLEARS DL IN THE FOLLOWING CHECKS THE INDICATED COMMAND LAMPS WILL LIGHT
00026		DP1

Figure 7-27. Self-Check Tape Instructions (Sheet 1 of 57)

Tape Word Count	Operation	Indication
00027	CP2	
00030	CP3	
00031	CP4	
00032	SIGN	
00033	B1	
00034	B2	
00035	B3	
00036	B4	
00037	B5	
00040	B6	
00041	B7	
00042	B8	
00043	B9	
00044	B10	
00045	B11	
00046	B12	
00047	B13	
00050	B14	
00051	B15	
00052	B16	
00053	B17	
00054	B18	
00055	B19	
00056	B20	
00057	B21	
00060	B22	
00061	B23	
00062	B24	
00063	B25	
00064		
00065		
00066		
00067		
00070		
00071		
00072	SIE	
00073	SPE	SYL1PB=1, DATA IS ODD SYL0PB=1, DATA IS EVEN
00074	SSL	
00075	SPE	SYL1PB=0, DATA IS EVEN SYL0PB=1, DATA IS EVEN

Figure 7-27. Self-Check Tape Instructions (Sheet 2)

```
Tape
Word Operation                          Indication
Count

00076 SSL
00077 SPE      SYL1PB=1, DATA IS EVEN   SYLOPB=1, DATA IS ODD
00100 SSL
00101 SPE      SYL1PB=1, DATA IS EVEN   SYLOPB=0, DATA IS EVEN
00102 SSL
00103 ST6
00104 FPE      ACME PB=0
00105 SSL
00106 SPE      ACME PB=1
00107 SSL
00110 RIE      END OF SERIAL PARITY CHECK
00111 RT6
00112 PIO      CLEARS PIO ADRESS REGISTER
00113 SPA
00114          PIO ADDRESS=ZERO  NO ADDRESS TRANSFER WITH PIO=0
00115 SPA
00116 PIO      PIO A2 TO A9 ARE ON
00117 SPA
00120 PIO      PIO A1 IS ON
00121 SPA
00122 PIO      CLEARS PIO ADR REG
00123 SPA
00124          CHECKS THAT NO ERROR OCCURS WITH NO SPA
00125 SIE
00126 SPA      PIO ADR ERROR   PIO ADRSO=0  DTSO=1
00127 SSL
00130 PIO      PIO A9=1
00131 SPA      PIO ADR ERROR   PIO ADRSO=1  DTSO=0
00132 SSL
00133 RIE      END OF PIO ADR TESTS
00134 LDLC3    LOADS DL WITH ALL ONES
00135 PIO      LOADS IO1 WITH ALL ONES
00136 LDLC3    CLEARS DL
00137 CI0001,006  LOADS IO2 WITH ALL ONES
00140 PIO      CHECKS IO1 FOR ONES
00141 PIO      CHECKS IO2 FOR ONES
00142 PIO      CHECKS THAT NO ERROR OCCURS WHEN OA4=1
00143 PIO      CLEARS IO1
```

Figure 7-27. Self-Check Tape Instructions (Sheet 3)

Tape Word Count	Operation	Indication
00144	PIO	CHECKS IO1 FOR ZEROES
00145	PIO	CHECKS IO2 FOR ONES
00146	CIO001,0C6	CLEARS IO2
00147	PIO	CHECKS IO2 FOR ZEROS
00150	PIO	CHECKS IO1 FOR ZEROS
00151	PIO	CHECKS IO2 CIRCULATE LOOP
00152	PIO	CHECKS IO2 FOR ZEROS
00153	LDLC3	LOADS DL WITH ONES
00154	PIO	LOADS IO1 WITH ONES
00155	LDLC3	CLEARS DL
00156	PIO	CHECKS IO1 FOR ONES
00157	PIO	CHECKS IO2 FOR ZEROS
00160	CIO001,0C6	LOADS IO2 WITH ONES
00161	PIO	CHECKS IO1 FOR ONES
00162	PIO	CHECKS IO2 FOR ONES
00163	PIO	CLEARS IO1
00164	PIO	CHECKS IO1 FOR ZEROS
00165	CIO002,025	LOADS IO1 WITH ONES
00166	PIO	CHECKS IO2 FOR ONES
00167	PIO	CHECKS IO1 FOR ONES
00170	PIO	CLEARS IO1
00171	CIO001,006	CLEARS IO2
00172	LDLC3	LOADS DL WITH ONES
00173	PIO	LOADS IO1 WITH ONES
00174	LDLC3	CLEARS DL
00175	CIO002,025	IO2 IS ZEROS IO1 IS ONES
00176	PIO	CHECK IO1 FOR ONES
00177	PIO	CHECK IO2 FOR ZEROS
00200	LDLC3	LOAD DL WITH ONES
00201	PIO	LOAD IO1 WITH ONES
00202	CIO001,0C6	LOAD IO2 WITH ONES
00203	LDLC3	CLEAR DL
00204	PIO	CLEAR IO1
00205	CIO001,025	IO1 IS ZEROS IO2 IS ONES
00206	PIO	CHECKS IO1 FOR ZEROS
00207	LDLC3	LOAD DL WITH ONES
00210	PIO	IO1 CONTAINS ZEROS
00211	PIO	CHECKS IO1 FOR ZEROS
00212	LDLC3	CLEARS DL

Figure 7-27. Self-Check Tape Instructions (Sheet 4)

```
Tape
Word Operation                          Indication
Count

00213 PIO       CLEARS IO1
00214 CI0001,006  CLEARS IO2
00215 LDLC3     LOADS DL WITH ONES
00216 PIO       LOADS IO1 WITH ONES
00217 CI0001,0025  IO2 CONTAINS ZEROS
00220 PIO       CHECKS IO2 FOR ZEROS
00221 CI0001,006  LOADS IO2 WITH ONES
00222 CI0016    CLEARS IO2
00223 PIO       CHECKS IO2 FOR ZEROS
00224 CI0001,006  LOADS IO2 WITH ONES
00225 CI0021    CLEARS IO2
00226 PIO       CHECKS IO2 FOR ZEROS
00227           CHECKS PIO A1 AND A2
00230 PIO       CHECKS PIO A1 AND A2
00231 PIO       CHECKS PIO A1 AND A2
00232 CI0016    CLEARS IO2
00233 CI0002,025  CLEARS IO1
00234 CI0002    PAM=0 WHEN PIO=0
00235 PIO       CHECK IO1 FOR ZEROS
00236 LDLC3     LOADS EVEN BITS INTO DL
00237 PIO       LOADS EVEN BITS INTO IO1
00240 PIO       CHECK IO1 FOR EVEN BITS
00241 CI0001,006  LOADS EVEN BITS INTO IO2
00242 PIO       CHECK IO1 FOR  EVEN BITS
00243 PIO       CHECK IO2 FOR  EVEN BITS
00244 CI0016    CLEAR IO2
00245 CI0002,025  CLEAR IO1
00246 CI0002,021  IO1 IS ZEROS
00247 PIO       CHECKS IO1 FOR ZEROS
00250 PIO       LOAD IO1 WITH EVEN BITS
00251 CI0001,006  LOAD IO2 WITH EVEN BITS
00252 LDLC3     CLEARS DL
00253 PIO       CLEARS IO1
00254 CI0002,021  IO1=000025252
00255 PIO       CHECK IO1 FOR ABOVE PATTERN
00256 CI0016    CLEAR IO2
00257 CI0002,025  CLEAR IO1
00260 SIE
```

Figure 7-27. Self-Check Tape Instructions (Sheet 5)

```
Tape
Word Operation                          Indication
Count
00261 PIO      CHECKS CPIOM LO BIT
00262 SSL
00263 PIO      CHECKS CPIOA LO BIT
00264 SSL
00265 PIO      CHECKS CPIOM HO BIT
00266 SSL
00267 PIO      CHECKS CPIOA HO BIT
00270 SSL
00271 LDLC3    LOAD B25 IN DL
00272 PIO      LOAD B25 IN IO1
00273 PIO      CHECK CPIOM
00274 SSL
00275 RIE      END OF IO TEST
00276 LDLC3    CLEAR DL
00277          CHECK DIN FOR TROP3=1  CHECK INSSO AND DSMSO FOR CYC2
00300 PIO      LOAD IO1 WITH ZEROS
00301 PIO      CHECK IO1 FOR ZEROS
00302 LDLC2    CHECK INSSO AND DSMSO FOR PHB AND PHC OF CYC2
00303 PIO      LOAD IO1 WITH 820 AND SIGN
00304 PIO      CHECK IC1 FOR 820 AND SIGN
00305 LDLC2
00306 LDLC2    CHECKS THAT DIN=DTSO DURRING CYC3 ONLY
00307 PIO      IC1 CONTAINS SIGN ONLY
00310 PIO      CHECKS IO1 FOR SIGN ONLY
00311 LDLC3    CLEARS DL
00312 PIO      CLEARS IO1
00313 CAL321   NO ADDRESS ERROR
00314          NO COMPARE ERROR
00315          NO COMPARE ERROR
00316 MPH      NO COMPARE ERROR
00317 TMI      NO COMPARE ERROR
00320          NO COMPARE ERROR
00321 LDLC3    LOADS IS1,IS2,IS3,IS4 IN DL
00322          NO COMPARE ERROR
00323 TRA      NO COMPARE ERROR
00324 LDLC3    CLEAR DL  END OF COMPARATOR CONTROL TEST
00325          A1 TO A8 ARE ONES
00326          A9=1
00327 SIE
```

Figure 7-27. Self-Check Tape Instructions (Sheet 6)

Tape Word Count	Operation	Indication
00330	CAL321 NA1=1,OA1=0	
00331	SSL	
00332	LDLC3 CLEAR DL	
00333	CAL321 NA2=1,OA2=0	
00334	SSL	
00335	LDLC3 CLEAR DL	
00336	CAL321 NA3=1,OA3=0	
00337	SSL	
00340	CLEAR DL	
00341	CAL321 NA4=1,OA4=0	
00342	SSL	
00343	LDLC3 CLEAR DL	
00344	CAL321 NA5=1,OA5=0	
00345	SSL	
00346	LDLC3 CLEAR DL	
00347	CAL321 NA6=1,OA6=0	
00350	SSL	
00351	LDLC3 CLEAR DL	
00352	CAL321 NA7=1,OA7=0	
00353	SSL	
00354	LDLC3 CLEAR DL	
00355	CAL321 NA8=1,OA8=0	
00356	SSL	
00357	LDLC3 CLEAR DL	
00360	CAL321 NA9=1,OA9=0	
00361	SSL	
00362	LDLC3 CLEAR DL	
00363	CAL0 NA1=0,OA1=1	
00364	SSL	
00365	CAL0 NA2=0,OA2=1	
00366	SSL	
00367	CAL0 NA3=0,OA3=1	
00370	SSL	
00371	CAL0 NA4=0,OA4=1	
00372	SSL	
00373	CAL0 NA5=0,OA5=1	
00374	SSL	
00375	CAL0 NA6=0,OA6=1	

Figure 7-27. Self-Check Tape Instructions (Sheet 7)

```
Tape
Word Operation                          Indication
Count
00376 SSL
00377 CALO      NA7=0,CA7=1
00400 SSL
00401 CALO      NA8=0,CA8=1
00402 SSL
00403 CALO      NA9=0,CA9=1
00404 SSL
00405 XOR       NOP1=1,OP1=0
00406 SSL
00407 PIO       NOP2=1,OP2=0
00410 SSL
00411 TMI       NOP3=1,OP3=0
00412 SSL
00413 TRA       NOP3=0,OP3=1
00414 SSL
00415 HOP       NOP4=0,OP4=1
00416 SSL
00417 STO       NOP4=1,OP4=0
00420 SSL
00421 MPY       NOP2=0,OP2=1
00422 SSL
00423 SUB       NOP1=0,OP1=1
00424 SSL
00425 RIE
00426 CIO002,045  CLEAR IO1
00427 PIO       CHECK IO1 FOR ZEROS
00430 CIO002,045  LOAD IO1 WITH B16,14,12,10
00431 PIO       CHECK IO1 FOR B16,14,12,10
00432 CIO002,045  LOAD IO1 WITH B17
00433 PIO       CHECK IO1 FOR B17
00434 CIO002,045  LOAD IO1 WITH B15,13,11,9
00435 PIO       CHECK IO1 FOR B15,13,11,9
00436 SIE
00437 CIO002,045  CLEAR IO1
00440 SSL
00441 RIE
00442 PIO       CHECK IO1 FOR ZEROS
00443 SIE
00444 CIO002,045  CLEAR IO1
```

Figure 7-27. Self-Check Tape Instructions (Sheet 8)

```
Tape
Word Operation                          Indication
Count

00445 SSL
00446 RIE
00447 PIO      CHECK IO1 FOR ZEROS
00450 CI0002   IO1 CONTAINS ZEROS
00451 PIO      CHECKS IO1 FOR ZEROS
00452          NO ADDRESS ERROR   OA8  OP4  OP2
00453 SIE
00454          NOP1=0,OP1=1
00455 SSL
00456          NOP3=1,OP3=0
00457 SSL
00460          NA8=1,OA8=0
00461 SSL
00462 RIE      END OF ADRSR TEST
00463 LDLC3    CLEAR DL
00464 PIO      LOAD PIO A1
00465 CI0002,011  LOAD IO1 WITH B25,11
00466 PIO      CHECK IO1 FOR B25,11
00467 CI0002   CLEAR IO1
00470 PIO      CHECK IO1 FOR ZEROS
00471 PIO      CLEAR PIO ADR
00472          OP1,OP3,OP4
00473 CAL321   LOADS A1 TO A9
00474 SIE
00475 LDLC3    CLEAR DL
00476 CAL321   NA1=1,OA1=0
00477 SSL
00500 LDLC3    CLEAR DL
00501 CAL321   NA2=1,OA2=0
00502 SSL
00503 LDLC3    CLEAR DL
00504 CAL321   NA3=1,OA3=0
00505 SSL
00506 LDLC3    CLEAR DL
00507 CAL321   NA4=1,OA4=0
00510 SSL
00511 LDLC3    CLEAR DL
00512 CAL321   NA5=1,OA5=0
```

Figure 7-27. Self-Check Tape Instructions (Sheet 9)

Tape Word Count	Operation	Indication
00513	SSL	
00514	LDLC3	CLEAR DL
00515	CAL321	NA6=1,OA6=0
00516	SSL	
00517	LDLC3	CLEAR DL
00520	CAL321	NA7=1,OA7=0
00521	SSL	
00522	LDLC3	CLEARS DL
00523	CAL321	NA8=1,OA8=0
00524	SSL	
00525	LDLC3	CLEAR DL
00526	CAL321	NA9=1,OA9=0
00527	SSL	
00530	LDLC3	CLEAR DL
00531	CALO	NA1=0,OA1=1
00532	SSL	
00533	CALO	NA2=0,OA2=1
00534	SSL	
00535	CALO	NA3=0,OA3=1
00536	SSL	
00537	CALO	NA4=0,OA4=1
00540	SSL	
00541	CALO	NA5=0,OA5=1
00542	SSL	
00543	CALO	NA6=0,OA6=1
00544	SSL	
00545	CALO	NA7=0,OA7=1
00546	SSL	
00547	CALO	NA8=0,OA8=1
00550	SSL	
00551	CALO	NA9=0,OA9=1
00552	SSL	
00553	AND	NOP3=1,OP3=0
00554	SSL	
00555	SUB	NOP3=0,OP3=1
00556	SSL	
00557	HOP	NOP2=0,OP2=1
00560	SSL	
00561	DIV	NOP1=1,OP1=0

Figure 7-27. Self-Check Tape Instructions (Sheet 10)

```
Tape
Word Operation                          Indication
Count

00562 SSL
00563 PIO       NOP4=1,OP4=0
00564 SSL
00565 STO       NOP2=1,OP2=0
00566 SSL
00567 MPY       NOP4=0,OP4=1
00570 SSL
00571 TRA       NOP1=0,OP1=1
00572 SSL
00573 RIE       END OF INSDR TEST
00574           LOAD A1 TO A8    NO ERROR
00575 SIE
00576 CAL321    NA1=1,OA1=0
00577 SSL
00600 CAL321    NA2=1,OA2=0
00601 SSL
00602 CAL321    NA3=1,OA3=0
00603 SSL
00604 CAL321    NA4=1,OA4=0
00605 SSL
00606 CAL321    NA5=1,OA5=0
00607 SSL
00610 CAL321    NA6=1,OA6=0
00611 SSL
00612 CAL321    NA7=1,OA7=0
00613 SSL
00614 CAL321    NA8=1,OA8=0
00615 SSL
00616 CALO      NA1=0,OA1=1
00617 SSL
00620 CALO      NA2=0,OA2=1
00621 SSL
00622 CALO      NA3=0,OA3=1
00623 SSL
00624 CALO      NA4=0,OA3=1
00625 SSL
00626 CALO      NA5=0,OA5=1
00627 SSL
```

Figure 7-27. Self-Check Tape Instructions (Sheet 11)

```
Tape
Word Operation                          Indication
Count
00630 CALO     NA6=0,OA6=1
00631 SSL
00632 CALO     NA7=0,OA7=1
00633 SSL
00634 CALO     NA8=0,OA8=1
00635 SSL
00636 RIE      END OF IADR TEST
00637 LDLC3    LOAD DL WITH IM2,DM2,IS2,DS2
00640          CHECK SSMSC
00641 LDLC3    LOAD DL WITH B13
00642          CHECKS SSMSC
00643 LDLC3    LOAD DL WITH DDX,DS3
00644 SHFC1    CHECKS SSMSC   DM1,DS4
00645 SIE
00646 LDLC3    CLEAR DL
00647 LDLC3    SSMSC ERROR  DL CONTAINS ZEROS  TRS DDX=0  DSMSO DDX=1
00650 SSL
00651 PIO      LOAD IO1 WITH ZEROS
00652 PIO      CHECK IO1 FOR ZEROS    B9
00653 SSL
00654 LDLC3    LOAD DL WITH DS1
00655          SSMSC TRS ERROR   DSMSO=0  TRS HAS DS1
00656 SSL
00657          SSMSC HOPC1 ERROR   HOPC1=0  DSMSO HAS DS1
00660 SSL
00661 LDLC3    CLEAR DL
00662 LDLC3    SSMSC HOPC1 ERROR   DSMSO=0  HOPC1 HAS DS1   DL CONTAINS B5,25
00663 SSL
00664 PIO      LOAD IO1 WITH B5,25
00665 PIO      CHECK IO1 FOR B5,25
00666 SSL
00667          SSMSC HOPC1 ERROR   HOPC1=0  DSMSO HAS DS1   IO1 CONTAINS S TO B25
00670 SSL
00671 PIO      CHECKS IO1 FOR S TO B25
00672 SSL
00673 RIE
00674 LDLC3    CLEAR DL
00675 PIO      CLEAR IO1    END OF SSMSC TEST
00676 LDLC3    LOAD DL WITH IM1,DS3
```

Figure 7-27. Self-Check Tape Instructions (Sheet 12)

```
Tape
Word Operation                          Indication
Count

00677 CI0002,045  LOADS IO1 WITH B22,25
00700 PIO         CHECK IO1 FOR B22,25
00701 LDLC3       LOAD DL WITH IM2
00702 CI0002,051  LOAD IO1 WITH B11
00703 PIO         CHECK IO1 FOR B11
00704 CI0002      CLEAR IO1
00705 PIO         CHECK IO1 FOR ZEROS
00706 CI0002,045,051  LOADS IO1 WITH B11,17
00707 PIO         CHECK IO1 FOR B11,17
00710 LDLC3       CLEAR DL
00711 PIO         CLEAR IO1
00712 LDLC3       LOAD DL WITH ALL SECTORS,MODULES,DUPLEX,SYLLABLE
00713             CHECK SSMBR
00714 LDLC3       LOAD DL WITH IM2
00715 SIE
00716             SSMBR TRS ERROR     TRS=IM2  TRR=0
00717 SSL
00720 SHFC1       SSMBR TRS ERROR     TRS=IM3  TRR=0
00721 SSL
00722 SHFC1       SSMBR TRS ERROR     TRS=IS1  TRR=0
00723 SSL
00724 SHFC1       SSMBR TRS ERROR     TRS=IS2  TRR=0
00725 SSL
00726 SHFC1       SSMBR TRS ERROR     TRS=IS3  TRR=0
00727 SSL
00730 SHFC1       SSMBR TRS ERROR     TRS=IS4  TRR=0
00731 SSL
00732 SHFC1       SSMBR TRS ERROR     TRS=SYL  TRR=0
00733 SSL
00734 LDLC3       LOADS DL WITH DDX
00735             SSMBR TRS ERROR     TRS=DDX  TRR=0
00736 SSL
00737 SHFC1       SSMBR TRS ERROR     TRS=DM1  TRR=0
00740 SSL
00741 SHFC1       SSMBR TRS ERROR     TRS=DM2  TRR=0
00742 SSL
00743 SHFC1       SSMBR TRS ERROR     TRS=DM3  TRR=0
00744 SSL
```

Figure 7-27. Self-Check Tape Instructions (Sheet 13)

```
Tape
Word  Operation                          Indication
Count
00745 SHFC1   SSMBR TRS ERROR     TRS=DS1  TRR=0
00746 SSL
00747 SHFC1   SSMBR TRS ERROR     TRS=DS2  TRR=0
00750 SSL
00751 SHFC1   SSMBR TRS ERROR     TRS=DS3  TRR=0
00752 SSL
00753         SSMBR TRS ERROR     TRS=DS3  TRR=0
00754 SSL
00755 SHFC1   SSMBR TRS ERROR     TRS=DS4  TRR=0
00756 SSL
00757 SHFC1   SSMBR TRS ERROR     TRS=IDX  TRR=0
00760 SSL
00761 SHFC1   SSMBR TRS ERROR     TRS=IM1  TRR=0
00762 SSL
00763 RIE
00764 LDLC3   LOAD DL WITH  ALL SECTORS,MODULES,DUPLEX,SYLLABLE
00765         CHECK SSMDR
00766 SIE
00767 LDLC3   LOAD DL WITH IM2
00770         SSMBR TRS ERROR     TRS=0  TRR=DM2      IM2    HOPC1=IM2,DM2
00771 SSL
00772         SSMDR TRS ERROR     TRS=0  TRR=DM2      IM2    HOPC1=IM2,DM2
00773 SSL
00774 SHFC1   SSMBR TRS ERROR     TRS=0  TRR=DM3      IM3    HOPC1=IM3,DM3
00775 SSL
00776         SSMDR TRS ERROR     TRS=0  TRR=DM3      IM3    HOPC1=IM3,DM3
00777 SSL
01000 SHFC1   SSMBR TRS ERROR     TRS=0  TRR=DS1      IS1    HOPC1=IS1,DS1
01001 SSL
01002         SSMDR TRS ERROR     TRS=0  TRR=DS1      IS1    HOPC1=IS1,DS1
01003 SSL
01004 SHFC1   SSMBR TRS ERROR     TRS=0  TRR=DS2      IS2    HOPC1=IS2,DS2
01005 SSL
01006         SSMDR TRS ERROR     TRS=0  TRR=DS2      IS2    HOPC1=IS2,DS2
01007 SSL
01010 SHFC1   SSMBR TRS ERROR     TRS=0  TRR=DS3      IS3    HOPC1=IS3,DS3
01011 SSL
01012         SSMDR TRS ERROR     TRS=0  TRR=DS3      IS3    HOPC1=IS3,DS3
01013 SSL
```

Figure 7-27. Self-Check Tape Instructions (Sheet 14)

Tape Word Count	Operation	Indication				
01014	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=DS4	IS4	HOPC1=IS4,DS4
01015	SSL					
01016		SSMDR TRS ERROR	TRS=0	TRR=DS4	IS4	HOPC1=DS4,IS4
01017	SSL					
01020	LDLC3	LOAD DL WITH IDX,DDX				
01021		SSMBR TRS ERROR	TRS=0	TRR=SYL	IDX,DDX	HOPC1=IDX,DDX,SYL
01022	SSL					
01023		SSMDR TRS ERROR	TRS=0	TRR=SYL	IDX,DDX	HOPC1=IDX,DDX,SYL
01024	SSL					
01025	LDLC3	LOADS DL WITH SYL,IDX				
01026		SSMBR TRS ERROR	TRS=0	TRR=DDX	IDX,SYL	HOPC1=IDX,DDX,SYL
01027	SSL					
01030		SSMDR TRS ERROR	TRS=0	TRR=DDX	IDX,SYL	HOPC1=IDX,DDX,SYL
01031	SSL					
01032	LDLC3	LOAD DL WITH SYL,DDX				
01033		SSMBR TRS ERROR	TRS=0	TRR=IDX	DDX,SYL	HOPC1=IDX,DDX,SYL
01034	SSL					
01035		SSMDR TRS ERROR	TRS=0	TRR=IDX	DDX,SYL	HOPC1=IDX,DDX,SYL
01036	SSL					
01037	LDLC3	LOAD DL WITH DM1				
01040		SSMBR TRS ERROR	TRS=0	TRR=IM1	DM1	HOPC1=IM1,DM1
01041	SSL					
01042		SSMDR TRS ERROR	TRS=0	TRR=IM1	DM1	HOPC1=IM1,DM1
01043	SSL					
01044	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=IM2	DM2	HOPC1=IM2,DM2
01045	SSL					
01046		SSMDR TRS ERROR	TRS=0	TRR=IM2	DM2	HOPC1=IM2,DM2
01047	SSL					
01050	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=IM3	DM3	HOPC1=IM3,DM3
01051	SSL					
01052		SSMDR TRS ERROR	TRS=0	TRR=IM3	DM3	HOPC1=IM3,DM3
01053	SSL					
01054	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=IS1	DS1	HOPC1=IS1,DS1
01055	SSL					
01056		SSMDR TRS ERROR	TRS=0	TRR=IS1	DS1	HOPC1=IS1,DS1
01057	SSL					
01060	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=IS2	DS2	HOPC1=IS2,DS2
01061	SSL					

Figure 7-27. Self-Check Tape Instructions (Sheet 15)

Tape Word Count	Operation		Indication			
01062		SSMDR TRS ERROR	TRS=0	TRR=IS2	DS2	HOPC1=IS2,DS2
01063	SSL					
01064	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=IS3	DS3	HOPC1=IS3,DS3
01065	SSL					
01066		SSMDR TRS ERROR	TRS=0	TRR=IS3	DS3	HOPC1=IS3,DS3
01067	SSL					
01070	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=IS4	DS4	HOPC1=IS4,DS4
01071	SSL					
01072		SSMDR TRS ERROR	TRS=0	TRR=IS4	DS4	HOPC1=IS4,DS4
01073	SSL					
01074	SHFC1	SSMBR TRS ERROR	TRS=0	TRR=DM1	IM1	HOPC1=IM1,DM1
01075	SSL					
01076	SHFC1	SSMDR TRS ERROR	TRS=0	TRR=DM1	IM1	HOPC1=IM1,DM1
01077	SSL					
01100		SSMBR TRS ERROR				
01101	SSL					
01102	LDLC3	LOAD DL WITH IM2				
01103		SSMDR TRS ERROR	TRS=IM2	TRR=0		HOPC1=0
01104	SSL					
01105	SHFC1	SSMDR TRS ERROR	TRS=IM3	TRR=0		HOPC1=0
01106	SSL					
01107	SHFC1	SSMDR TRS ERROR	TRS=IS1	TRR=0		HOPC1=0
01110	SSL					
01111	SHFC1	SSMDR TRS ERROR	TRS=IS2	TRR=0		HOPC1=0
01112	SSL					
01113	SHFC1	SSMDR TRS ERROR	TRS=IS3	TRR=0		HOPC1=0
01114	SSL					
01115	SHFC1	SSMDR TRS ERROR	TRS=IS4	TRR=0		HOPC1=0
01116	SSL					
01117	SHFC1	SSMDR TRS ERROR	TRS=SYL	TRR=0		HOPC1=0
01120	SSL					
01121	LDLC3	LOAD DL WITH DX				
01122		SSMDR TRS ERROR	TRS=DDX	TRR=0		HOPC1=0
01123	SSL					
01124	SHFC1	SSMDR TRS ERROR	TRS=DM1	TRR=0		HOPC1=0
01125	SSL					
01126	SHFC1	SSMDR TRS ERROR	TRS=DM2	TRR=0		HOPC1=0
01127	SSL					
01130	SHFC1	SSMDR TRS ERROR	TRS=DM3	TRR=0		HOPC1=0

Figure 7-27. Self-Check Tape Instructions (Sheet 16)

```
Tape
Word  Operation                          Indication
Count

01131 SSL
01132 SHFC1    SSMDR TRS ERROR     TRS=DS1  TRR=0              HOPC1=0
01133 SSL
01134 SHFC1    SSMDR TRS ERROR     TRS=DS2  TRR=0              HOPC1=0
01135 SSL
01136 SHFC1    SSMDR TRS ERROR     TRS=DS3  TRR=0              HOPC1=0
01137 SSL
01140 SHFC1    SSMDR TRS ERROR     TRS=DS4  TRR=0              HOPC1=0
01141 SSL
01142 SHFC1    SSMDR TRS ERROR     TRS=IDX  TRR=0              HOPC1=0
01143 SSL
01144 SHFC1    SSMDR TRS ERROR     TRS=IM1  TRR=0              HOPC1=0
01145 SSL
01146 LDLC3    LOAD DL WITH IM1,DM1
01147          SSMBR HOPC1 ERROR   HOPC1=0  TRR=DM1,IM1  TRS=DM1,IM1
01150 SSL
01151          SSMDR HOPC1 ERROR   HOPC1=0  TRR=DM1,IM1  TRS=DM1,IM1
01152 SSL
01153          SSMBR HOPC1 ERROR   HOPC1=0  TRR=DM1,IM1  TRS=DM1,IM1
01154 SSL
01155          SSMBR HOPC1 ERROR   HOPC1=IM1,IM2,DM1  TRR=IM1,DM1  TRS=IM1,DM1
01156 SSL
01157          SSMDR HOPC1 ERROR   HOPC1=IM1,IM2,DM1  TRR=IM1,DM1  TRS=IM1,DM1
01160 SSL
01161 LDLC3    CLEAR DL
01162 RIE      END OF SSMBR AND SSMDR TESTS
01163          IO1 CONTAINS ZEROS       OP3
01164 PIO      CHECK IO1 FOR ZEROS
01165 LDLC3    LOAD DL WITH B25
01166          IO1 CONTAINS B25
01167 PIO      CHECK IO1 FOR B25
01170 LDLC3    CLEAR DL
01171 PIO      CHECK IO1 FOR B25
01172 LDLC3    LOAD DL WITH SIGN
01173          IO1 CONTAINS SIGN
01174 PIO      CHECK IO1 FOR SIGN
01175 SHFEXM,LDLC2  LOAD DL WITH S,B2 THEN CLEAR DL  IO1 CONTAINS B5,7
01176 PIO      CHECK IC1 FOR B5,7
```

Figure 7-27. Self-Check Tape Instructions (Sheet 17)

```
Tape
Word  Operation                          Indication
Count
01177 LDLC2    LOAD DL WITH S,B2 THEN CLEAR DL   IO1 CONTAINS S,B2
01200 PIO      CHECK IO1 FOR S,B2
01201 LDLC2,RSU  IO1 CONTAINS S,B2
01202 PIO      CHECK IO1 FOR S,B2
01203 LDLC2,IMI  IO1 CONTAINS S,B2
01204 PIO      CHECK IO1 FOR S,B2
01205 LDLC2,PIO  IO1 CONTAINS S,B2
01206 PIO      CHECK IO1 FOR S,B2
01207 LDLC2,ANC  IO1 CONTAINS S,B2
01210 PIO      CHECK IO1 FOR S,B2
01211 LDLC3    LOADS DL WITH S,B2
01212 SHF      IO1 CONTAINS S,B2
01213 PIO      CHECKS IO1 FOR S,B2
01214 SHF      IO1 CONTAINS S,B2
01215 PIO      CHECKS IO1 FOR S,B2
01216 CIO002,035  IO1 CONTAINS ZEROS
01217 PIO      CHECK IO1 FOR ZEROS
01220 CIO002,031  IO1 CONTAINS ZEROS
01221 PIO      CHECK IO1 FOR ZEROS
01222 LDLC3    CLEAR DL
01223 LDLC2    NO ERRORS
01224 CIO002   CLEARS IO1
01225 SIE
01226 LDLC3    CLEAR DL
01227 LDLC2    TRS SER ERROR     IO1=ZEROS  DD=S,B1,2,4
01230 SSL
01231 PIO      CHECK IO1 FOR ZEROS       2BDDTSO=S,B1,2,4
01232 SSL
01233 LDLC3    CLEARS DL
01234 LDLC2    TRS SER ERROR     DL=S,B1,2,4
01235 SSL
01236 PIO      CHECK IO1 FOR ZEROS       2BDDTSO=S,B1,3,4,5
01237 SSL
01240 LDLC3    CLEAR DL
01241 LDLC2    AI3 SER ERROR     IO1=S,B1,2,4
01242 SSL
01243 RIE
01244 PIO      CHECK IO1 FOR S,B1,2,4
01245 CIO002   CLEAR IO1
```

Figure 7-27. Self-Check Tape Instructions (Sheet 18)

```
Tape
Word Operation                          Indication
Count

01246 LDLC3   CLEAR DL
01247 SIE
01250 LDLC2,LDLC3  AI3 SER ERROR   IO1=S,B1,2,4
01251 SSL
01252 CIO002  CLEAR IO1
01253 LDLC3   CLEAR DL
01254 LDLC2   TRS SER ERROR    DD=S,B1,2,4
01255 SSL
01256 CIO002,035  IO1 CONTAINS B23,24,25
01257 RIE
01260 PIO     CHECK IO1 FOR B23,24,25
01261 SIE
01262 LDLC3   CLEAR DL
01263 LDLC2   TRS SER ERROR    DD=S,B1,2,4
01264 SSL
01265 CIO002,031  IO1 CONTAINS B5,6,7,9
01266 RIE
01267 PIO     CHECK IO1 FOR B5,6,7,9
01270 SIE
01271 LDLC3   CLEAR DL
01272         TRS SER ERROR    DD=S,B1,2,4
01273 SSL
01274 CIO002  IO1 CONTAINS ZEROS
01275 RIE
01276 PIO     CHECK IO1 FOR ZEROS
01277 SIE
01300 LDLC3   LOAD DL WITH DM1
01301         SSMSC TRS ERROR
01302 SSL
01303 CIO002,031  IO1 CONTAINS ZEROS
01304 RIE
01305 PIO     CHECK IO1 FOR ZEROS
01306 SIE
01307 LDLC3   CLEAR DL
01310 LDLC2,LDLC3  AI3 SER ERROR
01311 SSL
01312 CIO002,031  IO1 CONTAINS ZEROS
01313 RIE
```

Figure 7-27. Self-Check Tape Instructions (Sheet 19)

```
Tape
Word Operation                                  Indication
Count
01314 PIO      CHECK IO1 FOR ZEROS
01315 SIE
01316 LDLC3    LOAD DL WITH DM1
01317          SSMSC HOPC1 ERROR    DD=88
01320 SSL
01321 CI0002,031  IO1 CONTAINS 813
01322 RIE
01323 PIO      CHECK IO1 FOR 813
01324 LDLC3    CLEAR DL
01325 LDLC2    NO ERROR     28DDTSO=85,6,7,8      DTDRB25=85,6,7,8
01326 SIE
01327 LDLC3    CLEAR DL
01330          TRS PAR ERROR    DD=S,81,2,3       28DDTSO=0     DTDRB25=1 (S)
01331 SSL
01332 LDLC3    CLEAR DL
01333          TRS PAR ERROR    DD=S,81,2,3       28DDTSO=1(81) DTDRB25=0
01334 SSL
01335 RIE      END OF DD CHECKS
01336 LDLC2    LOAD DL WITH ZEROS
01337 CI0002,051  IO1 CONTAINS B20
01340 PIO      CHECK IO1 FOR B20
01341 LDLC3    CLEAR DL
01342 PIO      CLEAR IO1
01343 STO      SYL0=0  SYL1=0
01344 STO      SYL0=1  SYL1=0
01345          DM1    SYL0=0  SYL1=1
01346 CLA      SYL0=0  SYL1=1
01347 DIV      SYL0=0  SYL1=1
01350 XOR      SYL0=0  SYL1=1
01351 PIO      SYL0=0  SYL1=1
01352          SYL0=0  SYL1=0   DX
01353 BRA1B    SYL0=1  SYL1=0  BRB=0(0,1)  BRASYL1=0  BRASYL0=1
01354 BRA1C    SYL0=0  SYL1=1  BRB=0(0,1)  BRASYL1=1  BRASYL0=0
01355 BRB1B    SYL0=1  SYL1=0  BRA=0(0,1)  BRBSYL1=0  BRBSYL0=1   DM1
01356 BRB1C    SYL0=0  SYL1=1  BRA=0(0,1)  BRBSYL1=1  BRBSYL0=1   DM1
01357          SYL0=0  SYL1=0  BRA=0(0,1)  BRB=0(0,1)             DX
01360 BRA1B,BRA1C      SYL0=1  SYL1=1   BRA=1(0,1)  BRB=0(0,1)
01361 BRB1B,BRB1C      SYL0=1  SYL1=1   BRA=0(0,1)  BRB=1(0,1)    DM1
01362 STO      SYL0=0  SYL1=0  BRA=0(0,1)  BRB=0(0,1)             DX
```

Figure 7-27. Self-Check Tape Instructions (Sheet 20)

```
Tape
Word Operation                          Indication
Count

01363          SYL0=0  SYL1=1  BRASYL0=0  BRASYL1=1  BRBSYL0=0  BRBSYL1=1  DX
01364 STO      SYL0=0  SYL1=1  BRASYL0=0  BRASYL1=1  BRBSYL0=0  BRBSYL1=1  DX
01365          SYL0=1  SYL1=0  BRASYL0=1  BRASYL1=0  BRBSYL0=1  BRBSYL1=0  DX
01366 STO      SYL0=1  SYL1=0  BRASYL0=1  BRASYL1=0  BRBSYL0=1  BRBSYL1=0  DX
01367 SIE
01370 BRB1B,BRB1C  BR14 ERROR  SYL0=0  SYL1=0  BRA=0(0,1)  BRB=1(0,1)      DX
01371 SSL
01372 BRA1B,BRB1C  BR14 ERROR  SYL0=0  SYL1=0  BRA=1(0,1)  BRB=0(0,1)      DX DM1
01373 SSL
01374 BRA1C,BRB1B,BRB1C BR14 ERR  SYL0=1 SYL1=1 BRASYL0=0 BRASYL1=1 BRB=1(0,1)
01375 SSL
01376 BRA1B,BRB1B,BRB1C BR14 ERR  SYL0=1 SYL1=1 BRASYL0=1 BRASYL1=0 BRB=1(0,1)
01377 SSL
01400 BRA1B    BR14 ERROR  SYL0=0  SYL1=0  BRASYL0=1  BRASYL1=0  BRB=0(0,1)
01401 SSL
01402 BRA1C    BR14 ERROR  SYL0=0  SYL1=0  BRASYL0=0  BRASYL1=1  BRB=0(0,1)
01403 SSL                                              DM1 WILL BE ON FOR TEST 1404
01404 BRA1B,BRA1C,BRB1C BR14 ERR  SYL0=1 SYL1=1 BRA=1(0,1) BRBSYL0=0 BRBSYL1=1
01405 SSL                                              DM1 WILL BE ON FOR TEST 1406
01406 BRA1B,BRA1C,BRB1B BR14 ERR  SYL0=1 SYL1=1 BRA=1(0,1) BRBSYL0=1 BRBSYL1=0
01407 SSL
01410 BRB1B    BR14 ERROR  SYL0=0  SYL1=0  BRA=0(0,1)  BRBSYL0=1  BRBSYL1=0  DM1
01411 SSL
01412 BRB1C    BR14 ERROR  SYL0=0  SYL1=0  BRA=0(0,1)  BRBSYL0=0  BRBSYL1=1
01413 SSL
01414          BR14 ERROR  SYL0=0  SYL1=1  BRA=0(0,1)  BRB=0(0,1)
01415 SSL      END OF BRA,BRB TEST
01416 CI0022   SWITCH TO TMR
01417          THE NEXT FOUR TESTS ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
01420
01421
01422
01423 RIE      MAKE SURE NO ERROR EXISTS
01424 ST6
01425          NO ERRORS
01426 SIE
01427 EP1
01430 SSL
```

Figure 7-27. Self-Check Tape Instructions (Sheet 21)

```
Tape
Word Operation                          Indication
Count
01431 EP2
01432 SSL
01433 EP3
01434 SSL
01435 EP4
01436 SSL
01437 EP5
01440 SSL
01441 EP6
01442 SSL
01443 EP7
01444 SSL
01445 EP8
01446 SSL
01447 EP9
01450 SSL
01451 EP10
01452 SSL
01453 EP11
01454 SSL
01455 EP12
01456 SSL
01457 EP13
01460 SSL
01461 CI0056  SWITCH OUT OF TMR
01462         THE NEXT FOUR TESTS ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
01463
01464
01465
01466 RIE
01467 EP1     READER SHOULD NOT STOP
01470 RIE
01471 CI0022  SWITCH TO TMR
01472         THE NEXT FOUR TEST ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
01473
01474
01475
01476 SSL     END OF DISAGREEMENT ERROR TEST
01477 LDLC3   LOAD  DL WITH B3,4,8,9
```

Figure 7-27. Self-Check Tape Instructions (Sheet 22)

```
Tape
Word Operation                          Indication
Count

01500 PIO      LOAD IO1 WITH B3,4,8,9
01501 CIO001,0C6  LOAD IO2 WITH B3,4,8,9
01502 LDLC3    LOAD DL WITH B3,4,8,9,17,18,22,23
01503 RIE
01504 FPIO     NO ERRORS
01505 LDLC3    LOAD DL WITH ONES
01506 PIO      LOAD IO1 WITH ONES
01507 CIO001,0C6  LOAD IO2 WITH ONES
01510 LDLC3    LOAD DL WITH B1 TO 9,17,18,22,23
01511 FPIO,CSVE12  TRS VEDT3  VT8  SVP1 INTO IO1   A3 TRS ERROR
01512 SSL
01513 FPIO     CHECK IO1 FOR SVP1   ERROR
01514 SSL
01515 FPIO,CSVE3   TRS VEDT3  VT5  SVP1 INTO IO1   A3 TRS ERROR
01516 SSL
01517 FPIO     CHECK IO1 FOR SVP1   ERROR
01520 SSL
01521 FPIO,CSVE31  TRS VEDT5  VT7  SVP1 INTO IO1   A2 TRS ERROR
01522 SSL
01523 FPIO     CHECK IO1 FOR SVP1   ERROR
01524 SSL
01525 FPIO,CSVE2   TRS VEDT6  VT4  SVP1 INTO IO1   A2 TRS ERROR
01526 SSL
01527 FPIO     CHECK IO1 FOR SVP1   ERROR
01530 SSL
01531 FPIO,CSVE32  TRS VEDT7  VT6  SVP1 INTO IO1   A1 TRS ERROR
01532 SSL
01533 FPIO     CHECK IO1 FOR SVP1   ERROR
01534 SSL
01535 FPIO,CSVE1   TRS VEDT8  VT3  SVP1 INTO IO1   A1 TRS ERROR
01536 SSL
01537 FPIO     CHECK IO1 FOR SVP1   ERROR
01540 SSL      END OF TRS VED AND VOTER TESTS
01541 LDLC3    LOAD DL WITH B3,4,8,9,17 TO 23
01542 FPIO,CSVE21  AI3 VEDT3  VT8  SVP2 INTO IO1   A3 AI3 ERROR
01543 SSL
01544 FPIO     CHECK IO1 FOR SVP2   ERROR
01545 SSL
```

Figure 7-27. Self-Check Tape Instructions (Sheet 23)

```
Tape
Word  Operation                                  Indication
Count
01546 FPIO,CSVE3   AI3 VEDT4  VT5  SVP2 INTO IO1   A3 AI3 ERROR
01547 SSL
01550 FPIO     CHECK IO1 FOR SVP2   ERROR
01551 SSL
01552 FPIO,CSVE31  AI3 VEDT5  VT7  SVP2 INTO IO1   A2 AI3 ERROR
01553 SSL
01554 FPIO     CHECK IO1 FOR SVP2   ERROR
01555 SSL
01556 FPIO,CSVE2   AI3 VEDT6  VT4  SVP2 INTO IO1   A2 AI3 ERROR
01557 SSL
01560 FPIO     CHECKS IO1 FOR SVP2  ERROR
01561 SSL
01562 FPIO,CSVE32  AI3 VEDT7  VT6  SVP2 INTO IO1   A1 AI3 ERROR
01563 SSL
01564 FPIO     CHECK IO1 FOR SVP2   ERROR
01565 SSL
01566 FPIO,CSVE1   AI3 VEDT8  VT3  SVP2 INTO IO1   A1 AI3 ERROR
01567 SSL
01570 FPIO     CHECK IO1 FOR SVP2  ERROR
01571 SSL
01572 LDLC3    LOAD DL WITH ONES
01573 LDLC3,FPIO,CSVE21  PRO VEDT3  VT8  SVP3 INTO DL  A3 PRO ERROR
01574 SSL
01575 FPIO     LOAD IO1 WITH SVP3
01576 FPIO     CHECK IO1 FOR SVP3  ERROR
01577 SSL
01600 LDLC3    LOAD DL WITH ONES
01601 LDLC3,FPIO,CSVE3   PRO VEDT4  VT5  SVP3 INTO DL  A3 PRO ERROR
01602 SSL
01603 FPIO     LOAD IO1 WITH SVP3
01604 FPIO     CHECK IO1 FOR SVP3  ERROR
01605 SSL
01606 LDLC3    LOAD DL WITH ONES
01607 LDLC3,FPIO,CSVE31  PRO VEDT5  VT7  SVP3 INTO DL  A2 PRO ERROR
01610 SSL
01611 FPIO     LOAD IO1 WITH SVP3
01612 FPIO     CHECK IO1 FOR SVP3   ERROR
01613 SSL
01614 LDLC3    LOAD DL WITH ONES
```

Figure 7-27. Self-Check Tape Instructions (Sheet 24)

```
Tape
Word Operation                                  Indication
Count

01615 LDLC3,FPIO,CSVE2   PRO VEDT6  VT4  SVP3 INTO DL  A2 PRO ERROR
01616 SSL
01617 FPIO     LOAD IO1 WITH SVP3
01620 FPIO     CHECK IO1 FOR SVP3   ERROR
01621 SSL
01622 LDLC3    LOAD DL WITH ONES
01623 LDLC3,FPIO,CSVE32  PRO VEDT7  VT6  SVP3 INTO DL  A1 PRO ERROR
01624 SSL
01625 FPIO     LOAD IO1 WITH SVP3
01626 FPIO     CHECK IO1 FOR SVP3   ERROR
01627 SSL
01630 LDLC3    LOAD DL WITH ONES
01631 LDLC3,FPIO,CSVE1   PRO VEDT8  VT3  SVP3 INTO DL  A1 PRO ERROR
01632 SSL
01633 FPIO     LOAD IO1 WITH SVP3
01634 FPIO     CHECK IO1 FOR SVP3   ERROR
01635 SSL
01636 LDLC3    LOAD DL WITH B3,4,8,9
01637 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
01640 FPIO,CSVE21  MD7 VEDT3   A3 MD7 ERROR
01641 SSL
01642 LDLC3    LOAD DL WITH B3,4,8,9
01643 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
01644 FPIO,CSVE3   MD7 VEDT7   A3 MD7 ERROR
 1645 SSL
 1646 LDLC3    LOAD DL WITH B3,4,8,9
 1647 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
 1650 FPIO,CSVE31  MD7 VEDT5  A2 MD7 ERROR
 1651 SSL
 1652 LDLC3    LOAD DL WITH B3,4,8,9
 1653 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
 1654 FPIO,CSVE2   MD7 VEDT6  A2 MD7 ERROR
 1655 SSL
 1656 LDLC3    LOAD DL WITH B3,4,8,9
 1657 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
 1660 FPIO,CSVE32  MD7 VEDT7  A1 MD7 ERROR
 1661 SSL
 1662 LDLC3    LOAD DL WITH B3,4,8,9
```

Figure 7-27. Self-Check Tape Instructions (Sheet 25)

```
Tape
Word Operation                          Indication
Count
1663 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
1664 FPIO,CSVE1   MD7 VEDT8  A1 MD7 ERROR
1665 SSL
1666 LDLC3   LOAD DL WITH B3,4,8,9
1667 FPIO,LDLC3  LOAD IO1 WITH B3,4,8,9  LOAD DL WITH ONES
1670 CI0001,0C6  LOAD IO2 WITH B3,4,8,9
1671 PIO     LOAD IO1 WITH ONES
1672 FPIO,CSVE21  MR1 VEDT3  A3 MR1 ERROR
1673 SSL
1674 FPIO,CSVE3   MR1 VEDT4  A3 MR1 ERROR
1675 SSL
1676 FPIO,CSVE31  MR1 VEDT5  A2 MR1 ERROR
1677 SSL
1700 FPIO,CSVE2   MR1 VEDT6  A2 MR1 ERROR
1701 SSL
1702 FPIO,CSVE32  MR1 VEDT7  A1 MR1 ERROR
1703 SSL
1704 FPIO,CSVE1   MR1 VEDT8  A1 MR1 ERROR
1705 SSL
1706 LDLC3   CLEAR DL
1707 FPIO,LDLC3   CLEAR IO1   LOAD DL WITH SIGN TO B24
1710 CI0001,0C6   CLEAR IO2
1711 FPIO1   PIO VEDT8  VT3  IO1 CONTAINS ZEROS   A1 PIO ERROR
1712 SSL
1713 FPIO    CHECK IO1 FOR ZEROS    ERROR
1714 SSL
1715 FPIO2   PIO VEDT7  VT4  IO1 CONTAINS ZEROS   A2 PIO ERROR
1716 SSL
1717 FPIO    CHECK IO1 FOR ZEROS    ERROR
1720 SSL
1721 FPIO3   PIO VEDT6  VT5  IO1 CONTAINS ZEROS   A3 PIO ERROR
1722 SSL
1723 FPIO    CHECK IO1 FOR ZEROS    ERROR
1724 SSL
1725 FPIO32  PIO VEDT7  VT6  IO1 CONTAINS B1 TO B24   A1 PIO ERROR
1726 SSL
1727 FPIO    CHECK IO1 FOR B1 TO B24    ERROR
1730 SSL
1731 CI0002  CLEAR IO1
```

Figure 7-27. Self-Check Tape Instructions (Sheet 26)

```
Tape
Word Operation                          Indication
Count

1732 FPI031   PIO VEDT5  VT7  IO1 CONTAINS B1 TO B24   A2 PIO ERROR
1733 SSL
1734 FPIO     CHECK IC1 FOR B1 TO B24    ERROR
1735 SSL
1736 CI0002   CLEAR IO1
1737 FPI021   PIO VEDT3  VT8  IO1 CONTAINS B1 TO B24  A3 PIO ERROR
1740 SSL
1741 FPIO     CHECKS IO1 FOR B1 TO B24    ERROR
1742 SSL
1743 CI0001,0C6  LOAD IO2 WITH B1 TO B24
1744 FPIO,CSVE21  HOPC1 VEDT3  A3 HOPC1 ERROR
1745 SSL
1746 FPIO,CSVE3   HOPC1 VEDT4  A3 HOPC1 ERROR
1747 SSL
1750 FPIO,CSVE31  HOPC1 VEDT5  A2 HOPC1 ERROR
1751 SSL
1752 FPIO,CSVE2   HOPC1 VEDT6  A2 HOPC1 ERROR
1753 SSL
1754 FPIO,CSVE32  HOPC1 VEDT7  A1 HOPC1 ERROR
1755 SSL
1756 FPIO,CSVE1   HOPC1 VEDT8  A1 HOPC1 ERROR
1757 SSL
1760 RIE
1761 RT6
1762 LDLC3    LOAD DL WITH ONES       CA1,CA2,ETC.
1763 PIO      LOAD IO1 WITH ONES
1764 CI0001,0C6  LOAD IO2 WITH ONES
1765 ST6
1766 FPIO,CSVE321  NO ERRORS
1767 FPIO,CSVE321  NO ERRORS
1770 LDLC3    CLEAR DL
1771 CI0002,0C6  CLEAR IO1 AND IO2
1772 SIE      TAADR6,5NOT,4,3NOT,2NOT,1NOT
1773 RIE
1774 RIE
1775 ST6
1776 LDLC3    LOAD DL WITH ONES
1777 PIC      LOAD IC1 WITH ONES
```

Figure 7-27. Self-Check Tape Instructions (Sheet 27)

```
Tape
Word Operation                          Indication
Count
2000 C10001,006  LOAD IO2 WITH ONES
2001 FPIO,LDLC3,CSVE321  NO ERROR  LOAD DL WITH B1 TO B7 AND B17 TO B23
2002 PIO      LOAD IO1 WITH B1 TO B7 AND B17 TO B23
2003 RT6
2004 PIO      CHECK IO1 FOR B1 TO B7 AND B17 TO B23
2005 ST6
2006 C10002,006  CLEAR IO1 AND IO2
2007 LDLC3    LOAD DL WITH SIGN
2010 STO      IO1 CONTAINS ZEROS
2011 RT6
2012 PIO      CHECK IO1 FOR ZEROS
2013 ST6
2014 TRA      IO1 CONTAINS ZEROS
2015 RT6
2016 PIO      CHECK IO1 FOR ZEROS
2017 ST6
2020 SHF      IO1 CONTAINS ZEROS
2021 RT6
2022 PIO      CHECK IO1 FOR ZEROS
2023 ST6
2024 SUB      IO1 CONTAINS ZEROS
2025 RT6
2026 PIO      CHECK IO1 FOR ZEROS
2027 ST6
2030          TAADR6,5NOT,4NOT,3NOT,2,1NOT  0A4        CHECK HELP NOT
2031          TAADR6,5NOT,4NOT,3,2,1
2032 LDLC3    LOAD DL WITH ONES
2033 PIO      LOAD IO1 WITH ONES
2024 C10001,006  LOAD IO2 WITH ONES
2035          TAADR6,5NOT,4,3NOT,2,1   0A3
2036          TAADR6,5,4NOT,3NOT,2,1   0A4
2037 RT6
2040          TAADR6NOT,5NOT,4NOT,3NOT,2,1
2041 RT6
2042          TAADR6NOT,5NOT,4NOT,3,2NOT,1       CHECK LEMMON 1
2043          TAADR6NOT,5NOT,4NOT,3,2,1NOT
2044          TAADR6NOT,5NOT,4,3,2NOT,1NOT
2045          TAATR6NOT,5,4NOT,3,2NOT,1NOT
2046 ST6
```

Figure 7-27. Self-Check Tape Instructions (Sheet 28)

```
Tape
Word Operation                          Indication
Count

2047          TAADR6,5NOT,4NOT,3,2NOT,1NOT
2050 RT6      TAADR6NOT,5NOT,4NOT,3,2NOT,1NOT
2051 SIE
2052 LDLC2    LOAD DL WITH SIGN          A1 AOC ERROR
2053 SSL
2054 RIE
2055 PIO      LOAD IO1 WITH SIGN
2056 PIO      CHECK IO1 FOR SIGN
2057 SIE      CHECK SC ADDRESS
2060 LDLC3    CLEAR DL
2061 CAL3,LDLC2  A3 AOC ERROR   LOAD DL WITH SIGN
2062 SSL
2063 RIE
2064 PIO      LOAD IO1 WITH SIGN
2065 PIO      CHECK IO1 FOR SIGN
2066 ST6      TAADR6NOT,5NOT,4,3NOT,2NOT,1NOT
2067 RIE      TAADR6NOT,5NOT,4NOT,3,2,1
2070 RIE
2071 ST6
2072 LDLC3    CLEAR DL
2073 SIE      TAADR6,5NOT,4,3NOT,2NOT,1NOT
2074 RIE
2075 RT6
2076          TAADR6NOT,5NOT,4,3NOT,2NOT,1
2077 LDLC3    CLEAR DL
2100          TAADR6NOT,5NOT,4,3NOT,2,1NOT
2101 LDLC3    CLEAR DL
2102          TAADR6NOT,5NOT,4,3,2NOT,1NOT
2103 LDLC3    CLEAR DL
2104          TAADR6NOT,5NOT,4NOT,3NOT,2NOT,1NOT   OA1
2105          TAADR6NOT,5,4,3NOT,2NOT,1NOT    OA1 OA4
2106          TAADR6NOT,5,4NOT,3NOT,2NO1,1NOT   OA1,2,3    CHECK SCOP CODES
2107 ST6
2110          TAADR6,5,4NOT,3NOT,2NOT,1NOT   OA1,2,3
2111 RT6
2112 LDLC3    CLEAR DL
2113 PIO      CLEAR IO1
2114 LDLC3    LOAD DL WITH SIGN,B8
```

Figure 7-27. Self-Check Tape Instructions (Sheet 29)

```
Tape
Word Operation                          Indication
Count
2115          IO1 CONTAINS ZEROS
2116 PIO      CHECK IO1 FOR ZEROS
2117 LDLC3    CLEAR DL
2120          TAADR6NOT,5NOT,4NOT,3,2,1
2121          TAADR6NOT,5NOT,4,3,2NOT,1NOT
2122 LDLC3    CLEAR DL
2123          TAADR6NOT,5NOT,4NOT,3,2,1
2124 ST6
2125          TAADR6,5,4NOT,3NOT,2NOT,1NOT   0A9 0A8
2126 RT6
2127 SIE      CHECKING IE LATCH
2130          SSMSC TRS ERROR
2131          TAADR5NOT,4NOT,3,2NOT,1
2132 SSL
2133          SSMSC TRS ERROR
2134          TAADR5NOT,4NOT,3NOT,2,1
2135 SSL
2136          SSMSC TRS ERROR
2137          TAADR5NOT,4,3,2,1
2140 SSL
2141          SSMSC TRS ERROR
2142          TAADR5,4NOT,3,2,1
2143 SSL
2144 RIE
2145 RT6
2146          TAADR5NOT,4NOT,3,2NOT,1        CHECKING TAADRC LATCH
2147          TAADR5,4NOT,3NOT,2NOT,1NOT     0A1
2150          TAADR5NOT,4NOT,3,2,1NOT
2151          TAADR5,4NOT,3NOT,2NOT,1NOT     0A1
2152          TAADR5NOT,4NOT,3NOT,2NOT,1NOT
2153          TAADR5,4NOT,3NOT,2NOT,1NOT     0A1
2154          TAADR5NOT,4,3,2NOT,1NOT
2155          TAADR5,4NOT,3NOT,2NOl,1NOT     0A1
2156          TAADR5,4NOT,3,2NOT,1NOT
2157          TAADR5,4NOT,3NOT,2NOT,1NOT     0A1
2160 ST6      TAADR5NOT,4NOT,3NOT,2,1        0A1
2161 PIO      CLEAR PIO ADR
2162          TAADR6,5NOT,4NOT,3NOT,2,1NOT
2163          TAADR6,5NOT,4NOT,3NOT,2,1NOT 0A1
```

Figure 7-27. Self-Check Tape Instructions (Sheet 30)

```
Tape
Word Operation                                  Indication
Count

2164          TAADR6,5NOT,4NOT,3,2,1
2165          TAADR6,5NOT,4NOT,3NOT,2,1NOT OA1
2166 LDLC3    LOAD DL WITH ONES
2167 PIO      LOAD IO1 WITH ONES
2170 CIOOO1,006  LOAD IO2 WITH ONES
2171          TAADR6,5NOT,4,3NOT,2,1
2172          TAADR6,5NOT,4NOT,3NOT,2,1NOT OA1
2173          TAADR6,5,4NOT,3NOT,2,1
2174          TAADR6,5NOT,4NOT,3NOT,2,1NOT OA1
2175 LDLC3    CLEAR DL
2176 PIO      CLEAR IO1
2177 CIOOO6   CLEAR IO2
2200 RT6      END OF SC CIRCUITS TEST
2201 SIE
2202 ST6
2203 COP21,ADD  OP4 VEDT3     A3 AOC ERROR
2204 SSL
2205 COP3,ADD   OP4 VEDT4     A3 AOC ERROR
2206 SSL
2207 COP31,ADD  OP4 VEDT5     A2 AOC ERROR
2210 SSL
2211 COP2,ADD   OP4 VEDT6     A2 AOC ERROR
2212 SSL
2213 COP32,ADD  OP4 VEDT7     A1 AOC ERROR
2214 SSL
2215 COP1,ADD   OP4 VEDT8     A1 AOC ERROR
2216 SSL
2217 COP21,STO  OP3 VEDT3     A3 AOC ERROR
2220 SSL
2221 COP3,STO   OP3 VEDT4     A3 AOC ERROR
2222 SSL
2223 COP31,STO  OP3 VEDT5     A2 AOC ERROR
2224 SSL
2225 COP2,STO   OP3 VEDT6     A2 AOC ERROR
2226 SSL
2227 COP32,STO  OP3 VEDT7     A1 AOC ERROR
2230 SSL
2231 COP1,STO   OP3 VEDT8     A1 AOC ERROR
```

Figure 7-27. Self-Check Tape Instructions (Sheet 31)

Tape Word Count	Operation		Indication
2232	SSL		
2233	COP21,RSU	OP2 VEDT3	A3 AOC ERROR
2234	SSL		
2235	COP3,RSU	OP2 VEDT4	A3 AOC ERROR
2236	SSL		
2237	COP31,RSU	OP2 VEDT5	A2 AOC ERROR
2240	SSL		
2241	COP2,RSU	OP2 VEDT6	A2 AOC ERROR
2242	SSL		
2243	COP32,RSU	OP2 VEDT7	A1 AOC ERROR
2244	SSL		
2245	COP1,RSU	OP2 VEDT8	A1 AOC ERROR
2246	SSL		
2247	COP21,SHF	OP1 VEDT3	A3 AOC ERROR
2250	SSL		
2251	COP3,SHF	OP1 VEDT4	A3 AOC ERROR
2252	SSL		
2253	COP31,SHF	OP1 VEDT5	A2 AOC ERROR
2254	SSL		
2255	COP2,SHF	OP1 VEDT6	A2 AOC ERROR
2256	SSL		
2257	COP32,SHH	OP1 VEDT7	A1 AOC ERROR
2260	SSL		
2261	COP1,SHF	OP1 VEDT8	A1 AOC ERROR
2262	SSL	END OF OP1 VED TESTS	
2263	RT6		
2264	PEA	EAM ERROR	
2265	SSL		
2266	PEA	EAM ERROR	
2267	SSS		
2270	PEA	EAM ERROR	
2271	SSL		
2272	PEA	EAM ERROR	
2273	SSL		
2274	PEA	EAM ERROR	
2275	SSL		
2276	PEA	EAM ERROR	
2277	SSL		
2300	PEB	EBM ERROR	

Figure 7-27. Self-Check Tape Instructions (Sheet 32)

```
Tape
Word Operation                                  Indication
Count

2301 SSL
2302 PEB      EBM ERROR
2303 SSL
2304 PEB      EBM ERROR
2305 SSL
2306 PEB      EBM ERROR
2307 SSL
2310 PEB      EBM ERROR
2311 SSL
2312 PEB      EBM ERROR
2313 SSL
2314 PEL1,PEL2   TLC VEDT3     A3 TLC   TLC ERRORS
2315 SSL
2316 PEL3        TLC VEDT4     A3 TLC   TLC ERRORS
2317 SSL
2320 PEL3,PEL1   TLC VEDT5     A2 TLC   TLC ERRORS
2321 SSL
2322 PEL2        TLC VEDT6     A2 TLC   TLC ERRORS
2323 SSL
2324 PEL2,PEL3   TLC VEDT7     A1 TLC   TLC ERRORS
2325 SSL
2326 PEL1        TLC VEDT8     A1 TLC   TLC ERRORS
2327 SSL      END OF TLC VED TESTS
2330 CAL21       A2 VEDT3      A3 AOC ERROR    TROA2=0
2331 SSL
2332 CAL3        A2 VEDT4      A3 AOC ERROR    TROA2=0
2333 SSL
2334 CAL31       A2 VEDT5      A2 AOC ERROR    TROA2=0
2335 SSL
2336 CAL2        A2 VEDT6      A2 AOC ERROR    TROA2=0
2337 SSL
2340 CAL32       A2 VEDT7      A1 AOC ERROR    TROA2=0
2341 SSL
2342 CAL1        A2 VEDT8      A1 AOC ERROR    TROA2=0
2343 SSL      END OF A2 VED TESTS
2344 CAL21       A1 VEDT3      A3 AOC ERROR    TROA1=0
2345 SSL
2346 CALC        A1 VEDT4      A3 AOC ERROR    TROA1=0
```

Figure 7-27. Self-Check Tape Instructions (Sheet 33)

Tape Word Count	Operation		Indication	
2347	SSL			
2350	CAL31	A1 VEDT5	A2 AOC ERROR	TROA1=0
2351	SSL			
2352	CAL2	A1 VEDT6	A2 AOC ERROR	TROA1=0
2353	SSL			
2354	CAL32	A1 VEDT7	A1 AOC ERROR	TROA1=0
2355	SSL			
2356	CAL1	A1 VEDT8	A1 AOC ERROR	TROA1=0
2357	SSL	END OF A1 VED TESTS		
2360	CAL21	A3 VEDT3	A3 AOC ERROR	TROA3=0
2361	SSL			
2362	CAL3	A3 VEDT4	A3 AOC ERROR	TROA3=0
2363	SSL			
2364	CAL31	A3 VEDT5	A2 AOC ERROR	TROA3=0
2365	SSL			
2366	CAL2	A3 VEDT6	A2 AOC ERROR	TROA3=0
2367	SSL			
2370	CAL32	A3 VEDT7	A1 AOC ERROR	TROA3=0
2371	SSL			
2372	CAL1	A3 VEDT8	A1 AOC ERROR	TROA3=0
2373	SSL	END OF A3 VED TESTS		
2374	CAL21	A4 VEDT3	A3 AOC ERROR	TROA4=0
2375	SSL			
2376	CAL3	A4 VEDT4	A3 AOC ERROR	TROA4=0
2377	SSL			
2400	CAL31	A4 VEDT5	A2 AOC ERROR	TROA4=0
2401	SSL			
2402	CAL2	A4 VEDT6	A2 AOC ERROR	TROA4=0
2403	SSL			
2404	CAL32	A4 VEDT7	A1 AOC ERROR	TROA4=0
2405	SSL			
2406	CAL1	A4 VEDT8	A1 AOC ERROR	TROA4=0
2407	SSL	END OF A4 VED TESTS		
2410	CAL21	A5 VEDT3	A3 AOC ERROR	TROA5=0
2411	SSL			
2412	CAL3	A5 VEDT4	A3 AOC ERROR	TROA5=0
2413	SSL			
2414	CAL31	A5 VEDT5	A2 AOC ERROR	TROA5=0
2415	SSL			

Figure 7-27. Self-Check Tape Instructions (Sheet 34)

Tape Word Count	Operation		Indication	
2416	CAL2	A5 VEDT6	A2 AOC ERROR	TROA5=0
2417	SSL			
2420	CAL32	A5 VEDT7	A1 AOC ERROR	TROA5=0
2421	SSL			
2422	CAL1	A5 VEDT8	A1 AOC ERROR	TROA5=0
2423	SSL	END OF A5 VED TESTS		
2424	CAL21	A6 VEDT3	A3 AOC ERROR	TROA6=0
2425	SSL			
2426	CAL3	A6 VEDT4	A3 AOC ERROR	TROA6=0
2427	SSL			
2430	CAL31	A6 VEDT5	A2 AOC ERROR	TROA6=0
2431	SSL			
2432	CAL2	A6 VEDT6	A2 AOC ERROR	TROA6=0
2433	SSL			
2434	CAL32	A6 VEDT7	A1 AOC ERROR	TROA6=0
2435	SSL			
2436	CAL1	A6 VEDT8	A1 AOC ERROR	TROA6=0
2437	SSL	END OF A6 VED TESTS		
2440	CAL21	A7 VEDT3	A3 AOC ERROR	TROA7=0
2441	SSL			
2442	CAL3	A7 VEDT4	A3 AOC ERROR	TROA7=0
2443	SSL			
2444	CAL31	A7 VEDT5	A2 AOC ERROR	TROA7=0
2445	SSL			
2446	CAL2	A7 VEDT6	A2 AOC ERROR	TROA7=0
2447	SSL			
2450	CAL32	A7 VEDT7	A1 AOC ERROR	TROA7=0
2451	SSL			
2452	CAL1	A7 VEDT8	A1 AOC ERROR	TROA7=0
2453	SSL	END OF A7 VED TESTS		
2454	CAL21	A8 VEDT3	A3 AOC ERROR	TROA8=0
2455	SSL			
2456	CAL3	A8 VEDT4	A3 AOC ERROR	TROA8=0
2457	SSL			
2460	CAL31	A8 VEDT5	A2 AOC ERROR	TROA8=0
2461	SSL			
2462	CAL2	A8 VEDT6	A2 AOC ERROR	TROA8=0
2463	SSL			

Figure 7-27. Self-Check Tape Instructions (Sheet 35)

```
Tape
Word Operation                          Indication
Count
2464 CAL32       A8 VEDT7      A1 AOC ERROR    TROA8=0
2465 SSL
2466 CAL1        A8 VEDT8      A1 AOC ERROR    TROA8=0
2467 SSL      END OF A8 VED TESTS
2470 CAL21       A9 VEDT3      A3 AOC ERROR    TROA9=0
2471 SSL
2472 CAL3        A9 VEDT4      A3 AOC ERROR    TROA9=0
2473 SSL
2474 CAL31       A9 VEDT5      A2 AOC ERROR    TROA9=0
2475 SSL
2476 CAL2        A9 VEDT6      A2 AOC ERROR    TROA9=0
2477 SSL
2500 CAL32       A9 VEDT7      A1 AOC ERROR    TROA9=0
2501 SSL
2502 CAL1        A9 VEDT8      A1 AOC ERROR    TROA9=0
2503 SSL      END OF A9 VED TESTS
2504 RIE
2505 CI0002,0C6  CLEAR IO1 AND IO2
2506 LDLC3    CLEAR DL
2507 ST6
2510 FPIO     IO1 CONTAINS ZEROS
2511 RIE
2512 FPIO     CHECK IO1 FOR ZEROS
2513 RIE
2514 LDLC3    LOAD DL WITH B1
2515 RT6
2516          LOAD IO1 WITH B1
2517 CI0001,0C6  LOAD IO2 WITH B1
2520 LDLC3    CLEAR DL
2521 PIO      CP3  0A9  0A8  0A3    IO1 CONTAINS SIGN,B2
2522 PIO      CHECK IO1 FOR SIGN,B2
2523 LDLC3    CLEAR DL
2524 ST6
2525 FPIO     IO1 CONTAINS ZEROS        0A3
2526 RIE
2527 RT6
2530 PIO      CHECK IO1 FOR ZEROS
2531 PIO      IO1 CONTAINS ZEROS
2532 PIO      CHECK IO1 FOR ZEROS
```

Figure 7-27. Self-Check Tape Instructions (Sheet 36)

```
Tape
Word Operation                          Indication
Count

2533 LDLC3    LOAD DL WITH SIGN,B1,25
2534 PIO      LOAD IO1 WITH SIGN,B1,25
2535 CI0001,006  LOAD IO2 WITH SIGN,B1,25
2536 LDLC3    CLEAR DL
2537 ST6
2540 FPIO     CA9  OP3    IO1 CONTAINS SIGN,B1
2541 RIE
2542 FPIO     CHECK IO1 FOR SIGN,B1
2543 RIE
2544          IO1 CONTAINS ZEROS
2545 FPIO     CHECK IO1 FOR ZEROS
2546 RIE
2547 FPIO     CP3  0A8  0A3    IO1 CONTAINS SIGN,B1
2550 RIE
2551 FPIO     CHECK IO1 FOR SIGN,B1
2552 RIE
2553 PIO      CP3  0A9    IO1 CONTAINS ZEROS
2554 FPIO     CHECK IO1 FOR ZEROS
2555 CI0022   SELECT TMR
2556          THE NEXT FOUR TESTS ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
2557
2560
2561
2562 RIE
2563          CP3  0A4  0A3    IO1 CONTAINS ZEROS
2564 RT6
2565 PIO      CHECK IO1 FOR ZEROS
2566          CP3  0A9  0A1    IO1 CONTAINS SIGN,B2
2567 PIO      CHECK IO1 FOR SIGN,B2
2570 ST6
2571          CP3  0A4  0A3    IO1 CONTAINS B19
2572 RIE
2573 RT6
2574 PIO      CHECKS IO1 FOR B19
2575 ST6
2576          CP3  0A3         IO1 CONTAINS ZEROS
2577 RIE
2600 RT6
```

Figure 7-27. Self-Check Tape Instructions (Sheet 37)

```
Tape
Word Operation                          Indication
Count
2601 PIO      CHECK IO1 FOR ZEROS
2602 ST6
2603          OP3  CA4          IO1 CONTAINS ZEROS
2604 RIE
2605 RT6
2606 PIO      CHECK IO1 FOR ZEROS
2607 SIE
2610 CI0056   SWITCH TO SIMPLEX
2611          THE NEXT FOUR TESTS ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
2612
2613
2614
2615 RIE
2616 ST6
2617 FPIO      OP3  OA8      IO1 CONTAINS ZEROS
2620 RIE
2621 RT6
2622 PIO       CHECK IO1 FOR ZEROS
2623 ST6
2624 SIE       OP3  CA4  OA3     IO1 CONTAINS ZEROS
2625 RIE
2626 RT6
2627 PIO       CHECK IO1 FOR ZEROS
2630 SIE
2631 CI0022    SELECT TMR
2632           THE NEXT FOUR TESTS ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
2633
2634
2635
2636 RIE
2637 CI0002,0C6  CLEAR IO1 AND IO2
2640 CI0002,041  IO1 CONTAINS B19
2641 PIO      CHECK IO1 FOR B19
2642 CI0002   CLEAR IO1
2643 PIO      CHECK IO1 FOR ZEROS
2644 SIE
2645 LDLC3    LOAD DL WITH SIGN
2646 ST6
2647 COP1     A1 AOC ERROR    IO1 CONTAINS ZEROS    DD CONTAINS SIGN
```

Figure 7-27. Self-Check Tape Instructions (Sheet 38)

```
Tape
Word Operation                          Indication
Count

2650 SSL
2651 RIE
2652 RT6
2653 PIO      CHECK IO1 FOR ZEROS
2654 ST6
2655          TAADR6,5,4NOT,3,2NOT,1NOT
2656 LDLC3    LOAD DL WITH ONES
2657 PIO      LOAD IO1 WITH ONES
2660 CIOOO1,OO6  LOAD IO2 WITH ONES
2661 FPIO     TAADR6,5NOT,4,3,2NOT,1NOT
2662 LDLC3    CLEAR DL
2663 RT6
2664 CIOOO2,OC6  CLEAR IO1 AND IO2
2665 SIE
2666 CBS123   BSE
2667 SSL
2670 CBS1     A1 G5 NOT ERROR
2671 SSL
2672 CBS2     A2 G5NOT ERROR
2673 SSL
2674 CBS3     A3 G5NOT ERROR
2675 SSL
2676 CPS1     A1 PBNOT ERROR
2677 SSL
2700 CPS2     A2 PBNOT ERROR
2701 SSL
2702 CPS3     A3 PBNOT ERROR
2703 SSL
2704 CBS1,LDLC3  A1 G5NOT ERROR    LOAD DL WITH SIGN
2705 SSL
2706 RIE
2707 PIO      LOAD IO1 WITH SIGN
2710 PIO      CHECK IO1 FOR SIGN
2711 PIO      CLEAR PIO ADR
2712          TAADR6NOT,5NOT,4NOT,3,2NOT,1NOT DS1 DS2 DS3 DS4
2713          TAADR6NOT,5NOT,4NOT,3,2,1  DS1
2714          TAADR6NOT,5NOT,4,3,2NOT,1  DS1    0A9 TO 0A1
2715          TAADR6NOT,5,4NOT,3,2NOT,1  DS1     END OF PBNOT AND G5NOT TESTS
```

Figure 7-27. Self-Check Tape Instructions (Sheet 39)

```
Tape
Word Operation                          Indication
Count
2716 LDLC3   CLEAR DL
2717         OP3  OA8  OA7  S     DL CONTAINS ZEROS
2720 PIO     LOAD IO1 WITH ZEROS
2721 PIO     CHECK IO1 FOR ZEROS
2722 LDLC3   LOAD DL WITH B25
2723         OA6  OA5     DL CONTAINS B25
2724 PIO     LOAD IO1 WITH B25
2725 PIO     CHECK IO1 FOR B25
2726 SHFC1,SHFC2   DL CONTAINS B23
2727 PIO     LOAD IO1 WITH B23
2730 PIO     CHECK IO1 FOR B23
2731         OA9  S      DL CONTAINS B23
2732 PIO     LOAD IO1 WITH B23
2733 PIO     CHECK IO1 FOR B23
2734 PIO     PIO OA9 OA8 OA4    IO1 CONTAINS SIGN
2735 PIO     CHECK IO1 FOR SIGN
2736 LDLC3   LOAD DL WITH B13
2737         OP4 OP3 OP2 OA4
2740         OP4 OP3 OP2 OA9
2741 LDLC3   CLEAR DL
2742 PIO     CLEAR IO1    END OF LOADING DL TESTS
2743 SIE
2744         SE1    SEQUENCE BIT PROGRAMMED IN TRCB5  TWC ADVANCES TWO COUNTS
2745
2746 SSL
2747         TPE   PARITY OF CB3 IS EVEN
2750 SSL
2751 LDLC3   TPE   PARITY OF CB4 IS EVEN       DL CONTAINS ZEROS
2752 SSL
2753 PIO     IO1 CONTAINS ZEROS
2754 RIE
2755 PIO     CHECK IO1 FOR ONES
2756 LDLC3   LOAD DL WITH IM1
2757         SPE    TAPE READER STOPS
              THE FOLLOWING COMMAND AND COMPUTER LAMPS ARE LIT ON THE
              MEMORY LOAD AND DATA DISPLAY PANEL
                 COMMAND                 COMPUTER
                  DS1                      ISX
                  OP1                      SYLO
```

Figure 7-27. Self-Check Tape Instructions (Sheet 40)

Tape Word Count	Operation	Indication
	OP2	DSX
	OP3	
	OP4	
	ISX	
	SYLO	
	DSX	
	SIGN	
	B1	
	SYL1	
	ALL OTHER COMMAND AND COMPUTER LAMPS ARE OUT	
	LAMPS OTHER THAN COMMAND AND COMPUTER LAMPS MAY OR MAY NOT BE LIT	
	THE SERIAL PARITY ERROR LAMP ON THE INTERFACE EXERCISER PANEL IS LIT. ALL OTHER ERROR LAMPS ARE OUT.	
	OTHER LAMPS ON THE INTERFACE EXERCISER PANEL MAY OR MAYNOT BE LIT	
	THE FOLLOWING LAMPS ARE LIT ON THE TAPE READER PANEL	
	TAPE ADDRESS TWC 0,1,2,3,5,6,7,8,10	
	AUTO	
	ML	
	PWR ON	
	FORWARD	
	STOP	
	ADV CTR OR SEL ADR	
	ALL OTHER LAMPS ON THE TAPE READER PANEL ARE OUT	
	OPERATE TAPE START P/B	TAPE READER SHALL NOT ADVANCE TAPE
	OPERATE ERROR RESET P/B	ERROR LAMP GOES OUT
		TAPE READE START LAMP LIGHTS
	OPERATE TAPE START P/B	TAPE ADVANCES TO 02760
2760	SSMSC TRS ERRORS ONLY	TAPE READER STOPS COMPUTER IM1 LAMP IS LIT
	DISREGARD ALL OTHER LAMPS	
	OPERATE ERROR RESET P/B	ERROR LAMPS GO OUT
	OPERATE TAPE START P/B	TAPE ADVANCES TO 02761
2761	SSMBR TRS ERRORS ONLY	TAPE READER STOPS COMPUTER IM1 LAMP IS LIT
	DISREGARD ALL OTHER LAMPS	
	OPERATE ERROR RESET P/B	ERROR LAMPS GO OUT
	OPERATE TAPE START P/B	TAPE ADVANCES TO 02762
2762	SSMDR TRS ERRORS ONLY	TAPE READER STOPS COMPUTER IM1 LAMP IS LIT
	DISREGARD ALL OTHER LAMPS	
	OPERATE ERROR RESET P/B	ERROR LAMPS GO OUT

Figure 7-27. Self-Check Tape Instructions (Sheet 41)

Tape Word Count	Operation	Indication
		OPERATE TAPE START P/B TAPE ADVANCES TO 02763
2763		IO1 ERROR ONLY TAPE READER STOPS
		DISREGARD ALL OTHER LIGHTS
		OPERATE ERROR RESET P/B ERROR LAMP GOES OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02764
2764		IO2 ERROR ONLY TAPE READER STOPS
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMP GOES OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02766
2765	LDLC3	CLEAR DL
2766		TRS SER ERRORS ONLY TAPE READER STOPS
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02767
2767	MAIC4	AI3 SER ERRORS ONLY TAPE READER STOPS
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02771
2770	LDLC3	LOADS DL WITH IM1,DM1
2771		TRS PAR SSMBR HOPC1 ERRORS ONLY TAPE READER STOPS
		COMPUTER DM1 LAMP IS ON
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02772
2772		TRS PAR SSMBR HOPC1 ERRORS ONLY TAPE READER STOPS
		ONLY SYLO AND SX LAMPS ARE LIT IN COMPUTER SSM DISPLAY
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02773
2773		SSMSC SSMDR SSMBR HOPC1 TRS SER ERROR ONLY TAPE READER STOPS
		ONLY SYLO AND SX LAMPS ARE LIT IN COMPUTER SSM DISPLAY
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02774
2774		SSMSC HOPC1 ERRORS ONLY TAPE READER STOPS
		ONLY SYLO AND SX LAMPS ARE LIT IN COMPUTER SSM DISPLAY
		DISREGARD ALL OTHER LAMPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 02775

Figure 7-27. Self-Check Tape Instructions (Sheet 42)

```
Tape
Word  Operation                    Indication
Count

2775          SSMDR HOPC1 ERRORS ONLY  TAPE READER STOPS
              ONLY SYLO AND SX LAMPS ARE LIT IN COMPUTER SSM DISPLAY
              DISREGARD ALL OTHER LAMPS
              OPERATE ERROR RESET P/B   ERROR LAMPS GO OUT
             OPERATE TAPE START P/B   TAPE ADVANCES   TO 02776
2776          SSMSC HOPC1 ERRORS ONLY  TAPE READER STOPS
              ONLY SYLO AND SX LAMPS ARE LIT IN COMPUTER SSM DISPLAY
              DISREGARD ALL OTHER LAMPS
              OPERATE ERROR RESET P/B   ERROR LAMPS GO OUT
             OPERATE TAPE START P/B   TAPE ADVANCES   TO 02777
2777          IADR ERROR ONLY  TAPE READER STOPS
              ONLY SYLO AND SX LAMPS ARE LIT IN COMPUTER SSM DISPLAY
              DISREGARD ALL OTHER LAMPS
              OPERATE ERROR RESET P/B   ERROR LAMP GOES OUT
              OPERATE SWITCH  1  ON TAPE READER PANEL. THIS WILL ALLOW THE TAPE
              READER TO BE OPERATED IN A SINGLE STEP MODE. IT WILL BE NECESSARY
              TO OPERATE THE TAPE START SWITCH FOR EACH OF THE FOLLOWING STEPS.
              IN THE FOLLOWING STEPS THE INDICATE LAMPS ON THE SIMPLEX AND
              MODULE SELECTION SECTION WILL BE LIT.
3000 CI0022   ALL
3001 CI0066   CH1 CH2=1 CH3=0
3002 CI0066   CH2 CH1=0 CH3=1
3003 CI0072   CH2 CH1=1 CH3=0
3004 CI0076   CH3 CH1=1 CH2=0
3005 CI0102   CH3 CH1=0 CH3=1
3006 CI0056   CH1 CH2=0 CH3=1
3007 CI0062   CH1 CH2=1 CH3=0
3010 CI0022   ALL          END OF CHANEL SWITCHING CHECKS
3011 CBS1,CBS2  BSE A3G5NOT ERRORS  OPERATE ERROR RESET P/B  ERROR LAMPS GO OUT
3012 CBS1,CBS3  BSE A2G5NOT ERRORS  OPERATE ERROR RESET P/B  ERROR LAMPS GO OUT
3013 CBS2,CBS3  BSE A1G5NOT ERRORS  OPERATE ERROR RESET P/B  ERROR LAMPS GO OUT
              OPERATE SWITCH  1  ON TAPE READER PANEL. SWITCH LAMP GOES OUT
              TAPE WILL NOW OPERATE AUTOMATICALLY
             OPERATE TAPE START P/B   TAPE ADVANCES   TO 03016A
3014 LDLC3     CLEAR DL
3015 PIO       CLEAR IO1
3016 CI0006    CLEAR IO2
0316A         SE2 ERROR   TAPE READER STOPS
```


Figure 7-27. Self-Check Tape Instructions (Sheet 43)

Tape Word Count	Operation	Indication
		OPERATE AUTO/MANUAL P/B MANUAL PORTION OF SWITCH LIGHTS
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03017
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03020
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03021
		OPERATE FORWARD/REVERSE P/B REVERSE PORTION OF SWITCH LIGHTS
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03023
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03024
		OPERATE FORWARD/REVERS P/B FORWARD PORTION OF SWITCH LIGHTS
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03026
		OPERATE MANUAL ADVANCE TAPE P/B TWC INDICATES 03027
		OPERATE ERROR RESET P/B ERROR LAMP GOES OUT
		OPERATE AUTO/MANUAL P/B AUTO PORTION OF SWITCH LIGHTS
		OPERATE TAPE START P/B TAPE ADVANCES TO 03032
3030	SIE	
03031	ST6	
03032		A1 AND A2 VOTER ERRORS TAPE READER STOPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 03034
03033		
03034		A2 AND A3 VOTER ERRORS TAPE READER STOPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 03036
03035		
03036		A1 AND A3 VOTER ERRORS TAPE READER STOPS
		OPERATE ERROR RESET P/B ERROR LAMPS GO OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 03040
03037	RIE	
3040	SIE	AOC ERROR TAPE READER STOPS INV ERR LAMP IS LIT
		OPERATE ERROR RESET P/B ERROR LAMP GOES OUT
		OPERATE TAPE START P/B TAPE ADVANCES TO 03041
3041	SSL	NO ERROR TAPE READER STOPS
		OPERATE AUTO/MANUAL P/B MANUAL PORTION OF SWITCH LIGHTS
		OPERATE ADV CTR/SEL ADR P/B SEL ADR PORTION LIGHTS
		OPERATE ADR2 P/B ADR2 AND ADR6 GO OUT
		OPERATE AUTO/MANUAL P/B AUTO PORTION OF SWITCH LIGHTS
		OPERATE ERROR OVERIDE P/B SWITCH LAMP LIGHTS
		OPERATE TAPE START P/B TAPE ADVANCES TO 03564
3042		
3043		

Figure 7-27. Self-Check Tape Instructions (Sheet 44)

```
Tape
Word Operation                              Indication
Count

3044
3045
3046 RIE      END OF CHECK OF SCIEC DIODES
3047 LDLC3    CLEAR DL
3050 RT6
3051 CAL1     A1 AOC ERROR        0A9 TO 0A1     VT3
3052 CAL3     A3 AOC ERROR
3053 SIE
3054 CAL1     AOC ERROR
3055 SSL
3056 LDLC3    CLEAR DL
3057 RIE
3060 CAL2     A2 AOC ERROR        0A9 TO 0A1     VT4
3061 CAL1     A1 AOC ERROR
3062 SIE
3063 CAL2     AOC ERROR
3064 SSL
3065 LDLC3    CLEAR DL
3066 RIE
3067 CAL3     A3 AOC ERROR        0A9 TO A01     VT5
3070 SIE
3071 CAL3     AOC ERROR
3072 SSL
3073 LDLC3    CLEAR DL
3074 CAL32    A1 AOC AND AOC ERRORS    A1 VT6
3075 SSL
3076 CAL31    A2 AOC AND AOC ERRORS    A1  VT7
3077 SSL
3100 CAL21    A3 AOC AND AOC ERRORS    A1  VT8
3101 SSL      END OF A1 VOTER CHECKS
3102 CAL32    A1 AOC AND AOC ERRORS    A2  VT6
3103 SSL
3104 CAL31    A2 AOC AND AOC ERRORS    A2  VT7
3105 SSL
3106 CAL21    A3 AOC AND AOC ERRORS    A2  VT8
3107 SSL      END OF A2 VOTER CHECKS
3110 CAL32    A1 AOC AND AOC ERRORS    A3  VT6
3111 SSL
```

Figure 7-27. Self-Check Tape Instructions (Sheet 45)

Tape Word Count	Operation		Indication	
3112	CAL31	A2 AOC AND AOC ERRORS	A3	VT7
3113	SSL			
3114	CAL21	A3 AOC AND AOC ERRORS	A3	VT8
3115	SSL	END OF A3 VOTER CHECKS		
3116	CAL32	A1 AOC AND AOC ERRORS	A4	VT6
3117	SSL			
3120	CAL31	A2 AOC AND AOC ERRORS	A4	VT7
3121	SSL			
3122	CAL21	A3 AOC AND AOC ERRORS	A4	VT8
3123	SSL	END OF A4 VOTER CHECKS		
3124	CAL32	A1 AOC AND AOC ERRORS	A5	VT6
3125	SSL			
3126	CAL31	A2 AOC AND AOC ERRORS	A5	VT7
3127	SSL			
3130	CAL21	A3 AOC AND AOC ERRORS	A5	VT8
3131	SSL	END OF A5 VOTER CHECKS		
3132	CAL32	A1 AOC AND AOC ERRORS	A6	VT6
3133	SSL			
3134	CAL31	A2 AOC AND AOC ERRORS	A6	VT7
3135	SSL			
3136	CAL21	A3 AOC AND AOC ERRORS	A6	VT8
3137	SSL	END OF A6 VOTER CHECKS		
3140	CAL32	A1 AOC AND AOC ERRORS	A7	VT6
3141	SSL			
3142	CAL31	A2 AOC AND AOC ERRORS	A7	VT7
3143	SSL			
3144	CAL21	A3 AOC AND AOC ERRORS	A7	VT8
3145	SSL	END OF A7 VOTER CHECKS		
3146	CAL32	A1 AOC AND AOC ERRORS	A8	VT6
3147	SSL			
3150	CAL31	A2 AOC AND AOC ERRORS	A8	VT7
3151	SSL			
3152	CAL21	A3 AOC AND AOC ERRORS	A8	VT8
3153	SSL	END OF A8 VOTER CHECKS		
3154	CAL32	A1 AOC AND AOC ERRORS	A9	VT6
3155	SSL			
3156	CAL31	A2 AOC AND AOC ERRORS	A9	VT7
3157	SSL			
3160	CAL21	A3 AOC AND AOC ERRORS	A9	VT8

Figure 7-27. Self-Check Tape Instructions (Sheet 46)

```
Tape
Word Operation                                  Indication
Count

3161 SSL      END OF A9 VOTER CHECKS
3162 RIE
3163 ST6
3164 COP1     CP1 TO OP3  VT3
3165 COP2     CP1 TO OP3  VT4
3166 COP3     CP1 TO CP3  VT5
3167 COP1     CP4  VT3
3170 COP2     CP4  VT4
3171 COP3     CP4  VT5
3172 LDLC3    CLEAR DL
3173 COP32    CP4 TO CP1  VT6
3174 COP31    CP4 TO CP1  VT7
3175 COP21    CP4 TO CP1  VT8   END OF OP CODE VOTER TESTS
3176 LDLC3    LOAD DL WITH DS1,DS2,DS3,IS1,IS2,IS3
3177 FPIO,CSVE1  A1 HOPC1 AND OTHER A1 VOTER ERRORS    HOPC1 VT3
3200 SIE
3201          SSMBR TRS ERRORS
3202 SSL
3203 RIE
3204 FPIO,CSVE2  A2 HOPC1 AND OTHER A1 VOTER ERRORS    HOPC1 VT4
3205 SIE
3206          SSMBR TRS ERRORS
3207 SSL
3210 RIE
3211 FPIO,CSVE3  A3 HOPC1 AND OTHER A1 VOTER ERRORS    HOPC1 VT5
3212 SIE
3213          SSMBR TRS ERROR
3214 SSL
3215 LDLC3    LOAD DL WITH DS1,2,3,4,IS1,2,3,4,DM2,3,IM2,3,SYL1,IDX,DDX
3216 RIE
3217 FPIO,CSVE32  A1 HOPC1 AND OTHER A1 VOTER ERRORS   HOPC1 VT6
3220 SIE
3221          SSMBR TRS ERRORS
3222 SSL
3223 RIE
3224 FPIO,CSVE31  A2 HOPC1 AND OTHER A2 VOTER ERRORS   HOPC1 VT7
3225 SIE
3226          SSMBR TRS ERRORS
```

Figure 7-27. Self-Check Tape Instructions (Sheet 47)

```
Tape
Word Operation                          Indication
Count
3227 SSL
3230 RIE
3231 FPIO,CSVE21  A3 HOPC1 AND OTHER A3 VOTER ERRORS   HOPC1 VT8
3232 SIE
3233          SSMBR TRS ERRORS
3234 SSL      END OF HOPC1 VOTER CHECKS
3235 LDLC3    LOAD DL WITH B3,4,8,9
3236 PIO      LOAD IO1 WITH B3,4,8,9
3237 CI0001,0C6  LOAD IO2 WITH B3,4,8,9
3240 LDLC3    CLEAR DL
3241 RIE
3242 FPIO,CSVE1  A1 VOTER ERRORS   IO1 CONTAINS B3,4,8,9    MR1 VT3
3243 FPIO     CHECK IO1 FOR B3,4,8,9
3244          SSMSC TRS ERRORS
3245 SSL
3246 RIE
3247 FPIO,CSVE2  A2 VOTER ERRORS   IO1 CONTAINS B3,4,8,9    MR1 VT4
3250 FPIO     CHECK IO1 FOR B3,4,8,9
3251          SSMSC TRS ERRORS
3252 SSL
3253 RIE
3254 FPIO,CSVE3  A3 VOTER ERRORS   IO1 CONTAINS B3,4,8,9    MR1 VT5
3255 FPIO     CHECK IO1 FOR B3,4,8,9
3256          SSMSC TRS ERRORS
3257 SSL
3260 RIE
3261 FPIO,CSVE32  A1 VOTER ERRORS  IO1 CONTAINS B3 TO B9    MR1 VT6
3262 FPIO     CHECK IO1 FOR B3 TO B9
3263          SSMSC TRS ERRORS
3264 SSL
3265 RIE
3266 FPIO,CSVE31  A2 VOTER ERRORS  IO1 CONTAINS B3 TO B9    MR1 VT7
3267 FPIO     CHECKS IO1 FOR B3 TO B9
3270          SSMSC TRS ERRORS
3271 SSL
3272 RIE
3273 FPIO,CSVE21  A3 VOTER ERRORS  IO1 CONTAINS B3 TO B9    MR1 VT8
3274 FPIO     CHECK IO1 FOR B3 TO B9
3275          SSMSC TRS ERRORS
```

Figure 7-27. Self-Check Tape Instructions (Sheet 48)

```
Tape
Word Operation                          Indication
Count

3276 SSL
3277 RIE      END OF MR1 VOTER TESTS
3300 FPIO,CSVE1   A1 VOTER ERRORS  IO1 CONTAINS B3,4,8,9    MD7 VT3
3301 FPIO     CHECK IO1 FOR B3,4,8,9
3302          SSMSC TRS ERRORS
3303 SSL
3304 RIE
3305 FPIO,CSVE2   A2 VOTER ERRORS  IO1 CONTAINS B3,4,8,9    MD7 VT4
3306 FPIO     CHECK IO1 FOR B3,4,8,9
3307          SSMSC TRS ERRORS
3310 SSL
3311 RIE
3312 FPIO,CSVE3   A3 VOTER ERRORS  IO1 CONTAINS B3,4,8,9    MD7 VT5
3313 FPIO     CHECK IO1 FOR B3,4,8,9
3314          SSMSC TRS ERRORS
3315 SSL
3316 RIE
3317 FPIO,CSVE32  A1 VOTER ERRORS  IO1 CONTAINS B3 TO B9    MD7 VT6
3320 FPIO     CHECK IO1 FOR B3 TO B9
3321          SSMSC TRS ERRORS
3322 SSL
3323 RIE
3324 FPIO,CSVE31  A2 VOTER ERRORS  IO1 CONTAINS B3 TO B9    MD7 VT7
3325 FPIO     CHECK IO1 FOR B3 TO B9
3326          SSMSC TRS ERRORS
3327 SSL
3330 RIE
3331 FPIO,CSVE21  A3 VOTER ERRORS  IO1 CONTAINS B3 TO B9    MD7 VT8
3332 FPIO     CHECK IO1 FOR B3 TO B9
3333          SSMSC TRS ERRORS
3334 SSL      END OF MD7 VOTER TESTS
3335 FPIO1    A1 PIO ERROR
3336 CIO022   SELECT TMR
3337          THE NEXT FOUR TESTS ARE BLANK TO ALLOW TIME FOR RELAYS TO SETTLE
3340
3341
3342
3343 CIO006,041   IO2 CONTAINS B18,19
```

Figure 7-27. Self-Check Tape Instructions (Sheet 49)

```
Tape
Word Operation                          Indication
Count

3344          SSMSC TRS ERRORS
3345 SSL
3346 RIE
3347 FPIO     CHECK IO2 FOR B18,19
3350 FPIO2    A2 PIO ERROR
3351 CIO006,041  IO2 CONTAINS B17,19
3352          SSMSC TRS ERROR
3353 SSL
3354 RIE
3355 FPIO     CHECK IO2 FOR B17,19
3356 FPIO3    A3 PIO ERROR
3357 CIO006,041  IO2 CONTAINS B16,19
3360          SSMSC TRS ERROR
3361 SSL
3362 RIE
3363 FPIO     CHECK IO2 FOR B16,19
3364 EP1
3365 CIO006,041  IO2 CONTAINS B15,19
3366 RIE
3367 FPIO     CHECK IO2 FOR B15,19
3370 CIO026   RESET EP1
3371 CIO006,041 IO2 CONTAINS B19
3372 RIE
3373 FPIO     CHECK IO2 FOR B19
3374 EP2
3375 CIO006,041  IO2 CONTAINS B14,19
3376 RIE
3377 FPIO     CHECK IO2 FOR B14,19
3400 CIO026   RESET EP2
3401 EP3
3402 CIO006,041  IO2 CONTAINS B13,19
3403 RIE
3404 FPIO     CHECK IO2 FOR B13,19
3405 CIO026   RESET EP3
3406 EP4
3407 CIO006,041  IO2 CONTAINS B12,19
3410 RIE
3411 FPIO     CHECK IO2 FOR B12,19
3412 CIO026   RESET EP4
```

Figure 7-27. Self-Check Tape Instructions (Sheet 50)

Tape Word Count	Operation	Indication
3413	EP5	
3414	CI0006,041	IO2 CONTAINS B11,19
3415	RIE	
3416	FPIO	CHECK IO2 FOR B11,19
3417	CI0026	RESET EP5
3420	EP6	
3421	CI0006,041	IO2 CONTAINS B10,19
3422	RIE	
3423	FPIO	CHECK IO2 FOR B10,19
3424	CI0026	RESET EP6
3425	EP7	
3426	CI0006,041	IO2 CONTAINS B9,19
3427	RIE	
3430	FPIO	CHECK IO2 FOR B9,19
3431	CI0026	RESET EP7
3432	EP8	
3433	CI0006,041	IO2 CONTAINS B8,19
3434	RIE	
3435	FPIO	CHECKS IO2 FOR B8,19
3436	CI0026	RESET EP8
3437	EP9	
3440	CI0006,041	IO2 CONTAINS B7,19
3441	RIE	
3442	FPIO	CHECK IO2 FOR B7,19
3443	CI0026	RESET EP9
3444	EP10	
3445	CI0006,041	IO2 CONTAINS B6,19
3446	RIE	
3447	FPIO	CHECK IO2 FOR B6,19
3450	CI0026	RESET EP10
3451	EP11	
3452	CI0006,041	IO2 CONTAINS B5,19
3453	RIE	
3454	FPIO	CHECK IO2 FOR B5,19
3455	CI0026	RESET EP11
3456	EP12	
3457	CI0006,041	IO2 CONTAINS B4,19
3460	RIE	

Figure 7-27. Self-Check Tape Instructions (Sheet 51)

Tape Word Count	Operation	Indication
3461	FPIO	CHECK IO2 FOR B4,19
3462	CIO026	RESET EP12
3463	EP13	
3464	CIO006,041	IO2 CONTAINS B3,19
3465	RIE	
3466	FPIO	CHECK IO2 FOR B3,19
3467	CIO026	RESET EP13
3470	RIE	
3471	RT6	
3472	PEA	EAM ERROR
3473	CIO006,041	IO2 CONTAINS B2,19
3474	PIO	CHECK IO2 FOR B2,19
3475	CIO026	RESET EAM ERROR
3476	PEB	EBM ERROR
3477	CIO006,041	IO2 CONTAINS B1,19
3500	PIO	CHECK IO2 FOR B1,19
3501	CIO026	RESET EBM ERROR
3502	PEL123	TLC ERROR
3503	CIO006,041	IO2 CONTAINS SIGN,B19
3504	PIO	CHECK IO2 FOR SIGN,B19
3505	PEA,PEB	EAM EBM ERRORS
3506		CA5
3507	CIO006,041	IO2 CONTAINS SIGN,B1,2,19
3510	PIO	CHECK IO2 FOR SIGN,B1,2,19
3511	PIO	CA5NOT
3512	CIO006,041	IO2 CONTAINS SIGN,B1,2,19
3513	PIO	CHECK IO2 FOR SIGN,B1,2,19
3514	PIO	CA9 CA5
3515	CIO006,041	IO2 CONTAINS SIGN,B1,2,19
3516	PIO	CHECK IO2 FOR SIGN,B1,2,19
3517	PIO	CA5 CA1
3520	CIO006,041	IO2 CONTAINS SIGN,B1,2,19
3521	PIO	CHECK IO2 FOR SIGN,B1,2,19
3522	PIO	CA5 CA2
3523	CIO006,041	IO2 CONTAINS SIGN,B1,2,19
3524	PIO	CHECK IO2 FOR SIGN,B1,2,19
3525	PIO	RESET TLC EAM EBM ERRORS
3526	CIO006,041	IO2 CONTAINS B19
3527	PIO	CHECK IO2 FOR B19 END ERROR SERIALIZER TESTS

Figure 7-27. Self-Check Tape Instructions (Sheet 52)

```
Tape
Word Operation                          Indication
Count

3530 PEA,PEB,PEL1  EAM EBM TLC  A1 TLC ERRORS
3531 CI0006,041  IO2 CONTAINS SIGN,B1,2,18,19
3532 PIO      CHECK IO2 FOR SIGN,B1,2,18,19
3533 SIE
3534          SSMSC TRS ERROR
3535 SSL
3536 RIE
3537 PEA,PEB,PEL2  EAM EBM TLC  A2 TLC ERRORS
3540 CI0006,041  IO2 CONTAINS SIGN,B1,2,17,19
3541 PIO      CHECK IO2 FOR SIGN,B1,2,17,19
3542 SIE
3543          SSMSC TRS ERRORS
3544 SSL
3545 RIE
3546 PEA,PEB,PEL3  EAM EBM TLC  A3 TLC ERRORS
3547 CI0006,041  IO2 CONTAINS SIGN,B1,2,16,19
3550 PIO      CHECK IO2 FOR SIGN,B1,2,16,19
3551 SIE
3552          SSMSC TRS ERRORS
3553 SSL
3554 RIE      END OF EAM EBM TLC TESTS
3555 LDLC3    CLEAR DL
3556 CI0002,0C6  CLEAR IO1 AND IO2
3557 LDLC3    LOAD DL WITH B25
3560 PIO      LOAD MLC  IO2 CONTAINS ZEROS
3561 PIO      CHECK IO2 FOR ZEROS
3562 PIO      LOAD SSC  IO2 CONTAINS ZEROS
3563 PIO      CHECK IO2 FOR ZEROS
3564          SPE  TAPE READER STOPS
              OPERATE OP/TP P/B   OP PORTION OF SWITCH LIGHTS
              OPERATE ERROR RESET P/B   ERROR LAMP GOES OUT
              OPERATE TAPE START P/B   TAPE ADVANCES   TO 03770
3565 LDLC3    LOAD DL WITH B13
3566 PIO      IO2 CONTAINS SIGN
3567 CI0002,021  IO1 CONTAINS B13
3570 PIO      CHECK IO1 FOR B13
3571 LDLC3    CLEAR DL
3572 PIO      CLEAR IO2
```

Figure 7-27. Self-Check Tape Instructions (Sheet 53)

Tape Word Count	Operation		Indication
3573	CI0002,021	I01 CONTAINS ZEROS	
3574	PIO	CHECK I01 FOR ZEROS	
3575	LDLC3	LOAD DL WITH B13	
3576	PIO	I02 CONTAINS SIGN	
3577	CI0002,021	I01 CONTAINS B13	
3600	CI0002,021	I01 CONTAINS B13	
3601	PIO	CHECK I01 FOR B13	
3602	LDLC3	LOAD DL WITH B25	
3603	PIO	LOAD I01 WITH B25	
3604	CI0002,021	I02 CONTAINS B12	
3605	CI0002,021	I01 CONTAINS B25	
3606	PIO	CHECK I01 FOR B25	
3607	LDLC3	LOAD DL WITH B13	
3610	PIO	I01 CONTAINS B13	
3611	CI0001,006	I02 CONTAINS SIGN	
3612	CI0002,021	I01 CONTAINS B13	
3613	PIO	CHECK I01 FOR B13	
3614	LDLC3	CLEAR DL	
3615	PIO	A7,6,5,4,3,2,1NOT	I02 CONTAINS SIGN
3616	CI0002,021	I01 CONTAINS B13	
3617	PIO	CHECK I01 FOR B13	
3620	PIO	A7NOT,6NOT,5,4,3,2,1NOT	I02 CONTAINS SIGN
3621	CI0002,021	I01 CONTAINS B13	
3622	PIO	CHECK I01 FOR B13	
3623	PIO	A7NOT,6,5NOT,4,3,2,1NOT	I02 CONTAINS SIGN
3624	CI0002,021	I01 CONTAINS B13	
3625	PIO	CHECK I01 FOR B13	
3626	PIO	A7NOT,6,5,4NOT,3,2,1NOT	I02 CONTAINS SIGN
3627	CI0002,021	I01 CONTAINS B13	
3630	PIO	CHECK I01 FOR B13	
3631	PIO	A7NOT,6,5,4,3NOT,2,1NOT	I02 CONTAINS SIGN
3632	CI0002,021	I01 CONTAINS B13	
3633	PIO	CHECK I01 FOR B13	
3634	PIO	A7NOT,6,5,4,3,2NOT,1NOT	I02 CONTAINS SIGN
3635	CI0002,021	I01 CONTAINS B13	
3636	PIO	CHECK I01 FOR B13	
3637	PIO	A7NOT,6,5,4,3,2,1	I02 CONTAINS SIGN
3640	CI0002,021	I01 CONTAINS B13	
3641	PIO	CHECK I01 FOR B13	

Figure 7-27. Self-Check Tape Instructions (Sheet 54)

```
Tape
Word Operation                          Indication
Count

3642          A7NOT,6,5,4,3,2,1NOT      IO2 CONTAINS SIGN
3643 CI0002,021  IO1 CONTAINS B13
3644 PIO      CHECK IO1 FOR B13
3645 LDLC3    LOAD DL WITH SIGN
3646 PIO      LOAD IO1 WITH SIGN
3647 LDLC3    CLEAR DL
3650 PIO      CHECK IO1 FOR SIGN
3651 ST6
3652 SIE      CP3 0A4    IO1 CONTAINS SIGN
3653 RIE
3654 ST6
3655 PIO      CHECK IO1 FOR SIGN
3656 PEL1,PEL2,PEL3   TLC ERROR
3657 PIO      IO1 CONTAINS SIGN
3660 ST6
3661 SIE      CP3 0A4 0A3  IO1 CONTAINS ZEROS
3662 RT6
3663 RIE
3664 PIO      CHECK IO1 FOR ZEROS
3665 CI0026   RESET TLC ERROR
3666 PIO      CLEAR MLC AND IO1
3667 LDLC3    LOAD DL WITH B13
3670 PIO      A7NOT,6,5,4NOT,3NOT,2,1   IO2 CONTAINS B13
3671 LDLC3    CLEAR DL
3672 CI0002,025  IO1 CONTAINS B13
3673 PIO      CHECK IO1 FOR B13
3674 PIO      CLEAR SSC
3675 CI0002,025  IO1 CONTAINS ZEROS
3676 PIO      CHECK IO1 FOR ZEROS
3677 LDLC3    LOAD DL WITH B13
3700 PIO      SSC CONTAINS ZEROS
3701 CI0002,025  IO1 CONTAINS ZEROS
3702 PIO      CHECK IO1 FOR ZEROS
3703 CI0001,016  SSC CONTAINS ZEROS
3704 CI0002,025  IO1 CONTAINS ZEROS
3705 PIO      CHECK IO1 FOR ZEROS
3706 PIO      IO1 CONTAINS B13
3707 CI0001,016  SSC CONTAINS B13
```

Figure 7-27. Self-Check Tape Instructions (Sheet 55)

```
Tape
Word Operation                          Indication
Count

3710 CI0002,025  IO1 CONTAINS B13
3711 PIO         CHECK IO1 FOR B13
3712 LDLC3       LOAD DL WITH B25
3713 CI0001,016  SSC CONTAINS B13
3714 CI0002,025  IO1 CONTAINS B13
3715 PIO         CHECK IO1 FOR B13
3716 PIO         IO1 CONTAINS B25
3717 CI0001
3720 CI0002,025  IO1 CONTAINS B13
3721 PIO         CHECK IO1 FOR B13
3722 LDLC3       CLEAR DL
3723             A7,6,5,4NOT,3NOT,2,1NOT          SSC CONTAINS B13
3724 CI0002,025  IO1 CONTAINS B13
3725 PIO         CHECK IO1 FOR B13
3726 PIO         A7NOT,6NOT,5,4NOT,3NOT,2,1NOT    SSC CONTAINS B13
3727 CI0002,025  IO1 CONTAINS B13
3730 PIO         CHECK IO1 FOR B13
3731 PIO         A7NOT,6,5NOT,4NOT,3NOT,2,1NOT    SSC CONTAINS B13
3732 CI0002,025  IO1 CONTAINS B13
3733 PIO         CHECK IO1 FOR B13
3734 PIO         A7NOT,6,5,4,3NOT,2,1NOT          SSC CONTAINS B13
3735 CI0002,025  IO1 CONTAINS B13
3736 PIO         CHECK IO1 FOR B13
3737 PIO         A7NOT,6,5,4NOT,3,2,1NOT          SSC CONTAINS B13
3740 CI0002,025  IO1 CONTAINS B13
3741 PIO         CHECK IO1 FOR B13
3742 PIO         A7NOT,6,5,4NOT,3NOT,2NOT,1NOT    SSC CONTAINS B13
3743 CI0002,025  IO1 CONTAINS B13
3744 PIO         CHECK IO1 FOR B13
3745 PIO         A7NOT,6,5,4NOT,3NOT,2,1          SSC CONTAINS B13
3746 CI0002,025  IO1 CONTAINS B13
3747 PIO         CHECK IO1 FOR B13
3750             A7NOT,6,5,4NOT,3NOT,2,1NOT       SSC CONTAINS B13
3751 CI0002,025  IO1 CONTAINS B13
3752 PIO         CHECK IO1 FOR B13
3753 PIO         CLEAR SSC
3754 LDLC3       LOAD DL WITH B20
3755 PIO         MLC CONTAINS B7
3756 PIO         SSC CONTAINS ZEROS
```

Figure 7-27. Self-Check Tape Instructions (Sheet 56)

```
Tape
Word Operation                          Indication
Count

3757 C10002,025  101 CONTAINS ZEROS
3760 PIO      CHECK 101 FOR ZEROS
3761 PIO      CLEAR MLC
3762 PIO      SSC CONTAINS B20
3763 PIO      MLC CONTAINS ZEROS
3764 C10002,021  101 CONTAINS ZEROS
3765 PIO      CHECK 101 FOR ZEROS
3766 PIO      CLEARS PIO ADR   END OF OPM CHECKS
3767 LDLC3    CLEAR DL
3770          SPE   TAPE READER STOPS
               OPERATE OP/TP P/B  TP PORTION LIGHTS   OP PORTION GOES OUT
               OPERATE VERIFY ONLY P/B    SWTCH LAMP LIGHTS
               OPERATE ERROR RESET P/B    ERROR LAMP GOES OUT
              OPERATE ERROR OVERRIDE P/B    SWITCH LAMP GOES OUT
               OPERATE TAPE START P/B   TAPE RUNS TO END AND REWINDS IF NO ERROR
3771           NO ERRORS
3772           NO ERRORS
3773           NO ERRORS
3774           NO ERRORS
3775 SIE
3776           SSMSC SSMBR SSMDR TRS ERRORS
3777 SSL
3800 RIE
3801 ISP       NO ERROR
3802 SIE
3803 ST6       SSMSC SSMBR SSMDR TRS ERRORS
3804 SSL
3805 RT6
3806           SSMSC SSMBR SSMDR TRS ERRORS
3807 SSL
3810           A2 AOC ERROR
3811 SSL
3812          AOC INSDR ADRSR ERRORS
3813 SSL
3814 ST6      SSMSC SSMBR SSMDR TRS ERRORS
3815 SSL
3816 RIE
3817 SSL
3820 TSC      END OF TAPE   READER REWINDS IF NO ERRORS EXIST
              TAPE STOPS   TWC INDICATES 06465
              OPERATE TAPE START P/B 9 TIMES.  ON THE NINTH OPERATION THE TAPE
              COMPLETES REWINDING
            END OF AUTOMATIC TESTS
```

Figure 7-27. Self-Check Tape Instructions (Sheet 57)

CODE	TAADR 654321	CONTROLS	FUNCTION
TSC	X00001		TAPE STOP, AUTOMATIC REWIND IF NO ERRORS
ISP	X00010	VERIFY ONLY MODE	INHIBIT SCRATCHPAD LOCATIONS
SPA	000010		SAMPLE PIO ADDRESS REGISTER
ST6	000011		SET TAADR6 LATCH
PEA	00100C	TROA1	A1EAM=1
PEB	00010C	TROA4	A1EBM=1
PEL1	00100C	TROA7	A1TLC=1
PEL2	00100C	TROA8	A2TLC=1
PEL3	00100C	TROA9	A3TLC=1
BRA1B	00100C	TRDS1	BRA=1 DURRING PHB
BRA1C	00100C	TRDS2	BRA=1 DURRING PHC
BRB1B	00100C	TRDS3	BRB=1 DURRING PHB
BRB1C	00100C	TRDS4	BRB=1 DURRING PHC
CPS1	000101	TRDS1,SCG5	A1PBNOT=0
CPS2	000101	TRDS2,SCG5	A2PBNOT=0
CPS3	000101	TRDS3,SCG5	A3PBNOT=0
CBS1	000101	TRMM1,SCPC	A1G5NOT=0
CBS2	000101	TRMM2,SCPC	A2G5NOT=0
CBS3	000101	TRMM3,SCPC	A3G5NOT=0
SSL	X00110	INVERT ERROR MODE	SAMPLE STOP LATCH
RT6	X00111		RESET INVERT ERROR
SIE	X0100C		SET INVERT ERROR LATCH
CALC	001000		ALL ADDRESS LINES=0
CAL1	001001		A1A1 TO A1A9=0
CAL2	001010		A2A1 TO A2A9=0
CAL21	001011		A2A1 TO A2A9 AND A1A1 TO A1A9=0
CAL3	001100		A3A1 TO A3A9=0
CAL31	001101		A3A1 TO A3A9 AND A1A1 TO A1A9=0
CAL32	001110		A3A1 TO A3A9 AND A2A1 TO A2A9=0
CAL321	001111		A3A1 TO A3A9,A2A1 TO A2A9,A1A1 TO A1A9=0
CIO001	X1000C	SIGN	READ IO1
CIO002	X1000C	B1	LOAD IO1
CIO005	X10000	B2	NOT USED
CIO006	X1000C	B3	LOAD IO2, LOAD MLC IN OP
CIO011	X1000C	B4	READ PIO ADR
CIO012	X10000	B5	NOT USED

Figure 7-28. Self-Check Tape Instruction and Operation Codes (Sheet 1 of 3)

CODE	TAADR 654321	CONTROLS	FUNCTION
CI0015	X10000	B6	READ RTC
CI0016	X10000	B7	LOAD SSC
CI0021	X10C0C	B8	READ I02, READ MLC IN OP
CI0022	X10000	B9	SWITCH CHANNELS TO TMR
CI0025	X10000	B10	READ SSC
CI0026	X10000	B11	RESET DISAGREEMENT ERRORS
CI0031	X10000	B12	READ PHA INFORMATION FROM HISTORY
CI0035	X10000	B13	READ PHB AND PHC INFORMATION FROM HISTORY
CI0041	X10000	B14	READ DISAGREEMENT ERRORS
CI0051	X10000	B15	READ SSM AND IA FROM HISTORY
CI0045	X10000	B16	READ INSTRUCTION FROM HISTORY
CI0056	X10000	B17	SELECT CHANNEL1, 2=0, 3=1
CI0062	X10000	B18	SELECT CHANNEL1, 2=1, 3=0
CI0066	X10000	B19	SELECT CHANNEL2, 1=0, 3=1
CI0072	X10000	B20	SELECT CHANNEL2, 1=1, 3=0
CI0076	X10000	B21	SELECT CHANNEL3, 1=1, 2=0
CI0102	X10C0C	B22	SELECT CHANNEL3, 1=0, 2=1
CI0106	X10000	B23	SET GC CST
CI0112	X10000	B24	RESET GC CST
CI0116	X10000	B25	SET GC HLT
CI0122	X10000	DS1	RESET GC HLT
CI0126	X10000	DS2	UNLOCK HISTORY LINES
CI0136	X10000	DS3	SET INTC
CI0142	X10000	DS4	RESET INTC
HOP	X10C0C		
MPY	X10001		
SUB	X1001C		
DIV	X10011		
TNZ	X10100		
MPH	X10101		
AND	X1011C		
ADD	X10111		
TRA	X11000		
XOR	X11001		
PIO	X11C1C		
STO	X11011		
TMI	X11100		
RSU	X11101		
SHF	X1111C		
CLA	X11111		
COPI	11XXXX	TROA1	A1OP1 TO A1OP4=1

Figure 7-28. Self-Check Tape Instruction and Operation Codes (Sheet 2)

CODE	TAADR 654321	CONTROLS	FUNCTION
COP2	11XXXX	TROA2	A2OP1 TO A2OP4=1
COP3	11XXXX	TROA3	A3OP1 TO A3OP4=1
LFW	X11111	REVERSE MODE	MARK BEGINNING OF TAPE. TAPE STOPS
EP1	100011	TRCA5	
EP2	100011	TROA4	
EP3	100011	TROA3	
EP4	100011	TRCA2	
EP5	100011	TRCA1	
EP6	100011	TRDS1	
EP7	100011	TRDS2	
EP8	100011	TRDS3	
EP9	100011	TRDS4	
EP10	100011	TROA9	
EP11	100011	TROA8	
EP12	100011	TROA7	
EP13	100011	TROA6	
RT6	X0C10C		RESET TAADR6
FPE	100101		FORCE SERIAL PARITY ERROR
FPIO1	101XXX	TRDS1	A1PIO=1
FPIO2	101XXX	TRDS2	A2PIO=1
FPIO3	101XXX	TRDS3	A3PIO=1
FPIO	101XXX	TRDS1,TRDS2,TRDS3	A1,A2,A3PIO=1
CSVE1	101001		SERIAL LINES A1=1
CSVE2	101010		SERIAL LINES A2=1
CSVE12	101011		SERIAL LINES A1 AND A2=1
CSVE3	101100		SERIAL LINES A3=1
CSVE31	101101		SERIAL LINES A3 AND A1=1
CSVE32	101110		SERIAL LINES A3 AND A2=1
CSVE321	101111		SERIAL LINES A3,A2,AND A1=1

NOTES

1 SERIAL LINES ARE TRS,AI3,MD7,MR1,PRO,HOPC1

2 DIE A9 LOADS MR1 INTO DD REGISTER

3 DIE A8 LOADS MD7 INTO DD REGISTER

SPECIAL INSTRUCTIONS

SHFC1	TROA9	TROA6	SHIFT CONTENTS OF DELAY LINE ONCE DURRING CYC1
SHFC2	TROA9	TROA5	SHIFT CONTENTS OF DELAY LINE ONCE DURRING CYC2
LDLC2	TROA9	TROA8	LOAD DIN INTO DELAY LINE DURRING CYC2
LDLC3	TROA9	TROA7	LOAD DIN INTO DELAY LINE DURRING CYC3
MA1C4	TROA9	TROA4	AI3=1 DURRING CYC4

Figure 7-28. Self-Check Tape Instruction and Operation Codes (Sheet 3)

SECTION VIII

TROUBLE ISOLATION

8-1. GENERAL.

8-2. Malfunctions of the LVDCME will be discovered either during calibrations or when the computer is under test. When a malfunction is discovered the calibration procedures outlined in Section VII should be performed to localize the malfunction to a particular functional area of the LVDCME.

8-3. When the malfunctioning functional area of the LVDCME has been determined, analyze the circuit(s) with the aid of the LVDCME Second Level Logic Diagrams in Section X and the descriptions of the circuit(s) in Section II. Reference is made from the second level logic diagrams to the Automated Logic Diagrams (ALD's). The ALD's, in turn, show the point to point wiring of the gate assemblies from which circuit points may be determined for testing signal levels.

8-4. PROBING CIRCUIT POINTS.

8-5. Each pin of an SMS card can be probed from the wiring side of the gate assembly to observe the signal levels. When probing an SMS card pin, care should be taken in locating the correct pin. The logic blocks on the ALD's reference the card location and pins in the gate assembly. (Refer to Section X for the Automated Logic Diagram Format.) Figure 8-1 illustrates the wiring side of a gate assembly in its extended or open position and shows the arrangement of pin locations of the SMS cards (or receptacle).

8-6. TROUBLE SHOOTING SMS CARDS.

8-7. SMS cards, except for the special printed circuit board assemblies (figures 10-40 through 10-55), are considered nonreparable and should be replaced by a new card when a failure occurs. If a special printed circuit board assembly (card) is determined to be faulty, the card circuits should be checked to determine the defective component. To check the card circuits, remove the card from its receptacle (use SMS Card Puller, IBM part number 6072429); insert Card Extender, IBM part number 6072431 into the card receptacle; and insert the card into the Card Extender. With the aid of the card schematic diagrams (figures 10-40 through 10-55), the defective card component can be determined. The card should then be repaired as described in Section IX.

8-8. SELF CHECK WIRED-IN PROGRAM.

8-9. A check of the data display portion of the LVDCME can be accomplished manually. A self-check wired-in program (figure 8-2) cycles continuously in the MEM SIM mode except when the CST function is used. The program data can be displayed at any time by manually inserting into the switches compare information as shown in the desired step of the program listing. The compare information consists of the bits shown in the first nine columns of the program step (figure 8-2). The Self Check TRS, or Self Check AI3 DATA, or Self Check AI3-Instruction Address information that appears in the program listing is displayed in the data display register when the DISPLAY SELECT rotary switch (MEMORY LOAD AND DATA DISPLAY panel) is in the TRS, or AI3 DATA or AI3-IA position respectively.

8-10. With programming and use of front panel controls, indicators and self-check facilities, further isolation of LVDCME malfunctions is possible. Errors encountered during the program will be displayed in the respective ERRORS lamps on the INTERFACE EXERCISER panel.

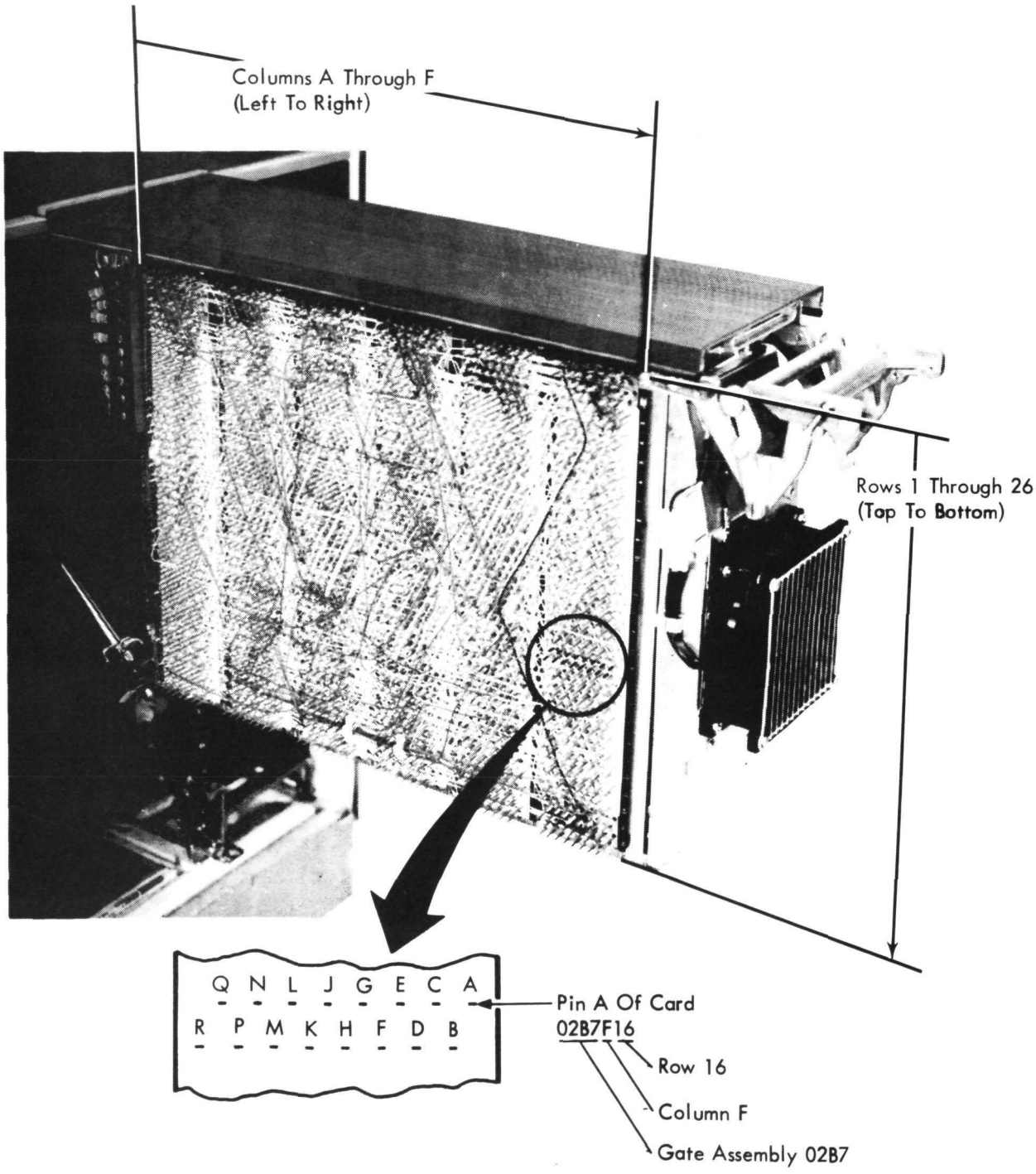


Figure 8-1. SMS Card Location and Pin Arrangement In Gate Assemblies

Instruction	Instruction Address	Instruction Module	Syllable	Instruction Duplex	Instruction Sector	Data Module	Data Duplex	Data Sector	Self Check AI3									Self Check TRS									Self Check AI3 Instruction Address		
		3 2 1			4 3 2 1	3 2 1		4 3 2 1	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	A9-A7	A6-A4	A3-A1
HOP	0 0 0							×	0	3	7	7	0	0	7	7	6	0	4	0	0	0	1	0	0	0	7	7	4
TRA	0 0 1								0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	2	0	0	0
HOP	0 0 2	×							0	0	0	1	0	0	0	0	2	0	0	0	2	0	0	0	0	4	0	0	4
TRA	0 0 3								0	0	0	2	0	0	0	0	4	0	0	0	3	0	0	0	0	6	0	1	0
HOP	0 0 4					×	×		0	0	0	3	0	0	0	0	6	0	0	0	4	0	0	0	1	0	0	1	4
TRA	0 0 5								0	0	0	4	0	0	0	1	0	0	0	0	5	0	0	0	1	2	0	2	0
SUB	0 0 6								0	0	0	5	0	0	0	1	2	0	0	0	6	0	0	0	1	4	0	2	4
PIO	0 0 7								0	0	0	6	0	0	0	1	4	0	0	0	7	0	0	0	1	6	0	3	0
MPH	0 1 0								0	0	0	7	0	0	0	1	6	0	0	1	0	0	0	0	2	0	0	3	4
RSU	0 1 1								0	0	1	0	0	0	0	2	0	0	0	1	1	0	0	0	2	2	0	4	0
TNZ	0 1 2								0	0	1	1	0	0	0	2	2	0	0	1	2	0	0	0	2	4	0	4	4
TMI	0 1 3								0	0	1	2	0	0	0	2	4	0	0	1	3	0	0	0	2	6	0	5	0
HOP	0 1 4					× ×	×		0	0	1	3	0	0	0	2	6	0	0	1	4	0	0	0	3	0	0	5	4
TRA	0 1 5								0	0	1	4	0	0	0	3	0	0	0	1	5	0	0	0	3	2	0	6	0
DIV	0 1 6								0	0	1	5	0	0	0	3	2	0	0	1	6	0	0	0	3	4	0	6	4
STO	0 1 7								0	0	1	6	0	0	0	3	4	0	0	1	7	0	0	0	3	6	0	7	0
HOP	0 2 0				×	×			0	0	1	7	0	0	0	3	6	0	0	2	0	0	0	0	4	0	0	7	4
PIO	0 2 1								0	0	2	0	0	0	0	4	0	0	0	2	1	0	0	0	4	2	1	0	0
TNZ	0 2 2								0	0	2	1	0	0	0	4	2	0	0	2	2	0	0	0	4	4	1	0	4
TMI	0 2 3								0	0	2	2	0	0	0	4	4	0	0	2	3	0	0	0	4	6	1	1	0
HOP	0 2 4				×	×	×		0	0	2	3	0	0	0	4	6	0	0	2	4	0	0	0	5	0	1	1	4
PIO	0 2 5								0	0	2	4	0	0	0	5	0	0	0	2	5	0	0	0	5	2	1	2	0
AND	0 2 6								0	0	2	5	0	0	0	5	2	0	0	2	6	0	0	0	5	4	1	2	4
SHF	0 2 7					*			0	0	2	6	0	0	0	5	4	0	0	2	7	0	0	0	5	6	1	3	0
MPY	0 3 0								0	0	2	7	0	0	0	5	6	0	0	3	0	0	0	0	6	0	1	3	4
STO	0 3 1								0	0	3	0	0	0	0	6	0	0	0	3	1	0	0	0	6	2	1	4	0
TNZ	0 3 2								0	0	3	1	0	0	0	6	2	0	0	3	2	0	0	0	6	4	1	4	4
TMI	0 3 3								0	0	3	2	0	0	0	6	4	0	0	3	3	0	0	0	6	6	1	5	0
HOP	0 3 4				× × ×	× ×	×		0	0	3	3	0	0	0	6	6	0	0	3	4	0	0	0	7	0	1	5	4
PIO	0 3 5								0	0	3	4	0	0	0	7	0	0	0	3	5	0	0	0	7	2	1	6	0
ADD	0 3 6								0	0	3	5	0	0	0	7	2	0	0	3	6	0	0	0	7	4	1	6	4
CLA	0 3 7								0	0	3	6	0	0	0	7	4	0	0	3	7	0	0	0	7	6	1	7	0
HOP	0 4 0				×	×			0	0	3	7	0	0	0	7	6	0	0	4	0	0	0	1	0	0	1	7	4
TRA	0 4 1								0	0	4	0	0	0	1	0	0	0	0	4	1	0	0	1	0	2	2	0	0
HOP	0 4 2	×			×	×			0	0	4	1	0	0	1	0	2	0	0	4	2	0	0	1	0	4	2	0	4
TRA	0 4 3								0	0	4	2	0	0	1	0	4	0	0	4	3	0	0	1	0	6	2	1	0
HOP	0 4 4				×	×	×		0	0	4	3	0	0	1	0	6	0	0	4	4	0	0	1	1	0	2	1	4
TRA	0 4 5								0	0	4	4	0	0	1	1	0	0	0	4	5	0	0	1	1	2	2	2	0
SUB	0 4 6								0	0	4	5	0	0	1	1	2	0	0	4	6	0	0	1	1	4	2	2	4
PIO	0 4 7								0	0	4	6	0	0	1	1	4	0	0	4	7	0	0	1	1	6	2	3	0
MPH	0 5 0								0	0	4	7	0	0	1	1	6	0	0	5	0	0	0	1	2	0	2	3	4
RSU	0 5 1								0	0	5	0	0	0	1	2	0	0	0	5	1	0	0	1	2	2	2	4	0
TNZ	0 5 2								0	0	5	1	0	0	1	2	2	0	0	5	2	0	0	1	2	4	2	4	4
TMI	0 5 3								0	0	5	2	0	0	1	2	4	0	0	5	3	0	0	1	2	6	2	5	0
HOP	0 5 4				×	× ×	×		0	0	5	3	0	0	1	2	6	0	0	5	4	0	0	1	3	0	2	5	4
TRA	0 5 5								0	0	5	4	0	0	1	3	0	0	0	5	5	0	0	1	3	2	2	6	0
DIV	0 5 6								0	0	5	5	0	0	1	3	2	0	0	5	6	0	0	1	3	4	2	6	4
STO	0 5 7								0	0	5	6	0	0	1	3	4	0	0	5	7	0	0	1	3	6	2	7	0
HOP	0 6 0				× ×	× ×			0	0	5	7	0	0	1	3	6	0	0	6	0	0	0	1	4	0	2	7	4
PIO	0 6 1								0	0	6	0	0	0	1	4	0	0	0	6	1	0	0	1	4	2	3	0	0
TNZ	0 6 2								0	0	6	1	0	0	1	4	2	0	0	6	2	0	0	1	4	4	3	0	4
TMI	0 6 3								0	0	6	2	0	0	1	4	4	0	0	6	3	0	0	1	4	6	3	1	0
HOP	0 6 4				× ×	× ×	×		0	0	6	3	0	0	1	4	6	0	0	6	4	0	0	1	5	0	3	1	4
PIO	0 6 5								0	0	6	4	0	0	1	5	0	0	0	6	5	0	0	1	5	2	3	2	0

Figure 8-2. Self Check Wired In Program Listing (Sheet 1 of 5)

Instruction	Instruction Address	Instruction Module	Syllable	Instruction Duplex	Instruction Sector	Data Module	Data Duplex	Data Sector	Self Check AI3									Self Check TRS									Self Check AI3 Instruction Address		
		3 2 1			4 3 2 1	3 2 1		4 3 2 1	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	A9-A7	A6-A4	A3-A1
AND	0 6 6					* *	*		0	0 6 5	0	0	1	5	2			0	0 6	6	0	0	1	5	4		3	2	4
SHF	0 6 7								0	0 6 6	0	0	1	5	4			0	0 6	7	0	0	1	5	6		3	3	0
MPY	0 7 0								0	0 6 7	0	0	1	5	6			0	0 7	0	0	0	1	6	0		3	3	4
STO	0 7 1								0	0 7 0	0	0	1	6	0			0	0 7	1	0	0	1	6	2		3	4	0
TNZ	0 7 2								0	0 7 1	0	0	1	6	2			0	0 7	2	0	0	1	6	4		3	4	4
TMI	0 7 3								0	0 7 2	0	0	1	6	4			0	0 7	3	0	0	1	6	6		3	5	0
HOP	0 7 4				× × × ×	× × ×	×		0	0 7 3	0	0	1	6	6			0	0 7	4	0	0	1	7	0		3	5	4
PIO	0 7 5								0	0 7 4	0	0	1	7	0			0	0 7	5	0	0	1	7	2		3	6	0
ADD	0 7 6								0	0 7 5	0	0	1	7	2			0	0 7	6	0	0	1	7	4		3	6	4
CLA	0 7 7								0	0 7 6	0	0	1	7	4			0	0 7	7	0	0	1	7	6		3	7	0
HOP	1 0 0		×					×	0	0 7 7	0	0	1	7	6			0	1 0	0	0	0	2	0	0		3	7	4
TRA	1 0 1								0	1 0 0	0	0	2	0	0			0	1 0	1	0	0	2	0	2		4	0	0
HOP	1 0 2	×	×					×	0	1 0 1	0	0	2	0	2			0	1 0	2	0	0	2	0	4		4	0	4
TRA	1 0 3								0	1 0 2	0	0	2	0	4			0	1 0	3	0	0	2	0	6		4	1	0
HOP	1 0 4		×		×	-	×	×	0	1 0 3	0	0	2	0	6			0	1 0	4	0	0	2	1	0		4	1	4
TRA	1 0 5								0	1 0 4	0	0	2	1	0			0	1 0	5	0	0	2	1	2		4	2	0
SUB	1 0 6								0	1 0 5	0	0	2	1	2			0	1 0	6	0	0	2	1	4		4	2	4
PIO	1 0 7								0	1 0 6	0	0	2	1	4			0	1 0	7	0	0	2	1	6		4	3	0
MPH	1 1 0								0	1 0 7	0	0	2	1	6			0	1 1	0	0	0	2	2	0		4	3	4
RSU	1 1 1								0	1 1 0	0	0	2	2	0			0	1 1	1	0	0	2	2	2		4	4	0
TNZ	1 1 2								0	1 1 1	0	0	2	2	2			0	1 1	2	0	0	2	2	4		4	4	4
TMI	1 1 3								0	1 1 2	0	0	2	2	4			0	1 1	3	0	0	2	2	6		4	5	0
HOP	1 1 4		×		× ×	×	×	×	0	1 1 3	0	0	2	2	6			0	1 1	4	0	0	2	3	0		4	5	4
TRA	1 1 5								0	1 1 4	0	0	2	3	0			0	1 1	5	0	0	2	3	2		4	6	0
DIV	1 1 6								0	1 1 5	0	0	2	3	2			0	1 1	6	0	0	2	3	4		4	6	4
STO	1 1 7								0	1 1 6	0	0	2	3	4			0	1 1	7	0	0	2	3	6		4	7	0
HOP	1 2 0		×		×	×		×	0	1 1 7	0	0	2	3	6			0	1 2	0	0	0	2	4	0		4	7	4
PIO	1 2 1								0	1 2 0	0	0	2	4	0			0	1 2	1	0	0	2	4	2		5	0	0
TNZ	1 2 2								0	1 2 1	0	0	2	4	2			0	1 2	2	0	0	2	4	4		5	0	4
TMI	1 2 3								0	1 2 2	0	0	2	4	4			0	1 2	3	0	0	2	4	6		5	1	0
HOP	1 2 4		×		× ×	×	×	×	0	1 2 3	0	0	2	4	6			0	1 2	4	0	0	2	5	0		5	1	4
PIO	1 2 5								0	1 2 4	0	0	2	5	0			0	1 2	5	0	0	2	5	2		5	2	0
AND	1 2 6								0	1 2 5	0	0	2	5	2			0	1 2	6	0	0	2	5	4		5	2	4
SHF	1 2 7								0	1 2 6	0	0	2	5	4			0	1 2	7	0	0	2	5	6		5	3	0
MPY	1 3 0								0	1 2 7	0	0	2	5	6			0	1 3	0	0	0	2	6	0		5	3	4
STO	1 3 1								0	1 3 0	0	0	2	6	0			0	1 3	1	0	0	2	6	2		5	4	0
TNZ	1 3 2								0	1 3 1	0	0	2	6	2			0	1 3	2	0	0	2	6	4		5	4	4
TMI	1 3 3								0	1 3 2	0	0	2	6	4			0	1 3	3	0	0	2	6	6		5	5	0
HOP	1 3 4		×		× × ×	× ×	×	×	0	1 3 3	0	0	2	6	6			0	1 3	4	0	0	2	7	0		5	5	4
PIO	1 3 5								0	1 3 4	0	0	2	7	0			0	1 3	5	0	0	2	7	2		5	6	0
ADD	1 3 6								0	1 3 5	0	0	2	7	2			0	1 3	6	0	0	2	7	4		5	6	4
CLA	1 3 7								0	1 3 6	0	0	2	7	4			0	1 3	7	0	0	2	7	6		5	7	0
HOP	1 4 0		×		×	×		×	0	1 3 7	0	0	2	7	6			0	1 4	0	0	0	3	0	0		5	7	4
TRA	1 4 1								0	1 4 0	0	0	3	0	0			0	1 4	1	0	0	3	0	2		6	0	0
HOP	1 4 2	×	×		×	×		×	0	1 4 1	0	0	3	0	2			0	1 4	2	0	0	3	0	4		6	0	4
TRA	1 4 3								0	1 4 2	0	0	3	0	4			0	1 4	3	0	0	3	0	6		6	1	0
HOP	1 4 4		×		× ×	×	×	×	0	1 4 3	0	0	3	0	6			0	1 4	4	0	0	3	1	0		6	1	4
TRA	1 4 5								0	1 4 4	0	0	3	1	0			0	1 4	5	0	0	3	1	2		6	2	0
SUB	1 4 6								0	1 4 5	0	0	3	1	2			0	1 4	6	0	0	3	1	4		6	2	4
PIO	1 4 7								0	1 4 6	0	0	3	1	4			0	1 4	7	0	0	3	1	6		6	3	0
MPH	1 5 0								0	1 4 7	0	0	3	1	6			0	1 5	0	0	0	3	2	0		6	3	4
RSU	1 5 1								0	1 5 0	0	0	3	2	0			0	1 5	1	0	0	3	2	2		6	4	0
TNZ	1 5 2								0	1 5 1	0	0	3	2	2			0	1 5	2	0	0	3	2	4		6	4	4
TMI	1 5 3								0	1 5 2	0	0	3	2	4			0	1 5	3	0	0	3	2	6		6	5	0

Figure 8-2. Self Check Wired In Program Listing (Sheet 2)

Instruction	Instruction Address	Instruction Module	Syllable	Instruction Duplex	Instruction Sector	Data Module	Data Duplex	Data Sector	Self Check AI3									Self Check TRS									Self Check AI3 Instruction Address		
		3 2 1			4 3 2 1	3 2 1		4 3 2 1	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	A9-A7	A6-A4	A3-A1
HOP	1 5 4		×		× × ×	× ×	×	×	0	1	5	3	0	0	3	2	6	0	1	5	4	0	0	3	3	0	6	5	4
TRA	1 5 5								0	1	5	4	0	0	3	3	0	0	1	5	5	0	0	3	3	2	6	6	0
DIV	1 5 6								0	1	5	5	0	0	3	3	2	0	1	5	6	0	0	3	3	4	6	6	4
STO	1 5 7								0	1	5	6	0	0	3	3	4	0	1	5	7	0	0	3	3	6	6	7	0
HOP	1 6 0		×		× ×	× ×		×	0	1	5	7	0	0	3	3	6	0	1	6	0	0	0	3	4	0	6	7	4
PIO	1 6 1								0	1	6	0	0	0	3	4	0	0	1	6	1	0	0	3	4	2	7	0	0
TNZ	1 6 2								0	1	6	1	0	0	3	4	2	0	1	6	2	0	0	3	4	4	7	0	4
TMI	1 6 3								0	1	6	2	0	0	3	4	4	0	1	6	3	0	0	3	4	6	7	1	0
HOP	1 6 4		×		× × ×	× ×	×	×	0	1	6	3	0	0	3	4	6	0	1	6	4	0	0	3	5	0	7	1	4
PIO	1 6 5								0	1	6	4	0	0	3	5	0	0	1	6	5	0	0	3	5	2	7	2	0
AND	1 6 6								0	1	6	5	0	0	3	5	2	0	1	6	6	0	0	3	5	4	7	2	4
SHF	1 6 7					* *	*	*	0	1	6	6	0	0	3	5	4	0	1	6	7	0	0	3	5	6	7	3	0
MPY	1 7 0								0	1	6	7	0	0	3	5	6	0	1	7	0	0	0	3	6	0	7	3	4
STO	1 7 1								0	1	7	0	0	0	3	6	0	0	1	7	1	0	0	3	6	2	7	4	0
TNZ	1 7 2								0	1	7	1	0	0	3	6	2	0	1	7	2	0	0	3	6	4	7	4	4
TMI	1 7 3								0	1	7	2	0	0	3	6	4	0	1	7	3	0	0	3	6	6	7	5	0
HOP	1 7 4								0	1	7	3	0	0	3	6	6	0	1	7	4	0	0	3	7	0	7	5	4
PIO	1 7 5								0	1	7	4	0	0	3	7	0	0	1	7	5	0	0	3	7	2	7	6	0
ADD	1 7 6								0	1	7	5	0	0	3	7	2	0	1	7	6	0	0	3	7	4	7	6	4
CLA	1 7 7								0	1	7	6	0	0	3	7	4	0	1	7	7	0	0	3	7	6	7	7	0
HOP	2 0 0							×	0	1	7	7	0	0	3	7	6	0	2	0	0	0	0	4	0	0	7	7	4
TRA	2 0 1								0	2	0	0	0	0	4	0	0	0	2	0	1	0	0	4	0	2	0	0	0
HOP	2 0 2	×						×	0	2	0	1	0	0	4	0	2	0	2	0	2	0	0	4	0	4	0	0	4
TRA	2 0 3								0	2	0	2	0	0	4	0	4	0	2	0	3	0	0	4	0	6	0	1	0
HOP	2 0 4						×	×	0	2	0	3	0	0	4	0	6	0	2	0	4	0	0	4	1	0	0	1	4
TRA	2 0 5								0	2	0	4	0	0	4	1	0	0	2	0	5	0	0	4	1	2	0	2	0
SUB	2 0 6								0	2	0	5	0	0	4	1	2	0	2	0	6	0	0	4	1	4	0	2	4
PIO	2 0 7								0	2	0	6	0	0	4	1	4	0	2	0	7	0	0	4	1	6	0	3	0
MPH	2 1 0								0	2	0	7	0	0	4	1	6	0	2	1	0	0	0	4	2	0	0	3	4
RSU	2 1 1								0	2	1	0	0	0	4	2	0	0	2	1	1	0	0	4	2	2	0	4	0
TNZ	2 1 2								0	2	1	1	0	0	4	2	2	0	2	1	2	0	0	4	2	4	0	4	4
TMI	2 1 3								0	2	1	2	0	0	4	2	4	0	2	1	3	0	0	4	2	6	0	5	0
HOP	2 1 4						×	×	0	2	1	3	0	0	4	2	6	0	2	1	4	0	0	4	3	0	0	5	4
TRA	2 1 5								0	2	1	4	0	0	4	3	0	0	2	1	5	0	0	4	3	2	0	6	0
DIV	2 1 6								0	2	1	5	0	0	4	3	2	0	2	1	6	0	0	4	3	4	0	6	4
STO	2 1 7								0	2	1	6	0	0	4	3	4	0	2	1	7	0	0	4	3	6	0	7	0
HOP	2 2 0				×	×		×	0	2	1	7	0	0	4	3	6	0	2	2	0	0	0	4	4	0	0	7	4
PIO	2 2 1								0	2	2	0	0	0	4	4	0	0	2	2	1	0	0	4	4	2	1	0	0
TNZ	2 2 2								0	2	2	1	0	0	4	4	2	0	2	2	2	0	0	4	4	4	1	0	4
TMI	2 2 3								0	2	2	2	0	0	4	4	4	0	2	2	3	0	0	4	4	6	1	1	0
HOP	2 2 4				×	×	×	×	0	2	2	3	0	0	4	4	6	0	2	2	4	0	0	4	5	0	1	1	4
PIO	2 2 5								0	2	2	4	0	0	4	5	0	0	2	2	5	0	0	4	5	2	1	2	0
AND	2 2 6								0	2	2	5	0	0	4	5	2	0	2	2	6	0	0	4	5	4	1	2	4
SHF	2 2 7					*	*	*	0	2	2	6	0	0	4	5	4	0	2	2	7	0	0	4	5	6	1	3	0
MPY	2 3 0								0	2	2	7	0	0	4	5	6	0	2	3	0	0	0	4	6	0	1	3	4
STO	2 3 1								0	2	3	0	0	0	4	6	0	0	2	3	1	0	0	4	6	2	1	4	0
TNZ	2 3 2								0	2	3	1	0	0	4	6	2	0	2	3	2	0	0	4	6	4	1	4	4
TMI	2 3 3								0	2	3	2	0	0	4	6	4	0	2	3	3	0	0	4	6	6	1	5	0
HOP	2 3 4				× × ×	× ×	×	×	0	2	3	3	0	0	4	6	6	0	2	3	4	0	0	4	7	0	1	5	4
PIO	2 3 5								0	2	3	4	0	0	4	7	0	0	2	3	5	0	0	4	7	2	1	6	0
ADD	2 3 6								0	2	3	5	0	0	4	7	2	0	2	3	6	0	0	4	7	4	1	6	4
CLA	2 3 7								0	2	3	6	0	0	4	7	4	0	2	3	7	0	0	4	7	6	1	7	0
HOP	2 4 0				×	×		×	0	2	3	7	0	0	4	7	6	0	2	4	0	0	0	5	0	0	1	7	4
TRA	2 4 1								0	2	4	0	0	0	5	0	0	0	2	4	1	0	0	5	0	2	2	0	0

Figure 8-2. Self Check Wired In Program Listing (Sheet 3)

Instruction	Instruction Address	Instruction Module	Syllable	Instruction Duplex	Instruction Sector	Data Module	Data Duplex	Data Sector	Self Check AI3									Self Check TRS									Self Check AI3 Instruction Address		
		3 2 1			4 3 2 1	3 2 1		4 3 2 1	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	A9-A7	A6-A4	A3-A1
HOP	2 4 2	×			×	×		×	0	2	4	1	0	0	5	0	2	0	2	4	2	0	0	5	0	4	2	0	4
TRA	2 4 3								0	2	4	2	0	0	5	0	4	0	2	4	3	0	0	5	0	6	2	1	0
HOP	2 4 4				× ×	×	×	×	0	2	4	3	0	0	5	0	6	0	2	4	4	0	0	5	1	0	2	1	4
TRA	2 4 5								0	2	4	4	0	0	5	1	0	0	2	4	5	0	0	5	1	2	2	2	0
SUB	2 4 6								0	2	4	5	0	0	5	1	2	0	2	4	6	0	0	5	1	4	2	2	4
PIO	2 4 7								0	2	4	6	0	0	5	1	4	0	2	4	7	0	0	5	1	6	2	3	0
MPH	2 5 0								0	2	4	7	0	0	5	1	6	0	2	5	0	0	0	5	2	0	2	3	4
RSU	2 5 1								0	2	5	0	0	0	5	2	0	0	2	5	1	0	0	5	2	2	2	4	0
TNZ	2 5 2								0	2	5	1	0	0	5	2	2	0	2	5	2	0	0	5	2	4	2	4	4
TMI	2 5 3								0	2	5	2	0	0	5	2	4	0	2	5	3	0	0	5	2	6	2	5	0
HOP	2 5 4				× × ×	× ×	×	×	0	2	5	3	0	0	5	2	6	0	2	5	4	0	0	5	3	0	2	5	4
TRA	2 5 5								0	2	5	4	0	0	5	3	0	0	2	5	5	0	0	5	3	2	2	6	0
DIV	2 5 6								0	2	5	5	0	0	5	3	2	0	2	5	6	0	0	5	3	4	2	6	4
STO	2 5 7								0	2	5	6	0	0	5	3	4	0	2	5	7	0	0	5	3	6	2	7	0
HOP	2 6 0				× ×	× ×		×	0	2	5	7	0	0	5	3	6	0	2	6	0	0	0	5	4	0	2	7	4
PIO	2 6 1								0	2	6	0	0	0	5	4	0	0	2	6	1	0	0	5	4	2	3	0	0
TNZ	2 6 2								0	2	6	1	0	0	5	4	2	0	2	6	2	0	0	5	4	4	3	0	4
TMI	2 6 3								0	2	6	2	0	0	5	4	4	0	2	6	3	0	0	5	4	6	3	1	0
HOP	2 6 4				× × ×	× ×		×	0	2	6	3	0	0	5	4	6	0	2	6	4	0	0	5	5	0	3	1	4
PIO	2 6 5								0	2	6	4	0	0	5	5	0	0	2	6	5	0	0	5	5	2	3	2	0
AND	2 6 6								0	2	6	5	0	0	5	5	2	0	2	6	6	0	0	5	5	4	3	2	4
SHF	2 6 7					*	*	* *	0	2	6	6	0	0	5	5	4	0	2	6	7	0	0	5	5	6	3	3	0
MPY	2 7 0								0	2	6	7	0	0	5	5	6	0	2	7	0	0	0	5	6	0	3	3	4
STO	2 7 1								0	2	7	0	0	0	5	6	0	0	2	7	1	0	0	5	6	2	3	4	0
TNZ	2 7 2								0	2	7	1	0	0	5	6	2	0	2	7	2	0	0	5	6	4	3	4	4
TMI	2 7 3								0	2	7	2	0	0	5	6	4	0	2	7	3	0	0	5	6	6	3	5	0
HOP	2 7 4				× × × ×	× × ×	×	×	0	2	7	3	0	0	5	6	6	0	2	7	4	0	0	5	7	0	3	5	4
PIO	2 7 5								0	2	7	4	0	0	5	7	0	0	2	7	5	0	0	5	7	2	3	6	0
ADD	2 7 6								0	2	7	5	0	0	5	7	2	0	2	7	6	0	0	5	7	4	3	6	4
CLA	2 7 7								0	2	7	6	0	0	5	7	4	0	2	7	7	0	0	5	7	6	3	7	0
HOP	3 0 0		×					× ×	0	2	7	7	0	0	5	7	6	0	3	0	0	0	0	6	0	0	3	7	4
TRA	3 0 1								0	3	0	0	0	0	6	0	0	0	3	0	1	0	0	6	0	2	4	0	0
HOP	3 0 2	×	×					× ×	0	3	0	1	0	0	6	0	2	0	3	0	2	0	0	6	0	4	4	0	4
TRA	3 0 3								0	3	0	2	0	0	6	0	4	0	3	0	3	0	0	6	0	6	4	1	0
HOP	3 0 4		×		×		×	× ×	0	3	0	3	0	0	6	0	6	0	3	0	4	0	0	6	1	0	4	1	4
TRA	3 0 5								0	3	0	4	0	0	6	1	0	0	3	0	5	0	0	6	1	2	4	2	0
SUB	3 0 6								0	3	0	5	0	0	6	1	2	0	3	0	6	0	0	6	1	4	4	2	4
PIO	3 0 7								0	3	0	6	0	0	6	1	4	0	3	0	7	0	0	6	1	6	4	3	0
MPH	3 1 0								0	3	0	7	0	0	6	1	6	0	3	1	0	0	0	6	2	0	4	3	4
RSU	3 1 1								0	3	1	0	0	0	6	2	0	0	3	1	1	0	0	6	2	2	4	4	0
TNZ	3 1 2								0	3	1	1	0	0	6	2	2	0	3	1	2	0	0	6	2	4	4	4	4
TMI	3 1 3								0	3	1	2	0	0	6	2	4	0	3	1	3	0	0	6	2	6	4	5	0
HOP	3 1 4		×		× ×		×	× ×	0	3	1	3	0	0	6	2	6	0	3	1	4	0	0	6	3	0	4	5	4
TRA	3 1 5								0	3	1	4	0	0	6	3	0	0	3	1	5	0	0	6	3	2	4	6	0
DIV	3 1 6								0	3	1	5	0	0	6	3	2	0	3	1	6	0	0	6	3	4	4	6	4
STO	3 1 7								0	3	1	6	0	0	6	3	4	0	3	1	7	0	0	6	3	6	4	7	0
HOP	3 2 0		×		×	×		× ×	0	3	1	7	0	0	6	3	6	0	3	2	0	0	0	6	4	0	4	7	4
PIO	3 2 1								0	3	2	0	0	0	6	4	0	0	3	2	1	0	0	6	4	2	5	0	0
TNZ	3 2 2								0	3	2	1	0	0	6	4	2	0	3	2	2	0	0	6	4	4	5	0	4
TMI	3 2 3								0	3	2	2	0	0	6	4	4	0	3	2	3	0	0	6	4	6	5	1	0
HOP	3 2 4		×		× ×	×	×	× ×	0	3	2	3	0	0	6	4	6	0	3	2	4	0	0	6	5	0	5	1	4
PIO	3 2 5								0	3	2	4	0	0	6	5	0	0	3	2	5	0	0	6	5	2	5	2	0
AND	3 2 6								0	3	2	5	0	0	6	5	2	0	3	2	6	0	0	6	5	4	5	2	4
SHF	3 2 7					*	*	* *	0	3	2	6	0	0	6	5	4	0	3	2	7	0	0	6	5	6	5	3	0

Figure 8-2. Self Check Wired In Program Listing (Sheet 4)

Instruction	Instruction Address	Instruction Module	Syllable	Instruction Duplex	Instruction Sector	Data Module	Data Duplex	Data Sector	Self Check AI3									Self Check TRS									Self Check AI3 Instruction Address		
		3 2 1			4 3 2 1	3 2 1		4 3 2 1	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	S-2	3-5	6-8	9-11	12-14	15-17	18-20	21-23	24-26	A9-A7	A6-A4	A3-A1
MPY	3 3 0								0	3	2	7	0	0	6	5	6	0	3	3	0	0	0	6	6	0	5	3	4
STO	3 3 1								0	3	3	0	0	0	6	6	0	0	3	3	1	0	0	6	6	2	5	4	0
TNZ	3 3 2								0	3	3	1	0	0	6	6	2	0	3	3	2	0	0	6	6	4	5	4	4
TMI	3 3 3								0	3	3	2	0	0	6	6	4	0	3	3	3	0	0	6	6	6	5	5	0
HOP	3 3 4								0	3	3	3	0	0	6	6	6	0	3	3	4	0	0	6	7	0	5	5	4
PIO	3 3 5								0	3	3	4	0	0	6	7	0	0	3	3	5	0	0	6	7	2	5	6	0
ADD	3 3 6								0	3	3	5	0	0	6	7	2	0	3	3	6	0	0	6	7	4	5	6	4
CLA	3 3 7								0	3	3	6	0	0	6	7	4	0	3	3	7	0	0	6	7	6	5	7	0
HOP	3 4 0		×		×	×		× ×	0	3	3	7	0	0	6	7	6	0	3	4	0	0	0	7	0	0	5	7	4
TRA	3 4 1								0	3	4	0	0	0	7	0	0	0	3	4	1	0	0	7	0	2	6	0	0
HOP	3 4 2	×	×		×	×		× ×	0	3	4	1	0	0	7	0	2	0	3	4	2	0	0	7	0	4	6	0	4
TRA	3 4 3								0	3	4	2	0	0	7	0	4	0	3	4	3	0	0	7	0	6	6	1	0
HOP	3 4 4		×		× ×	×	×	× ×	0	3	4	3	0	0	7	0	6	0	3	4	4	0	0	7	1	0	6	1	4
TRA	3 4 5								0	3	4	4	0	0	7	1	0	0	3	4	5	0	0	7	1	2	6	2	0
SUB	3 4 6								0	3	4	5	0	0	7	1	2	0	3	4	6	0	0	7	1	4	6	2	4
PIO	3 4 7								0	3	4	6	0	0	7	1	4	0	3	4	7	0	0	7	1	6	6	3	0
MPH	3 5 0								0	3	4	7	0	0	7	1	6	0	3	5	0	0	0	7	2	0	6	3	4
RSU	3 5 1								0	3	5	0	0	0	7	2	0	0	3	5	1	0	0	7	2	2	6	4	0
TNZ	3 5 2								0	3	5	1	0	0	7	2	2	0	3	5	2	0	0	7	2	4	6	4	4
TMI	3 5 3								0	3	5	2	0	0	7	2	4	0	3	5	3	0	0	7	2	6	6	5	0
HOP	3 5 4		×		× ×	×	×	× ×	0	3	5	3	0	0	7	2	6	0	3	5	4	0	0	7	3	0	6	5	4
TRA	3 5 5								0	3	5	4	0	0	7	3	0	0	3	5	5	0	0	7	3	2	6	6	0
DIV	3 5 6								0	3	5	5	0	0	7	3	2	0	3	5	6	0	0	7	3	4	6	6	4
STO	3 5 7								0	3	5	6	0	0	7	3	4	0	3	5	7	0	0	7	3	6	6	7	0
HOP	3 6 0		×		× ×	× ×		× ×	0	3	5	7	0	0	7	3	6	0	3	6	0	0	0	7	4	0	6	7	4
PIO	3 6 1								0	3	6	0	0	0	7	4	0	0	3	6	1	0	0	7	4	2	7	0	0
TNZ	3 6 2								0	3	6	1	0	0	7	4	2	0	3	6	2	0	0	7	4	4	7	0	4
TMI	3 6 3								0	3	6	2	0	0	7	4	4	0	3	6	3	0	0	7	4	6	7	1	0
HOP	3 6 4		×		× ×	× ×	×	× ×	0	3	6	3	0	0	7	4	6	0	3	6	4	0	0	7	5	0	7	1	4
PIO	3 6 5								0	3	6	4	0	0	7	5	0	0	3	6	5	0	0	7	5	2	7	2	0
AND	3 6 6								0	3	6	5	0	0	7	5	2	0	3	6	6	0	0	7	5	4	7	2	4
SHF	3 6 7					* *	*	* *	0	3	6	6	0	0	7	5	4	0	3	6	7	0	0	7	5	6	7	3	0
MPY	3 7 0								0	3	6	7	0	0	7	5	6	0	3	7	0	0	0	7	6	0	7	3	4
STO	3 7 1								0	3	7	0	0	0	7	6	0	0	3	7	1	0	0	7	6	2	7	4	0
TNZ	3 7 2								0	3	7	1	0	0	7	6	2	0	3	7	2	0	0	7	6	4	7	4	4
TMI	3 7 3								0	3	7	2	0	0	7	6	4	0	3	7	3	0	0	7	6	6	7	5	0
HOP	3 7 4		×		× × × ×	× × ×	×	× ×	0	3	7	3	0	0	7	6	6	0	3	7	4	0	0	7	7	0	7	5	4
PIO	3 7 5								0	3	7	4	0	0	7	7	0	0	3	7	5	0	0	7	7	2	7	6	0
ADD	3 7 6								0	3	7	5	0	0	7	7	2	0	3	7	6	0	0	7	7	4	7	6	4
CLA	3 7 7								0	3	7	6	0	0	7	7	4	0	3	7	7	0	0	7	7	6	7	7	0

*CDS Code

Figure 8-2. Self Check Wired In Program Listing (Sheet 5)

SECTION IX

REPAIR

9-1. SCOPE.

9-2. This section contains (1) lists of replaceable LVDCME assemblies and parts; (2) descriptions of recommended methods of replacement and repair of these assemblies and parts; (3) a list of materials required to refurbish the LVDCME exterior surfaces; and (4) a description of recommended methods for refurbishing these surfaces.

9-3. REPLACEABLE ASSEMBLIES AND PARTS.

9-4. Figure 9-1 lists the replaceable LVDCME assemblies. Figures 9-2 through 9-10 list the recommended replaceable parts to be supplied by the International Business Machines Corporation. Figure 9-11 identifies the vendors and their codes as contained in the Federal Supply Code for Manufacturers, Cataloging Handbook H4-1. Reference should be made to the assembly drawings (figures 10-31 thru 10-55) when replacing assemblies.

9-5. REPAIR TECHNIQUES.

9-6. The following paragraphs discuss repair techniques applicable to the LVDCME. Many of the special tools listed and illustrated in Section IV are referenced in these discussions.

9-7. SWITCH ASSEMBLIES.

9-8. As shown on figure 9-12, a switch assembly consists of four basic parts: switch, switch housing, light module, and screen. Switches, blank screens, light modules, and lamp bulbs within the light modules are replaceable parts, as indicated on figures 9-3, 9-4, 9-7, and 9-8; switch housings are not replaceable parts.

9-9. WRAPPED CONNECTIONS.

9-10. The wire wrapped connection is a precision pressure junction. A special wrapping tool wraps the stripped end of a wire tightly around the stationary terminal on a gate assembly. The resulting connection is a highly reliable permanent connection because of the high local residual stresses produced in the wire and terminal. Figure 9-13 illustrates a typical wrapped connection. The following paragraphs discuss the processes for using manual tools to wrap and unwrap connections.

9-11. SECTION OF MATERIALS. Recommended tools for wrapped connections are listed in figure 9-14.

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
01A1	Power Control Panel Assembly	Refer to figure 9-3	
01A2	Tape Control Panel Assembly	Refer to figure 9-4	
01A3	Tape Reader Assembly	Model RR1002-B	16550
01A4	Tape Spooler Assembly	Model RS-500A	16550
01A5	Power Supply	Model M15-50A-0V	09206
01A6	Power Supply	Model M15-15A-0V	09206
01A7	Power Supply	Model M36-10A-0V	09206
01A8	Power Supply	Model M15-10-0V	09206
91A9	Power Sequence Relay Gate Assembly	Refer to figure 10-38*	
01B1	Gate Assembly	Refer to figure 10-38*	
01B2	Gate Assembly	Refer to figure 10-38*	
01B3	Gate Assembly	Refer to figure 10-38*	
01B4	Gate Assembly	Refer to figure 10-38*	
01B5	AC Power Gate Assembly	Refer to figure 9-5	
01B6	Gate Assembly	Refer to figure 10-38*	
01B7	Gate Assembly	Refer to figure 10-38*	
01B8	Module Switching Relay Gate Assembly	Refer to figure 9-6	
02A1	Memory Loader and Data Display Panel Assembly	Refer to figure 9-7	
02A2	Interface Exerciser Panel Assembly	Refer to figure 9-8	
02A3	Connector Panel Assembly	Refer to figure 9-9	
02A4	Power Supply	Model M36-5-0V	09206
02A5	Power Supply	Model M15-5-0V	09206
02A6	Power Supply	Model M15-30A-0V	09206
02A7	Power Supply	Model M15-15A-0V	09206
02A8	Computer Power Sequence Relay Gate Assembly	Refer to figure 9-10	
02A9	Power Supply	Model M15-10-0V	09206
02A10	Power Supply	Model M15-5-0V	09206
02B1	Gate Assembly	Refer to figure 10-38*	
02B2	Gate Assembly	Refer to figure 10-38*	
02B3	Gate Assembly	Refer to figure 10-38*	
02B4	Gate Assembly	Refer to figure 10-38*	
02B5	Gate Assembly	Refer to figure 10-38*	
02B6	Gate Assembly	Refer to figure 10-38*	
02B7	Gate Assembly	Refer to figure 10-38*	
02B8	Delay Line Gate Assembly	Refer to figure 10-38*	

*Note: Figure 10-38 identifies the part numbers of the LVDCME ALD circuit card location charts for each gate assembly by reference designation. These charts define (1) the location of each SMS card in a gate assembly; (2) the IBM part number of each SMS card; and (3) the LVDCME ALD pages on which each SMS card is shown.

Figure 9-1. LVDCME Replaceable Assemblies and Parts

Vendor Code	Part Number	Nomenclature	Description
03640	6901030	Printed Circuit Board Assembly	Refer to figure 10-40
	6901330		Refer to figure 10-41
	6901332		Refer to figure 10-42
	6901336		Refer to figure 10-43
	6901338		Refer to figure 10-44
	6901340		Refer to figure 10-45
	6901342		Refer to figure 10-46
	6901344		Refer to figure 10-47
	6901346		Refer to figure 10-48
	6901348		Refer to figure 10-49
	6901349		Refer to figure 10-50
	6901350		Refer to figure 10-51
	6901354		Refer to figure 10-52
	6901355		Refer to figure 10-53
	6901356		Refer to figure 10-54
	6901358		Refer to figure 10-55

Figure 9-2. Repairable Printed Circuit Board (SMS Card) Assemblies

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
DS1 thru DS9	Lamp bulb	6028030	03640
R1, R2	Potentiometer	6078360	
R3, R4	Potentiometer	6078362	
R5 thru R7	Potentiometer	6078360	
R8 thru R10	Potentiometer	6078362	
R11, R12	Resistor	6078367	
R13	Resistor	6078364	
R14 thru R16	Resistor	6078368	
R17	Resistor	6078369	
R18	Resistor	6078363	
R19	Resistor	6078365	
R20	Resistor	6078409	
R21 thru R52	Resistor	6011557	
S1	Switch (Light module 6079731)	6078534	
S2	Switch (Light module 6079733)	6078534	
S3	Switch (Light module 6079731)	6078534	

Figure 9-3. Power Control Panel Assembly (01A1) Replaceable Parts (Sheet 1 of 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
S4	Switch (Light module 6079733)	6078534	03640
S5	Switch	6080135	
S6	Switch (Light module 6079731)	6078534	
S7	Switch (Light module 6079733)	6078790	
TP1 thru TP7	Test Point	6015339	
TP8 thru TP15	Test Point	6015537	
TP16 thru TP45	Test Point	6015339	
TP46 thru TP51	Test Point	6015537	
XDS5	Light Module	6078419	
XDS8	Light Module	6079726	
XDS9	Light Module	6079281	
Note: Use switch housing part number 6078422 and screen 6078943 for all switches.			

Figure 9-3. Power Control Panel Assembly (01A1) Replaceable Parts (Sheet 2)

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR9	Diode	492543	88360
DS1 thru DS21	Lamp bulb	6078990	03640
S1, S2	Switch (Light module 6079732)	6078534	
S3, S4	Switch (Light module 6079719)	6078529	
S5 thru S9	Switch (Light module 6079417)	6078534	
S10	Switch (Light module 6079730)	6078529	
S11	Switch (Light module 6079732)	6078529	
S12	Switch (Light module 6079719)	6078529	
S13, S14	Switch (Light module 6079732)	6078529	
S15	Switch (Light module 6079730)	6078534	
S16	Switch (Light module 6079733)	6078534	
S17	Switch (Light module 6079732)	6078529	
S18	Switch (Light module 6079732)	6078534	
S19	Switch (Light module 6079719)	6078534	
S20	Switch (Light module 6079723)	6078529	
S21	Switch (Light module 6079730)	6078529	
TP1 thru TP52 and GRD (4)	Test Point	6015339 (Red) 6015537 (Black)	
Note: Use switch housing part number 6078442 and screen 6078943 for all switches.			

Figure 9-4. Tape Control Panel Assembly (01A2) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
C1	Capacitor	6081074	03640
CB1	Circuit breaker	6078938	
CB2	Circuit breaker	6079224	
CB3	Circuit breaker	6078937	
CB4	Circuit breaker	6078935	
CR1, CR2	Diode	6018033	
FL1	Filter	6079865	
J1	Connector	6901040	
K1, K2	Relay	6078431	
M1	Meter	6018105	
R1 thru R4	Resistor	6078366	
R5	Resistor	6078972	
R6 thru R9	Resistor	6041432	
T1	Transformer	6077905	

Figure 9-5. AC Power Gate Assembly (01B5) Replaceable Parts

Reference Designator	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR51	Diode	369218	88360
J1	Connector	6073936	03640
J2	Connector	6078451	
J3	Connector	6078450	
J4	Connector	6075989	
K1 thru K37	Relay	6017242	
TB1, TB2	Connector	6073067	
XK1 thru XK37	Connector	6016600	

Figure 9-6. Module Switching Relay Gate Assembly (01B8) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
DS1 thru DS78	Lamp bulb	6078990	03640
S1	Switch (Light module 6078420)	6078534	
S2 thru S8	Switch (Light module 6079720)	6078534	
S9	Switch (Light module 6078420)	6078534	
S10 thru S34	Switch (Light module 6079720)	6078534	
S35	Switch (Light module 6079732)	6078534	
S36	Switch (Light module 6079730)	6078529	
S37 thru S40	Switch (Light module 6079722)	6078534	
S41 thru S45	Switch (Light module 6079721)	6078534	
S46 thru S50	Switch (Light module 6079722)	5078534	
S51 thru S54	Switch (Light module 6079721)	6078534	
S55 thru S58	Switch (Light module 6079722)	6078534	
S59 thru S62	Switch (Light module 6079721)	6078534	
S63 thru S65	Switch (Light module 6079732)	6078534	
S66	Switch (Light module 6079719)	6078534	
S67 thru S70	Switch (Light module 6079732)	6078534	
S71	Switch (Light module 6079719)	6078534	
S72	Switch (Light module 6079732)	6078534	
S73, S74	Switch (Light module 6079719)	6078534	
S75	Switch	6035437	
S76	Switch (Light module 6079732)	6078534	
S77	Switch (Light module 6079719)	6078534	
S78	Switch	6035437	
S79	Switch (Light module 6079719)	6078529	
S80	Switch (Light module 6079719)	6078534	
XDS1	Light module	6078419	
XDS6	Light module	6079732	
XDS24	Light module	6079724	
XDS40	Light module	6079729	
XDS41	Light module	6079728	

Note: For all switches except S75 and S78 use switch housing part number 6078442 and screen 6078943.

Figure 9-7. Memory Loader and Data Display Panel Assembly (02A1) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR6	Diode	492457	88360
DS1 thru DS91	Lamp bulb	6078990	03640
R1, R2	Resistor	6017937	
S1	Switch (Light module 6079732)	6078534	
S2 thru S27	Switch (Light module 6079722)	6078534	
S28	Switch (Light module 6079732)	6078534	
S29, S30	Switch (Light module 6079732)	6078529	
S31	Switch (Light module 6079719)	6078529	
S32	Switch (Light module 6079732)	6078534	
S33 thru S35	Switch (Light module 6079719)	6078534	
S36	Switch (Light module 6079719)	6078529	
S37	Switch (Light module 6079732)	6078529	
S38 thru S58	Switch (Light module 6079719)	6078534	
S59	Switch (Light module 6079730)	6078529	
S60 thru S62	Switch	6035437	
S63	Switch (Light module 6079732)	6078534	
S64	Switch (Light module 6079719)	6078529	
S65	Switch (Light module 6079732)	6078534	

Note: For all switches except S60, S61 and S62 use switch housing part number 6078442 and screen 6078943.

Figure 9-8. Interface Exerciser Panel Assembly (02A2) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
C1, C2	Capacitor	6079338	03640
CR1	Diode	6018033	
J1, J2	Connector	6070209	
J3, J4	Connector	6078536	
J5	Connector	6076337	
J6	Connector	6076335	
J7	Connector	6071957	
J8	Connector	6075189	
J9	Connector	6078961	
J10	Connector	6078962	
J11	Connector	6076336	
J12	Connector	6078960	
J13	Connector	6076336	
J14	Connector	6078960	
J15	Connector	6075290	
J16	Connector	6073942	
J17	Connector	6075290	
J18	Connector	6073942	
J19	Connector	6078450	
J20	Connector	6076335	
J21	Connector	6081188	
J22	Connector	6078961	
J23	Connector	6075181	
R1	Resistor	6079323	
R2	Resistor	6079322	
R3	Resistor	6079331	
R4	Resistor	6079332	
R5	Resistor	6079329	
R6	Resistor	6079324	
R7	Resistor	6079325	
R8	Resistor	6079327	
R9	Resistor	6079326	
R10	Resistor	6079328	
R11	Resistor	6079326	
R12 thru R32	Resistor	6041407	
R33 thru R53	Resistor	6079230	
R54	Resistor	6079330	
TP1 thru TP54	Test Point	6015339	
TP55	Test Point	6015337	

Figure 9-9. Connector Panel Assembly (02A3) Replaceable Parts

Reference Designation	Nomenclature	Manufacturer's Part Number	Vendor Code
CR1 thru CR27	Diode	6018033	03640
K1	Relay	6078430	
K2	Relay	6078320	
K3	Relay	6078318	
K4	Relay	6078319	
K5	Relay	6078359	
K6	Relay	6078322	
K7 thru K11	Relay	6078148	
K12	Relay	6078147	
K13	Relay	6073562	
K14	Relay	6078316	
K15	Relay	6078148	
K16	Relay	6078143	
K17, K18	Relay	6078148	
K19	Relay	6078143	
K20	Relay	6078321	
K21	Relay	6078979	
K22 thru K24	Relay	6078314	
K25	Relay	6078148	
K26, K27	Relay	6078149	
K28	Relay	6078317	
K29, K30	Relay	6078147	
K31	Relay	6078149	
K32	Relay	6078317	
K33	Relay	6078316	
K34, K35	Relay	6078143	
K36	Relay	6073562	
K37, K38	Relay	6078143	
K39	Relay	6078316	
K40	Relay	6078148	
R1, R2	Resistor	6079275	
VR1, VR2	Diode	6079005	
XK1 thru XK6	Socket	6013283	
XK7 thru XK12	Socket	6078153	
XK13	Socket	6073563	
XK15, XK17, XK18	Socket	6078153	
XK20, XK21	Socket	6013283	
XK25 thru XK32	Socket	6078153	
XK36	Socket	6073563	
XK40	Socket	6078153	

Figure 9-10. Computer Power Sequence Relay Gate Assembly (02A8) Replaceable Parts

Vendor Code	Name	Address
03640	International Business Machines Corp.	Owego, N. Y.
09206	Trygon Electronics, Inc.	Roosevelt, N. Y.
16550	Rheem Electronics Corp.	Los Angeles, Calif.
88360	International Business Machines Corp.	Endicott, N. Y.

Figure 9-11. Vendor Code Cross-Reference

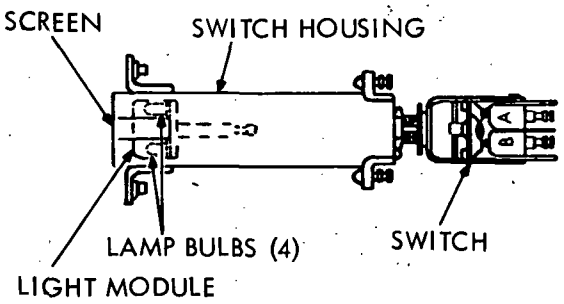


Figure 9-12. Switch Assembly

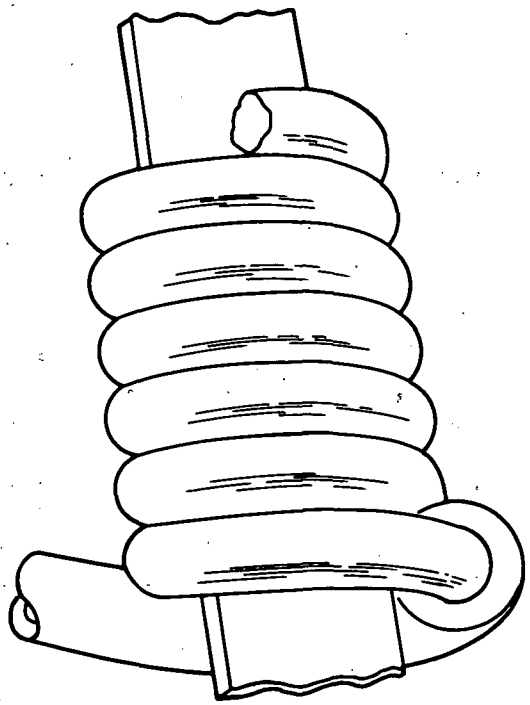


Figure 9-13. Wrapped Connection

Tool	Vendor/Part Number	Description
Hand Unwrap Tool	IBM 6072437	See figure 4-3, part O
Hand Wire Wrap Tool	IBM 6072438	See figure 4-3, part G
Wrapping Bit (No. 20)	Keller A-18633	See figure 4-3, part I
Wrapping Bit (No. 22)	Keller A-18632	See figure 4-3, part H
Wrapping Bit (No. 24)	Keller A-26232	See figure 4-3, part J
Wrapping Bit (No. 26)	Keller A-27611	See figure 4-3, part K
Sleeve (No. 20)	Keller A-18285	See figure 4-3, part N
Sleeve (No. 22, 24)	Keller A-18840	See figure 4-3, part M
Sleeve (No. 26)	Keller A-17611-2	See figure 4-3, part L

Figure 9-14. Recommended Wrapping Tools

CAUTION

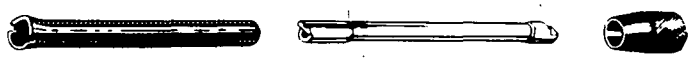
Only nylon-jacketed or semi-rigid PVC (polyvinyl chloride-insulated) wire should be used for re-wiring back panels. Teflon-insulated wire, used in panels produced by automation, is unsuitable for re-wiring in the field due to the difficulty in stripping without damaging the conductor.

9-12. WRAPPING. The following procedure indicates the necessary steps in making a wrapped connection.

a. Select the bit and sleeve for the wire size to be used.

Wire Size AWG	Wrapping Bit	Sleeve
26	Keller, A-27611	Keller, A-17611-2
24	Keller, A-26232	Keller, A-18840
22	Keller, A-18632	Keller, A-18840
20	Keller, A-18633	Keller, A-18285

b. Install bit and sleeve in the nose assembly of the wrapping tool (figure 9-15):



SLEEVE WRAPPING BIT COLLET NUT

Figure 9-15. Wrapping Tool Assembly

1. Loosen the collet nut on the nose assembly.

2. Insert the wrapping bit into the collet. Rotate the bit while applying slight pressure against the end until it seats itself. (To remove the bit, reverse this process.)

3. Place the sleeve over the bit and into the collet. Rotate until sleeve is seated and positioned. Apply slight pressure to the end of the sleeve and tighten collet nut.

c. Strip 1-3/8 to 1-1/2 inch of insulation from the end of the wire to be wrapped. This will result in about six wraps around the terminal. The completed terminal must have at least five turns of bare wire.

CAUTION

Do not nick or scrape the wire. A nicked wire is subject to breaks that are difficult to detect. Areas where plating is removed will oxidize, causing an unreliable connection.

d. Insert the stripped wire into the small hole of the wrapping bit (figure 9-16, part A) taking care to insert the wire up to the insulation. Do not bend the bare end of the wire; it may be difficult to slide into the bit. If the wire is not inserted in the wrapping bit up to the insulation, a "shiner" (bare wire between insulation and terminal) may result. There should be 1/4 turn to 3/4 turn of insulation at the beginning of each wrap, except for coaxial cable. Coaxial cable insulation should not be wrapped, but it must end no more than 1/16 inch from the terminal.

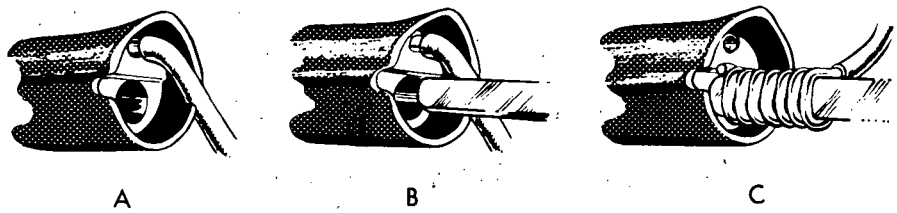


Figure 9-16. Wrapping Procedure

e. Hold the wire with the fingers and bend the insulated portion of the lead into the retaining notch in the sleeve (figure 9-16, part B). Use the right or left notch as determined by the direction of the approach (or exit) of the lead. Place the wrapping bit on the terminal. Be sure the terminal is inserted into the bit as far as it will go. Hold the tool in line with the terminal.

f. Hold the tool on the terminal and squeeze the trigger to wrap the wire on the terminal. The tool will automatically recede as the wire coils on the terminal. Release trigger and remove tool from terminal. The wrapped connection is complete (figure 9-16, part C).

NOTE

If too much pressure is used to push the tool on the terminal, a turn of wire will wrap over a previous turn. If too little pressure is exerted, the adjacent wraps of wire may not touch each other. Maximum separation between individual turns on the terminal must not exceed 0.005 inch, excluding the first and last wrap (figure 9-17).

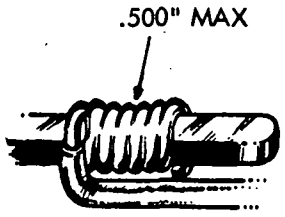


Figure 9-17. Wrap Spacing

9-13. UNWRAPPING. Wires can be removed from a terminal by using the hand unwrap tool illustrated on figure 9-18. This tool can unwrap both right and left-hand wraps.

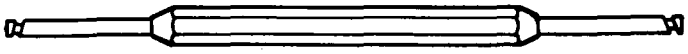


Figure 9-18. Unwrap Tool

9-14. Unwrapping is accomplished by catching the tail of the wire with the unwrap point and turning the tool in a direction opposite to that of the wrap. In some cases, it may be necessary to lift the wire tail away from the pin before the wire can be unwrapped. Apply only enough pressure to loosen turns.

CAUTION

An unwrapped wire must never be rewrapped. A new wire must be used as a replacement.

CAUTION

Never slide a termination on a pin because this rounds the sharp corner of the pin and makes subsequent connections unreliable. As you unwrap a wire, see that the first coil does not break off and drop into the panel. This breakage is often caused by the lip of the tool not engaging the tail of the wire. Terminals may be wrapped ten times before replacement is necessary.

9-15. WRAPPED CONNECTION QUALITY. Because the connection is destroyed if a wrap is disturbed in any manner, it is difficult to determine if a good quality junction has been made. The most common factors causing poor quality wraps are:

1. Incorrect wrapping bit for the wire size in use.

2. Worn or damaged wrapping bit.

3. Dirty wrapping bit.

9-16. A defective wrapped connection may be either too tight or too loose. If the wrap is made too tight, the wire is deformed to such an extent that it becomes brittle. The wire may then break under vibration and handling. A loose wrap will not have sufficient pressure to bond the wire to the terminal.

9-17. SMS back panel wires are frequently routed around, but not attached to, an intermediate terminal. If a wire is pulled too tight or excessive pressure is exerted at the point of contact with the intermediate terminal, insulation damage may result, allowing the wire to short to the terminal. This short may be intermittent. When wiring back panels, do not pull wires tightly around intermediate terminals, or allow a wire to rub along a terminal pin.

9-18. CRIMPED CONNECTIONS.

9-19. A crimped connection is a union of two electrical conductors formed by pressure. A crimped connection is usually made with a terminal that has a barrel or trough to accept a short length of wire. The wire is inserted in the terminal, which is then formed to compress and restrict the wire inside the terminal barrel as indicated on figure 9-19. If the correct pressure is applied during the forming process, a homogeneous mass will result in the crimped area.

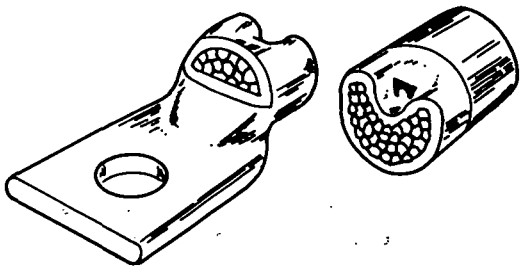


Figure 9-19. Crimped Connection, Cross Section

9-20. The critical factor in making a crimped connection is the extent to which the terminal and conductor are formed. Pressure produced in the process must be high enough to cause a bond between the terminal and conductor materials, yet low enough to prevent embrittlement of the formed parts.

9-21. RECOMMENDED CRIMPING TOOLS. Recommended crimping tools and their intended applications are listed in figure 9-20.

9-22. AMP tool 59501 is a ratchet crimping tool to be used with 22-24 AWG solid or stranded wire only. The die-set is not replaceable, and no adjustments are provided on the tool.

Crimping Tool	Application	Description
AMP 59501	Used to crimp AWG 22-24 solid or stranded wire.	See figure 4-3, part V.
Berg HT-3-20	Used to crimp AWG 20 solid or stranded wire to a slip-on terminal.	See figure 4-3, part W.
Berg HT-3-22	Used to crimp AWG 22 solid or stranded wire to a slip-on terminal.	See figure 4-3, part X.
Berg HT-3-24	Used to crimp AWG 24 solid or stranded wire to a slip-on terminal.	See figure 4-3, part Y.
Bendix 11-7295 (Kit)	Used to crimp size 12, 16, and 20 type connector contacts.	See figure 4-3, part P.

Figure 9-20. Recommended Crimping Tools

9-23. Terminals used with the AMP ratchet tool have a two-section crimping barrel as illustrated in figure 9-21. The tool crimps one section on the conductor and the other section on the insulation. Make certain to insert terminals into the die so that the larger die opening crimps the insulation.

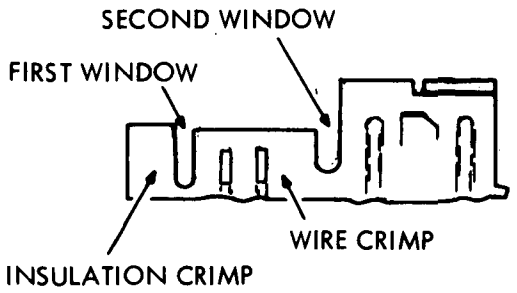


Figure 9-21. Slip-on Connector Terminal

9-24. CRIMPED CONNECTION QUALITY. The quality of a crimped connection depends largely on the correct combination of wire, terminal, and tool for each application. The following procedure is recommended for determining the quality of crimped connections:

a. Visually inspect all completed connections for the following:

CAUTION

Do not use a connection that does not meet these criteria.

1. Stripped portion of the wire centrally located under the crimp.

2. No deformation of the terminal outside of the crimp area.

3. No fractures of the terminal or wire.

b. Test completed connections having no visual defects as follows:

1. Grip the wire between the thumb and forefinger of one hand and the terminal between the thumb and forefinger of the other hand.

2. Pull the wire, exerting only enough pressure to make the wire taut. Check for any movement of the wire within the terminal barrel.

NOTE

Wire movement in the terminal barrel can often be heard, but not seen. Such a connection is called a clicker and must not be used.

3. Bend the wire about 30° from center and repeat step 2. Bend the wire in the opposite direction about 30° from center and repeat step 2.

9-25. SOLDERED CONNECTIONS.

9-26. The soldering process involves six steps: selection of materials, preparing the soldering iron and tip, preparing the work, heating the work, applying the flux and solder, and cooling.

9-27. SELECTION OF MATERIALS. Recommended soldering tools are listed in figure 9-22.

CAUTION

Do not use acid-core solder.

Tool	Vendor/Part No.	Description
Soldering Handle	Hexacon P25	See figure 4-3, part E.
Soldering Tip	Hexacon HT248D	See figure 4-3, part F.

Figure 9-22. Recommended Soldering Tools

9-28. Rosin cored wire solder (conforming to Federal Specification QQ-S-571) is similar to a piece of spaghetti; the hollow center is filled with flux that flows over the work when heated to a moderate temperature (about 300°F). This temperature is below the melting point of the solder (about 360°F). The flux becomes active upon further heating, but prolonged exposure to heat causes it to decompose.

9-29. PREPARING THE SOLDERING IRON AND TIP. The soldering iron is used only to transmit heat to the work. Before using the iron, heat it to operating temperature and tin it: wipe the tip with a clean cloth or canvas; then apply flux and solder, giving the tip a clean, shiny coat of solder. Tinning is done to insure good heat transfer and to keep the connection area free of contamination. Subsequent accumulation of flux residue and solder dross can be removed in the same manner.

9-30. PREPARING THE WORK. The work must be clean. No grease, wax, paint, dust or other foreign material should be present on the surfaces to be soldered. These surfaces should be pretinned. Pretinning is the application of a thin layer of solder over the surfaces of the metals to be joined, using the same process as for tinning the soldering iron tip.

9-31. Use extreme care when stripping insulation from wire. The stripping tools should be adjusted so that no metal is removed from the wire during the stripping operation. Cutting the strands in stranded wire reduces the cross-sectional area, which decreases current carrying capacity and presents a mechanically weak spot; a nick in solid wire has much the same effect.

9-32. Unless otherwise specified, insulation should be stripped so that not more than 1/8 inch nor less than 1/16 inch of wire will be exposed between the soldered terminal and the insulation (figure 9-23). Leads of an axial lead component should not be formed closer than 1/16 inch from the component body (figure 9-24).

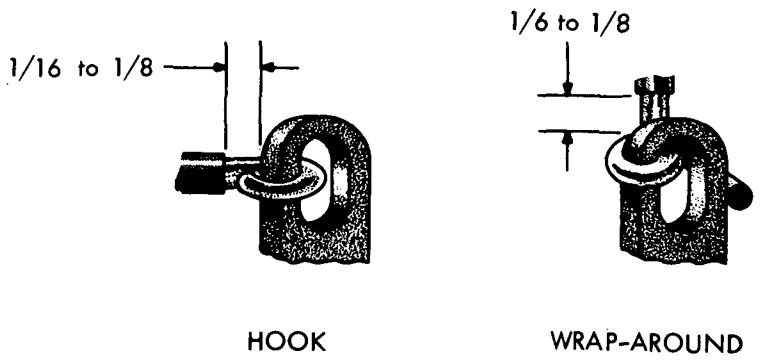


Figure 9-23. Terminal Connections

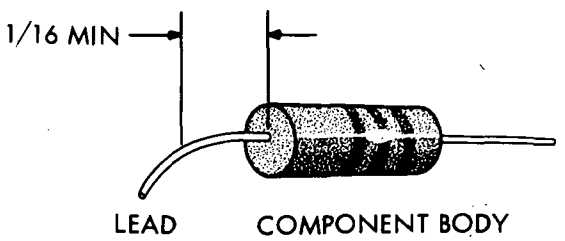


Figure 9-24. Axial Lead Connections

9-33. HEATING THE WORK. The joint must be thoroughly heated before applying solder. Efficient heat transfer from the iron to the work depends on the cleanliness of the surfaces and the size of the contact area. A small amount of clean solder on the iron tip will insure effective heat transfer.

9-34. Poor solder connections are often the result of insufficient heat. Protect components, but remember that a destroyed component is less expensive than a cold soldered joint that causes intermittent failures.

9-35. APPLYING THE FLUX AND SOLDER. The solder should be applied to the work, not to the iron. If the surfaces are clean and are at the correct temperature, flux and solder will flow freely over the surfaces and wet the metal. This wetting action is the basic solder bond. After the solder solidifies, it will remain adhered to the surface and will provide electrical continuity.

9-36. The proper amount of solder is important. The solder bond occurs on the metal surfaces and excessive solder does not improve the joint but can introduce undesirable side effects. Use enough solder to cover the parts to be joined, but leave the outlines visible.

9-37. COOLING. Once the solder has been applied, withdraw the soldering iron and allow the joint to cool. Solidification of solder is not instantaneous, and any movement during this time may cause a solder bond of unacceptable quality. Keep the parts perfectly still until the solder is frozen.

9-38. VISUAL INSPECTION. A good soldered connection is bright and smooth. The solder feathers out to a thin edge from the main body of solder in the joint. It also approximately outlines the wire and terminal. Figure 9-25 illustrates good soldered connections.

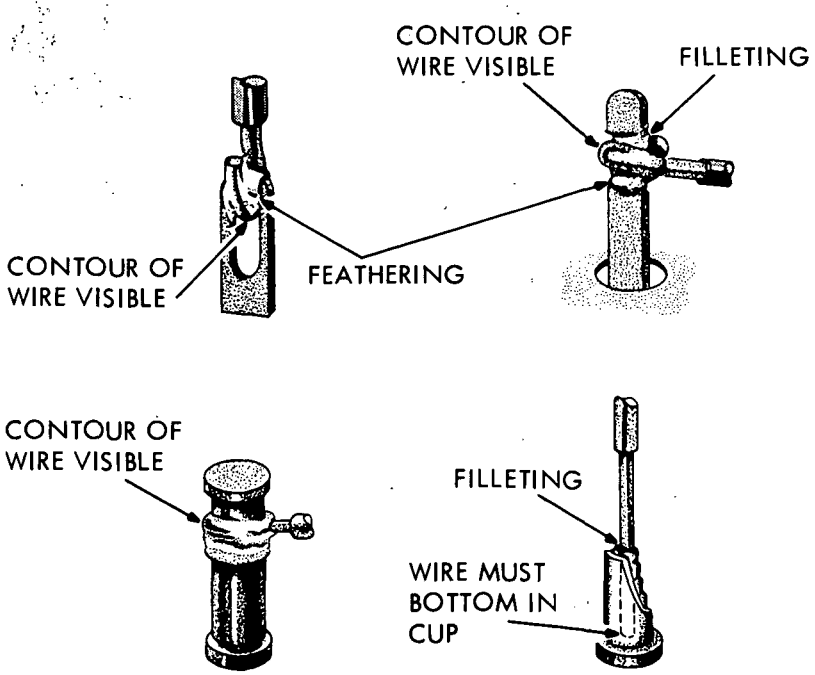


Figure 9-25. Good Soldered Connections

9-39. Figure 9-26 illustrates defective soldered connections.

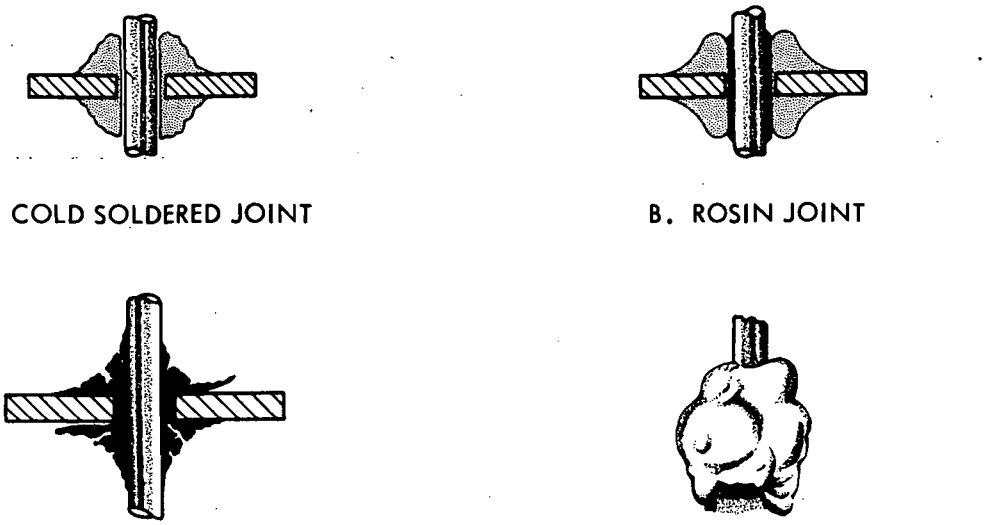


Figure 9-26. Defective Soldered Connections

9-40. The Cold Soldered Joint (figure 9-26, part A) has a dull, granular appearance. It is caused by insufficient heating, or movement of the work during cooling.

9-41. The Rosin Joint (figure 9-26, part B) has a rosin inclusion. Rosin joints can be due to insufficient heat to permit the rosin to be displaced by the solder, or insufficient heat to permit adequate melting of the flux.

9-42. The Excessively Soldered Joint (figure 9-26, part C) hides the outline of the joint components with an excessive amount of solder.

9-43. The Fractured Soldered Joint (figure 9-26, part D) is one in which small cracks are present. This condition can be due to stress applied before the solder is completely solidified.

9-44. SMS CARD REPLACEMENT.

9-45. The SMS card puller (IBM 6072429) facilitates insertion or removal of SMS cards from their sockets. Use of this tool reduces the probability of dropping cards and other handling damage. This tool is illustrated on figure 4-3, part A.

9-46. In operation, the card puller fits over the edges of an SMS card. When the tool is properly positioned, a tooth on the spring-loaded latch seats in a hole in the card. The card is released by depressing the latch.

CAUTION

Before removing an SMS card, insert IBM punched cards or similar material between the card to be removed and adjacent SMS cards. Damage to SMS cards or components may be eliminated in this manner.

CAUTION

Oil or moisture from the fingers can critically decrease the insulation resistance on the land pattern side of the card. Cards should be carefully handled by the edges only.

9-47. When an SMS card is removed from its socket, the card contacts should be cleaned and lubricated before the card is reinstalled if either of the following conditions exists:

1. The card contacts are visibly contaminated.

2. The card contacts have been handled. If there is any doubt about the contamination of the contacts, clean and relubricate them.

9-48. The following cleaning and lubricating procedure insures low contact resistance and reduces wear of the gold-plated contact surfaces. The procedure may be performed any number of times without affecting contact reliability. To clean and lubricate the contacts:

a. Apply lubricant (IBM part number 6072430) either directly to the contacts or indirectly with a saturated, clean, lint-free cloth or tissue.

b. Wipe the contacts toward the component section of the card with a cloth or tissue moistened with the lubricant.

CAUTION

Do not allow the lubricant to contact the clear plastic coating on the component portion of the card. The solvents in the lubricant can dissolve the plastic coating, which will act as an insulator if rubbed on the contacts.

c. Rub the contacts with a clean, dry piece of cloth of tissue until there is no visible trace of the lubricant. The cloth or tissue will darken if further cleaning is necessary. Repeat the procedure from step a if further cleaning is needed.

9-49. SMS CARD REPAIR.

9-50. Repair of printed circuit cards primarily consists of soldering and unsoldering operations. The specific jobs involved are:

1. Removal of defective components.

2. Installation of replacement components.

3. Joining broken printed conductors.

9-51. Care must be taken to avoid damage to the card assembly during the repair process. The card assembly is easily damaged in two ways:

1. Heat damage to the card or to components on the card.

2. Physical damage.

9-52. The card is made of an insulating material that will withstand a dipsolder temperature of about 515 °F for 30 seconds. This compares with a minimum solder melting temperature of 361 °F and an average soldering iron temperature of 750 °F. This means that the soldering iron must contact the card for only a short interval of time. Excessive heat may damage a card in two ways by:

1. Destroying the bond between the insulated board and a printed conductor, resulting in a raised conductor;

2. Scorching or burning the board.

9-53. Excessive heat may also damage components on the card. Semiconductors are especially sensitive to heat. Use of the soldering tools recommended under SOLDERED CONNECTIONS will help avoid heat damage.

9-54. Physical damage in the form of a raised conductor is easily inflicted if stress is applied in a direction that tends to separate the conductor from the board (figure 9-27).

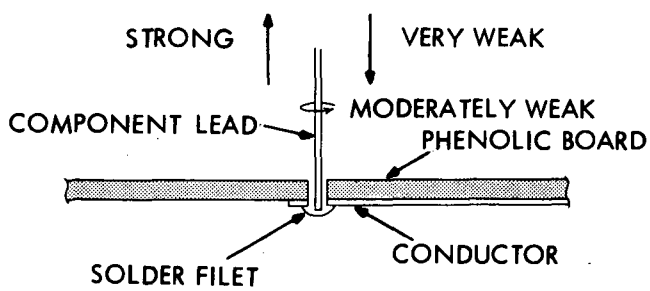


Figure 9-27. Stress Applied to Component Leads

9-55. COMPONENT REMOVAL. When the leads of the defective component must be saved, use the following procedure to remove the component:

a. Straighten the component leads that are bent over on the wiring side of the board. Figure 9-28 illustrates a method of using the soldering iron tip as a wedge to prevent

pulling the land away from the board. A pair of long-nose pliers may be used on the component side of the card to prevent downward movement of the lead.

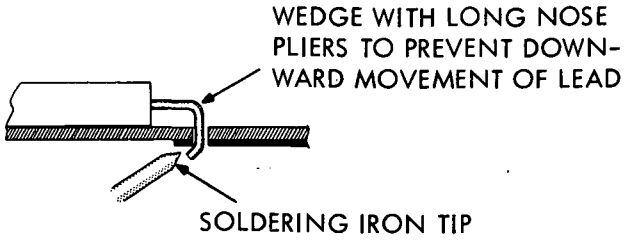


Figure 9-28. Component Removal

b. Heat the component leads and pull them through the holes from the component side of the board.

9-56. If the leads of the defective component may be destroyed, use the following removal procedure:

a. Cut the leads of the defective component as close as possible to the board on the component side of the card. Do not damage the board or adjacent components.

b. Hold the card in your hand and use a clean, tinned soldering iron to heat the solder connection between the remaining portion of the leads and the conductor pattern.

c. When the solder starts to flow, rap the hand holding the card on the work surface.

d. Repeat steps b and c if the solder and piece of lead do not leave the hole.

9-57. COMPONENT INSTALLATION. Use the following procedure for installing components on SMS cards.

a. Insert component leads through the holes in the board. Cut the leads so that about 1/16 inch remains to bend over on the conductor pattern. Bend the leads parallel to the component body and toward each other. Axial lead components, such as resistors, are mounted flush against the surface of the board.

CAUTION

Do not bend leads close to components (see SOLDERED CONNECTIONS for technique). The leads on tantalum capacitors are particularly subject to damage.

b. Solder the component leads to the conductor pattern. Avoid excessive heat and solder, particularly with transistors and diodes. It is not desirable to fill the hole in the board with solder.

c. Wash the general area of repair using a typewriter cleaning brush and IBM cleaning fluid (IBM part number 450608). Dry the affected area by wiping with a clean piece of cloth or tissue.

9-58. PRINTED CONDUCTOR REPAIR. Two printed conductor defects may be found: broken conductor, or delaminated conductor (raised land).

9-59. To repair a broken conductor, solder a 24 AWG solid wire jumper across the break. The wire should overlap the printed conductor at least 1/16 inch on each end. If the break is long, and the possibility of a short exists, use insulated wire stripped on each end.

9-60. To repair a delaminated conductor, cut both ends of the loose section at a point where the bond is not broken. After the loose section is removed, repair the conductor using the same method used for a broken conductor.

9-61. EXTERIOR SURFACE COATINGS.

9-62. Figure 9-29 lists the solvents, reducers, primers and paints needed to refurbish LVDCME coatings that become chipped, discolored, or otherwise defective.

NOTE

The dark gray, white, and black paints listed in figure 9-29 for the functional areas and panel markings are actually vinyl inks, originally applied by silk screen processes.

9-63. REPAINTING TECHNIQUES

9-64. The following paragraphs indicate the recommended consistencies for the paints and other fluids needed to repair the exterior coatings of the LVDCME. A fine brush should be used to retouch defective panel markings and any small scratches on the LVDCME. For repainting areas greater than 1 in. square, the paint should be applied by spraying.

9-65. SOLVENTS. The surface to be repainted should be thoroughly cleaned by wiping it with the solvent indicated in figure 9-29. The surface should then be allowed to dry for at least 30 minutes.

9-66. PRIMERS. If the coating has been marred so that the metal surface is exposed, a primer coating should be applied before the paint is applied. The primer need not be diluted for brush application; however, for spray application the primer should be diluted with one part reducer to two parts primer. The primer coating should be air dried for at least three minutes before paint is applied.

9-67. PAINTS. The paints need not be diluted for brush application; however, for spray application the paint should be diluted with one part reducer to four parts paint. Four or more sprayed coats should be applied, allowing a minimum time of one minute between the application of each coat. For a non-textured finish, these applications are the finish coat; however, for a textured finish these applications are only the first finish coat.

Surface	Solvent	Reducer*	Primer*	Paint (Vinyl)*	Notes*
Frame Covers	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903.	Charcoal-John L. Armitage Co., P-318.	Charcoal-John L. Armitage Co., U-211.	Use texturing agent, John L. Armitage Co., M-411.
Control Panels Background		John L. Armitage Co., A-903 or M-130.	Blue-Gray, John L. Armitage Co., P-350.	Light Gray-John L. Armitage Co., U-662S.	
Functional Areas				Dark Gray-John L. Armitage Co., M-1085.	
Panel Markings				White-John L. Armitage Co., M-1027.	Used on Dark Gray functional areas.
				Black-John L. Armitage Co., M-1035.	Used on Light Gray areas.
Name Plate	Xylene conforming to Federal Specification TT-X-916.	John L. Armitage Co., A-903, or M-130.	Yellow-John L. Armitage Co., P-321.	Yellow-John L. Armitage Co., U-333S.	
			Blue-John L. Armitage Co., P-300.	Sky Blue-John L. Armitage Co., U-396S.	
				White-John L. Armitage Co., M-1027.	Used as a filler for engraving.
*Equivalent materials may be used.					

Figure 9-29. Recommended Repainting Materials

NOTE

The number of paint coats required to adequately repair the defective surface depends on the depth of the defect and the thickness of the original coatings.

9-68. If the final surface is to be textured, a second finish coat of paint should be applied after the first finish coat has been air dried. The paint for this second finish coat need not be diluted for brush application; however, for spray application the paint should be diluted with one part reducer to eight parts paint. Five or more sprayed coats should be applied, allowing a minimum time of one minute between the application of each coat. (See note in preceding paragraph.)

9-69. TEXTURING AGENT. The texturing agent should not be diluted before being sprayed as a fine mist coat over the second finish coat.

SECTION X

DIAGRAMS

10-1. GENERAL.

10-2. The diagrams included in this section are Engineering drawings that are required to maintain the LVDCME. The Engineering drawings consist of the following:

Figure 10-4. LVDCME AC Power Distribution Electrical Schematic Diagram (LN 00.03.01.0)

Figure 10-5. Power Sequence, LVDCME and Computer, Electrical Schematic Diagram (LN 00.03.02.0)

Figure 10-6. LVDCME DC Power Distribution Electrical Schematic Diagram (LN 00.03.03.0 and LN 00.03.04.0)

Figure 10-7. LVDCME Computer Power Distribution Electrical Schematic Diagram (LN 00.03.05.0 and LN 00.03.06.0)

Figure 10-8. LVDCME Module Switching Power Distribution Electrical Schematic Diagram (LN 00.03.07.0)

Figure 10-9. LVDCME Self Test and Lamp Test Electrical Schematic Diagram (LN 00.03.08.0)

Figure 10-10. LVDCME DC Power Distribution and Grounding Electrical Schematic Diagram (LN 00.03.09.0)

Figure 10-11. Cable Drawing (AP, AZ and AN Cables) LVDCME to Computer and Test Stand (LN 00.03.10.0 and LN 00.03.11.0)

Figure 10-12. Tape Control Panel (01A2) Data Flow Diagram (LN 00.04.01.0, LN 00.04.02.0 and LN 00.04.03.0)

Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0)

Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0)

Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0)

Figure 10-16. Tape Reader and Tape Spooler Cabling Data Flow Diagram (LN 00.04.28.0)

Figure 10-17. Power Cable (AU Cable) Data Flow Diagram (LN 00.04.29.0)

Figure 10-44. TC2, $\overline{B0}$ Detect Printed Circuit Board Assembly (6901338)

Figure 10-45. NA1 Translator Printed Circuit Board Assembly (6901340)

Figure 10-46. NA2 Translator Printed Circuit Board Assembly (6901342)

Figure 10-47. SC1 Simulator Printed Circuit Board Assembly (6901344)

Figure 10-48. SC2 Simulator Printed Circuit Board Assembly (6901346)

Figure 10-49. Modified AN1 Printed Circuit Board Assembly (6901348)

Figure 10-50. 3.6 K Resistor Printed Circuit Board Assembly (6901349)

Figure 10-51. Temperature Monitoring Printed Circuit Board Assembly (6901350)

Figure 10-52. SCR Resistor Printed Circuit Board Assembly (6901354)

Figure 10-53. AN4 Translator Printed Circuit Board Assembly (6901355)

Figure 10-54. CD1 Printed Circuit Board Assembly (6901356)

Figure 10-55. SC3 Printed Circuit Board Assembly (6901358)

10-3. Automated Logic Diagrams (ALD's) are not included in the Manual but are supplied separately. Paragraphs 10-13 through 10-19 describe the physical make-up of the ALD's. Figure 10-1 lists the sheets of ALD's by Logic Page Number and IBM Page Part Number that are required to maintain the LVDCME.

10-4. Reference is made between pages of the Electrical Schematic Diagrams, Data Flow Diagrams and the ALD's. This reference is made by an "LN" seven-digit number (xx.xx.xx.x) assigned to each page (or sheet). The "LN" seven-digit number is related to the diagrams as follows:

Electrical Schematic Diagrams - LN 00.03.xx.x

Data Flow Diagrams - LN 00.04.xx.x and LN 04.00.xx.x

ALD's - LN 05.xx.xx.x

10-5. The "xx.x" in the "LN" numbers for the Electrical Schematic Diagrams and the Data Flow Diagrams specify the sequence of page or sheet numbers. The "05" in the ALD "LN" number specifies that the reference is to an ALD page. The entire LN number for the ALD's is described in paragraph 10-15.

10-6. CIRCUIT CARD LOCATION CHARTS AND EDGE CONNECTOR LISTS.

10-7. Included with the ALD's are Circuit Card Location Charts and Edge Connector Lists. The Circuit Card Location Charts (listed in figure 10-38) designate the SMS card by type and IBM part number for each card location on the gate assemblies. Also, the ALD sheet(s) on which the card appears and whether or not all of the circuits on the card are being used is referenced on the Circuit Card Location Charts. The Edge Connector Lists (listed in figure 10-39) list the edge connectors for each gate assembly, the signal present on each edge connector pin, and the ALD sheet on which the edge connector pin and signal appear.

10-8. SECOND LEVEL LOGIC DIAGRAMS.

10-9. The second level logic diagrams are provided to aid in the analysis of the LVDCME. These diagrams are arranged in a logical order by test set functions. Included with the second level logic diagrams is a chart of symbol definitions (figure 10-30, sheets 1 and 2) that defines all the symbols used in the diagrams. Also included is a block diagram (sheet 3) showing the relationship of the LVDCME functions.

10-10. The second level logic diagrams contain a table, in the lower left-hand corner of each sheet, listing the ALD sheets (by LN number) that are represented on the sheet of second level logic. In the upper left-hand corner of each sheet of the second level logic diagrams is a table listing the origins (by sheet number) of the input signals and the destinations (by sheet number) of the output signals. All input and output signals are listed in the tables except timing signals and the signals whose origin or destination appears on the data flow diagrams.

10-11. ASSEMBLY DRAWINGS.

10-12. The assembly drawings are provided to aid in the location of replaceable parts. Only the assembly drawings that are required for part replacement are included.

10-13. AUTOMATED LOGIC DIAGRAM FORMAT.

10-14. PAGE LAYOUT. The automated logic diagrams contain page identification, edge information, logic blocks, connecting lines, and an area for comments at the bottom of each page. Figure 10-2 shows a typical logic page. Each page has a possible logic format of five blocks wide and nine blocks long; thus logic blocks can occupy any of 45 possible positions.

10-15. PAGE IDENTIFICATION. As shown on figure 10-2, the following information appears at the top of each logic diagram page:

a. Page part number (1), used for ordering a specific page or series of pages.

b. Title (2), a description of the logic contained on the page.

c. Equipment name (3), the abbreviation of the equipment name and the configuration of the equipment.

d. Logic page number (4), a seven-digit number (xx.xx.xx.x) assigned to the logic page. For explanation purposes, letters are used to designate each position in the number (AB, CD, EF, G).

(1) Positions A and B specify that the sheets are ALD's.

(2) Positions C, D, E, F, and G represent the page number sequence.

e. Comments (5), a list of edge-connector locations used for the entry and exit lines on the logic page, and an area reserved for comments.

10-16. SIGNAL LINES. All lines entering or leaving a logic page are labeled and correspond to the labeling on the logic page to which they interconnect. Lines enter on the left side of the page and leave on the right side of the page. If a line leaves a page and goes to several locations on another page, the line is usually distributed on the "to" page

and not the "from" page. If a line leaves a page and goes to several other pages, but carries the same line name, it is shown as a branched line on the "from" page.

10-17. EDGE INFORMATION. Data shown in vertical page coordinates 1 and 7 are called edge information. Edge information includes names of input and output lines, and numbers of the logic pages the lines appear on again. The first line contains the signal name. The second line lists the number of the logic page on which the signal appears again. The logic page number is directly opposite the signal line.

10-18. EDGE CONNECTORS. When a signal or service wire enters or leaves a panel, it may be routed through an edge connector. Signal lines connected to edge connectors are indicated by an asterisk or lozenger and a number or letter combination (e.g., *2, *C, □1, □F, 1□, etc.) located on an entry or exit line. These notations refer to edge connector locations and pin letters given at the bottom of the logic page.

10-19. LOGIC BLOCKS. To simplify the logic pages, logic blocks are used to represent the SMS card circuits. A basic electronic function is usually represented by a single block, but some functions may require more than one block. In the case of multiple circuits on one SMS card, each circuit is represented by a separate logic block. The standard format of the logic block is shown on figure 10-3, and is explained as follows:

a. Timing. The timings of special circuits, such as single shots, oscillators, and delays, are printed above the logic blocks.

b. Functional Symbol. This symbol consists of a sign (when used) and letter(s) that indicate the type of circuit.

c. Machine Feature Index. This code indicates the configuration of the equipment. BA indicates the basic configuration.

Logic Page Number	Page Part Number
05.00.01.1	6901050
05.00.02.1	6901051
05.00.03.1	6901052
05.00.04.1	6901053
05.00.05.1	6901054
05.00.05.2	6902194
05.00.06.1	6901055
05.00.07.1	6901056
05.00.08.1	6901057
05.00.09.1	6901058
05.00.10.1	6901059
05.00.10.2	6902170
05.00.11.1	6901060
05.00.11.2	6901061
05.00.12.1	6901062
05.00.13.1	6901063
05.00.14.1	6901064
05.00.15.1	6901065
05.00.16.1	6901066
05.00.17.1	6901067
05.00.18.1	6901068
05.00.19.1	6901069
05.00.20.1	6901070
05.00.21.1	6901071
05.00.22.1	6901072
05.00.23.1	6901073
05.00.24.1	6901074
05.00.25.1	6901075
05.00.25.2	6902285

Logic Page Number	Page Part Number
05.00.25.3	6901440
05.00.25.4	6902286
05.00.26.1	6901076
05.00.27.1	6901077
05.00.28.1	6901078
05.00.29.1	6901079
05.00.30.1	6901080
05.00.31.1	6901081
05.00.32.1	6901082
05.00.33.1	6901083
05.00.34.1	6901084
05.00.35.1	6901085
05.00.36.1	6901086
05.00.37.1	6901087
05.00.38.1	6901088
05.00.38.2	6901089
05.00.39.1	6901090
05.00.40.1	6901091
05.00.41.1	6901092
05.00.42.1	6901093
05.00.43.1	6901094
05.00.44.1	6901096
05.00.45.1	6901097
05.00.46.1	6901098
05.00.47.1	6901099
05.00.48.1	6901150
05.00.49.1	6901151
05.00.50.1	6901152
05.00.51.1	6901153

Logic Page Number	Page Part Number
05.00.52.1	6901154
05.00.53.1	6901155
05.00.54.1	6901156
05.00.54.2	6902178
05.00.55.1	6901157
05.00.56.1	6901158
05.00.57.1	6901159
05.00.58.1	6901160
05.00.59.1	6901161
05.00.60.1	6901162
05.00.61.1	6901163
05.00.62.1	6901164
05.00.63.1	6901165
05.00.64.1	6901166
05.00.65.1	6901167
05.00.66.1	6901168
05.00.67.1	6901169
05.00.68.1	6901170
05.00.69.1	6901171
05.00.70.1	6901172
05.00.71.1	6901173
05.00.72.1	6901174
05.00.73.1	6901175
05.00.74.1	6901176
05.00.75.1	6901177
05.00.75.2	6901178
05.00.76.1	6901179
05.00.76.2	6901180
05.00.76.4	6901182

Figure 10-1. LVDCME Automated Logic Diagrams (Sheet 1 of 4)

Logic Page Number	Page Part Number
05.00.76.5	6901183
05.00.76.6	6902389
05.00.76.7	6902386
05.00.76.8	6902387
05.00.76.9	6902388
05.00.77.1	6901184
05.00.78.1	6901185
05.00.79.1	6901186
05.00.80.1	6901187
05.00.81.1	6901188
05.00.81.2	6901189
05.00.82.1	6901191
05.00.83.1	6901192
05.00.84.1	6901193
05.00.85.1	6901194
05.00.86.1	6901197
05.00.87.1	6901198
05.00.88.1	6901199
05.00.89.1	6901250
05.00.90.1	6901251
05.00.91.1	6901252
05.00.92.1	6901253
05.00.93.1	6901254
05.00.94.1	6901255
05.00.94.2	6901256
05.00.95.1	6901257
05.00.96.1	6901258
05.00.97.1	6901259
05.00.98.1	6901260

Logic Page Number	Page Part Number
05.00.99.1	6901261
05.01.00.1	6901262
05.01.01.1	6901263
05.01.02.1	6901264
05.01.02.2	6902379
05.01.03.1	6901265
05.01.04.1	6901266
05.01.05.1	6901267
05.01.06.1	6901268
05.01.06.2	6901269
05.01.07.1	6901270
05.01.09.1	6901271
05.01.11.1	6901272
05.01.13.1	6901273
05.01.14.1	6901274
05.01.14.3	6901276
05.01.14.2	6901275
05.01.15.1	6901277
05.01.16.1	6901278
05.01.17.1	6901279
05.01.19.1	6901280
05.01.20.1	6901281
05.01.21.1	6901282
05.01.22.1	6901283
05.01.23.1	6901284
05.01.24.1	6901285
05.01.25.1	6901286
05.01.25.2	6902174
05.01.25.3	6902175

Logic Page Number	Page Part Number
05.01.26.1	6901287
05.01.26.2	6902171
05.01.26.3	6902176
05.01.26.4	6902177
05.01.26.5	6902382
05.01.27.1	6901288
05.01.28.1	6901289
05.01.28.2	6901291
05.01.29.1	6901292
05.01.30.1	6901293
05.01.30.2	6901294
05.01.30.3	6902173
05.01.30.4	6902384
05.01.30.5	6902385
05.01.31.1	6901297
05.01.32.1	6901298
05.01.34.1	6901450
05.01.35.1	6901451
05.01.36.1	6901452
05.01.37.1	6901453
05.01.38.1	6901452
05.01.39.1	6901455
05.01.40.1	6901456
05.01.43.2	6901477
05.01.43.3	6901478
05.01.43.4	6901479
05.01.43.5	6901480
05.01.44.1	6901481
05.01.45.1	6901482

Figure 10-1. LVDCME Automated Logic Diagrams (Sheet 2)

Logic Page Number	Page Part Number
05.01.46.1	6901483
05.01.47.1	6901484
05.01.47.2	6901485
05.01.48.1	6901486
05.01.49.1	6901487
05.01.50.1	6901488
05.01.51.1	6901489
05.01.52.1	6901490
05.01.53.1	6901491
05.01.53.2	6902380
05.01.54.1	6901492
05.01.55.1	6901493
05.01.55.2	6902381
05.01.56.1	6901494
05.01.57.1	6901497
05.01.58.1	6901498
05.01.59.1	6901499
05.01.60.1	6901550
05.01.61.1	6901551
05.01.61.2	6901552
05.01.62.1	6901553
05.01.63.1	6901554
05.01.64.1	6901555
05.01.64.2	6902172
05.01.64.3	6902394
05.01.64.4	6902398
05.01.64.5	6902450
05.01.64.6	6902399
05.01.65.1	6901556

Logic Page Number	Page Part Number
05.01.65.2	6901557
05.01.65.3	6901558
05.01.66.1	6901559
05.01.67.1	6901650
05.01.68.1	6901651
05.01.69.1	6901652
05.01.70.1	6901653
05.01.71.1	6901654
05.01.72.1	6901655
05.01.73.1	6901656
05.01.73.2	6901657
05.01.73.3	6901658
05.01.73.4	6901659
05.01.73.5	6901682
05.01.74.1	6901659
05.01.75.1	6901684
05.01.76.1	6901685
05.01.77.1	6901686
05.01.77.2	6902383
05.01.78.1	6901687
05.01.79.1	6901688
05.01.80.1	6901689
05.01.81.1	6901690
05.01.81.2	6902168
05.01.82.1	6901691
05.01.83.1	6901692
05.01.84.1	6901693
05.01.84.2	6902378
05.01.85.1	6901694

Logic Page Number	Page Part Number
05.01.86.1	6901699
05.01.86.2	6902377
05.01.87.1	6902050
05.01.88.1	6902051
05.01.89.1	6902052
05.01.90.1	6902053
05.01.91.1	6902054
05.01.92.1	6902055
05.01.93.1	6902056
05.01.94.1	6902057
05.01.94.2	6902058
05.01.95.1	6902059
05.01.96.1	6902060
05.01.97.1	6902061
05.01.98.1	6902062
05.01.99.1	6902063
05.02.00.1	6902064
05.02.00.2	6902390
05.02.00.3	6902391
05.02.00.4	6902392
05.02.01.1	6902065
05.02.02.1	6902066
05.02.03.1	6902067
05.02.04.1	6902068
05.02.05.1	6902069
05.02.06.1	6902070
05.02.07.1	6902071
05.02.08.1	6902072
05.02.09.1	6902073

Figure 10-1. LVDCME Automated Logic Diagrams (Sheet 3)

Logic Page Number	Page Part Number
05.02.10.1	6902074
05.02.11.1	6902075
05.02.11.2	6902393
05.02.12.1	6902076
05.02.13.1	6902077
05.02.14.1	6902078
05.02.15.1	6902079
05.02.16.1	6902080
05.02.17.1	6902081
05.02.18.1	6902082
05.02.19.1	6902083
05.02.20.1	6902084
05.02.21.1	6902086
05.02.22.1	6902087
05.02.23.1	6902088
05.02.24.1	6902089
05.02.25.1	6902090
05.02.26.1	6902091
05.02.27.1	6902092
05.02.28.1	6902093
05.02.29.1	6902094
05.02.30.1	6902095
05.02.31.1	6902096
05.02.32.1	6902097
05.02.33.1	6902098
05.02.34.1	6902099
05.02.35.1	6902152
05.02.35.2	6902359
05.02.36.1	6902153

Logic Page Number	Page Part Number
05.02.37.1	6902154
05.02.38.1	6902155
05.02.39.1	6902156
05.02.40.1	6902157
05.02.41.1	6902158
05.02.42.1	6902159
05.02.43.1	6902160
05.02.44.1	6902161
05.03.01.1	6902162
05.03.02.1	6902163
05.03.03.1	6902164
05.03.04.1	6902165
05.03.05.1	6902166
05.03.06.1	6902167
05.03.07.1	6902287
05.03.08.1	6902288
05.03.09.1	6902289
05.03.10.1	6902290
05.03.11.1	6902291
05.03.12.1	6902292
05.03.13.1	6902293
05.03.14.1	6902294
05.03.15.1	6902298
05.03.16.1	6902299
05.03.17.1	6902350
05.03.18.1	6902351
05.03.19.1	6902352
05.03.20.1	6902353
05.03.21.1	6902354

Logic Page Number	Page Part Number
05.03.21.2	6902355
05.03.21.3	6902356
05.03.22.1	6902357
05.03.23.1	6902358
05.04.01.1	6902262
05.04.02.1	6902296
05.04.03.1	6902297
05.04.04.1	6902180
05.04.05.1	6902181
05.04.06.1	6902182
05.04.07.1	6902183
05.04.08.1	6902259
05.04.09.1	6902260
05.04.10.1	6902261
05.04.11.1	6902184
05.04.12.1	6902185
05.04.13.1	6902186
05.04.14.1	6902187
05.04.15.1	6902188
05.04.16.1	6902189
05.04.17.1	6902250
05.04.18.1	6902251
05.04.19.1	6902252
05.04.20.1	6902253
05.04.21.1	6902254
05.04.22.1	6902255
05.04.23.1	6902256

Figure 10-1. LVDCME Automated Logic Diagrams (Sheet 4)

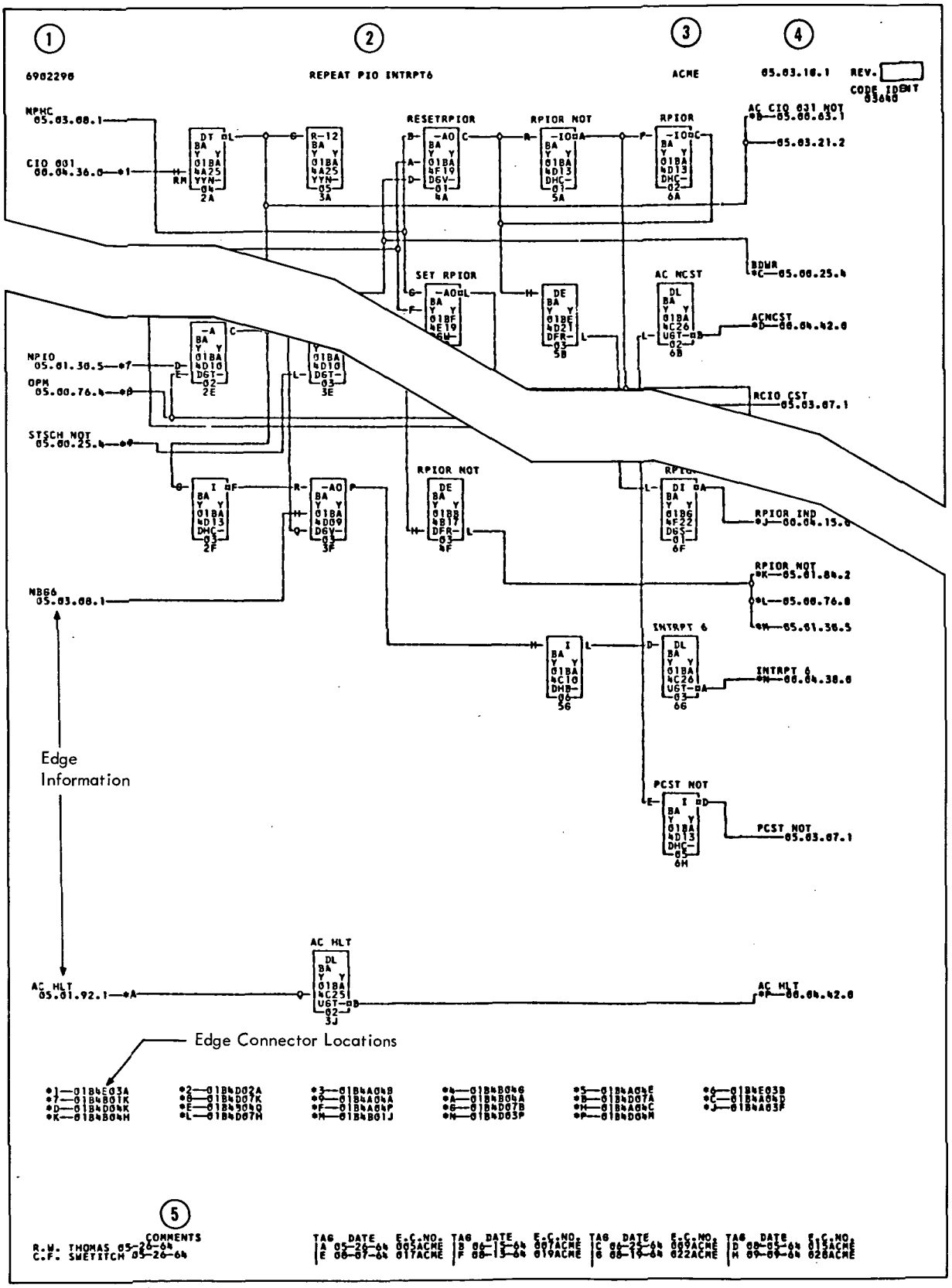
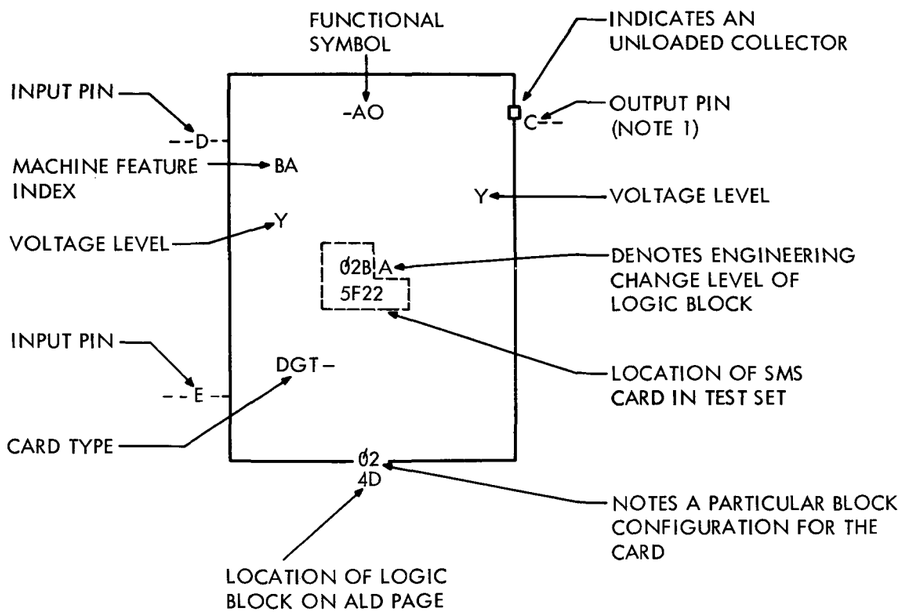


Figure 10-2. Typical Logic Page



NOTES:

1. IF THE OUTPUT PIN IS SHOWN IN THE TOP HALF OF THE LOGIC BLOCK, THE OUTPUT IS OUT OF PHASE WITH THE INPUT(S). IF THE OUTPUT PIN IS SHOWN IN THE BOTTOM HALF OF THE LOGIC BLOCK, THE OUTPUT IS IN PHASE WITH THE INPUT(S).

2. WHEN A LOGIC BLOCK HAS NO INPUTS THE LETTERS LISTED TO THE LEFT OF THE BLOCK INDICATE THAT THESE PINS ARE JUMPERED TOGETHER.

Figure 10-3. Typical Logic Block

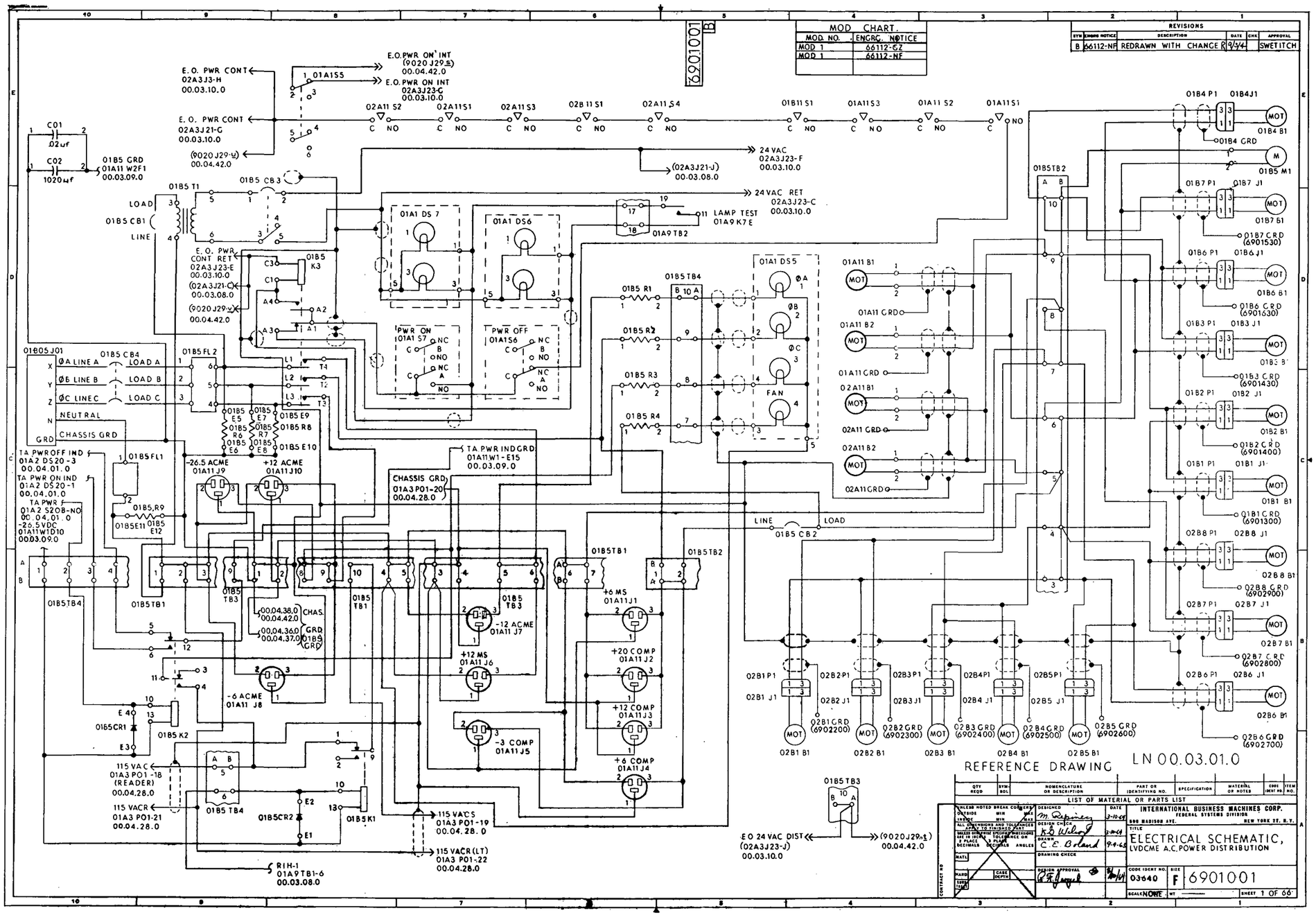


Figure 10-4. LVDCME AC Power Distribution Electrical Schematic Diagram (LN 00.03.01.0)

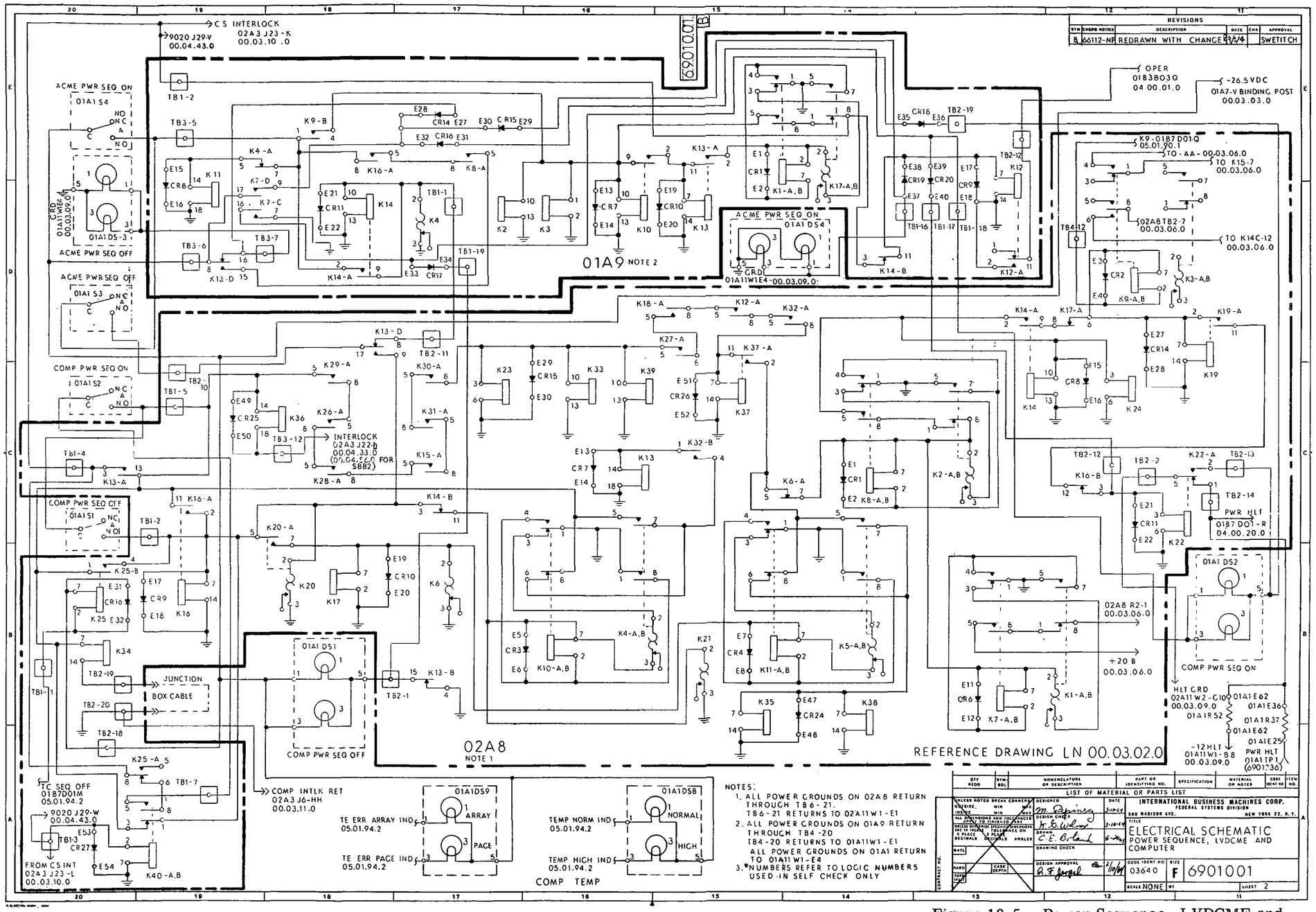


Figure 10-5. Power Sequence, LVDCME and Computer, Electrical Schematid Diagram (LN 00.03.02.0)

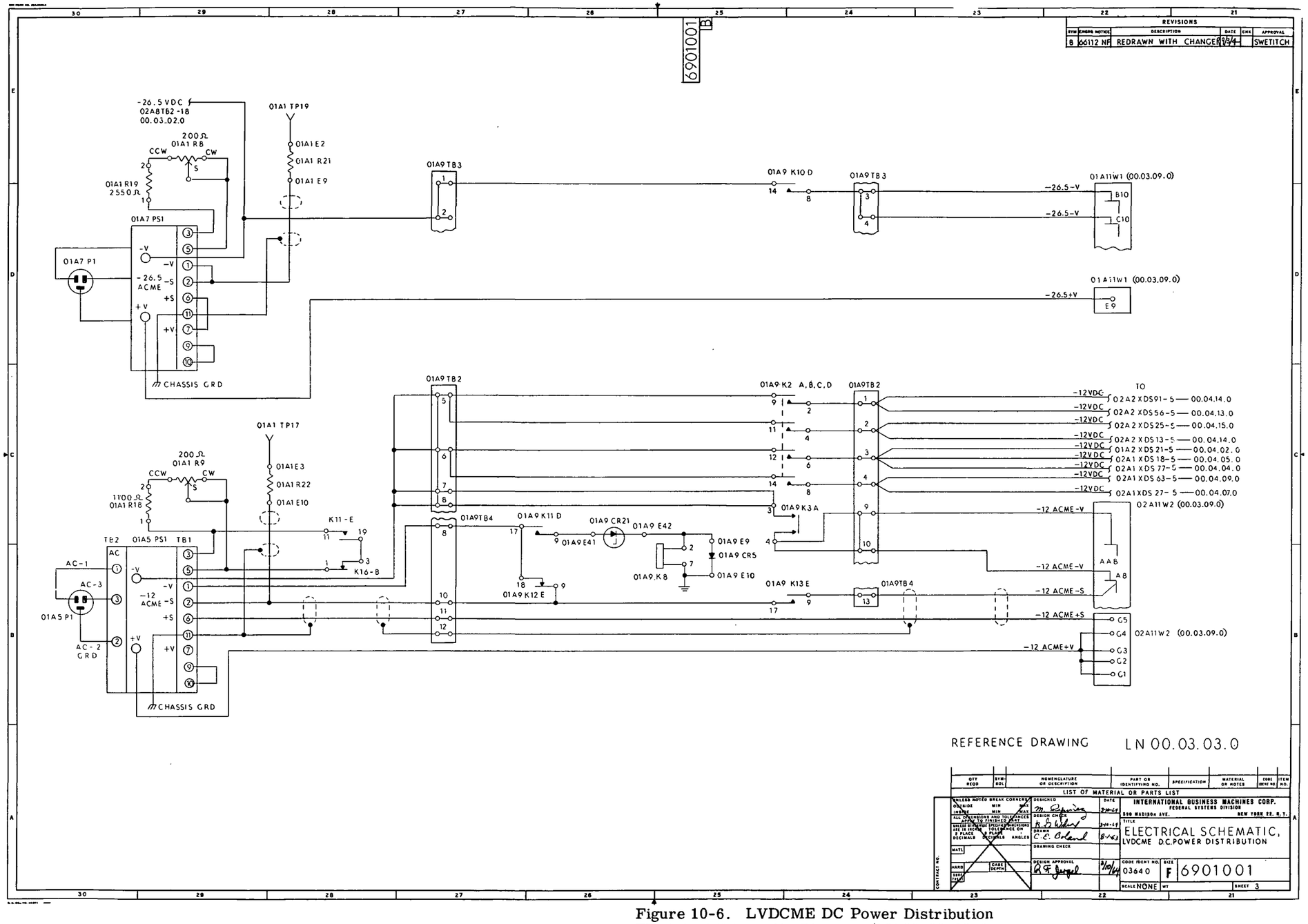


Figure 10-6. LVDCME DC Power Distribution Electrical Schematic Diagram (LN 00.03.03.0 and LN 00.03.04.0) (Sheet 1 of 2)

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
B	66112-NF	REDRAWN WITH CHANGES	6/5/64		SWETITCH

6901001 B

01A1 TP18
100Ω 01A1 R7
CCW CW
549Ω 01A1 R14
01A8 PS1
01A8 P1
+12 ACME
+V +S -S -V
CHASSIS GRD
01A1 E4
01A1 R23
01A1 E11
01A9TB4
01A9TB3
01A9 K11B
01A9 E44
01A9CR22
01A9 E43
01A9 K9
01A9 E12
01A9 CR6
01A9 E11
01A9 K12B
01A9 K10B
01A9 K13B
+12 VDC
01A9 K6-10
00.03.08.0
01A9 TB4
01A9 TB3
02A11W2 (00.03.09.0)
+12 LVDCME +V
+12 LVDCME +S
+12 LVDCME -S
+12 LVDCME -V
A5

01A1 TP16
200Ω 01A1 R10
CCW CW
499Ω 01A1 R11
01A6 PS1
01A6 P1
-6 ACME
-V -S +S +V
CHASSIS GRD
01A1 E5
01A1 R24
01A1 E12
K11-F
K13-F
01A9TB4
01A9 K11C
01A9 K16
01A9 K12C
01A9 E25
01A9 CR13
01A9 E26
01A9 K10C
01A9 K13C
01A9 TB4
02A11W2 (00.03.09.0)
-6 LVDCME -V
-6 LVDCME -V
-6 LVDCME -S
-6 LVDCME +S
-6 LVDCME +V
AA6
A6
E6
E7
E8
G8
G9

REFERENCE DRAWING LN 00.03.04.0

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS ON EDGE MIN INDICE MIN MAX ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 3 PLACE DECIMALS 2 PLACE DECIMALS ANGLES MATL HARD SURF ISSUE CASE DEPTH CONTRACT NO.	DESIGNED M. Kleinrock DESIGN CHIEF K.Y. Wilson DRAWN C.E. Boland 6-1-63 DRAWING CHECK DESIGN APPROVAL QE R.E. Jaegel 8/10/64	DATE 3-04-64 3-04-64
INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION 590 MADISON AVE. NEW YORK 22, N.Y.		
TITLE ELECTRICAL SCHEMATIC, LVDCME D.C. POWER DISTRIBUTION		
CODE IDENT NO. 03640	SIZE F	6901001
SCALE NONE	WT	SHEET 4

Figure 10-6. LVDCME DC Power Distribution Electrical Schematic Diagram (LN 00.03.03.0 and LN 00.03.04.0) (Sheet 2)

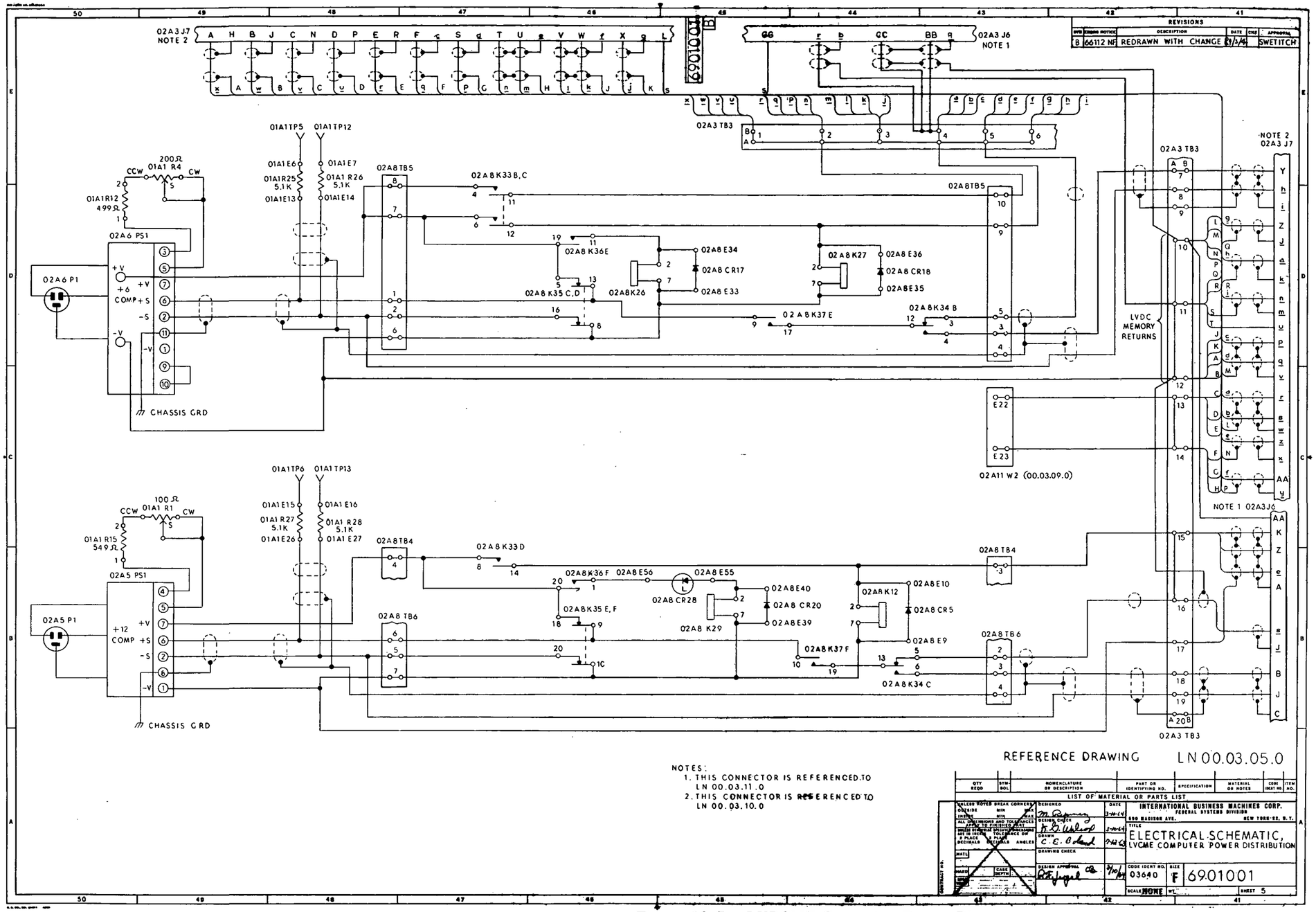


Figure 10-7. LVDCME Computer Power Distribution Electrical Schematic Diagram (LN 00.03.05.0 and LN 00.03.06.0) (Sheet 1 of 2)

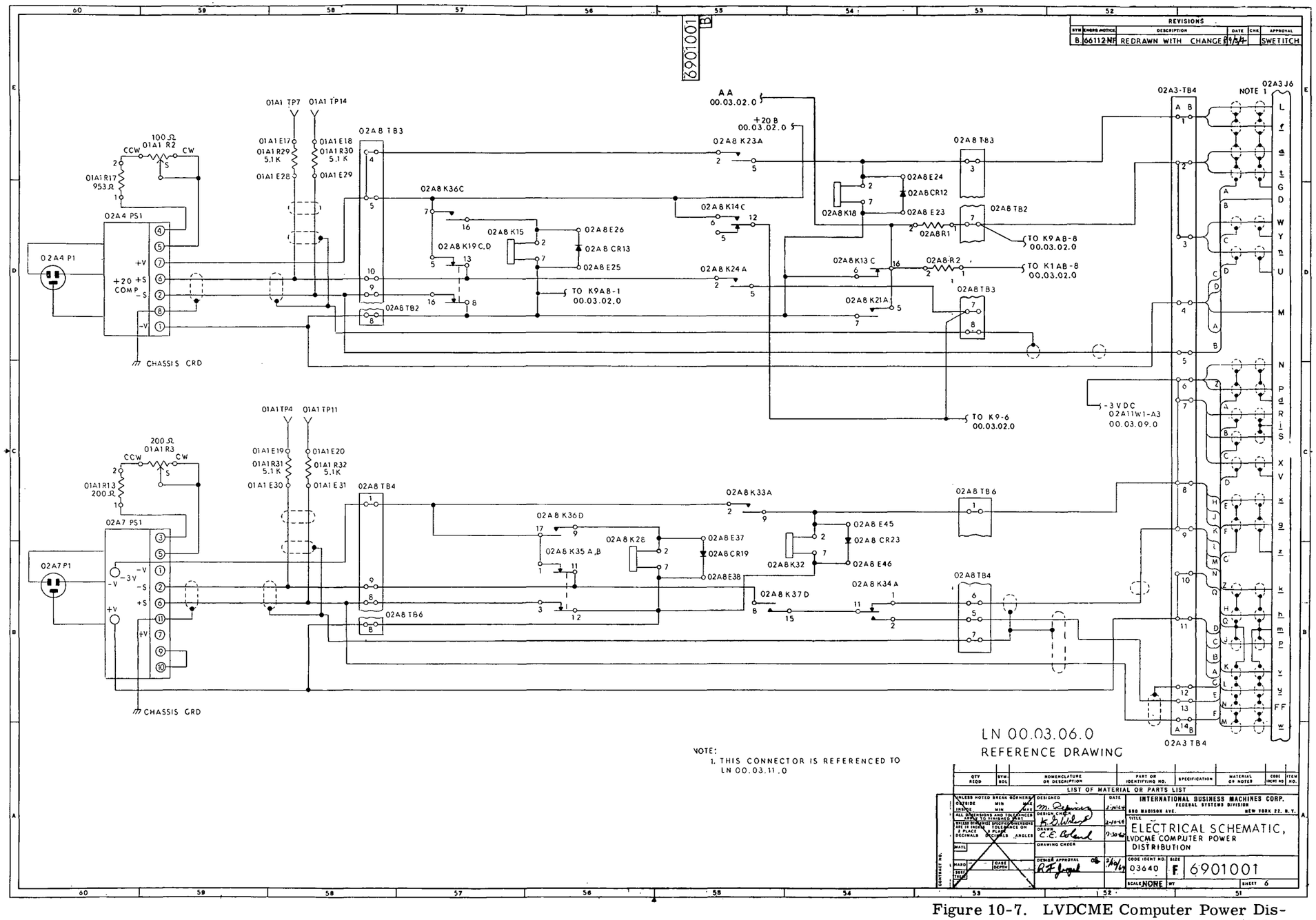


Figure 10-7. LVDCME Computer Power Distribution Electrical Schematic Diagram (LN 00.03.05.0 and LN 00.03.06.0) (Sheet 2)

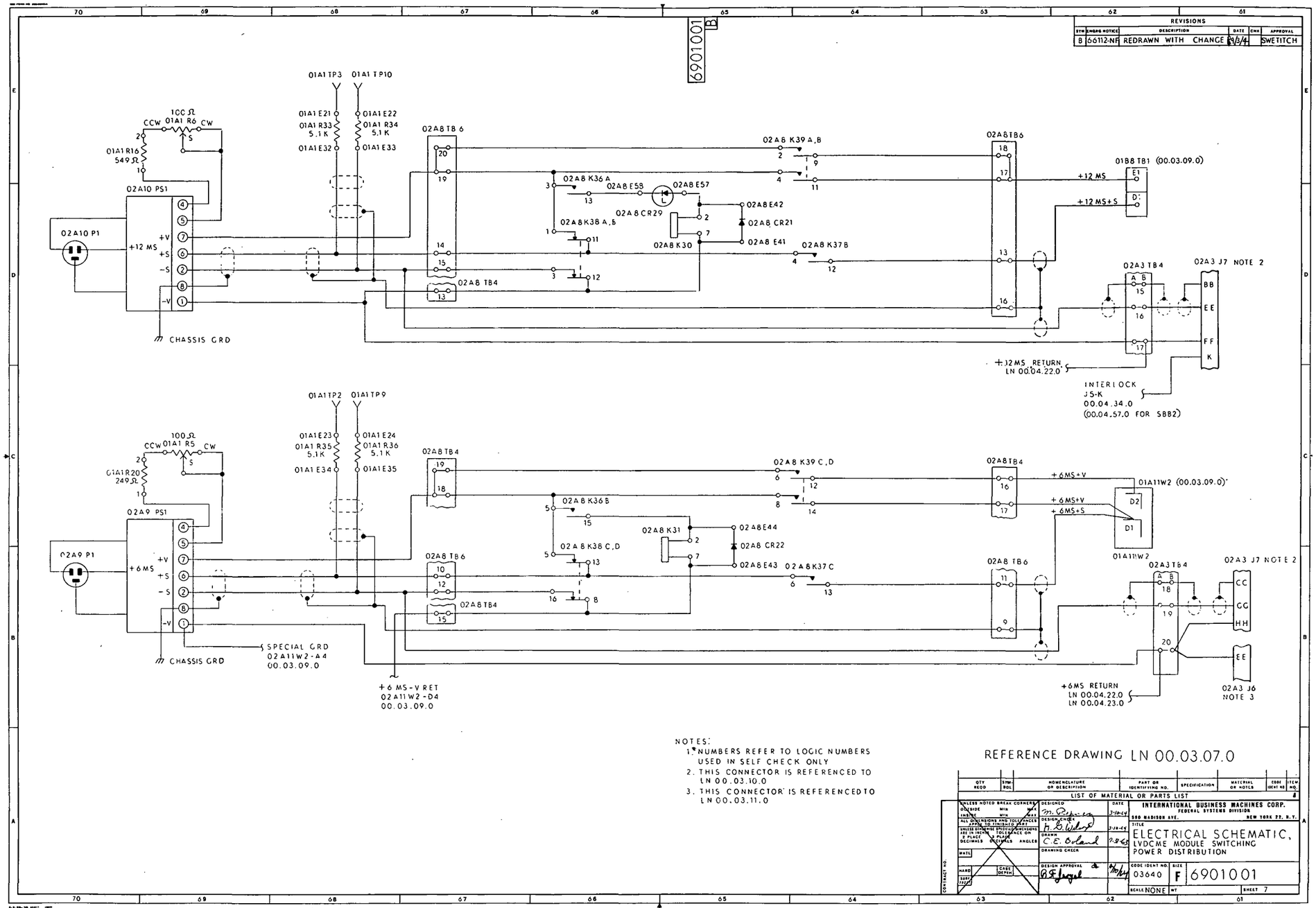


Figure 10-8. LVDCME Module Switching Power Distribution Electrical Schematic Diagram (LN 00.03.07.0)

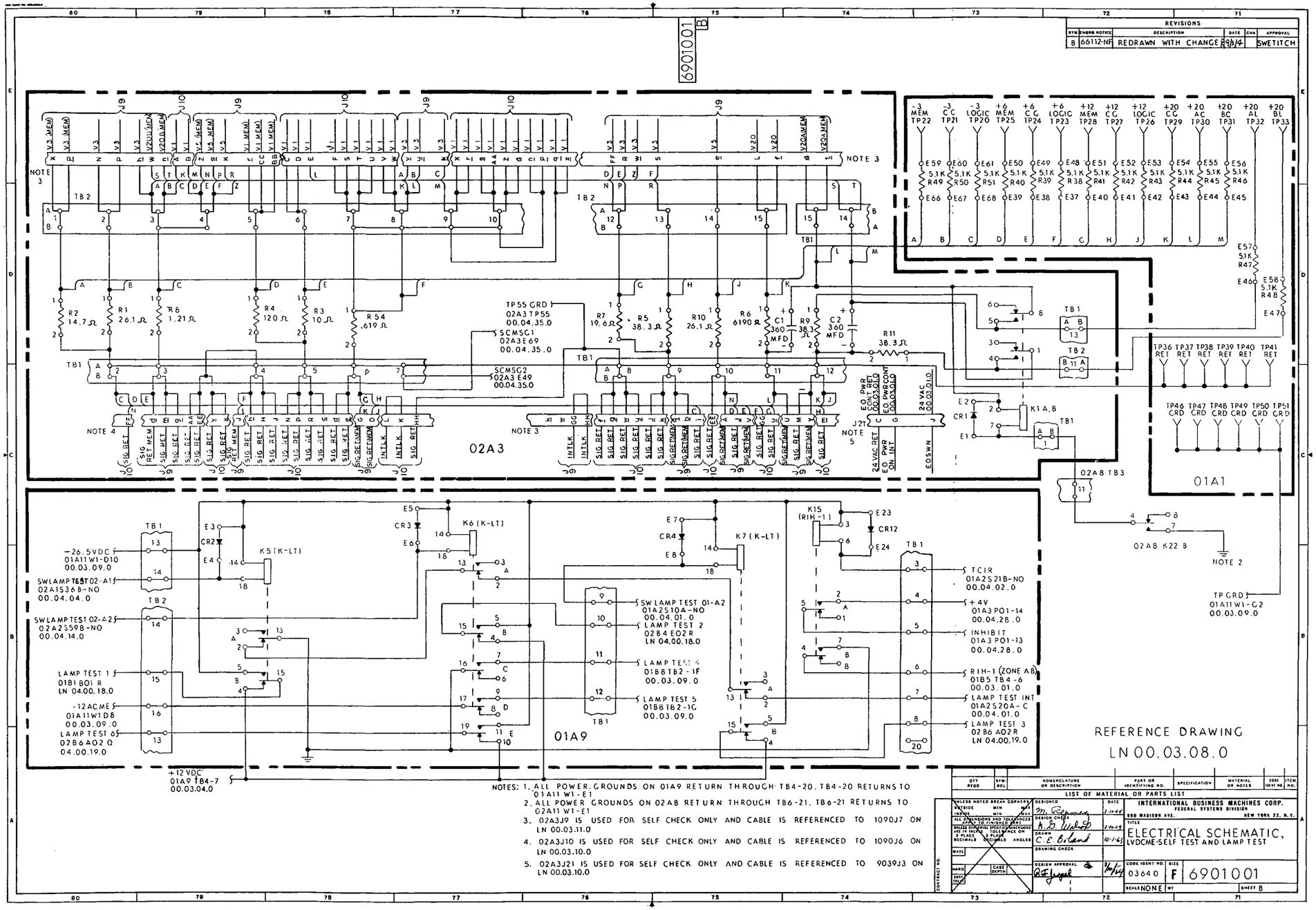


Figure 10-9. LVDCME Self Test and Lamp Test Electrical Schematic Diagram (LN 00.03.08.0)

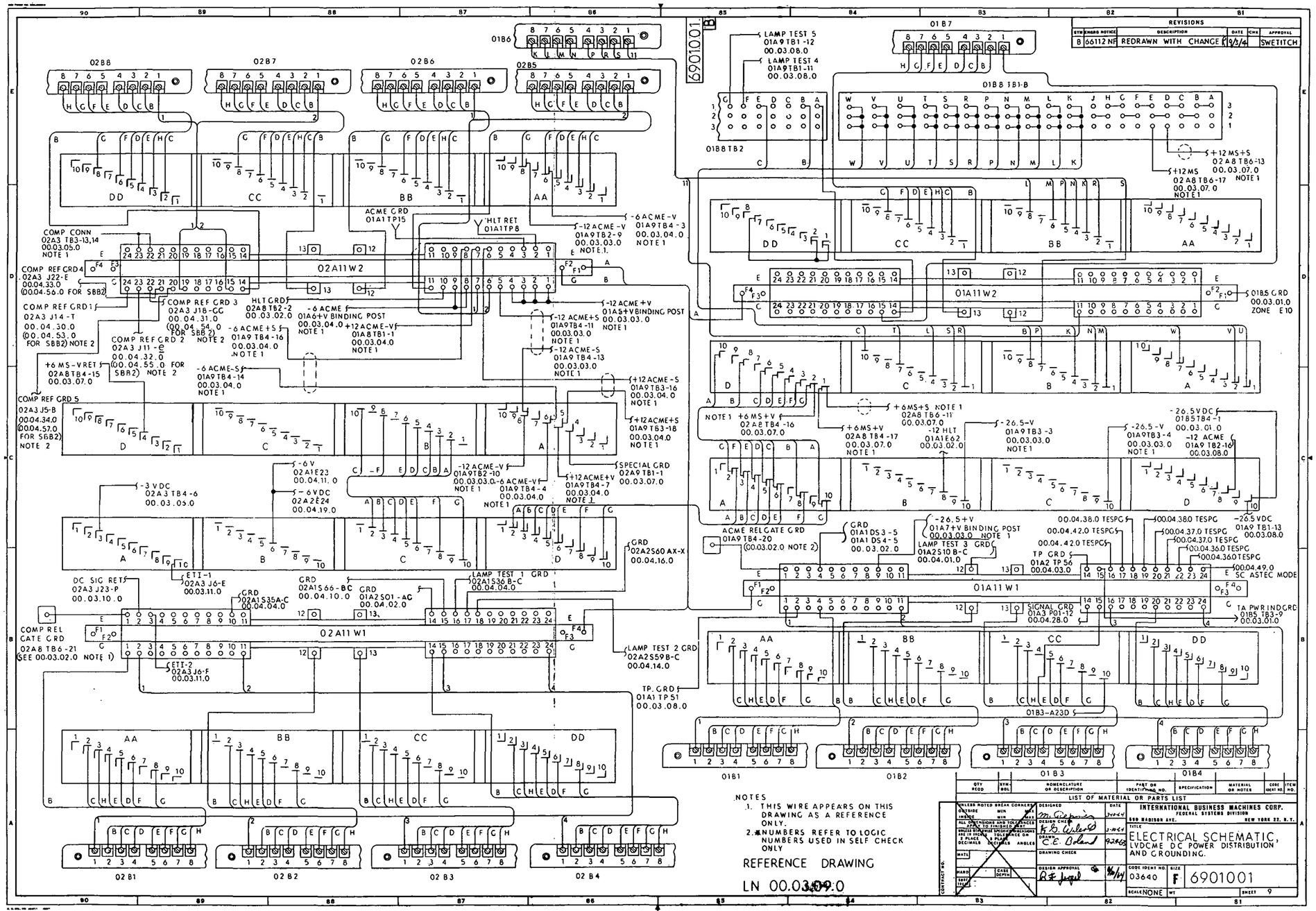
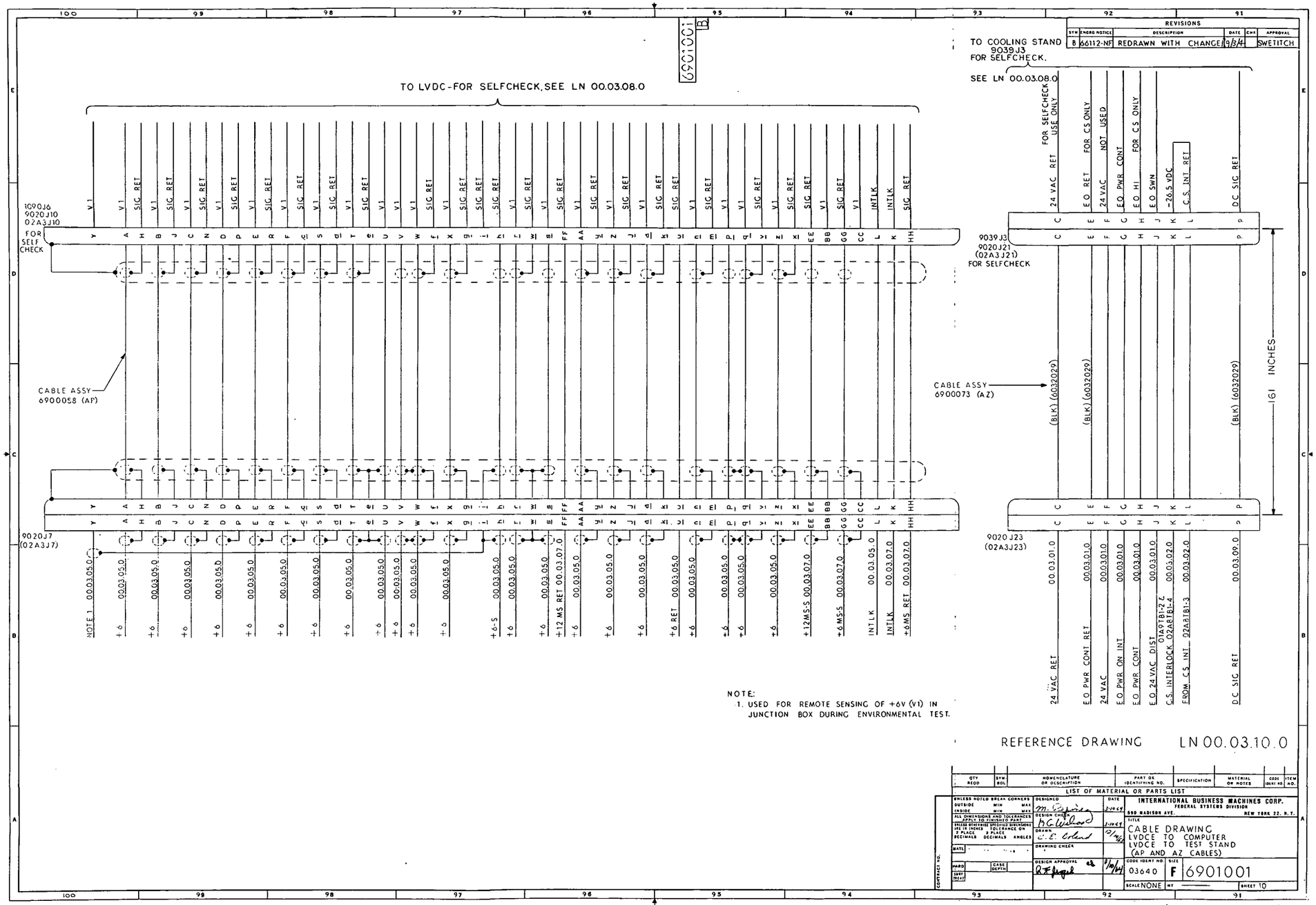


Figure 10-10. LVDCME DC Power Distribution and Grounding Electrical Schematic Diagram (LN 00.03.09.0)



REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
B	66112-NF	REDRAWN WITH CHANGE	9/3/64		SWETITCH

Figure 10-11. Cable Drawing (AP, AZ, and AN Cables) LVDCME to Computer and Test Stand (LN 00.03.10.0 and LN 00.03.11.0) (Sheet 1 of 2)

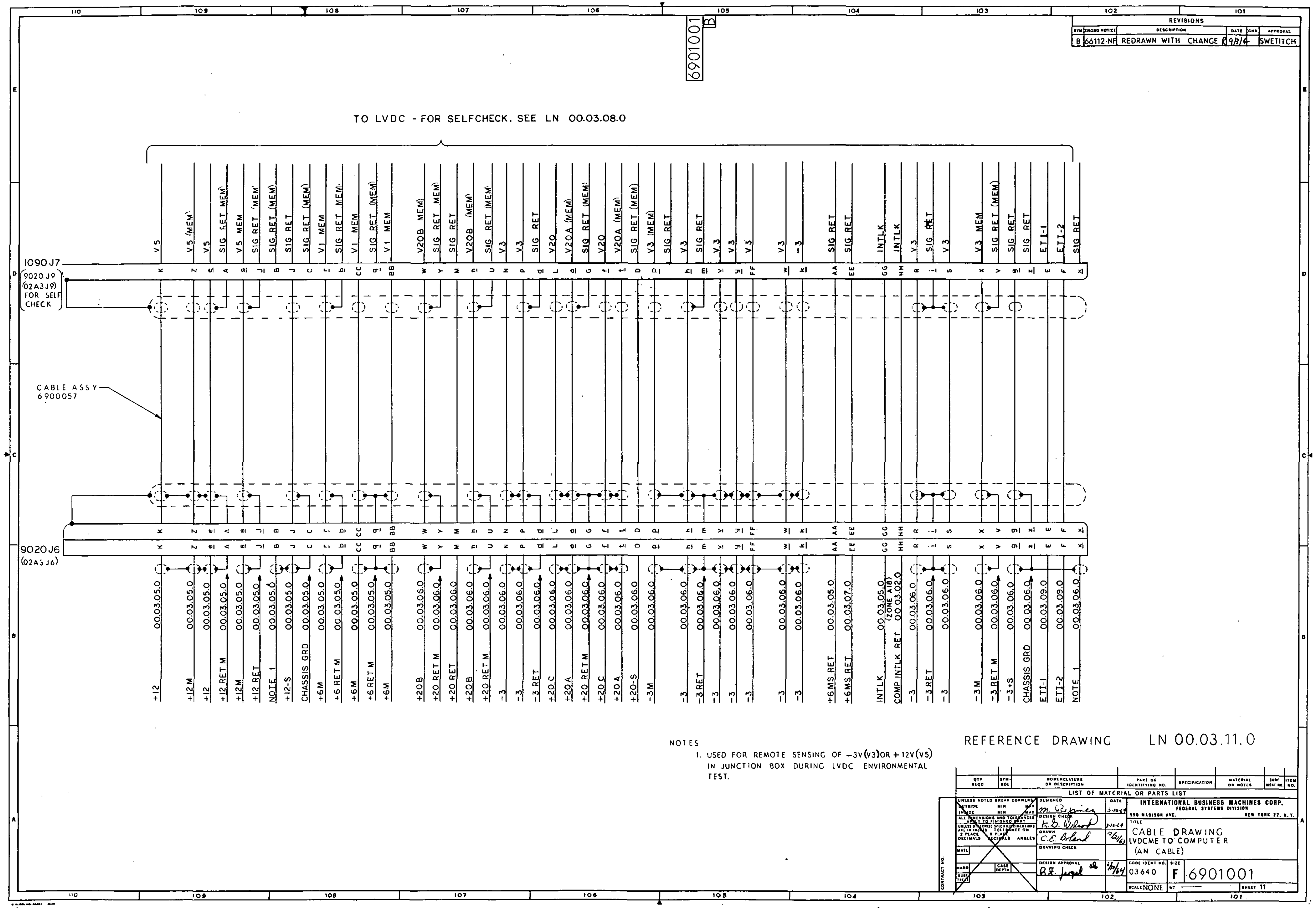


Figure 10-11. Cable Drawing (AP, AZ, and AN Cables) LVDCME to Computer and Test Stand (LN00.03.10.0 and LN 00.03.11.0) (Sheet 2)

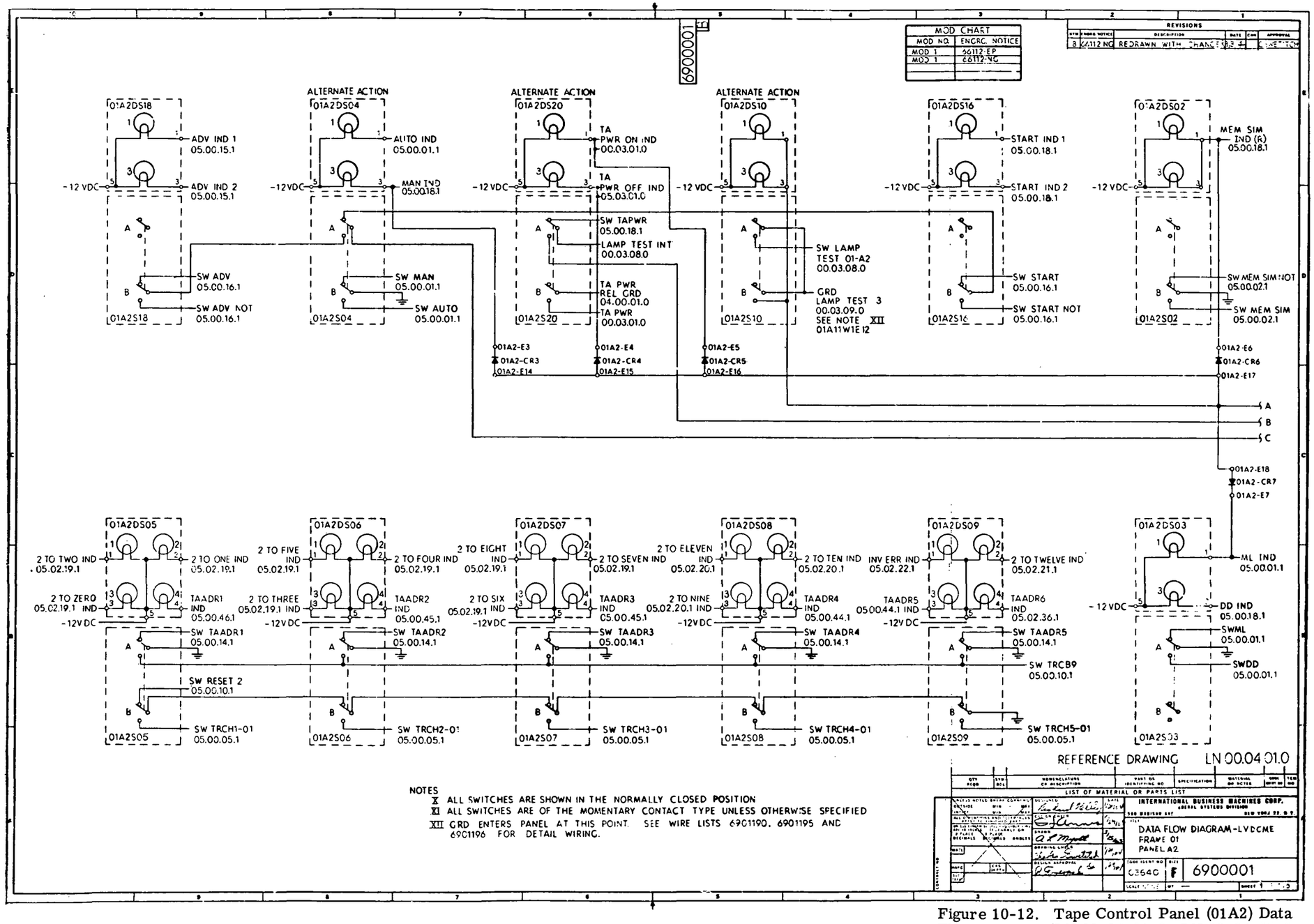


Figure 10-12. Tape Control Panel (01A2) Data Flow Diagram (LN 00.04.01.0, LN 00.04.02.0 and LN 00.04.03.0) (Sheet 1 of 3)

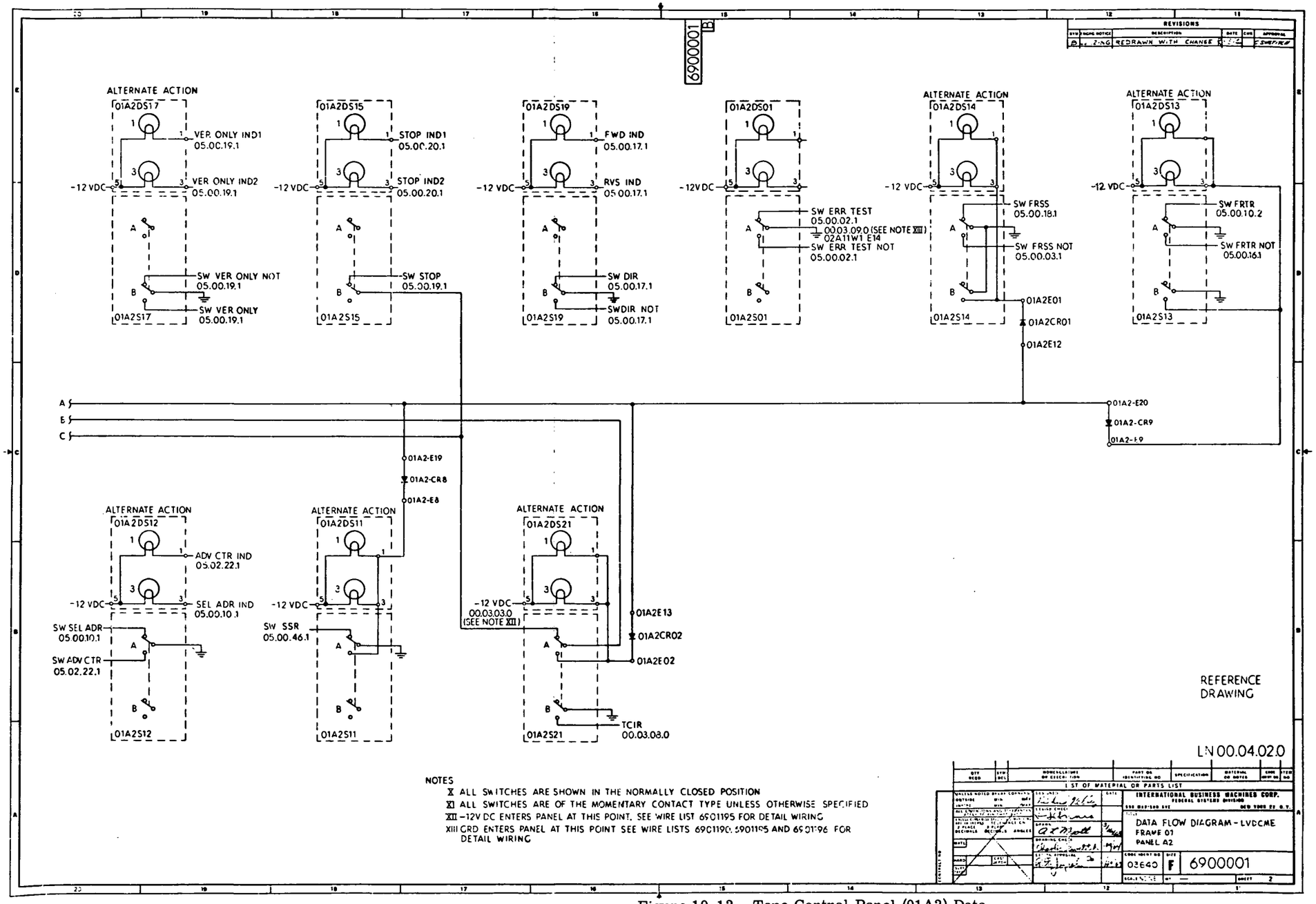


Figure 10-12. Tape Control Panel (01A2) Data Flow Diagram (LN 00.04.01.0, LN 00.04.02.0 and LN 00.04.03.0) (Sheet 2)

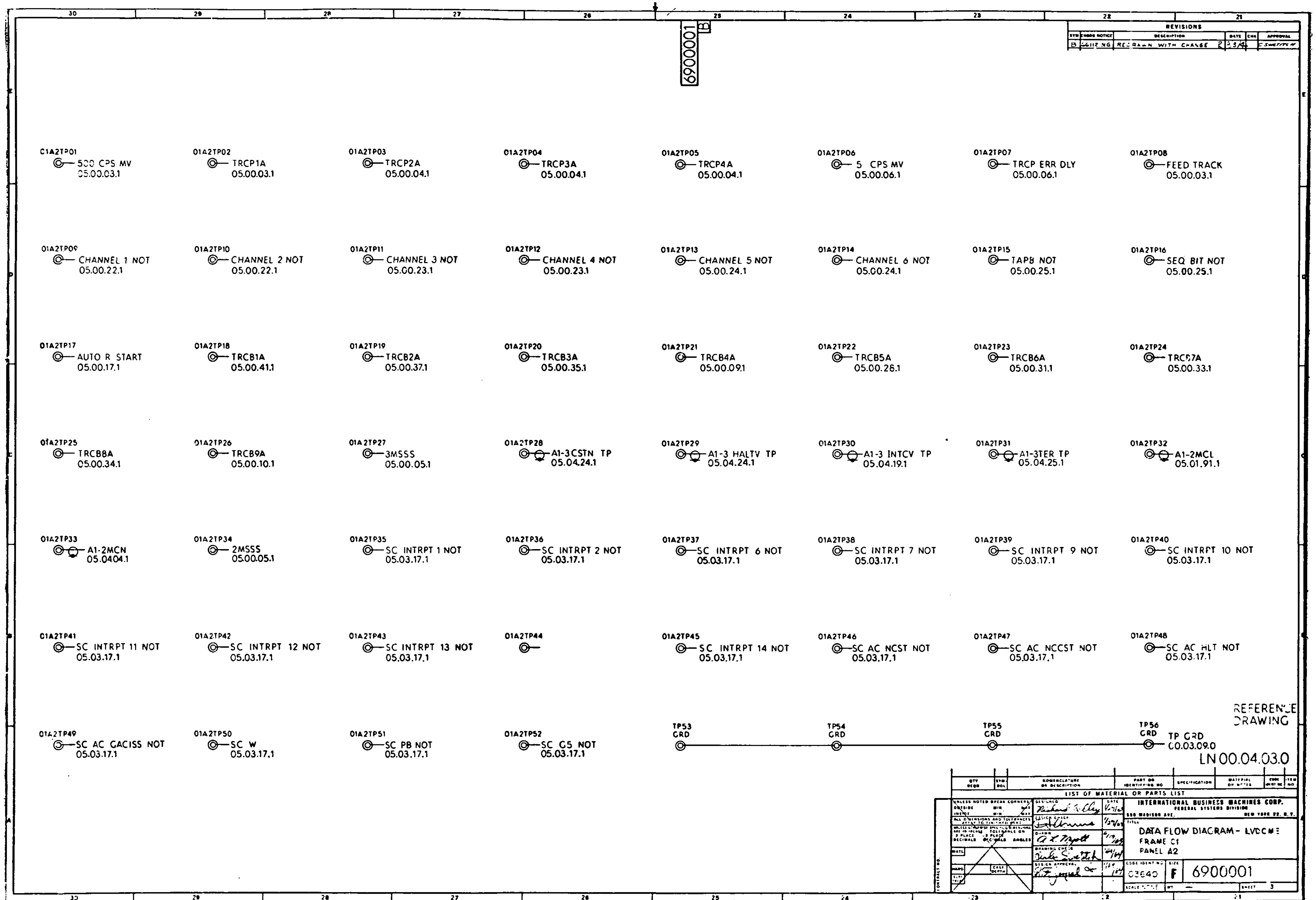


Figure 10-12. Tape Control Panel (01A2) Data Flow Diagram (LN 00.04.01.0, LN 00.04.02.0 and LN 00.04.03.0) (Sheet 3)

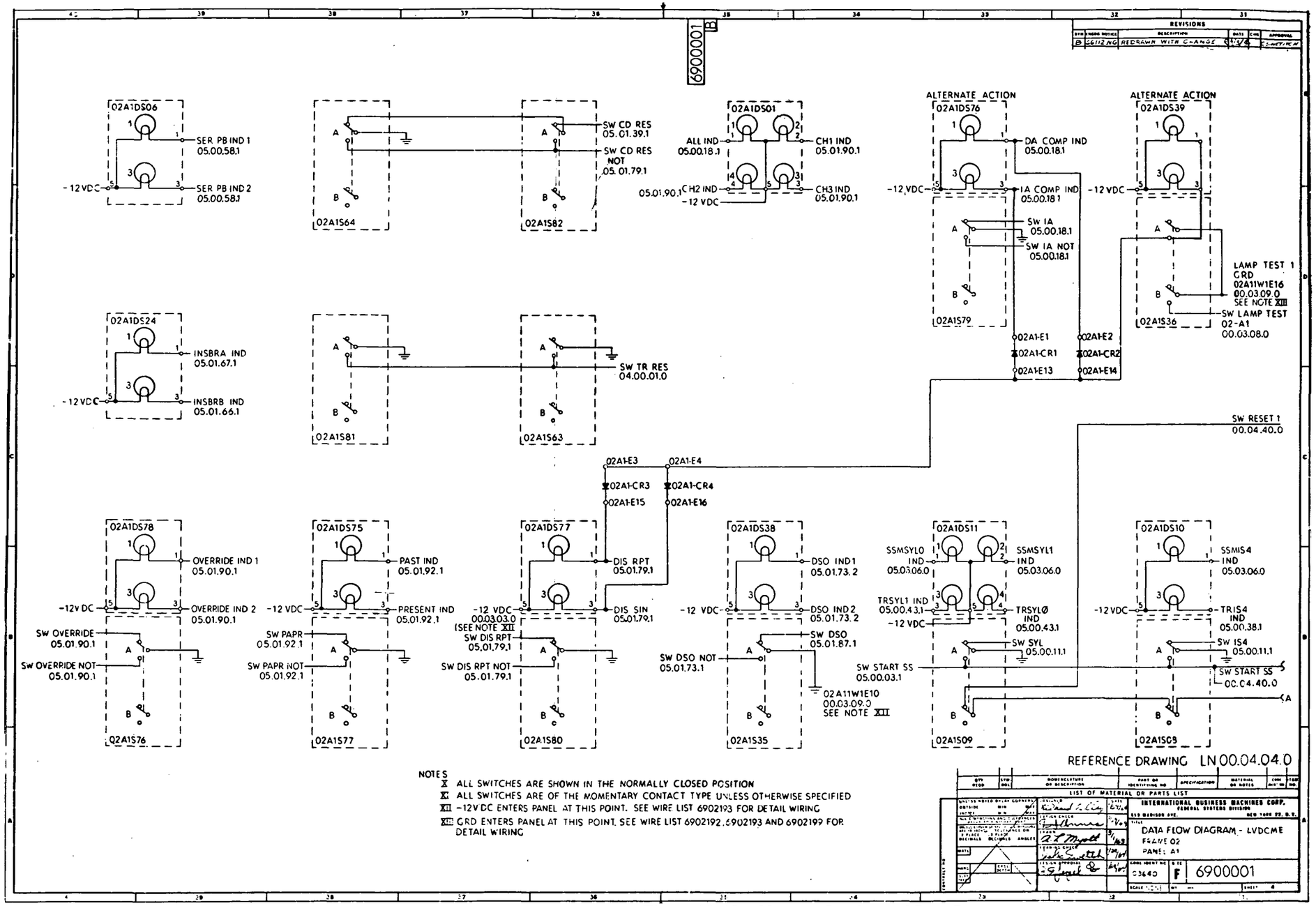


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 1 of 8)

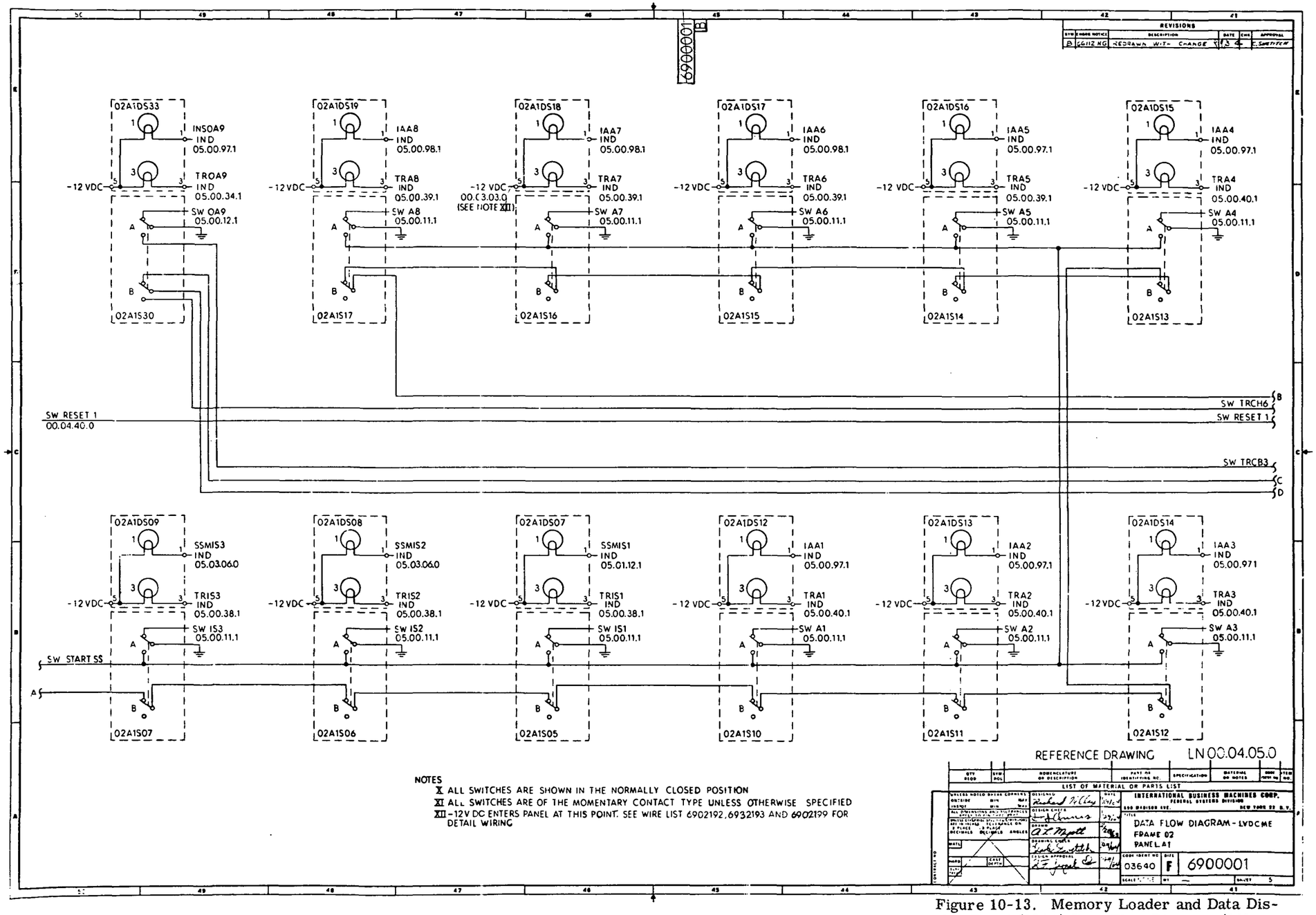


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 2)

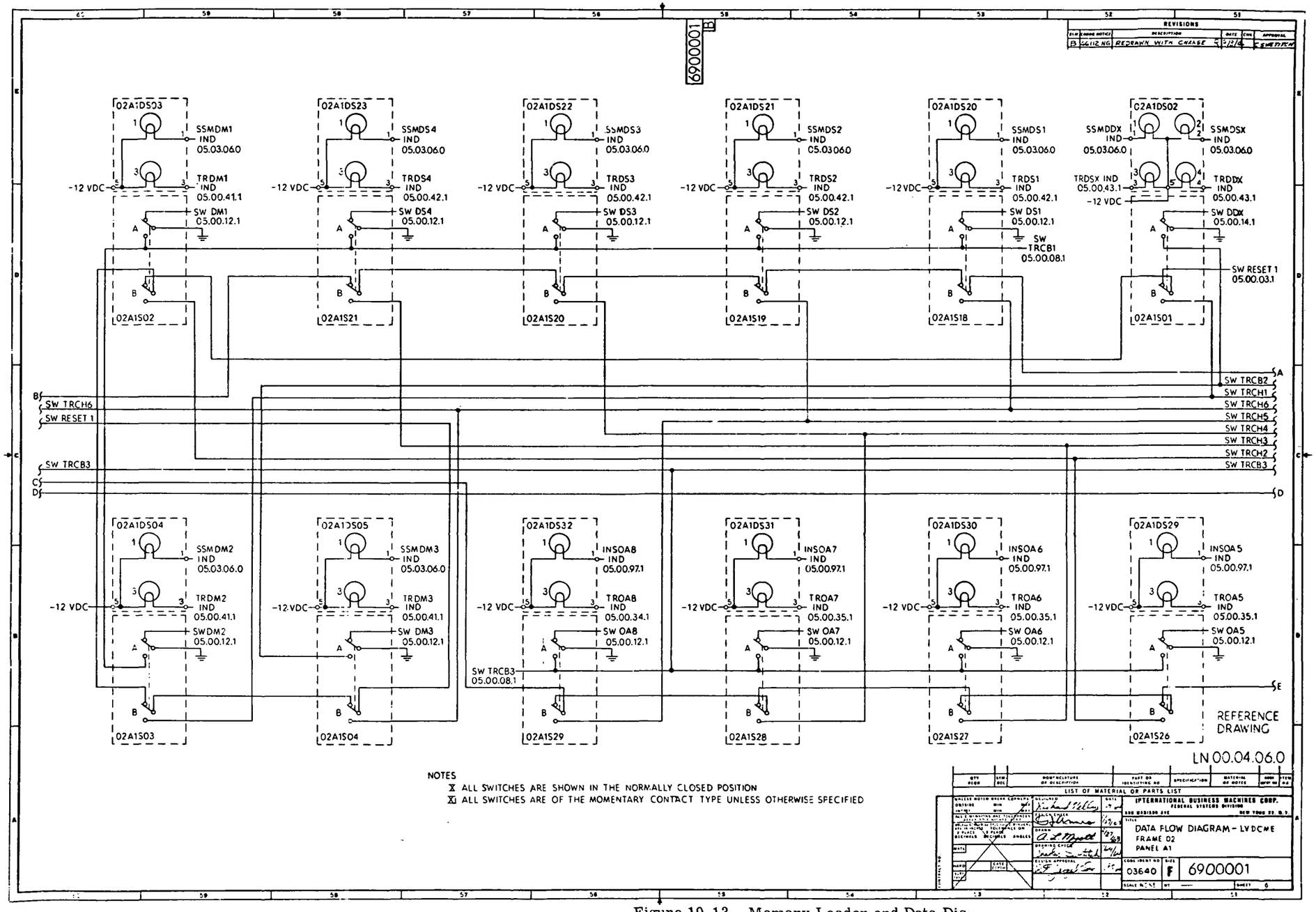


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 3)

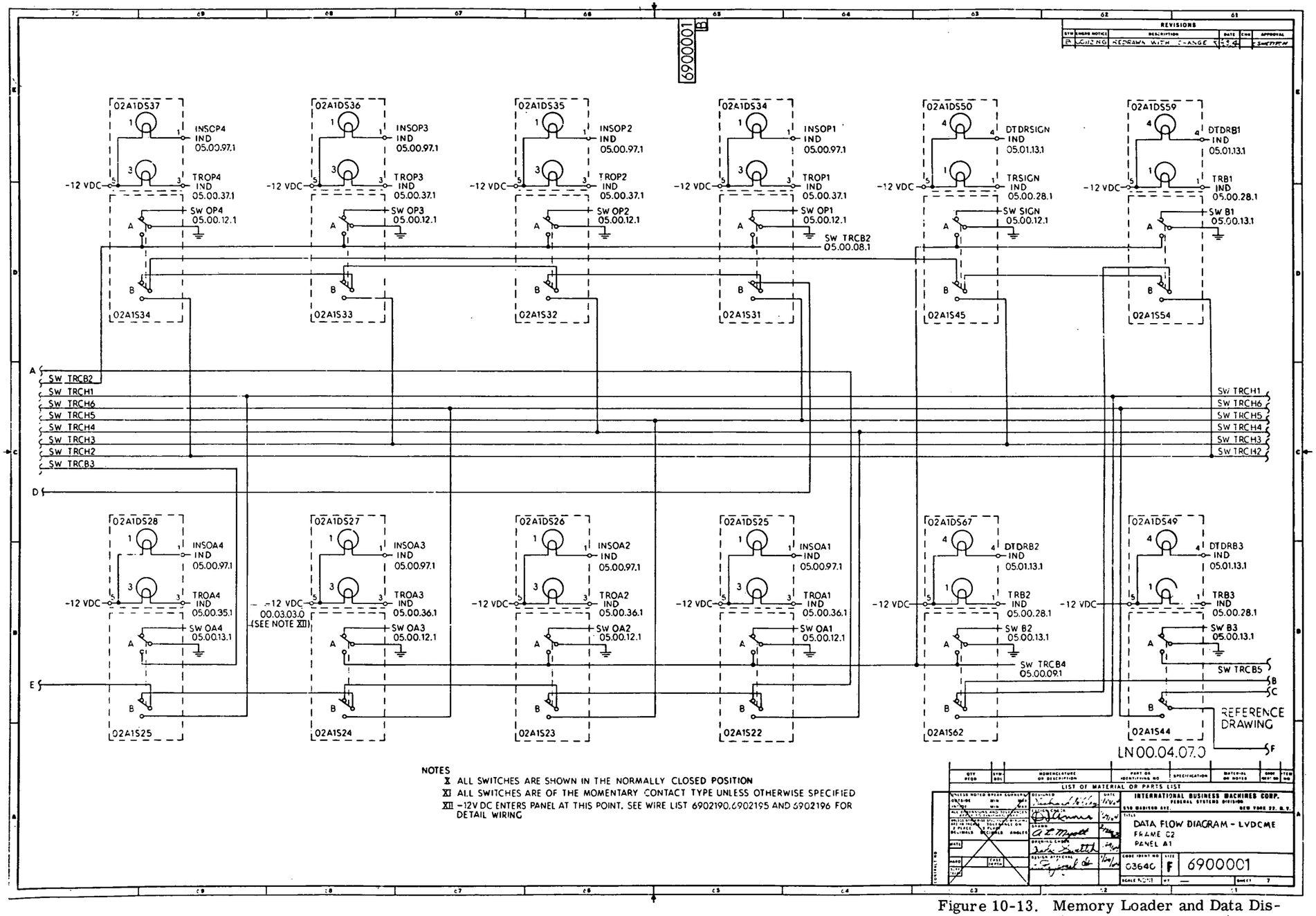


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 4)

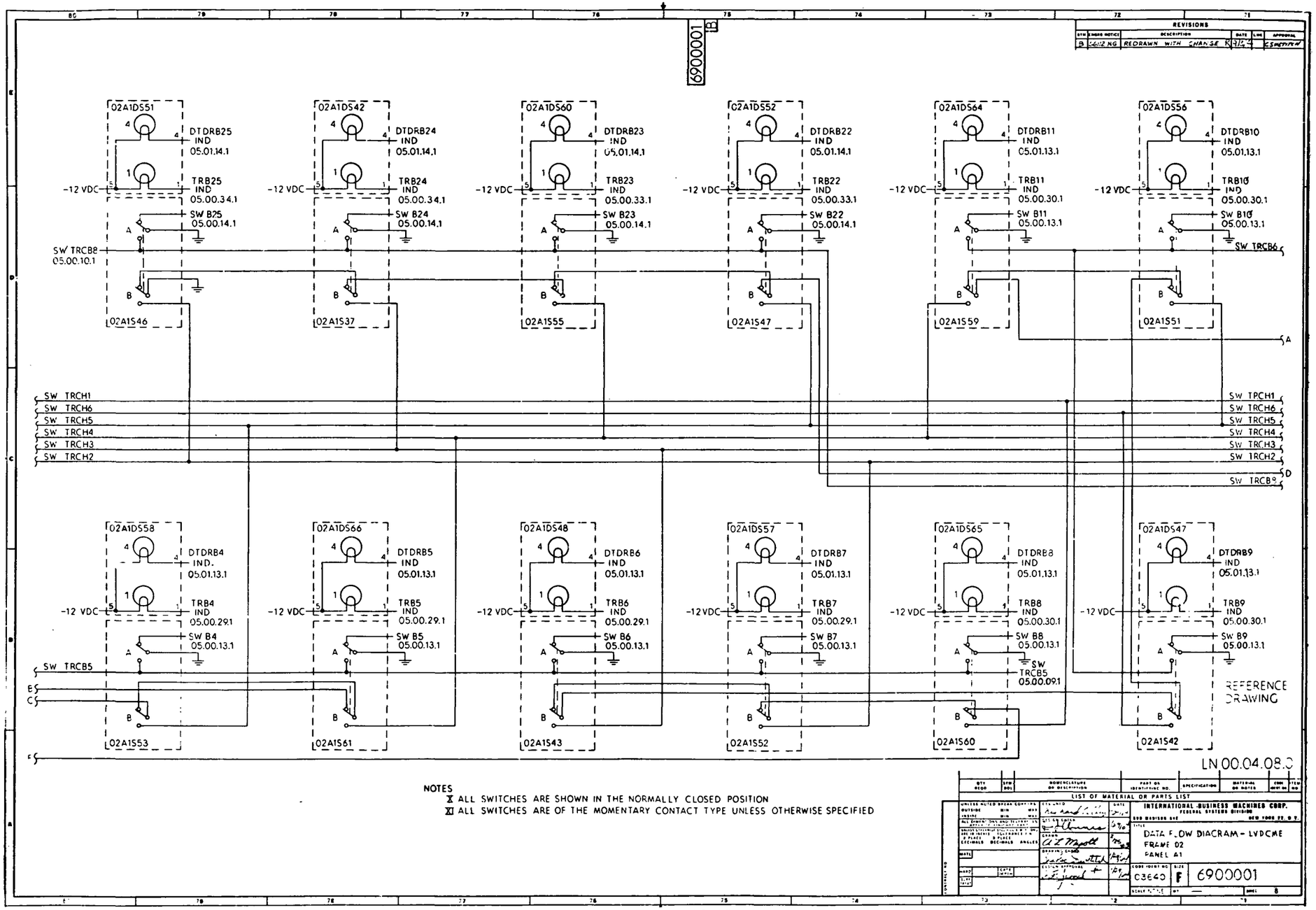


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 5)

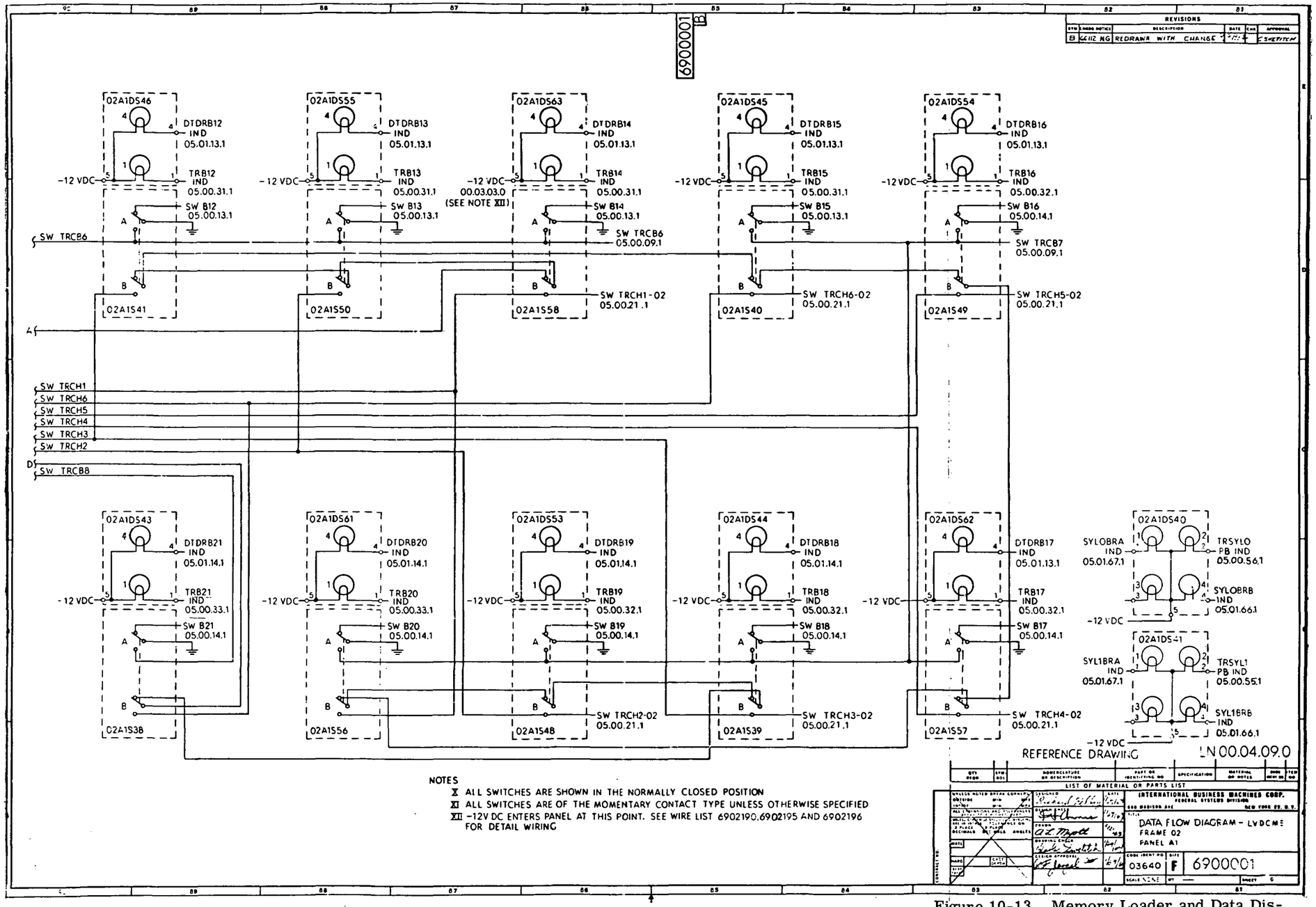


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 6)

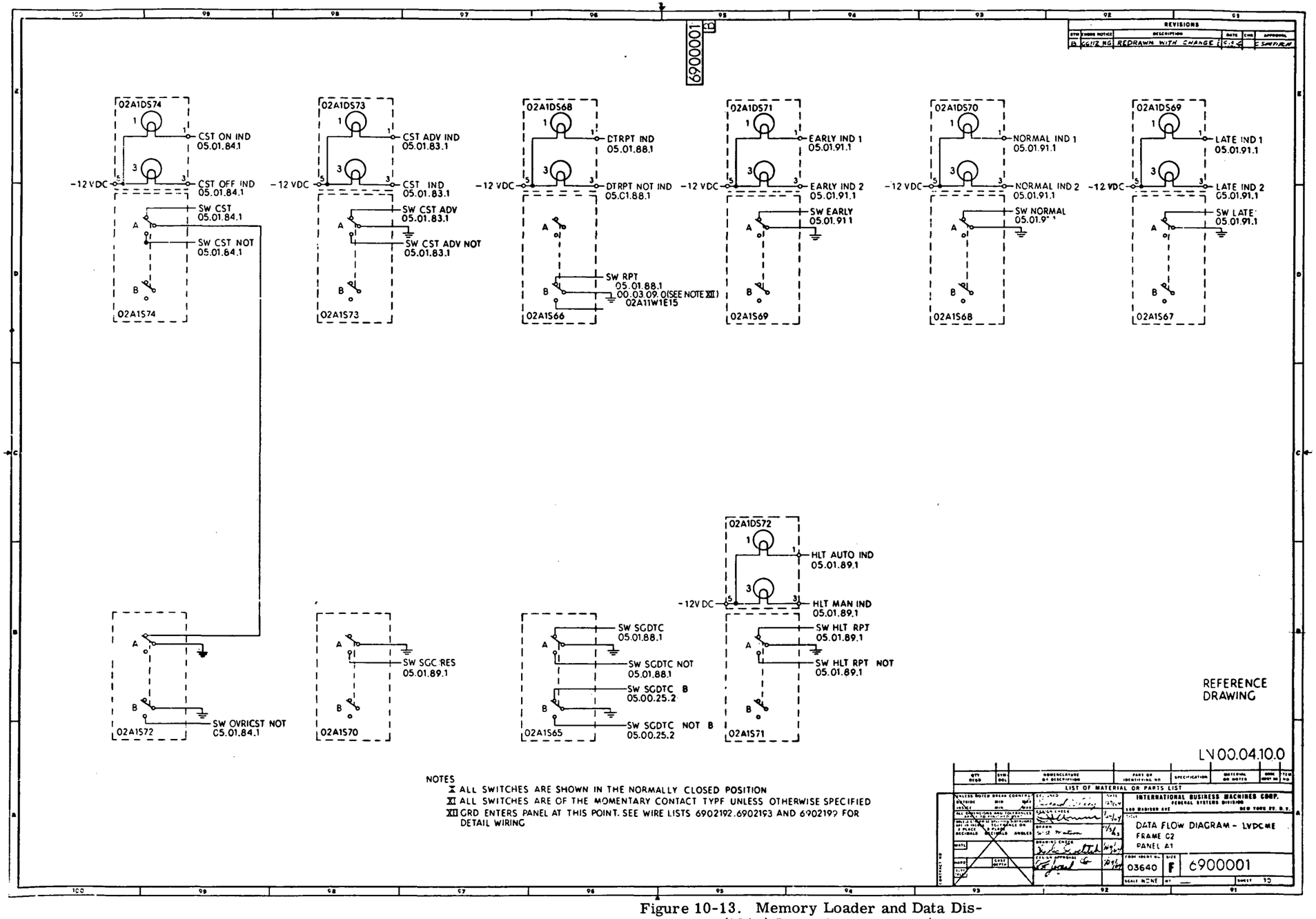
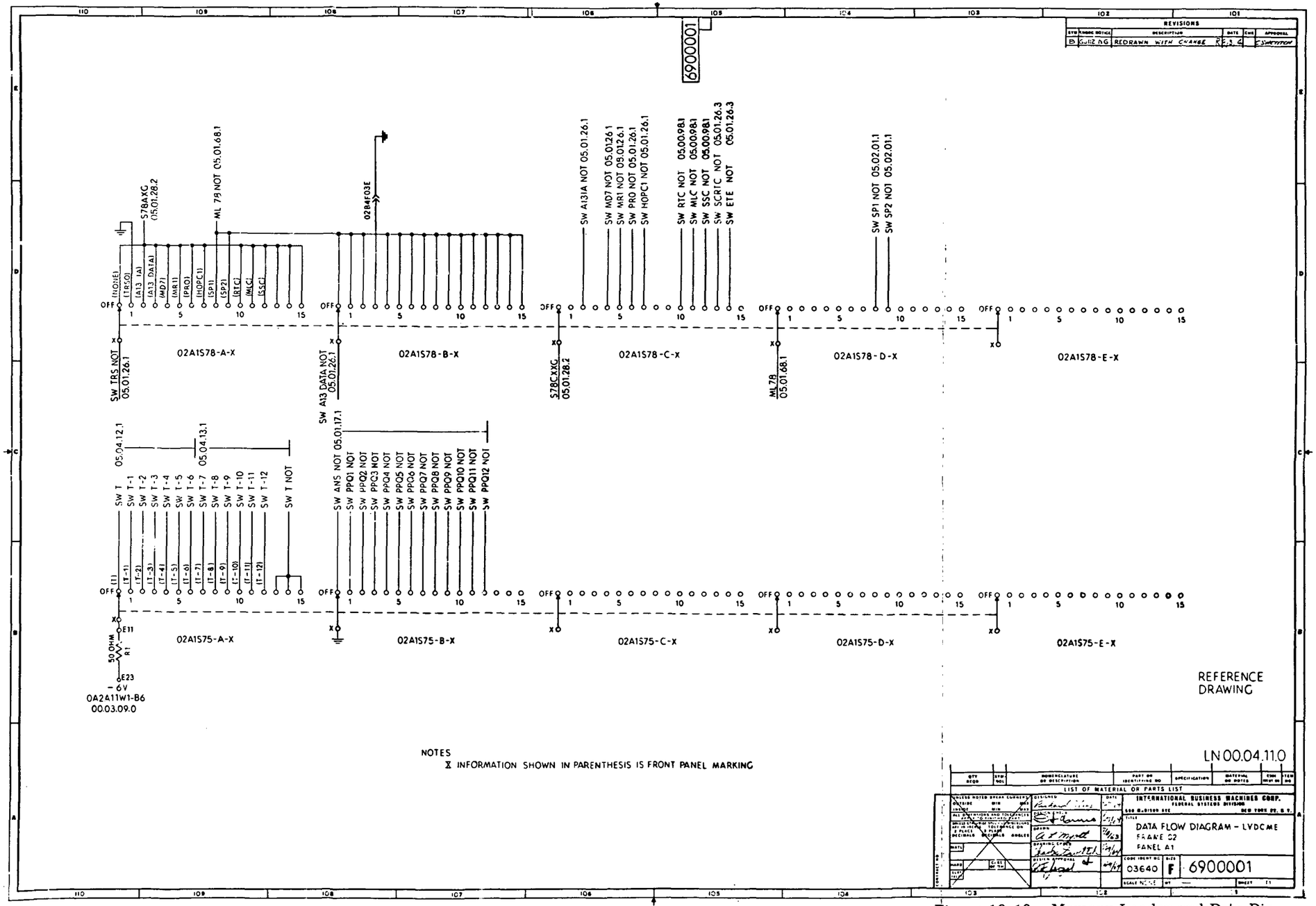


Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 7)



NOTES

X INFORMATION SHOWN IN PARENTHESIS IS FRONT PANEL MARKING

Figure 10-13. Memory Loader and Data Display Panel (02A1) Data Flow Diagram (LN 00.04.04.0 through LN 00.04.11.0) (Sheet 8)

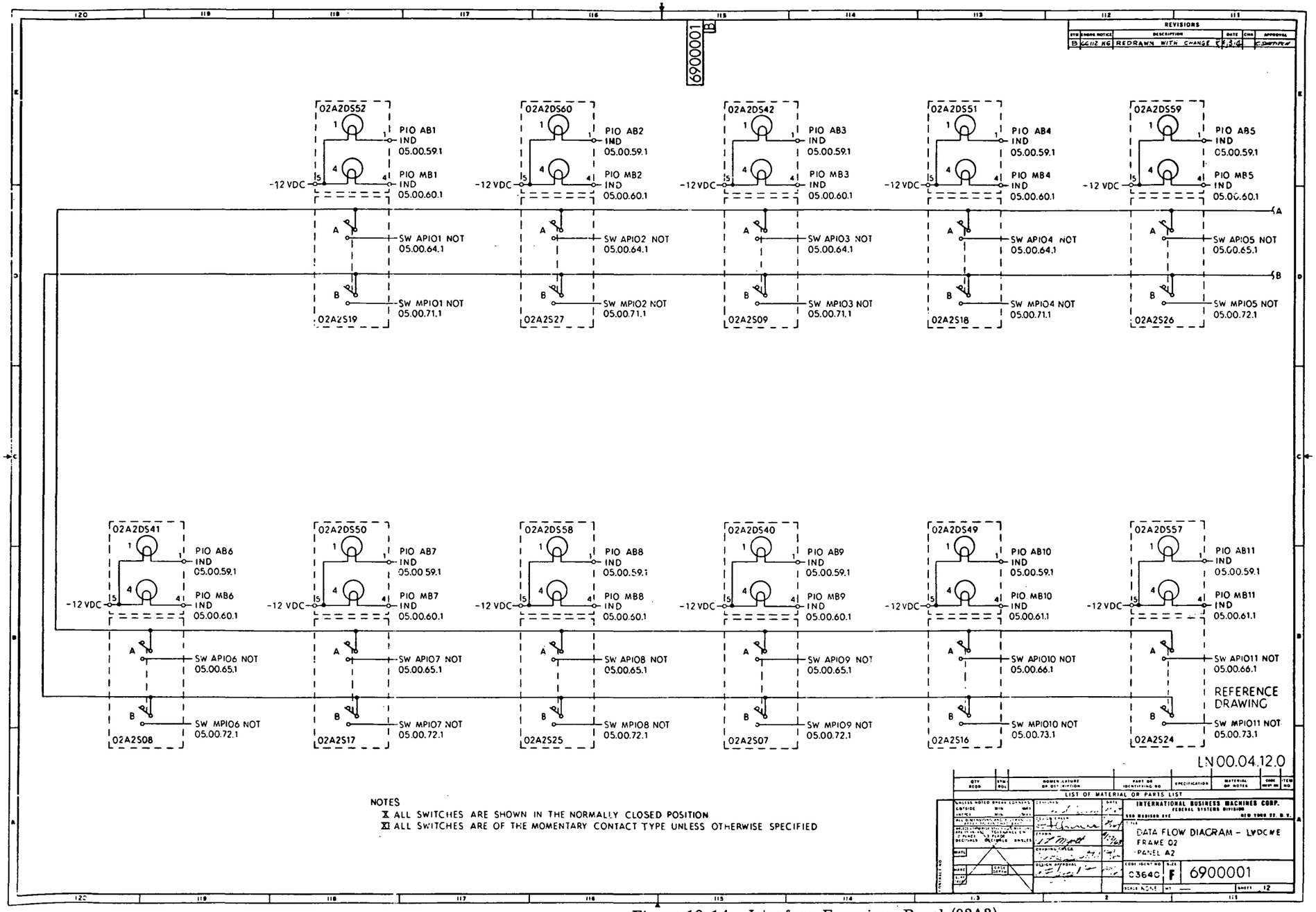


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 1 of 8)

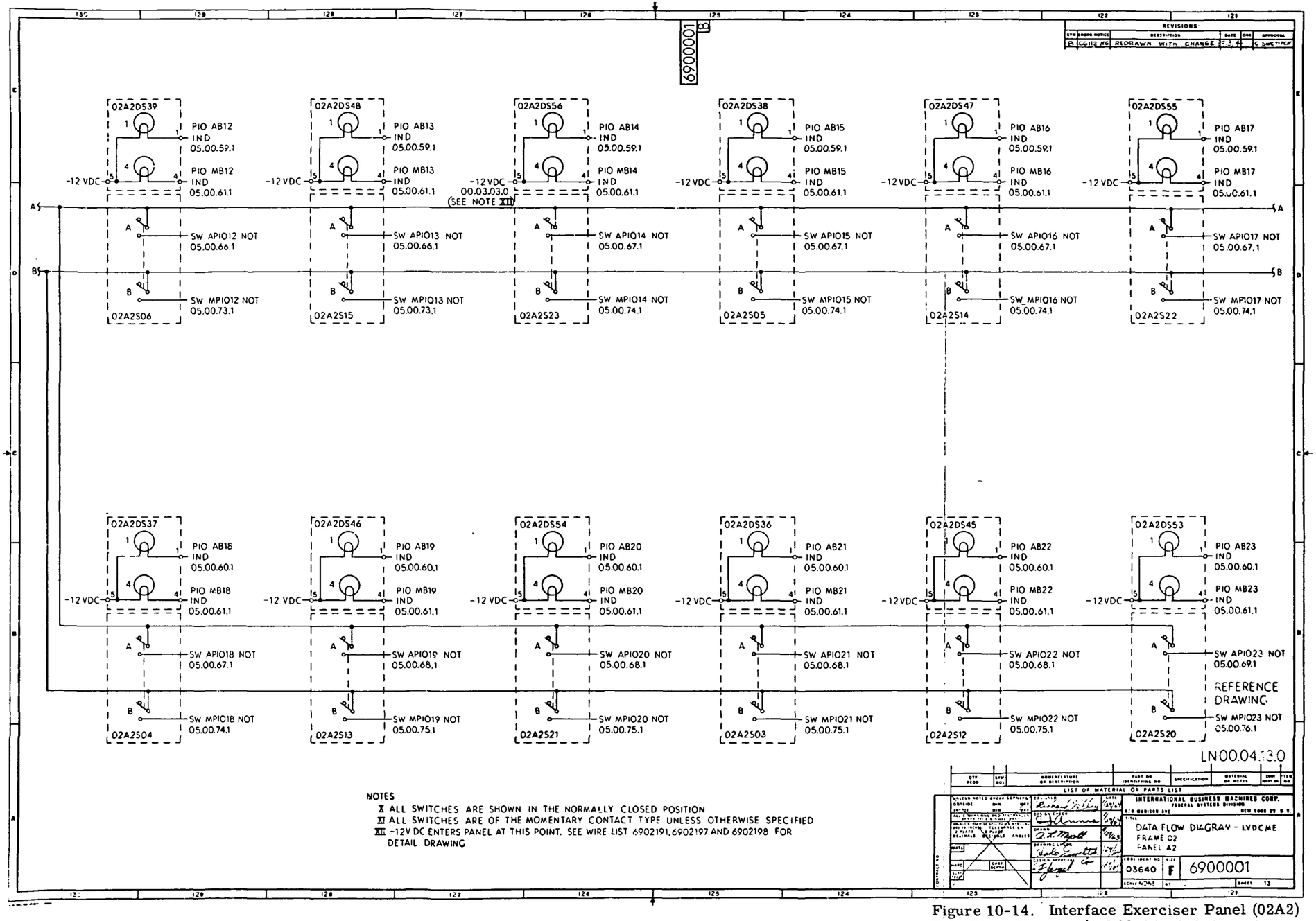


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 2)

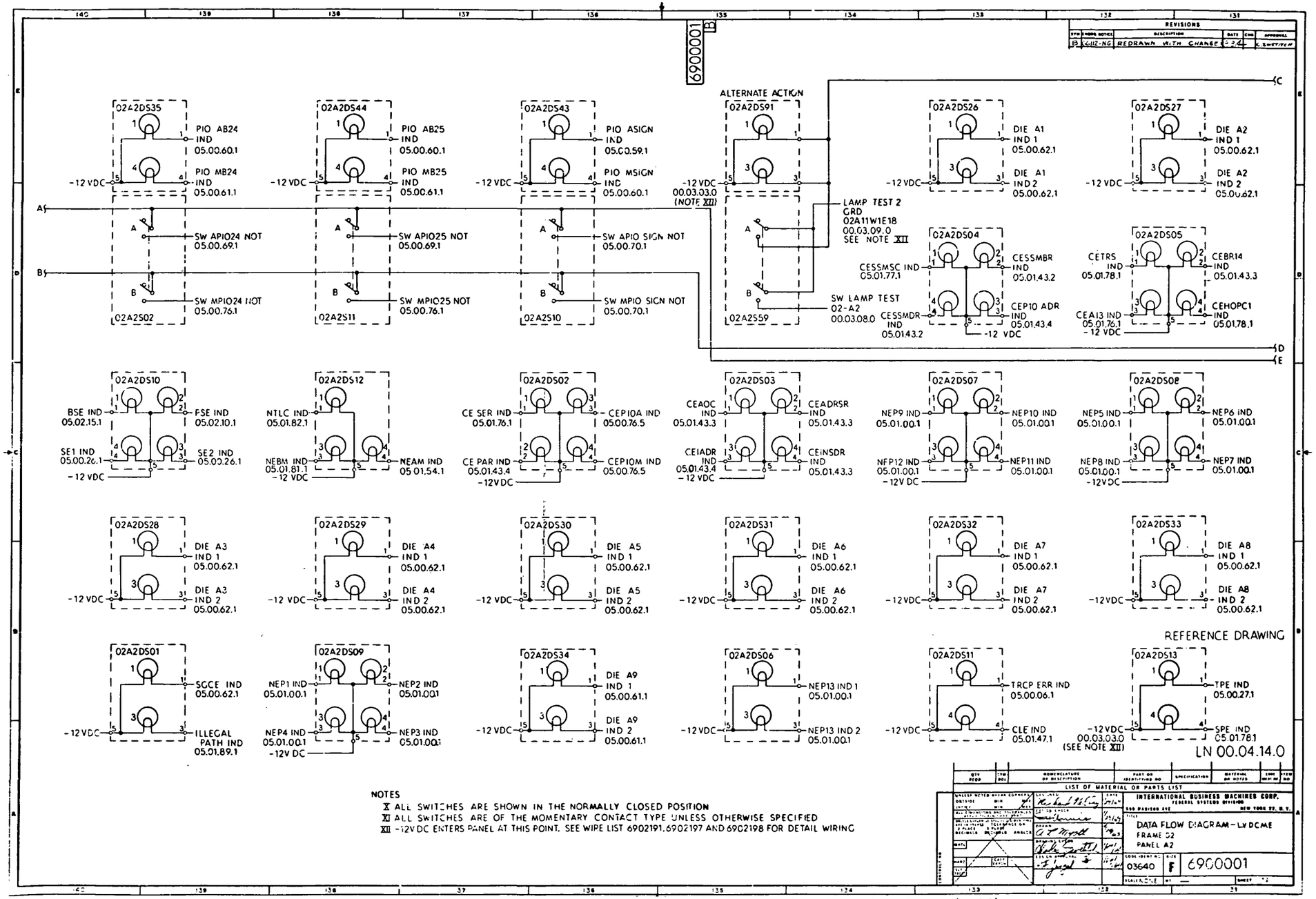


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 3)

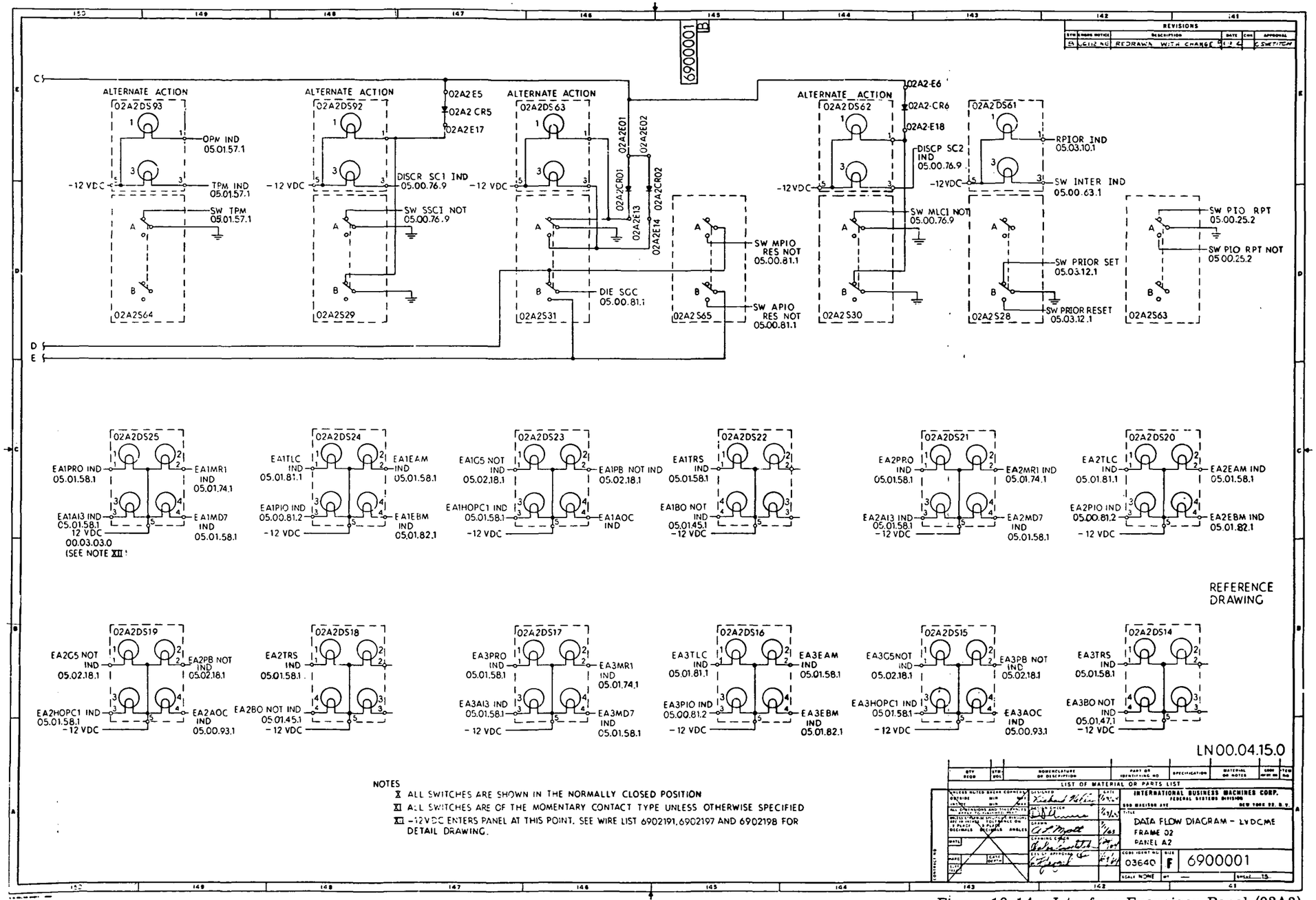


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 4)

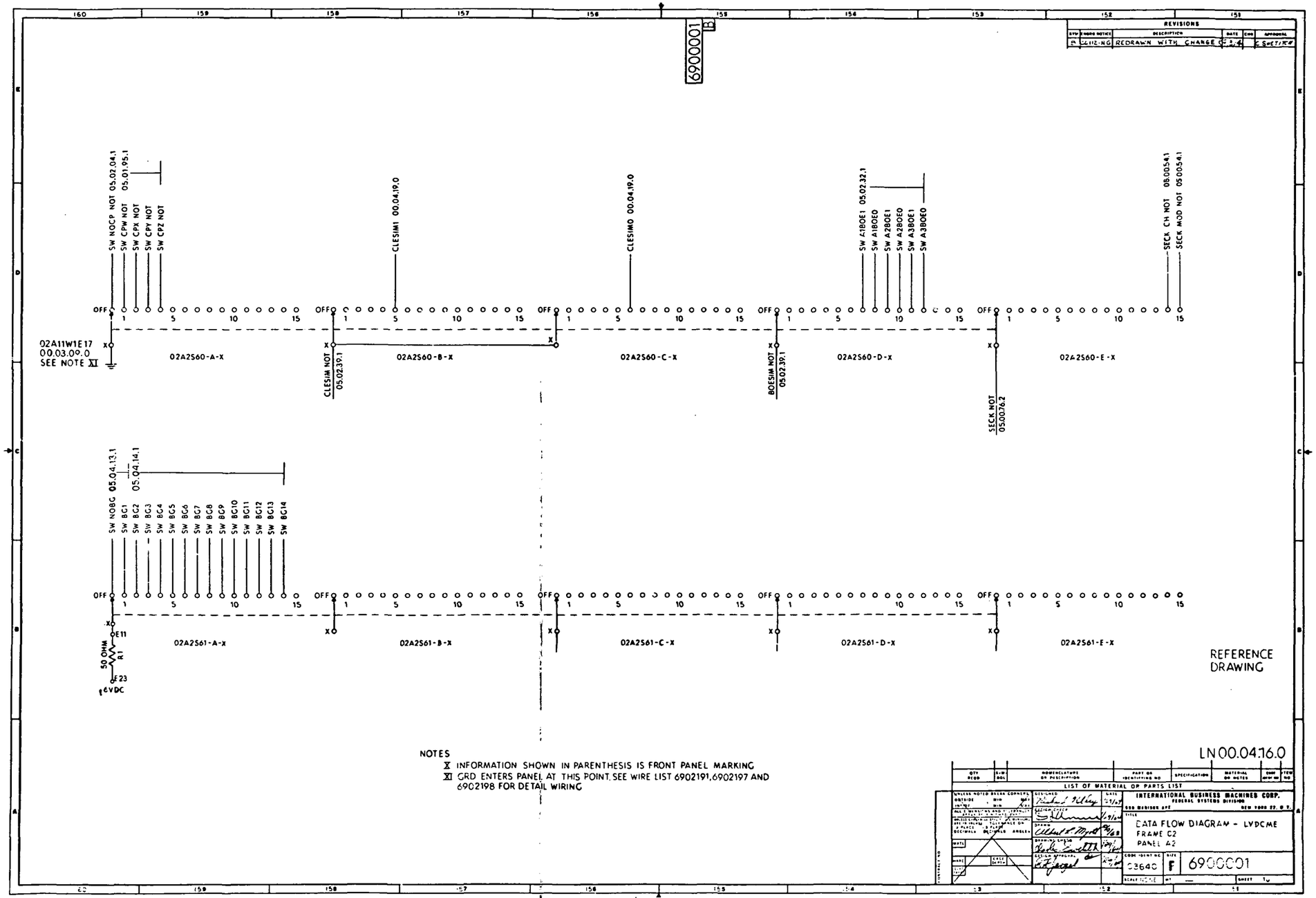


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 5)

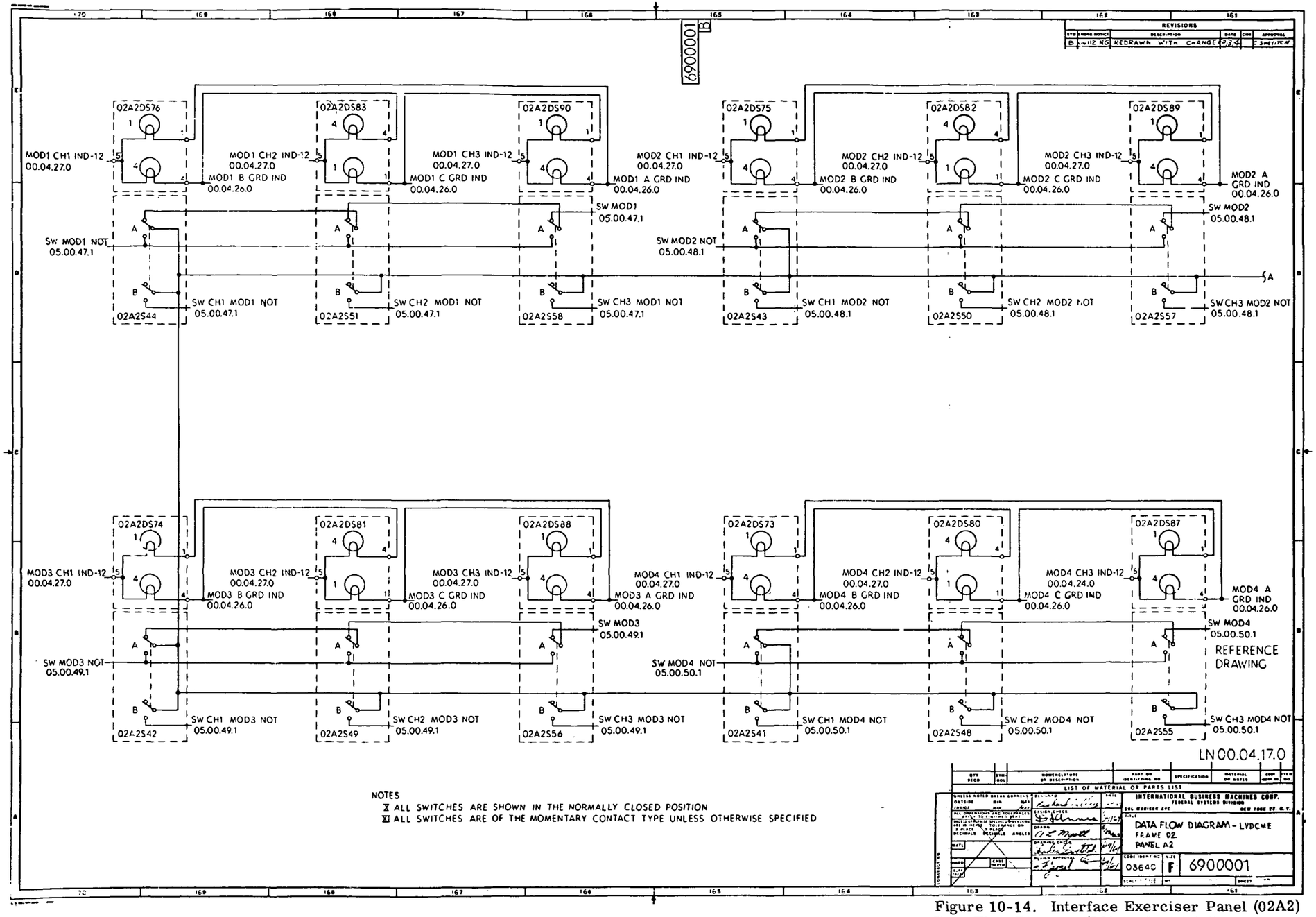


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 6)

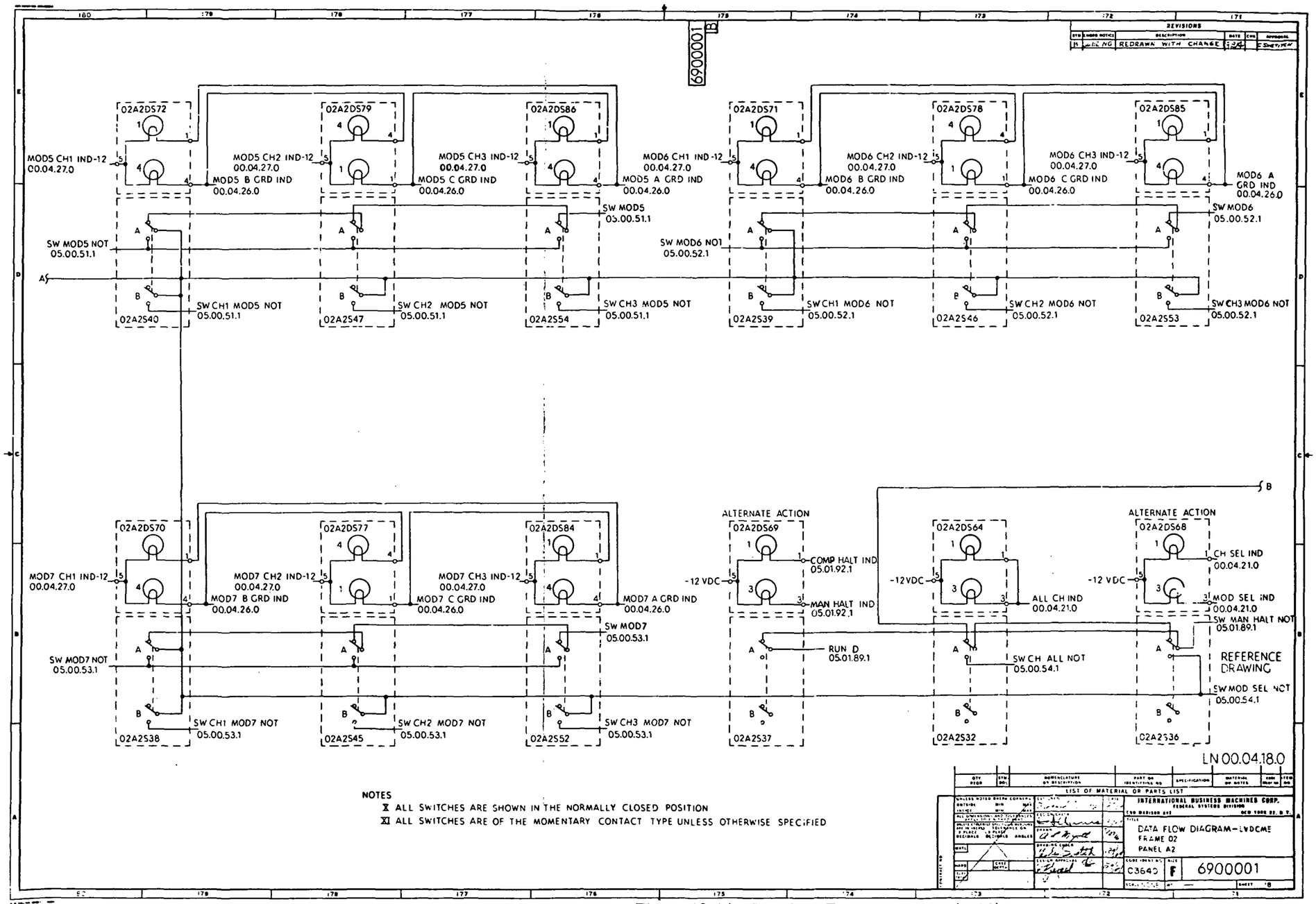
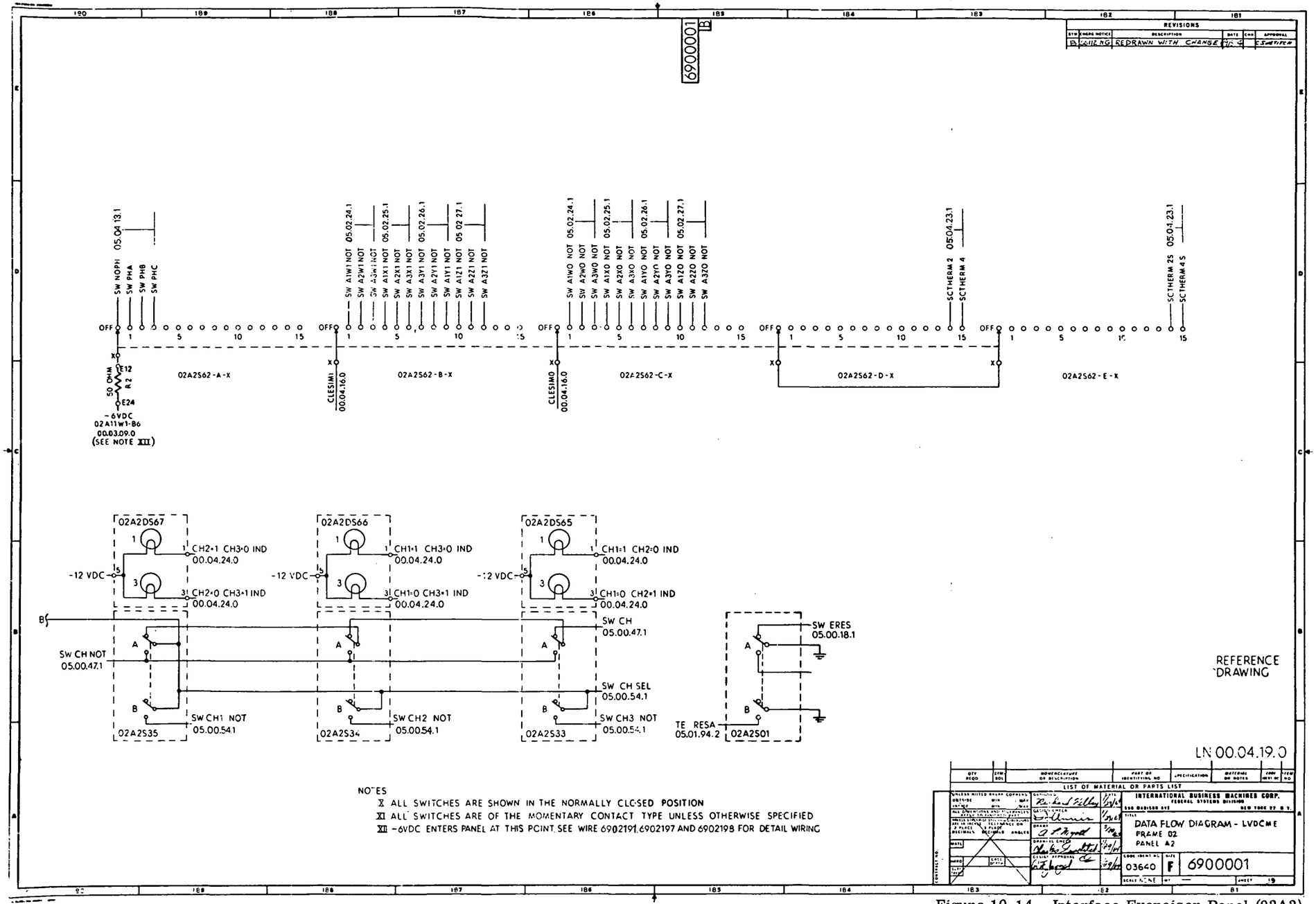


Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 7)



NOTES

X ALL SWITCHES ARE SHOWN IN THE NORMALLY CLOSED POSITION

XI ALL SWITCHES ARE OF THE MOMENTARY CONTACT TYPE UNLESS OTHERWISE SPECIFIED

XII -6VDC ENTERS PANEL AT THIS POINT. SEE WIRE 6902191,6902197 AND 6902198 FOR DETAIL WIRING

Figure 10-14. Interface Exerciser Panel (02A2) Data Flow Diagram (LN 00.04.12.0 through LN 00.04.19.0) (Sheet 8)

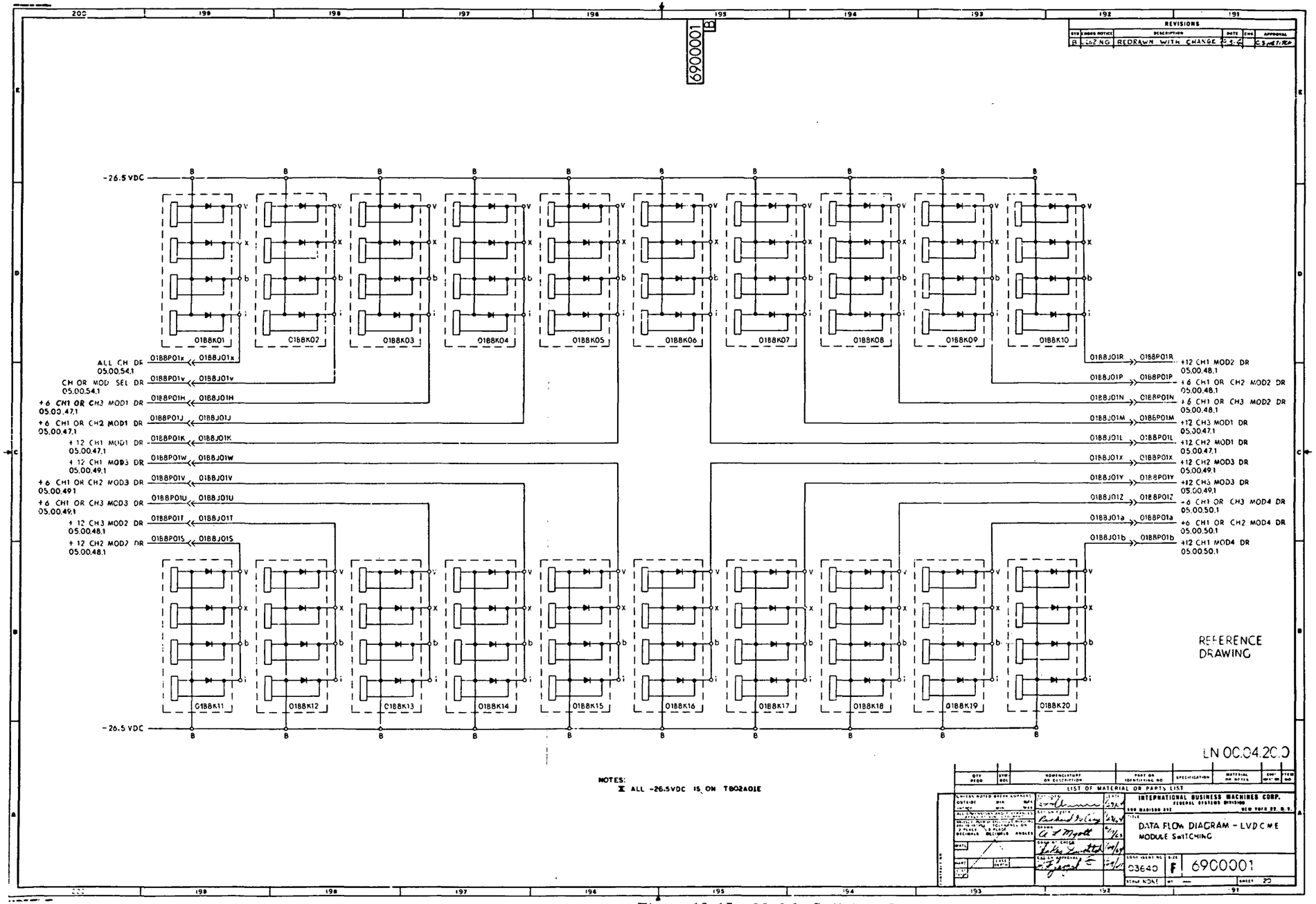


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 1 of 8)

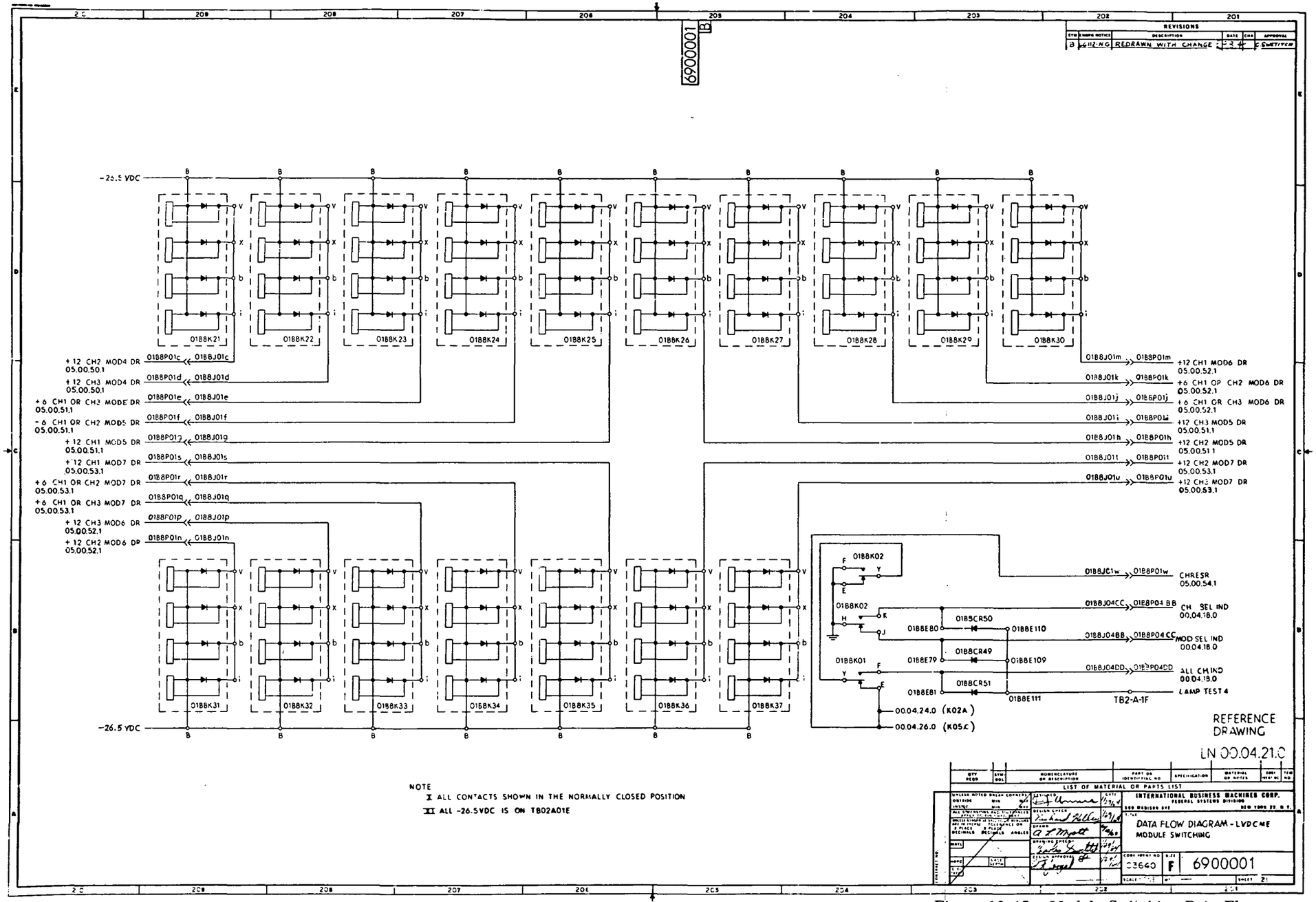


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 2)

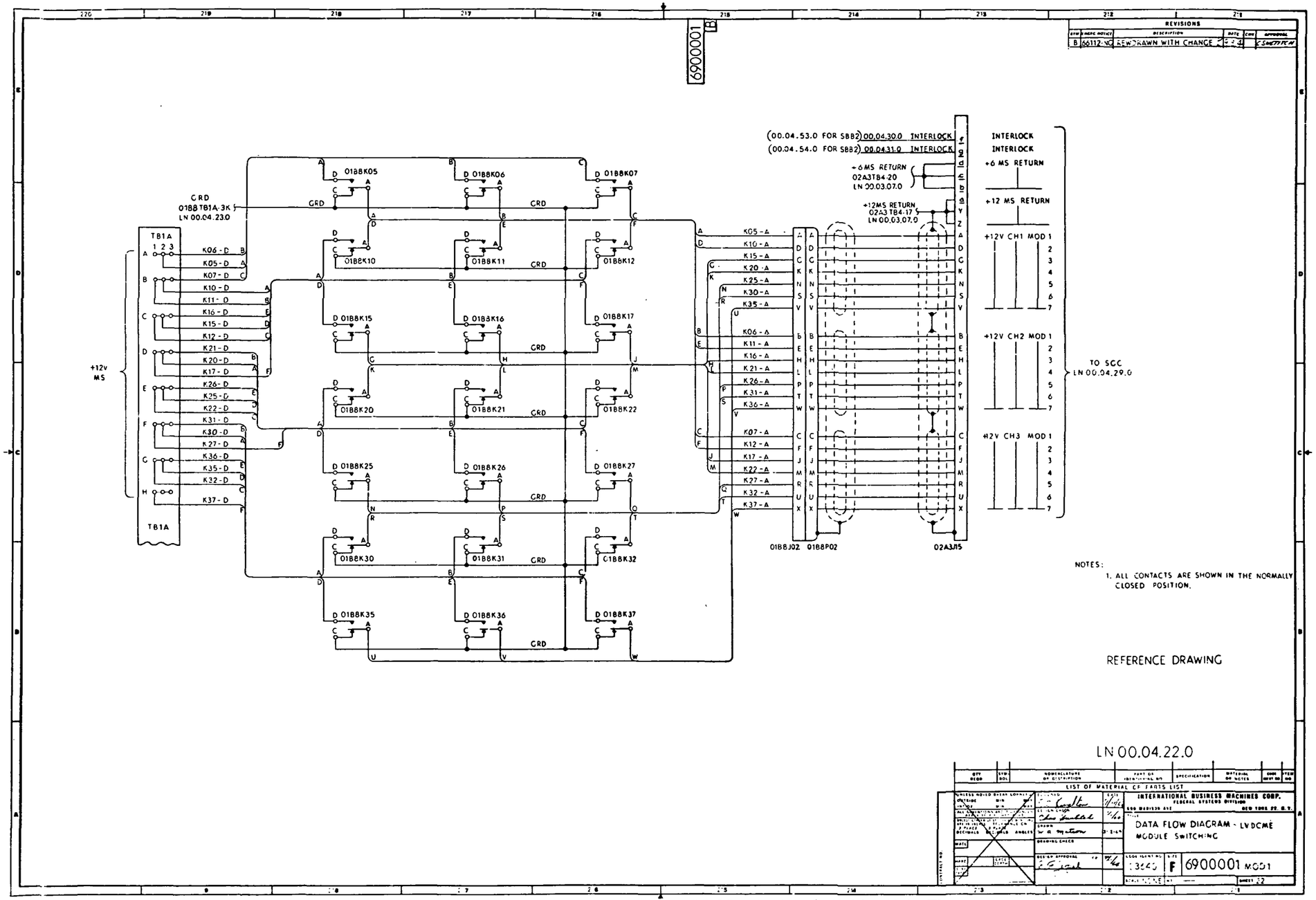


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 3)

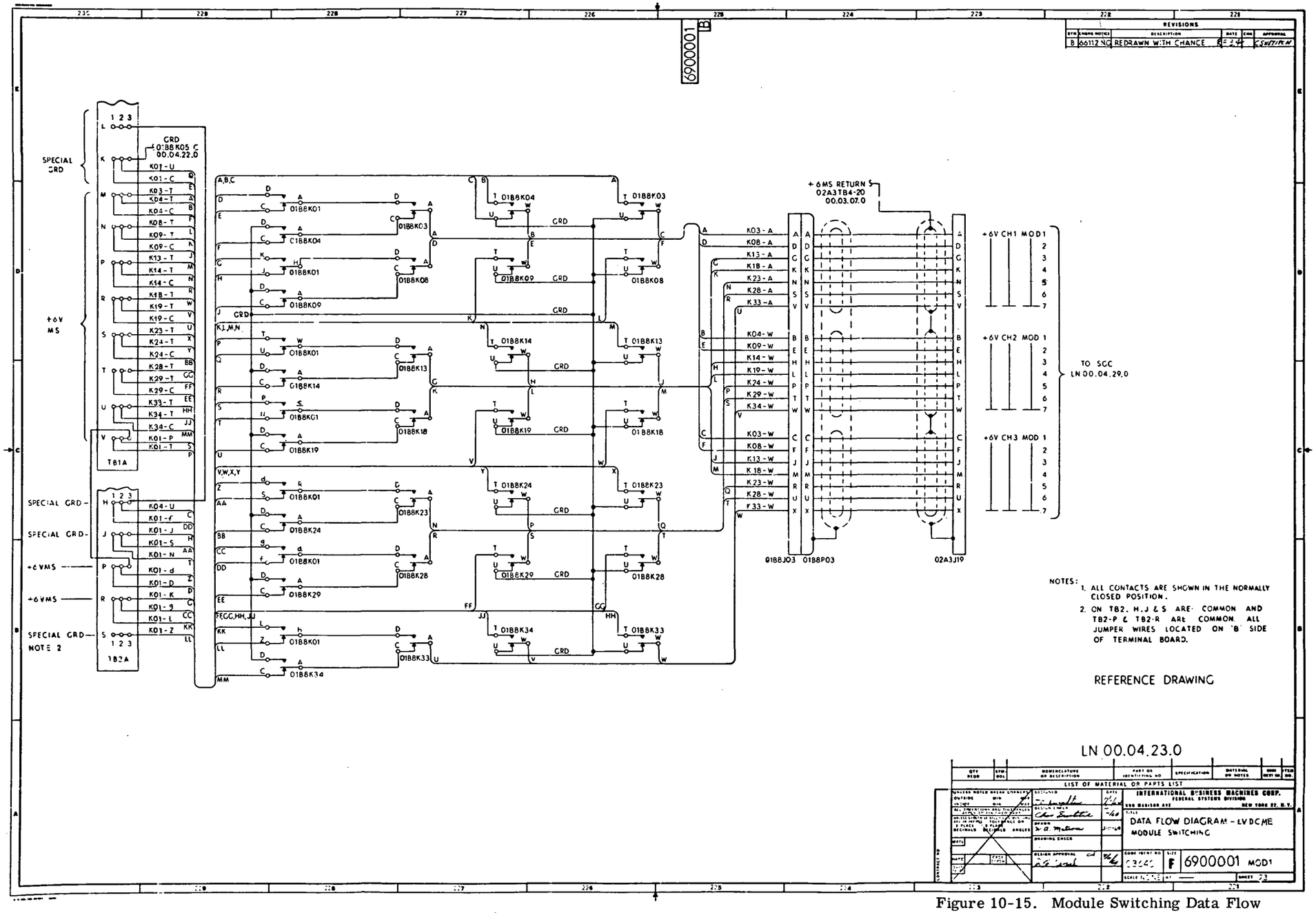


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 4)

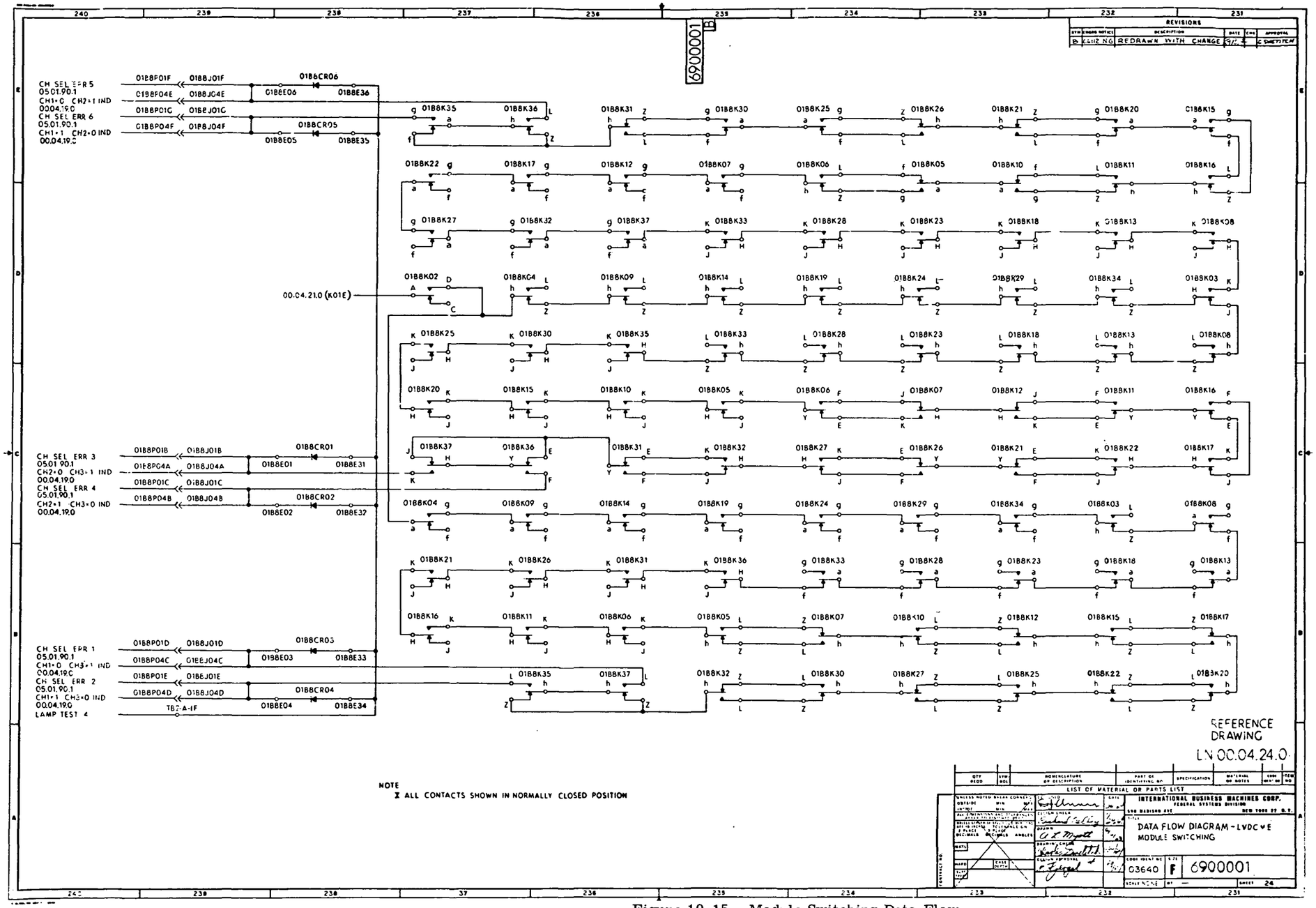
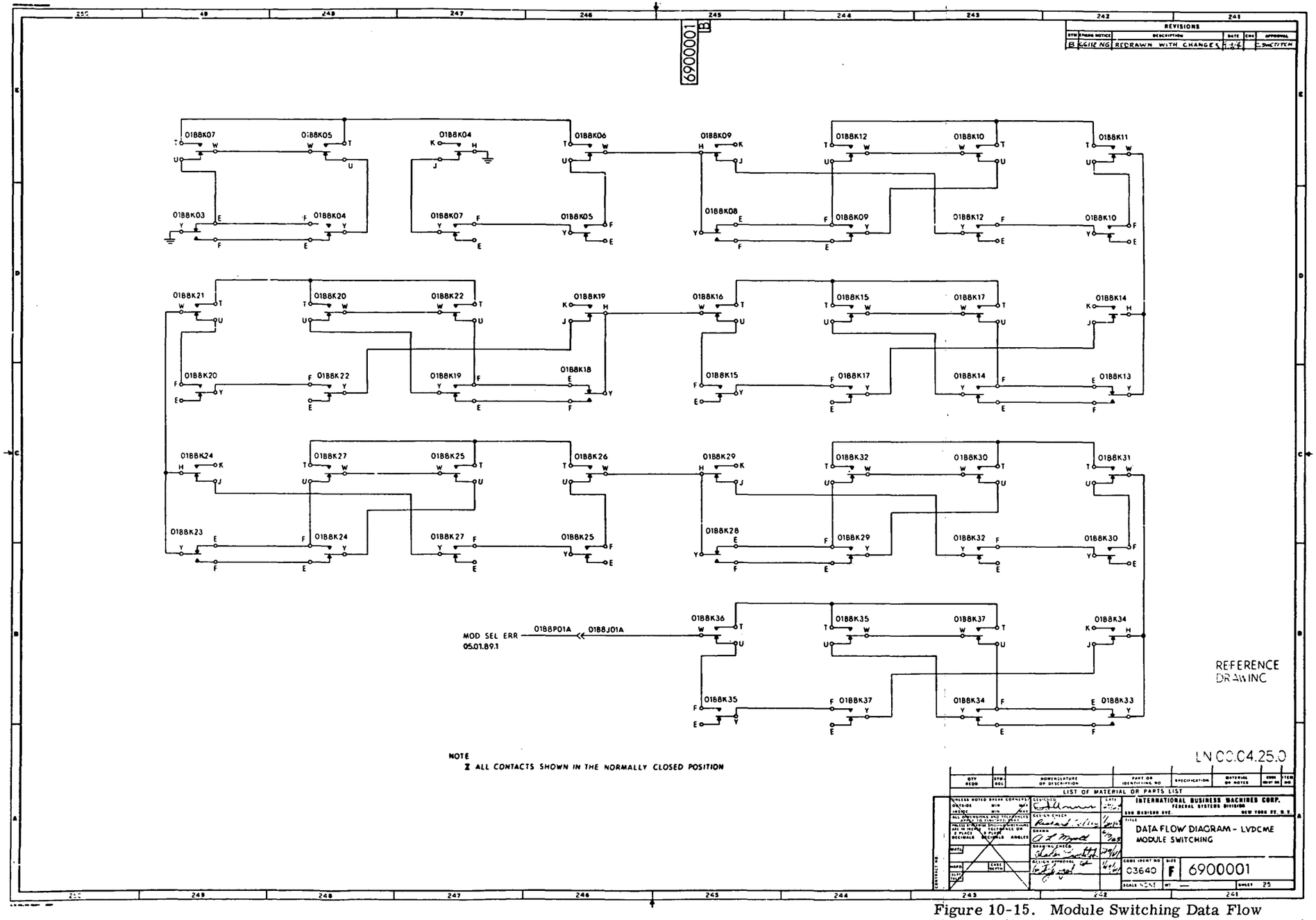


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 5)



NOTE
Σ ALL CONTACTS SHOWN IN THE NORMALLY CLOSED POSITION

REFERENCE
DRAWING

Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 6)

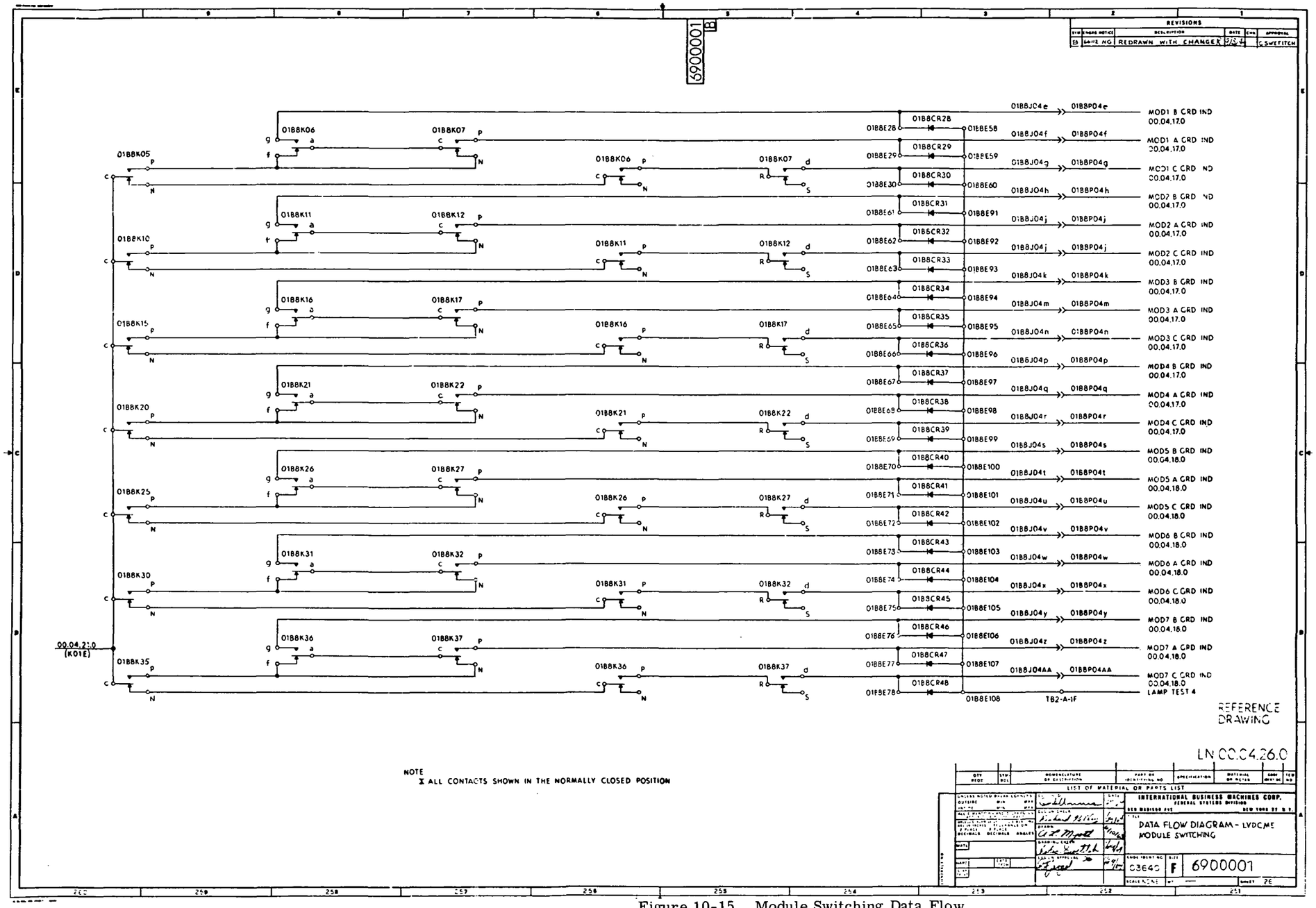


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 7)

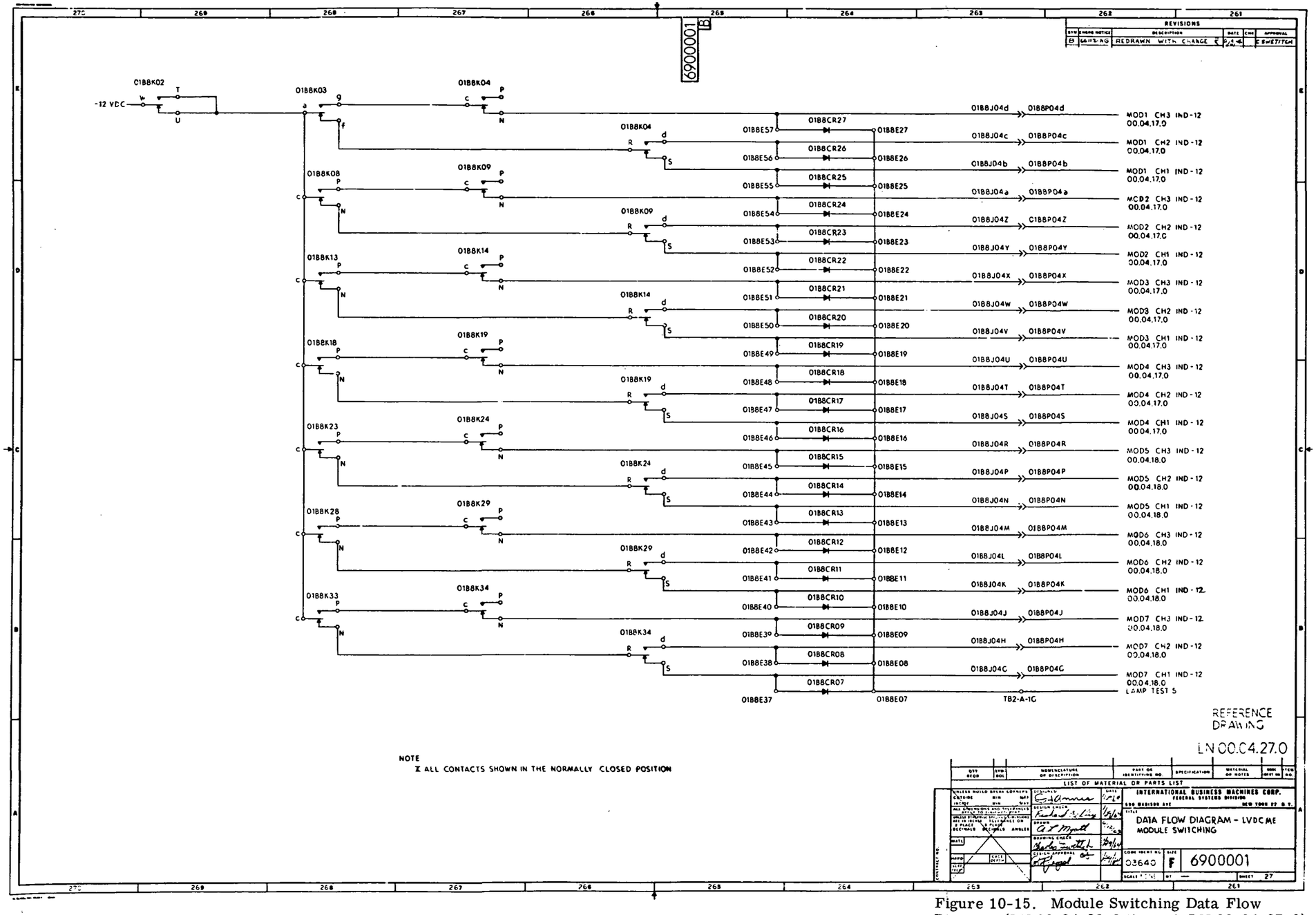


Figure 10-15. Module Switching Data Flow Diagram (LN 00.04.20.0 through LN 00.04.27.0) (Sheet 8)

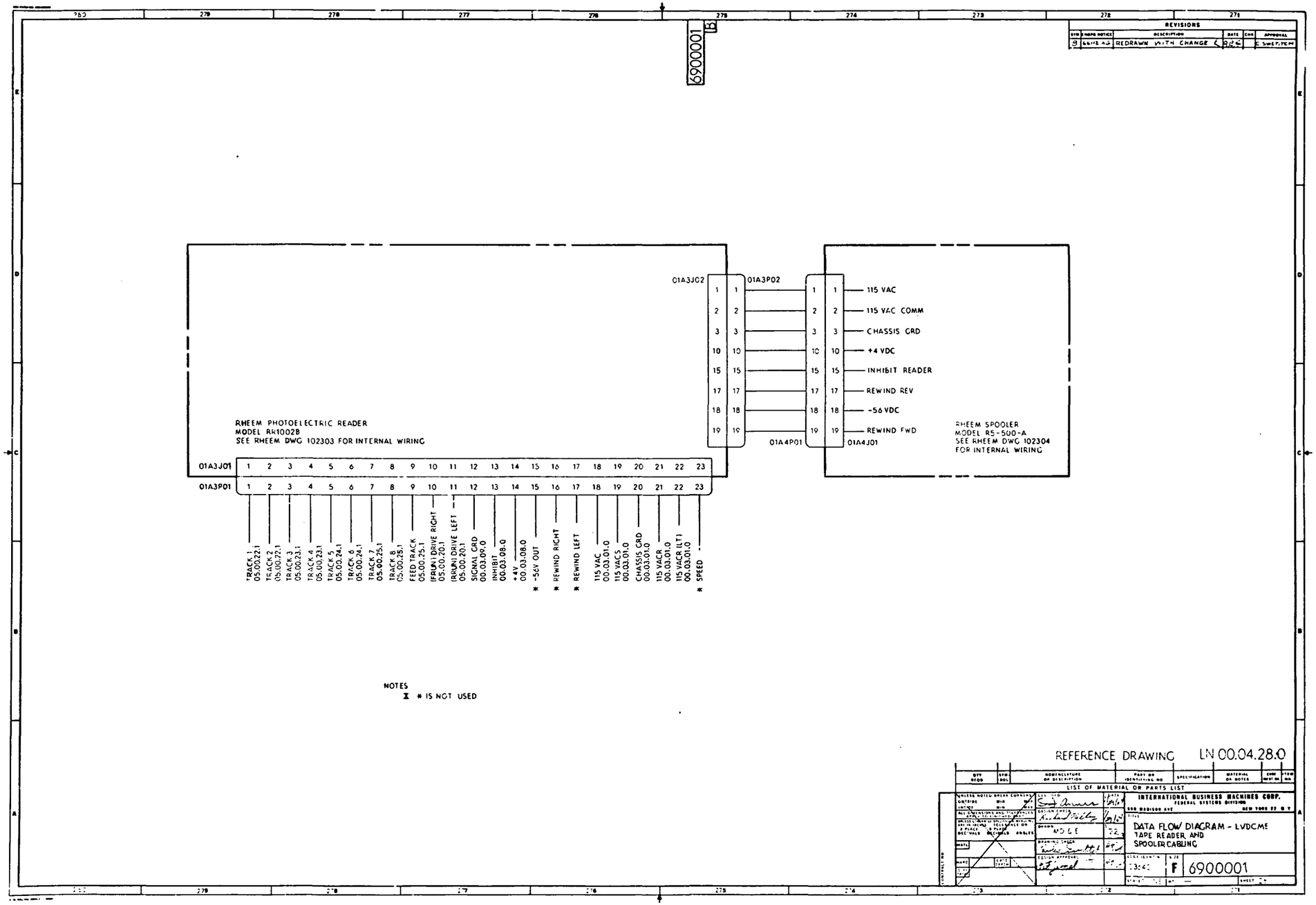


Figure 10-16. Tape Reader and Tape Spooler Cabling Data Flow Diagram (LN 00.04.28.0)

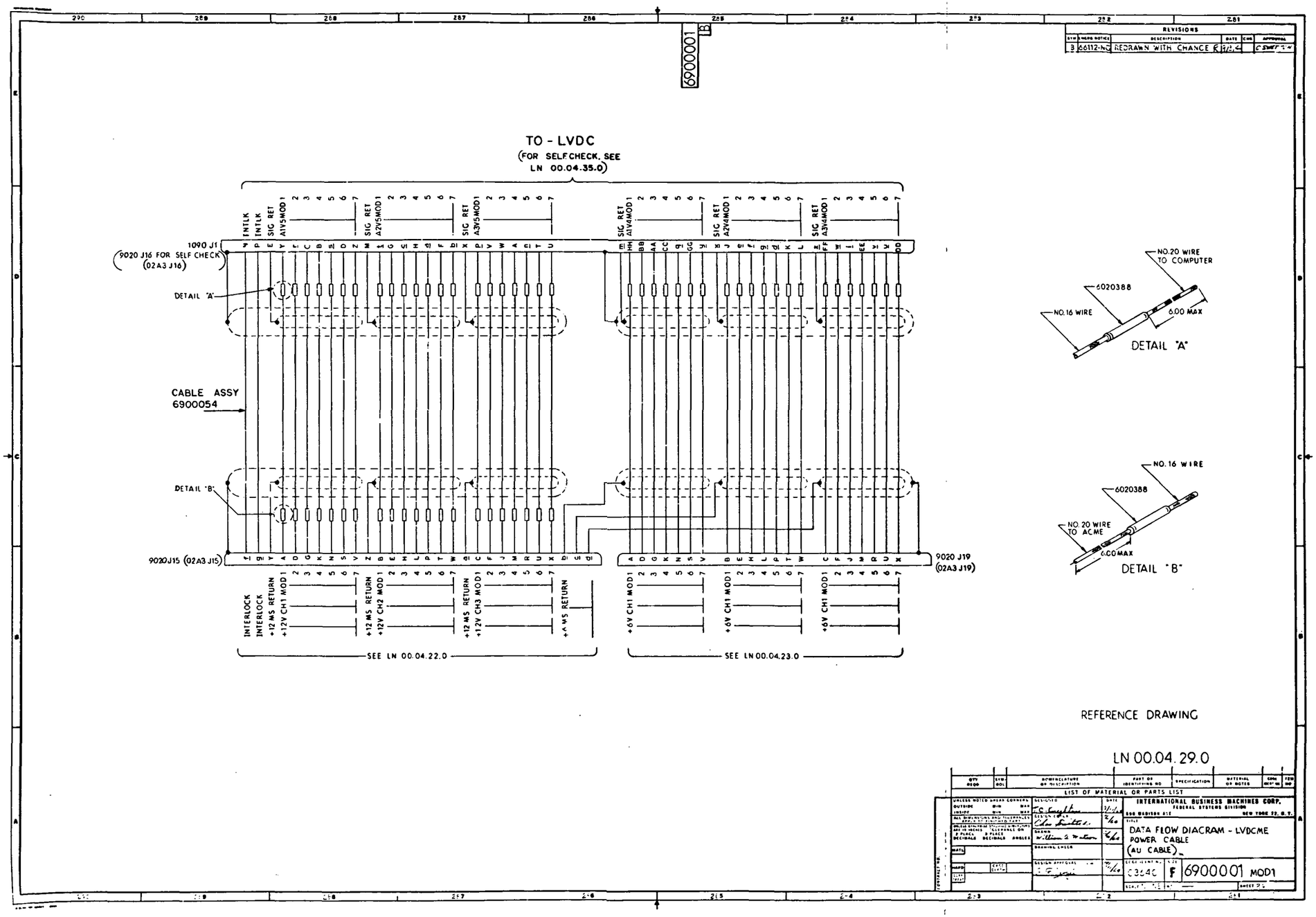


Figure 10-17. Power Cable (AU Cable) Data Flow Diagram (LN 00.04.29.0)

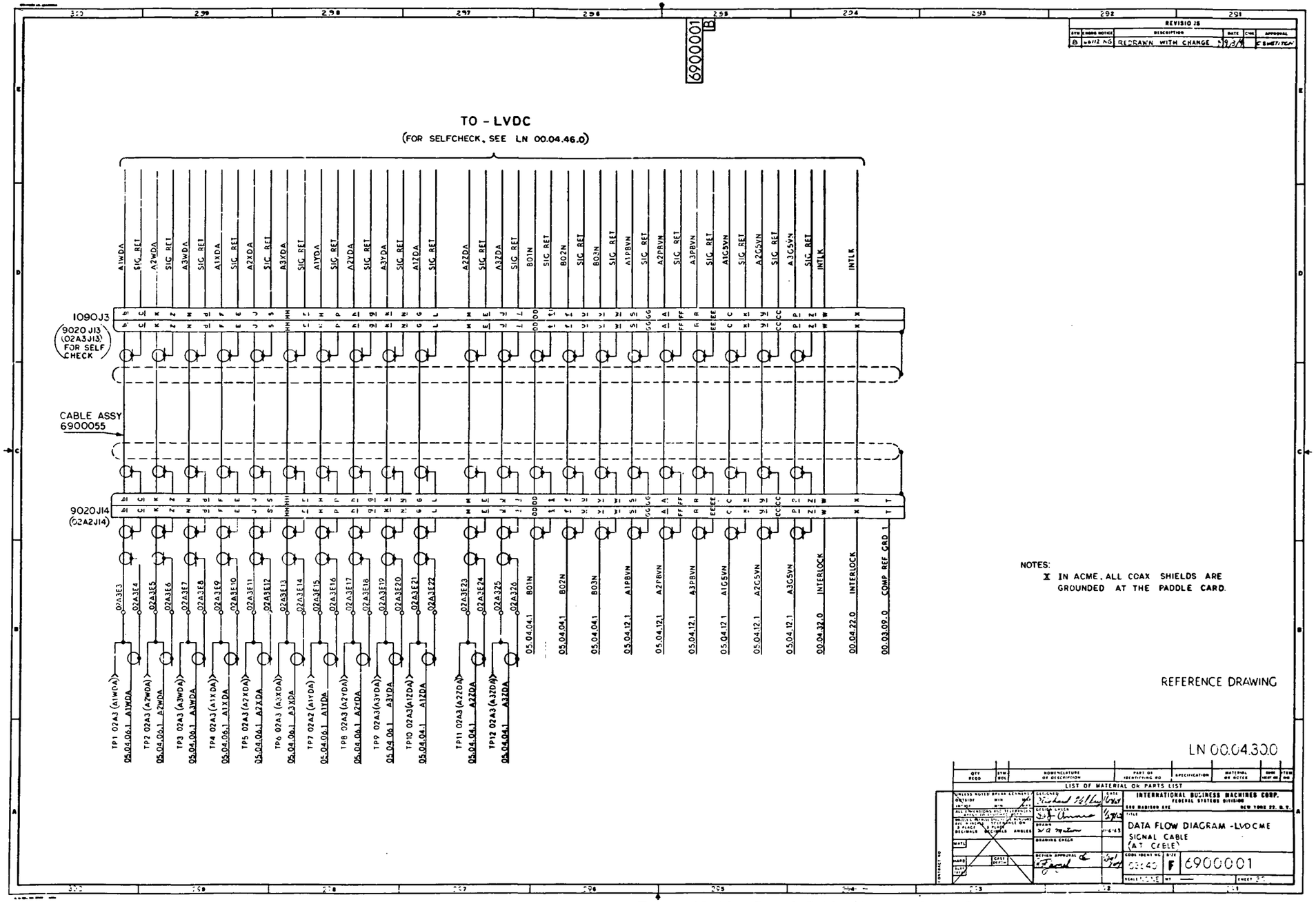


Figure 10-18. Signal Cable (AT, N, AR, AS and AM Cables) Data Flow Diagram (LN 00.04.30.0 through LN 00.04.34.0) (Sheet 1 of 5)

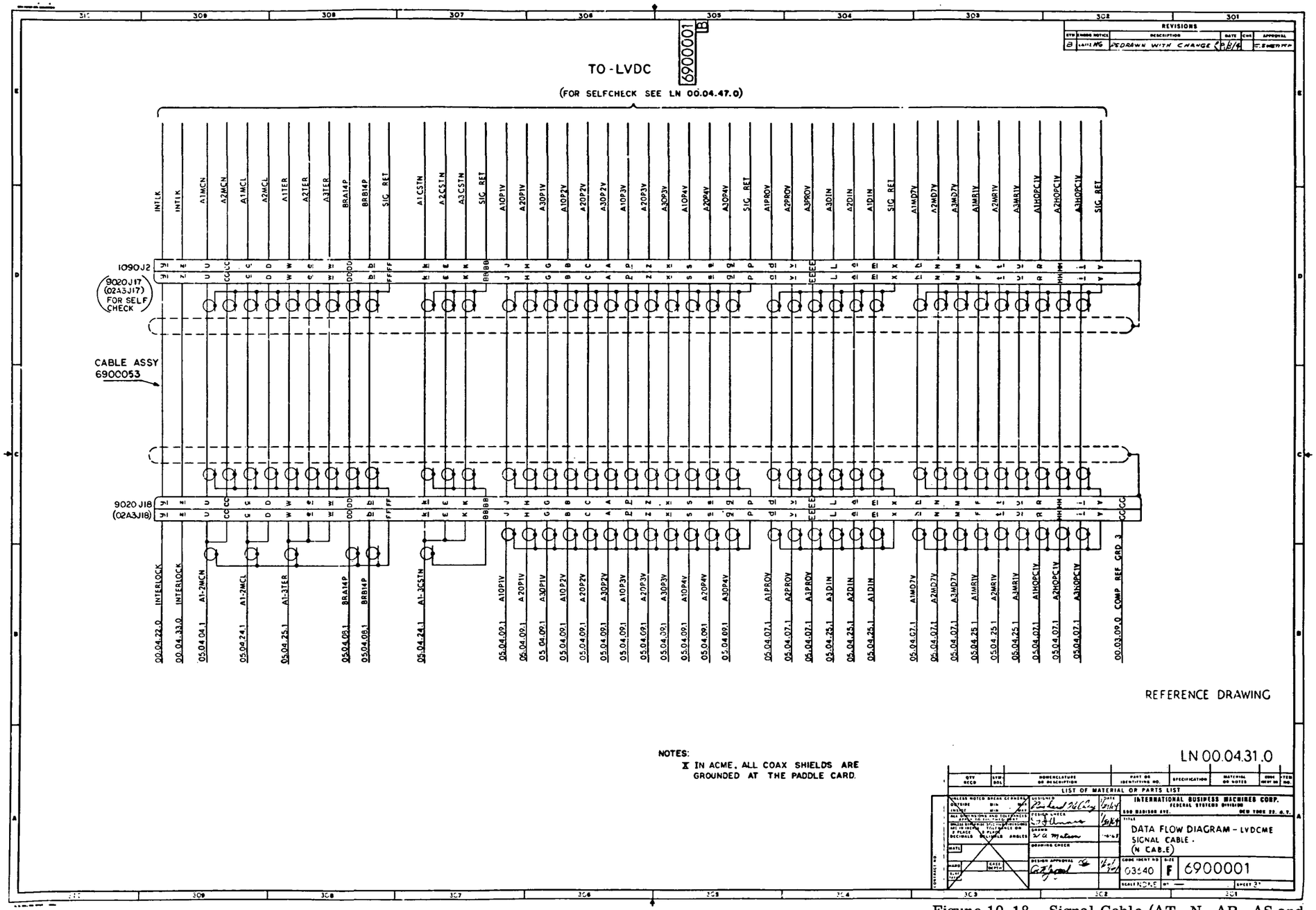


Figure 10-18. Signal Cable (AT, N, AR, AS and AM Cables) Data Flow Diagram (LN 00.04.30.0 through LN 00.04.34.0) (Sheet 2)

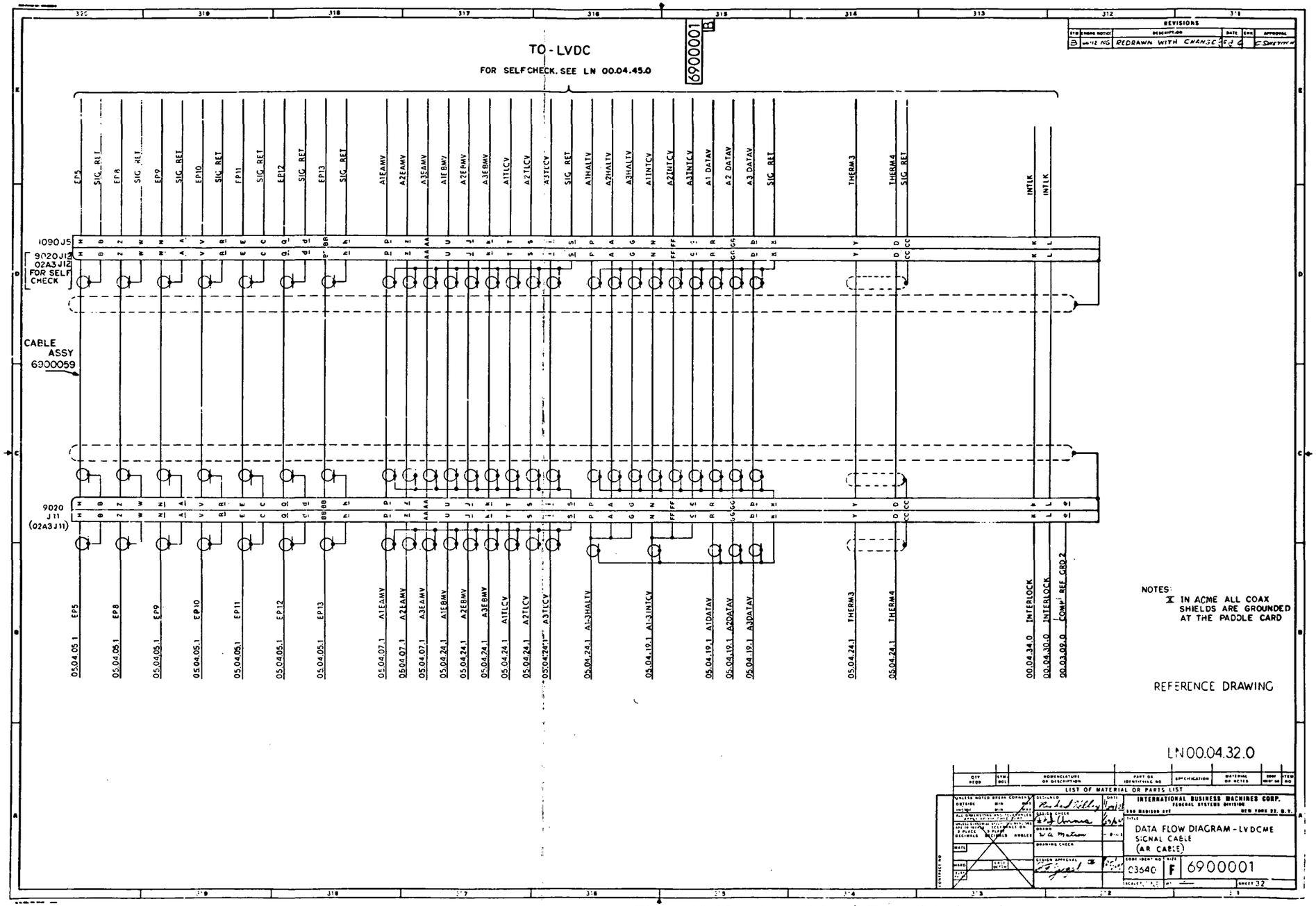


Figure 10-18. Signal Cable (AT, N, AR, AS and AM Cables) Data Flow Diagram (LN 00.04.30.0 through LN 00.04.34.0) (Sheet 3)

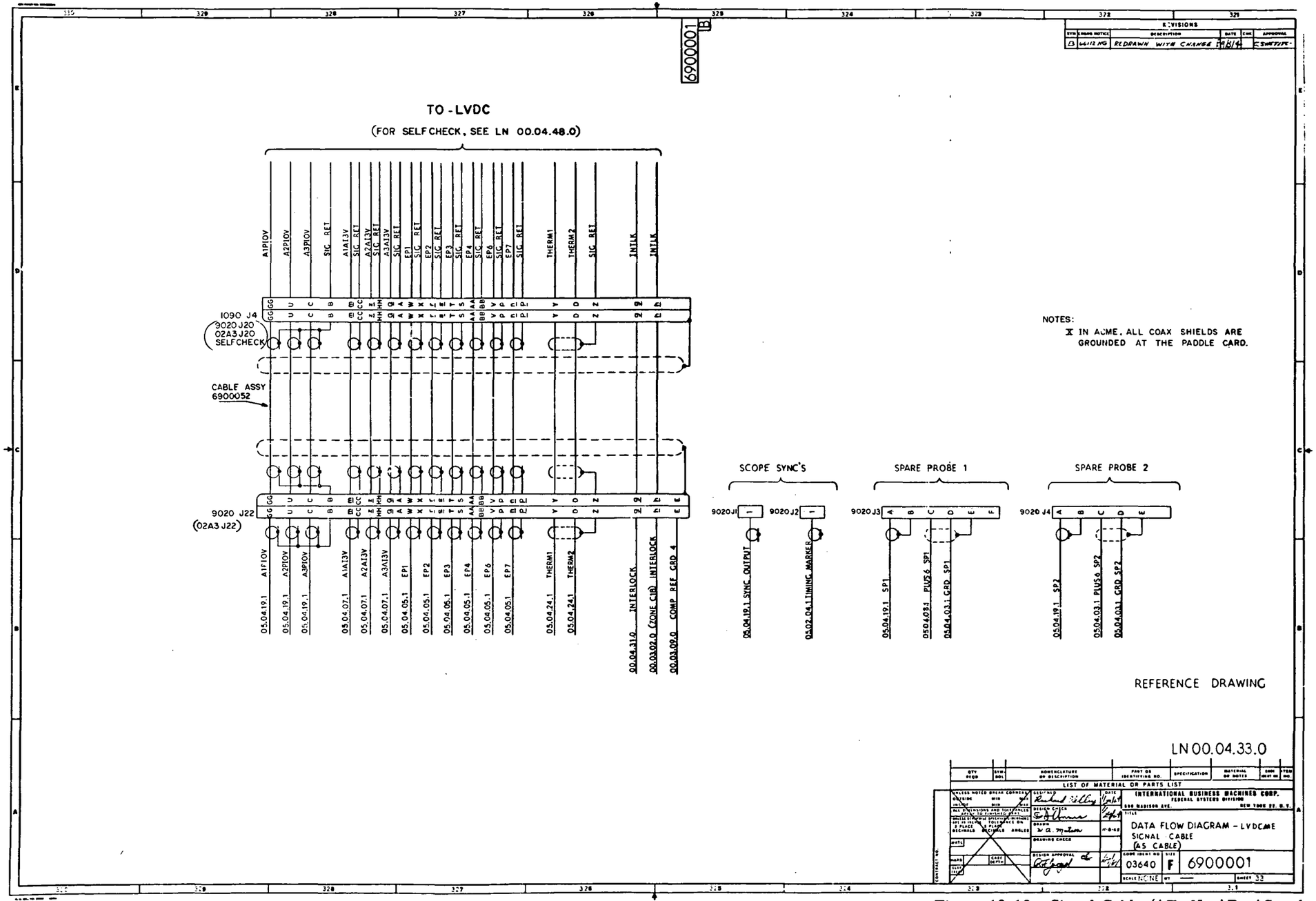


Figure 10-18. Signal Cable (AT, N, AR, AS and AM Cables) Data Flow Diagram (LN 00.04.30.0 through LN 00.04.34.0) (Sheet 4)

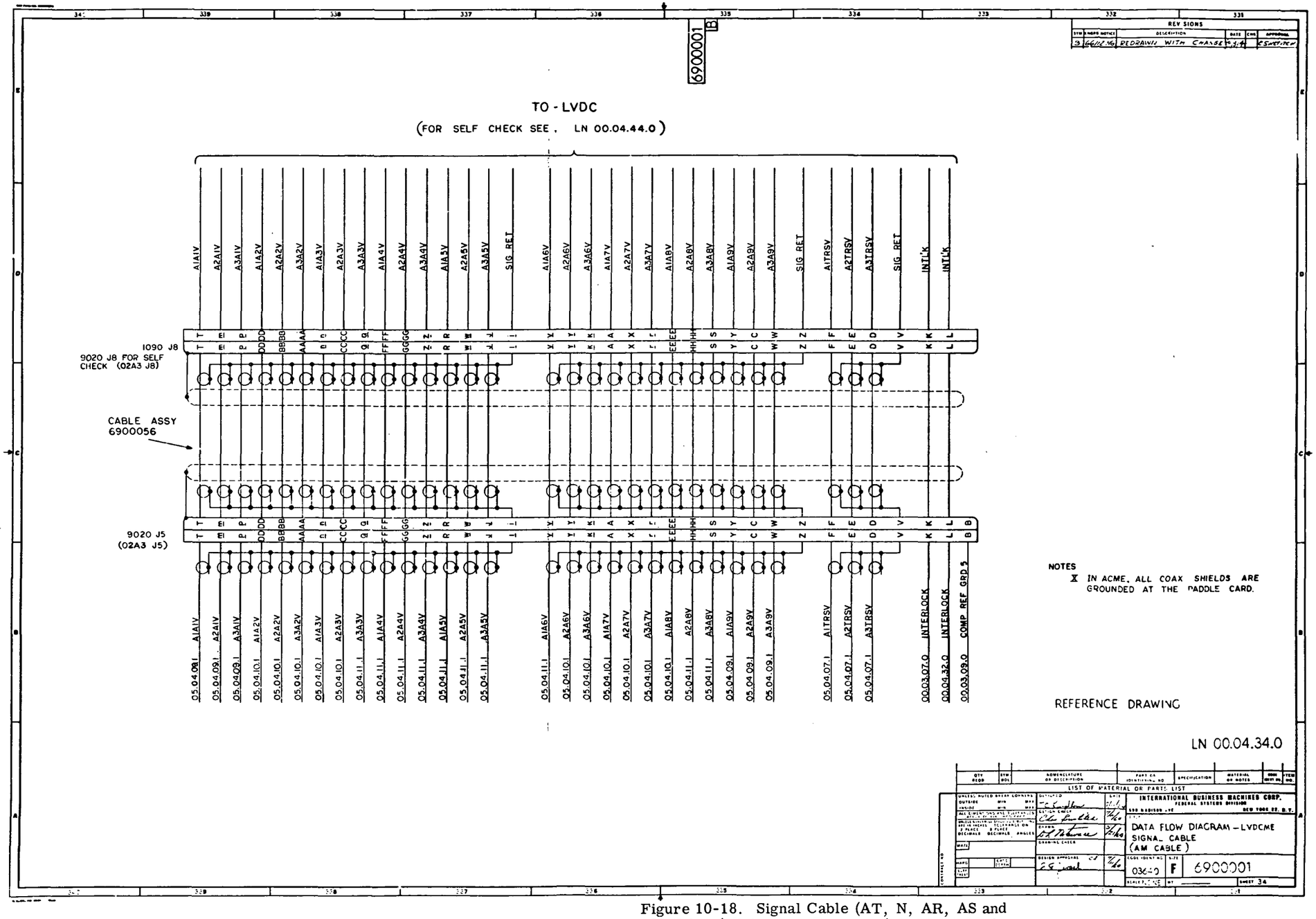


Figure 10-18. Signal Cable (AT, N, AR, AS and AM Cables) Data Flow Diagram (LN 00.04.30.0 through LN 00.04.34.0) (Sheet 5)

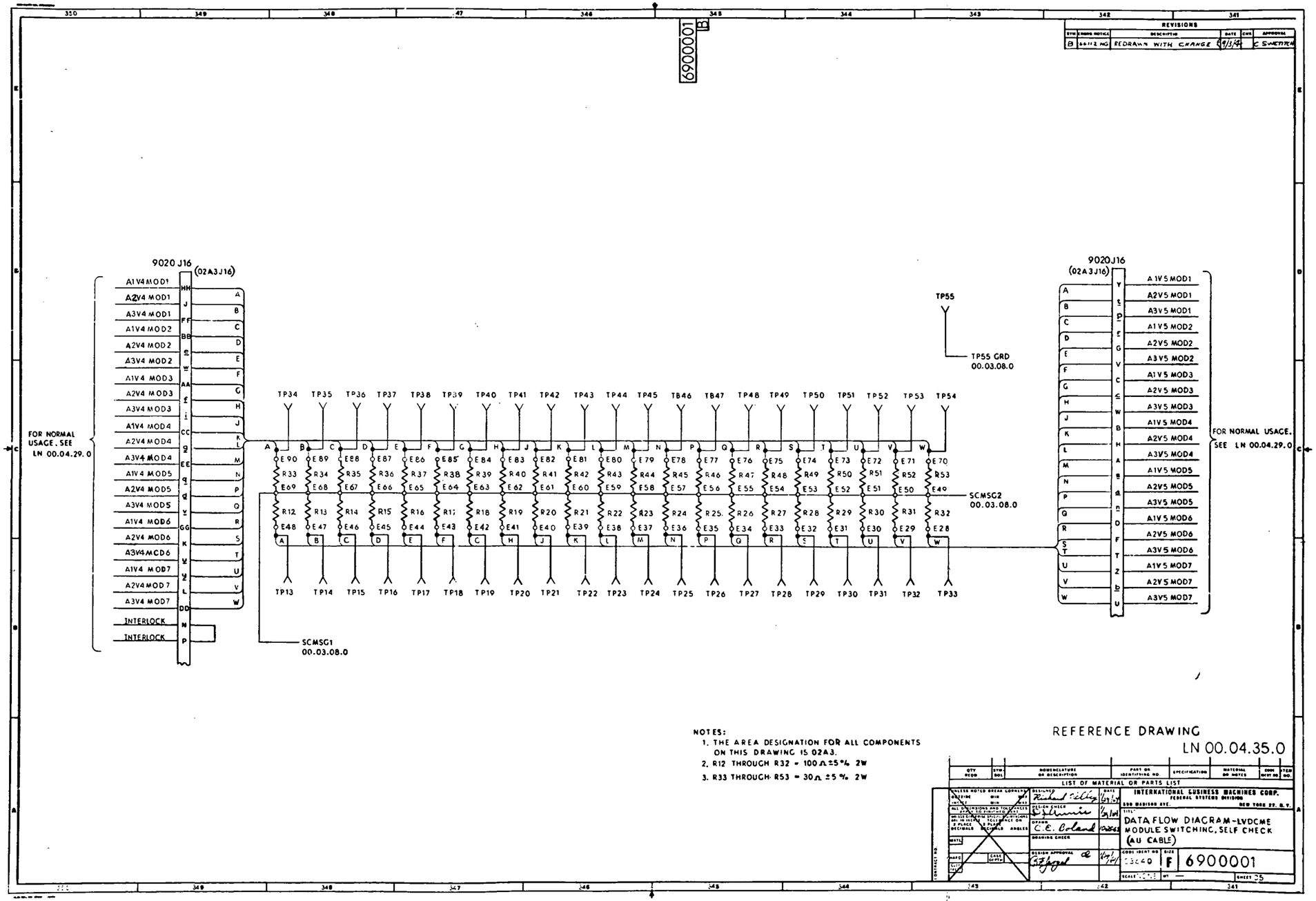


Figure 10-19. Module Switching, Self Check (AU Cable) Data Flow Diagram (LN 00.04.35.0)

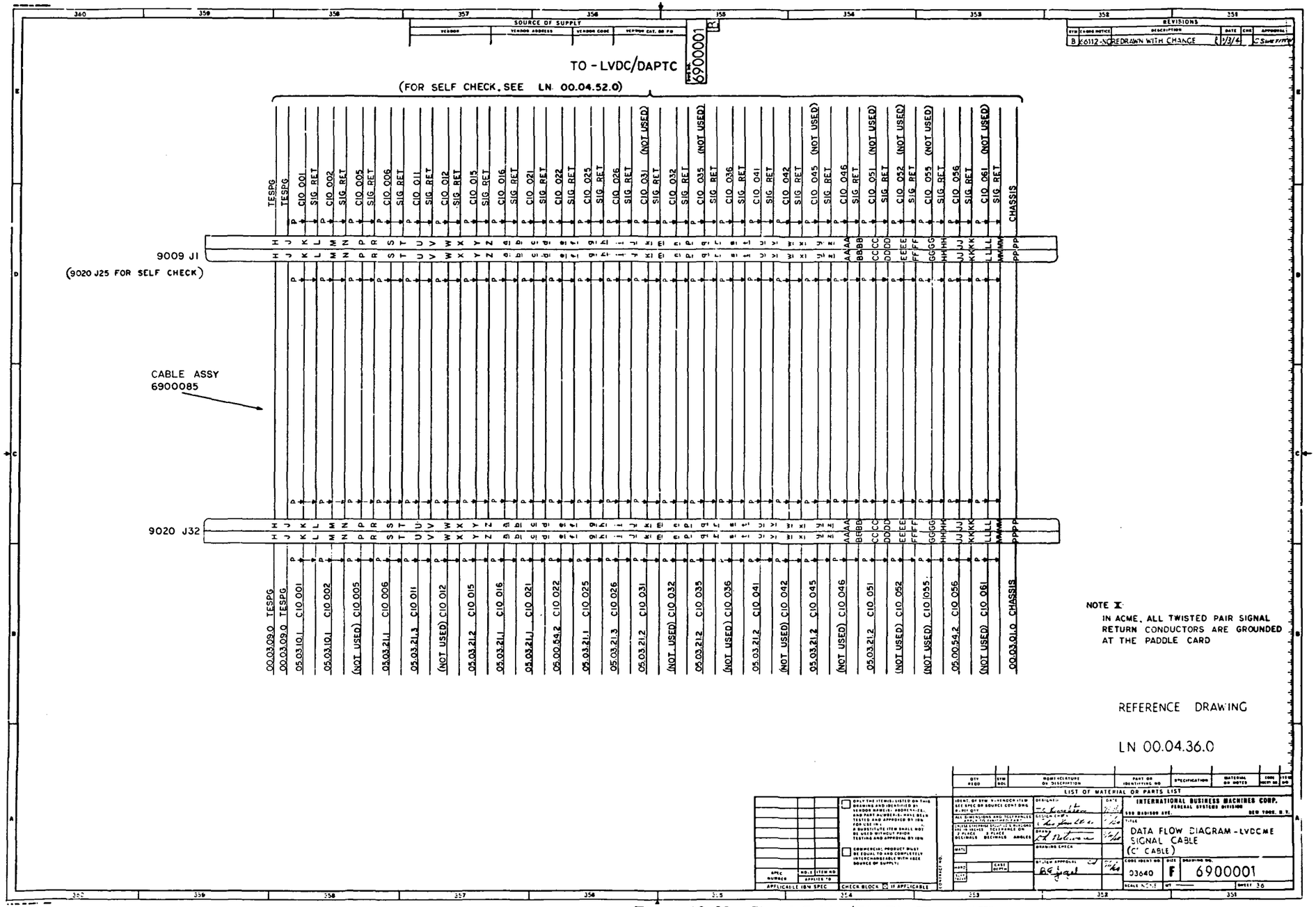


Figure 10-20. Signal Cable (C', D', E' and AW Cables) Data Flow Diagram (LN 00.04.36.0 through LN 00.04.39.0) (Sheet 1 of 4)

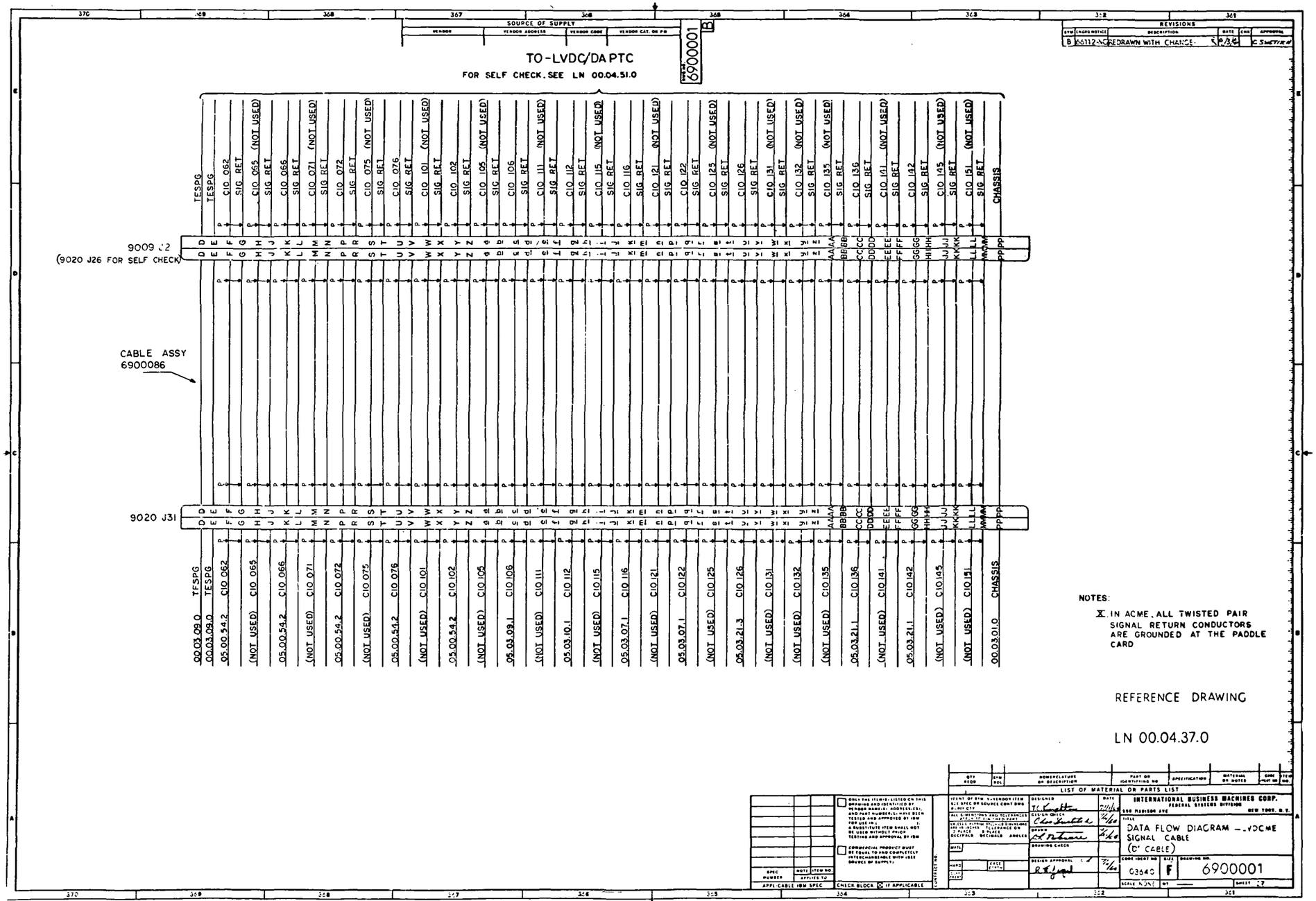


Figure 10-20. Signal Cable (C', D', E' and AW Cables) Data Flow Diagram (LN 00.04.36.0 through LN 00.04.39.0) (Sheet 2)

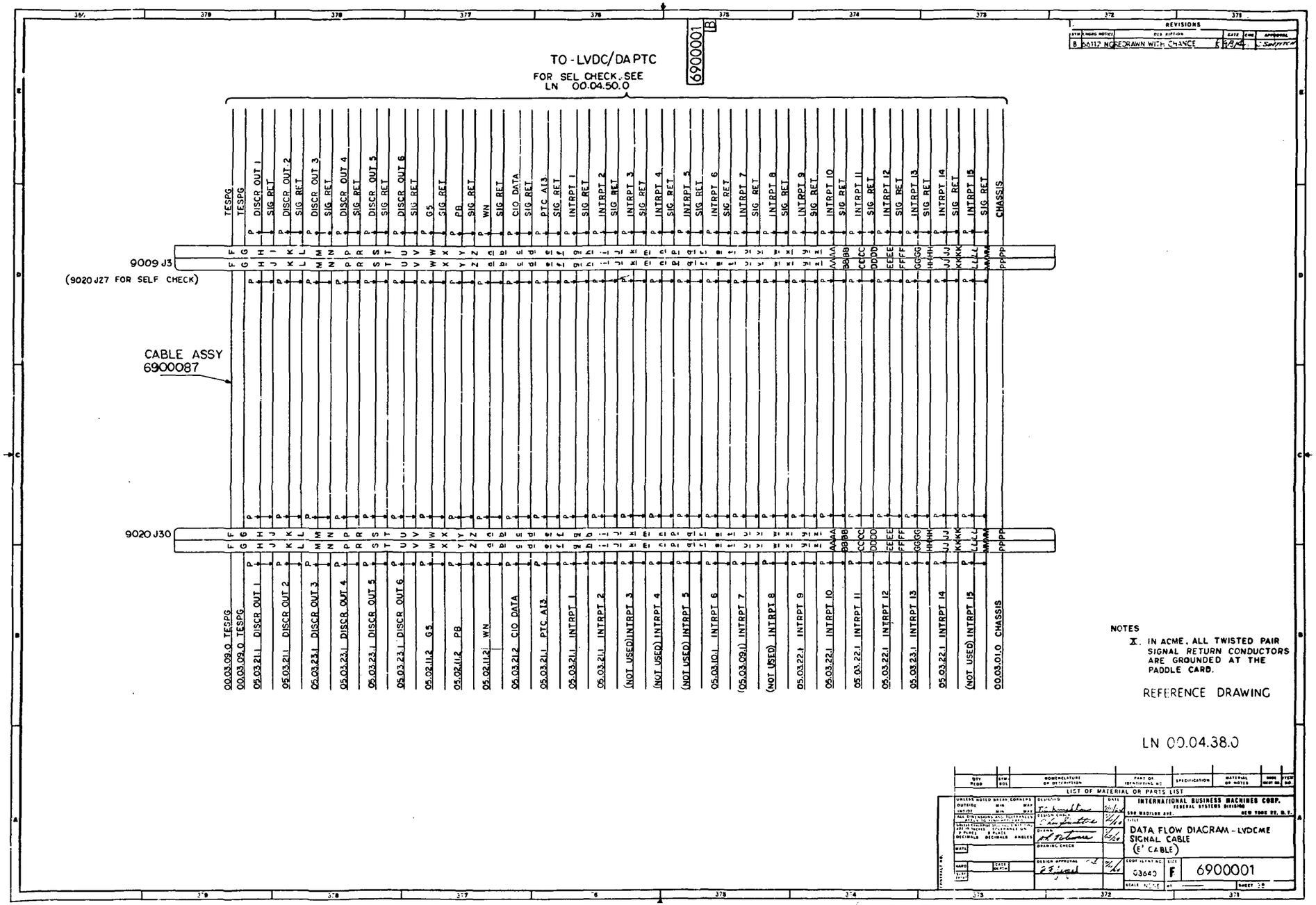


Figure 10-20. Signal Cable (C', D', E' and AW Cables) Data Flow Diagram (LN 00.04.36.0 through LN 00.04.39.0) (Sheet 3)

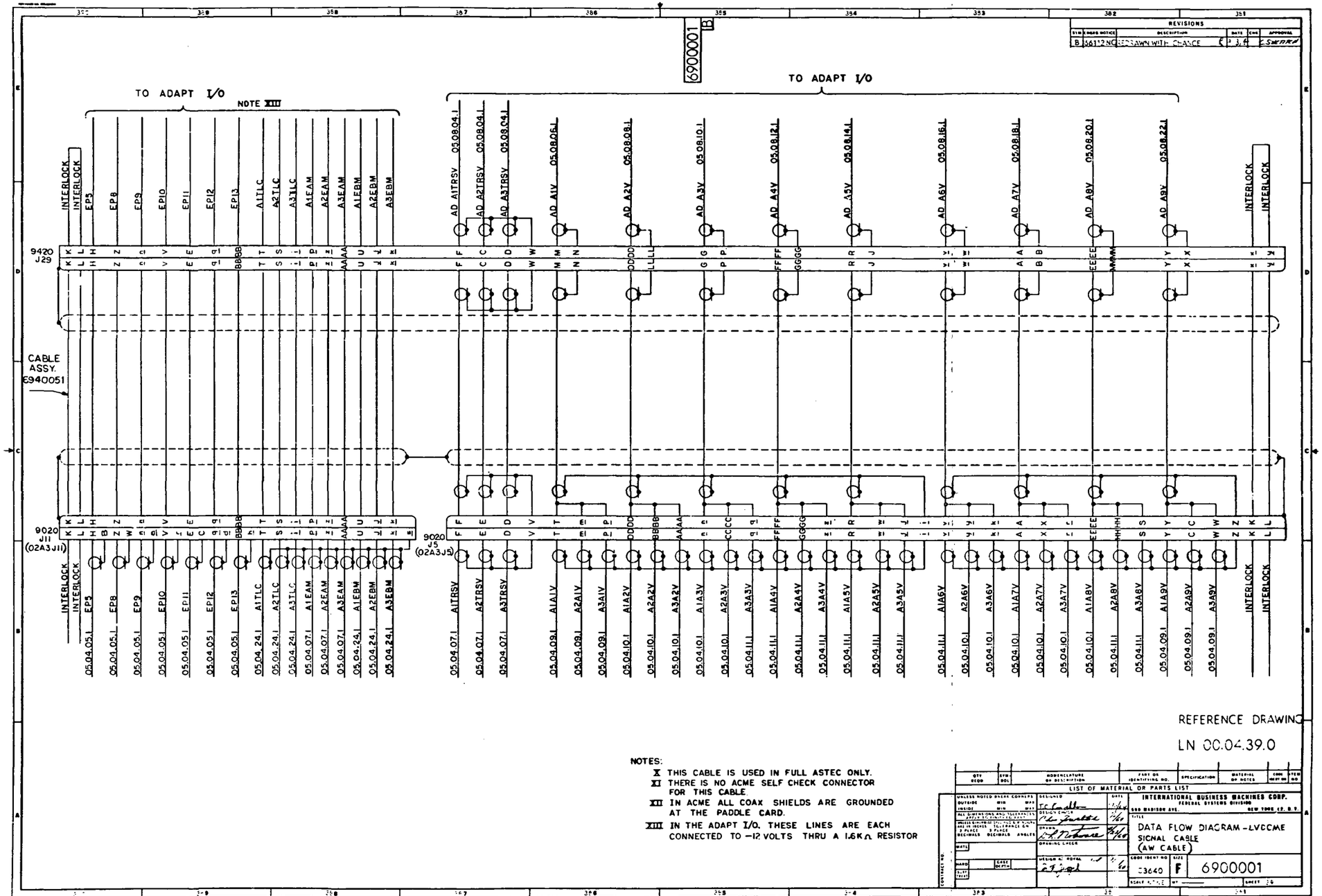


Figure 10-20. Signal Cable (C', D', E' and AW Cables) Data Flow Diagram (LN 00.04.36.0 through LN 00.04.39.0) (Sheet 4)

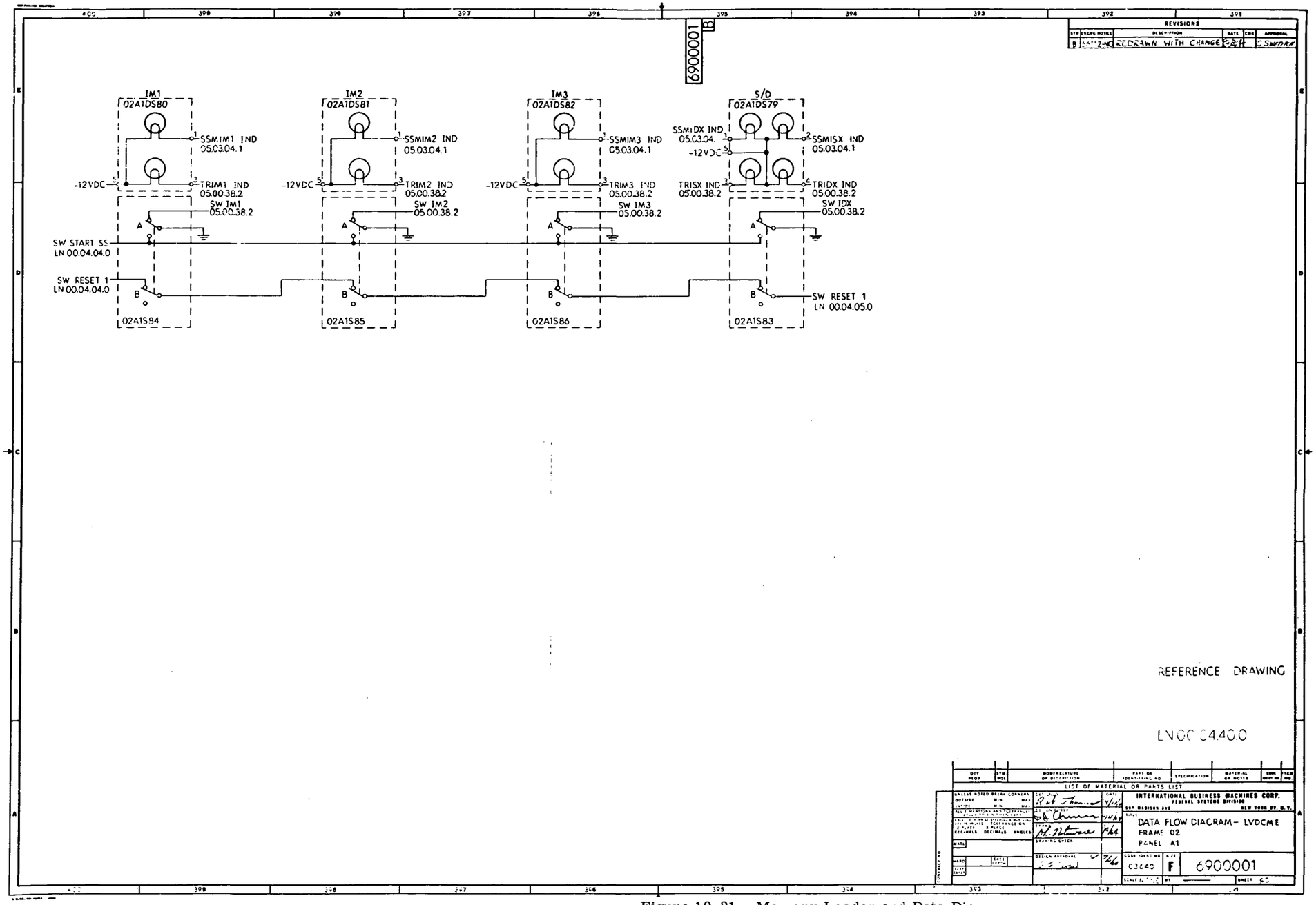


Figure 10-21. Memory Loader and Data Display Panel (02A1, Pushbutton/lamps IM1, IM2, IM3 and S/D) Data Flow Diagram (LN 00.04.40.0)

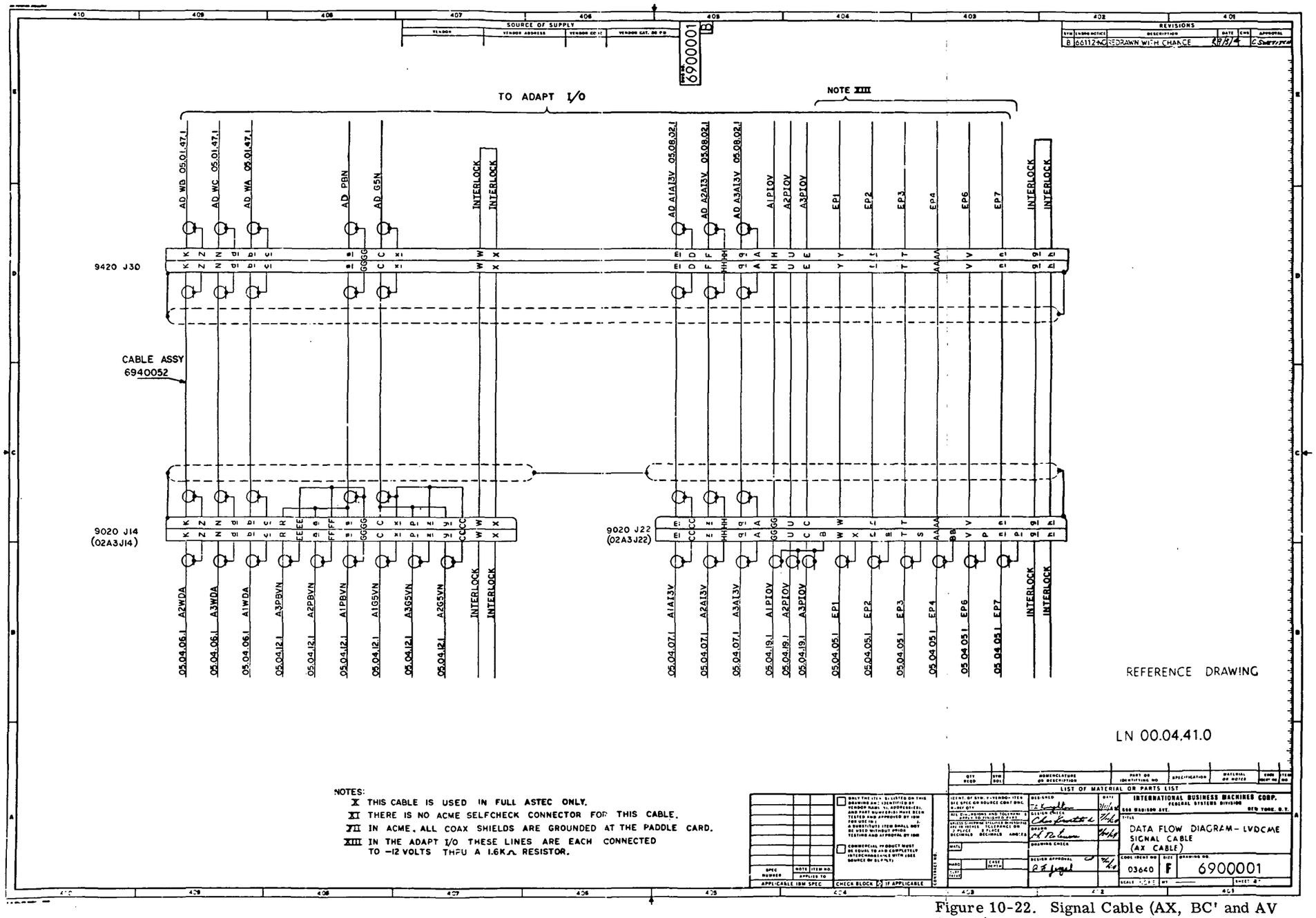


Figure 10-22. Signal Cable (AX, BC' and AV Cables) Data Flow Diagram (LN 00.04.41.0 through LN 00.04.43.0) (Sheet 1 of 3)

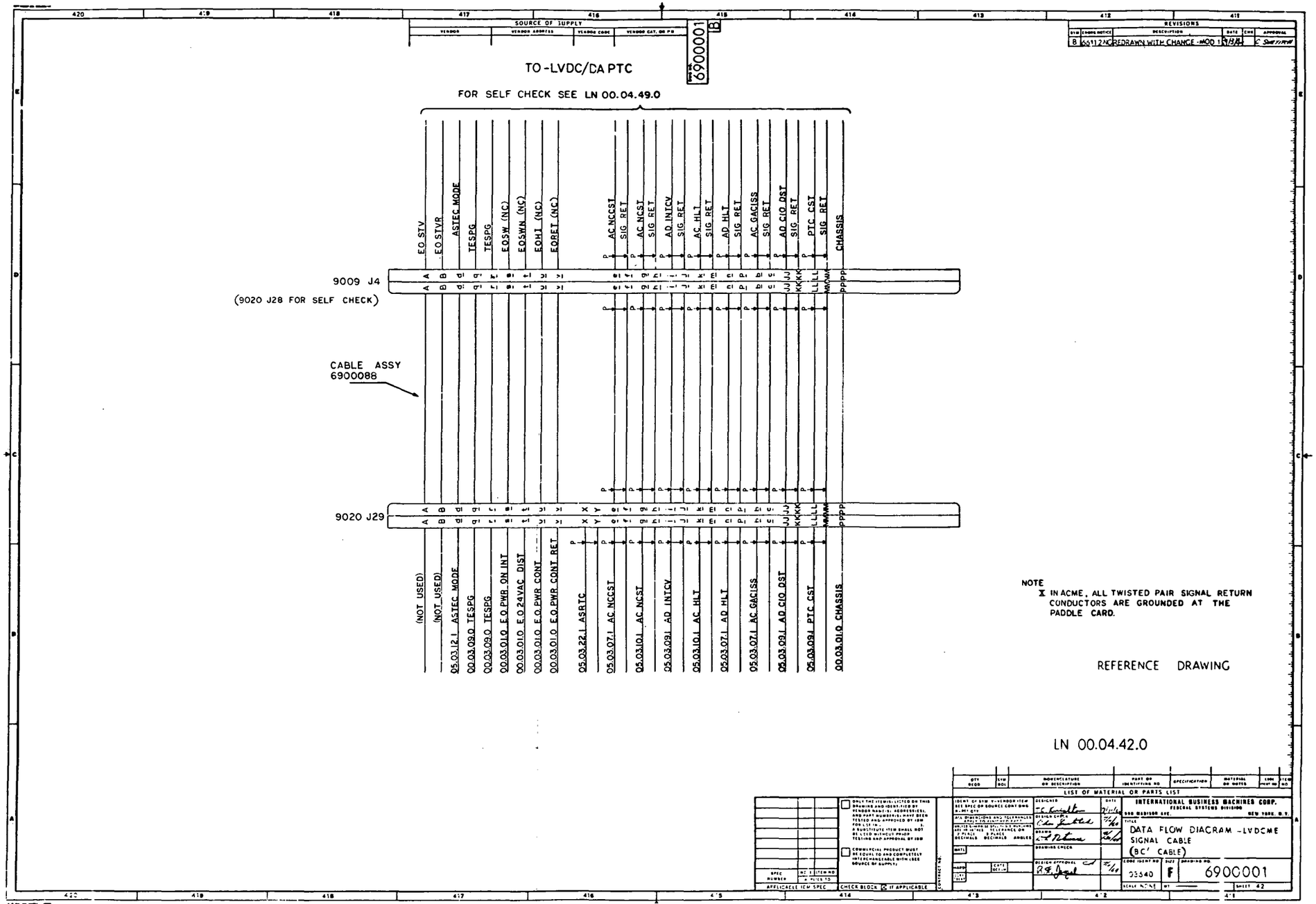


Figure 10-22. Signal Cable (AX, BC' and AV Cables) Data Flow Diagram (LN 00.04.41.0 through LN 00.04.43.0) (Sheet 2)

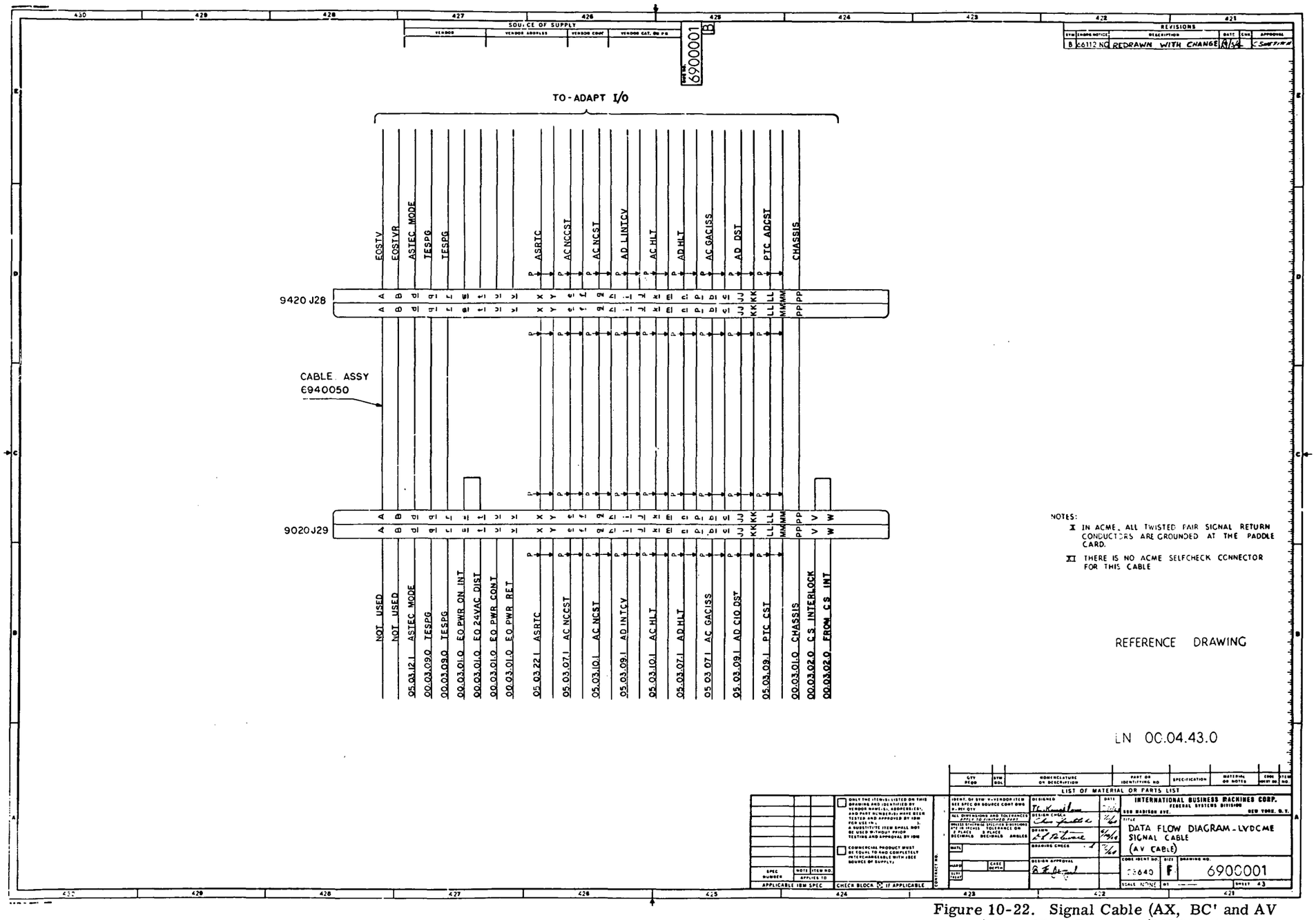


Figure 10-22. Signal Cable (AX, BC' and AV Cables) Data Flow Diagram (LN 00.04.41.0 through LN 00.04.43.0) (Sheet 3)

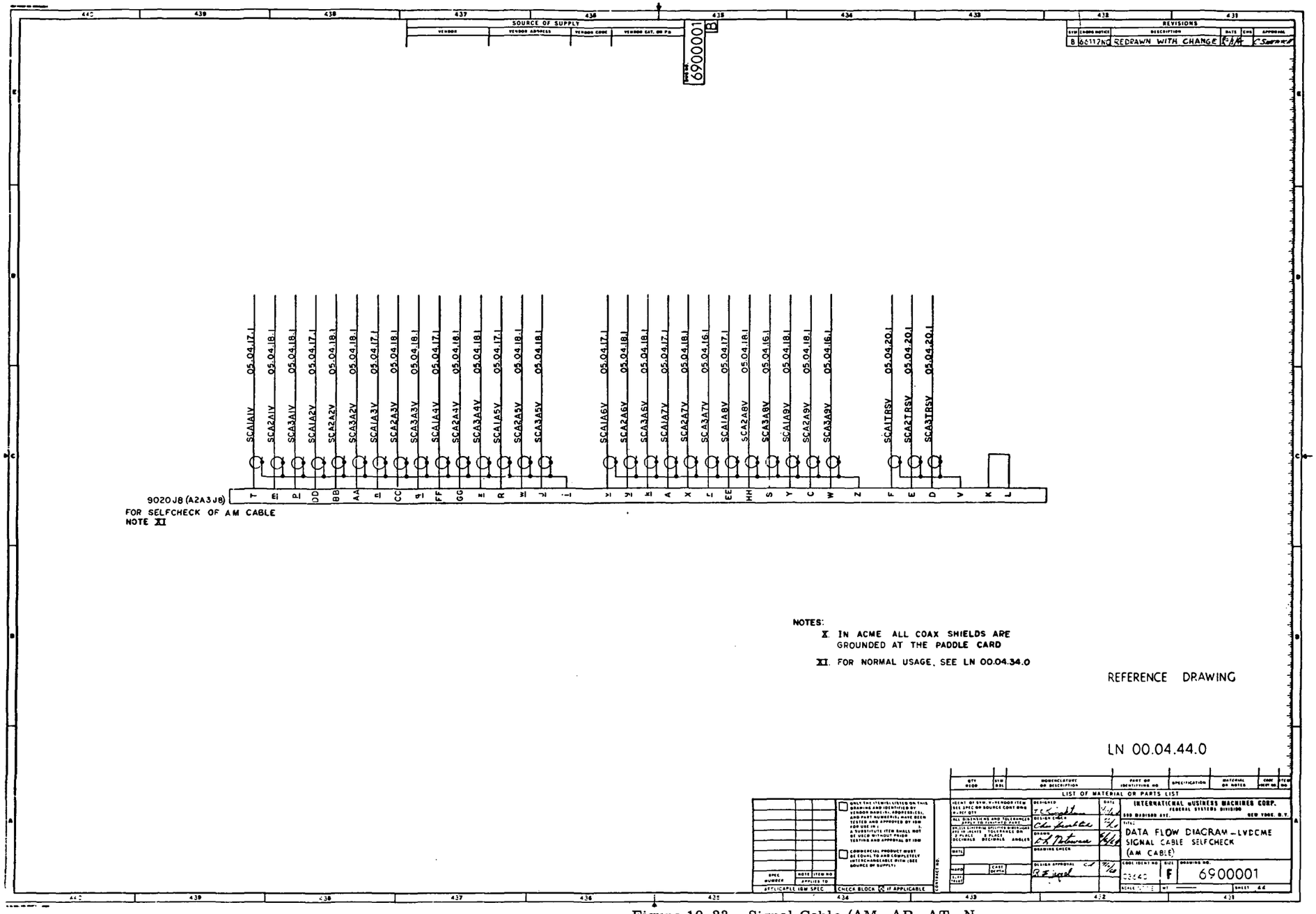


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 1 of 9)

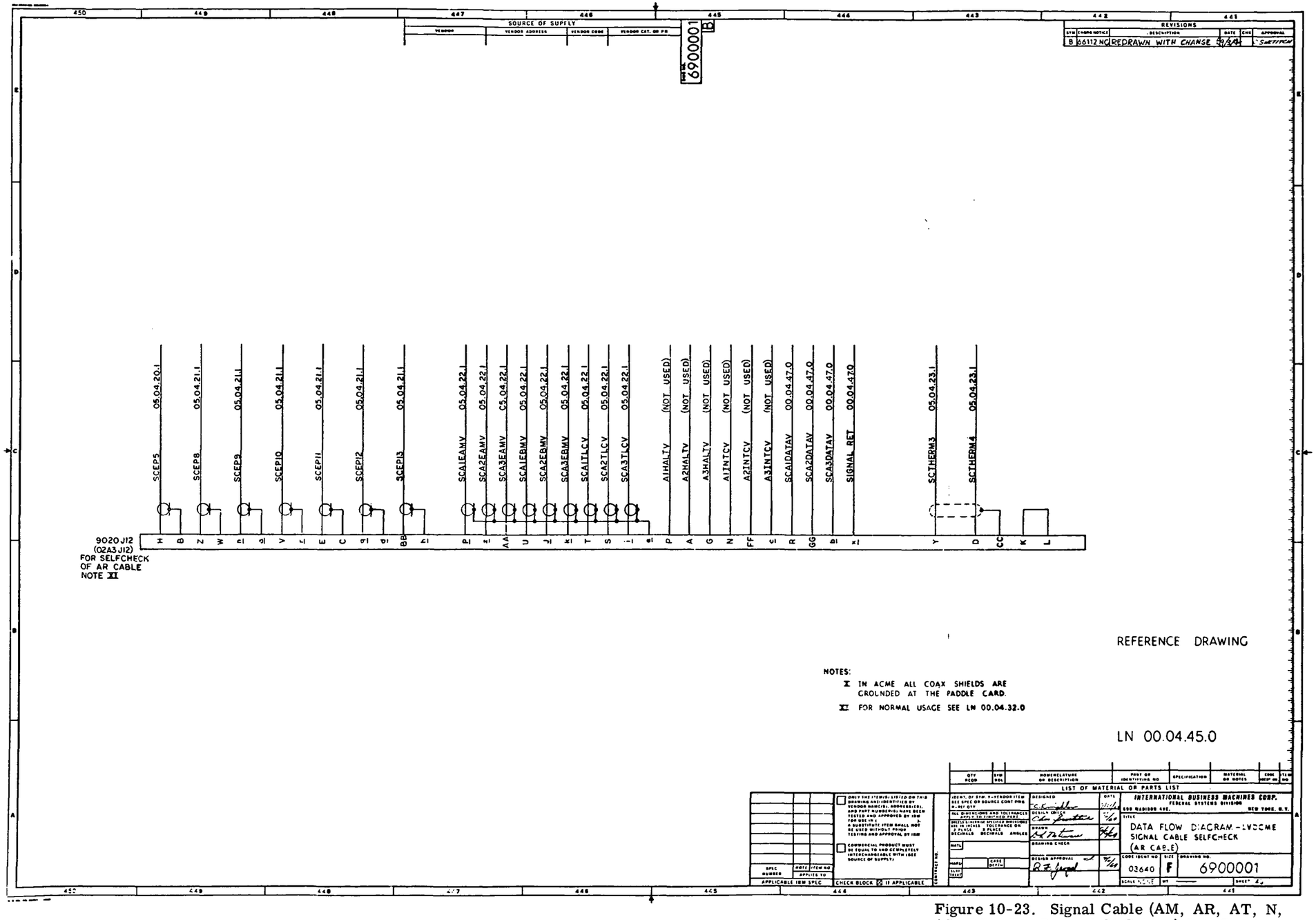


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 2)

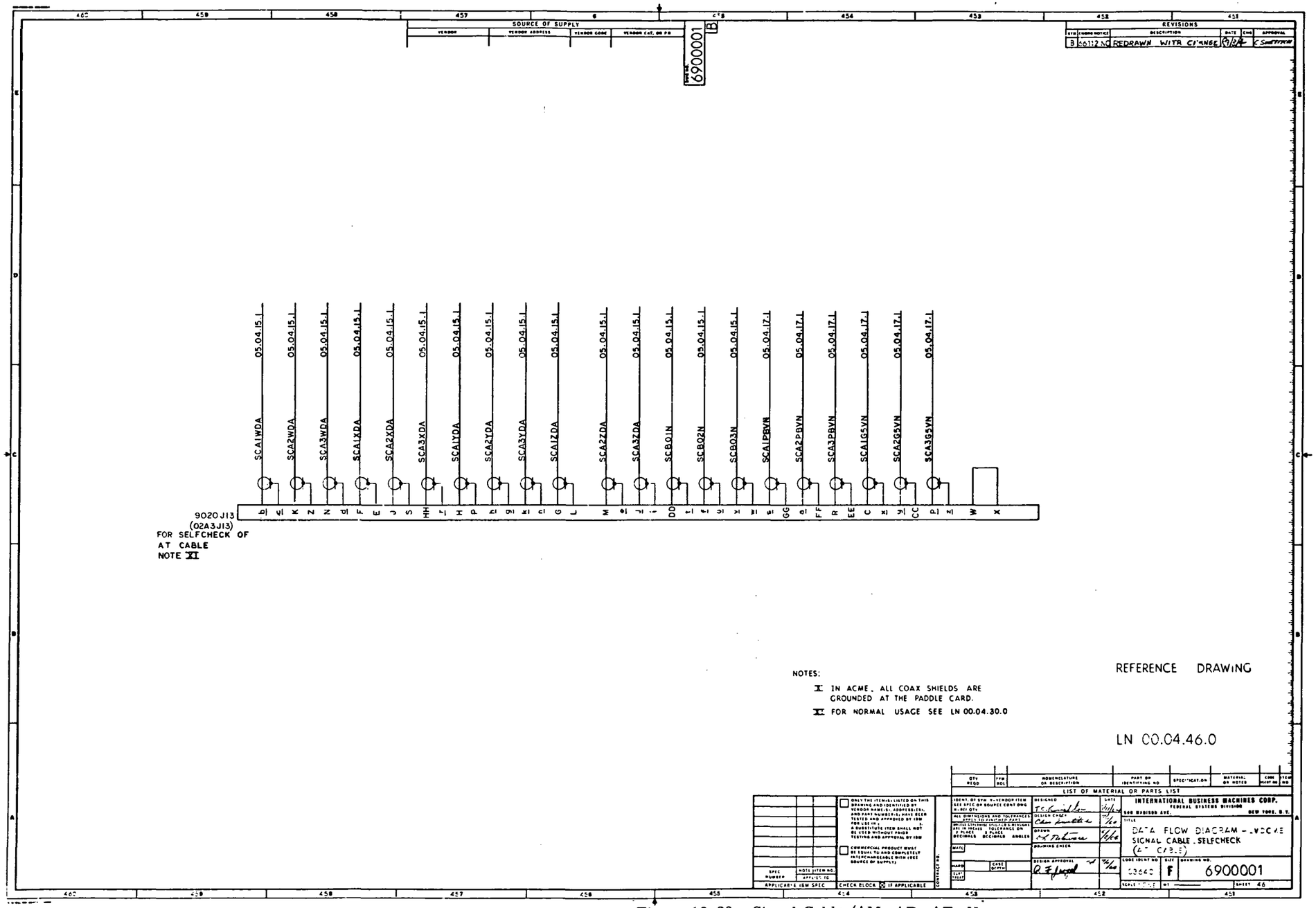
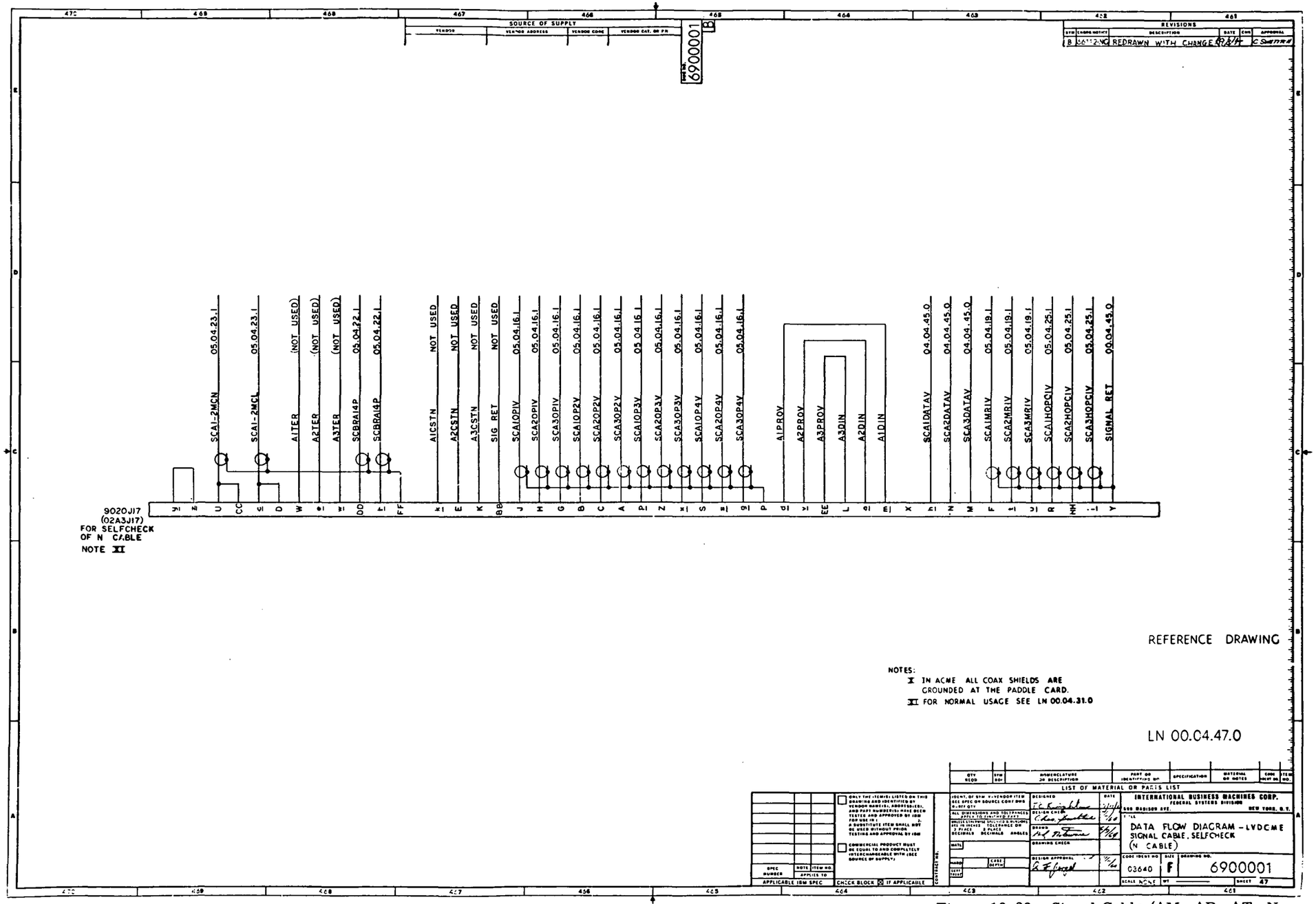


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 3)



REFERENCE DRAWING

NOTES:
- I IN ACME ALL COAX SHIELDS ARE GROUNDED AT THE PADDLE CARD.
- XI FOR NORMAL USAGE SEE LN 00.04.31.0

LN 00.04.47.0

LIST OF MATERIAL OR PARTS LIST

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
NEW YORK, N.Y.

DATA FLOW DIAGRAM - LVDCME SIGNAL CABLE, SELFCHECK (N CABLE)

CODE IDENT NO 03640 | SIZE F | DRAWING NO. 6900001 | SCALE NONE | SHEET 47

Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 4)

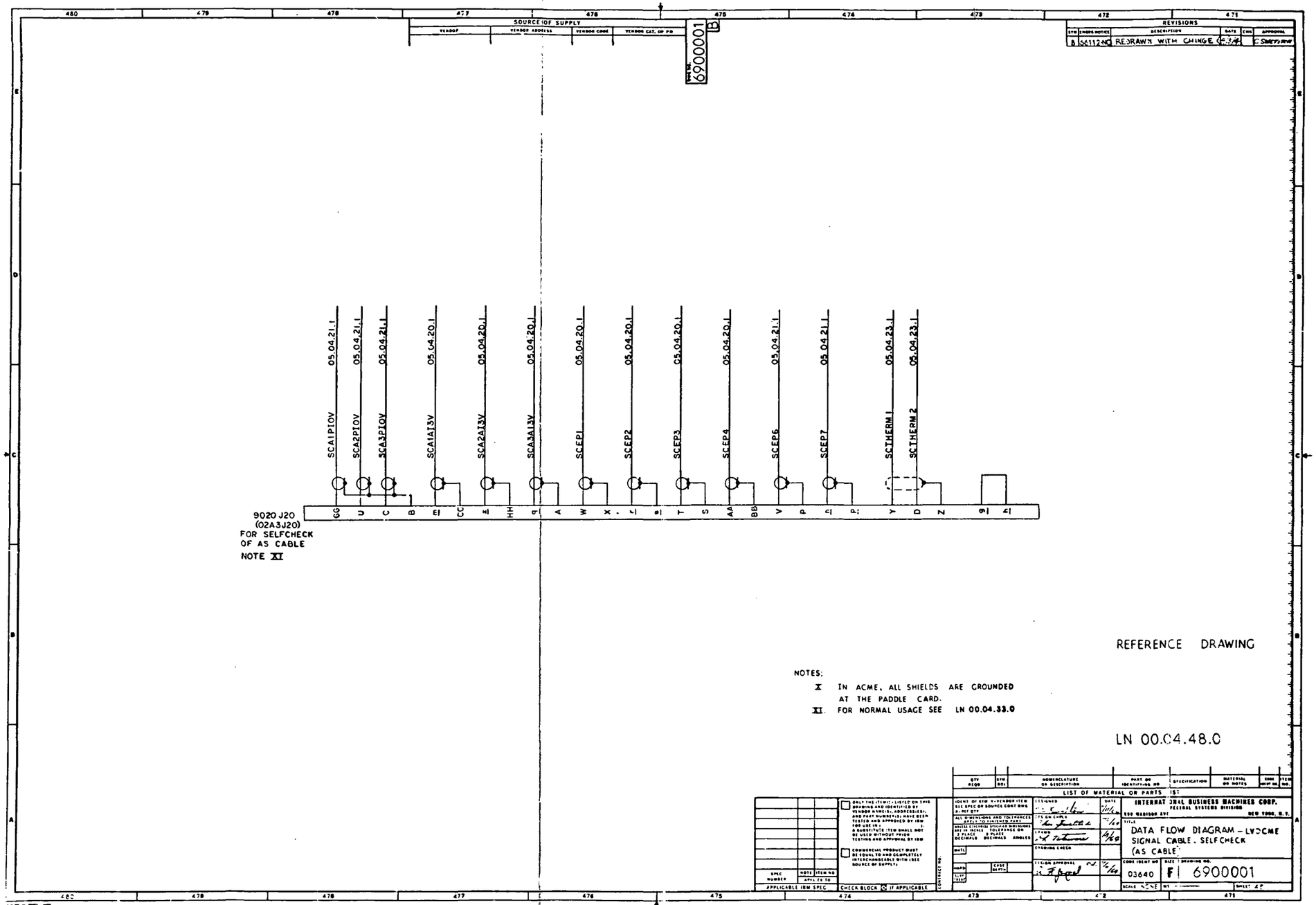


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 5)

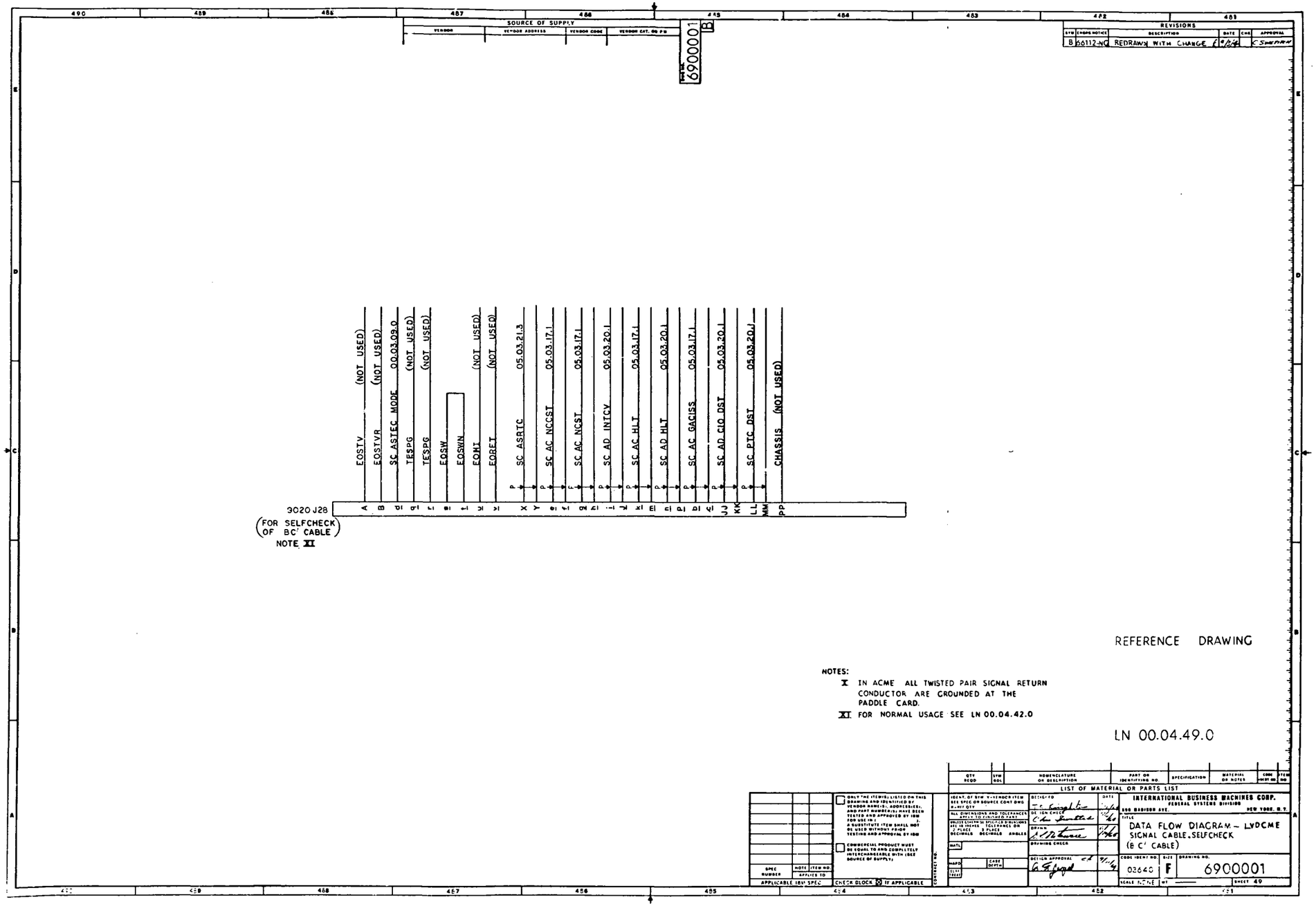


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 6)

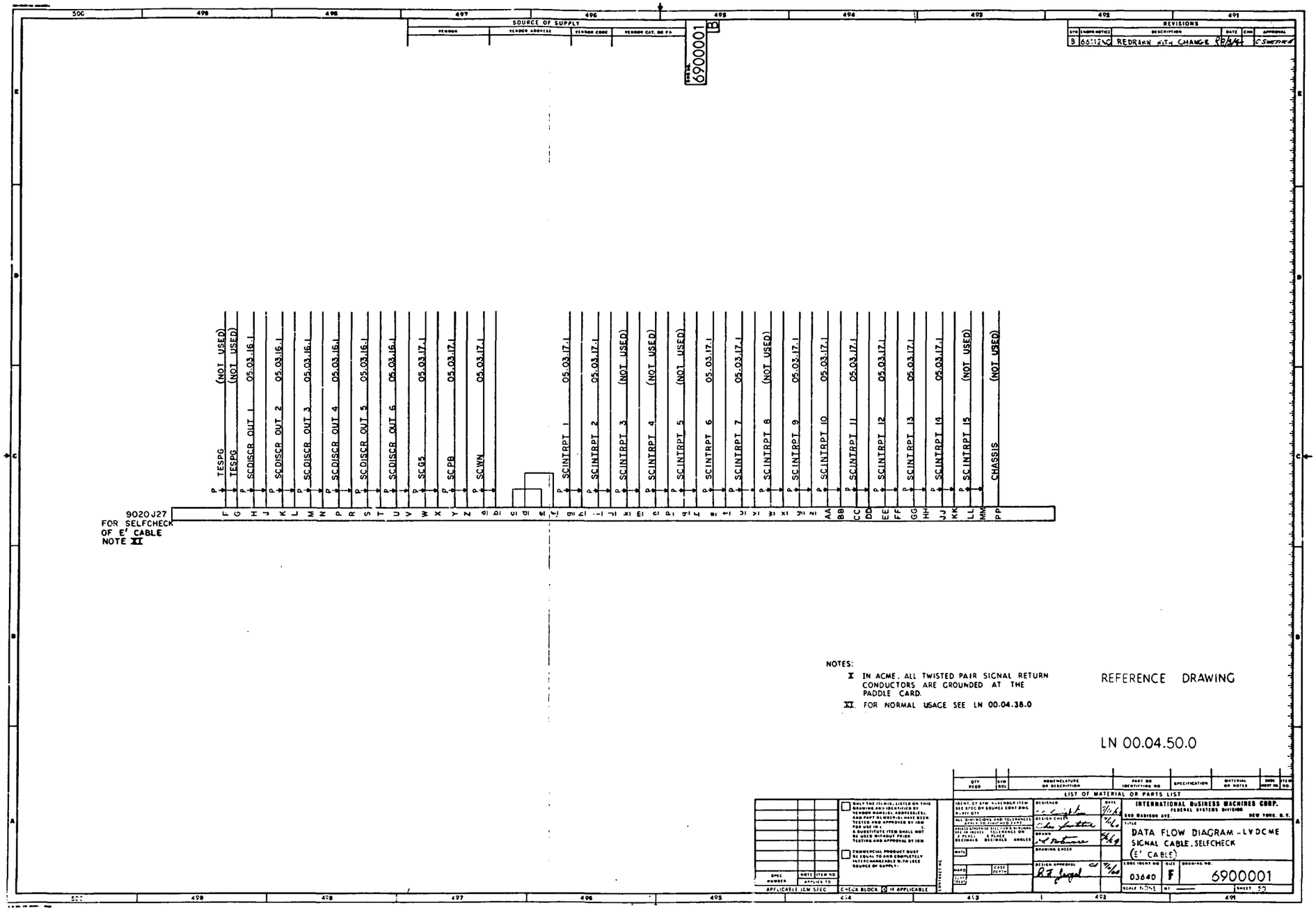


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 7)

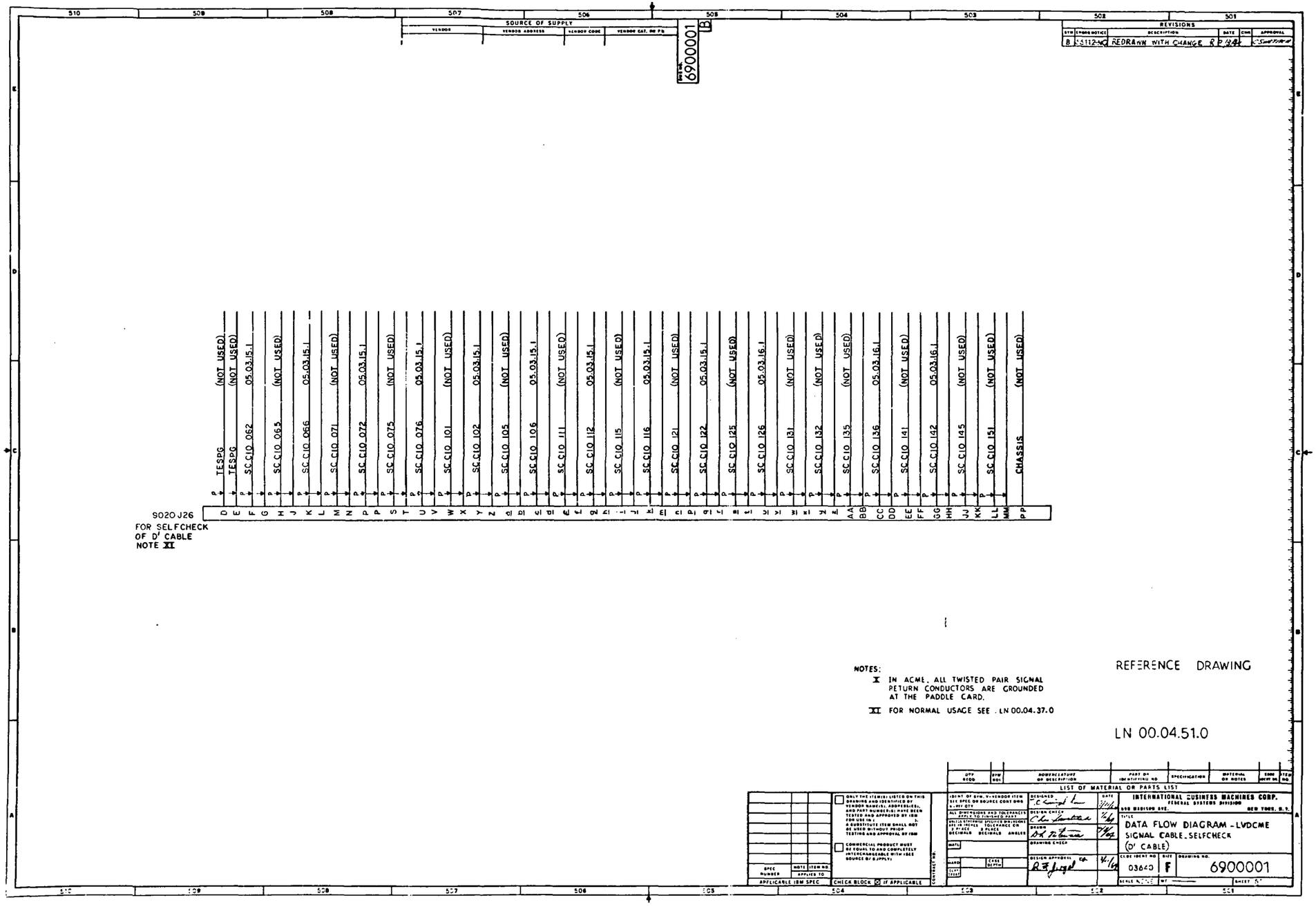


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 8)

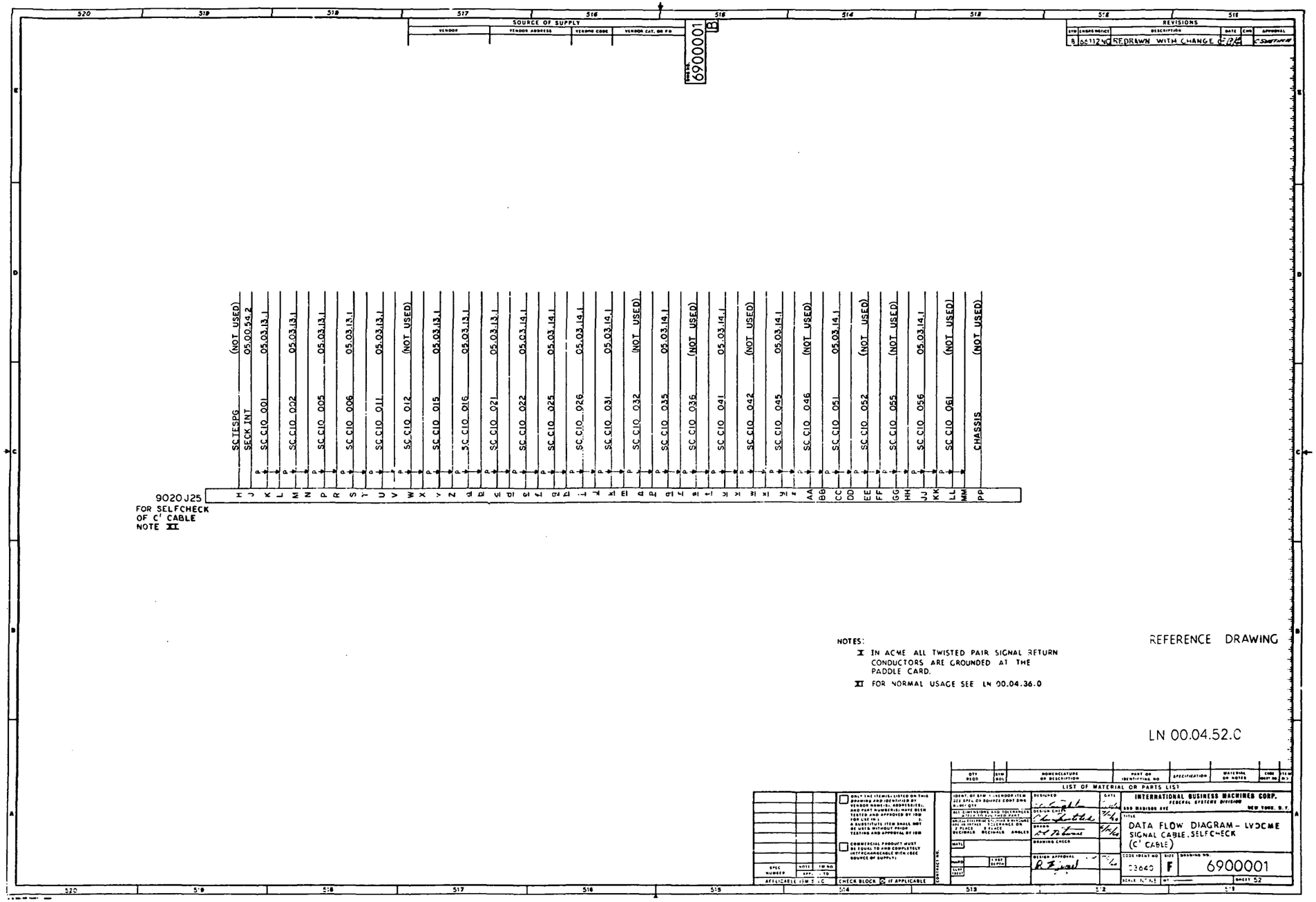


Figure 10-23. Signal Cable (AM, AR, AT, N, AS, BC', E', D', and C' Cables) Self Check Data Flow Diagram (LN 00.04.44.0 through 00.04.52.0) (Sheet 9)

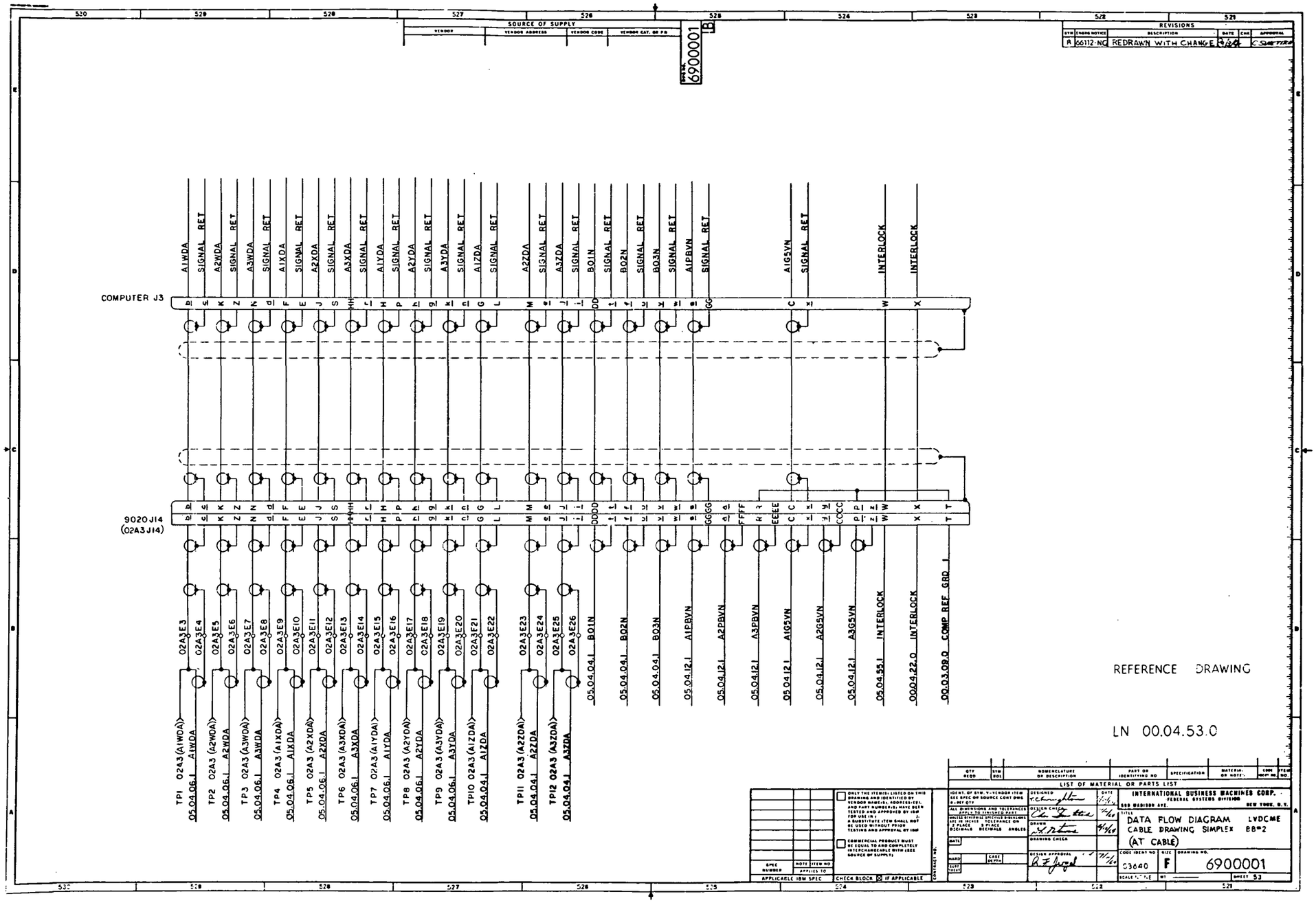


Figure 10-24. Signal (Simplex Computer BB #2) Cable (AT, N, AR, AS, and AM Cables) Data Flow Diagram (LN 00.04.53.0 through LN 00.04.57.0) (Sheet 1 of 5)

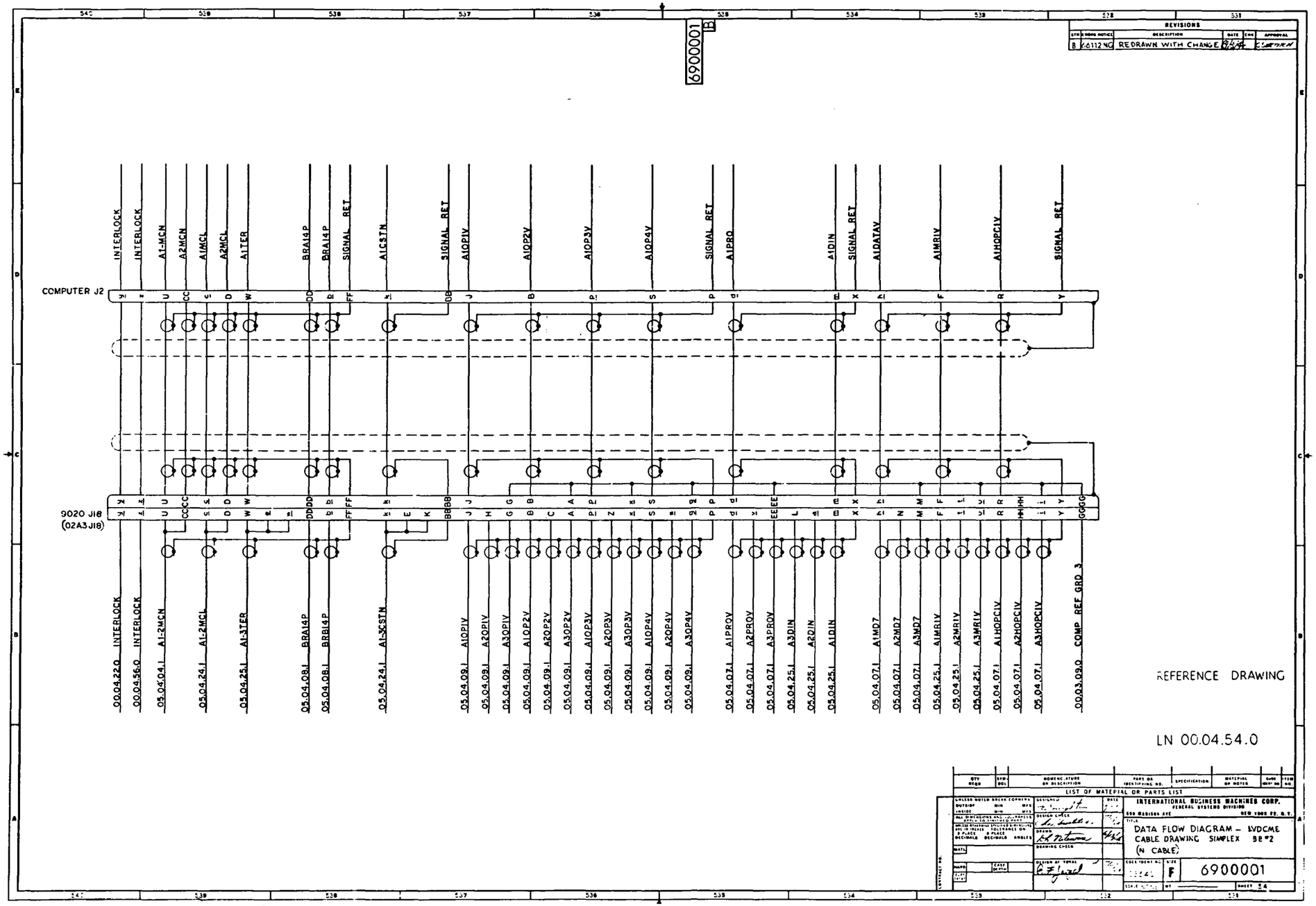


Figure 10-24. Signal (Simplex Computer BB #2) Cable (AT, N, AR, AS, and AM Cables) Data Flow Diagram (LN 00.04.53.0 through LN 00.04.57.0) (Sheet 2)

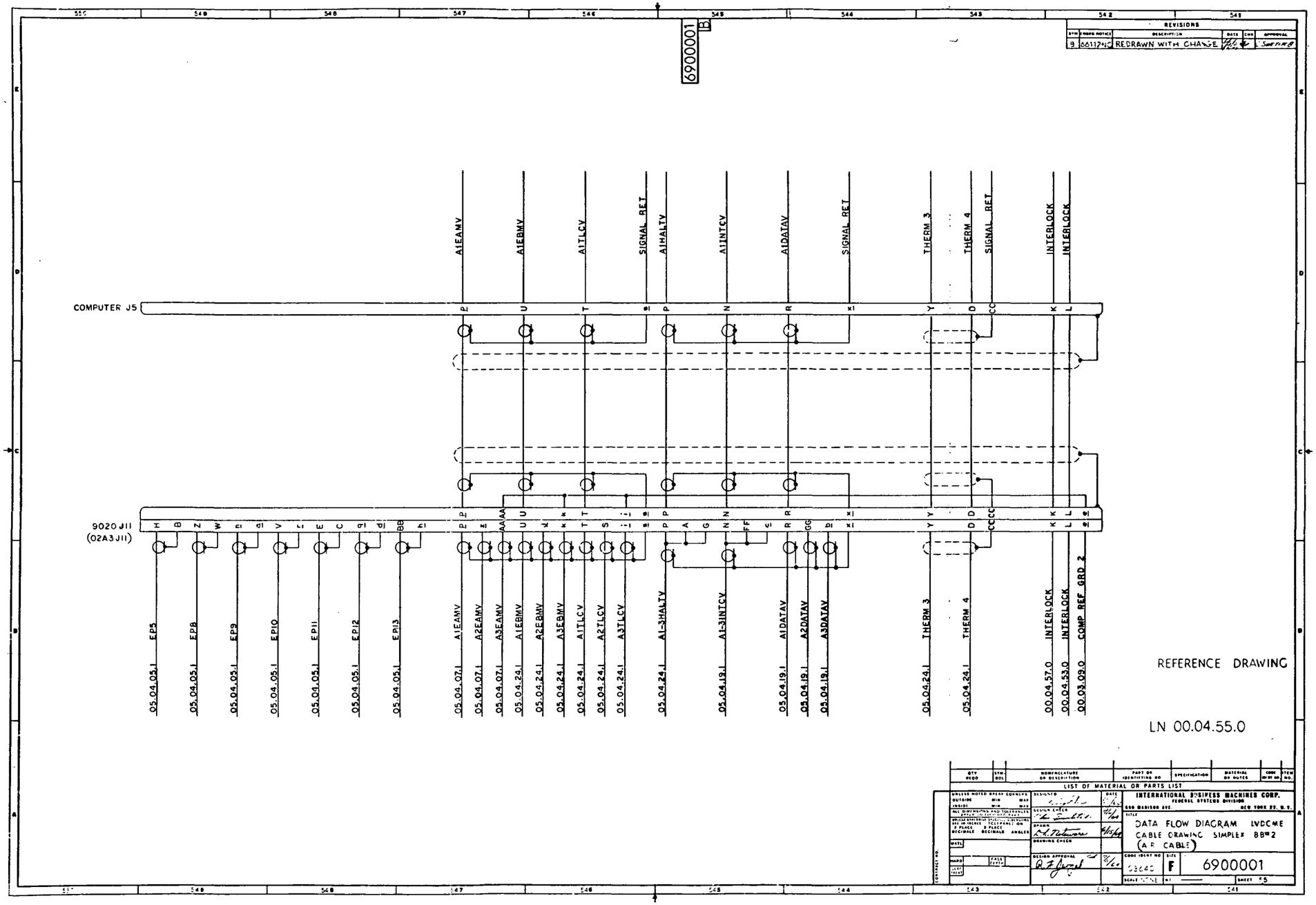


Figure 10-24. Signal (Simplex Computer BB #2) Cable (AT, N, AR, AS, and AM Cables) Data Flow Diagram (LN 00.04.53.0 through LN 00.04.57.0) (Sheet 3)

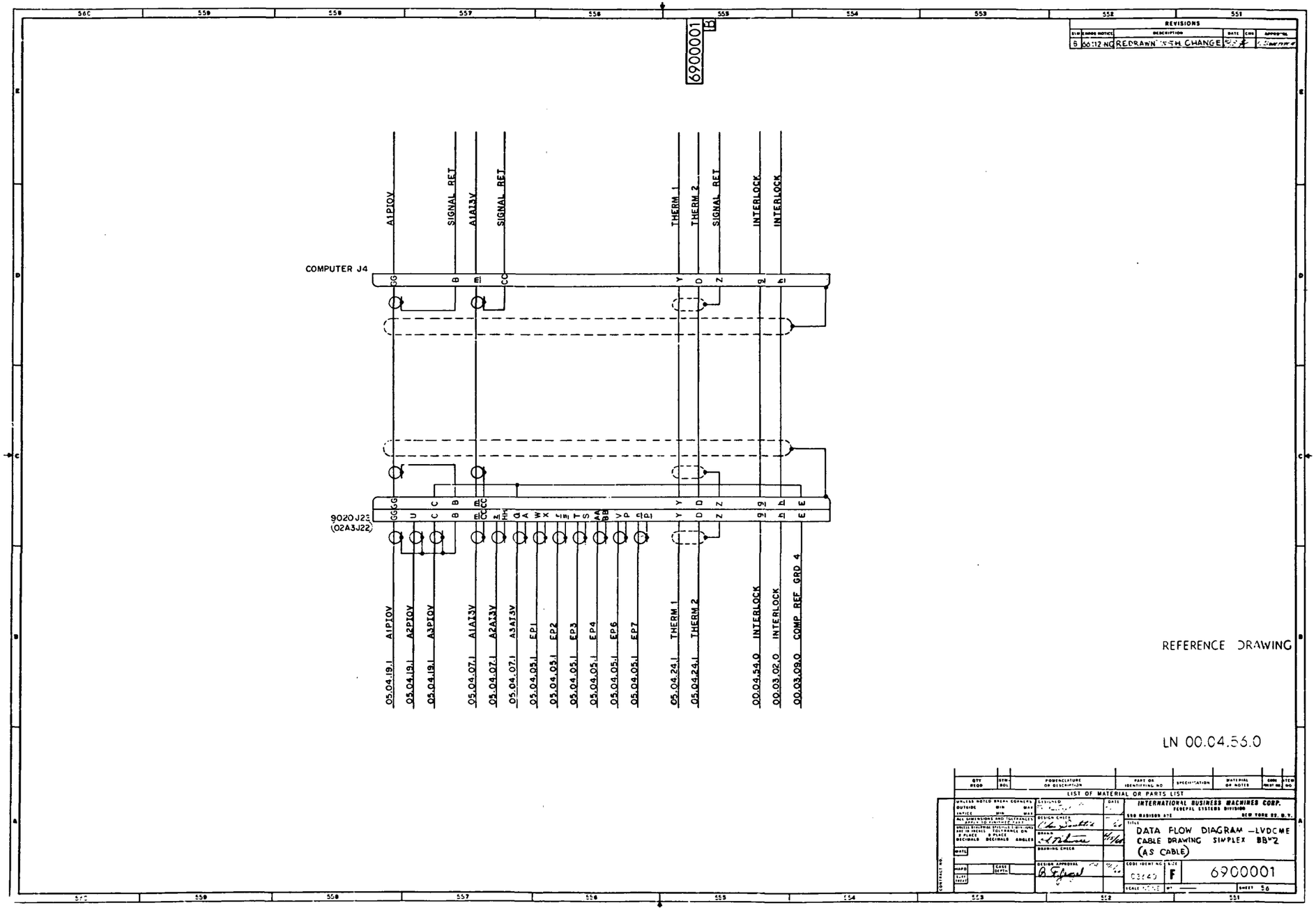


Figure 10-24. Signal (Simplex Computer BB #2) Cable (AT, N, AR, AS, and AM Cables) Data Flow Diagram (LN 00.04.53.0 through LN 00.04.57.0) (Sheet 4)

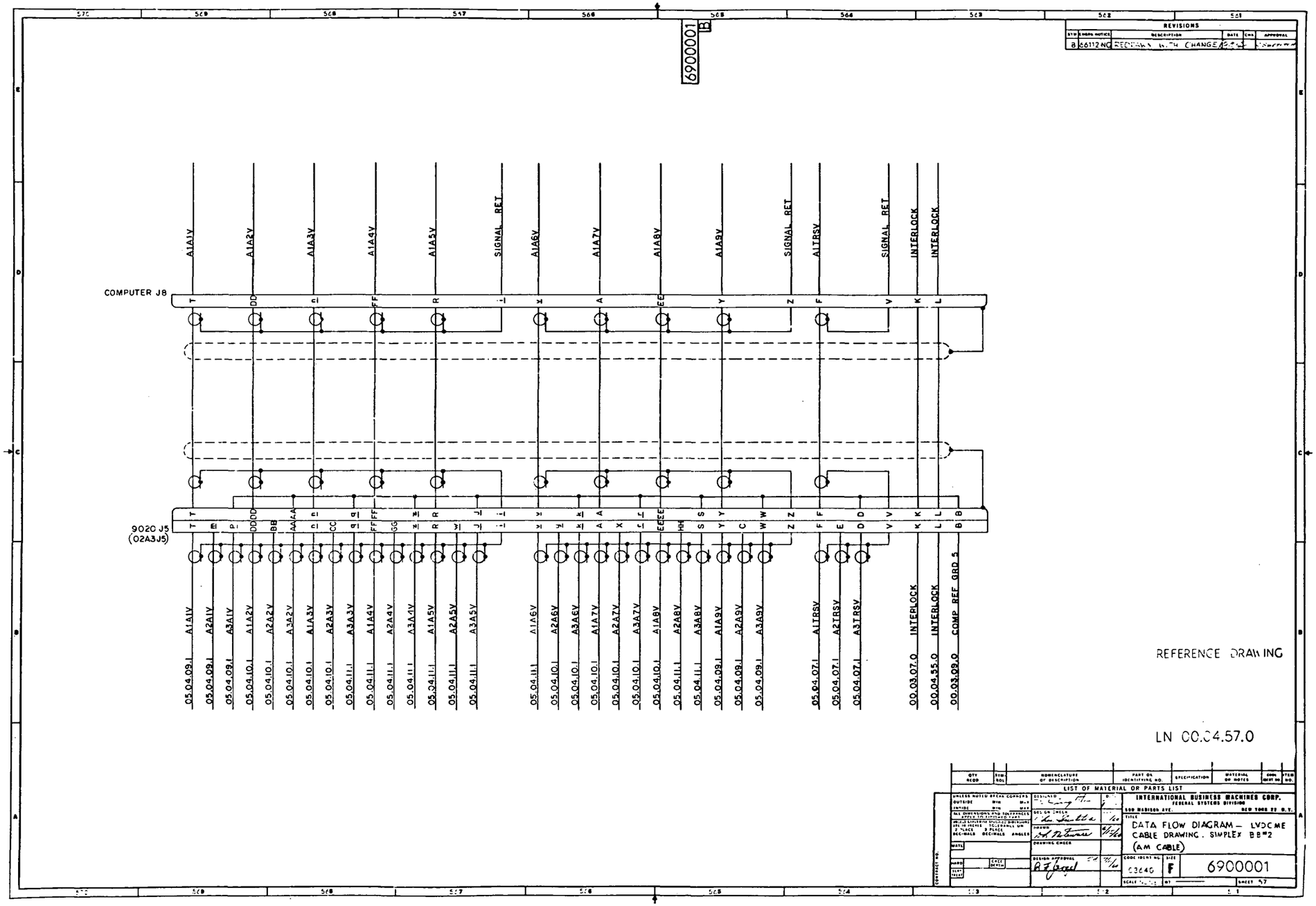


Figure 10-24. Signal (Simplex Computer BB #2) Cable (AT, N, AR, AS, and AM Cables) Data Flow Diagram (LN 00.04.53.0 through LN 00.04.57.0) (Sheet 5)

ACME MODULE SWITCHING RELAY CIRCUIT LOCATIONS

K NO.	COIL LOCATION	CIRCUIT "A" LOCATION	CIRCUIT "B" LOCATION	CIRCUIT "C" LOCATION	CIRCUIT "D" LOCATION	CIRCUIT "E" LOCATION	CIRCUIT "F" LOCATION	CIRCUIT "G" LOCATION	CIRCUIT "H" LOCATION
01	00.04.20.0	00.04.23.0	00.04.23.0	00.04.21.0	00.04.23.0	00 04.23.0	00.04.23.0	C0.04.23 0	00.04.23.0
02		OC 04.24.0		00.04.21.0	00.04.21.0				
03		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0		
04		00.04.23.0	00.04.23.0	00.04.25.0	C0.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
05		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	
06		00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
07		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0
08		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.27.0	
09		00.04.23.0	00.04.23.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
10		C0.04.22 0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24 0	00.04.26.0	
11		00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
12		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0
13		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.27.0	
14		00.04.23.0	00.04.23.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
15		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	
16		00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
17		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0
18		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.27.0	
19		00.04.23.0	00.04.23.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
20		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	
21	00.04.21.0	00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
22		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.25.0	00.04.26.0
23		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.27.0	
24		00.04.23.0	00.04.23.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
25		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	
26		00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
27		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0
28		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.27.0	
29		00.04.23.0	00.04.23.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
30		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	
31		00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
32		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0
33		00.04.23.0	00.04.23.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.27.0	
34		00.04.23.0	00.04.23.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.27.0	00.04.27.0
35		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.25.0	
36		00.04.22.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0	
37		00.04.22.0	00.04.25.0	00.04.25.0	00.04.24.0	00.04.24.0	00.04.24.0	00.04.26.0	00.04.26.0

REFERENCE DRAWING

LN 00.04.58.0

Figure 10-25. Relay Circuits Locations Data Flow Diagram (LN 00.04.58.0)

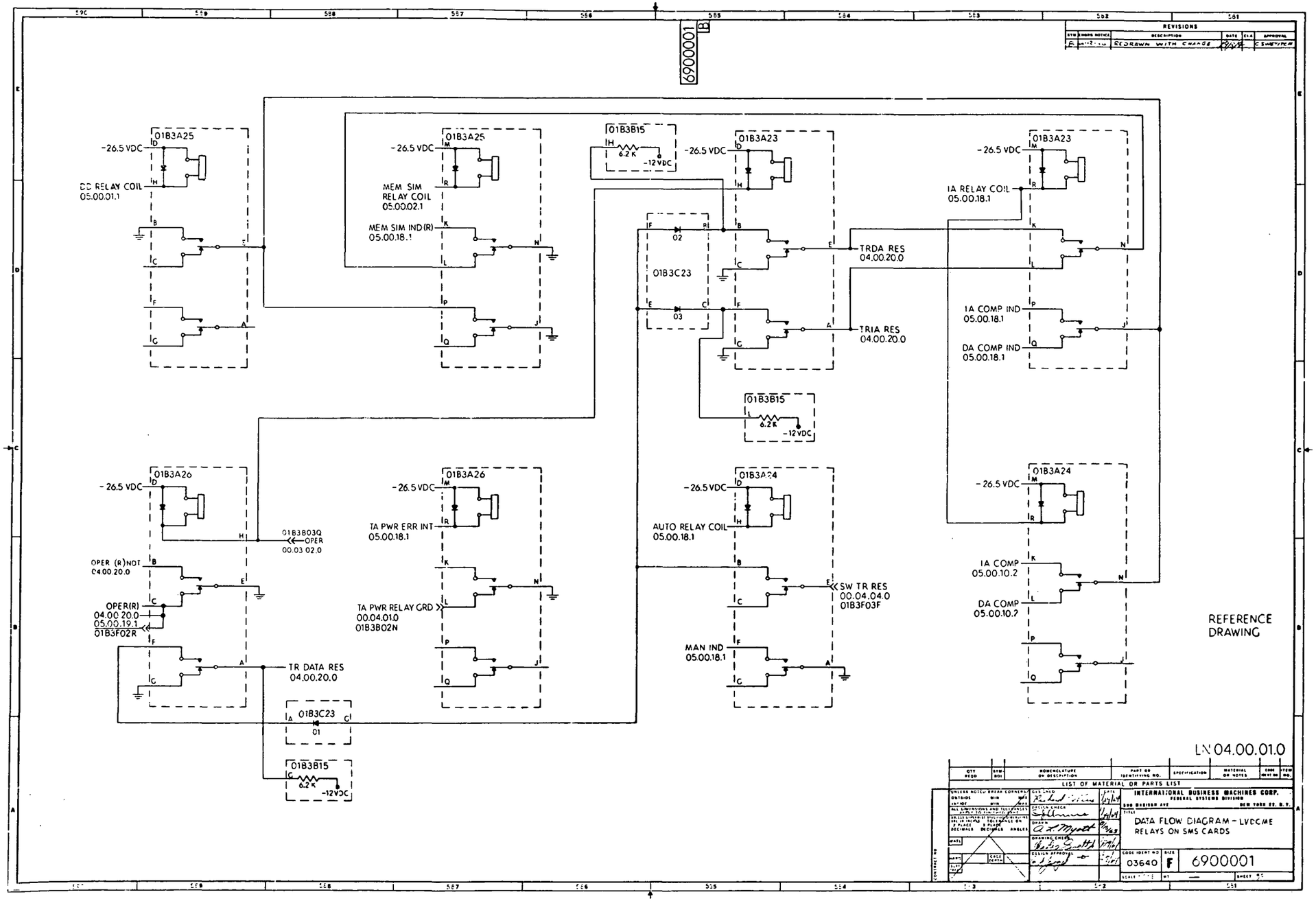


Figure 10-26. Relays on SMS Cards Data Flow Diagram (LN 04.00.01.0)

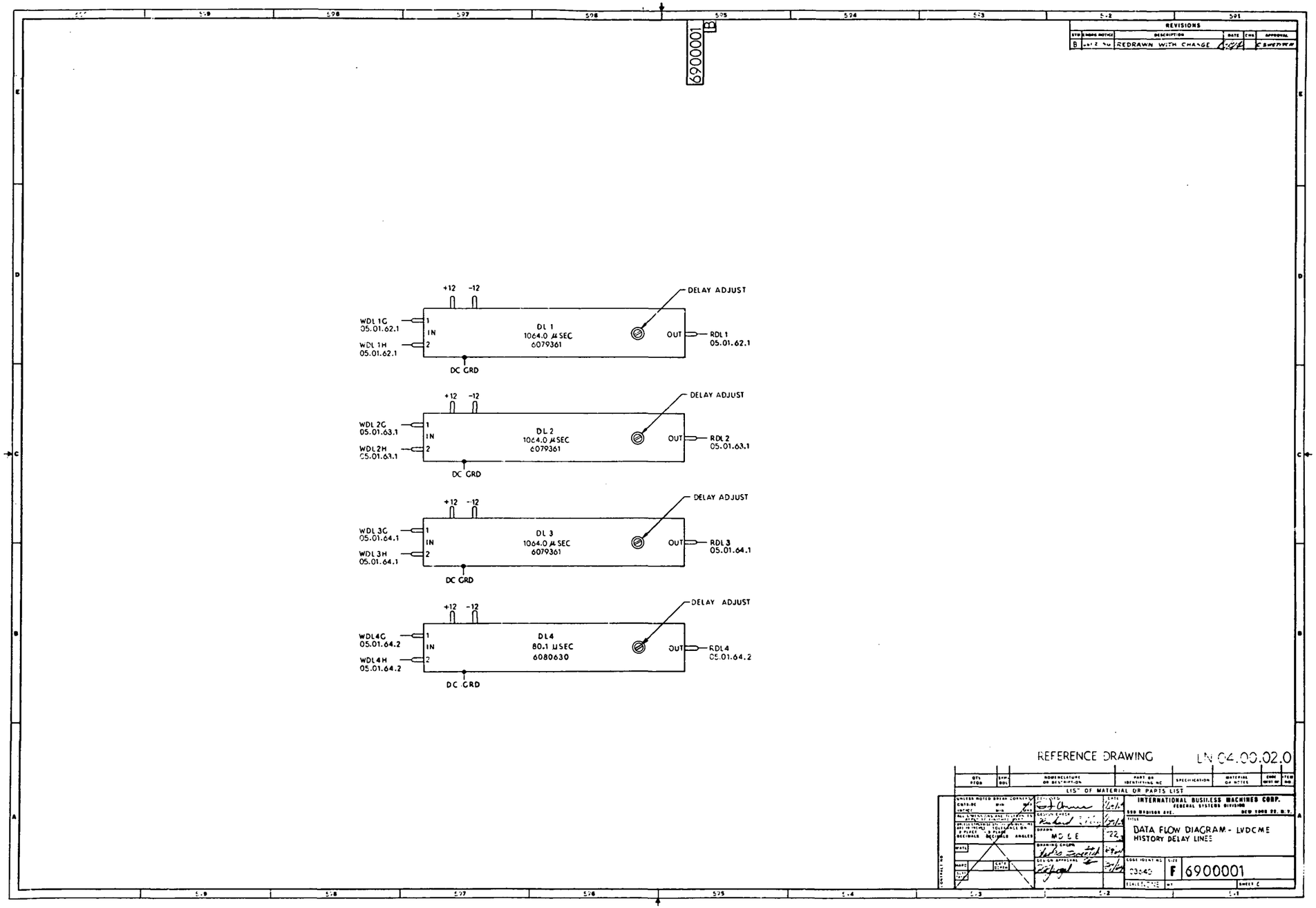


Figure 10-27. History Delay Lines Data Flow Diagram (LN 04.00.02.0)

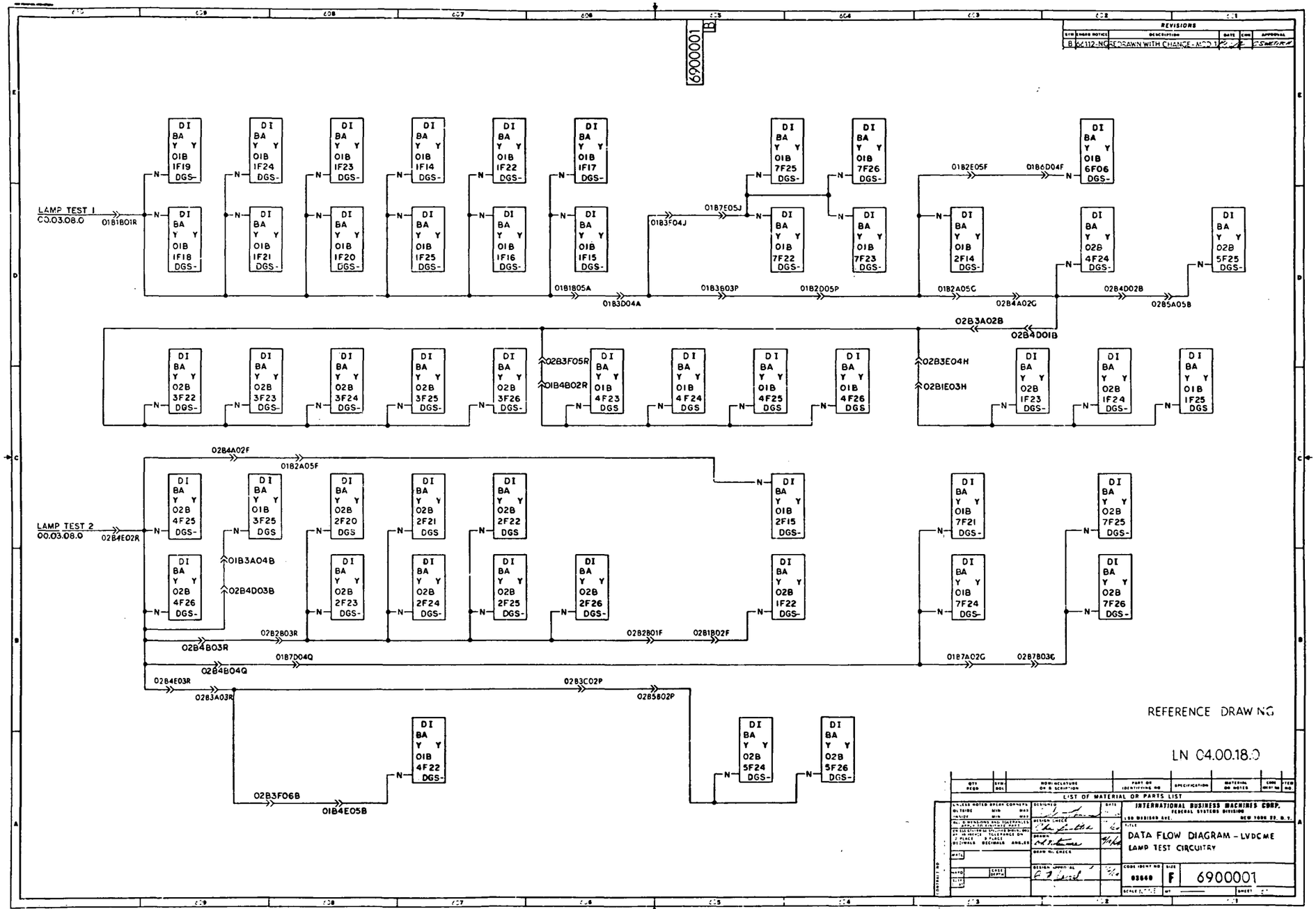


Figure 10-28. Lamp Test Circuitry Data Flow Diagram (LN 04.00.18.0 and LN 04.00.19.0) (Sheet 1 of 2)

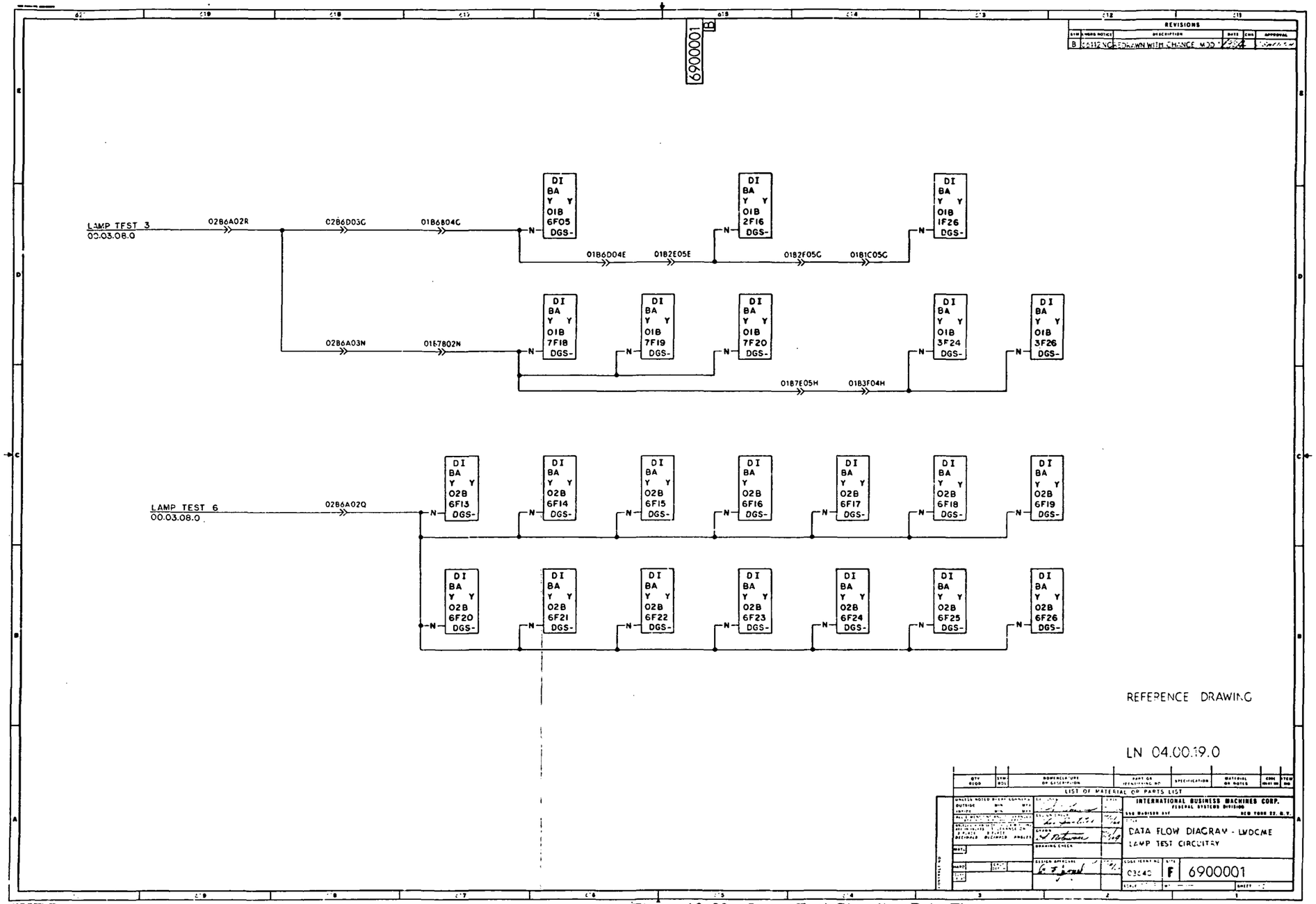


Figure 10-28. Lamp Test Circuitry Data Flow Diagram (LN 04.00.18.0 and LN 04.00.19.0) (Sheet 2)

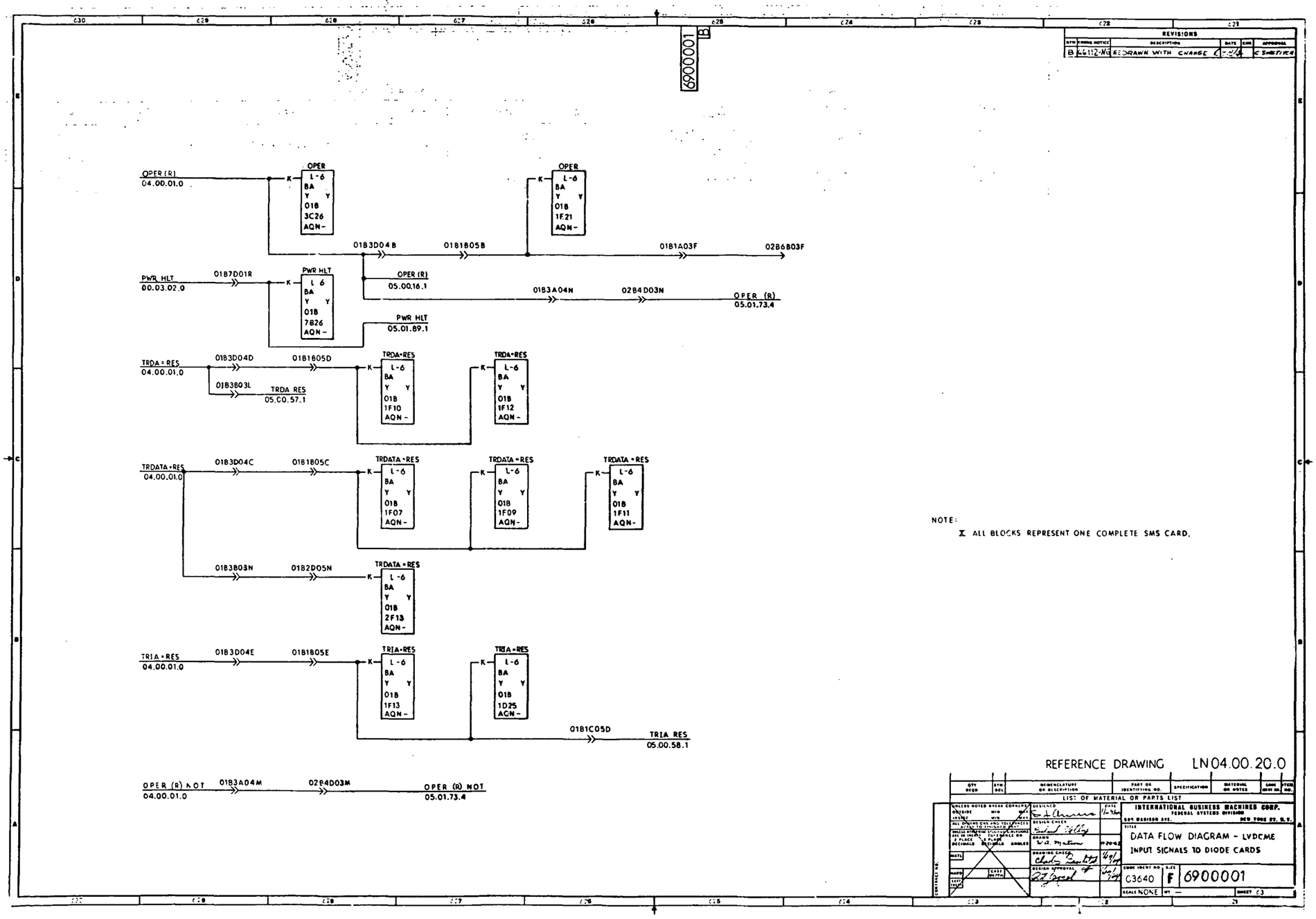


Figure 10-29. Input Signals To Diode Cards Data Flow Diagram (LN 04.00.20.0)

SYMBOL INDEX

1. AND
2. AND-Inverter
3. AND-OR-Inverter
4. Clock Driver
5. Detector
6. Delay
7. Delay Clock Monitor
8. Delay Line Monitor
9. Driver Terminator
10. Inverter
11. Inverter-Or
12. Latch L1
13. Latch L2
14. Latch L3
15. Latch L4
16. Latch L5
17. Latch L6
18. Latch L7
19. Latch L8
20. Lamp Driver
21. Line Driver
22. Oscillator
23. OR-Inverter
24. Power Driver
25. Relay Driver
26. Single Shot (Dual Input)
27. Single Shot (Tri-Input)
28. Translator
29. Translator Inverter
30. Tratch
31. Trigger 1
32. Trigger 2

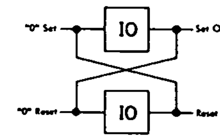
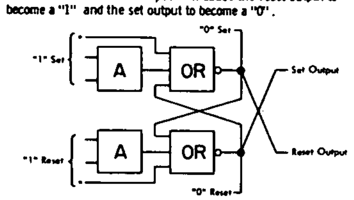
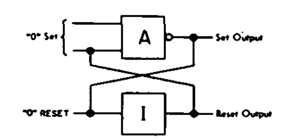
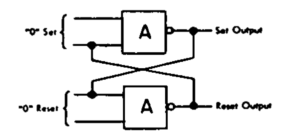
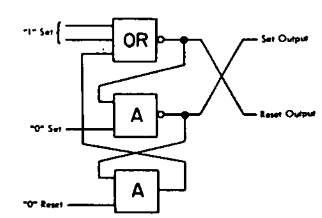
SYMBOL DEFINITIONS

NOTE

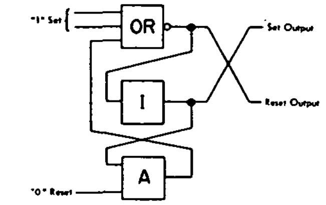
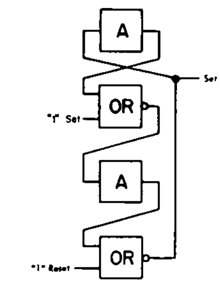
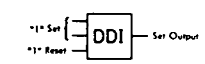
A logic "one" is a -6VDC (or -12VDC) level and a logic "zero" is a 0VDC level unless otherwise noted.

INDEX NO.	SYMBOL	NAME	DESCRIPTION
1.	A (Multiple Input)	AND	When all inputs are "1", the output is a "1". If any input is a "0", the output is a "0".
2.	A (Multiple Input)	AND-INVERTER	When all inputs are "1", the output is a "0". If any input is a "0", the output is a "1".
3.	AO (Multiple Input)	AND-OR-INVERTER	Inputs - outputs are the same as an And-Invert. The output transistor allows the outputs of several And-Or-Inverter to be connected (Anded) together. A "0" output of any AO of an "ANDed" group of AO's will form a "0" output from the group.
4.	CD	CLOCK DRIVER	Level shifter—a "1" input (low positive voltage) produces a "1" (+6VDC) output. A "0" input (low negative voltage) produces a "0" (0VDC) output.
5.	DET	DETECTOR	The Detector is driven by a Delay Line. A "1" input to the Delay Line causes the Detector normally "1" output to become a "0".
6.	X USEC DLY	DELAY	This circuit delays only the positive transition of its input; A delay occurs only when the input changes from a "1"(-6VDC) to a "0" (0 VDC). The nominal delay duration is indicated above the symbol. A "1" input causes a "1" output.
7.	400 NSEC DLC	DELAY CLOCK MONITOR	This circuit monitors delay line clock pulses; its normal output is a "0". If the input level does not change from a "0" to a "1" or from a "1" to a "0" during a time of 400 NSEC, the output level is forced to a "1" at the end of the 400NSEC period.
8.	DRVR	DELAY LINE DRIVER	A "1" at either input causes a pulse to be emitted at both outputs. The output pulses are tapped from a resistor divider network.
9.	DT	DRIVER TERMINATOR	Signal shaper, inverter and low impedance matching device.
10.	I	INVERTER	A "1" input will result in a "0" output and vice-versa.
11.	IO	INVERTER-OR	Input-output same as Inverter. The output transistor allows the outputs of several Inverter-Ors to be connected (ANDed) together; a "0" output of any IO of an "Anded" group of IO's will force a "0" output from the group.

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
12.	L1 ("0" Set, "0" Reset, Set Output, Reset Output)	LATCH 1	 The "one-drive" inputs ("1" set and "1" reset) are normally "0's" and the "zero-drive" inputs ("0" set and "0" reset) are normally "1's". The set and reset outputs are complementary; a "0" at the "0" set input or a "1" at the "1" set input will cause the set output to become a "1" and the reset output to become a "0". The outputs will remain in this condition even after the input conditioning level is removed. A "0" at the "0" reset input or a "1" at the "1" reset input will cause the reset output to become a "1" and the set output to become a "0".
13.	L2 ("0" Set, "1" Set, "1" Reset, "0" Reset, Set Output, Reset Output)	LATCH 2	 Asterisk inputs are grounded if no input signal is shown. See Latch 1.
14.	L3 ("0" Set, "0" Reset, Set Output, Reset Output)	LATCH 3	 See Latch 1.
15.	L4 ("0" Set, "0" Reset, Set Output, Reset Output)	LATCH 4	 See Latch 1.
16.	L5 ("0" Set, "1" Set, "0" Reset, Set Output, Reset Output)	LATCH 5	 See Latch 1.

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
17.	L6 ("1" Set, "0" Reset, Set Output, Reset Output)	LATCH 6	 See Latch 1.
18.	L7 ("1" Set, "1" Reset, Set Output)	LATCH 7	 See Latch 1.
19.	L8 ("1" Set, "1" Reset, Set Output)	LATCH 8	 Input: "1" = +6VDC, "0" = 0VDC. Output: "1" = -6VDC, "0" = 0VDC. See Latch 1.
20.	LD	LAMP DRIVER	A "1" input causes the LAMP DRIVER to turn on its associated indicator lamp; a "0" input causes the LAMP DRIVER to turn off its associated indicator lamp.
21.	LINE DR	LINE DRIVER	Signal driver and low impedance matching device. No inversion.
22.	OSC	OSCILLATOR	Generates a square wave signal (0VDC to -6VDC) which switches at a 2.048 MC rate.
23.	OR	OR-INVERTER	When all inputs are "0", the output is a "1". If any input is a "1", the output is a "0". The outputs of several Or-Inverts can be connected together.

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112-MP	RELEASE R	6/17/4		C. SWETITCH
A	66112 PM	SEE ENGRG NOTICE	10/1/64		DANNIS

REFERENCE DRAWING

LIST OF MATERIAL OR PARTS LIST

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: LOGIC DIAGRAM, LAUNCH VEHICLE DIGITAL COMPUTER MANUAL EXERCIZER (LVDC-ME)—SYMBOL DEFINITIONS

DESIGN CHECK: G. G. Kuter 7/24/64
DESIGN APPROVAL: 7/24/64

SIZE F — DRAWING NO. 6902020 — SHEET 1 OF 51

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 1 of 51)

SOURCE OF SUPPLY

VENDOR	VENDOR'S ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

SIZE A — 6902020

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 MP	RELEASE	R 8/1/64		C SWITCH
A	66112 PM	SEE ENGRG NOTICE	11/6/64		D ANNIS

SYMBOL DEFINITIONS (Cont)

INDEX NO.	SYMBOL	NAME	DESCRIPTION
23.	PD	POWER DRIVER	Signal shaper and driver—a "1" input causes a "1" output and vice-versa.
24.	RELAY DR	RELAY DRIVER	Input: "1" → Output: 0VDC; Input: "0" → Output: -26.5VDC
25.	X USEC SS (Dual-Input)	SINGLE SHOT	A negative going transition triggers the negative square wave output. The output is fed back to hold the signal shot on for the duration of the pulse. The pulse duration is shown above the symbol.
26.	X USEC SS (Tri-Input)	SINGLE SHOT	Any or all three inputs may be connected. An unconnected input (indicated by the absence of an input) is effectively a "1" input. All inputs must equal "1" to trigger the single shot. The negative going transition of the last input to become a "1" triggers the single shot. The duration of the negative square wave output is shown above the symbol.
27.	TSLT	TRANSLATOR	The TRANSLATOR circuits are level shifters that convert the negative logic levels used in the LVDCME to the positive logic levels used in the computer and LVDCME self-check circuitry. Inversion does not occur; a "1" input causes a "1" output, and a "0" input causes a "0" output.
28.	TSLI	TRANSLATOR-INVERTOR	The TRANSLATOR-INVERTER circuits perform both level shifting and inversion. These circuits convert the positive logic levels used in the computer and LVDCME self-check circuitry to the negative logic levels used in the LVDCME logic. A "1" input causes a "0" output, and a "0" input causes a "1" output.
29.	0 TCH 0; 1 1; 1 1	TRATCH	Only one input is a "0" and only one output is a "0" at any one time.
30.	A, B, C, D; "1" Set (1 Drive); "1" Reset (1 Drive); T1; Set Output; Reset Output	TRIGGER 1	The trigger is set (set output = "1" and reset output = "0") when input A is a "0" and input B goes from a "1" to a "0". The trigger is reset (set output = "0" and reset output = "1") when input D is a "0" and input C goes from a "1" to a "0". (The omission of the "1" set and "1" reset inputs indicates that these lines are grounded.)
31.	A, B, C; "1" Set (1 Drive); "1" Reset (1 Drive); T2; Set Output; Reset Output	TRIGGER 2	The trigger is set (set output = "1" and reset output = "0") when input A is a "0" and input B goes from a "1" to a "0". The trigger is reset (set output = "0" and reset output = "1") when input C is a "0" and input B goes from a "1" to a "0". (The omission of the "1" set and "1" reset inputs indicates that these lines are grounded.)

NOTES:

1. Abbreviations of signal names are defined in 6900008, Symbol Definitions and Signal Abbreviations for the ACME. Listing of additional abbreviations are:

USEC	microsecond
NSEC	nanosecond
MC	megacycles

2. The numbers listed in tabular INPUTS and OUTPUTS columns are sheet number locations of signal origin and destinations.
3. All logic blocks are defined on sheets 1 and 2.

REFERENCE DRAWING

QTY REQD	SYM SOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE	ITEM NO

LIST OF MATERIAL OR PARTS LIST

SPEC NUMBER	NOTE	ITEM NO.
APPLICABLE IBM SPEC	APPLIES TO	

☐ ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN ( ). A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

☐ COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH LISTED SOURCE OF SUPPLY.

CHECK BLOCK ☒ IF APPLICABLE

IDENT. OF SYM: Y-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG X-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES

MATL | HARD | SOFT | CASE DEPTH

DESIGNED | DATE

DESIGN CHECK J. D. Kester 7/24/64

DRAWN | DRAWING CHECK

DESIGN APPROVAL 7/24/64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
510 MADISON AVE. NEW YORK, N.Y.

TITLE: SYMBOL DEFINITIONS

CODE IDENT NO 03640 | SIZE F | DRAWING NO. 6902020

SCALE NONE | WT — | SHEET 2

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 2)

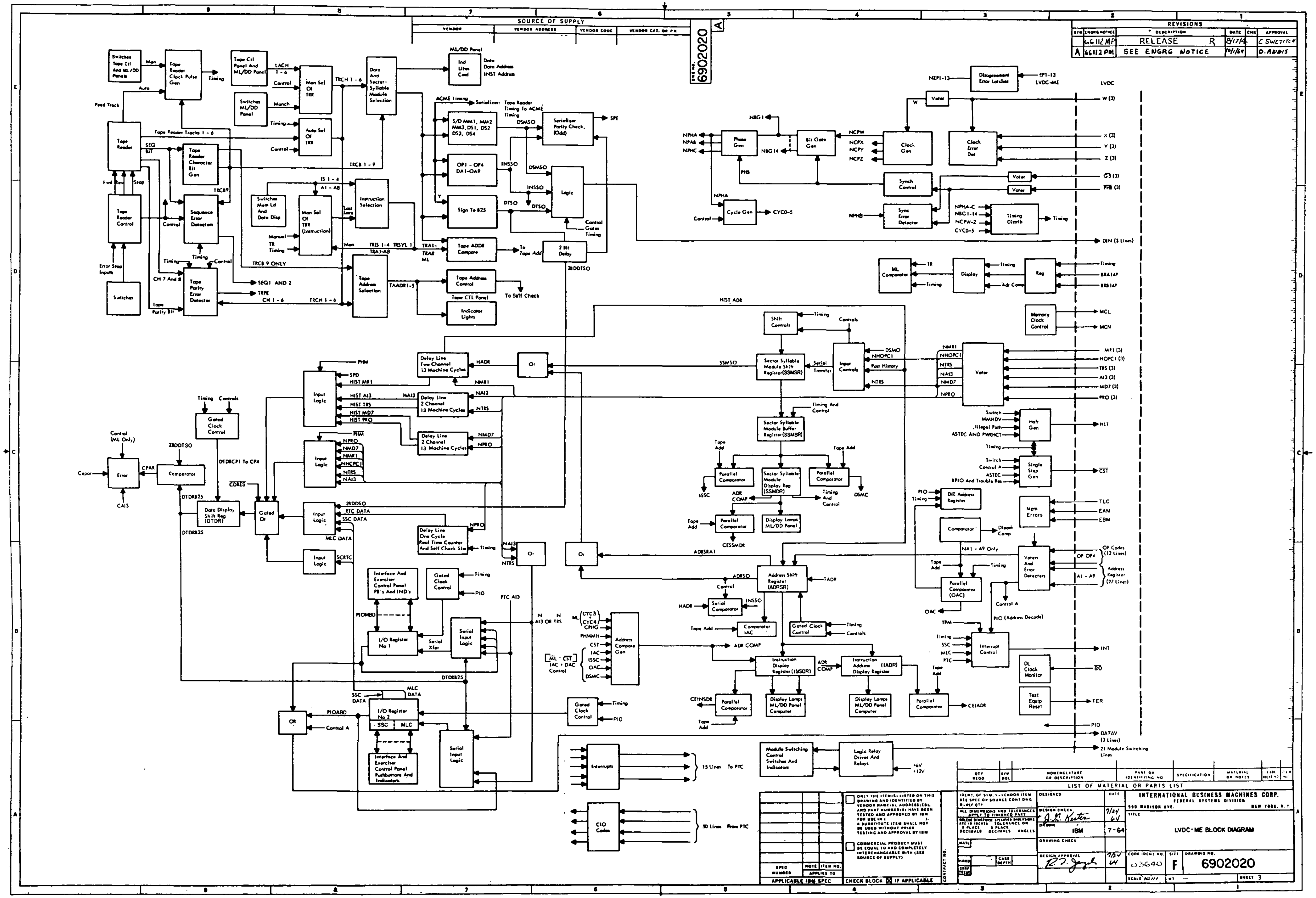


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 3)

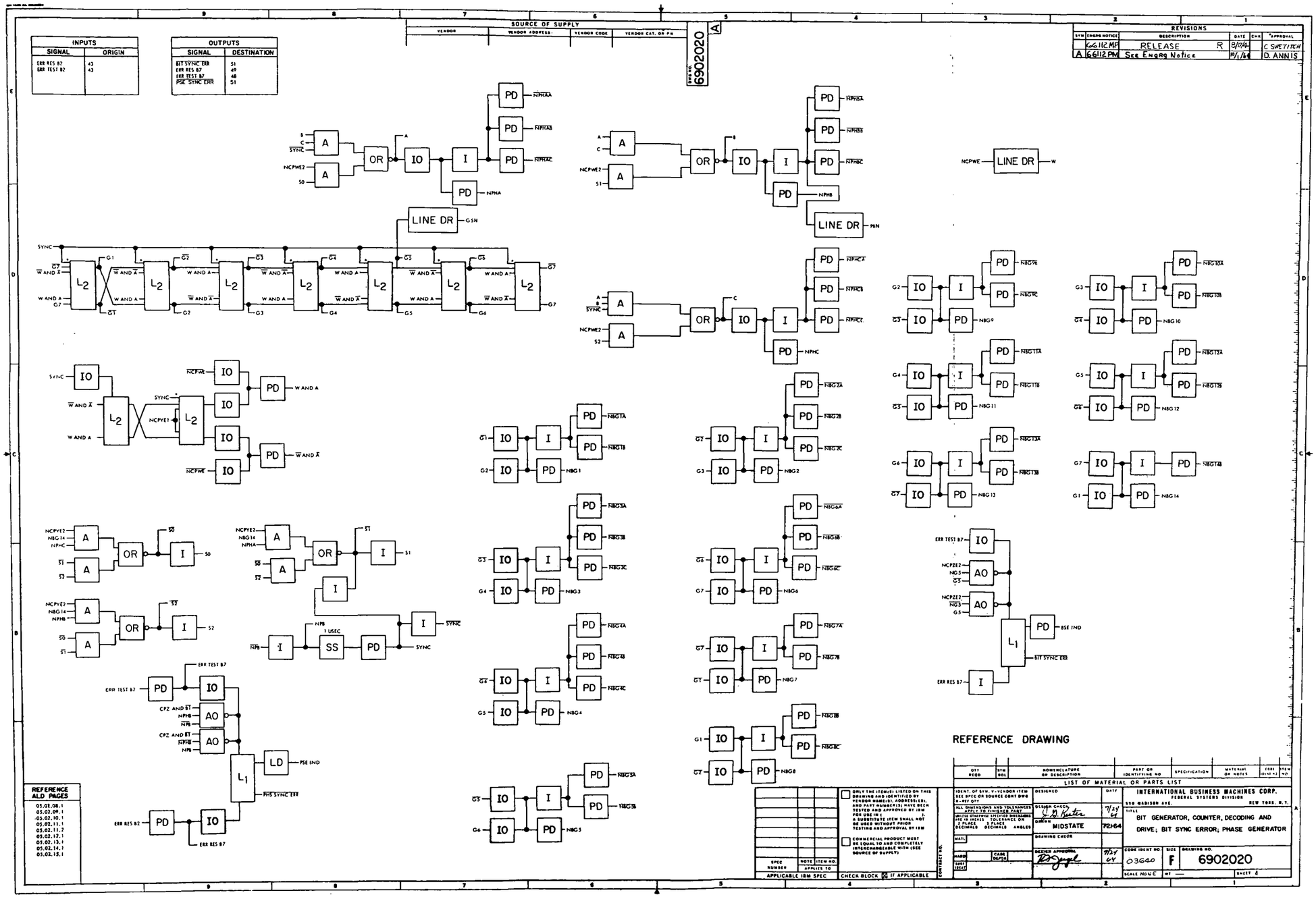


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 4)

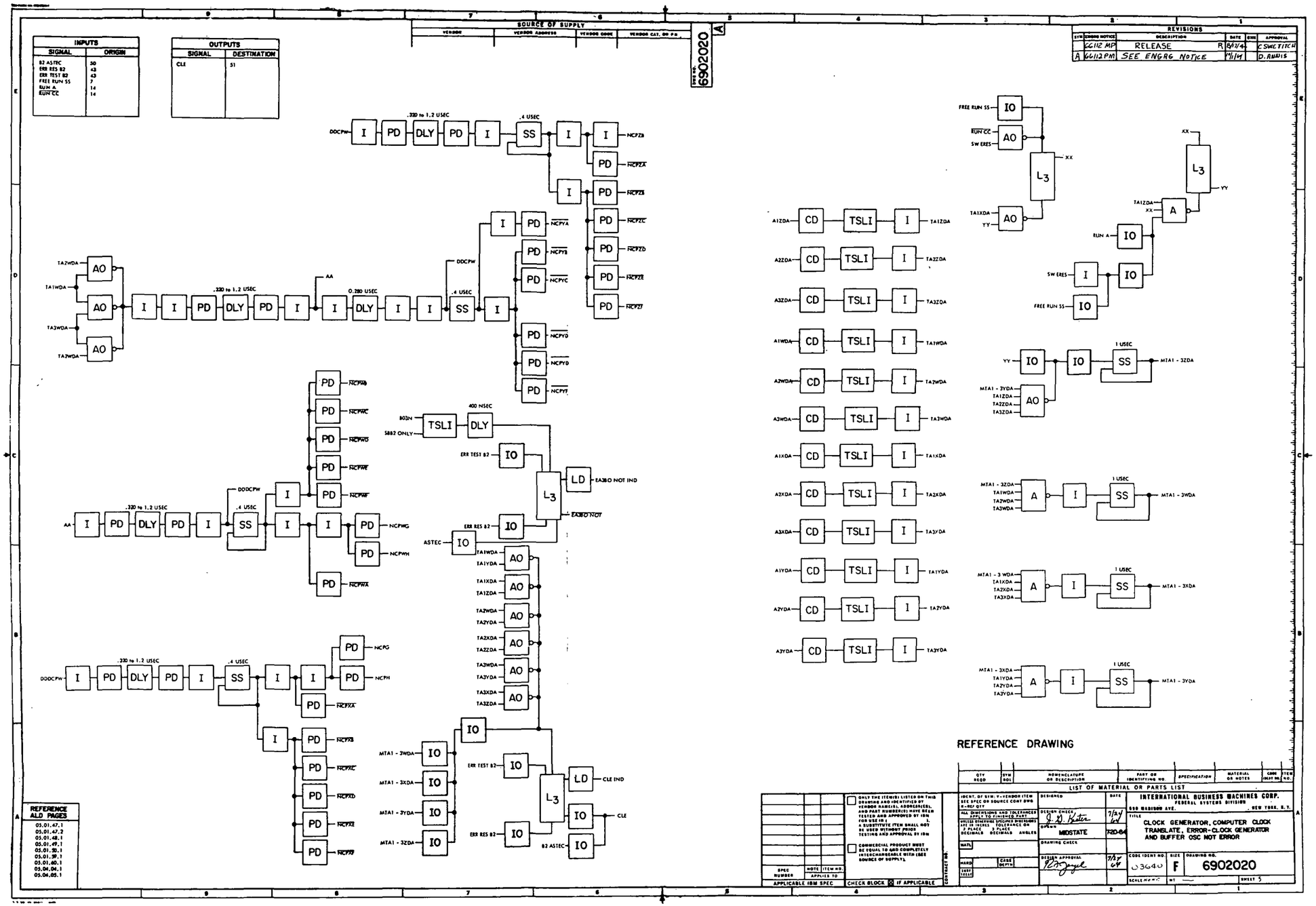


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 5)

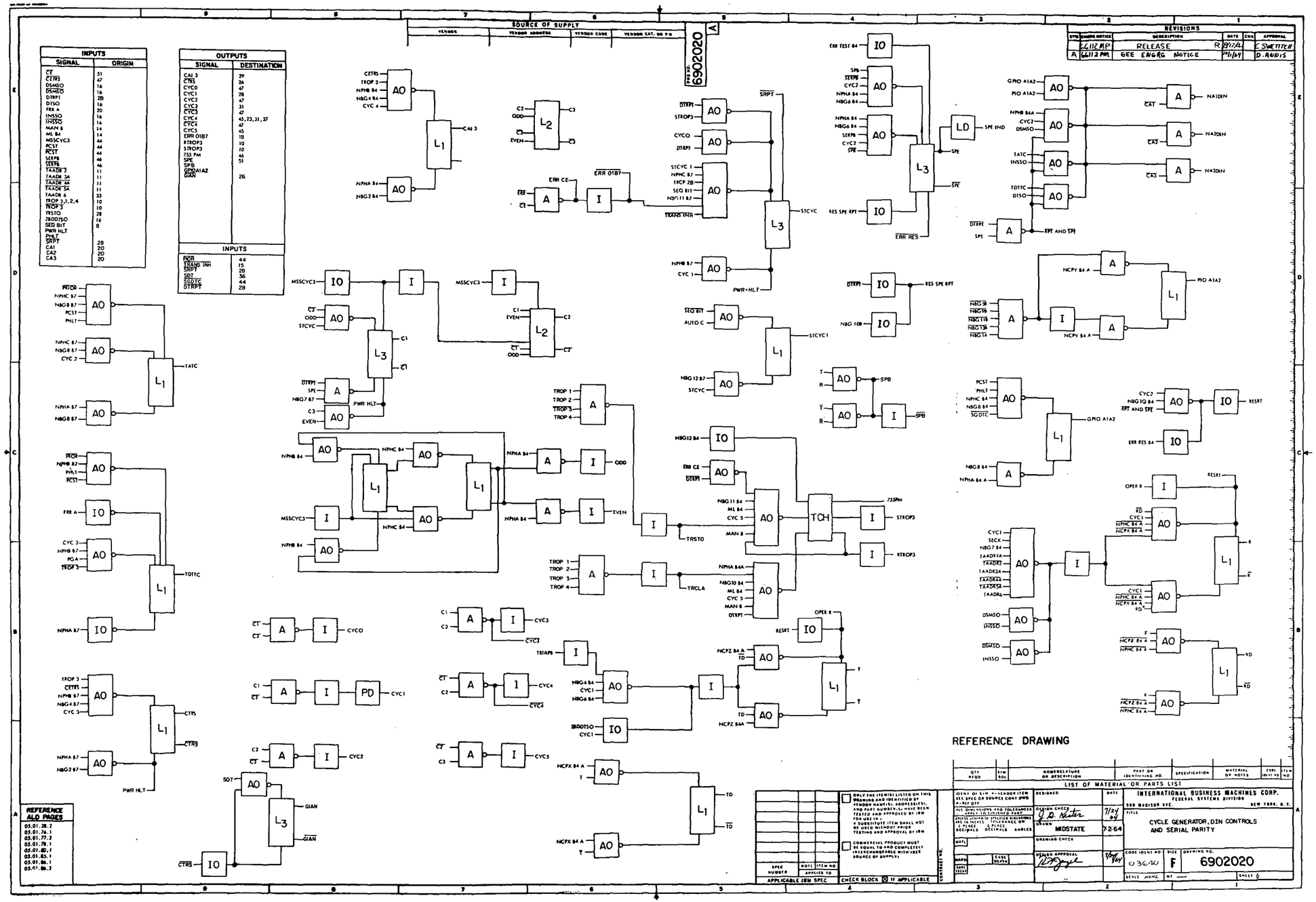


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 6)

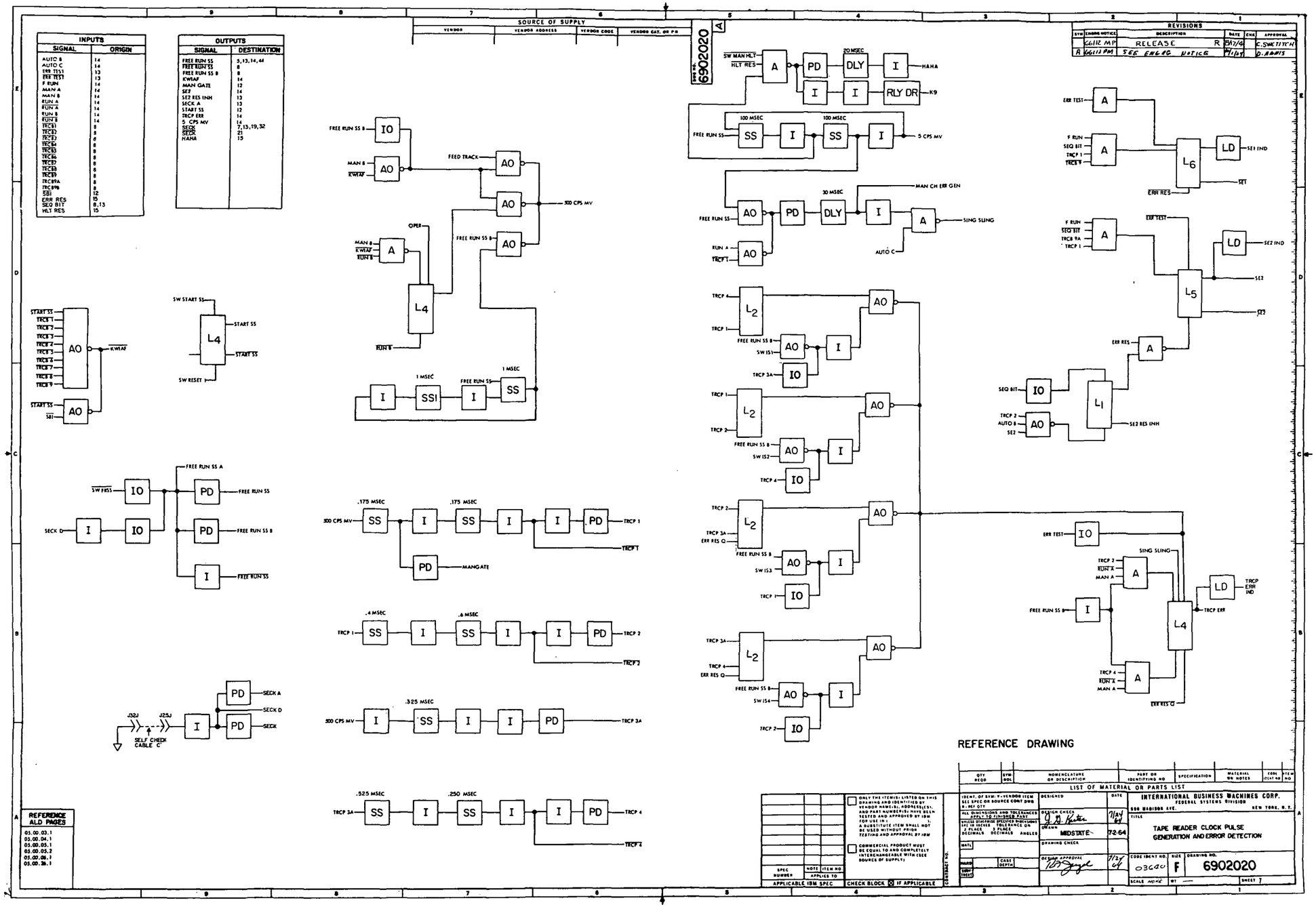


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 7)

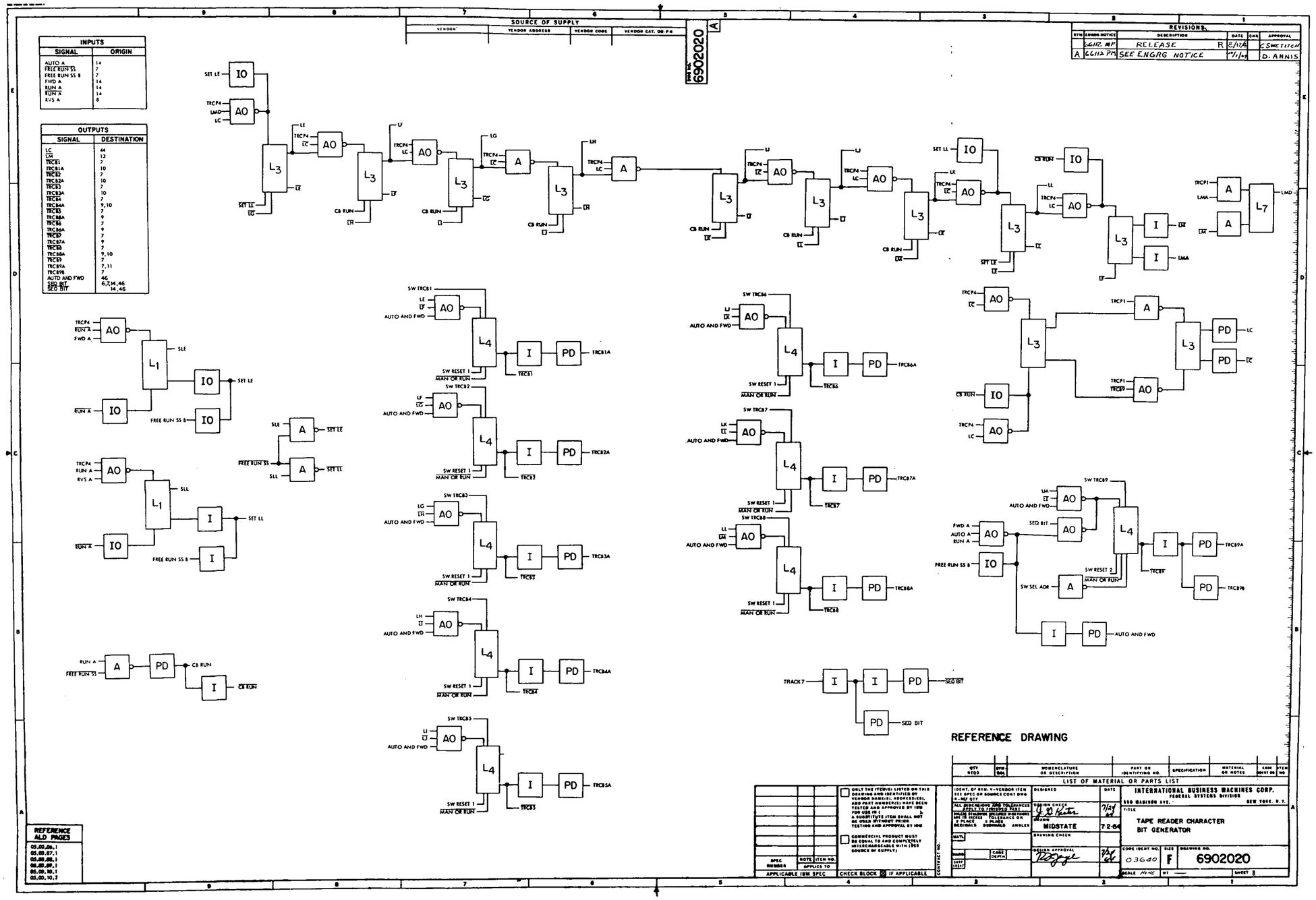


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 8)

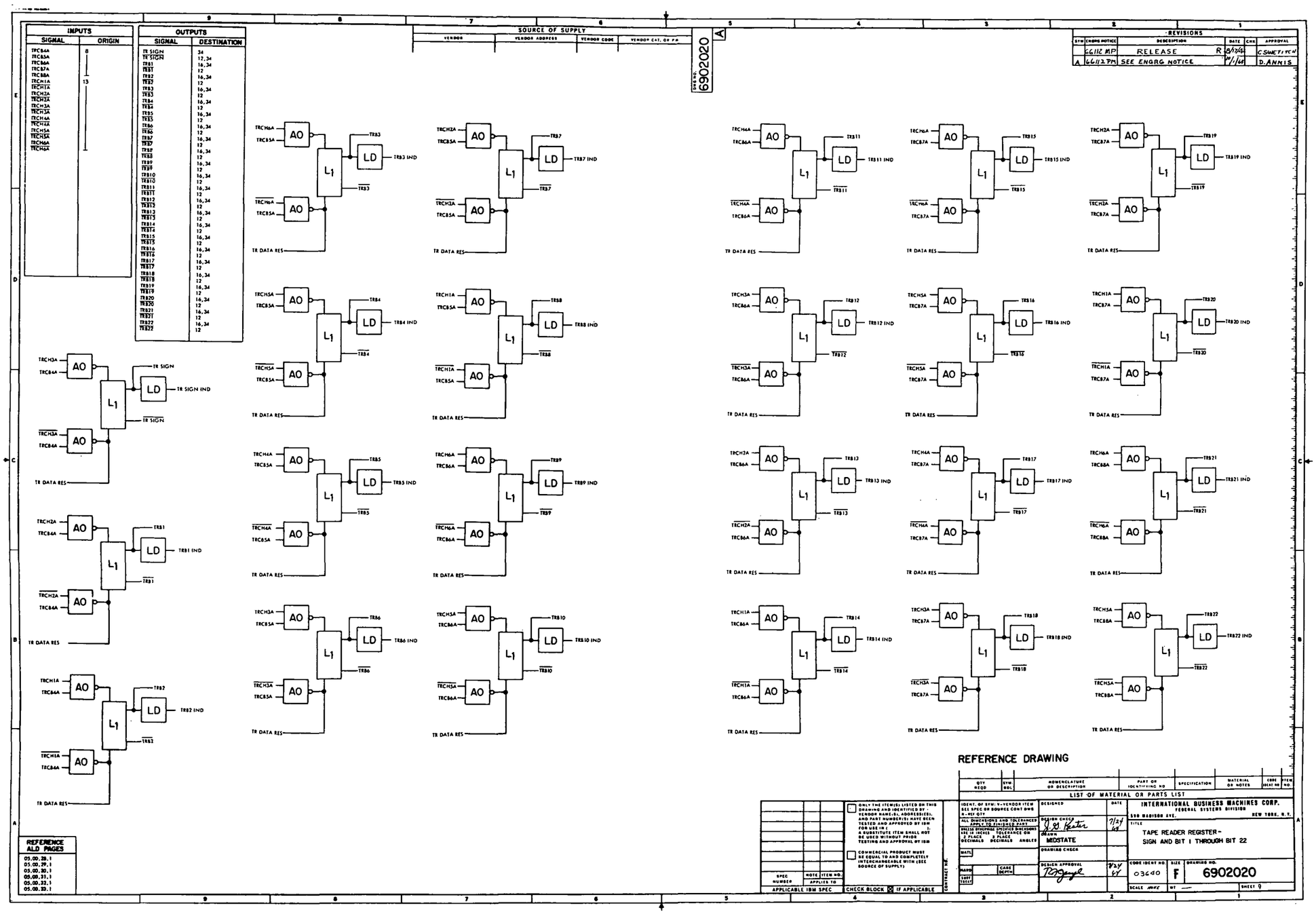


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 9)

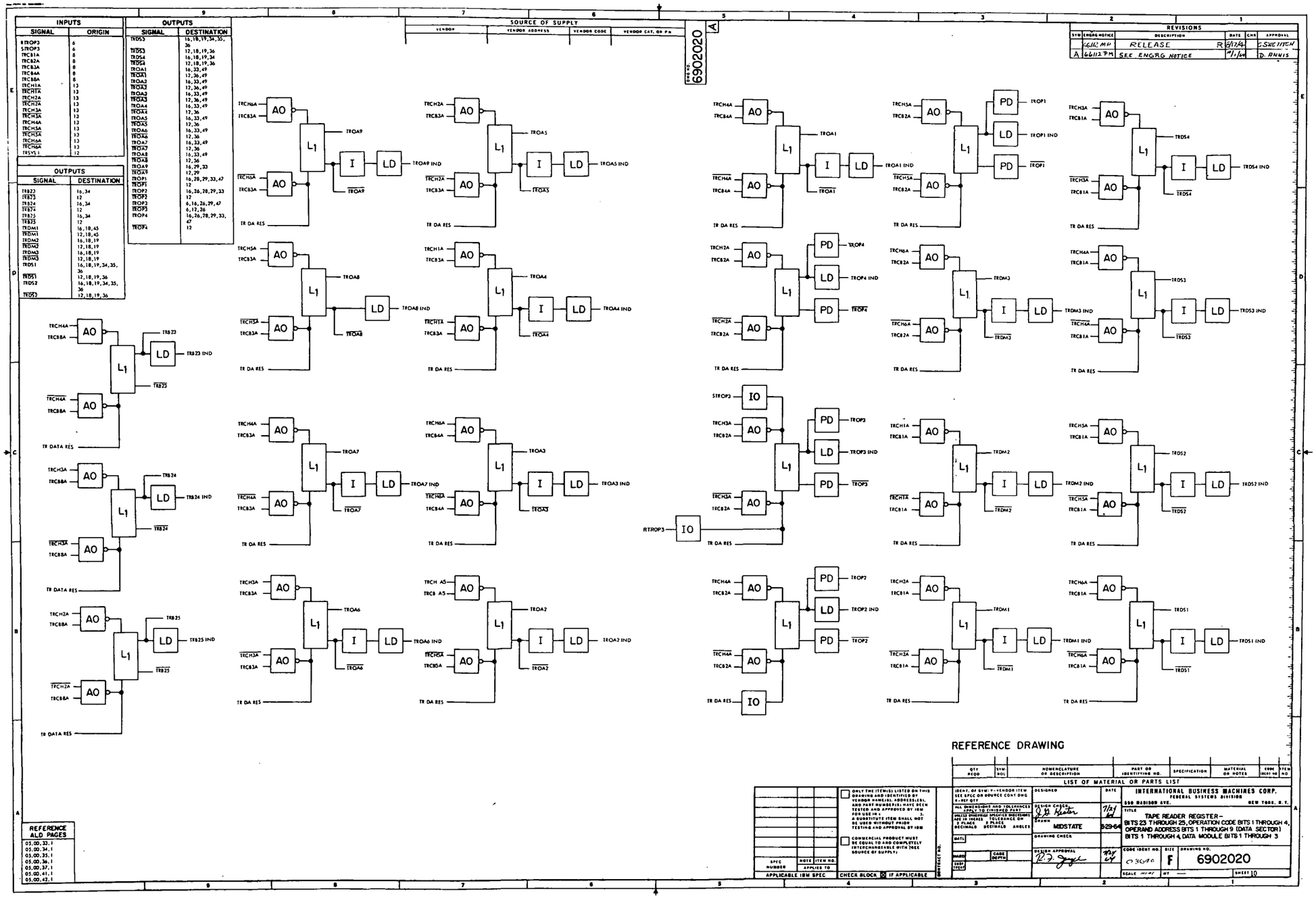


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 10)

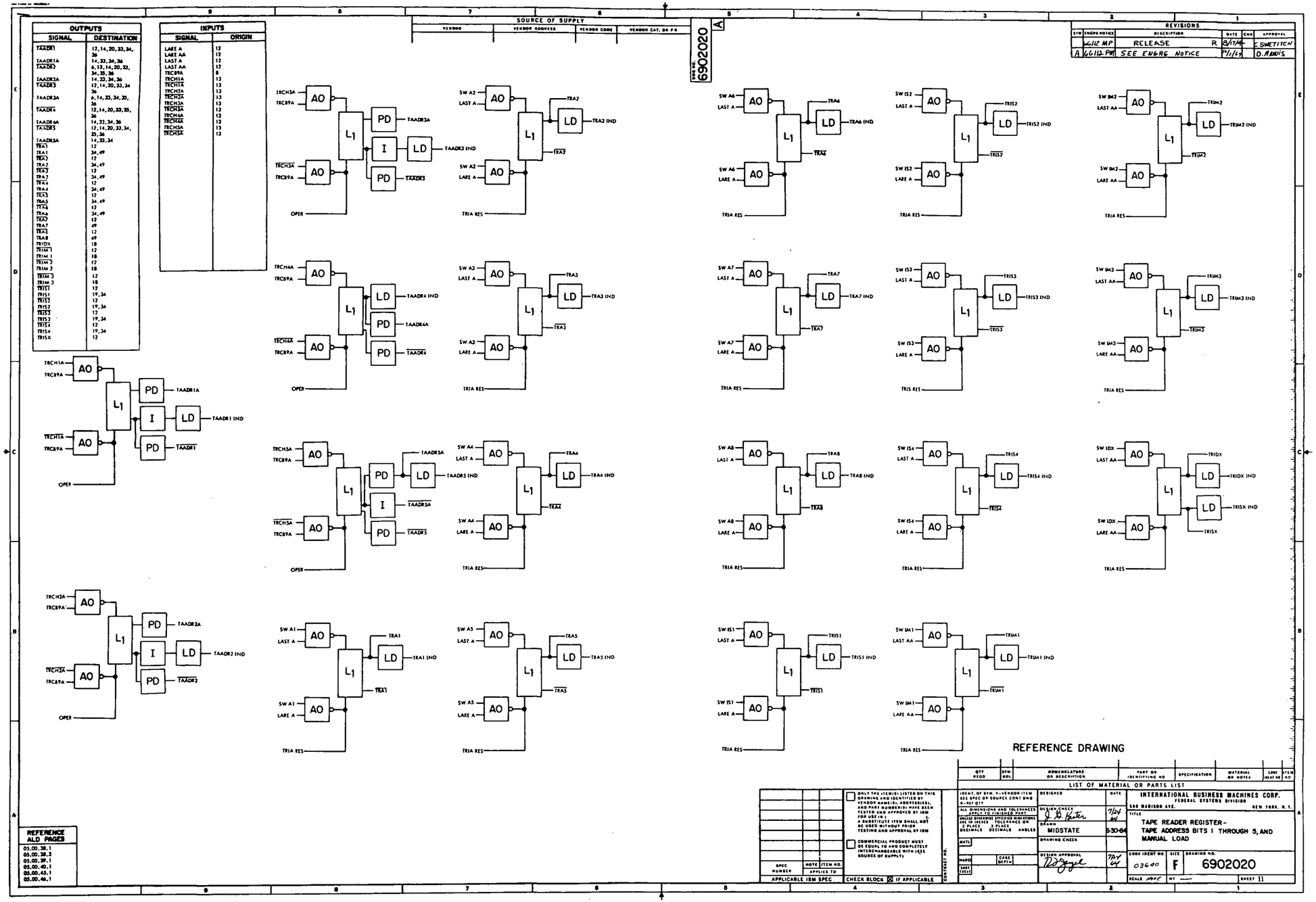


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 11)

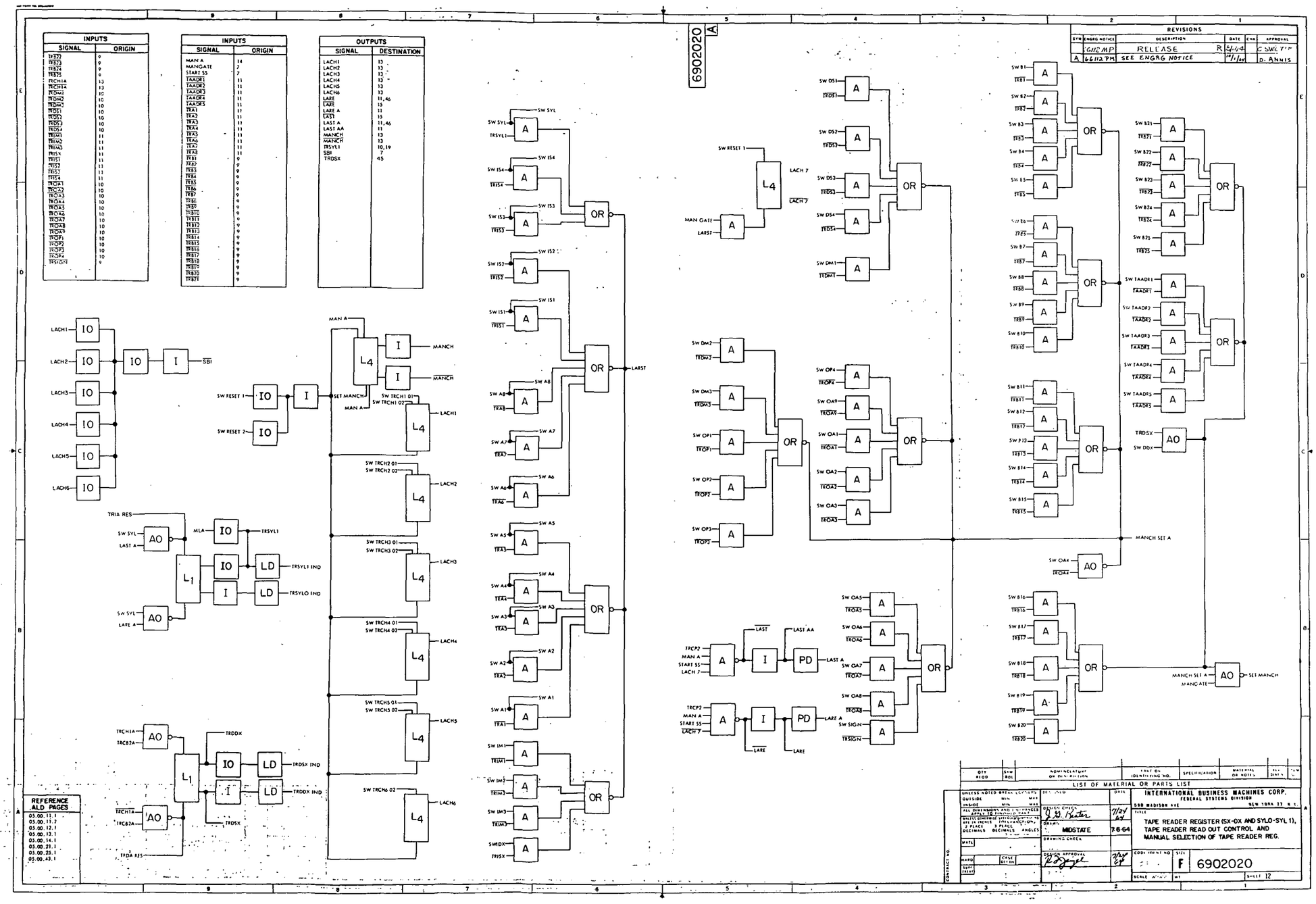


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 12)

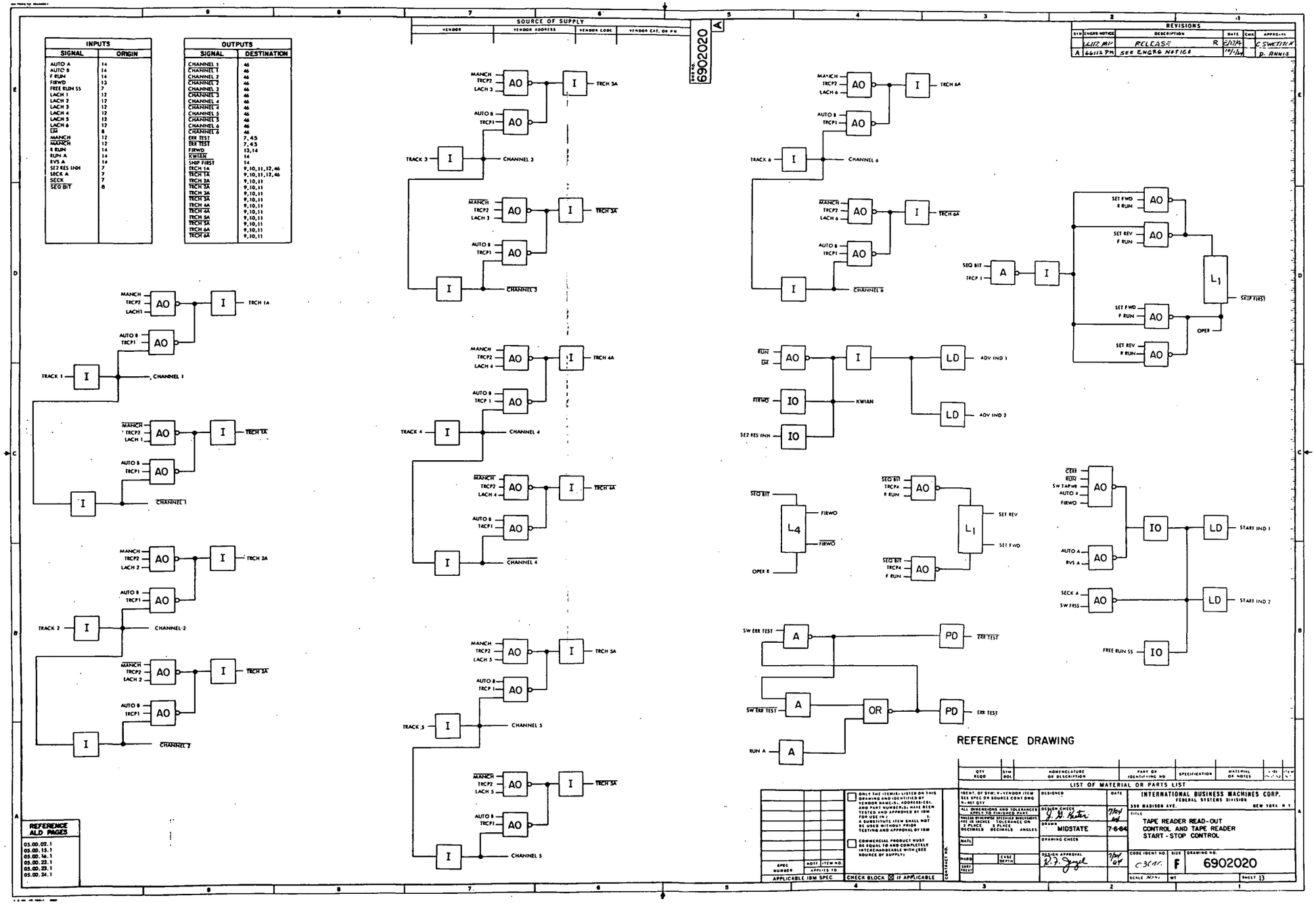


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 13)

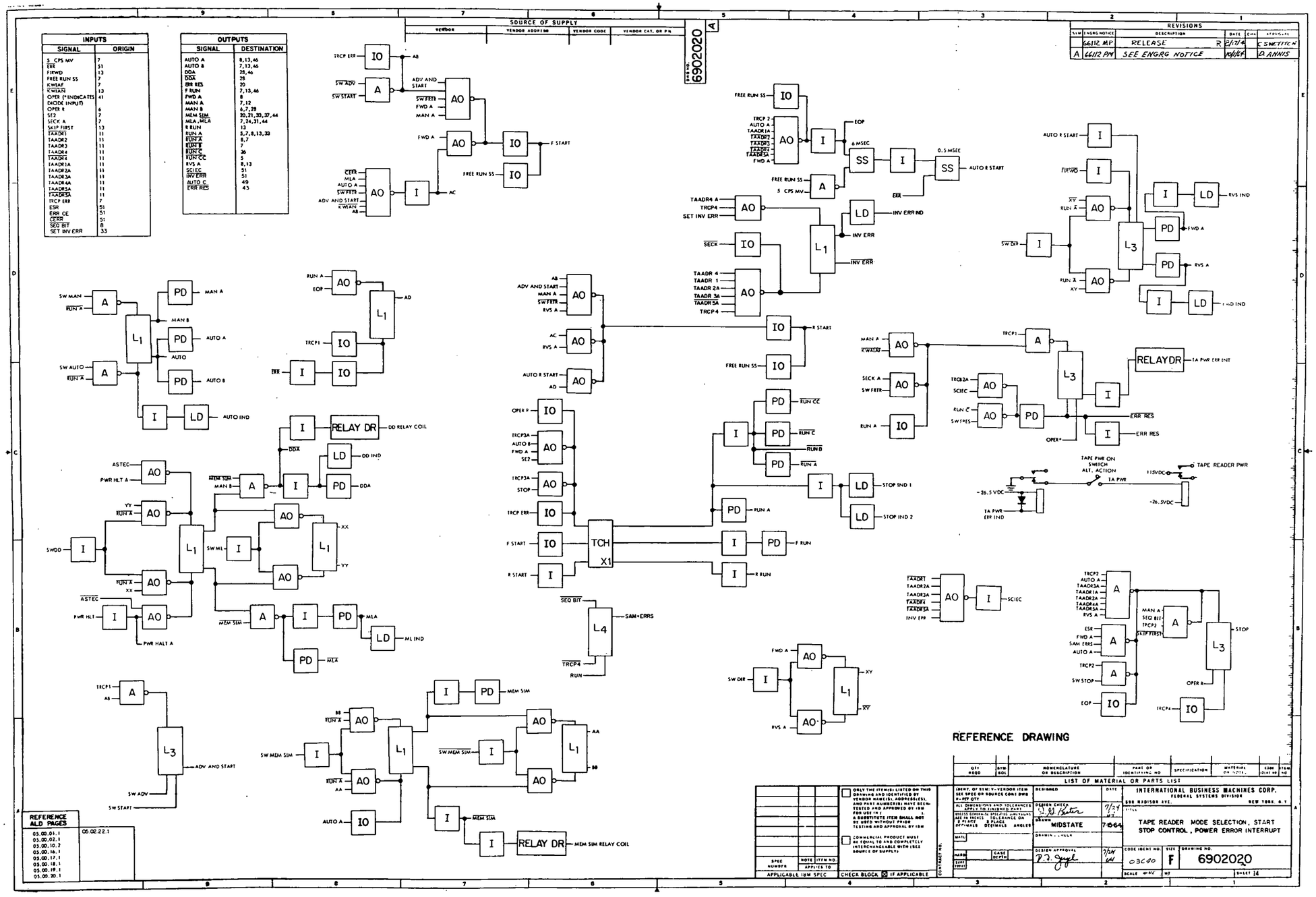


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 14)

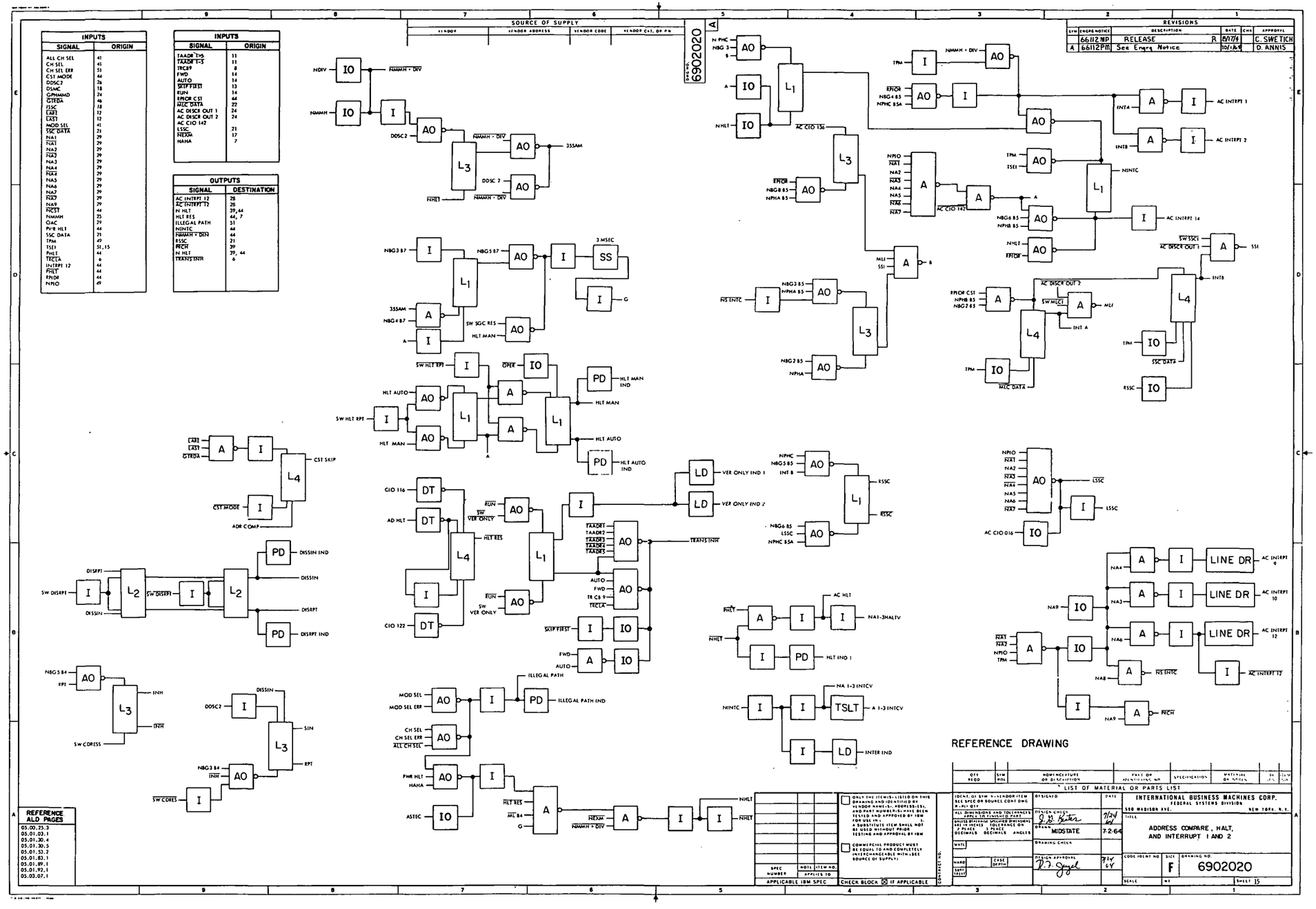


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 15)

INPUTS	
SIGNAL	ORIGIN
CAT0T	49
CA2DT	49
CA3DT	49
TRB1	10
TRB2	10
TRB3	10
TRB4	10
TRB5	10
TRB6	10
TRB7	10
TRB8	10
TRB9	10
TRB10	10
TRB11	10
TRB12	10
TRB13	10
TRB14	10
TRB15	10
TRB16	10
TRB17	10
TRB18	10
TRB19	10
TRB20	10
TRB21	10
TRB22	10
TRB23	10
TRB24	10
TRB25	10
TRDM1	10
TRDM2	10
TRDM3	10
TRDS1	10
TRDS2	10
TRDS3	10
TRDS4	10
TROA1	10
TROA2	10
TROA3	10
TROA4	10
TROA5	10
TROA6	10
TROA7	10
TROA8	10
TROA9	10
TROP1	10
TROP2	10
TROP3	10
TROP4	10
DD A	14
RUN A	14
REGGATE	39

OUTPUTS	
SIGNAL	DESTINATION
DSMSO	6
DSMSO	6
DTSO	6,20
DTSO	6,20
INSSO	6,30
INSSO	6,30
INSSOT	30
2BDDTSO	6,26,23,47
2BDDTSO	23,26,47
DSMSOE	47
DSO	24,26,30
DSO	17,39,50
DSOG	19,30,31

REFERENCE ALD PAGES
05.01.69.1
05.01.70.1
05.01.71.1
05.01.72.1
05.01.73.1

REFERENCE DRAWING

SYM	ENGRG NOTICE	REVISIONS DESCRIPTION	DATE	CHK	APPROVAL
		RELEASE R	7/24/64		E. SWEETMAN
A	6/12 PM	SEE ENGRG NOTICE	10/1/64		O. AGNES

SOURCE OF SUPPLY: VENDOR | VENDOR ADDRESS | VENDOR CODE | VENDOR CAT. OR P.N.

DRAWING 6902020

QTY REQD	SYM DES	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION

LIST OF MATERIAL OR PARTS LIST

SPEC NUMBER	NOTE APPLIES TO	ITEM NO

APPLICABLE IBM SPEC

CHECK BLOCK ☒ IF APPLICABLE

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CONTRACT NO.

DESIGNED — DATE 7/24/64

DESIGN CHECK U. D. Kester

DRAWN MIDSTATE 7-2064

DRAWING CHECK

DESIGN APPROVAL W. J. Joyce 7/24/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK N.Y.

TITLE: SERIALIZER AND SELF CHECK HOPCI SIMULATION

CODE IDENT NO — SIZE F — DRAWING NO. 6902020

SCALE — WT —

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 16)

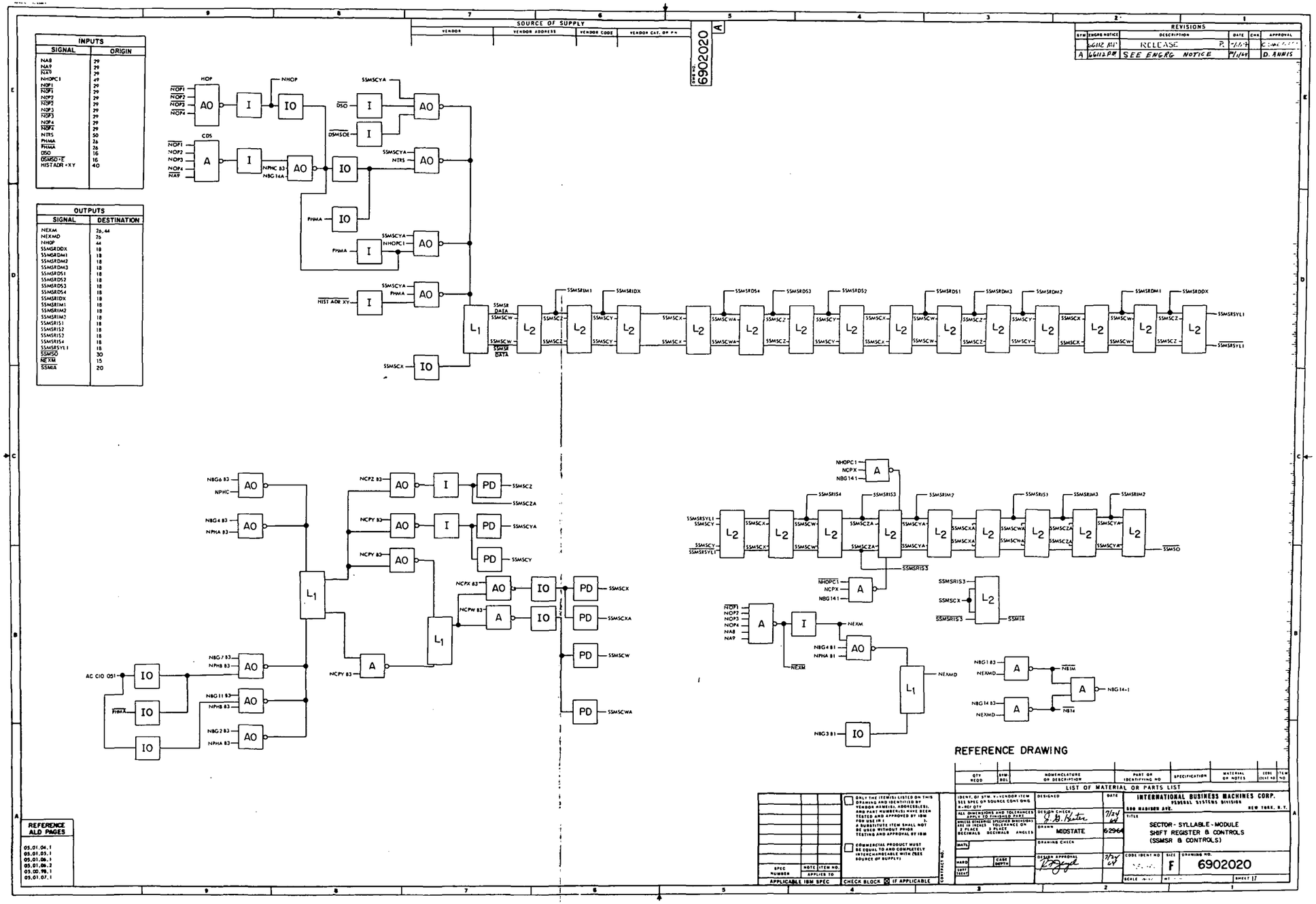


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 17)

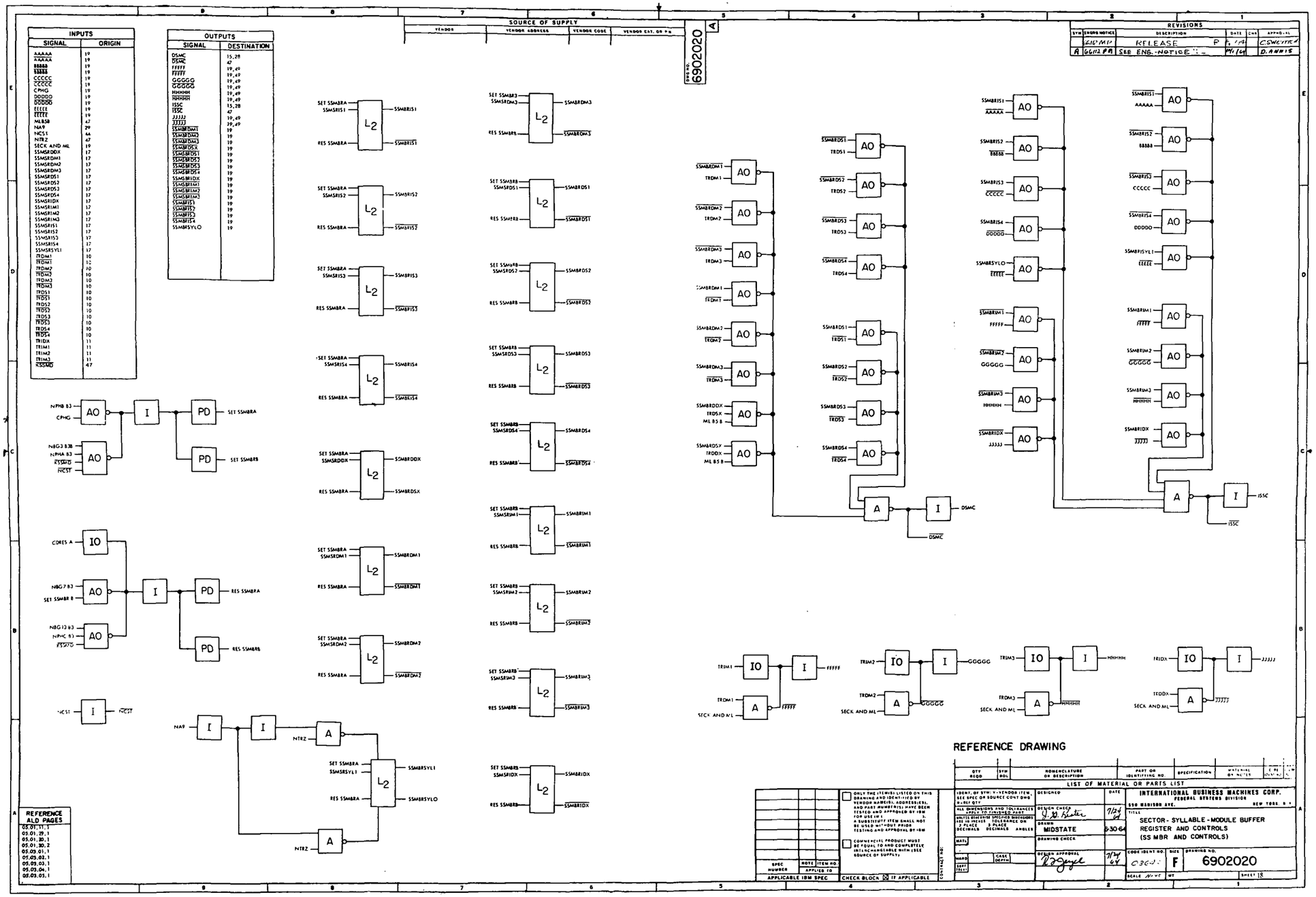


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 18)

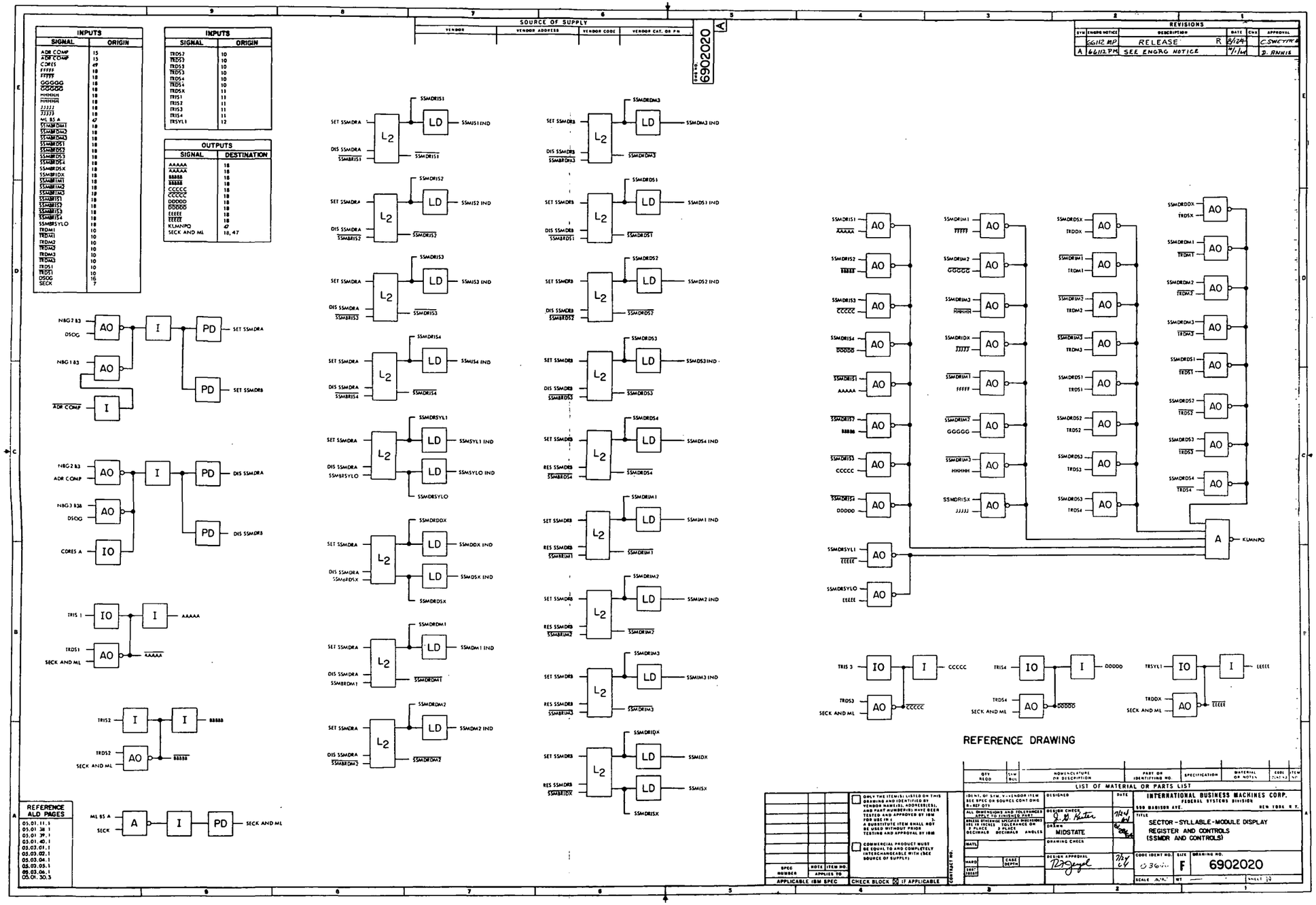


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 19)

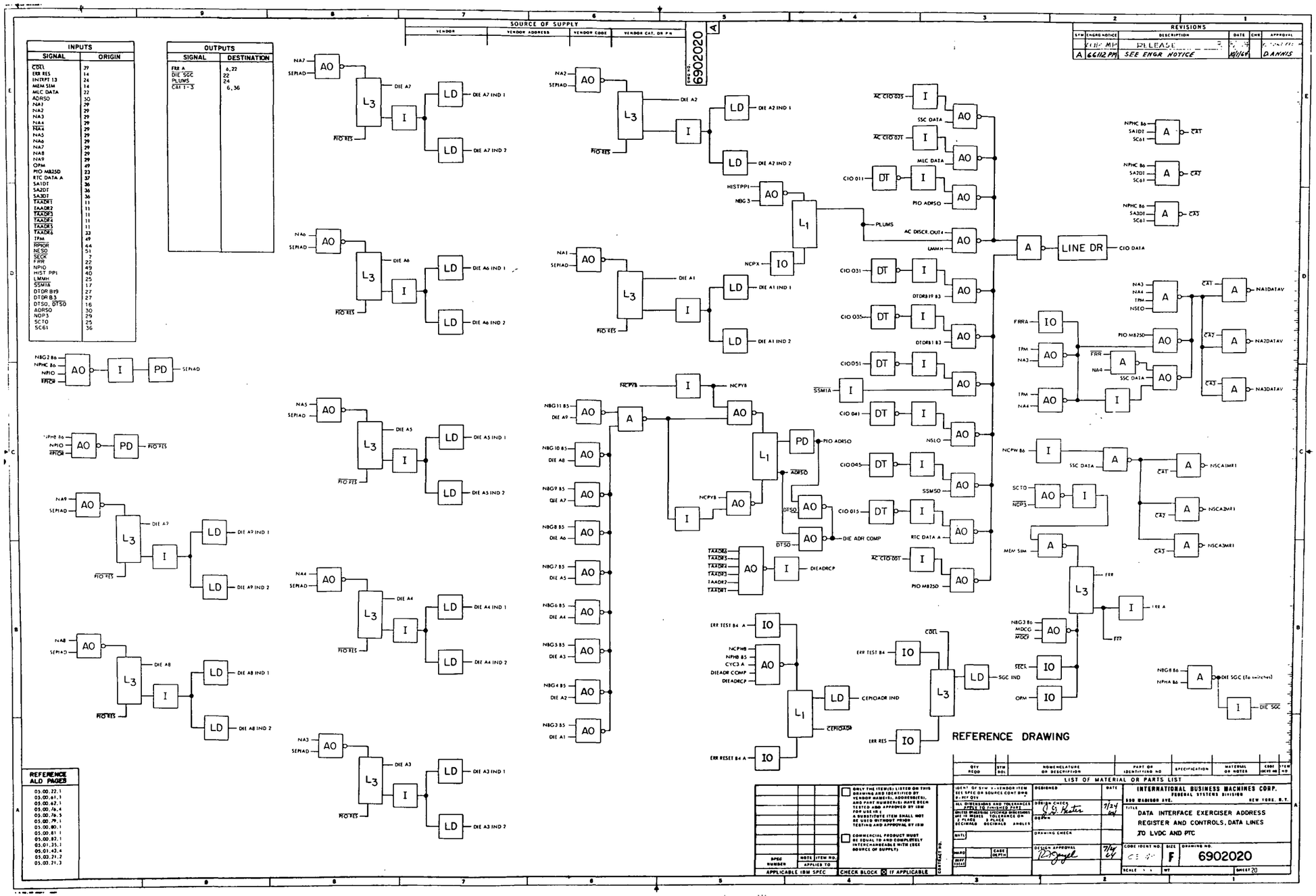


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 20)

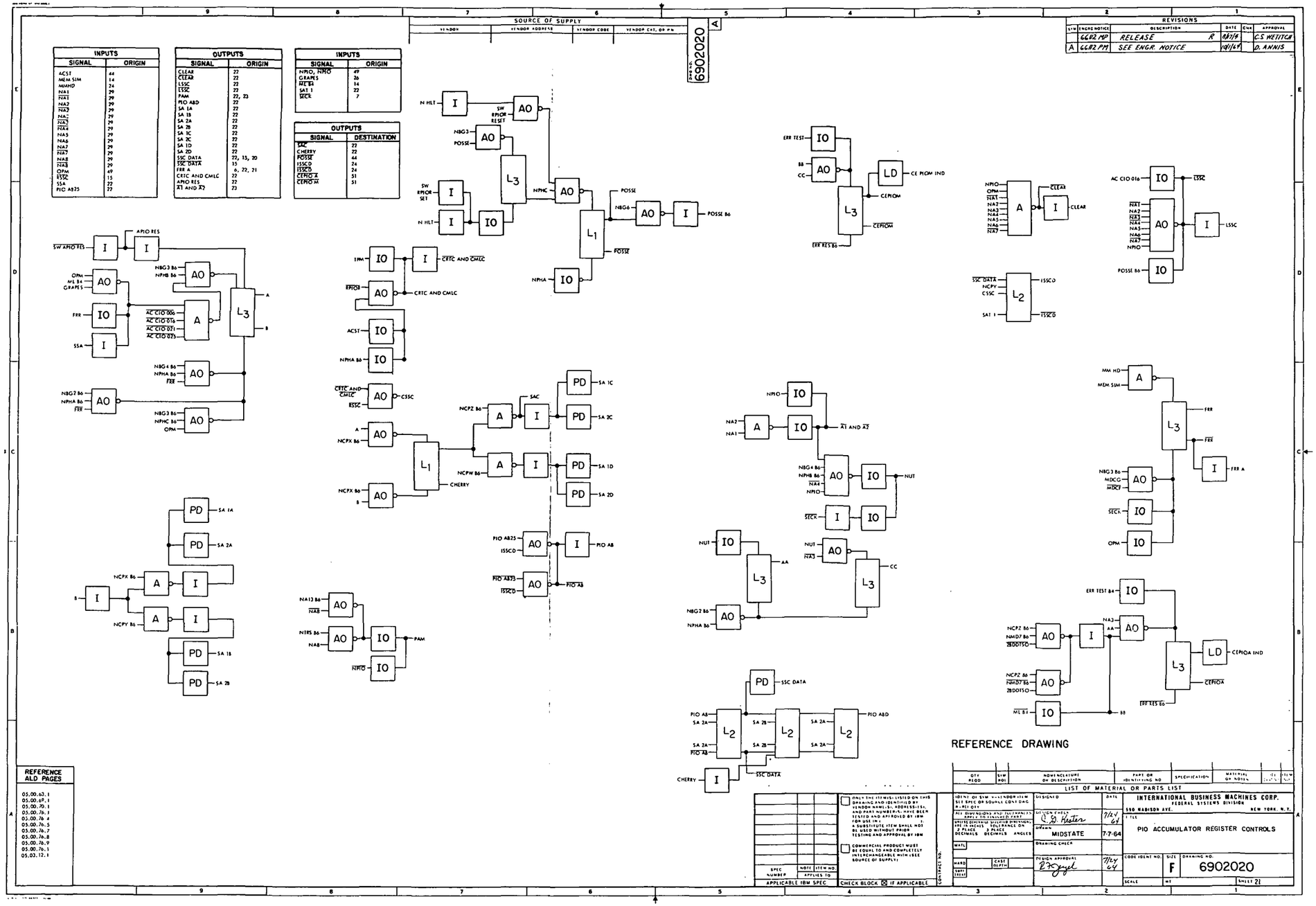


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 21)

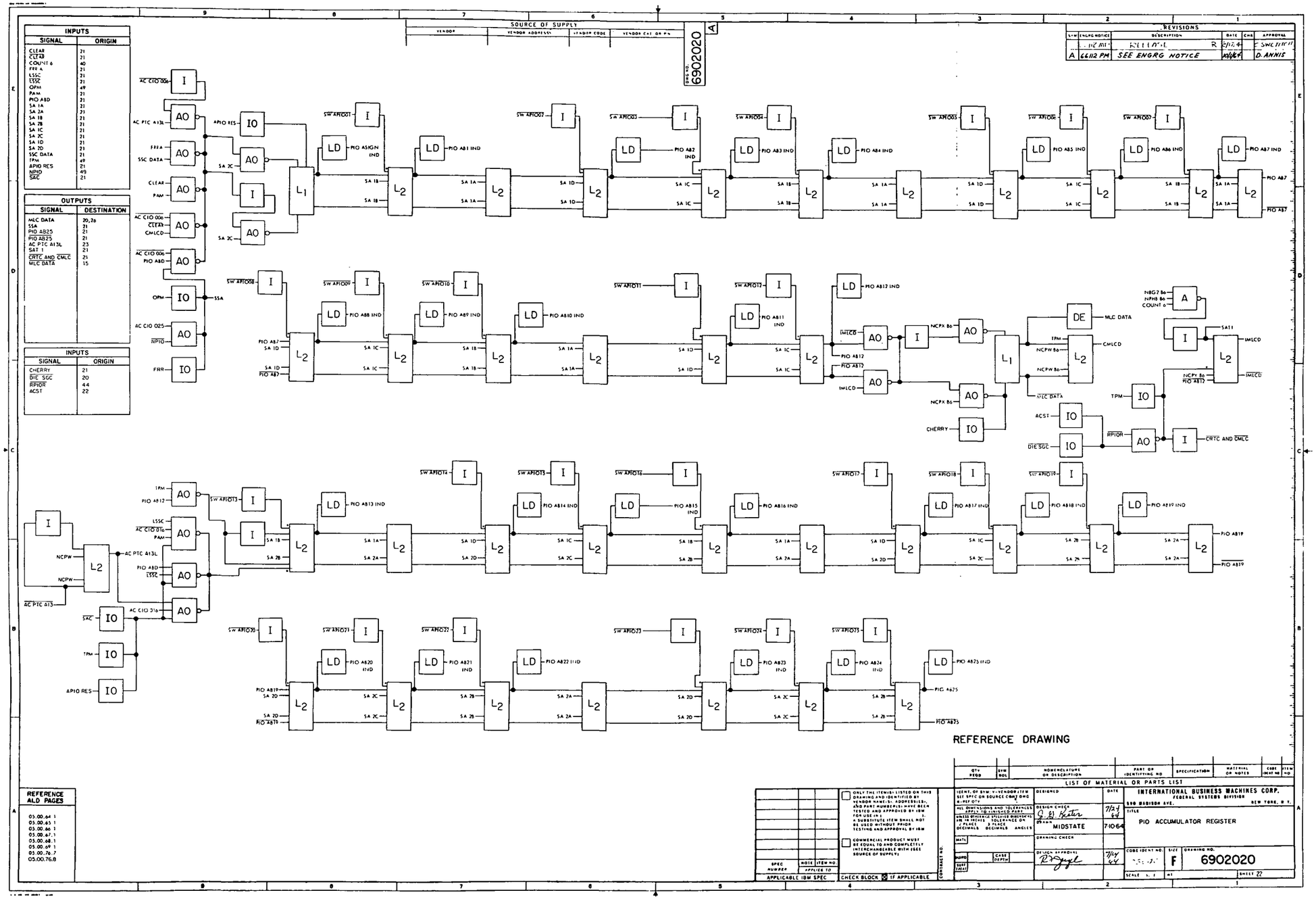


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 22)

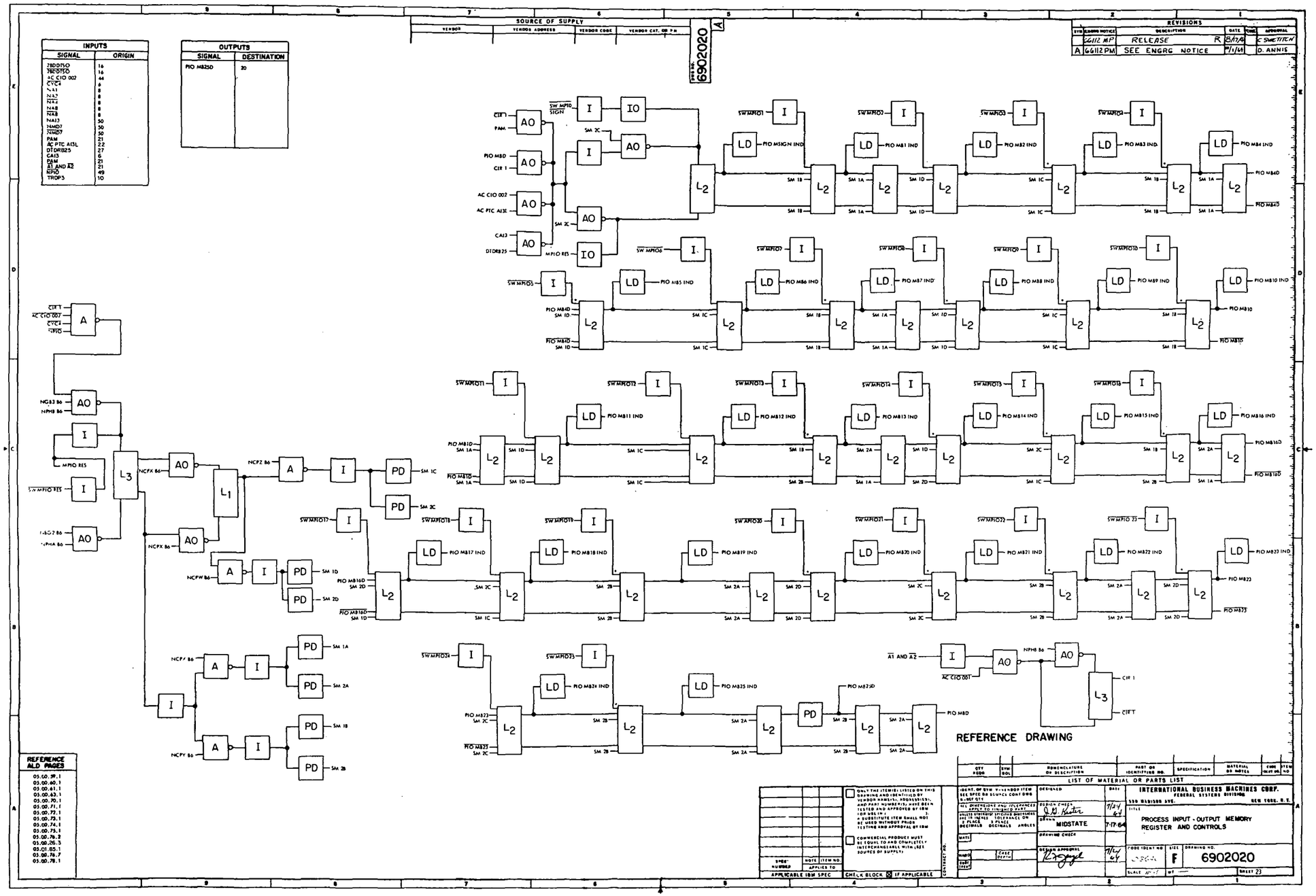


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 23)

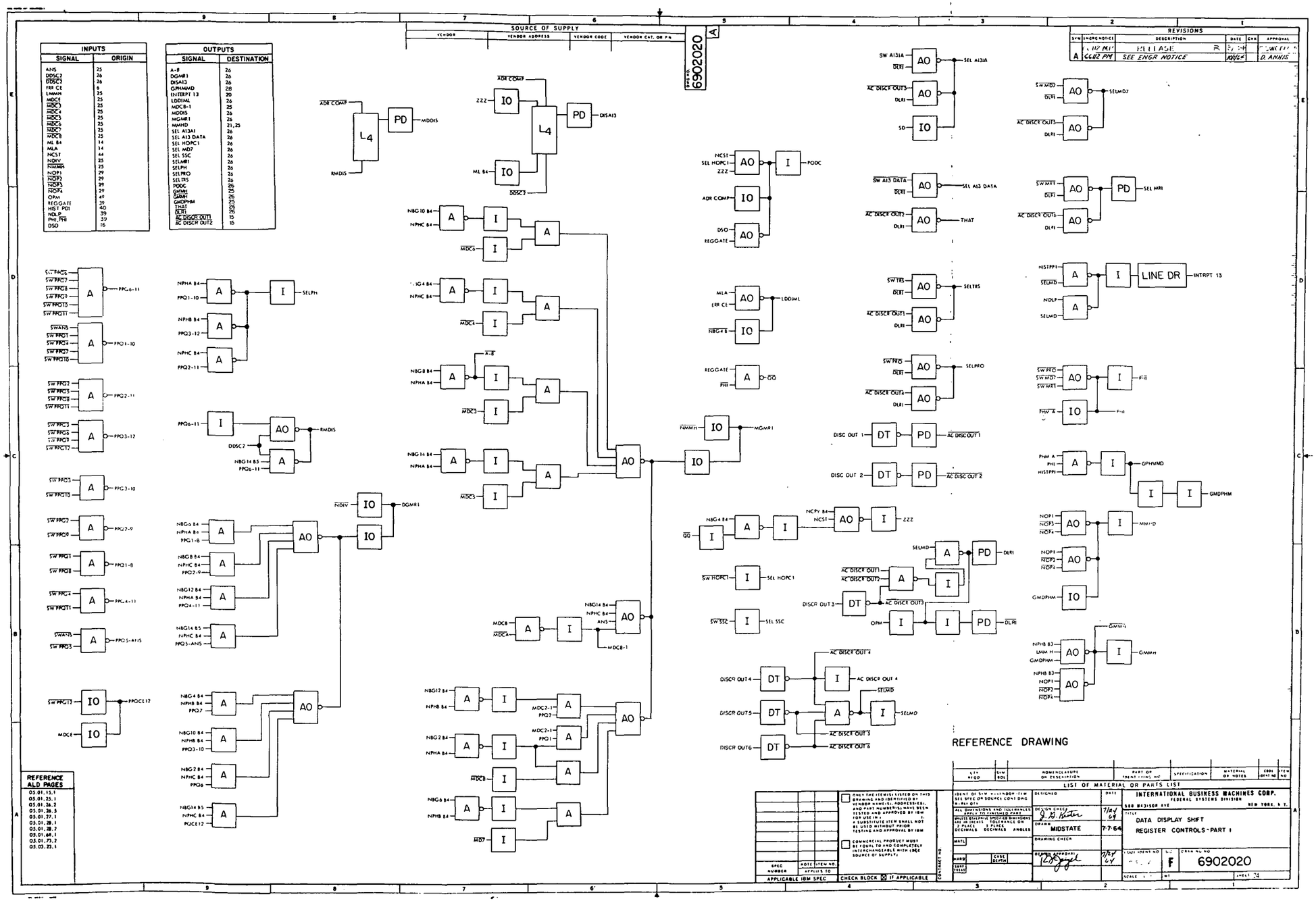


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 24)

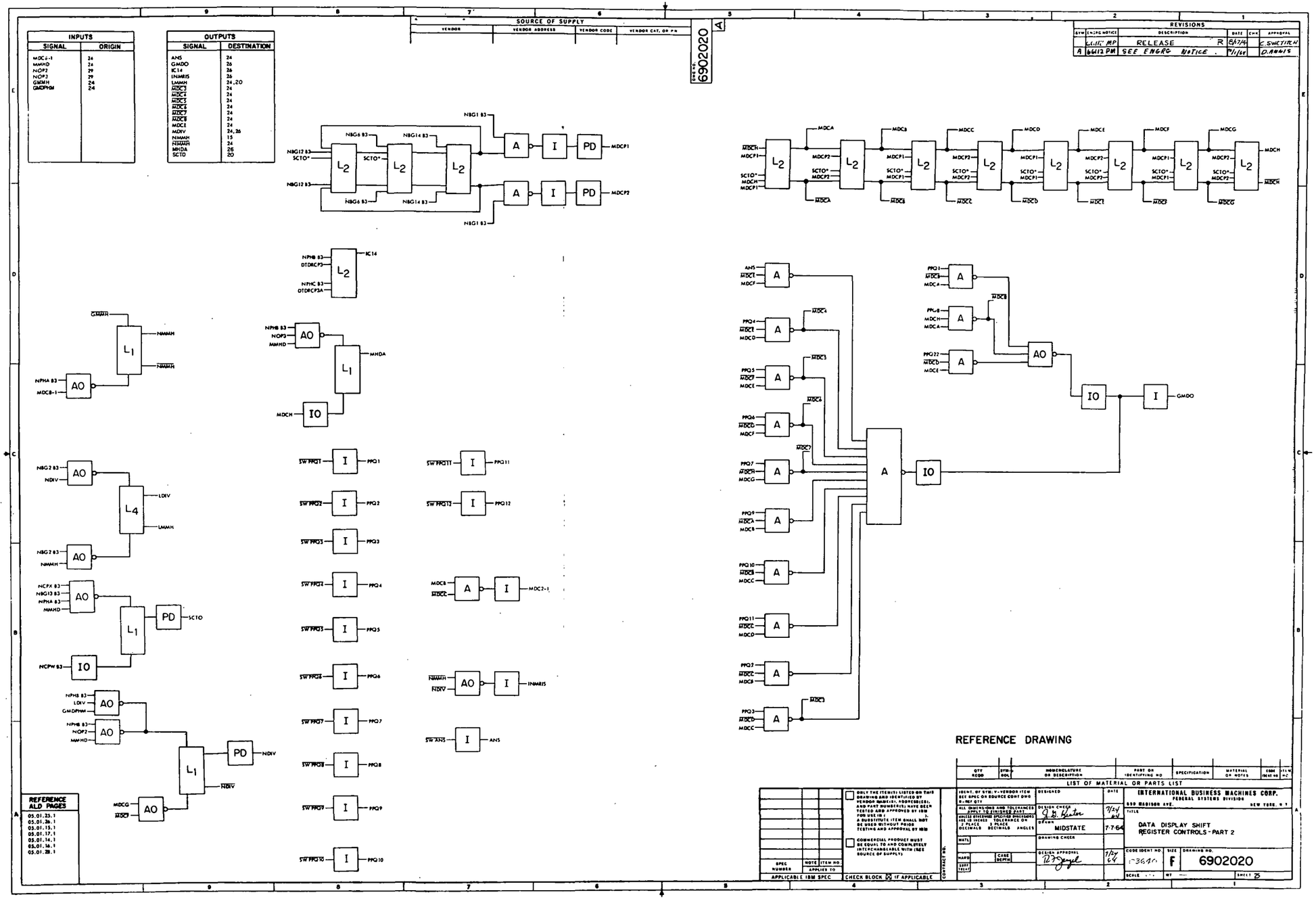


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 25)

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 26)

INPUTS	
SIGNAL	ORIGIN
DOSC1	26
DOSC2	26
DTDR DATA	26

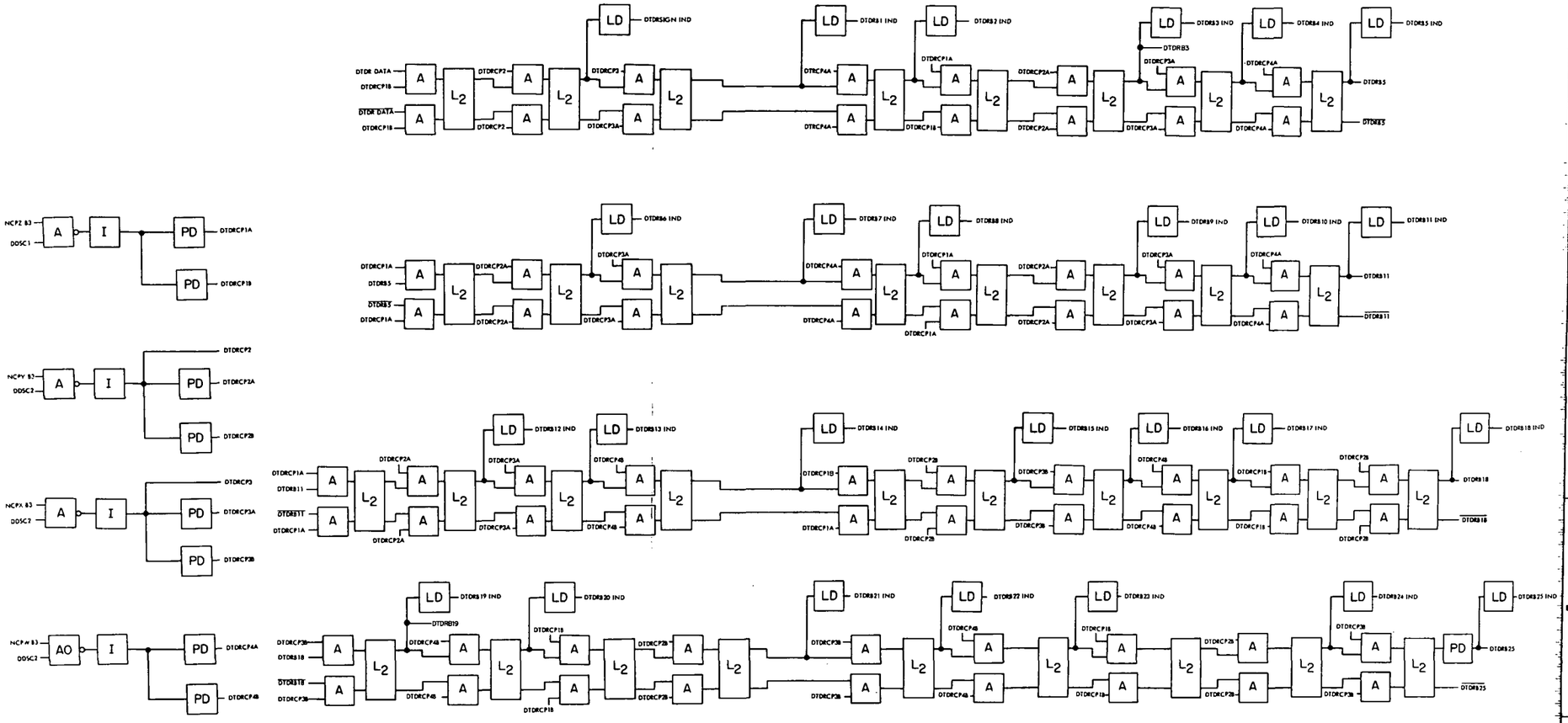
OUTPUTS	
SIGNAL	DESTINATION
DTDR835	26,23
DTDR835	26
DTDR819	20
DTDR83	20

SOURCE OF SUPPLY

VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

DRWG 6902020 A

REVISIONS					
SYM	ENGR NOTICE	DESCRIPTION		DATE	CHK	APPROVAL
	66112 MP	RELEASE	R	8/1/64		C.SWETICH
A	66112 PM	SEE ENGRG NOTICE		9/1/64		D.HARRIS



REFERENCE ALD PAGES

05.01.13.1
05.01.14.1
05.01.30.1
05.01.31.1
05.01.32.1
05.01.33.1
05.01.34.1

REFERENCE DRAWING

LIST OF MATERIAL OR PARTS LIST

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO

IDENT. OF SYM: V=VENDOR ITEM SEE SPEC OR SOURCE CONT DWG
R=REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE NOMINAL. TOLERANCE ON 2 PLACE DECIMALS ±.01 3 PLACE DECIMALS ±.005 ANGLES ±1°

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN _____. SUCH ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT WHICH IS EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH IBM SOURCE OF SUPPLY)

SPEC NUMBER | NOTE | ITEM NO. APPLIES TO

APPLICABLE IBM SPEC

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

DESIGNED		DATE 7/24/64
DESIGN CHECK		
DRAWN	MIDSTATE 7264	
DRAWING CHECK		
MATL		
HARD / SOFT	CASE DEPTH	
DESIGN APPROVAL		7/24/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK, N.Y.

TITLE: DATA DISPLAY REGISTER

CODE IDENT NO 03540 | SIZE F | DRAWING NO. 6902020

SCALE NONE | WT | SHEET 27

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 27)

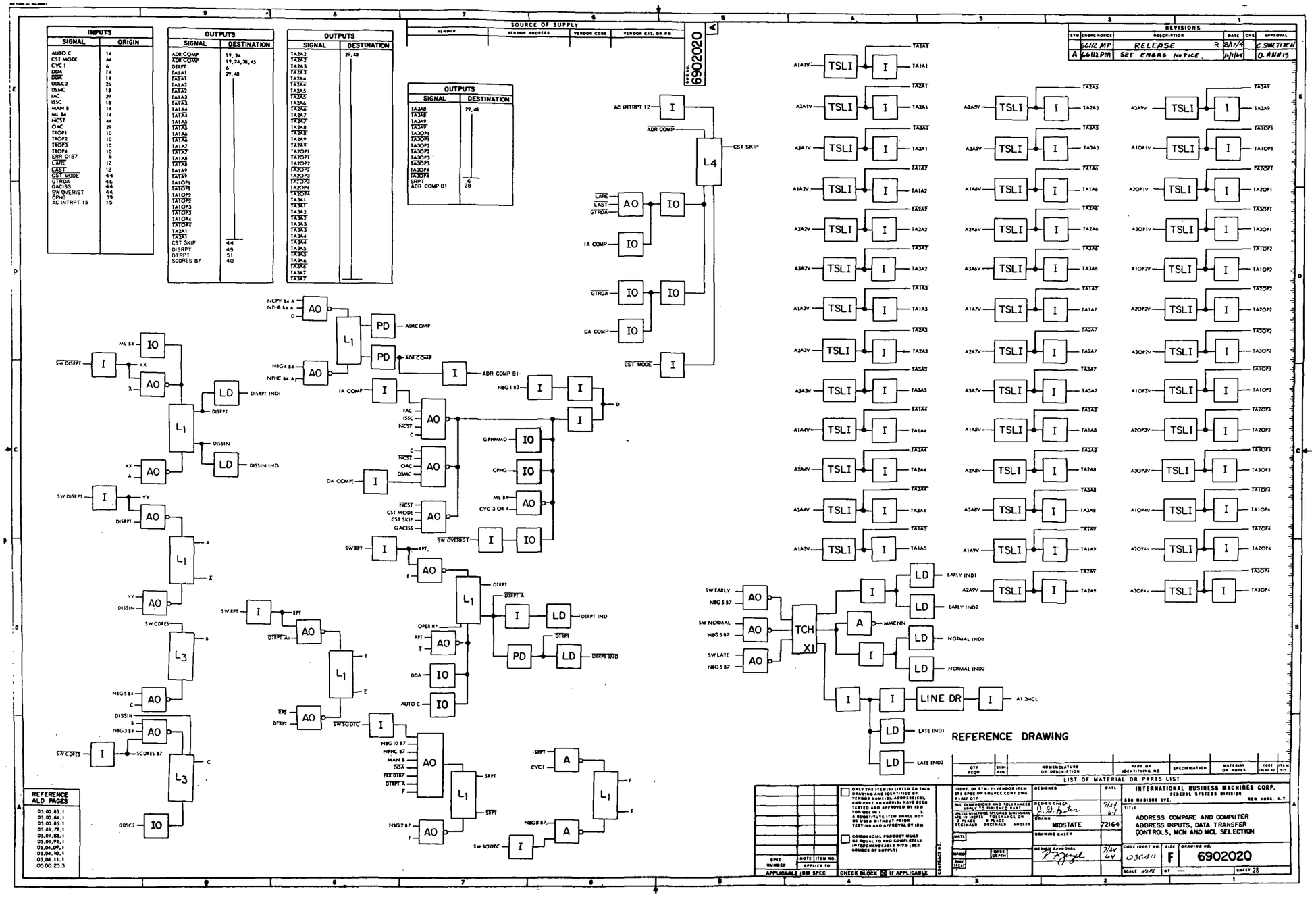


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 28)

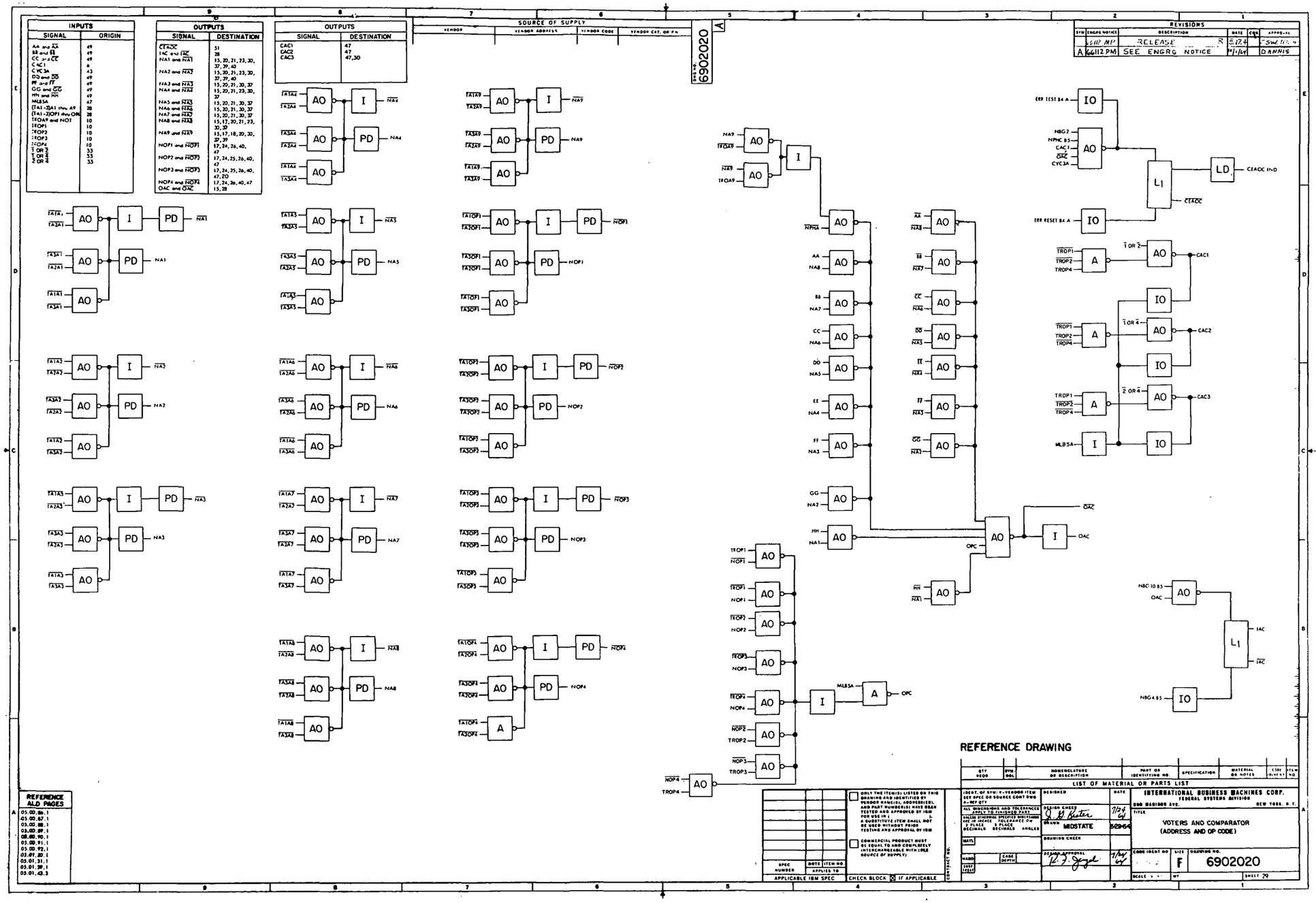


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 29)

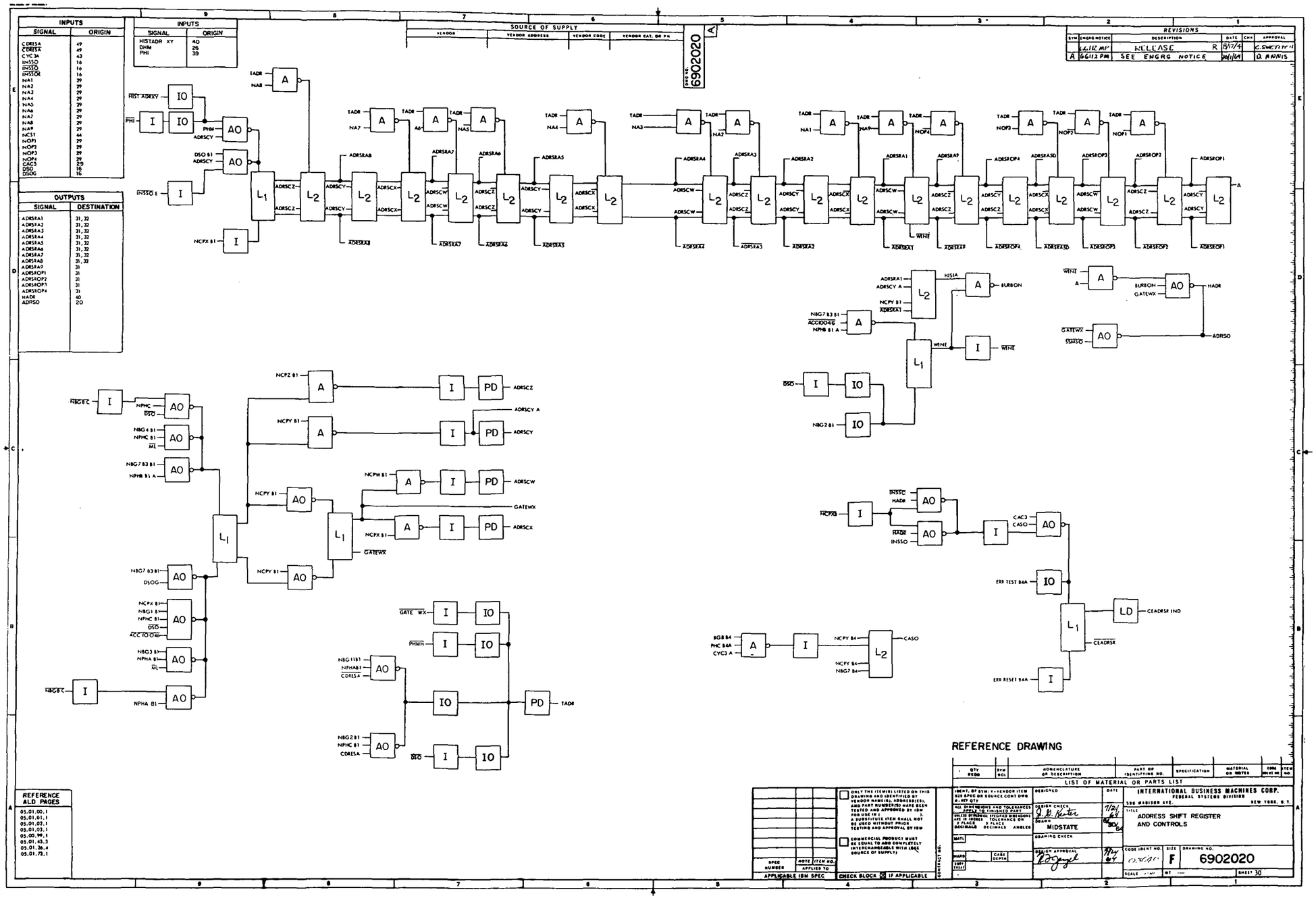


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 30)

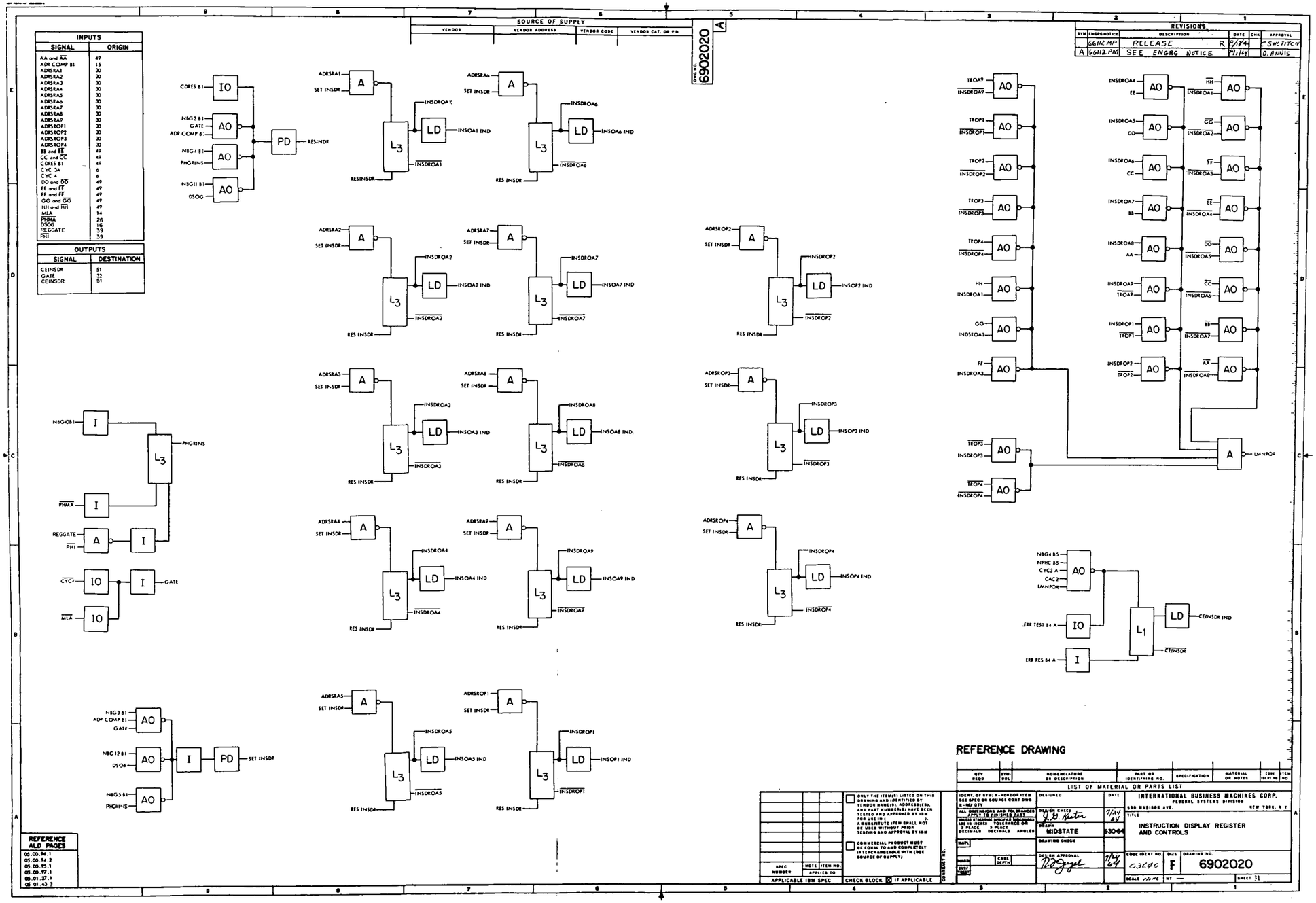


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 31)

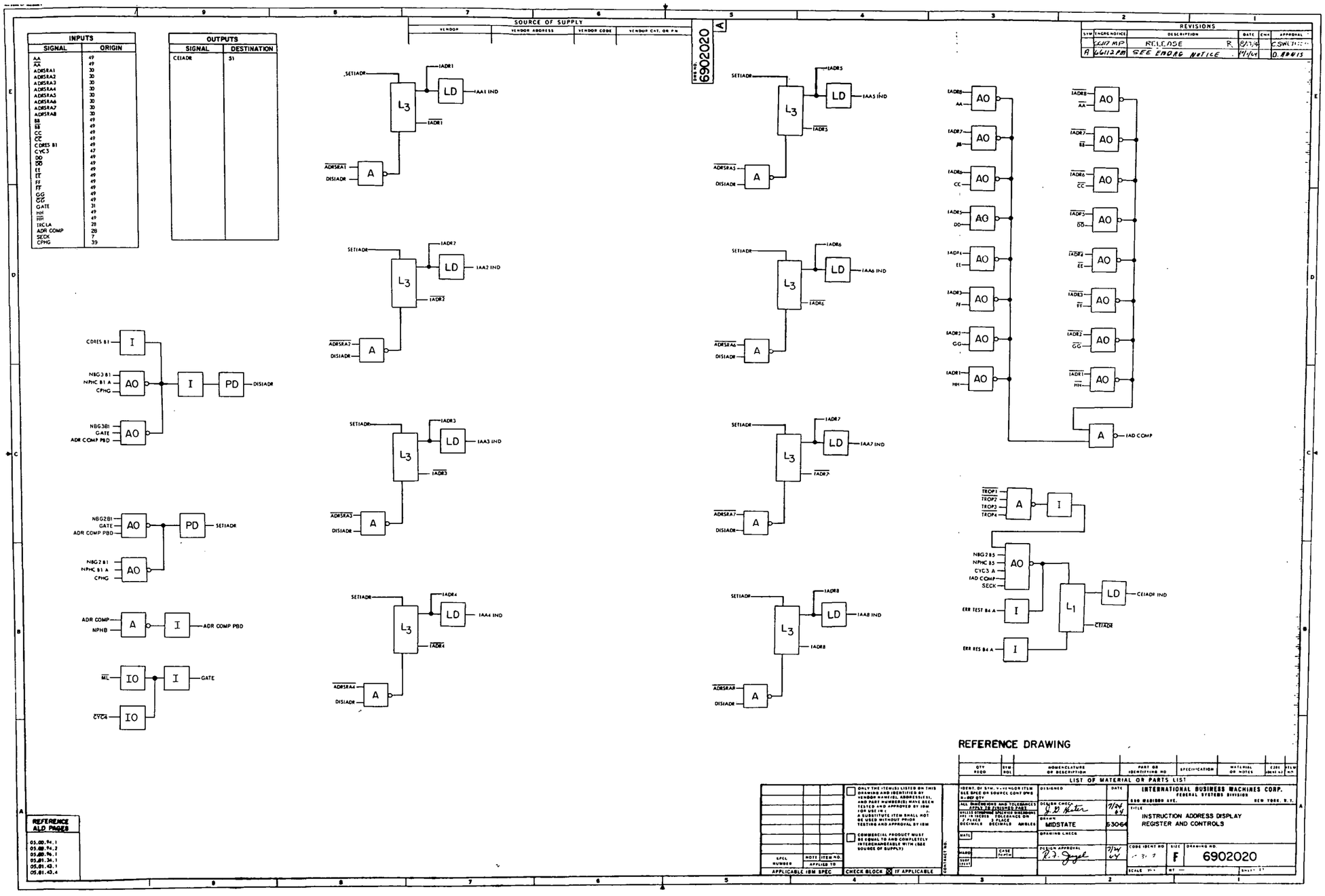


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 32)

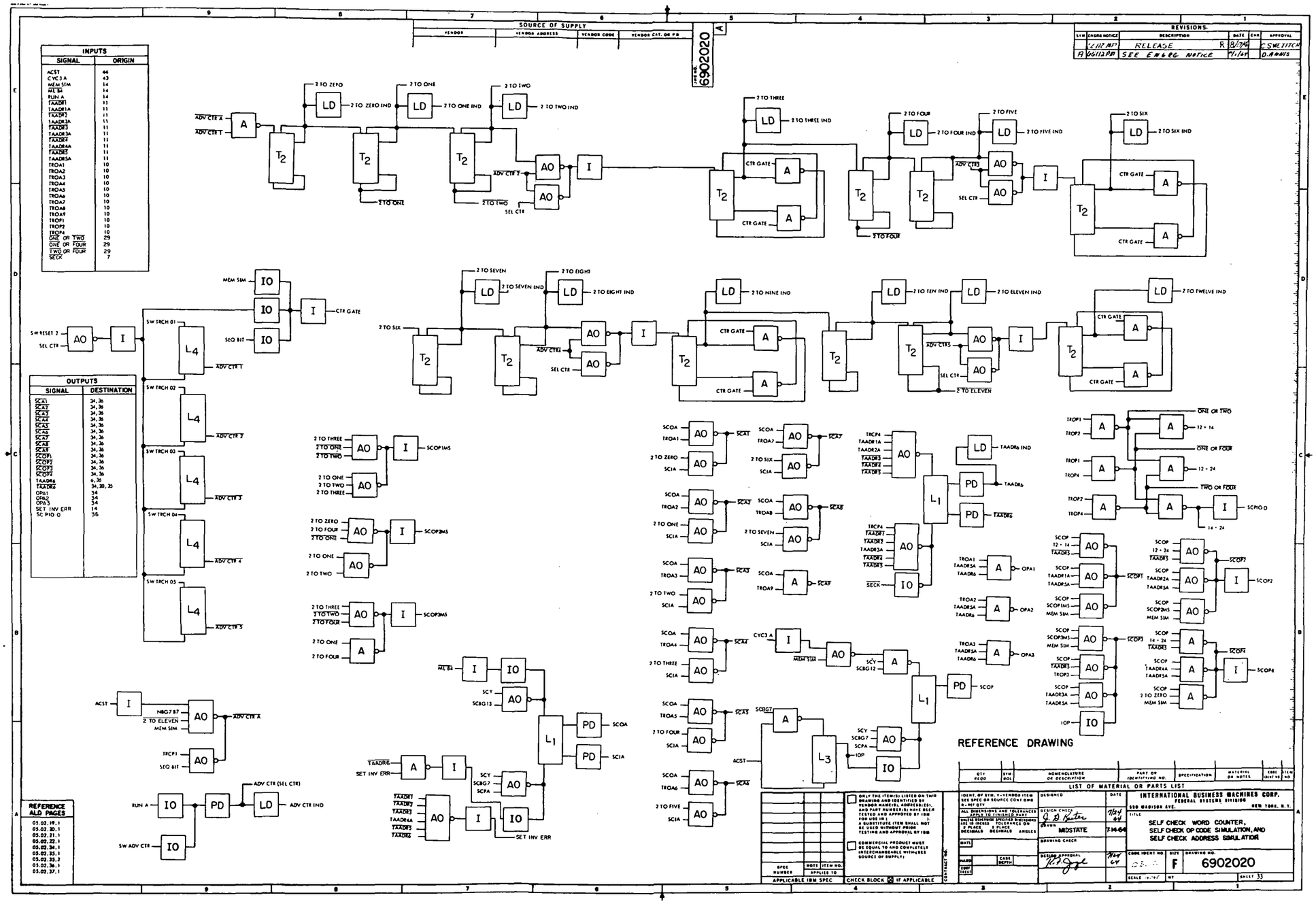


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 33)

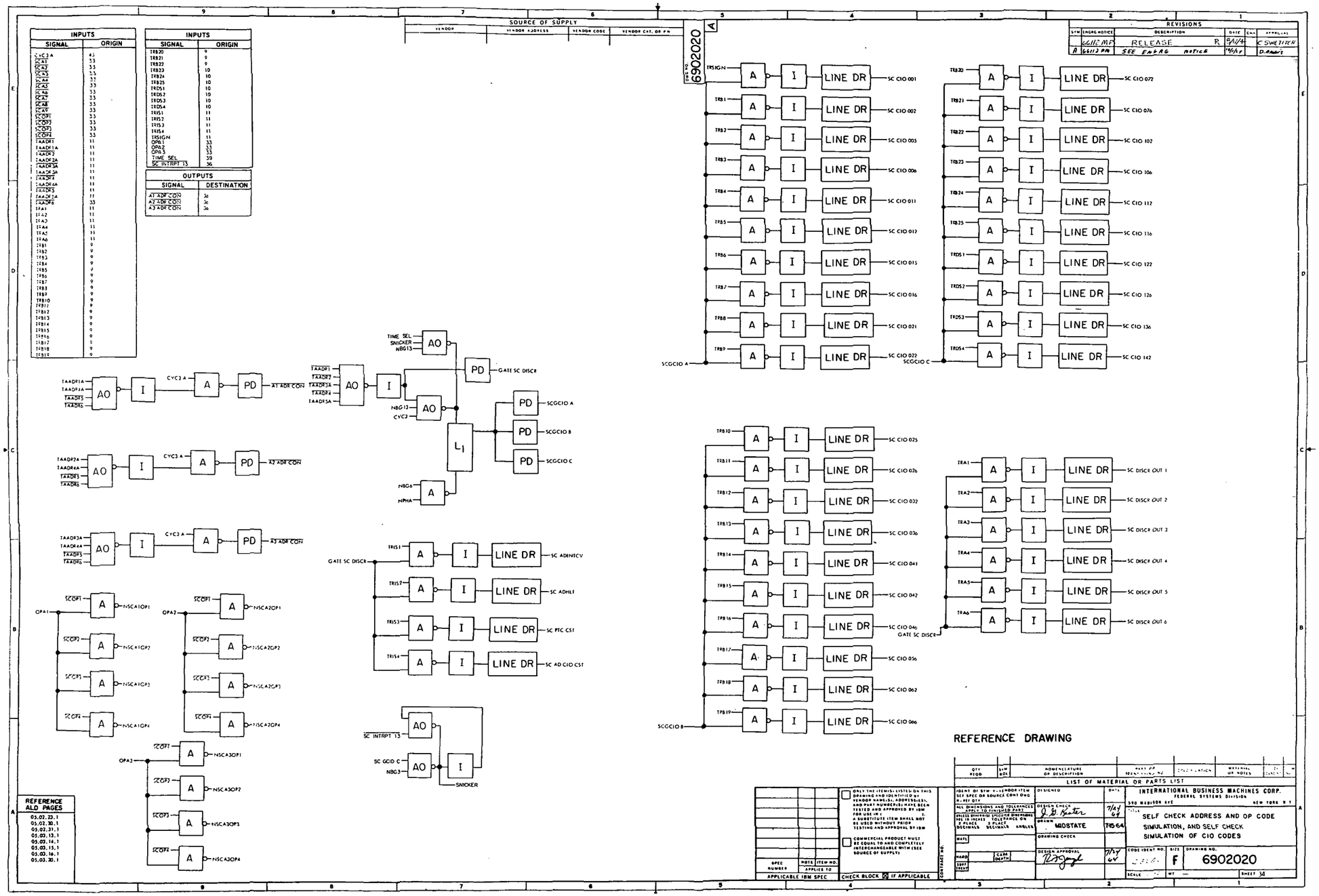


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 34)

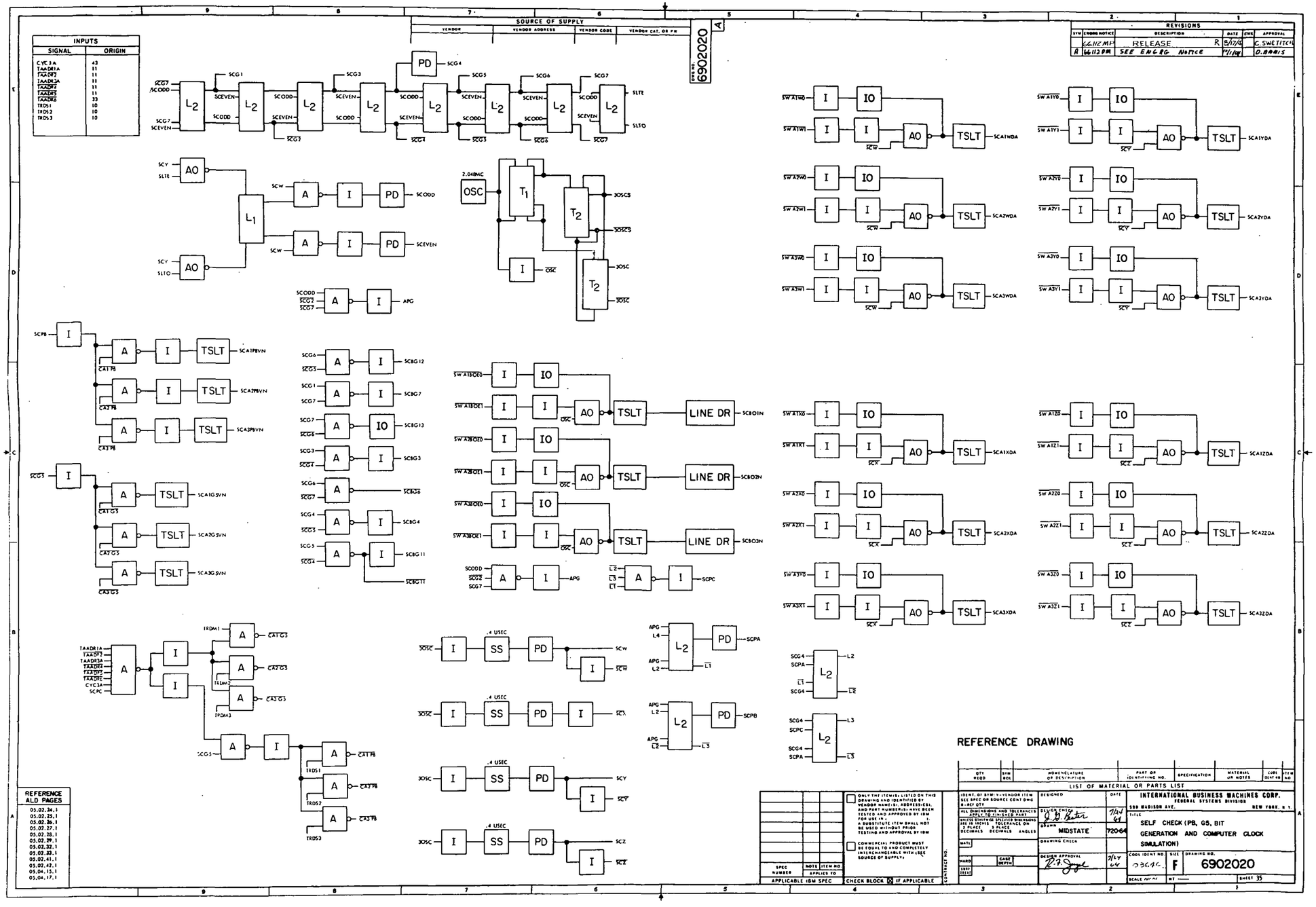


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 35)

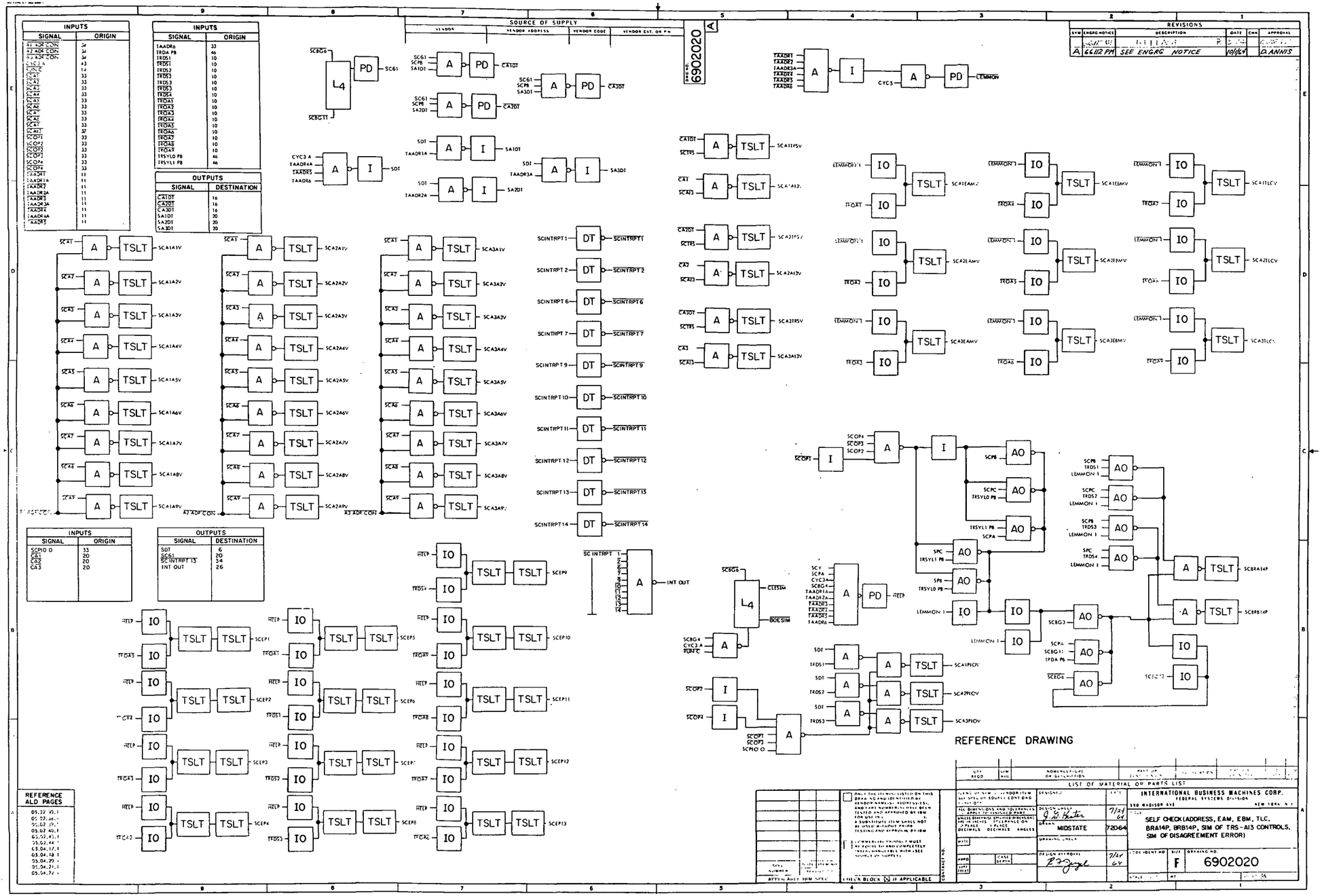


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 36)

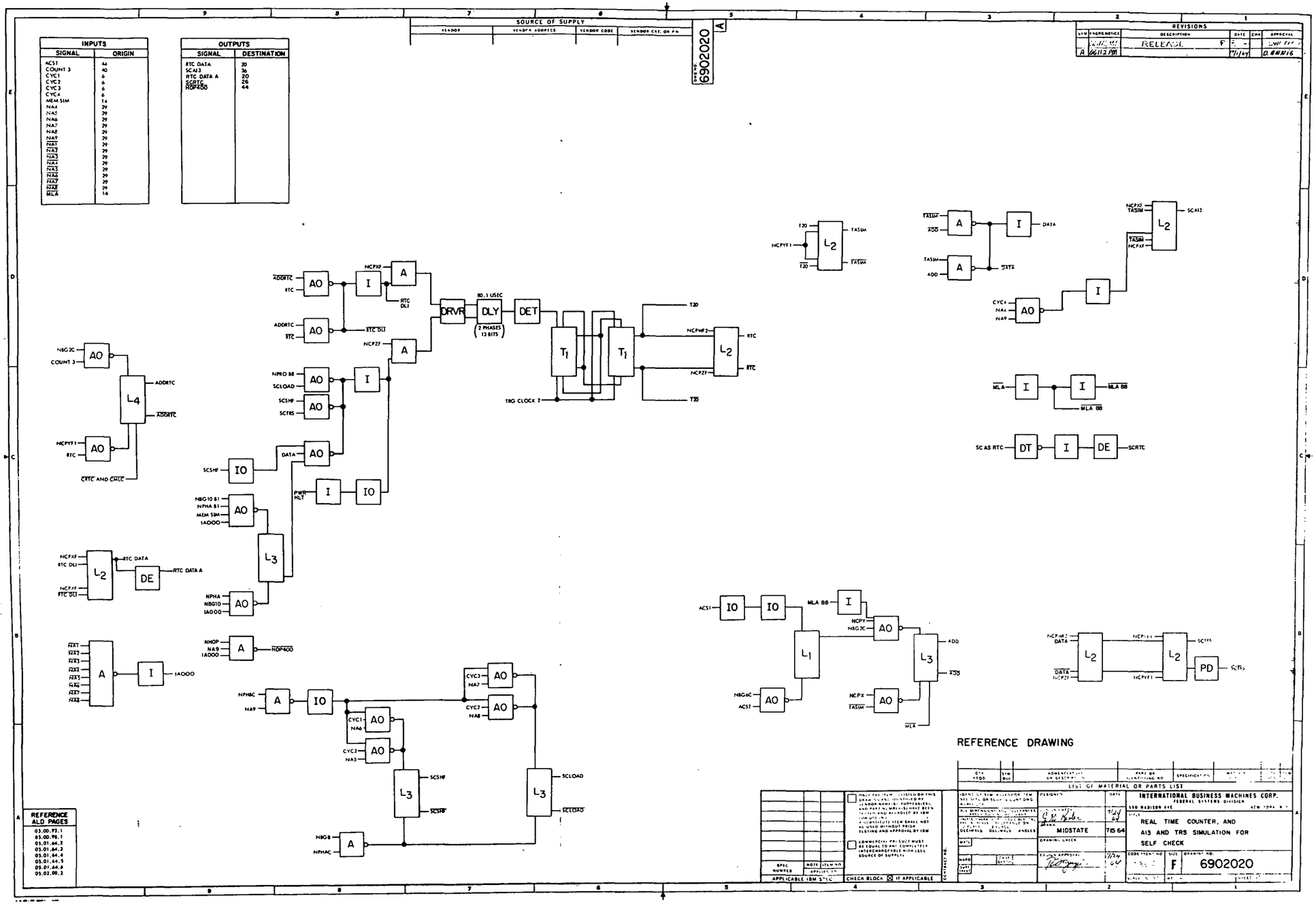


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 37)

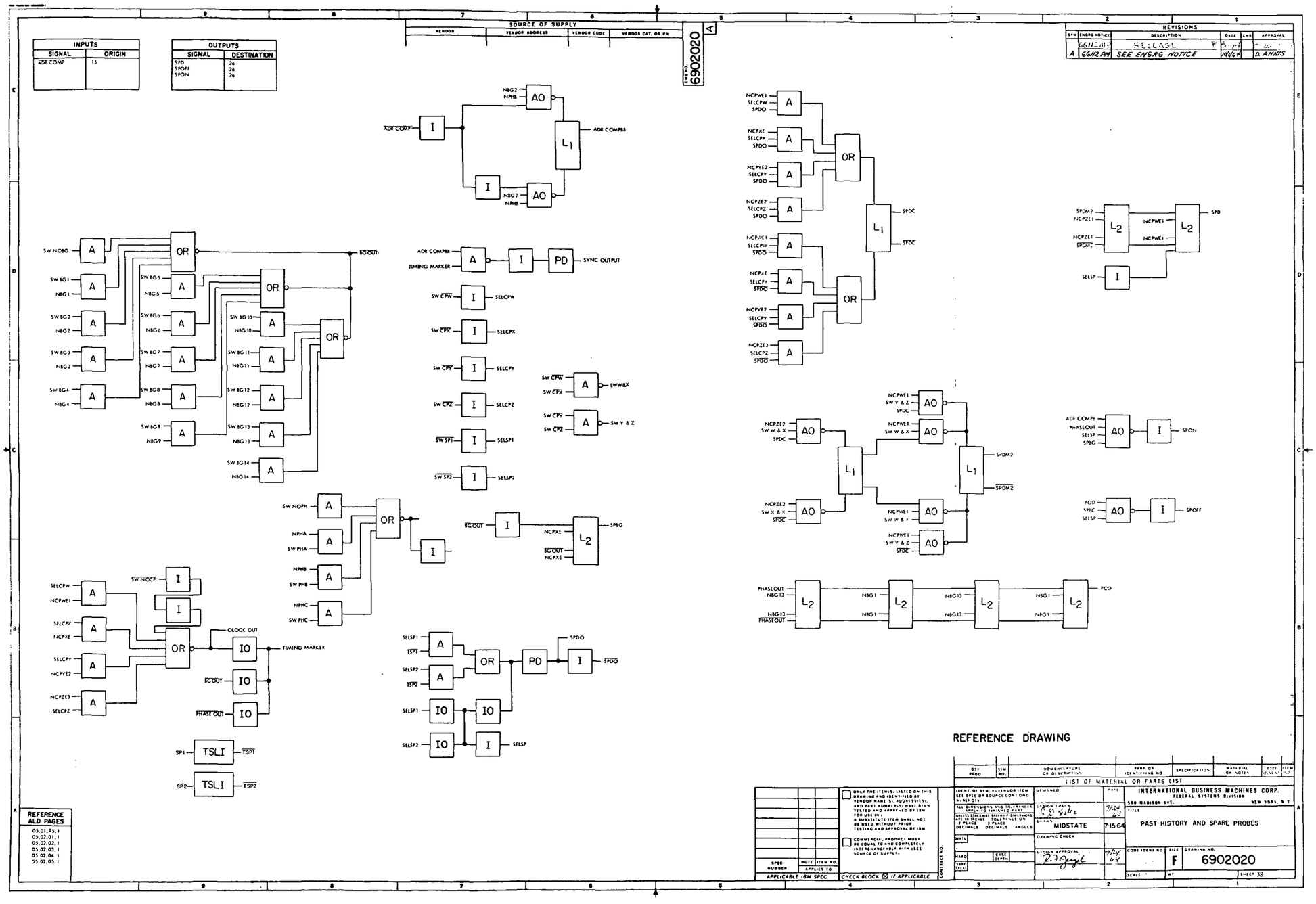


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 38)

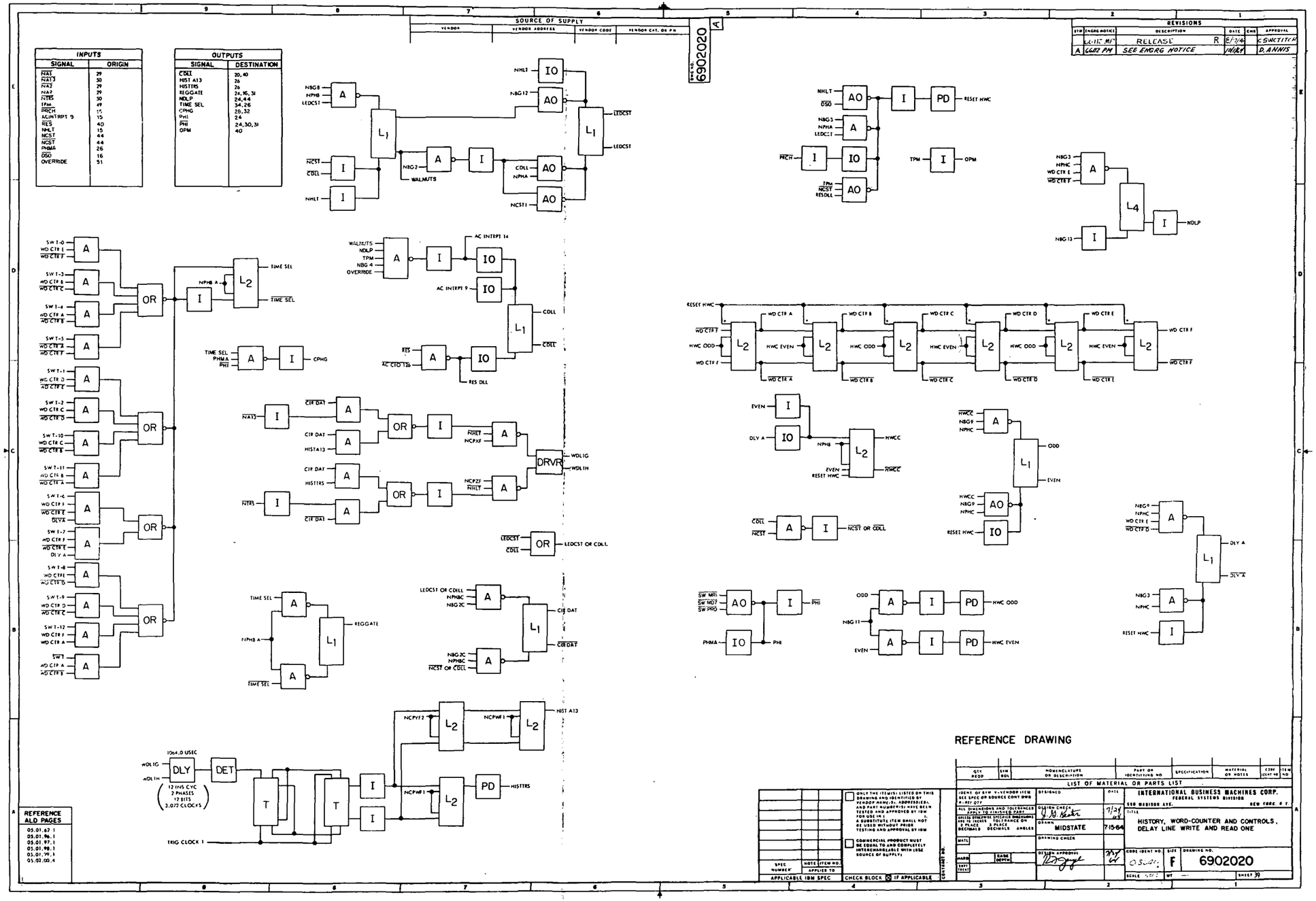


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 39)

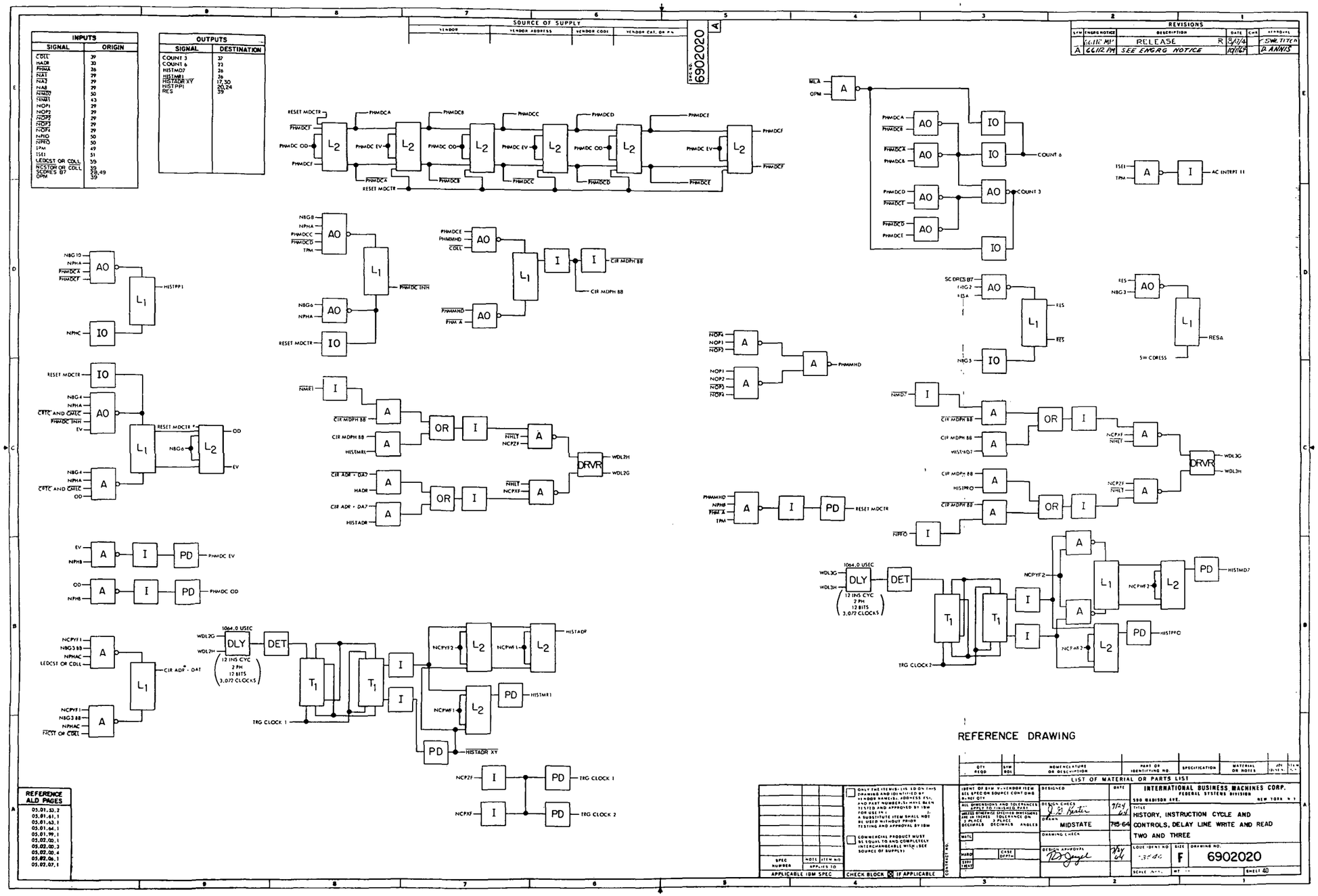


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 40)

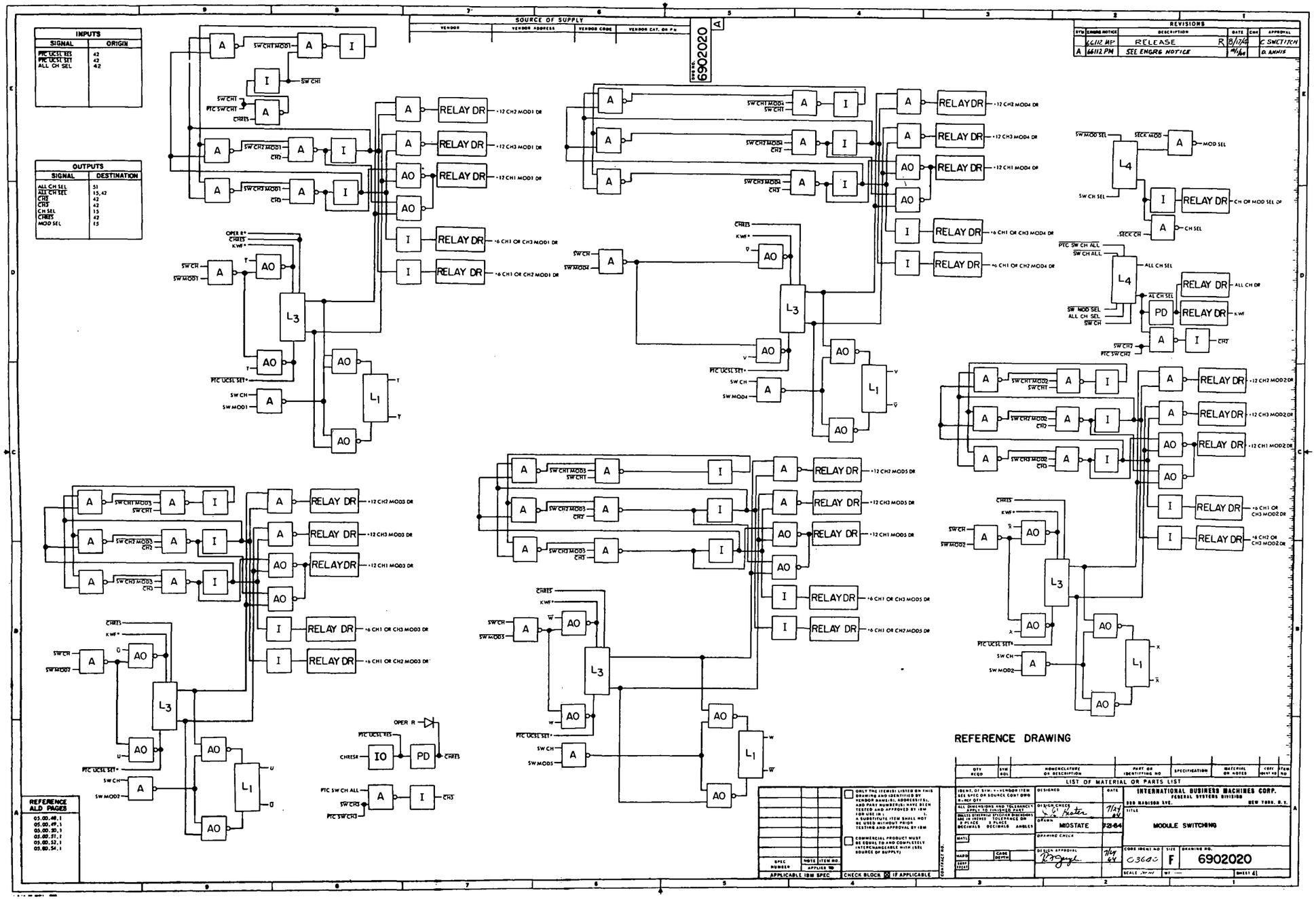


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 41)

INPUTS	
SIGNAL	ORIGIN
ALL CH SEL	41
CH2	41
CH3	41
CH1ES	41

OUTPUTS	
SIGNAL	DESTINATION
ALL CH SEL	41
PTC UCSL RESET	41
PTC UCSL SET	41

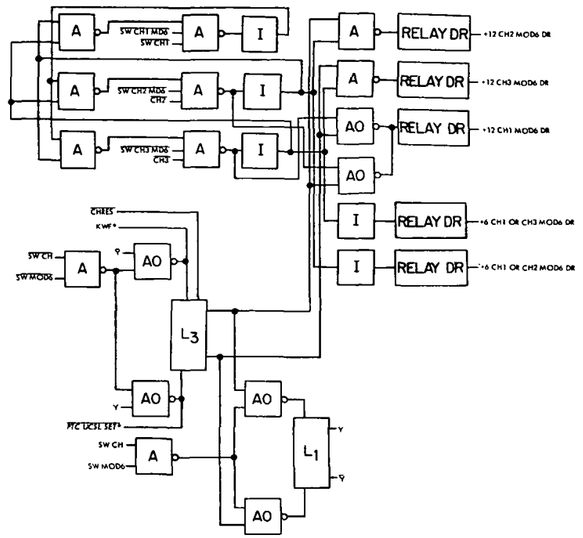
REFERENCE ALD PAGES
05.00.32.1
05.00.53.1
05.00.54.2

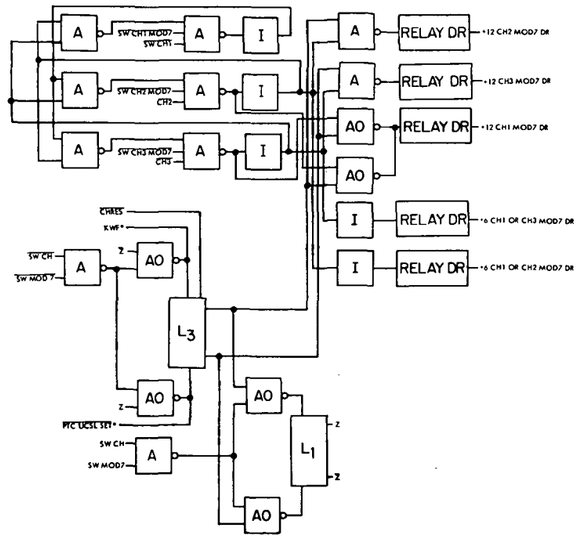
SOURCE OF SUPPLY

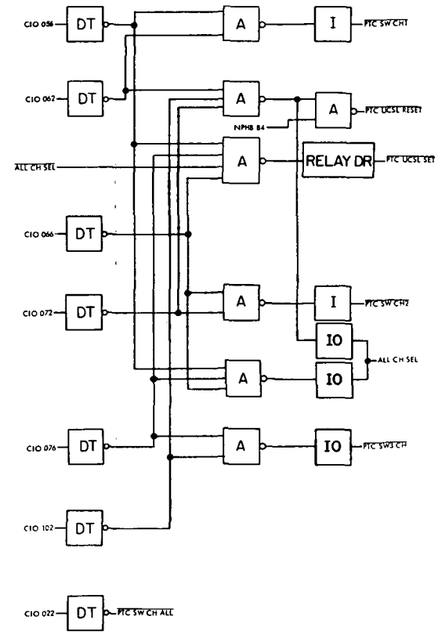
VENDOR	VENDOR ADDRESS	VENDOR CODE	VENDOR CAT. OR P.N.

DRWG. 6902020 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 MP	RELEASE R	8/12/66		E.SWETZER
A	66112 PM	SEE ENGRG NOTICE	9/16/66		D. ARMS







REFERENCE DRAWING

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO	ITEM NO

LIST OF MATERIAL OR PARTS LIST

ONLY THE ITEM(S) LISTED ON THIS DRAWING AND IDENTIFIED BY VENDOR NAME(S), ADDRESS(ES), AND PART NUMBER(S) HAVE BEEN TESTED AND APPROVED BY IBM FOR USE IN: (A SUBSTITUTE ITEM SHALL NOT BE USED WITHOUT PRIOR TESTING AND APPROVAL BY IBM

COMMERCIAL PRODUCT MUST BE EQUAL TO AND COMPLETELY INTERCHANGEABLE WITH (SEE SOURCE OF SUPPLY)

IDENT. OF SYM. V-VENDOR ITEM SEE SPEC OR SOURCE CONT DWG
R-REF QTY

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON DECIMALS: FRACTIONS DECIMALS ANGLES

DESIGNED	DATE
DESIGN CHECKED J.D. Hunter	7/24/64
DRAWN MIDSTATE	7/21/64
DRAWING CHECK	
DESIGN APPROVAL R.T. Lloyd	7/24/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
850 MADISON AVE. NEW YORK, N.Y.

TITLE
MODULE SWITCHING (CONT), PTC CONTROLED CHANNEL SWITCHING

CODE IDENT NO.	SIZE	DRAWING NO.
03640	F	6902020

SCALE NONE WT — SHEET 42

SPEC NUMBER	NOTE	ITEM NO. APPLIES TO
APPLICABLE IBM SPEC		

CHECK BLOCK ☒ IF APPLICABLE

CONTRACT NO.

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 42)

Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 43)

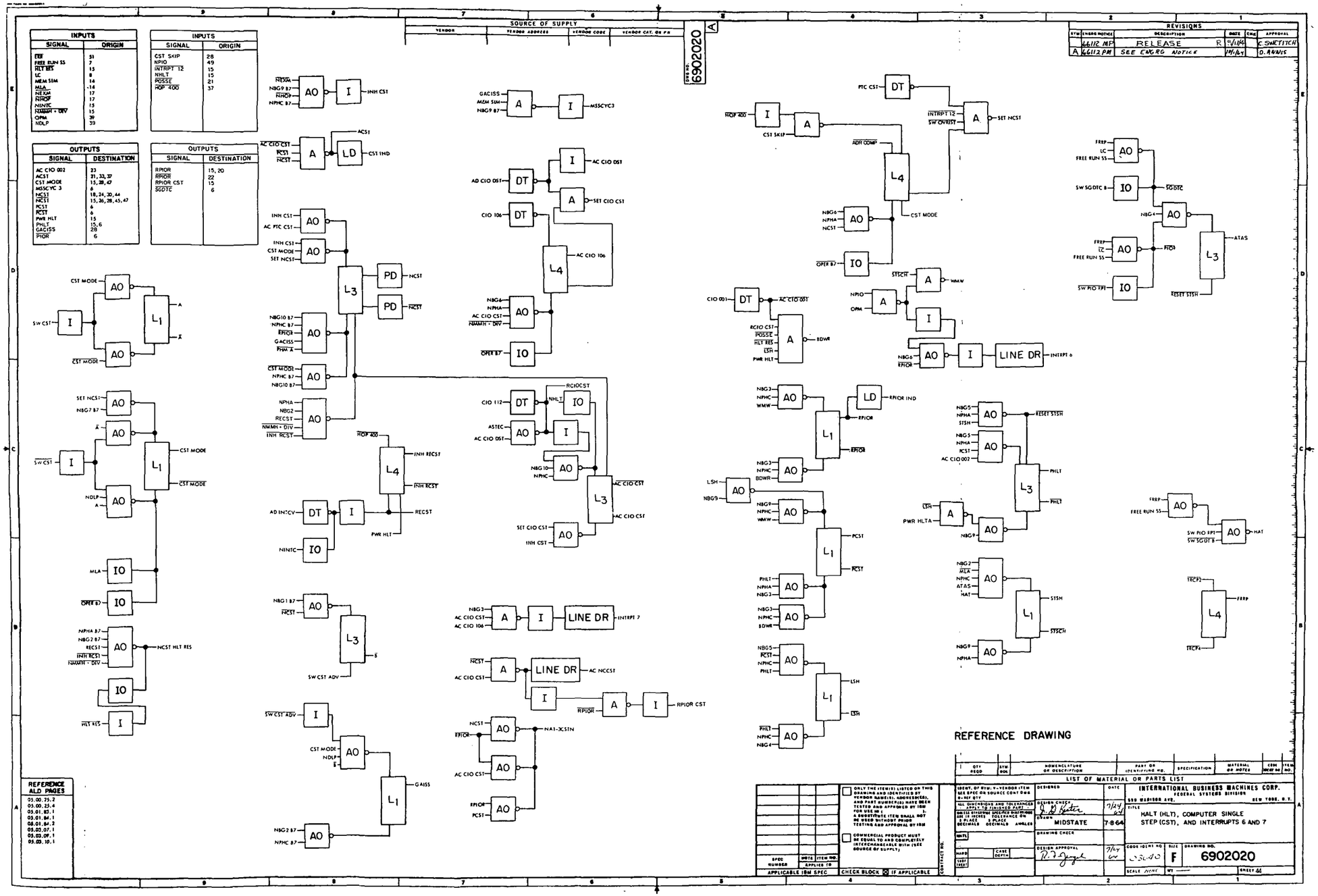


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 44)

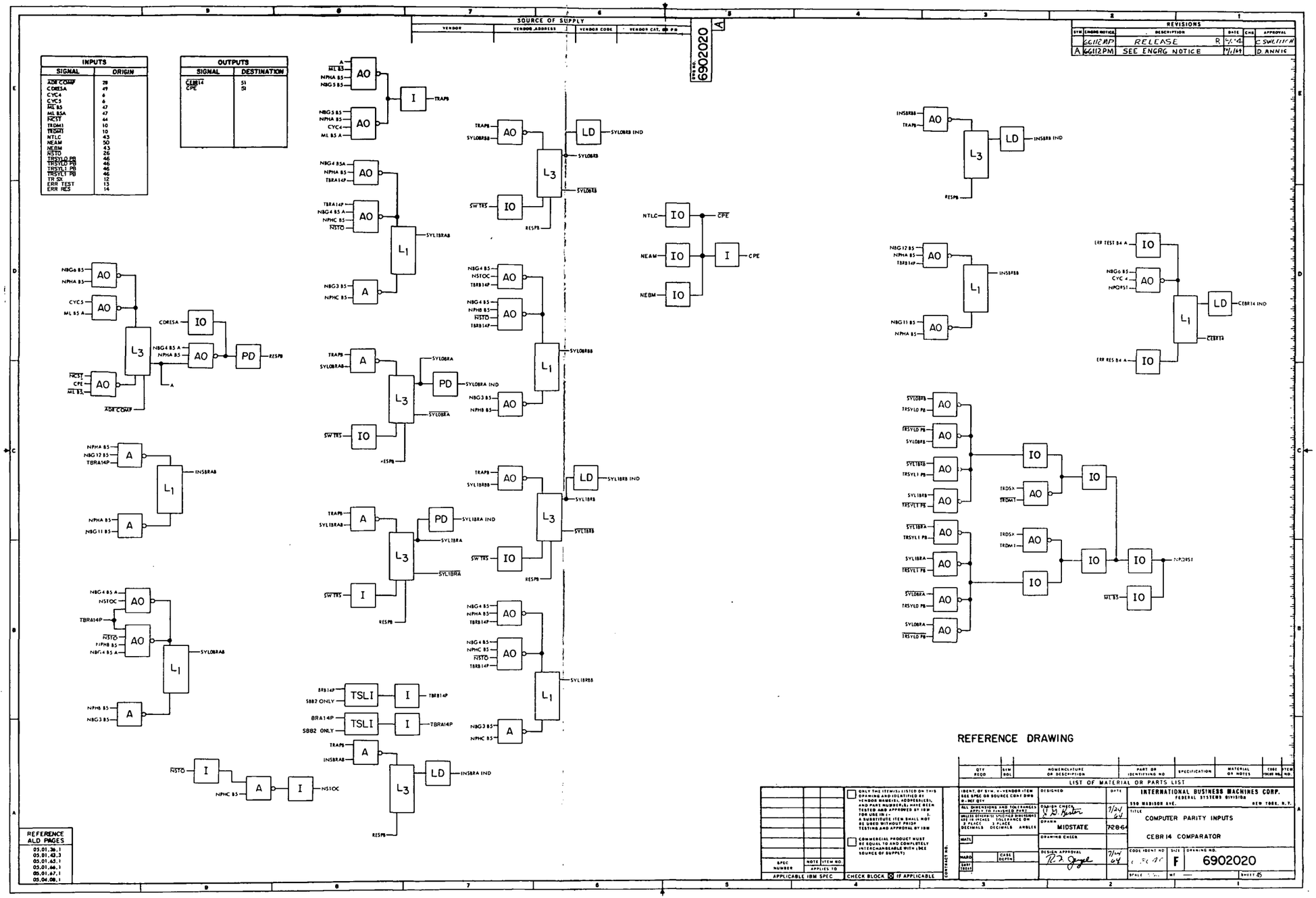


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 45)

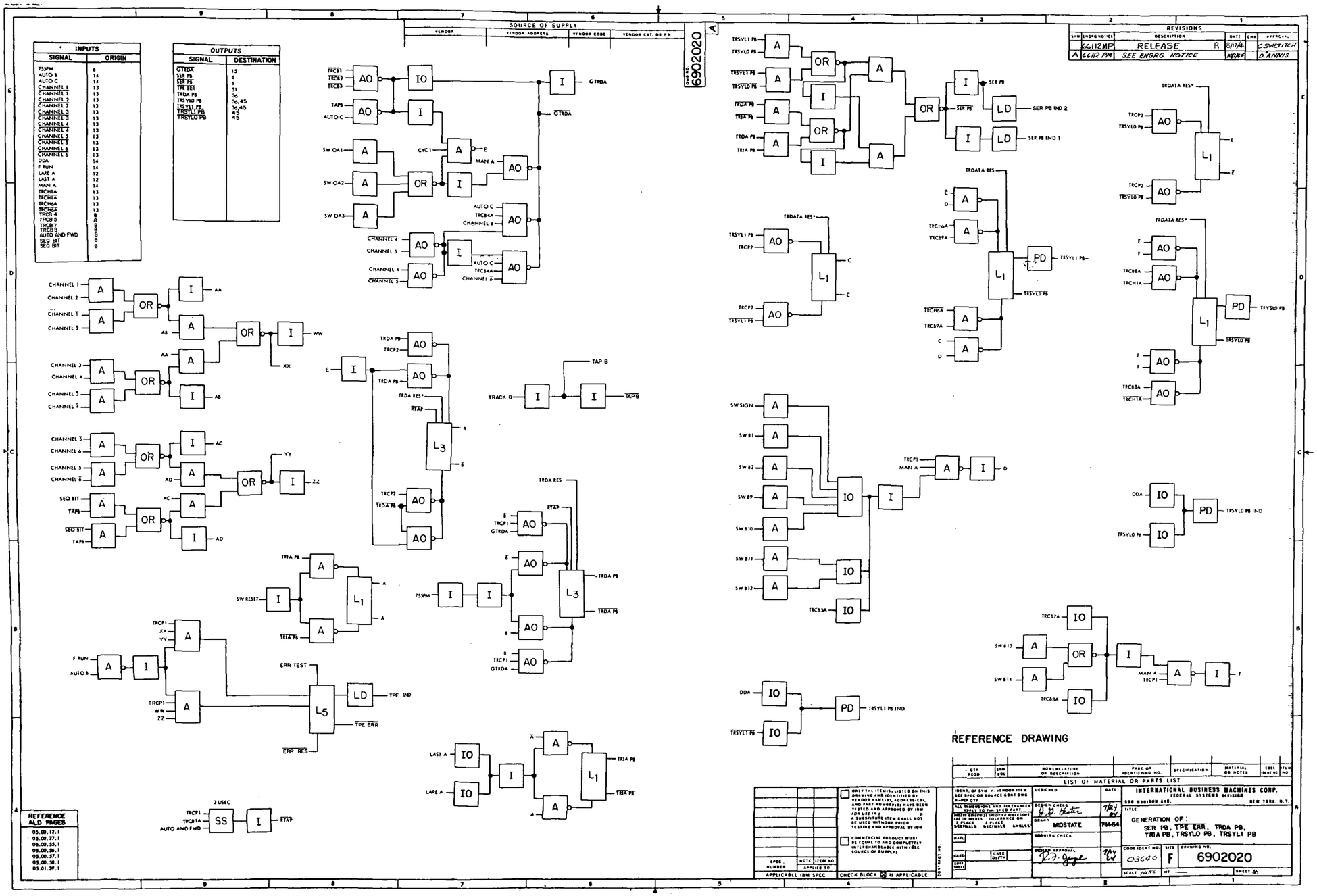


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 46)

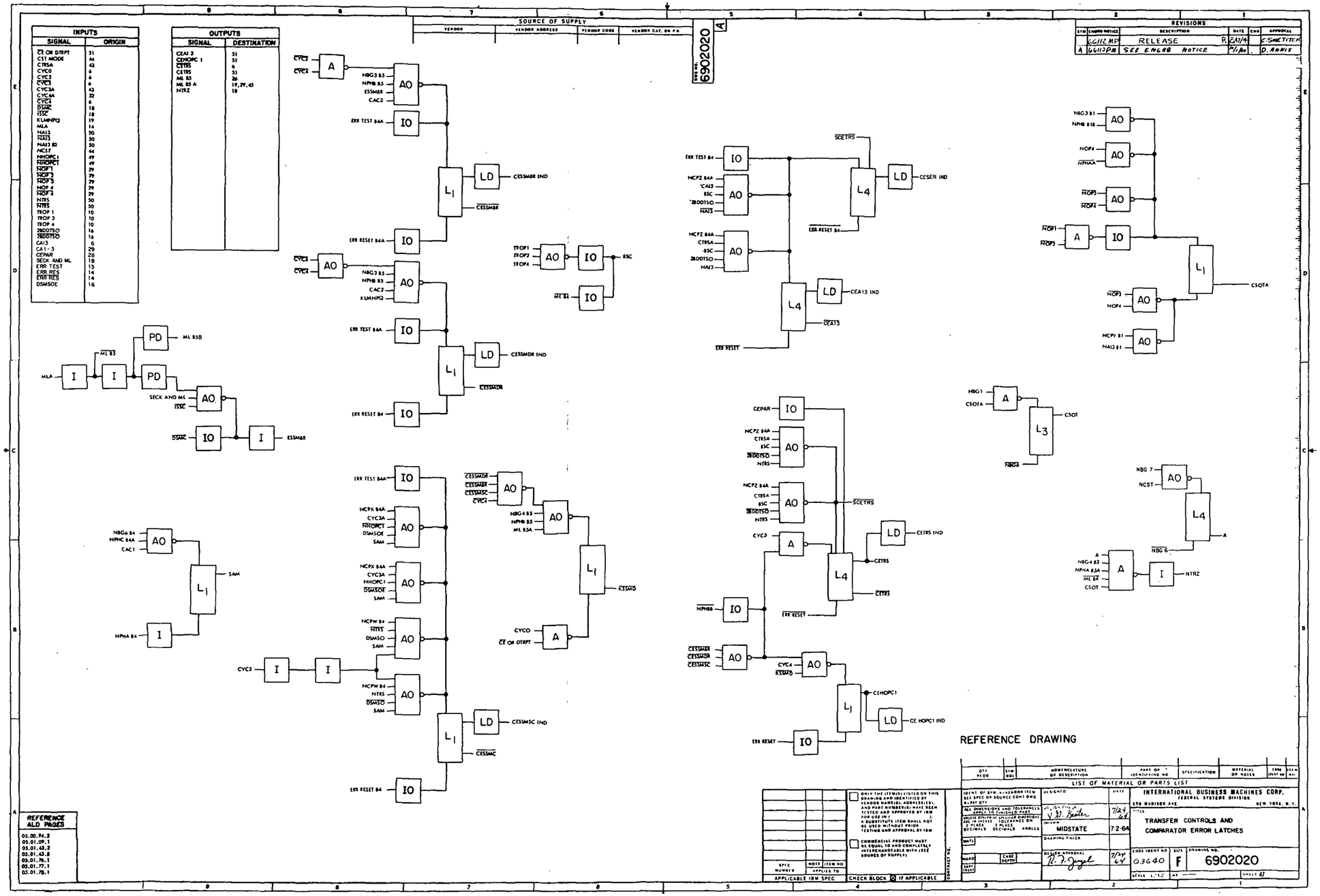


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 47)

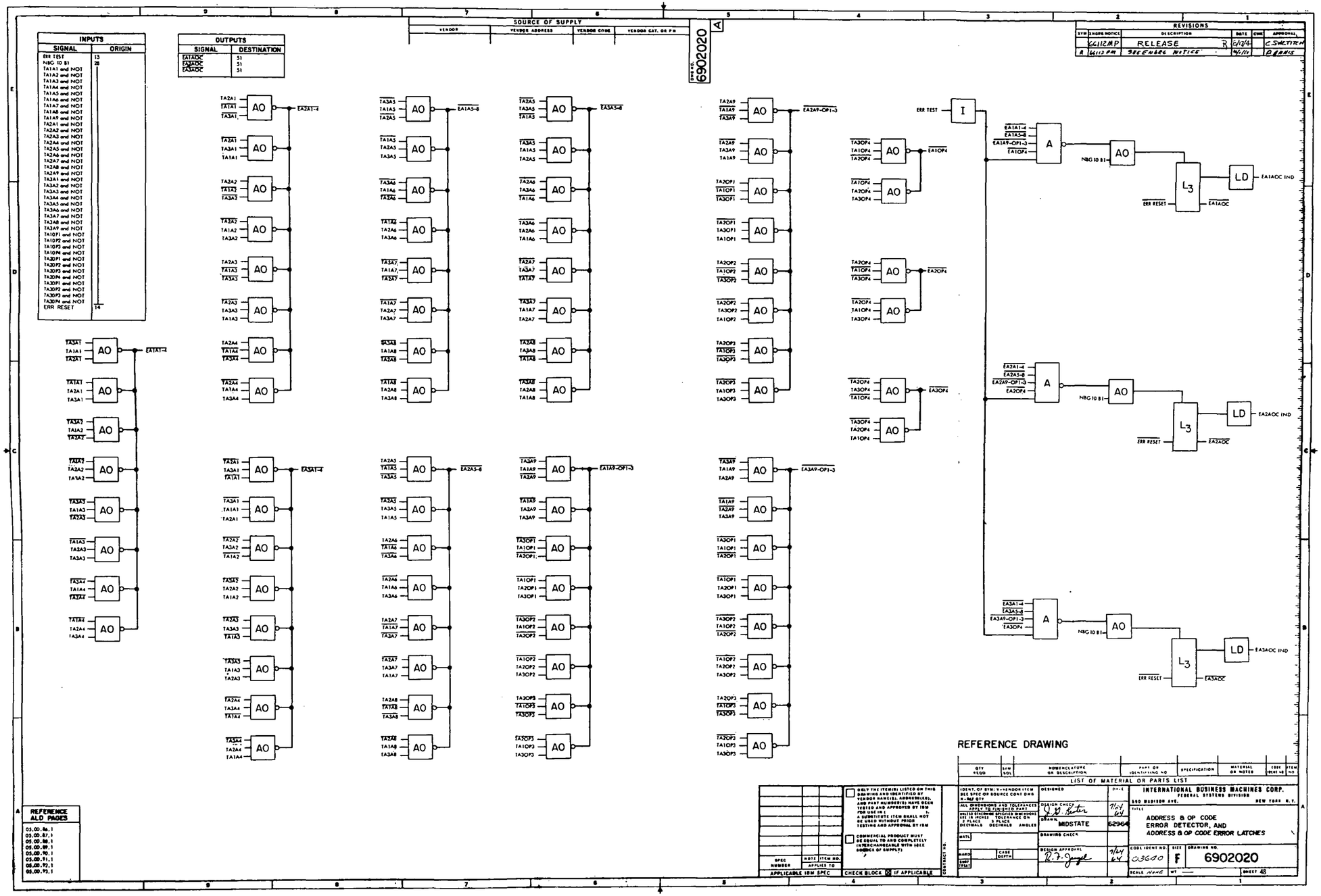


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 48)

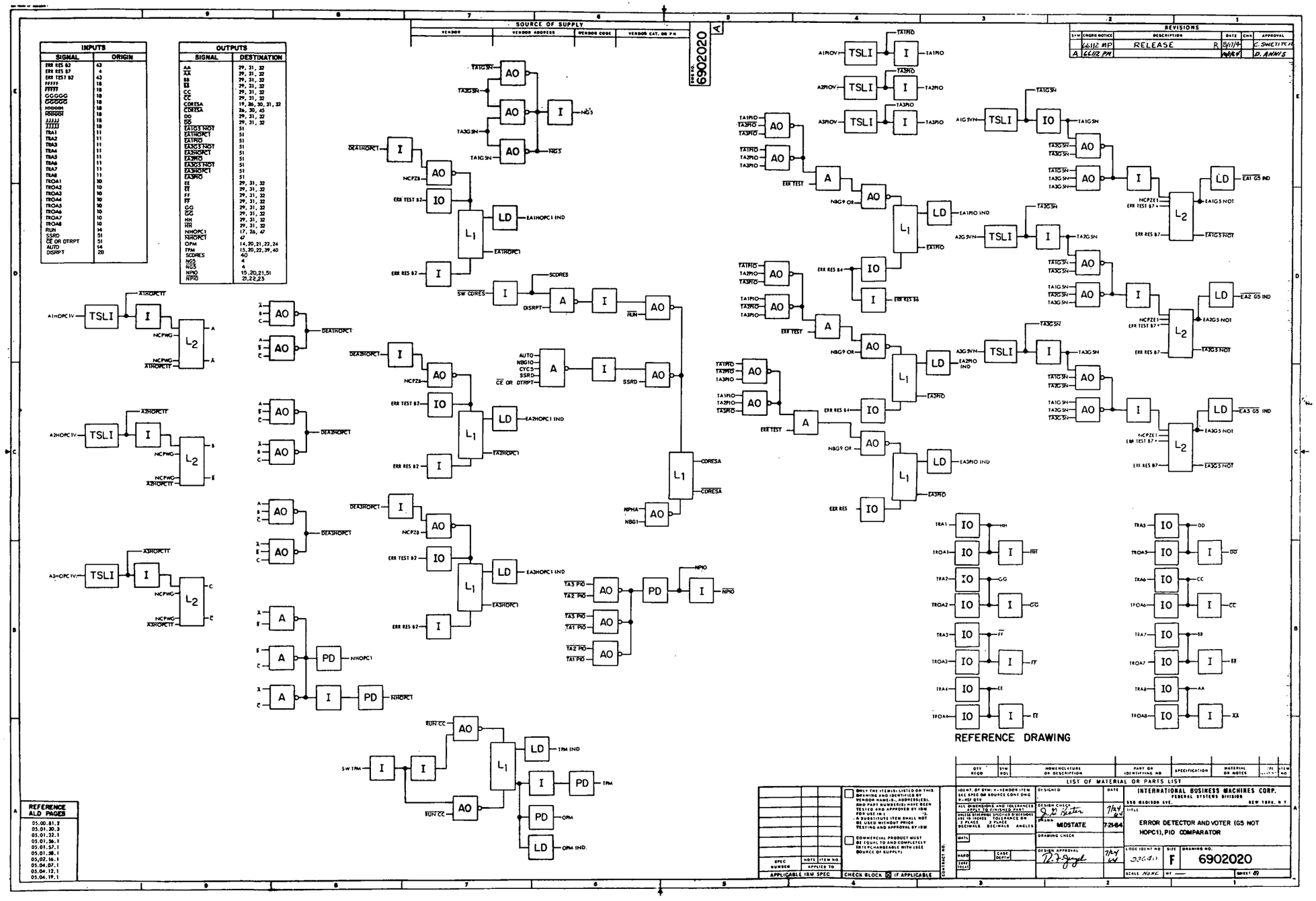


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 49)

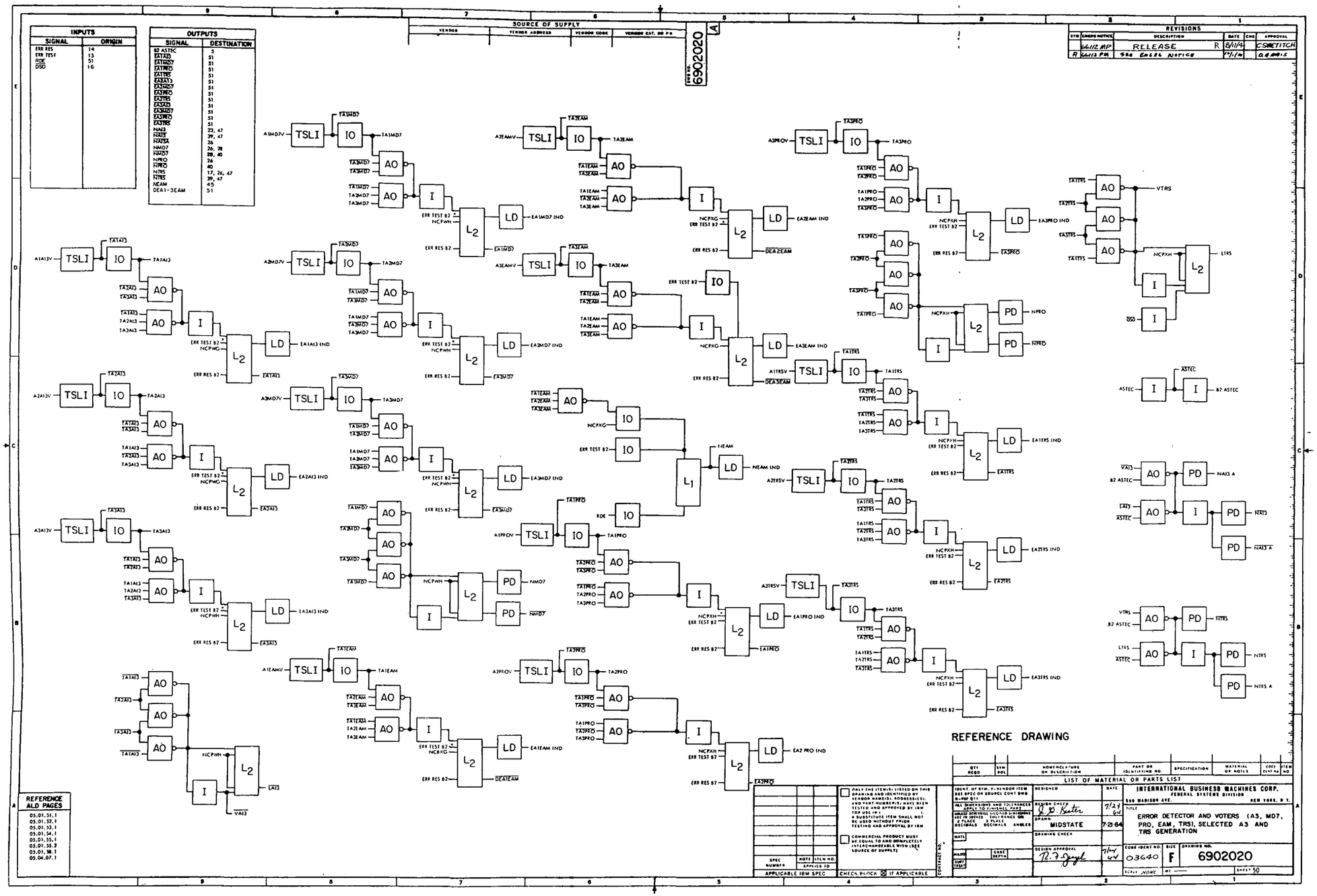


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 50)

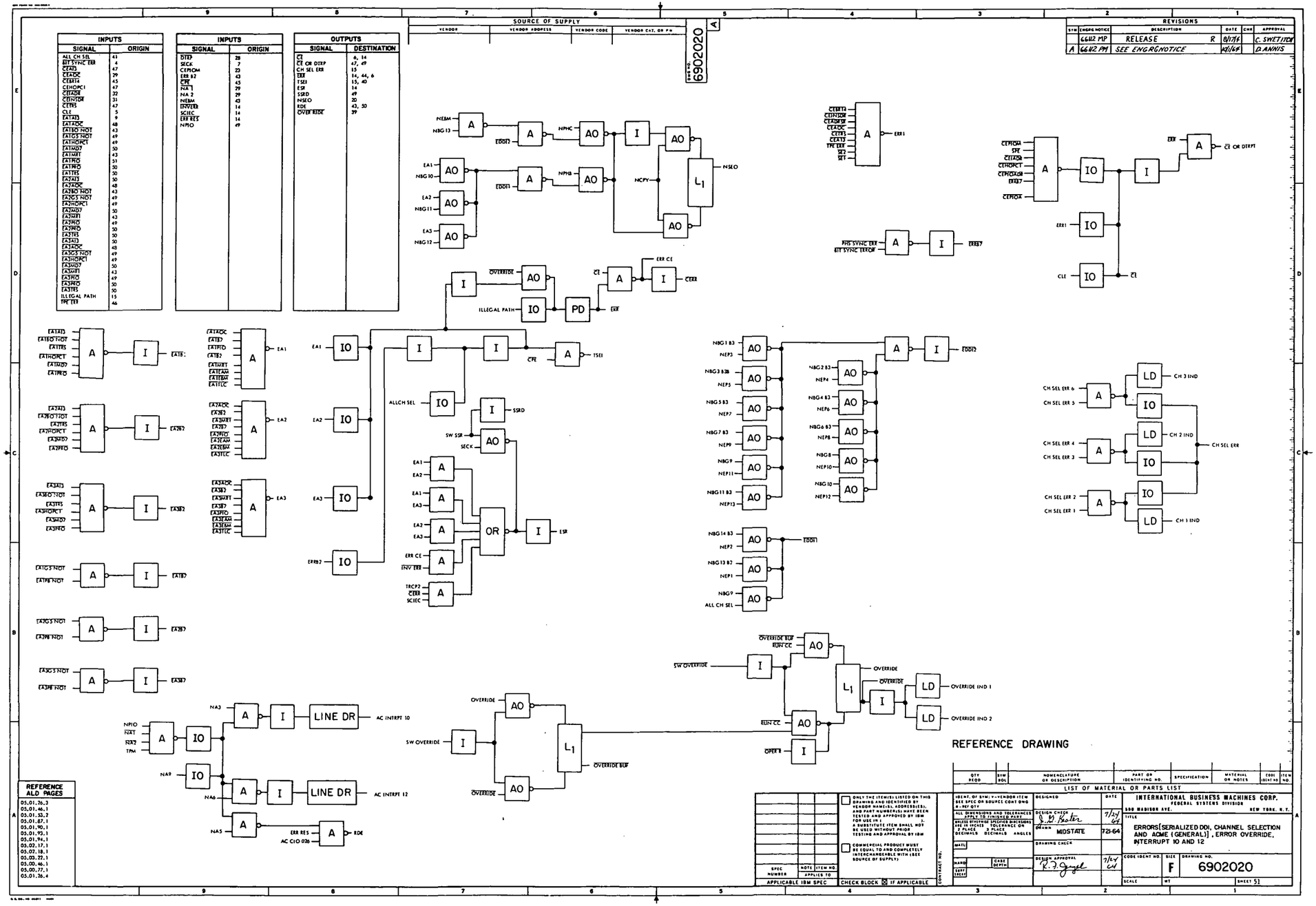
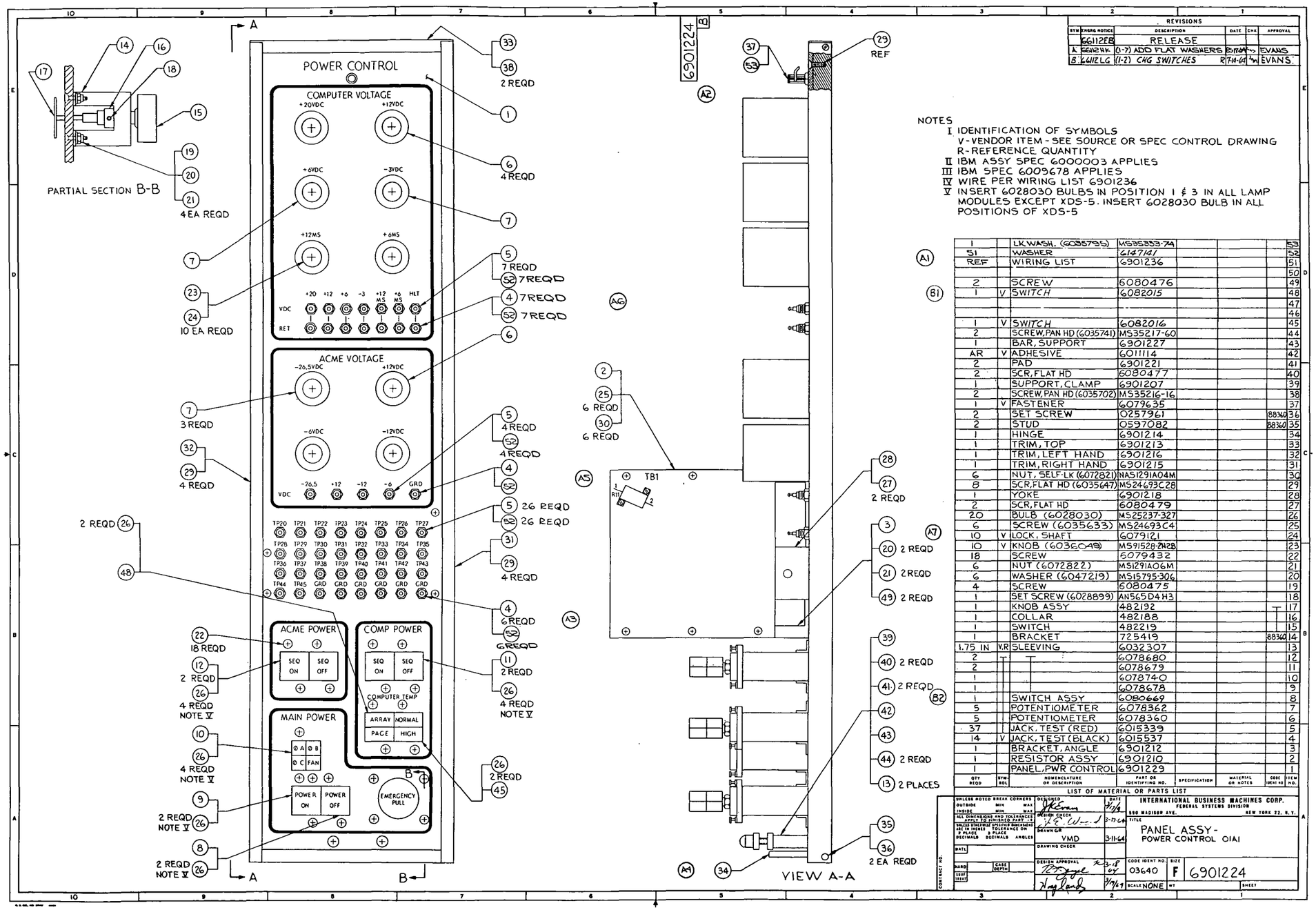


Figure 10-30. LVDCME Second Level Logic Diagrams (Sheet 51)



REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112E8	RELEASE			
A	66212WH	(1-7) ADD FLAT WASHERS	8-19-64	WH	EVANS
B	66312LG	(1-2) CHG SWITCHES	9-14-64	WH	EVANS

NOTES

I IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM - SEE SOURCE OR SPEC CONTROL DRAWING
R-REFERENCE QUANTITY

II IBM ASSY SPEC 6000003 APPLIES

III IBM SPEC 6009678 APPLIES

IV WIRE PER WIRING LIST 6901236

V INSERT 6028030 BULBS IN POSITION 1 & 3 IN ALL LAMP MODULES EXCEPT XDS-5. INSERT 6028030 BULB IN ALL POSITIONS OF XDS-5

1		LK WASH. (6035795)	MS35333-74					53
51		WASHER	6147147					52
REF		WIRING LIST	6901236					51
								50
2		SCREW	6080476					49
1	V	SWITCH	6082015					48
								47
								46
1	V	SWITCH	6082016					45
2		SCREW, PAN HD (6035741)	MS35217-60					44
1		BAR, SUPPORT	6901227					43
AR	V	ADHESIVE	6011114					42
2		PAD	6901221					41
2		SCR, FLAT HD	6080477					40
1		SUPPORT, CLAMP	6901207					39
2		SCREW, PAN HD (6035702)	MS35216-16					38
1	V	FASTENER	6079635					37
2		SET SCREW	0257961				88360	36
2		STUD	0597082				88360	35
1		HINGE	6901214					34
1		TRIM, TOP	6901213					33
1		TRIM, LEFT HAND	6901216					32
1		TRIM, RIGHT HAND	6901215					31
6		NUT, SELF-LK (6072821)	NAS1291A04M					30
8		SCR, FLAT HD (6035647)	MS24693C28					29
1		YOKE	6901218					28
2		SCR, FLAT HD	6080479					27
20		BULB (6028030)	MS25237-327					26
6		SCREW (6035633)	MS24693C4					25
10	V	LOCK, SHAFT	6079121					24
10	V	KNOB (6036049)	MS91528-2N2B					23
18		SCREW	6079432					22
6		NUT (6072822)	MS1291A06M					21
6		WASHER (6047219)	MS15795-306					20
4		SCREW	6080475					19
1		SET SCREW (6028899)	AN565D4H3					18
1		KNOB ASSY	482192					17
1		COLLAR	482188					16
1		SWITCH	482219					15
1		BRACKET	725419				88360	14
1.75 IN	V,R	SLEEVING	6032307					13
2			6078680					12
2			6078679					11
1			6078740					10
1			6078678					9
1		SWITCH ASSY	6080669					8
5		POTENTIOMETER	6078362					7
5		POTENTIOMETER	6078360					6
37		JACK, TEST (RED)	6015339					5
14	V	JACK, TEST (BLACK)	6015537					4
1		BRACKET, ANGLE	6901212					3
1		RESISTOR ASSY	6901210					2
1		PANEL, PWR CONTROL	6901229					1
QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES		CODE IDENT NO	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART -IS
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD
CASE DEPTH
SURF TREAT

DESIGNED		DATE 3/4
DESIGN CHECK		3-11-64
DRAWN GR		
DRAWING CHECK	VMD	3-11-64
DESIGN APPROVAL		3-18-64
		3/19/64

CONTRACT NO.

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PANEL ASSY-
POWER CONTROL 01A1

CODE IDENT NO. 03640 | SIZE F | 6901224

SCALE NONE | WT | SHEET

Figure 10-31. Power Control Panel (01A1) Assembly Drawing

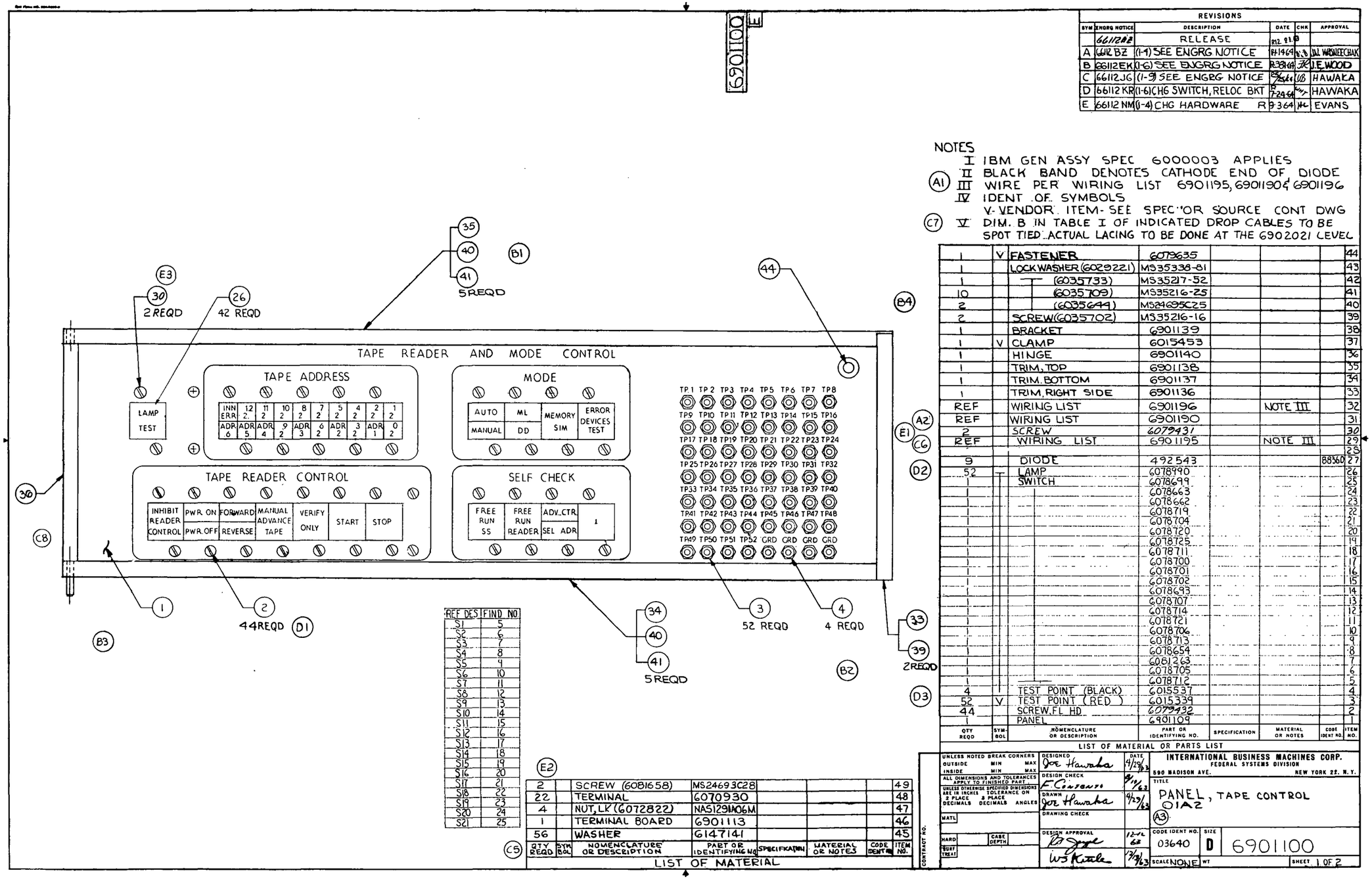


Figure 10-32. Tape Control Panel (01A2) Assembly Drawing (Sheet 1 of 2)

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112B2	RELEASE	4-21-63		
A	66112B2	(1-4) SEE ENGRG NOTICE	4-29-63	JC	J.N. VANCE/H.K.
B	66112EK	(1-6) SEE ENGRG NOTICE	8-30-63	JC	J.E. WOOD
C	66112JG	(1-9) SEE ENGRG NOTICE	9-26-63	HK	HAWAKA
D	66112KR	(1-6) CHG SWITCH RELOC BRKT	10-22-63	HK	HAWAKA
E	66112NM	(1-4) CHG HARDWARE	11-9-63	HK	EVANS

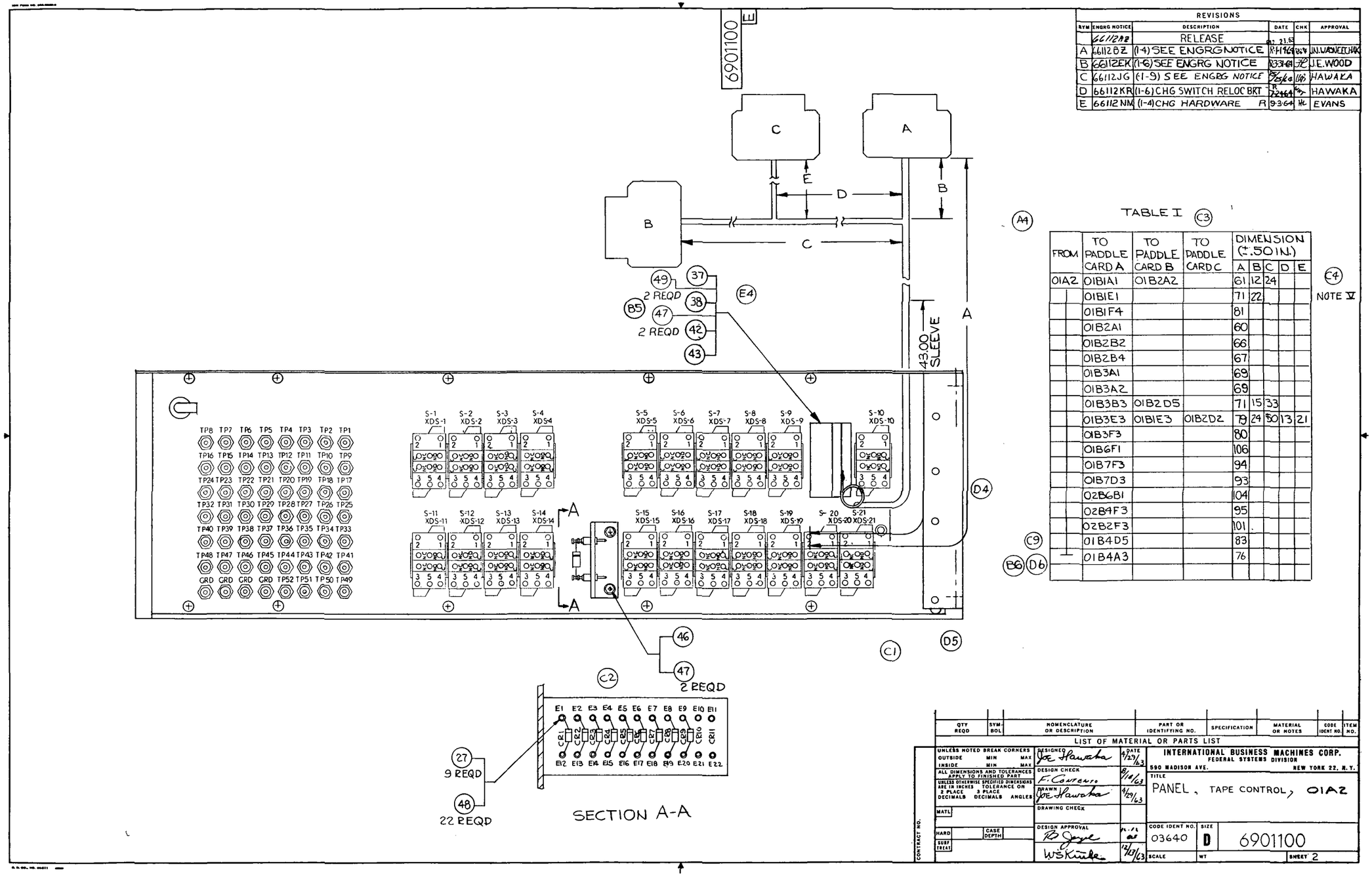


TABLE I (C3)

FROM	TO PADDLE CARD A	TO PADDLE CARD B	TO PADDLE CARD C	DIMENSION (±.501N.) A	B	C	D	E
01A2	01B1A1	01B2A2		61	12	24		
	01B1E1			71	22			
	01B1F4			81				
	01B2A1			60				
	01B2B2			66				
	01B2B4			67				
	01B3A1			69				
	01B3A2			69				
	01B3B3	01B2D5		71	15	33		
	01B3E3	01B1E3	01B2D2	79	24	50	13	21
	01B3F3			80				
	01B6F1			106				
	01B7F3			94				
	01B7D3			93				
	02B6B1			104				
	02B4F3			95				
	02B2F3			101				
	01B4D5			83				
	01B4A3			76				

(A4) (C4) NOTE V (C9) (B6) (D6)

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS — OUTSIDE MIN MAX — INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES — TOLERANCE ON 2 PLACE DECIMALS — 3 PLACE DECIMALS — ANGLES
MATL
HARD — CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED Joe Hawaka 4/29/63
DESIGN CHECK F. Cattanto 5/10/63
DRAWN Joe Hawaka 4/29/63
DRAWING CHECK
DESIGN APPROVAL R B Joyce 11-8-63
W S Kinder 12/3/63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PANEL, TAPE CONTROL, 01A2

CODE IDENT NO. 03640 | SIZE D | 6901100
SCALE | WT | SHEET 2

Figure 10-32. Tape Control Panel (01A2) Assembly Drawing (Sheet 2)

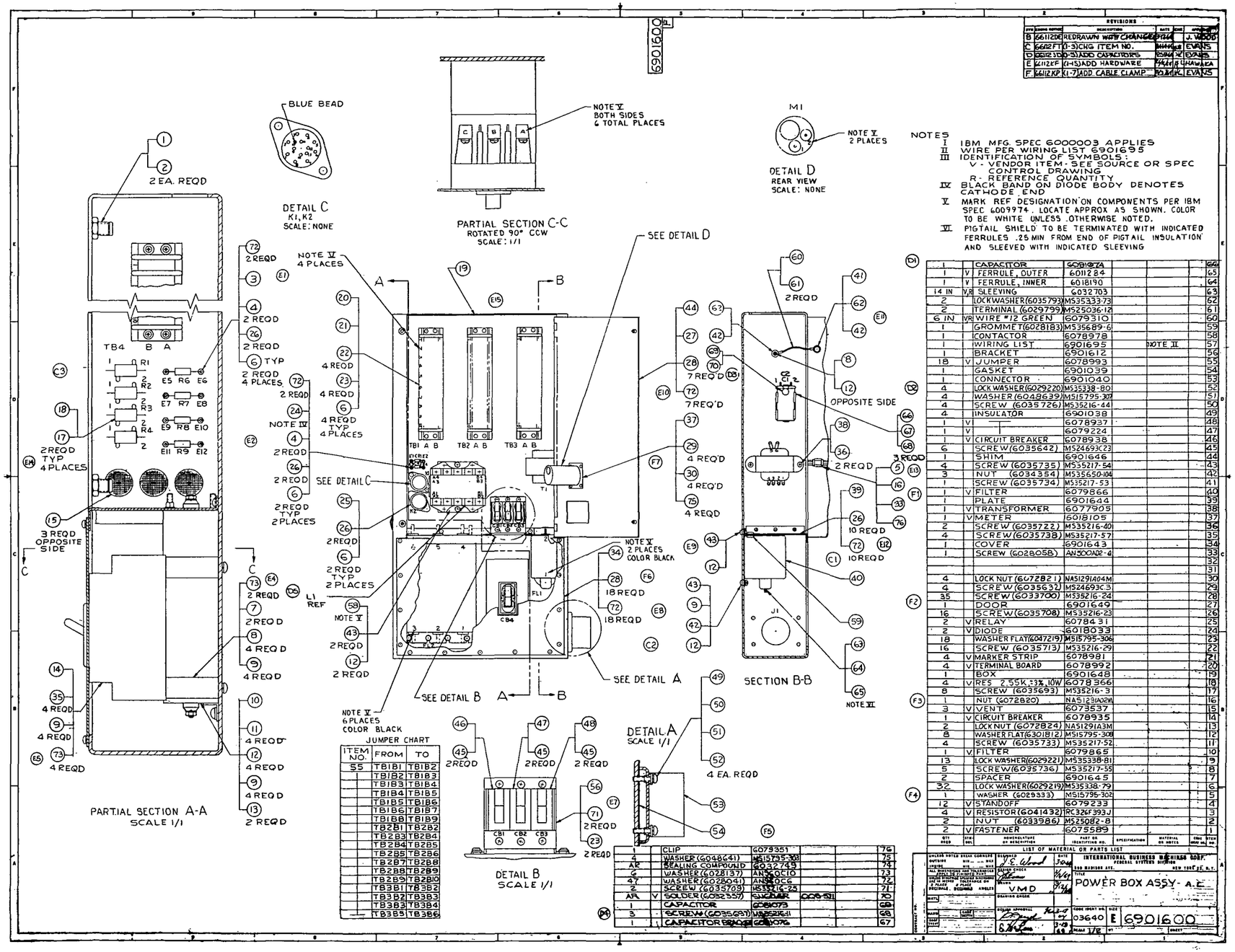
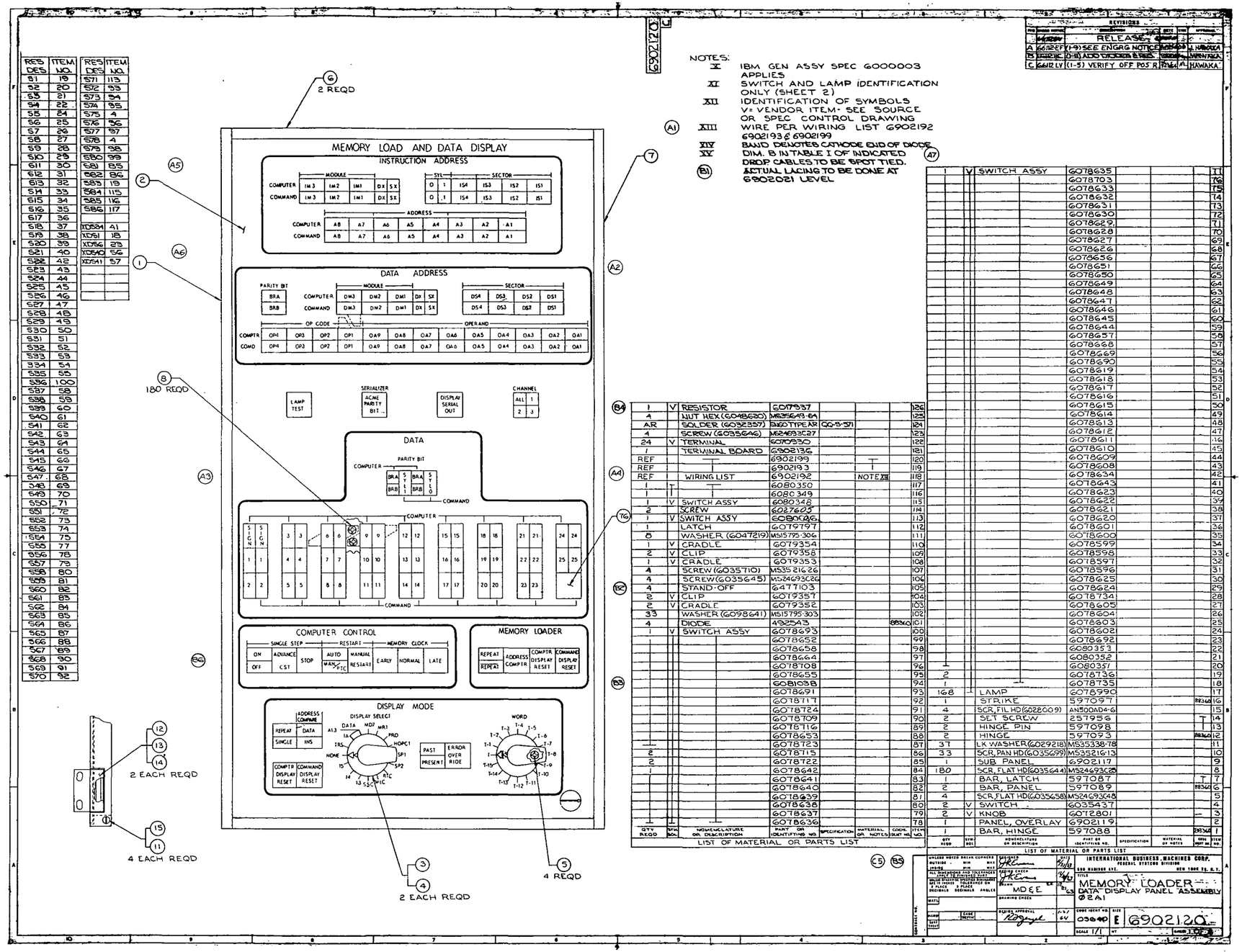


Figure 10-33. AC Power Gate (01B5) Assembly Drawing

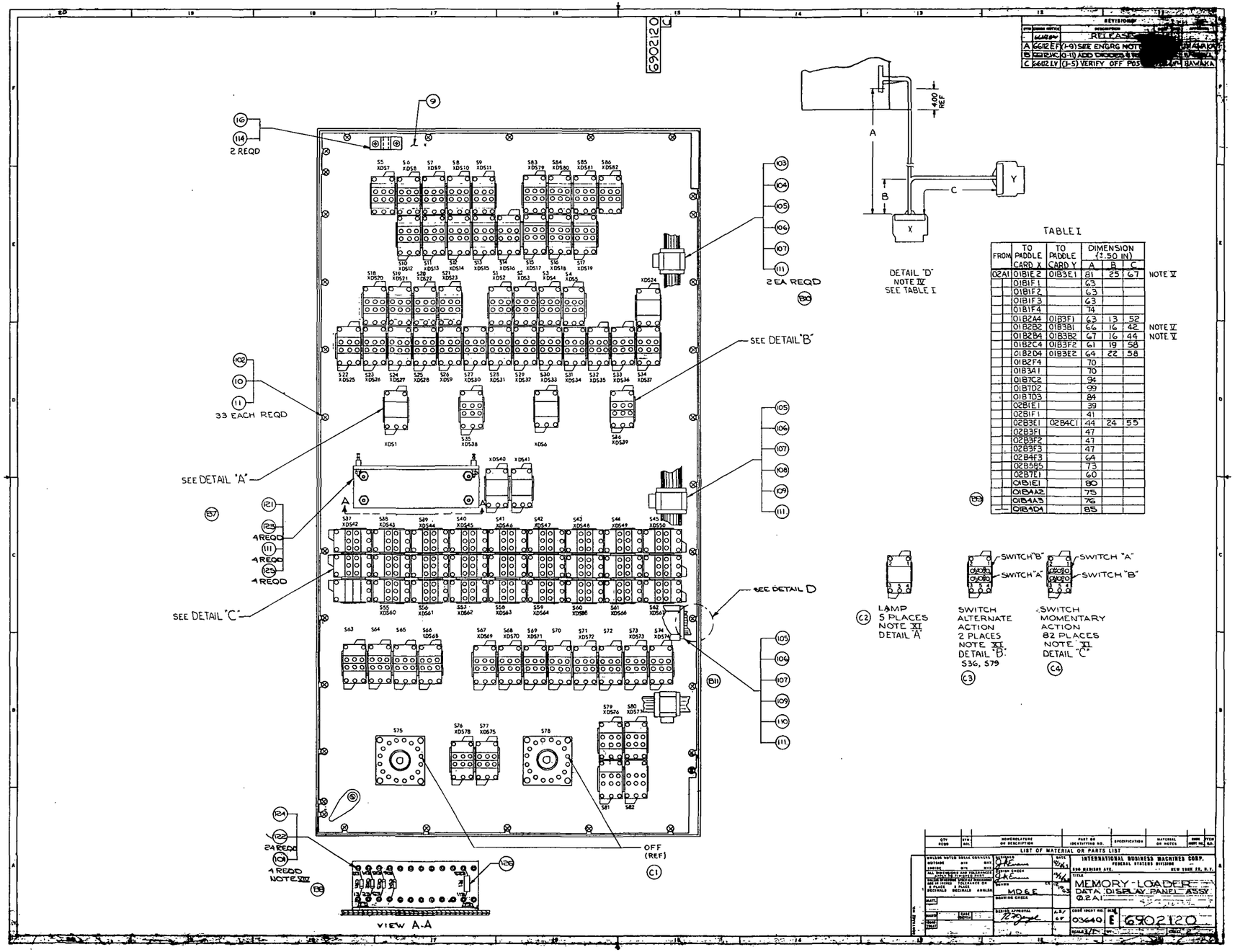


RES DES	ITEM NO.	RES DES	ITEM NO.
S1	19	S71	113
S2	20	S72	93
S3	21	S73	94
S4	22	S74	95
S5	24	S75	4
S6	25	S76	96
S7	26	S77	97
S8	27	S78	4
S9	28	S79	98
S10	29	S80	99
S11	30	S81	85
S12	31	S82	86
S13	32	S83	19
S14	33	S84	115
S15	34	S85	116
S16	35	S86	117
S17	36		
S18	37	XDS24	41
S19	38	XDS1	18
S20	39	XDS6	23
S21	40	XDS10	56
S22	42	XDS11	57
S23	43		
S24	44		
S25	45		
S26	46		
S27	47		
S28	48		
S29	49		
S30	50		
S31	51		
S32	52		
S33	53		
S34	54		
S35	55		
S36	100		
S37	58		
S38	59		
S39	60		
S40	61		
S41	62		
S42	63		
S43	64		
S44	65		
S45	66		
S46	67		
S47	68		
S48	69		
S49	70		
S50	71		
S51	72		
S52	73		
S53	74		
S54	75		
S55	77		
S56	78		
S57	79		
S58	80		
S59	81		
S60	82		
S61	83		
S62	84		
S63	85		
S64	86		
S65	87		
S66	88		
S67	89		
S68	90		
S69	91		
S70	92		

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (PART NO.)	ITEM NO.
1	V	RESISTOR	6017937				126
A		NUT HEX (6048630)	MS35649-64				125
AR		SOLDER (6032857)	SNDOTPEAR	QQ-S-571			124
4		SCREW (6035646)	MS24693C27				123
24	V	TERMINAL	6070330				122
1		TERMINAL BOARD	6902136				121
REF			6902199				120
REF			6902193				119
REF		WIRING LIST	6902192		NOTE XII		118
1			6080350				117
1			6080349				116
1	V	SWITCH ASSY	6080348				115
2		SCREW	6027605				114
1	V	SWITCH ASSY	6080046				113
1		LATCH	6079797				112
8		WASHER (6047219)	MS15795-306				111
1	V	CRADLE	6079354				110
2	V	CLIP	6079358				109
1	V	CRADLE	6079353				108
4		SCREW (6035710)	MS35216-26				107
4		SCREW (6035645)	MS24693C20				106
4		STAND-OFF	6477103				105
8	V	CLIP	6079357				104
2	V	CRADLE	6079352				103
33		WASHER (6098641)	MS15795-303				102
4		DIODE	492543			88360	101
1	V	SWITCH ASSY	6078693				100
			6078652				99
			6078658				98
			6078664				97
			6078708				96
			6078655				95
			6081038				94
			6078691				93
			6078717				92
			6078724				91
			6078709				90
			6078716				89
			6078653				88
			6078723				87
2			6078715				86
2			6078722				85
1			6078642				84
			6078641				83
			6078640				82
			6078639				81
			6078638				80
			6078637				79
			6078636				78

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE (PART NO.)	ITEM NO.
1	V	SWITCH ASSY	6078635				11
			6078703				76
			6078633				75
			6078632				74
			6078631				73
			6078630				72
			6078629				71
			6078628				70
			6078627				69
			6078626				68
			6078656				67
			6078651				66
			6078650				65
			6078649				64
			6078648				63
			6078647				62
			6078646				61
			6078645				60
			6078644				59
			6078657				58
			6078668				57
			6078669				56
			6078690				55
			6078619				54
			6078618				53
			6078617				52
			6078616				51
			6078615				50
			6078614				49
			6078613				48
			6078612				47
			6078611				46
			6078610				45
			6078609				44
			6078608				43
			6078634				42
			6078643				41
			6078623				40
			6078622				39
			6078621				38
			6078620				37
			6078601				36
			6078600				35
			6078599				34
			6078598				33
			6078597				32
			6078596				31
			6078625				30
			6078624				29
			6078734				28
			6078605				27
			6078604				26
			6078603				25
			6078602				24
			6078692				23
			6080353				22
			6080352				21
			6080351				20
2			6078736				19
1			6078735				18
168		LAMP	6078990				17
1		STRIKE	597097			88360	16
4		SCR, FIL HD (6028009)	AN500AD4-6				15
2		SET SCREW	2517956				14
2		HINGE PIN	597098				13
2		HINGE	597093			88360	12
37		LK WASHER (6029218)	MS35338-78				11
33		SCR, PAN HD (6035699)	MS35216-13				10
1		SUB PANEL	6902117				9
180		SCR, FLAT HD (6035644)	MS24693C28				8
1		BAR, LATCH	597087				7
2		BAR, PANEL	597089			88360	6
4		SCR, FLAT HD (6035658)	MS24693C48				5
2	V	SWITCH	6035437				4
2	V	KNOB	6072801				3
1		PANEL, OVERLAY	6902119				2
1		BAR, HINGE	597088			88360	1

Figure 10-34. Memory Loader and Data Display Panel (02A1) Assembly Drawing (Sheet 1 of 2)



FROM	TO PADDLE CARD X	TO PADDLE CARD Y	DIMENSION (±.50 IN) A	B	C	
02A1	01B1E2	01B3E1	81	25	67	NOTE V
	01B1F1		63			
	01B1F2		63			
	01B1F3		63			
	01B1F4		74			
	01B2A4	01B3F1	63	13	52	
	01B2B2	01B3B1	66	16	42	NOTE V
	01B2B4	01B3B2	67	16	44	NOTE V
	01B2C4	01B3F2	61	19	58	
	01B2D4	01B3E2	64	22	58	
	01B2F4		70			
	01B3A1		70			
	01B7C2		94			
	01B7D2		99			
	01B7D3		84			
	02B1E1		39			
	02B1F1		41			
	02B3E1	02B4C1	44	24	55	
	02B3F1		47			
	02B3F2		47			
	02B3F3		47			
	02B4F3		64			
	02B5B5		73			
	02B7E1		60			
	01B1E1		80			
	01B4A2		75			
	01B4A3		76			
	01B4D4		85			

Figure 10-34. Memory Loader and Data Display Panel (02A1) Assembly Drawing (Sheet 2)

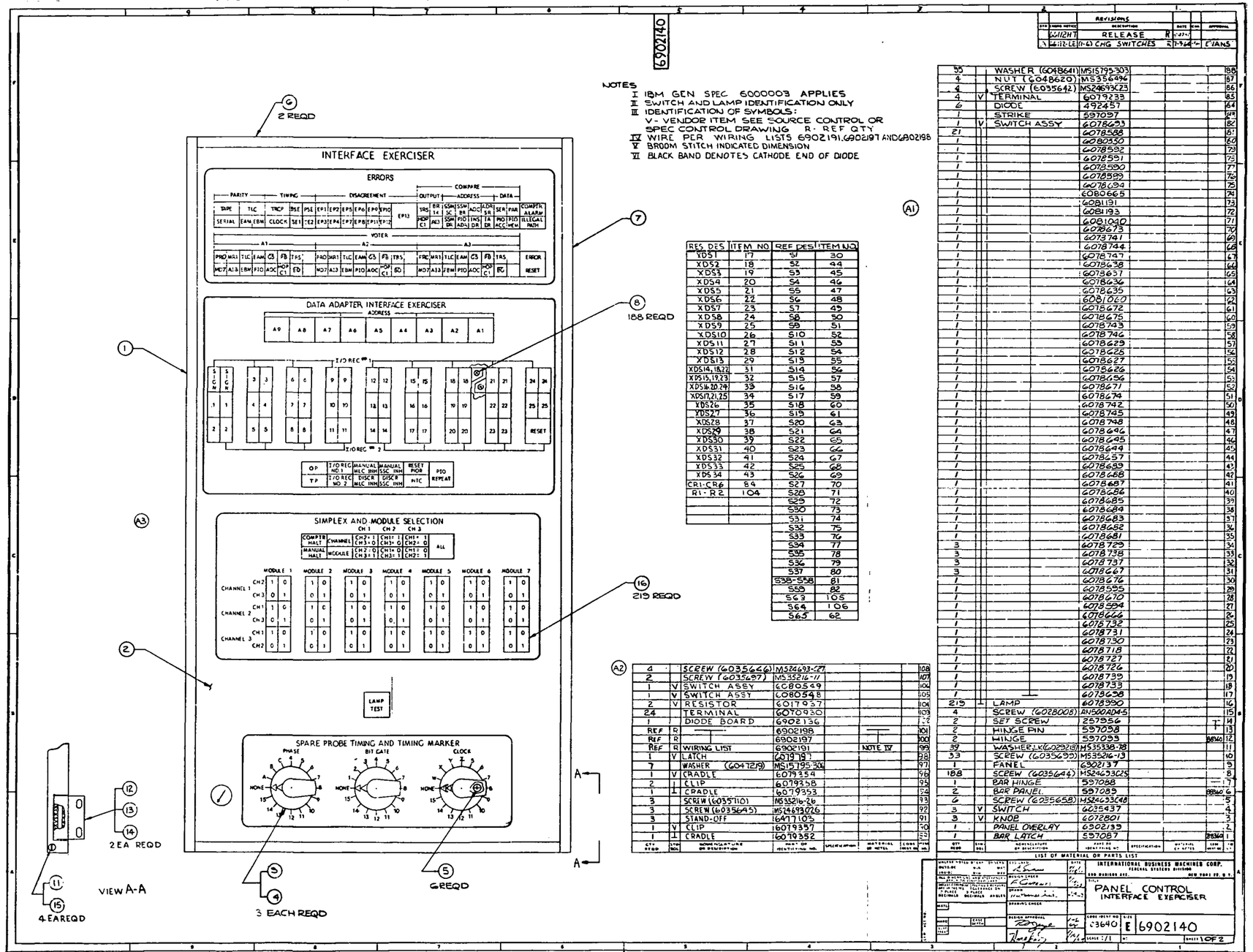


Figure 10-35. Interface Exerciser Panel (02A2) Assembly Drawing (Sheet 1 of 2)

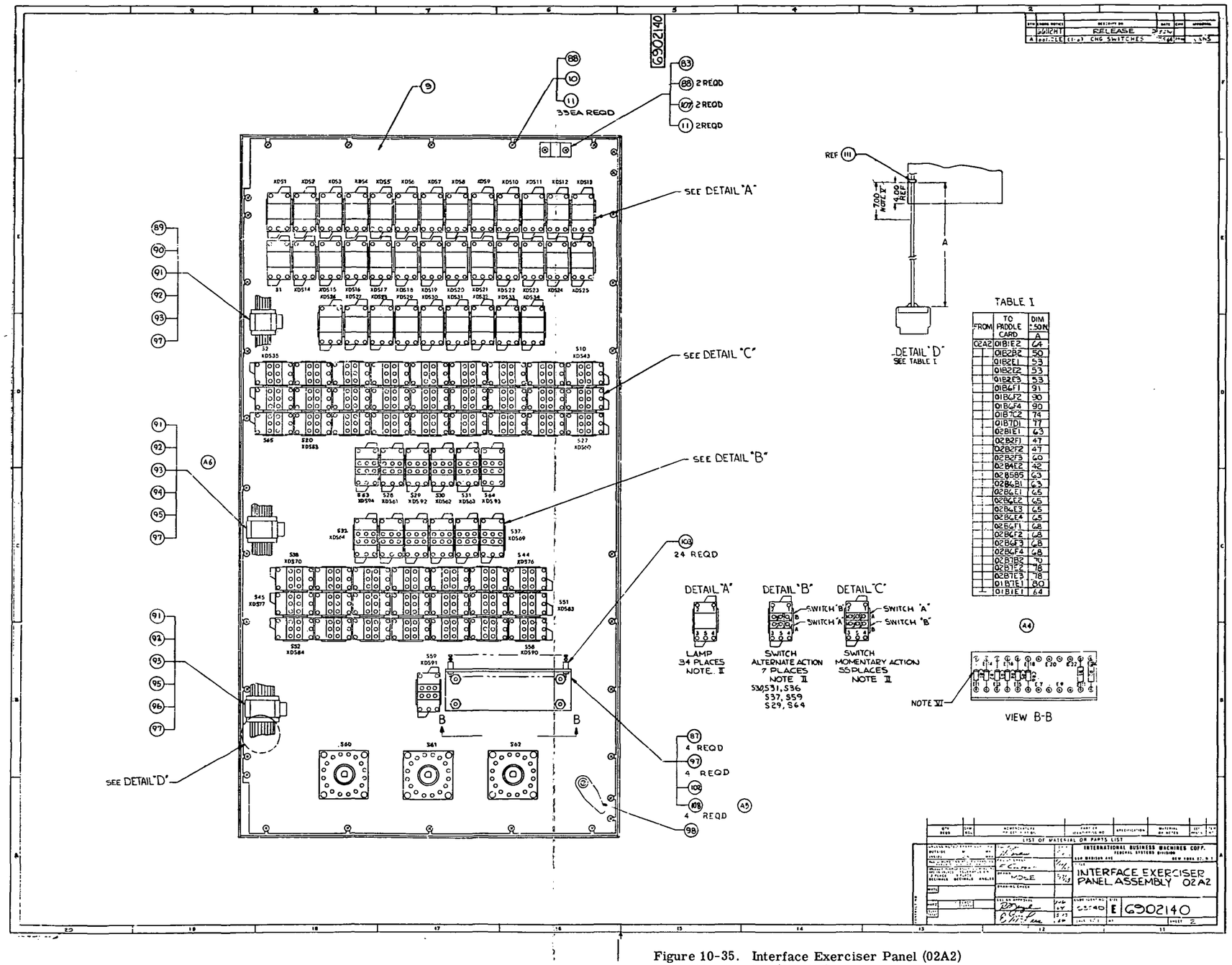
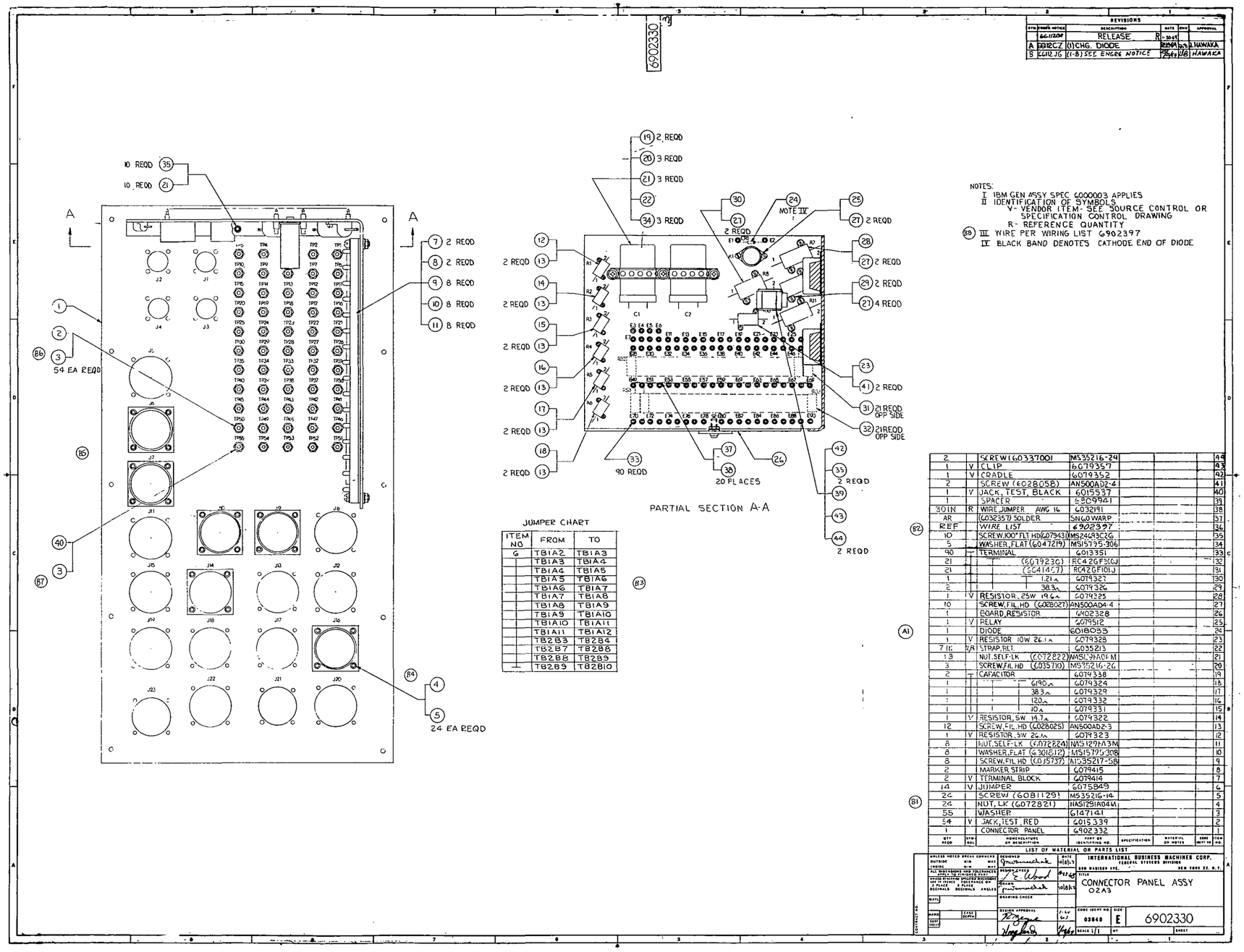


Figure 10-35. Interface Exerciser Panel (02A2) Assembly Drawing (Sheet 2)



ITEM NO	FROM	TO
6	TB1A2	TB1A3
	TB1A3	TB1A4
	TB1A4	TB1A5
	TB1A5	TB1A6
	TB1A6	TB1A7
	TB1A7	TB1A8
	TB1A8	TB1A9
	TB1A9	TB1A10
	TB1A10	TB1A11
	TB1A11	TB1A12
	TB2B3	TB2B4
	TB2B7	TB2B8
	TB2B8	TB2B9
—	TB2B9	TB2B10

2		SCREW (6033700)	MS35216-24			44
1	V	CLIP	6079357			43
1	V	CRADLE	6079352			42
2		SCREW (6028058)	AN500A02-4			41
1	V	JACK, TEST, BLACK	6015537			40
1		SPACER	6809941			39
30IN	R	WIRE, JUMPER AWG 16	6032191			38
AR		(6032357) SOLDER	SN60WARP			37
REF		WIRE LIST	6902397			36
10		SCREW, 100° FLT HD (607943)	MS24693C6			35
5		WASHER, FLAT (6047219)	MS15795-306			34
90		TERMINAL	6013351			33
21		(6079230)	RC42GF560J			32
21		(6041407)	RC42GF101J			31
1		1.21Ω	6079327			30
2		383Ω	6079326			29
1	V	RESISTOR, 25W 19.6Ω	6079329			28
10		SCREW, FIL HD (6028027)	AN500A04-4			27
1		BOARD, RESISTOR	6902328			26
1	V	RELAY	6079512			25
1		DIODE	6018033			24
1	V	RESISTOR 10W 26.1Ω	6079328			23
7 IN	RA	STRAP, RET	6035213			22
13		NUT, SELF-LK (6072822)	MS51921A04M			21
3		SCREW, FIL HD (6035710)	MS35216-26			20
2		CAPACITOR	6079338			19
1		6.90Ω	6079324			18
1		383Ω	6079329			17
1		120Ω	6079332			16
1		10Ω	6079331			15
1	V	RESISTOR, 5W 14.7Ω	6079322			14
12		SCREW, FIL HD (6028025)	AN500A02-3			13
1	V	RESISTOR, 5W 26.1Ω	6079323			12
8		NUT, SELF-LK (6072824)	MS21919A3M			11
8		WASHER, FLAT (6016112)	MS15795-308			10
8		SCREW, FIL HD (6035737)	MS35217-58			9
2		MARKER STRIP	6079415			8
2	V	TERMINAL BLOCK	6079414			7
14	V	JUMPER	6075849			6
24		SCREW (6081129)	MS35216-14			5
24		NUT, LK (6072821)	MS21919A04M			4
55		WASHER	6147141			3
54	V	JACK, TEST, RED	6015339			2
1		CONNECTOR PANEL	6902332			1

Figure 10-36. Control Panel (02A3) Assembly Drawing

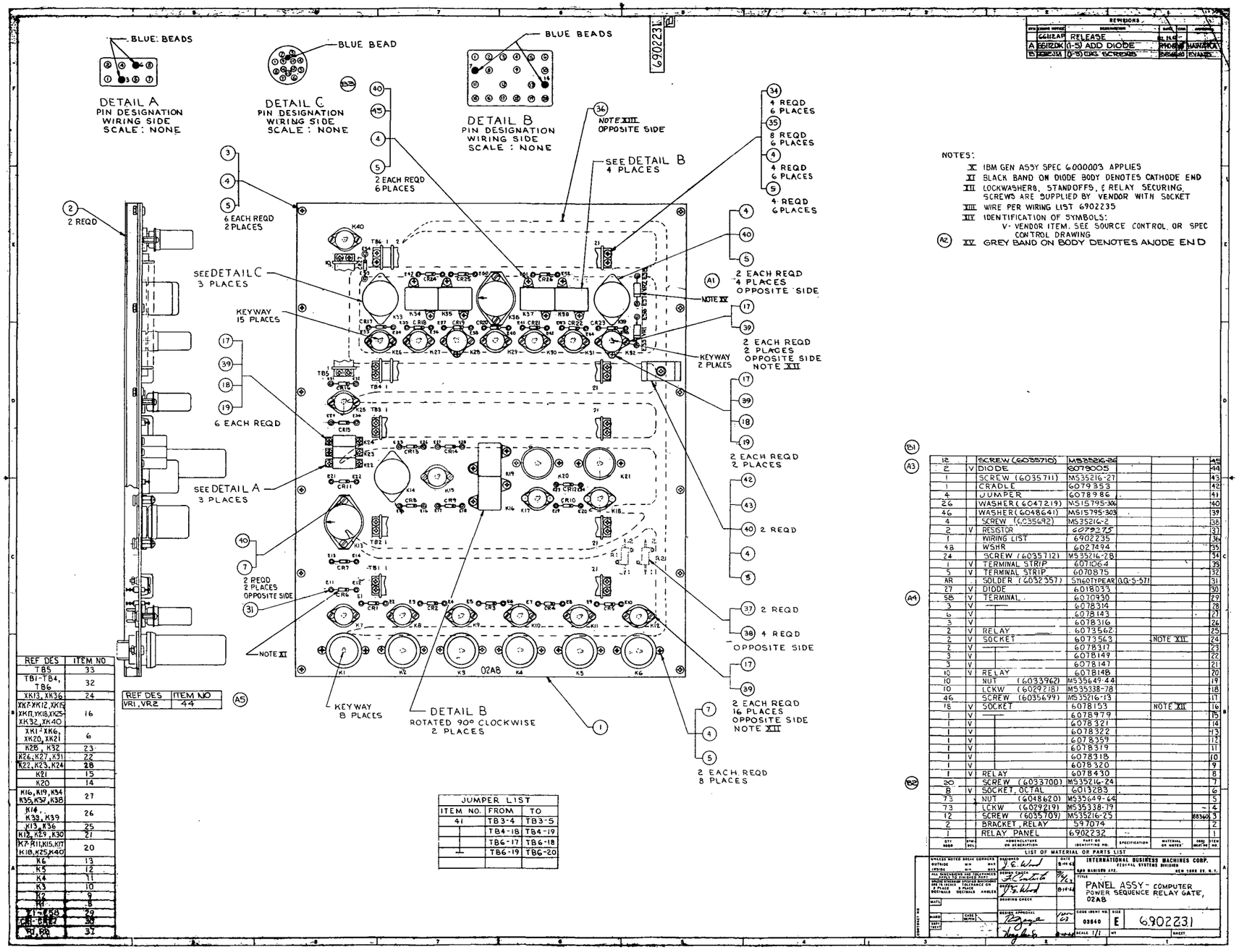


Figure 10-37. Computer Power Sequence Relay Gate (02A8) Assembly Drawing

Gate Assembly	IBM Part Number	"LN" Number	Number of Sheets
01B1	6902975	01.01.00.0	3
01B2	6902976	01.02.00.0	3
01B3	6902977	01.03.00.0	2
01B4	6902978	01.04.00.0	2
01B6	6902979	01.06.00.0	2
01B7	6902980	01.07.00.0	2
02B1	6906981	02.01.00.0	2
02B2	6902982	02.02.00.0	3
02B3	6902983	02.03.00.0	3
02B4	6902984	02.04.00.0	3
02B5	6902985	02.05.00.0	2
02B6	6902986	02.06.00.0	2
02B7	6902987	02.07.00.0	3
02B8	6902988	02.08.00.0	2

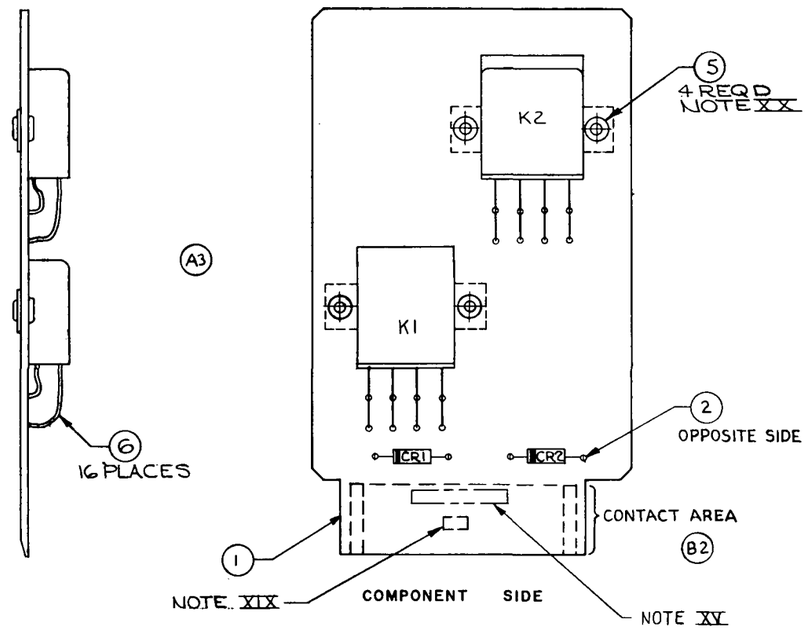
Figure 10-38. LVDCME Circuit Card Location Charts

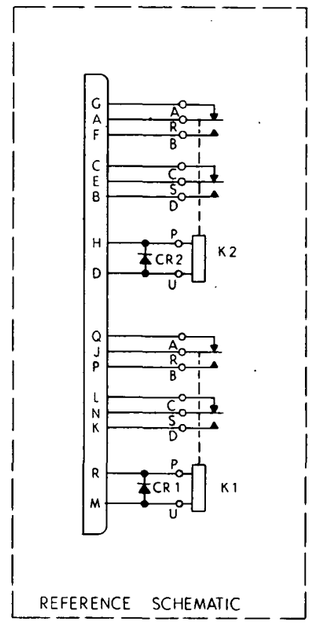
Gate Assembly	IBM Part Number	"LN" Number	Number of Sheets
01B1	6902969	01.01.00.0	5
01B2	6902970	01.02.00.0	5
01B3	6902971	01.03.00.0	4
01B4	6902972	01.04.00.0	6
01B6	6902973	01.06.00.0	5
01B7	6902974	01.07.00.0	5
02B1	6902989	02.01.00.0	4
02B2	6902990	02.02.00.0	4
02B3	6902991	02.03.00.0	4
02B4	6902992	02.04.00.0	5
02B5	6902993	02.05.00.0	4
02B6	6902994	02.06.00.0	4
02B7	6902997	02.07.00.0	3
02B8	6902998	02.08.00.0	1

Figure 10-39. LVDCME Edge Connector List

6901030 B

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BB	RELEASE	12.31.62		
A	66112 CJ	(1-3) SEE ENGRG NOTICE	8/20/63	JR	J.E. WOOD
B	66115 JF	(1-2) COATED WIRING TO PREVENT CORROSION	8/30/63		J.E. WOOD





NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901030 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REF QTY
A1 XIX MARK REVISION SYMBOL PER IBM SPEC 6009974 COLOR BLACK
XX RELAY MTG HOLES IN FLANGE MAY REQUIRE REAMING TO ACCEPT EYELET.
XXI ALL COPPER CONDUCTOR SURFACES SHALL BE TINNED WITH ITEM NO.2 OR THE CONDUCTOR (WIRING) SIDE OF THE CARD SHALL BE COATED WITH SEALANT ITEM NO.7. CONTACT AREA MUST BE KEPT FREE OFF SURFACE TREATMENT

B1

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
AR	V	SEALANT	6075477				7
16 IN.	V.R	SLEEVING	6032850				6
4	V	EYELET	6027021				5
2	V	RELAY	6080231				4
2	V	DIODE	6018033				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901017				1

A2

LIST OF MATERIAL OR PARTS LIST

REF DES	ITEM NO.
K2	4
K1	4
CR2	3
CR1	3

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J.E. Wood DATE 7-18-63
DESIGN CHECK F. Conklin 12-16-63
DRAWN J.E. Wood 7-18-63
DRAWING CHECK
DESIGN APPROVAL JR 12-26-62 / Hoagland 12-28-62

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE PRINTED CIRCUIT BOARD ASSY-RELAY CARD

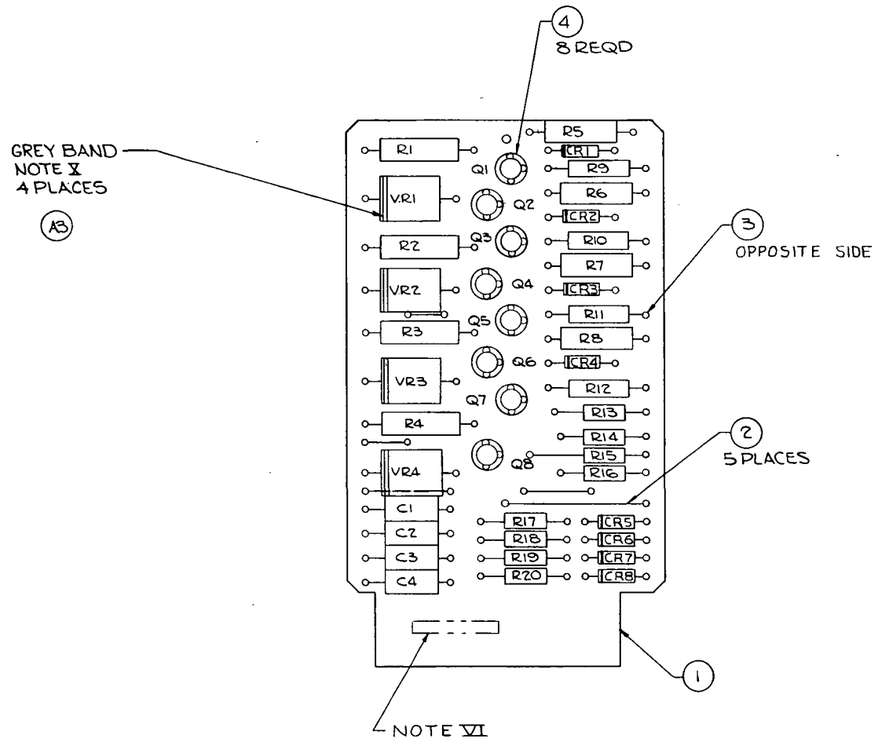
CODE IDENT NO. 03640 SIZE D 6901030
SCALE 2/1 WT SHEET

Figure 10-40. Relay Card Printed Circuit Board Assembly (6901030)

6901330 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BC	RELEASE	12-29-64		
A	66112DB	(1-3) ADD NOTE X	12-15-65		EVANS

NOTES
- I IBM GENERAL ASSEMBLY SPECIFICATION 6000003 APPLIES
- II MIN ELECTRICAL CLEARANCE TO BE .018
- III COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- IV COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN 06 INCHES
- V LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- VI PARTMARK 6901330 ASSY PER IBM SPEC 6009974 COLOR BLACK
- VII JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- VIII BLACK BAND DENOTES CATHODE END OF DIODE
- IX IDENTIFICATION OF SYMBOLS
  - V- VENDOR ITEM- SEE SPEC OR SOURCE CONTROL DWG
  - R- REFERENCE QUANTITY
- (A1) X GREY BAND ON (6) DENOTES ANODE SIDE OF DIODE



(A2)

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	RES, 1.4K, 1/8W, ±1%	6079011				13
4	V	RES, 1.24K, 1/8W, ±1%	6079010				12
4	V	RES, 1.1K, 1/4W, ±1%	6079008				11
4	V	RES, 383Ω, 1/2W, ±1%	6079047				10
4	V	RES, 402Ω, 1/2W, ±1%	6079009				9
8	V	TRANSISTOR	6079006				8
8	V	DIODE	6017645		NOTE VIII		7
4	V	DIODE, ZENER	6079005		NOTE X		6
4		CAP., .01UF, 100VDC ±10%	491228			88360	5
8		PAD	483070			88360	4
AR		SOLDER (6032357)	SN60 AR	QQ-S-571			3
10 IN	V,R	WIRE #22AWG, YEL	6036152				2
1		SMS CARD	6901331				1

LIST OF MATERIAL OR PARTS LIST

REF DES.	ITEM NO.
Q1 THRU Q8	8
R17 THRU R20	13
R13 THRU R16	12
R9 THRU R12	11
R5 THRU R8	10
R1 THRU R4	9
CR5 THRU CR8	7
CR1 THRU CR4	7
VR1 THRU VR4	6
C1 THRU C4	5

CIRCUIT	INPUT PIN	OUTPUT PIN
A	B	R
B	C	G
C	D	Q
D	E	F

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J.E. Wood 12-18-63
DESIGN CHECK F. Conklin 12-19-63
DRAWN MDSE 12-23-63
DRAWING CHECK
DESIGN APPROVAL 12-26-63 12-29-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

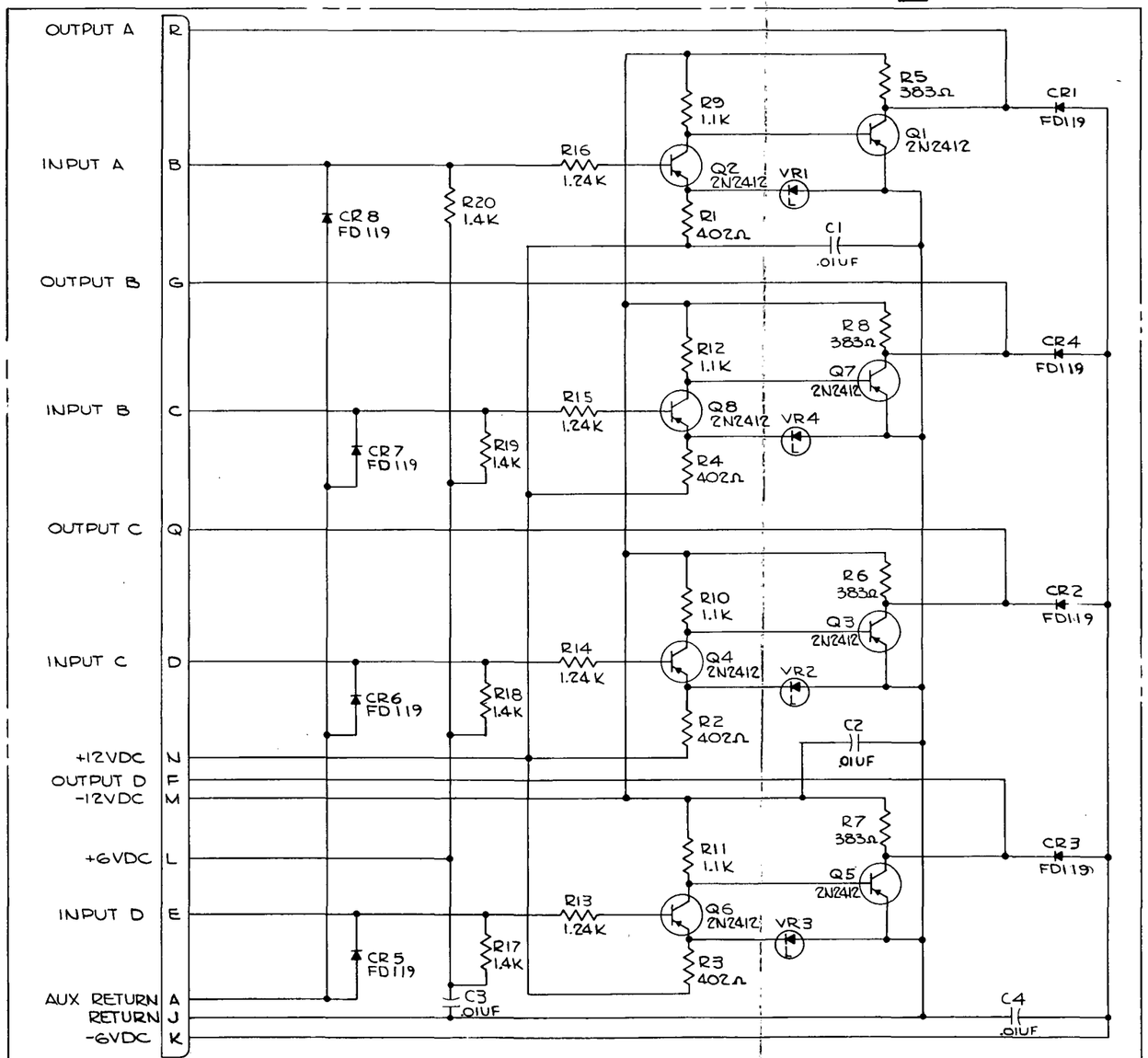
TITLE
PRINTED CIRCUIT BOARD ASSY-TRANSLATOR, AN1

CODE IDENT NO. 03640 SIZE D 6901330
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-41. AN1 Translator Printed Circuit Board Assembly (6901330) (Sheet 1 of 2)

6901330 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BC	RELEASE	11. 2.5		
A	66112DB	(1-3) ADD NOTE X	12/5/64		EVANS



QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS: OUTSIDE MIN MAX, INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS .03, 3 PLACE DECIMALS .010, ANGLES
MATL
HARD
SURF FREE
CASE DEPTH
CONTRACT NO.

DESIGNED J. E. Wood 9-10-63
DESIGN CHECK F. Contuto
DRAWN MD&E 10-25-63
DRAWING CHECK
DESIGN APPROVAL 10/28/63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY-TRANSLATOR, AN1

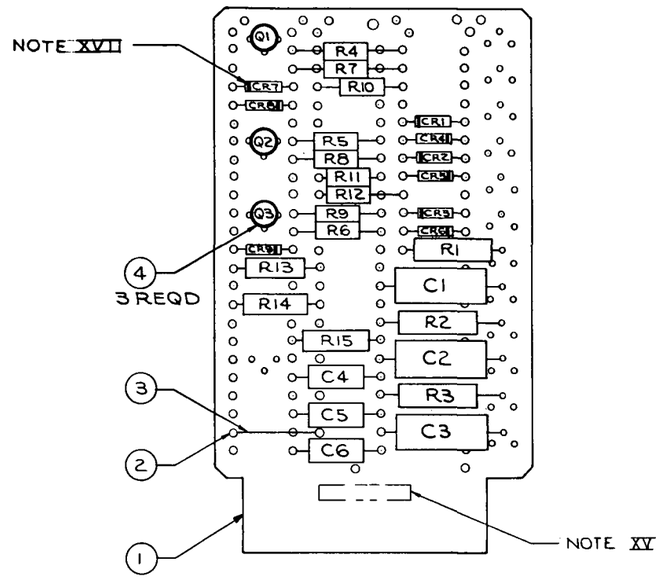
CODE IDENT NO. 03640 | SIZE D | 6901330

SCALE NONE WT SHEET 2

Figure 10-41. AN1 Translator Printed Circuit Board Assembly (6901330) (Sheet 2)

6901332 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BB	RELEASE	12.31.53		
A	66112 KG	(1) CHANGE TRANSISTOR	12-30-64		EVANS



COMPONENT SIDE

CIRCUIT	INPUT	SHIELD TIE OFF	OUTPUT
A	B	C	R
B	E	D	Q
C	A	F	G

R13-R15	13
R7 - R9	12
R4-6, R10-12	11
R1 - R3	10
Q1 - Q3	9
CR4-CR9	8
CR1-CR3	7
C4-C6	6
C1-C3	5
REF DES	ITEM NO.

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901332 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
3	V	261Ω ±1% 1/4W	6079209				13
3	V	3.01K ±1% 1/8W	6079214				12
6	V	10.5K ±1% 1/8W	6079211				11
3	V	RES. 267Ω ±1% 1/2W	6079206				10
3	V	TSTR	369587			88360	9
6	V	DIODE	6017645				8
3	V	DIODE	6079007				7
3		CAP. .01UF ±10% 100V DC	491228				6
3		CAP. .1UF ±5% 100V DC	491320				5
3		PAD	483070			88360	4
2 IN.	V,R	WIRE, 22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901333				1

(A1)

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD SURF TREAT CASE DEPTH
CONTRACT NO.

DESIGNED J. E. Wood 9-11-63
DESIGN CHECK T. Conturo 12-4-63
DRAWN M. Dee 9/NV/63
DRAWING CHECK
DESIGN APPROVAL 12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

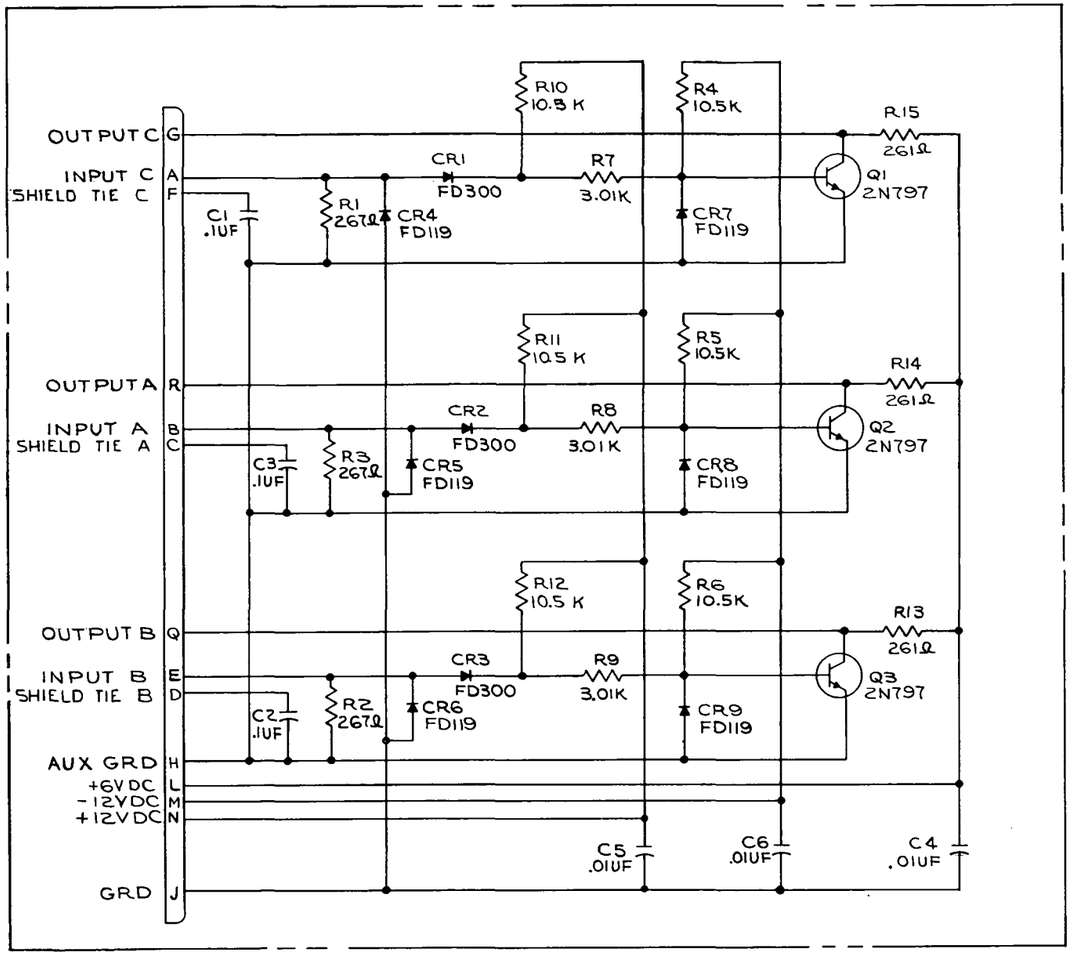
TITLE
PRINTED CIRCUIT BOARD ASSY- AN2 TRANSLATOR

CODE IDENT NO. 03640 SIZE D 6901332
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-42. AN2 Translator Printed Circuit Board Assembly (6901332) (Sheet 1 of 2)

6901332 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BB	RELEASE	7/2-1-[illegible]		
A	66112HG	(1) CHANGE TRANSISTOR	8-5-64	[illegible]	EVANS



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED G. E. Wood 9-11-63
DESIGN CHECK J. Conforto 12-26-63
DRAWN MD-E 9/11/63
DRAWING CHECK
DESIGN APPROVAL [illegible] 12-26-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

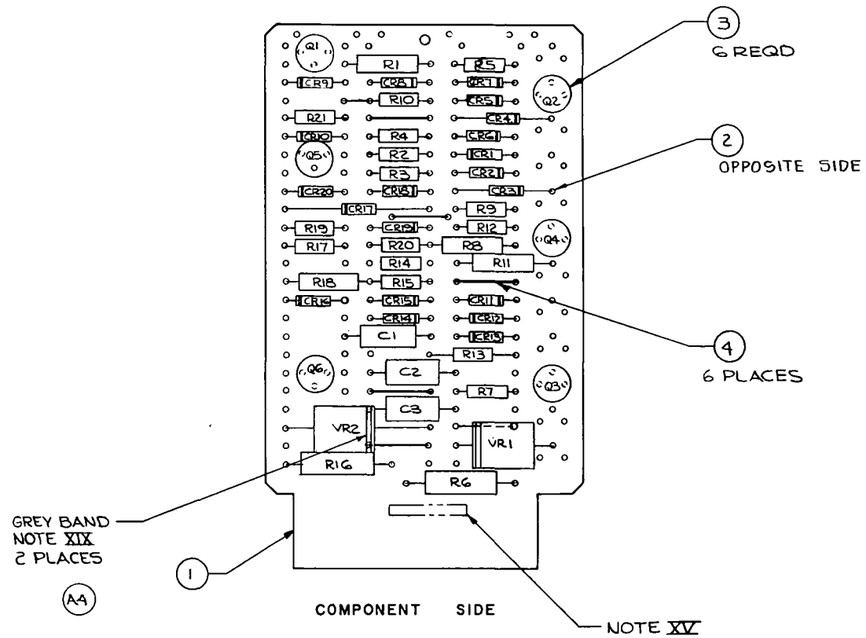
TITLE
PRINTED CIRCUIT BOARD ASSY- AN2 TRANSLATOR

CODE IDENT NO. 03640 | SIZE D | 6901332
SCALE NONE | WT | SHEET 2

Figure 10-42. AN2 Translator Printed Circuit Board Assembly (6901332) (Sheet 2)

6901336 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BC	RELEASE	8/ 2.[illegible]		
A	66112DB	(1-4) ADD NOTE XIX	12/3/64	[illegible]	EVANS



A1

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901336. ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX GREY BAND ON (5) DENOTES ANODE SIDE OF DIODE

A2

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
2	T	DIODE, ZENER	6079005		NOTE XIX		15
2	T	1.24K, 1/8W, ±1%	6079010				14
2	T	402Ω, 1/2W, ±1%	6079009				13
3	T	1.8K, 1/8W, ±1%	6079218				12
6	T	1.5K, 1/8W, ±1%	6079215				11
4	T	7.8K, 1/8W ± 1%	6079212				10
4		RES, 280Ω, 1/4W ± 1%	6079208				9
2		TRANSISTOR	6079006				8
4		TRANSISTOR	6079221				7
20	V	DIODE	6017645		NOTE XVII		6
3		CAP. 01UF, ±10%, 100VDC	491228			88360	5
15 IN	R	WIRE, #22 AWG	6036152				4
6		TRANSISTOR PAD	483070			88360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901337				1

LIST OF MATERIAL OR PARTS LIST

A3

CIRCUIT	INPUT PIN	RESET	OUTPUT PIN	ERROR TEST
A	A	D	C	R
B	F	G	Q	

A4

VR1, VR2	15
R7, R17	14
R6, R16	13
R5, R15, R21	12
R3, 4, 10, 13, 14, 20	11
R2, R9, R12, R8	10
R1, R8, R11, R18	9
Q3, Q6	8
Q1, 2, 4, 5	7
CR1-CR20	6
C1-C3	5
REF DES	ITEM NO.

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD
SURF TREAT
CASE DEPTH
CONTRACT NO.

DESIGNED J.E. Wood 9-13-65
DESIGN CHECK 9/14/65
DRAWN MDEE 9-18-65
DRAWING CHECK
DESIGN APPROVAL 12-17 65

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

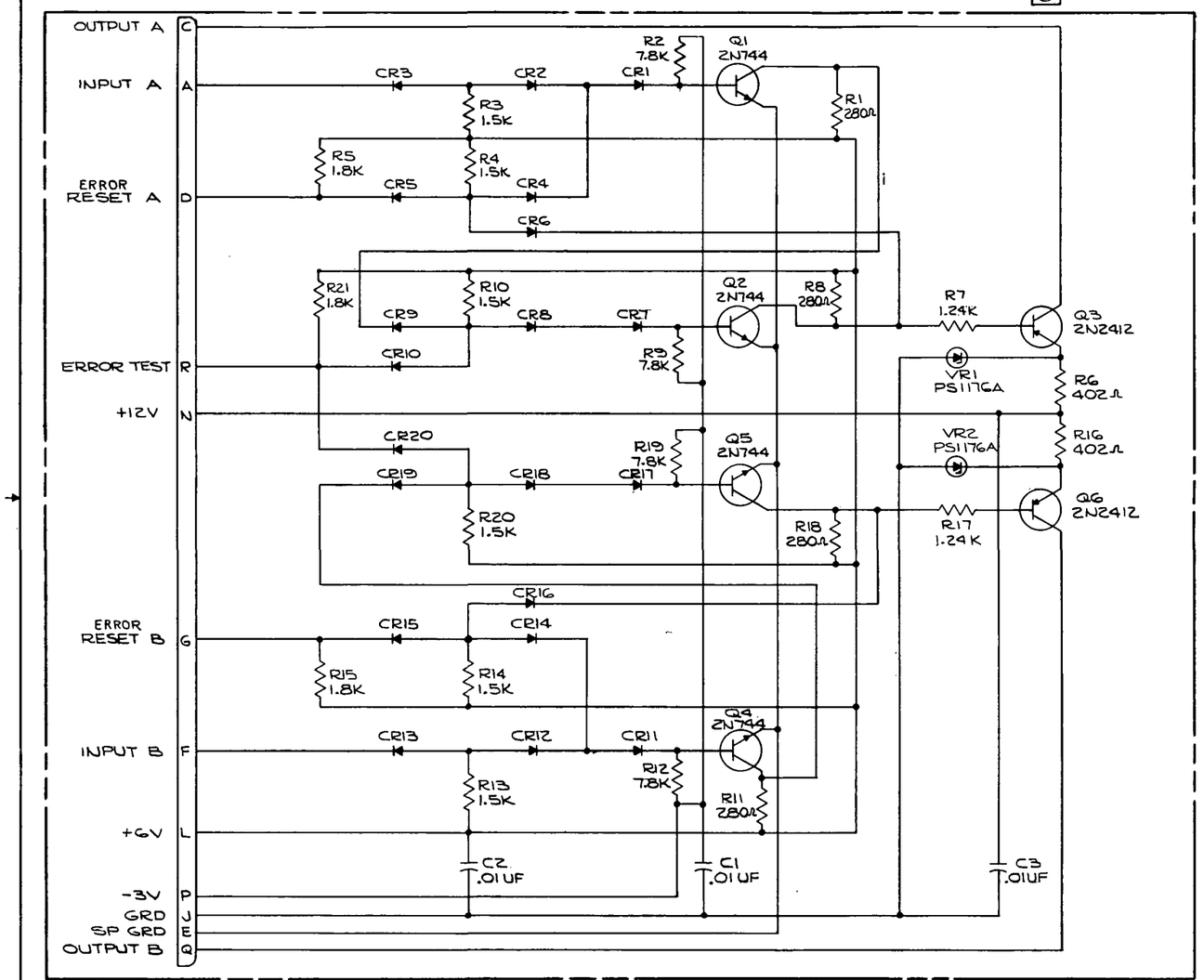
TITLE
PRINTED CIRCUIT BOARD ASSY- TC1, DD1 DETECT

CODE IDENT NO. 03640 | SIZE D | 6901336
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-43. TC1, DD1 Detect Printed Circuit Board Assembly (6901336) (Sheet 1 of 2)

6901336 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BC	RELEASE	[illegible]		
A	66112DB	(1-A) ADD NOTE XIX	12/13/63		EVANS



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS: OUTSIDE MIN MAX; INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES ± TOLERANCE ON 2 PLACE DECIMALS, 3 PLACE DECIMALS, ANGLES
MATL
HARD — CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Wood 9-24-62
DESIGN CHECK [illegible] 9/24/62
DRAWN MDE.E 9-18-63
DRAWING CHECK
DESIGN APPROVAL [illegible] for 10-8-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

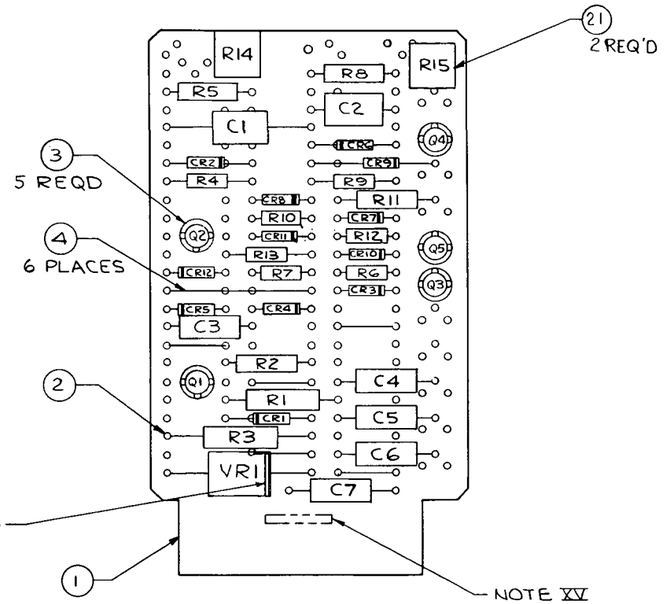
TITLE
PRINTED CIRCUIT BOARD ASSY- TC1, DD1 DETECT

CODE IDENT NO. 03640 | SIZE D | 6901336
SCALE NONE WT SHEET 2

Figure 10-43. TC1, DD1 Detect Printed Circuit Board Assembly (6901336) (Sheet 2)

6901338 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 BC	RELEASE	9/7		
A	66112 DB	(1-A) ADD NOTE XX	12/13 63		EVANS



COMPONENT SIDE

VR1	20
R14, R15	19
R11	18
R7, R10, R13	17
R6, R9, R12	16
R5, R8	15
R4	14
R3	13
R2	12
R1	11
Q3, Q4, Q5	10
Q1, Q2	9
CR2, CR6	8
CR9 THRU CR12	
CR5, CR7, CR8	7
CR1, CR3, CR4	
C3 THRU C7	6
C1, C2	5
REF DES	ITEM NO.

INPUT	OUT PUT	TEST POINT 1	TEST POINT 2
R	Q	C	D

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901338 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM - SEE SPEC OR SOURCE CONTROL DWG
R-REFERANCE QUANTITY
XIX PIN A IN TC2 CARD RECPTACLE MUST BE TIED TO PIN H
XX GREY BAND ON (20) DENOTES ANODE SIDE OF DIODE

A1

A2

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
2		PAD	491299			88360	21
1	V	DIODE ZENER	6079005		NOTE XX		20
2	V	POT. 5K ±5%	6079276				19
1	V	280Ω, ±1%, 1/4W	6079208				18
3	V	1.5K, ±1%, 1/8W	6079219				17
3	V	7.8K, ±1%, 1/8W	6079212				16
2	V	205Ω, ±1%, 1/4W	6079210				15
1	V	2.49K, ±1%, 1/8W	6079217				14
1	V	402Ω, ±1%, 1/2W	6079009				13
1	V	1.10K, ±1%, 1/4W	6079008				12
1	V	RES 383Ω, ±1%, 1/2W	6079047				11
3	V	TRANSISTOR	6079221				10
2	V	TRANSISTOR	6079006				9
2	V	DIODE	6079007				8
10	V	DIODE	6017645		NOTE XVII		7
5	V	CAP. .01UF, ± 10%, 100VDC	491228			88360	6
2		CAP.	6079202				5
10 IN.	V R	WIRE #22 AWG YELLOW	6036152				4
5		PAD	483070			88360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901339				1

A3

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Wood 9-1963
DESIGN CHECK 9/24/63
DRAWN MDE 9/13/63
DRAWING CHECK
DESIGN APPROVAL 12-13 63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY - TC2, $\overline{B0}$ DETECT

CODE IDENT NO. 03640 | SIZE D | 6901338
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-44. TC2, $\overline{B0}$ Detect Printed Circuit Board Assembly (6901338) (Sheet 1 of 2)

6901338 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BC	RELEASE	11. 2. 63		
A	66112DB	(1:4) ADD NOTE XX	12/13/64	JEW	EVANS

OUTPUT Q
TP1 C
INPUT R
TP2 D
-3VDC P
-6VDC K
-12VDC M
+6VDC L
+12VDC N
GRD J
AUX GRD A

R14 5K
R5 205Ω
R7 1.5K
R1 383Ω
R2 1.10K
CR1 FD119
Q1 2N2412
CR2 FD300
Q2 2N2412
CR5 FD119
CR4 FD119
CR3 FD119
Q3 2N744
C1 680PF
R4 2.49K
R3 402Ω
VR1 PS1176A
R6 7.8K
R15 5K
R13 1.5K
R12 7.8K
R11 280Ω
R10 1.5K
R9 7.8K
R8 205Ω
CR6 FD300
C2 680PF
CR9 FD119
CR8 FD119
CR7 FD119
CR12 FD119
CR11 FD119
CR10 FD119
Q5 2N744
Q4 2N744
C3 .01UF
C6 .01UF
C7 .01UF
C4 .01UF
C5 .01UF

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES 2 PLACE ± 3 PLACE ± DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J.E. Word DATE
DESIGN CHECK 11/1/63
DRAWN MDE 11/26/63
DRAWING CHECK
DESIGN APPROVAL 12/8/63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

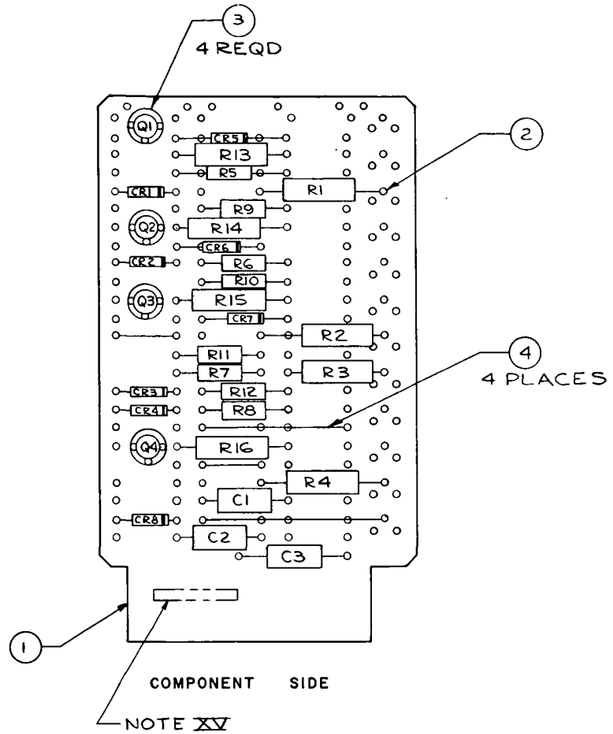
TITLE
PRINTED CIRCUIT BOARD ASSY-TC2, $\overline{B0}$ DETECT

CODE IDENT NO. 03640 | SIZE D | 6901338
SCALE NONE | WT | SHEET 2

Figure 10-44. TC2, $\overline{B0}$ Detect Printed Circuit Board Assembly (6901338) (Sheet 2)

6901340

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112 B8	RELEASE	12-11-63		



CIRCUIT	INPUT	OUTPUT
A	C	A
B	D	B
C	E	R
D	F	Q

C1, C2, C3	5
CR1 THRU CR8	6
Q1 — Q4	7
R1 — R4	8
R5 — R8	9
R9 — R12	10
R13 — R16	11
REF DES	ITEM NO.

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901340 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL BWG
R- REFERENCE QUANTITY

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	RES 750Ω, ±1% 1/2W	6079204				11
4	V	RES 4.75K, ±1%, 1/8W	6079213				10
4	V	RES 2.61K, ±1%, 1/8W	6079215				9
4	V	RES 768Ω, ±1%, 1/2W	6079229				8
4	V	TRANSISTOR	6079221				7
8	V	DIODE	6017645				6
3		CAP. 01UF, ±10%, 100VDC	491228			88360	5
10 IN.	V,R	WIRE #22 AWG YELLOW	6036152				4
4		PAD	483070			88360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901341				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED D E Wood 9-20-63
DESIGN CHECK 9/24/63
DRAWN MDE 9/14/63
DRAWING CHECK
DESIGN APPROVAL 12-17-63
12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

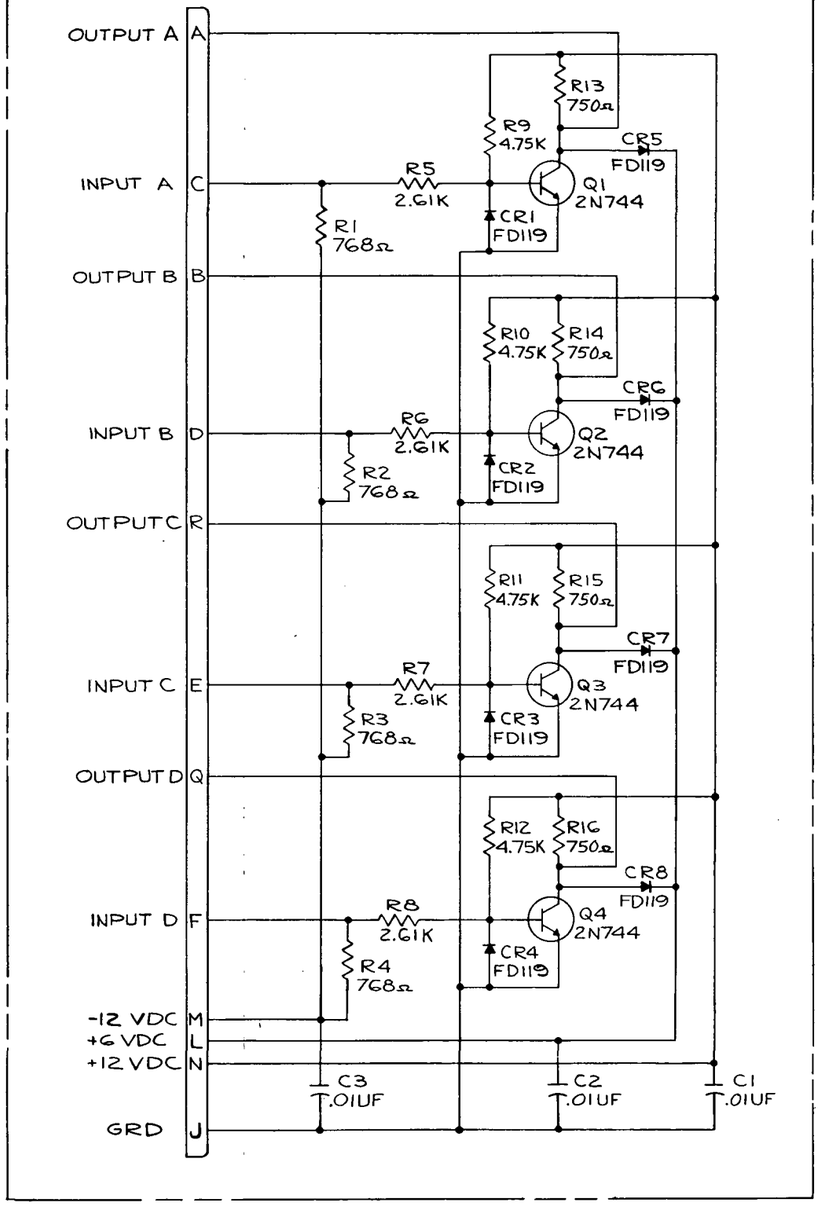
TITLE
PRINTED CIRCUIT BOARD ASSY-NA1, TRANSLATOR

CODE IDENT NO. 03640 | SIZE D | 6901340
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-45. NA1 Translator Printed Circuit Board Assembly (6901340) (Sheet 1 of 2)

6901340

REVISIONS					
BYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	661128B	RELEASE	12 31 63		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
LIST OF MATERIAL OR PARTS LIST							

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES

MATL
HARD — CASE DEPTH
SURF TREAT

CONTRACT NO.

DESIGNED J. E. Wood — DATE 9-10-63
DESIGN CHECK — 9/19/63
DRAWN MDE — 9/19/63
DRAWING CHECK
DESIGN APPROVAL — 9/19/63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

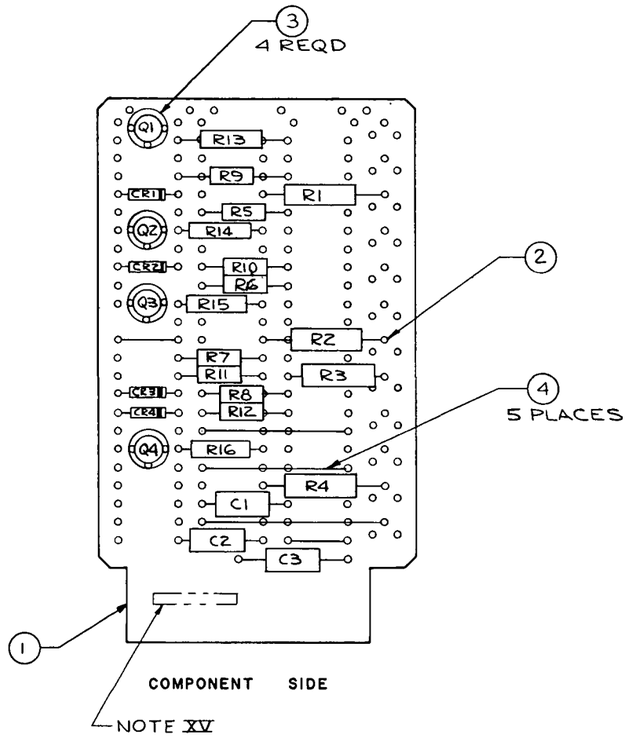
TITLE
PRINTED CIRCUIT BOARD ASSY- NA1, TRANSLATOR

CODE IDENT NO. 03640 — SIZE D — 6901340
SCALE NONE — WT — SHEET 2

Figure 10-45. NA1 Translator Printed Circuit Board Assembly (6901340) (Sheet 2)

690134 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6611288	RELEASE	12.31.63		
A	GG112HG	(1) CHANGE TRANSISTOR	2-8-64	%	EVANS



CIRCUIT	INPUT	OUTPUT
A	C	A
B	D	B
C	E	R
D	F	Q

C1,C2,C3	5
CR1 THRU CR4	6
Q1 — Q4	7
R1 — R4	8
R5 — R8	9
R9 — R12	10
R13 — R16	11
REF DES	ITEM NO.

NOTES
- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6901342 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	RES 330Ω ±1%, 1/4W	6079238				11
4	V	RES 1.58K, ±1%, 1/8W	6079235				10
4	V	RES 3.32Ω ±1%, 1/8W	6079236				9
4	V	RES 768Ω, ±1%, 1/2W	6079229				8
4	V	TRANSISTORS	369587				7
4	V	DIODE	6017645				6
3		CAP. 01UF, ± 10%, 100VDC	491228			88360	5
10 IN.	V,R	WIRE #22 AWG YELLOW	6036152				4
4		PAD	483070			88360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901341				1

(A1)

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

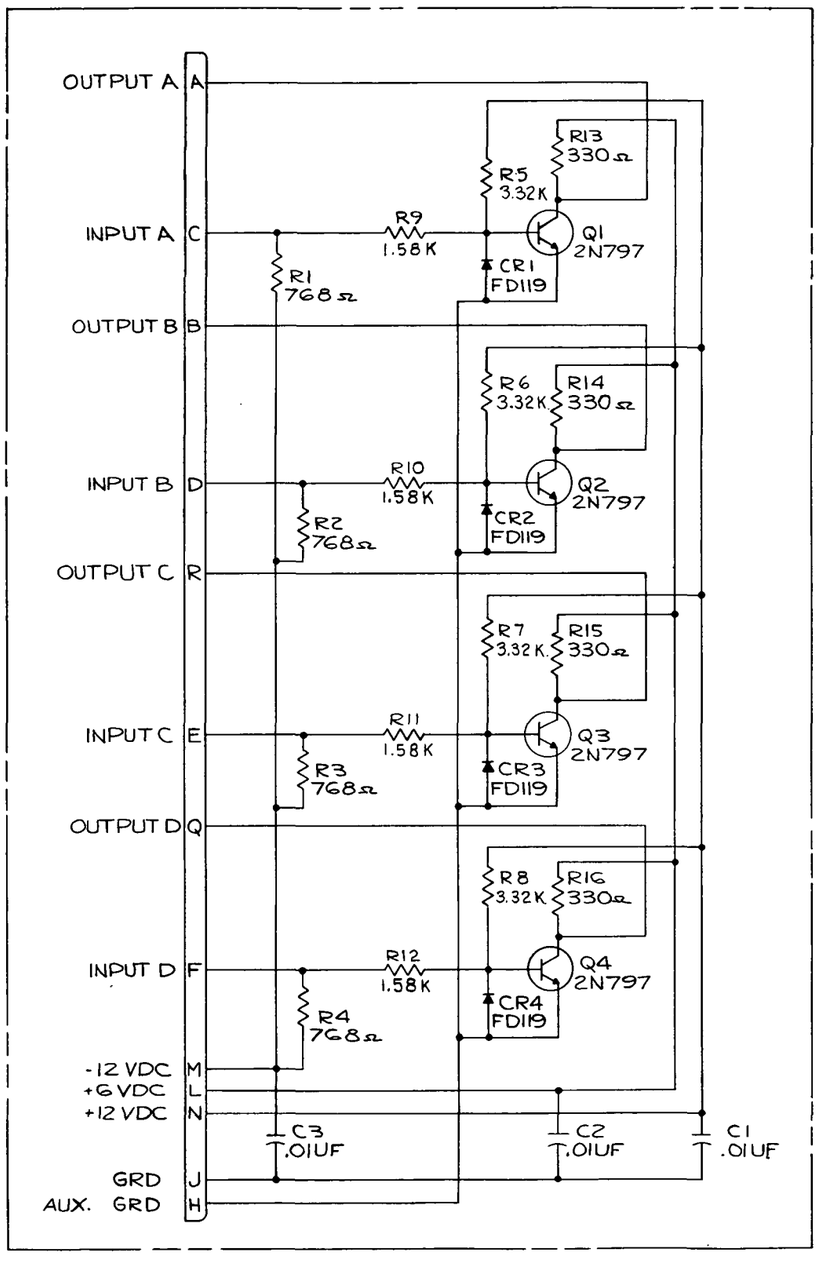
DESIGNED J. G. Wood 9-20-63
DESIGN CHECK 9/24/63
DRAWN MDE 9/11/63
DRAWING CHECK
DESIGN APPROVAL 9/24/63 12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY - NA2, TRASLATOR

CODE IDENT NO. 03640 | SIZE D | 6901342
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-46. NA2 Translator Printed Circuit Board Assembly (6901342) (Sheet 1 of 2)



6901342 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BB	RELEASE	12-11-63		
A	66121HG	(1) CHANGE TRANSISTOR	12-18-63	KA	EVANS

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED J. E. Ward 9-10-63
DESIGN CHECK Tony Allocca 9/26/63
DRAWN MDE 9/12/63
DRAWING CHECK
DESIGN APPROVAL W. Page 12-24-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

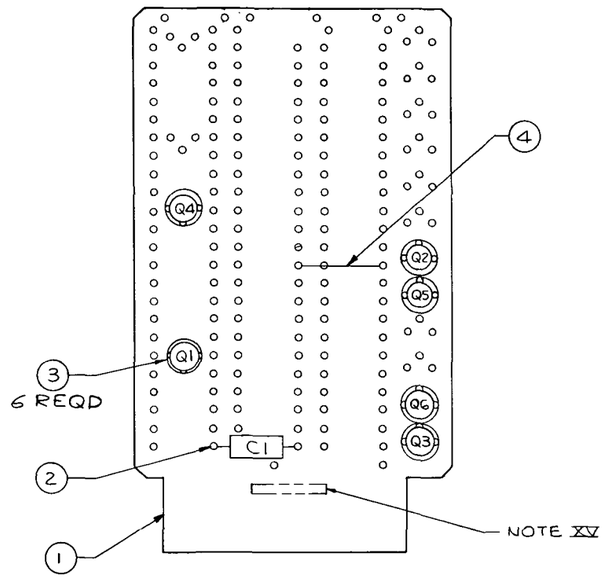
TITLE
PRINTED CIRCUIT BOARD ASSY- NA2, TRANSLATOR

CONTRACT NO.
CODE IDENT NO. 03640
SIZE D
6901342
SCALE NONE WT
SHEET 2

Figure 10-46. NA2 Translator Printed Circuit Board Assembly (6901342) (Sheet 2)

6901344

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BB	RELEASE			



COMPONENT SIDE

CIRCUIT	INPUT	OUTPUT
A	B	A
B	C	D
C	Q	R

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901344 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

REF DES	ITEM NO.
Q4,Q5,Q6	7
Q1,Q2,Q3	6
C1	5

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
3	V	TRANSISTOR	6079006				7
3	V	TRANSISTOR	6020887				6
1		CAP.01UF,±10%,100VDC	491228			88360	5
5 IN.	V/R	WIRE #22 AWG YELLOW	6036152				4
6		PAD	483070			88360	3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901345				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON: 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J.E. Word 9-20-63
DESIGN CHECK 9/30/63
DRAWN MDE 9/13/63
DRAWING CHECK
DESIGN APPROVAL 12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

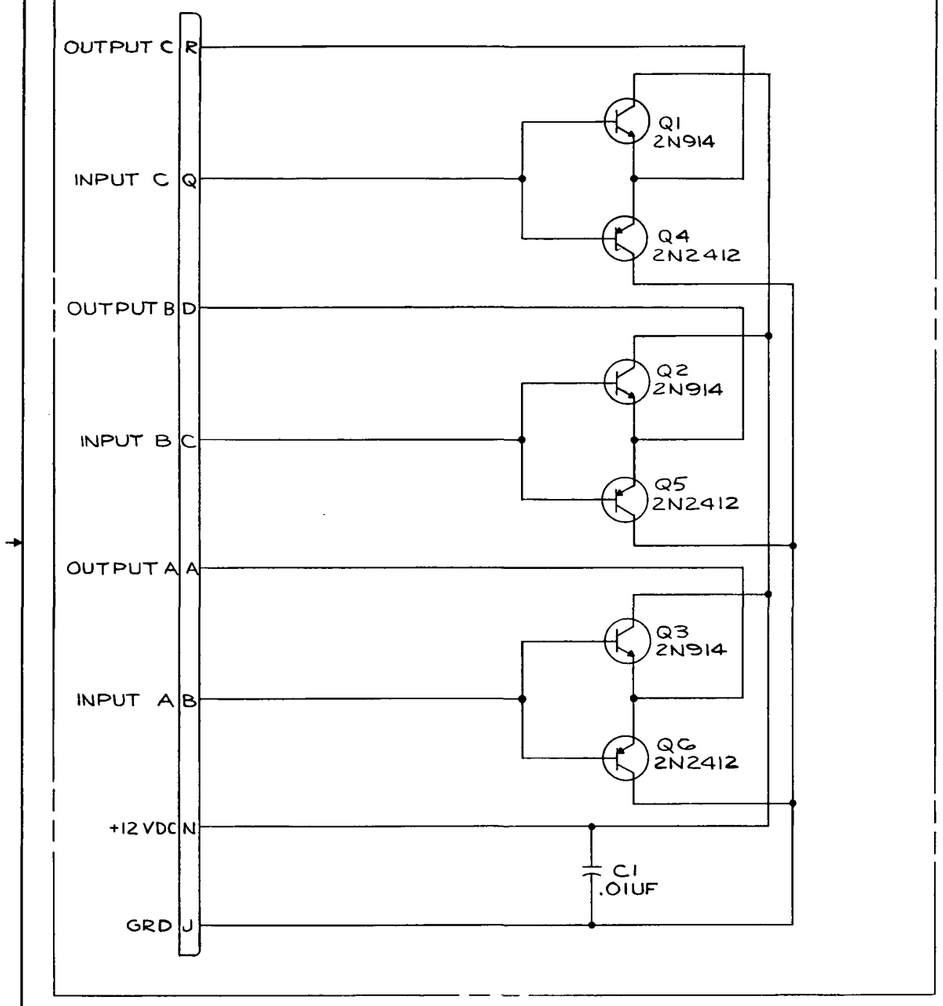
TITLE
PRINTED CIRCUIT BOARD ASSY-SC1, SIMULATOR

CODE IDENT NO. 03640 SIZE D 6901344
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-47. SC1 Simulator Printed Circuit Board Assembly (6901344) (Sheet 1 of 2)

6901344

REVISIONS					
BYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6611238	RELEASE	12.31 63		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS ON SIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 2 PLACE DECIMALS ± 3 PLACE DECIMALS ± ANGLES ±
MATL
HARD
SURF TREAT
CASE DEPTH
CONTRACT NO.

DESIGNED	K.E. Wood	DATE 9-24-63
DESIGN CHECK	Tom Allison	9/26/63
DRAWN	MDE	9/13/63
DRAWING CHECK		
DESIGN APPROVAL		10-21-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT BOARD ASSY - SC1, SIMULATOR

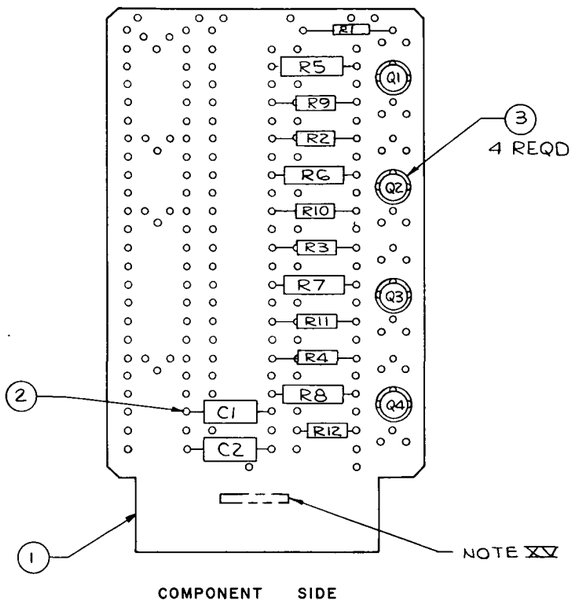
CODE IDENT NO. 03640 | SIZE D | 6901344

SCALE NONE | WT | SHEET 2

Figure 10-47. SC1 Simulator Printed Circuit Board Assembly (6901344) (Sheet 2)

6901346

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112DS	RELEASE	8-31-64		



COMPONENT SIDE

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901346 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL BWG
XIX 4 CIRCUITS PER BOARD

CIRCUIT	INPUT	OUTPUT
A	G	B
B	F	C
C	E	D
D	R	A

R9 THRU R12	8
R5 THRU R8	7
R1 THRU R4	6
Q1 THRU Q4	5
C1, C2	4
REF DES	ITEM NO.

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	RES 750Ω, ±1%, 1/8W	6079223				8
4	V	RES 200Ω, ±1%, 1/4W	6079237				7
4	V	RES 1.5K, ±1%, 1/8W	6079219				6
4	V	TRANSISTOR (2N744)	6079221				5
2		CAP. 01UF, ±10%, 100VDC	491228				4
4		PAD	483070				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901347				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD SURF TREAT CASE DEPTH
CONTRACT NO.

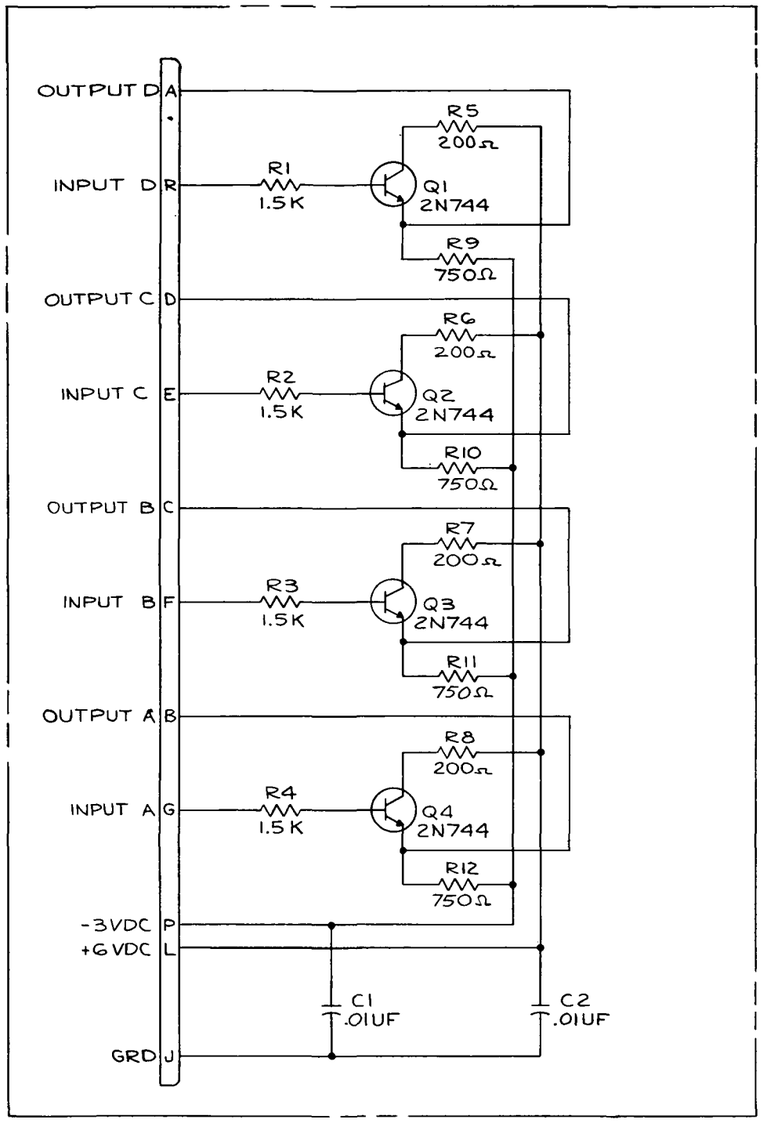
DESIGNED J.E. Wood 9-20-63
DESIGN CHECK Tony Alfonsi 9/29/63
DRAWN MDE 9/13/63
DRAWING CHECK
DESIGN APPROVAL J. Consuto 9/4/63
D. Boyd 2-17-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY-SC2, SIMULATOR

CODE IDENT NO. 03640 SIZE D 6901346
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-48. SC2 Simulator Printed Circuit Board Assembly (6901346) (Sheet 1 of 2)



6901346

REVISIONS					
BYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66 WRDS	RELEASE	9-3-64		

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD
SURF TREAT
4 CASE DEPTH
CONTRACT NO.

		DATE
DESIGNED	J.E. Wood	9-20-63
DESIGN CHECK	Tom Albert	9/20/63
DRAWN	MDE	9/12/63
DRAWING CHECK		
DESIGN APPROVAL	F. Contrato	9/19/63
		8-17-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY- SC2, SIMULATOR

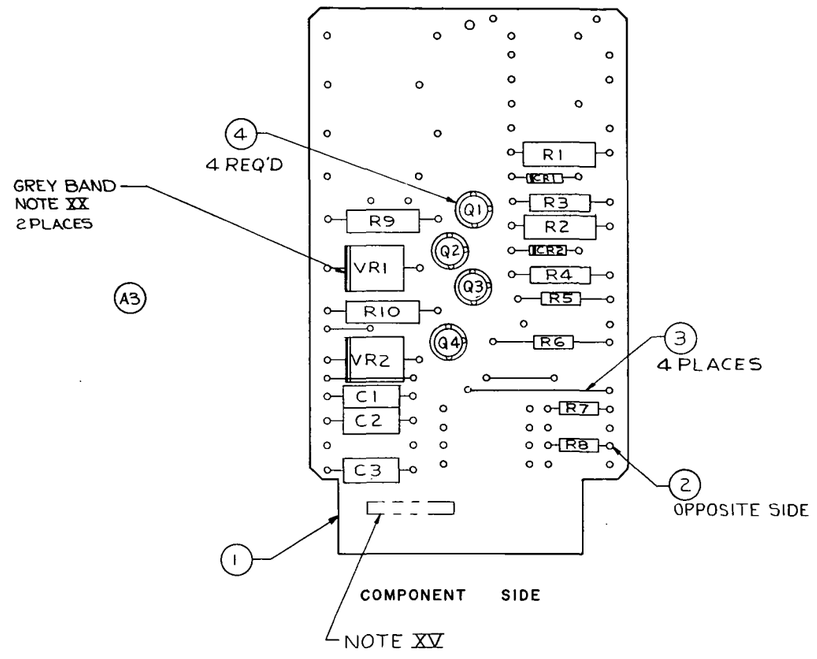
CODE IDENT NO.	SIZE	
03640	D	6901346

SCALE NONE WT SHEET 2

Figure 10-48. SC2 Simulator Printed Circuit Board Assembly (6901346) (Sheet 2)

6901348 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BJ	RELEASE	8.10.63		
A	66112DB	(1-3) ADD NOTE XX	8.13.63	J.J.	EVANS



CIRCUIT	INPUT PIN	OUTPUT PIN
A	C	G
B	E	F

Q1-Q4	13
R1, R2	12
R3, R4	11
R9, R10	10
R5, R6	9
R7, R8	8
VR1, VR2	7
CR1, CR2	6
C1-C3	5
REF DES	ITEM NO.

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901348 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX PIN A MUST BE JUMPERED TO PIN J IN RECEPTACLE WIRING
XX GREY BAND ON (7) DENOTES ANODE SIDE OF DIODE

A1

AC

QTY REQD	SYM BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	TRANSISTOR	6079006				13
2	V	RES, 383Ω, 1/2W, ±1%	6079047				12
2	V	RES, 1.10K, 1/4W, ±1%	6079008				11
2	V	RES, 402Ω, 1/2W, ±1%	6079009				10
2	V	RES, 1.65K, 1/8W, ±1%	6079316				9
2	V	RES, 715Ω, 1/8W, ±1%	6079315				8
2	V	DIODE, ZENER	6079005		NOTE XX		7
2	V	DIODE,	6017645		NOTE XVII		6
3		CAP, .01uf, 100VDC, ±10%	491228				5
4		PAD	483070				4
10 IN.	V,R	WIRE #22GA. YELLOW	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901331				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Wood 9-20-63
DESIGN CHECK 9/30/63
DRAWN MODE EN 9-18-63
DRAWING CHECK
DESIGN APPROVAL R Engel 9-27-63
W S Kinkle 10/24/63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

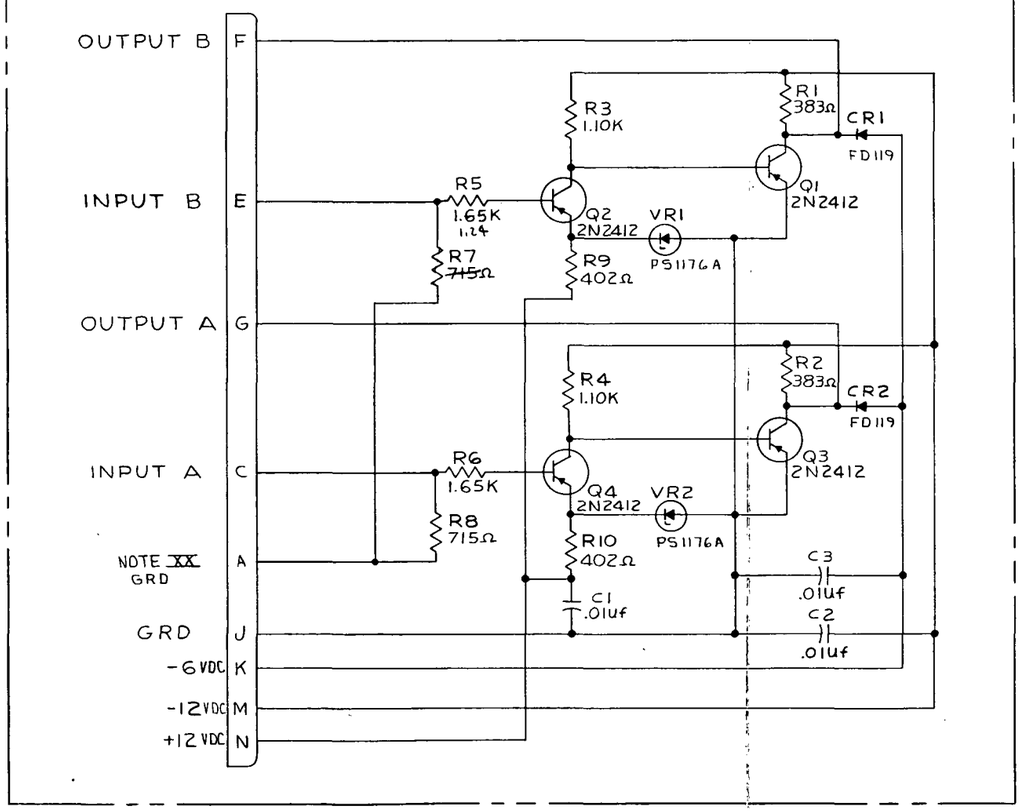
TITLE
PRINTED CIRCUIT BOARD ASSY-MODIFIED AN1

CODE IDENT NO. 03640 SIZE D 6901348
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-49. Modified AN1 Printed Circuit Board Assembly (6901348) (Sheet 1 of 2)

6901348 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BJ	RELEASE	10.10.64		
A	66112DB	(1-3) ADD NOTE XX	12-13-64		EVANS



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS — OUTSIDE MIN MAX — INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES — TOLERANCE ON 2 PLACE DECIMALS — 3 PLACE DECIMALS — ANGLES

MATL
HARD — CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED Y. E. Wood 9-20-63
DESIGN CHECK 9/24/63
DRAWN M D & E EH 9-18-63
DRAWING CHECK
DESIGN APPROVAL 12-31 65
1/3/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

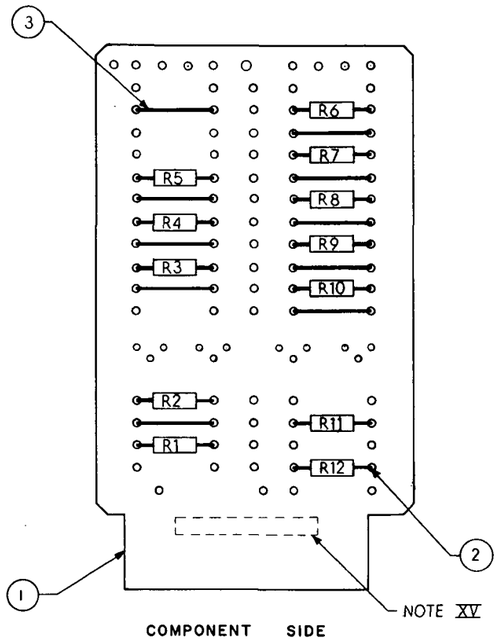
TITLE
PRINTED CIRCUIT BOARD ASSY MODIFIED AN1

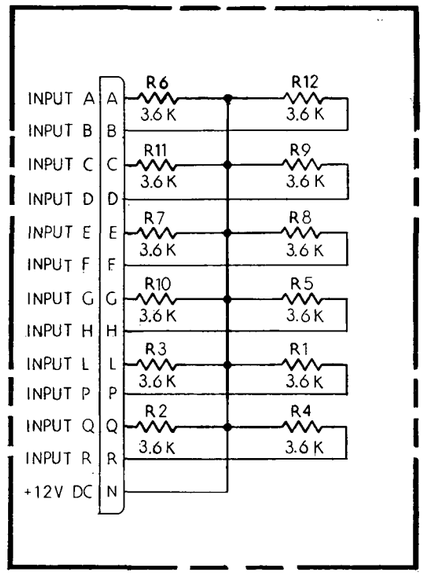
CODE IDENT NO. 03640 | SIZE D | 6901348
SCALE NONE | WT | SHEET 2

Figure 10-49. Modified AN1 Printed Circuit Board Assembly (6901348) (Sheet 2)

6901349

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6011288	RELEASE	12.31.63		





NOTES
- X IBM GEN ASSY SPEC 6000003 APPLIES
- XI MIN ELECTRICAL CLEARANCE TO BE .018
- XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
- XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
- XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
- XV PARTMARK 6901349 ASSY PER IBM SPEC 6009974, COLOR BLACK
- XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
- XVII BLACK BAND DENOTES CATHODE END OF DIODE
- XVIII IDENTIFICATION OF SYMBOLS
  V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
  R-REFERENCE QUANTITY

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
12		RESISTOR 3.6K,1/4W ±5%	334923			88360	4
16 IN	R	WIRE #22 AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	492345			88360	1

LIST OF MATERIAL OR PARTS LIST

R1 TO R12	4
REF. DES	ITEM NO.

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCE ON 3 PLACE DECIMALS ±, 2 PLACE DECIMALS ±, ANGLES ±
MATL
MARD CASE DEPTH
SURF TREAT
CONTRACT NO.

		DATE
DESIGNED	J.S. Wood	10-4-63
DESIGN CHECK	J. Conforto	12-16-63
DRAWN	J. Phillips	9-25-63
DRAWING CHECK		
DESIGN APPROVAL		12-18-63

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

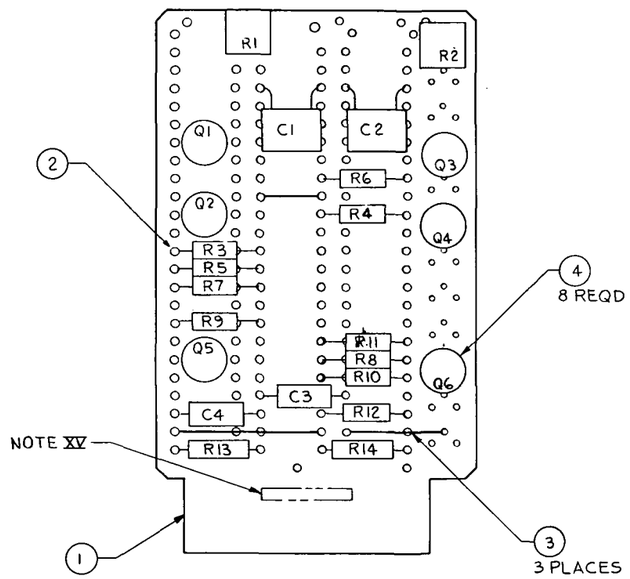
TITLE
PRINTED CIRCUIT BOARD ASS'Y-
3.6K RESISTOR

CODE IDENT NO.	SIZE	
03640	D	6901349
SCALE 2/1	WT	SHEET

Figure 10-50. 3.6K Resistor Printed Circuit Board Assembly (6901349)

6901350

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	(61128V)	RELEASE	10.10.63		



COMPONENT SIDE

CIRCUIT	INPUT 1	INPUT 2	OUTPUT
A	A	C	B
B	E	D	R

Q1 THRU Q4	13
Q5, Q6	12
C1, C2	11
C3, C4	10
R1, R2	9
R3-R4-R7-R8	8
R5, R6	7
R9 THRU R12	6
R13, R14	5
REF DES	ITEM NO.

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901350 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4		TRANSISTOR,	344892			88360	13
2		TRANSISTOR,	318324			88360	12
2	V	CAP, .25UF, +80% -20%, 50VDC	6075166				11
2		CAP, .01UF, ±10%, 100VDC	491228			88360	10
2		POT, 0-2K	6079650				9
4		RES, 4.75K ± 1%, 1/8W	6079213				8
2		RES, 2.21K ± 1%, 1/8W	6079652				7
4		RES, 2K ± 1%, 1/8W	6079651				6
2	V	RES, 1.5K ± 1%, 1/4W	6079653				5
8		SPACER, TRANSISTOR	491299			88360	4
10 IN.	V,R	WIRE NO. 22 AWG YELLOW	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901351				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED E. Ward 11.17.63
DESIGN CHECK J. Evans 11/16/63
DRAWN BY MD & E 11-13-63
DRAWING CHECK F.C.
DESIGN APPROVAL R. Boyle 12-27-63
W. S. Kinder 1/3/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

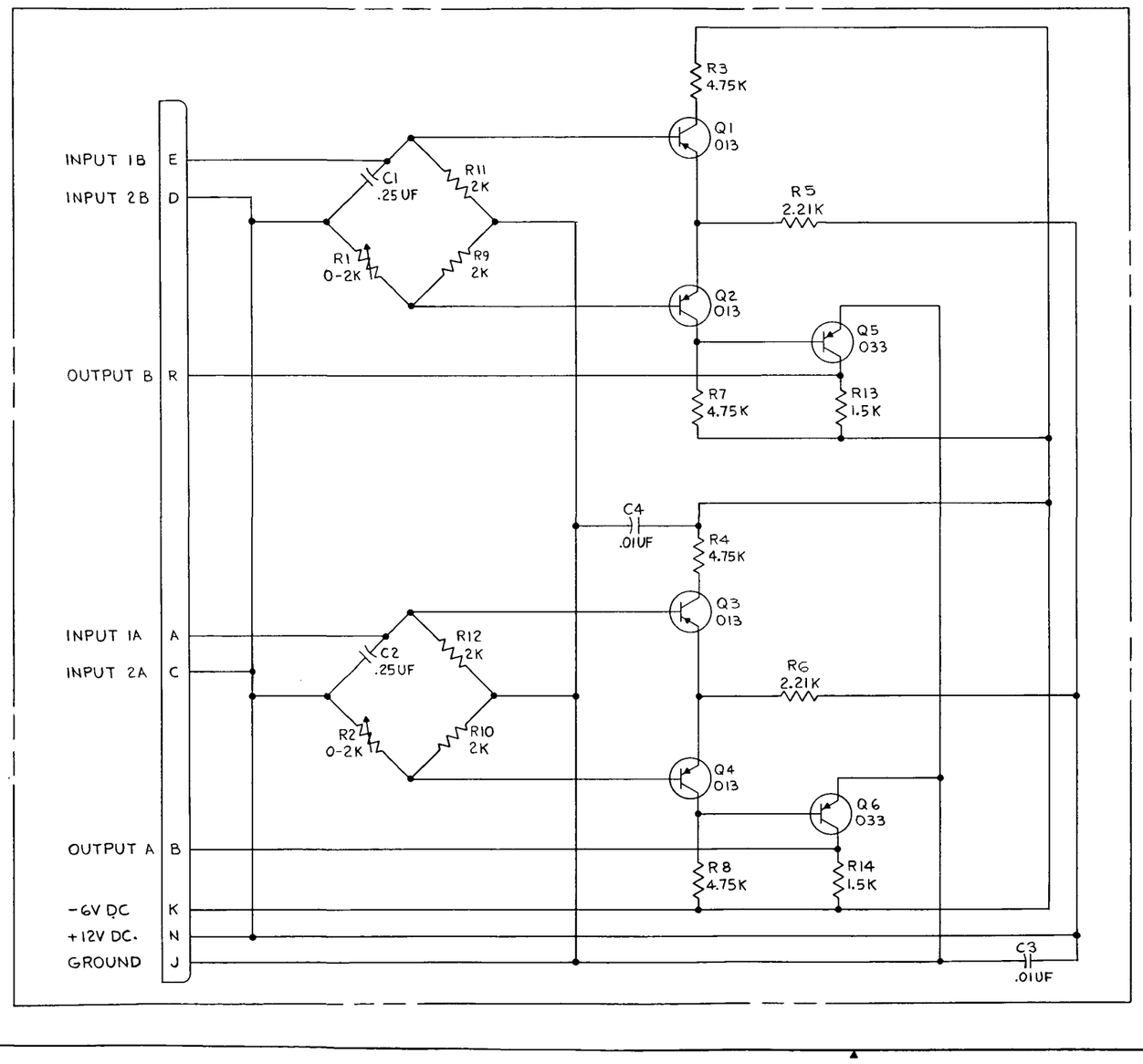
TITLE
PRINTED CIRCUIT BOARD ASSY-TEMPERATURE MONITORING CARD

CODE IDENT NO. 03640 | SIZE D | 6901350
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-51. Temperature Monitoring Printed Circuit Board Assembly (6901350) (Sheet 1 of 2)

6901350

REVISIONS					
BYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112-BJ	RELEASE	10.14		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED E. Wood 12-3-63
DESIGN CHECK J. K. Lowe 11/1/63
DRAWN MD & E 11-12-63
DRAWING CHECK
DESIGN APPROVAL F.C. Boyer 12/31/63
W S Kuhle 1/3/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

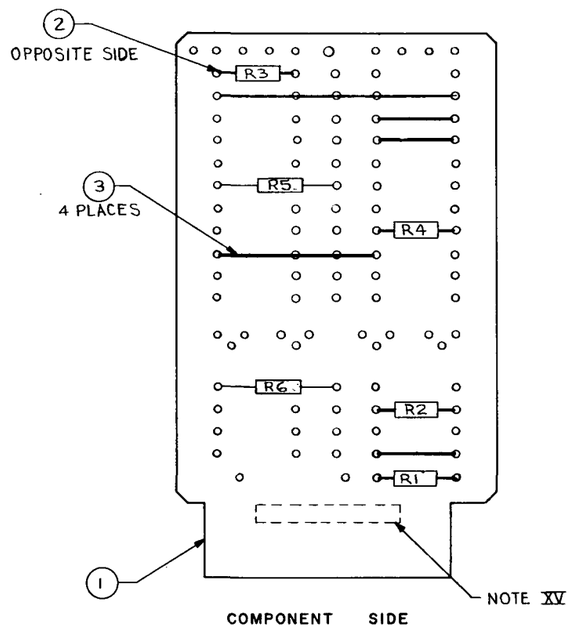
TITLE
PRINTED CIRCUIT BOARD ASSY - TEMPERATURE MONITORING CARD

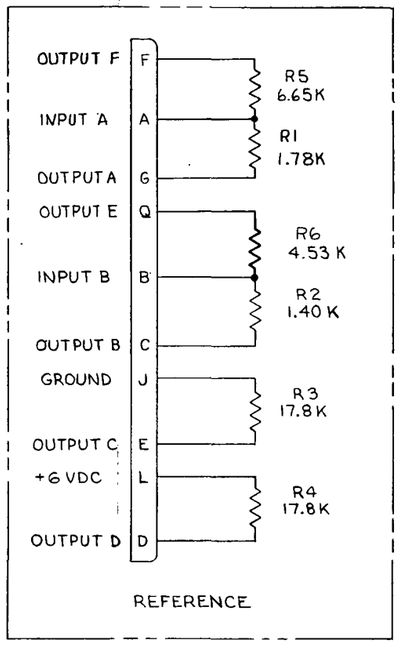
CODE IDENT NO. 03640 | SIZE D | 6901350
SCALE NONE | WT | SHEET 2

Figure 10-51. Temperature Monitoring Printed Circuit Board Assembly (6901350) (Sheet 2)

6901354

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	6611284	RELEASE	8.10.64		





NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901354 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

REF DES	ITEM NO.
R6	8
R5	7
R3 R4	6
R1	5
R2	4

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
1		4.53K±1% 1/8W	6079981				8
1		6.65K±1% 1/8W	6079979				7
2		17.8K±1% 1/8W	6079671				6
1		1.78K±1% 1/8W	6079980				5
1	V	RESISTOR 1.4K±1% 1/8W	6079011				4
16 IN.	V,R	WIRE #22 AWG, YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	492345			88360	1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Wood 11-12-63
DESIGN CHECK JK Evans 11/17/63
DRAWN N. A. Chilson 11/17/63
DRAWING CHECK
DESIGN APPROVAL J.C. Rogge 11/3/64
W S Kuntz 11/3/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

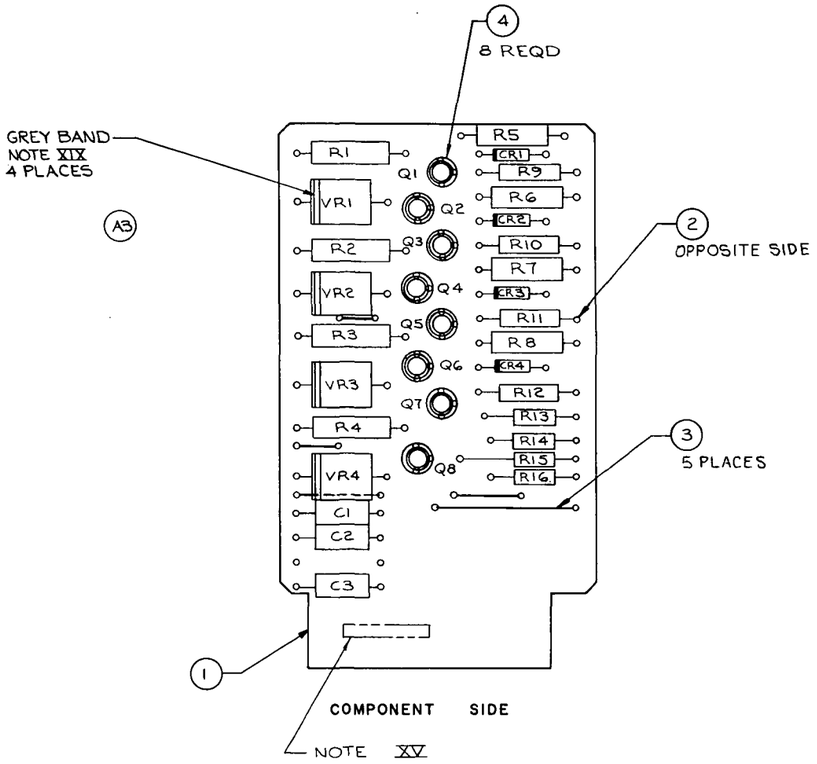
TITLE
PRINTED CIRCUIT BOARD ASSY-
RESISTOR CARD, SCR

CODE IDENT NO. 03640 SIZE D 6901354
SCALE 2/1 WT SHEET

Figure 10-52. SCR Resistor Printed Circuit Board Assembly (6901354)

6901355 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BJ	RELEASE	11.10.66		
A	66112DB	(1-3) ADD NOTE XIX	12.8.66	[illegible]	EVANS



CIRCUIT	INPUT PIN	OUTPUT PIN
A	B	R
B	C	G
C	D	Q
D	E	F

Q1 THRU Q8	8
R13 THRU R16	12
R9 THRU R12	11
R5 THRU R8	10
R1 THRU R4	9
CR1 THRU CR4	7
VR1 THRU VR4	6
C1 THRU C3	5
REF DES	ITEM NO.

A1

NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901355 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY
XIX GREY BAND ON (6) DENOTES ANODE SIDE OF DIODE

A2

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	RES, 825Ω, 1/8W, ± 1%	6079920				12
4	V	RES, 1.1K, 1/4W, ± 1%	6079008				11
4	V	RES, 383Ω, 1/2W, ± 1%	6079047				10
4	V	RES, 402Ω, 1/2W, ± 1%	6079009				9
8	V	TRANSISTOR	6079006				8
4	V	DIODE	6017645		NOTE XVII		7
4	V	DIODE, ZENER	6079005		NOTE XIX		6
3		CAP., .01uf, 100VDC, ±10%	491228			88360	5
8		PAD	483070			88360	4
10 IN	V,R	WIRE #22 GA, YELLOW	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901331				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD SURF TREAT CASE DEPTH
CONTRACT NO.

DESIGNED J E Wood 12-31-62
DESIGN CHECK F Contato 1/4/63
DRAWN MD & E EE 12-17-63
DRAWING CHECK
DESIGN APPROVAL 12-31-63
W E Kuhle 1/3/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

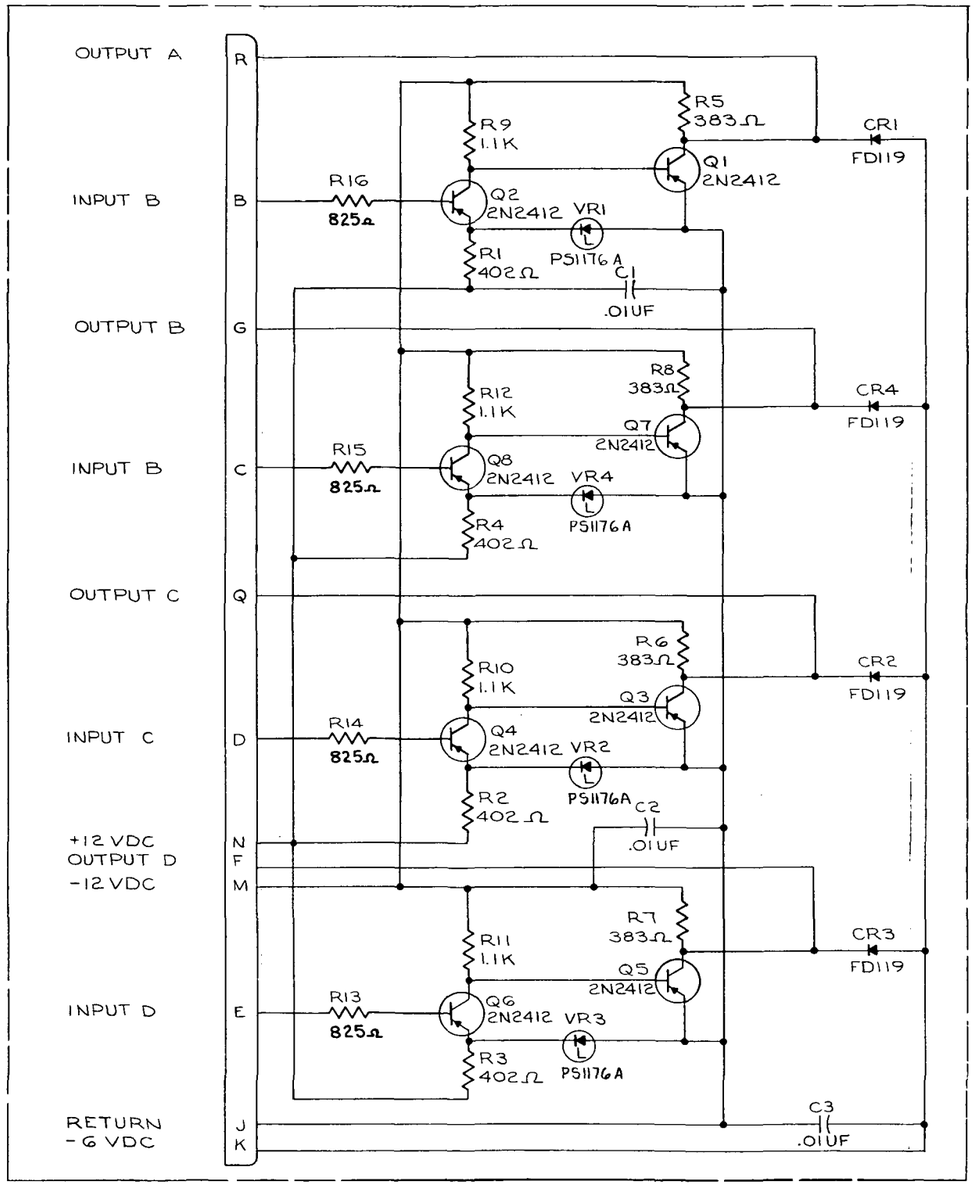
TITLE
PRINTED CIRCUIT BOARD ASSY-TRANSLATOR, AN4

CODE IDENT NO. 03640 SIZE D 6901355
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-53. AN4 Translator Printed Circuit Board Assembly (6901355) (Sheet 1 of 2)

6901355 A

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BJ	RELEASE	11.10.6		
A	66112DB	(1-3) ADD NOTE XIX	12/13/63		EVANS



QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD SURF TREAT CASE DEPTH
CONTRACT NO.

DESIGNED	J.E. Wood	DATE 12-31-63
DESIGN CHECK	J Contento	1/1/64
DRAWN	MD E2 E	12-18-63
DRAWING CHECK		
DESIGN APPROVAL	R Joyce	12-31-63
	W S Kinzle	1/3/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE: PRINTED CIRCUIT BOARD ASSY-TRANSLATOR, AN4

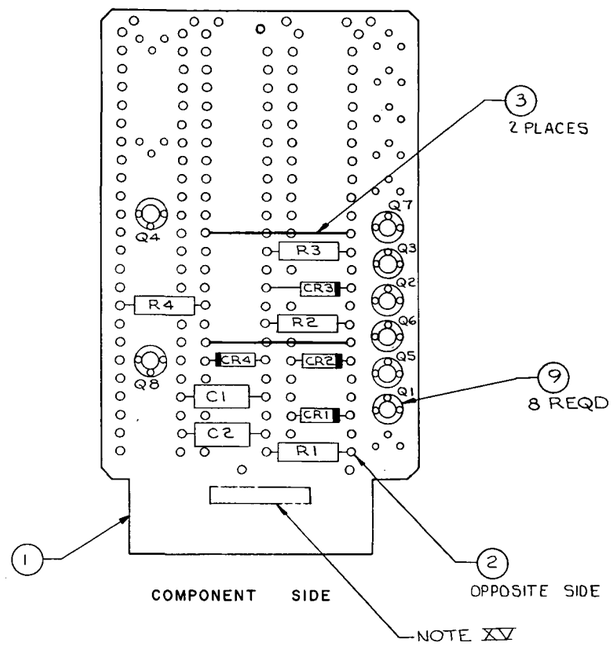
CODE IDENT NO. 03640 | SIZE D | 6901355

SCALE NONE | WT | SHEET 2

Figure 10-53. AN4 Translator Printed Circuit Board Assembly (6901355) (Sheet 2)

6901356

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	661128N	RELEASE	8/20/64		



NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901356 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

CIRCUIT	INPUT PIN	OUTPUT PIN
A	G	B
B	E	A
C	D	C
D	R	Q

R1-R4	8
Q5-Q8	7
Q1-Q4	6
CR1-CR4	5
C1 & C2	4
REF DES	ITEM NO.

QTY REQD	SYM-BOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
8		PAD	483070			88360	9
4	V	RESISTOR 26.1Ω ±1% 1/4W	6079906				8
4	V	TRANSISTOR	6079006				7
4	V	TRANSISTOR	6079221				6
4	V	DIODE	6017645				5
2		CAP,.01UF ±10% 100VDC	491228			88360	4
6 IN.	V,R	WIRE NO.22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901357				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Wood 12-64
DESIGN CHECK W A Morton 12-64
DRAWN MD E 12-18-63
DRAWING CHECK
DESIGN APPROVAL R Joyce 1-7-65
E McLure 1-8-65

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

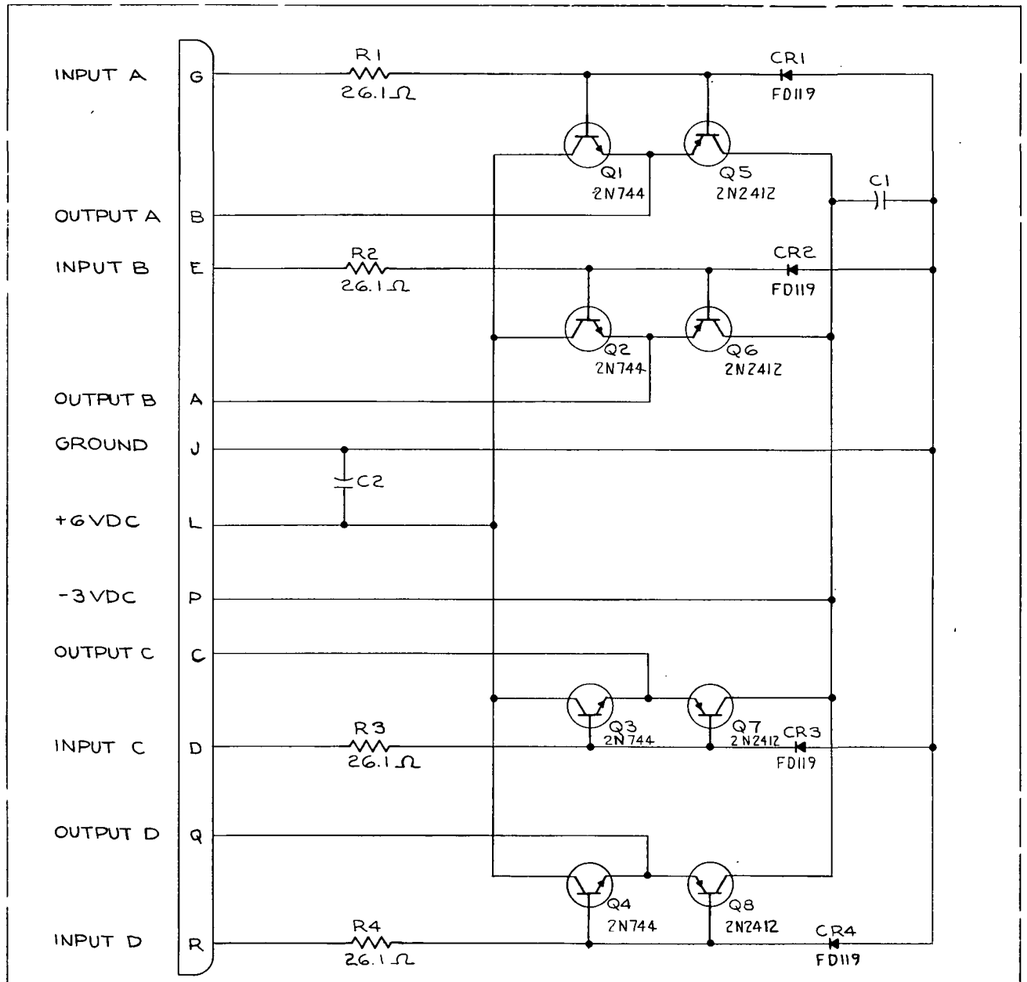
TITLE
PRINTED CIRCUIT BOARD ASSY-CD1

CODE IDENT NO. 03640 SIZE D 6901356
SCALE 2/1 WT SHEET 1 OF 2

Figure 10-54. CD1 Printed Circuit Board Assembly (6901356) (Sheet 1 of 2)

6901356

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BM	RELEASE	12-20-64		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

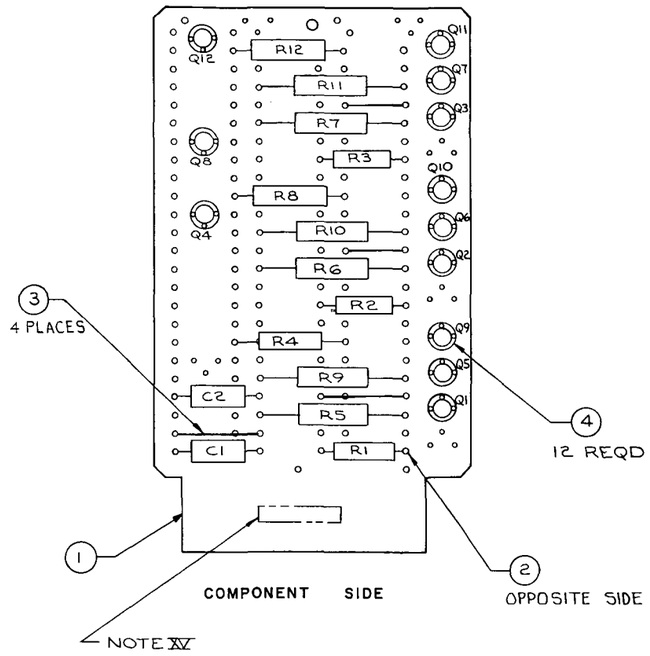
UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX	DESIGNED J. E. Wood	DATE 1-2-64	INTERNATIONAL BUSINESS MACHINES CORP. FEDERAL SYSTEMS DIVISION
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART	DESIGN CHECK W. A. Matson	1-2-64	590 MADISON AVE. NEW YORK 22, N. Y.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES	DRAWN MD&E EZ 12 18 63		TITLE PRINTED CIRCUIT BOARD ASSY-CD
MATL	DRAWING CHECK		
HARD CASE DEPTH	DESIGN APPROVAL R. D. Joyce	1-7 65	CODE IDENT NO. 03640 SIZE D 6901356
SURF TREAT	E. McLeod	1-8 65	SCALE NONE WT SHEET 2

CONTRACT NO.

Figure 10-54. CD1 Printed Circuit Board Assembly (6901356) (Sheet 2)

6901358

SYM	ENGRG NOTICE	DESCRIPTION	DATE
	66112 E V	RELEASE	



NOTES

X IBM GEN ASSY SPEC 6000003 APPLIES
XI MIN ELECTRICAL CLEARANCE TO BE .018
XII COMPONENTS TO BE ASSEMBLED FLAT AGAINST THE BOARD AND/OR OTHER COMPONENTS
XIII COMPONENTS TO BE CENTERED BETWEEN HOLES WITHIN .06 INCHES
XIV LEADS TO BE MAINTAINED AXIAL WITH RESPECT TO COMPONENT BODY WHERE POSSIBLE
XV PARTMARK 6901358 ASSY PER IBM SPEC 6009974, COLOR BLACK
XVI JUMPER AND COMPONENT LEADS TO BE BENT FLAT AGAINST BOARD BEFORE DIP SOLDERING
XVII BLACK BAND DENOTES CATHODE END OF DIODE
XVIII IDENTIFICATION OF SYMBOLS
V-VENDOR ITEM-SEE SPEC OR SOURCE CONTROL DWG
R-REFERENCE QUANTITY

CIRCUIT	INPUT PIN	OUTPUT PIN
A	G	A
B	F	B
C	D	C
D	E	R

R9-R12	10
R5-R8	9
R1-R4	8
Q1-Q4, Q9-Q12	7
Q5-Q8	6
C1 & C2	5
REF DES	ITEM NO.

QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.
4	V	61.9Ω ±1% 1/2W	6079907				10
4	V	1.0K ±1% 1/4W	6079905				9
4	V	RESISTOR 1.0K ±1% 1/8W	6079220				8
8	V	TSTR	6079909				7
4	V	TSTR	6079006				6
2		CAP, .01UF ±10% 100VDC	491228			88360	5
12		PAD	483070			88360	4
10IN	V,R	WIRE NO.22 AWG YEL	6036152				3
AR		SOLDER (6032357)	Sn 60 AR	QQ-S-571			2
1		SMS CARD	6901359				1

LIST OF MATERIAL OR PARTS LIST

UNLESS NOTED BREAK CORNERS OUTSIDE MIN MAX INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT
CONTRACT NO.

DESIGNED J. E. Ward 1-2-64
DESIGN CHECK 1/2/64
DRAWN MD & E 12-18-63
DRAWING CHECK
DESIGN APPROVAL R. D. Spigel 1-3-64
E. M. Lees 1/8/64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
580 MADISON AVE. NEW YORK 22, N.Y.

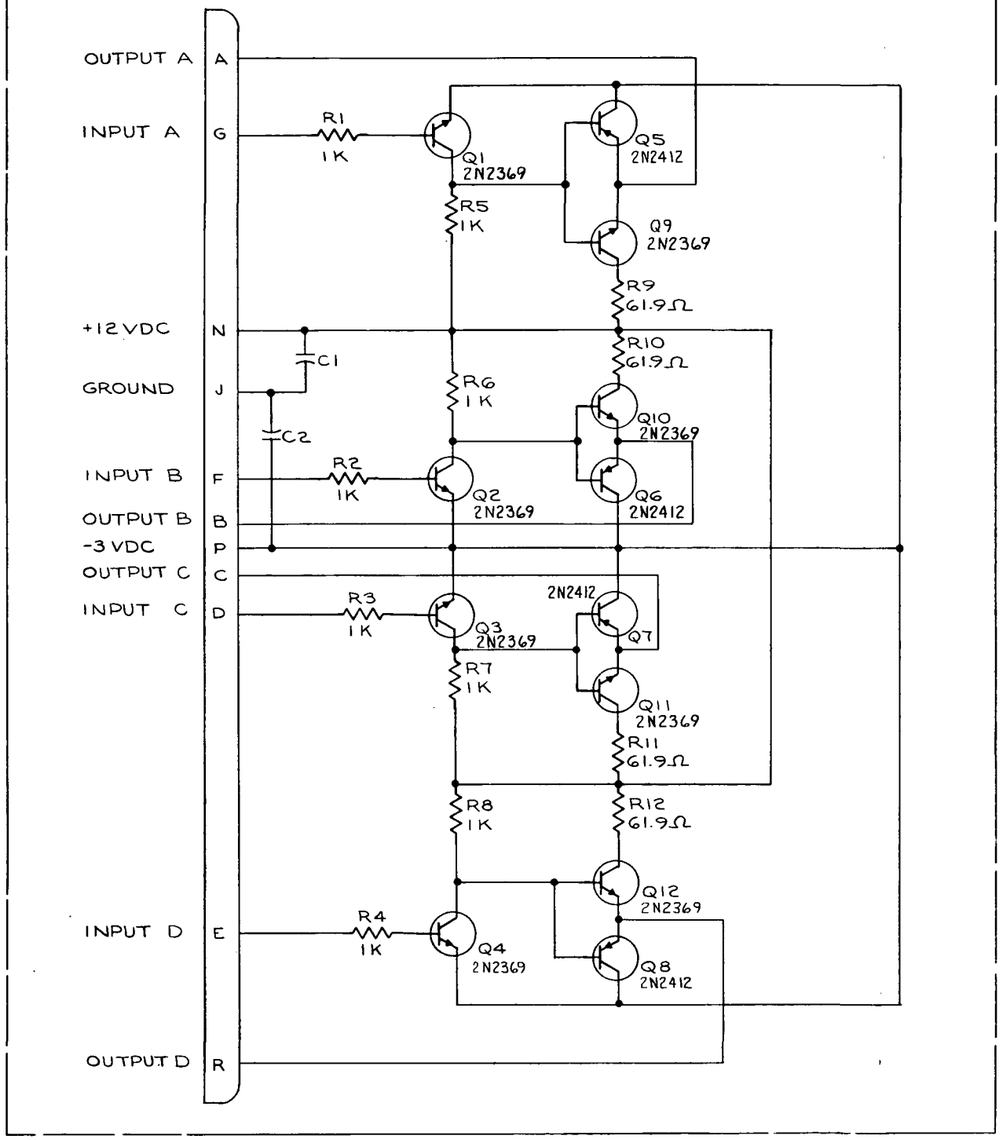
TITLE
PRINTED CIRCUIT BOARD ASSY- SC3

CODE IDENT NO. 03640 | SIZE D | 6901358
SCALE 2/1 | WT | SHEET 1 OF 2

Figure 10-55. SC3 Printed Circuit Board Assembly (6901358) (Sheet 1 of 2)

6901358

REVISIONS					
SYM	ENGRG NOTICE	DESCRIPTION	DATE	CHK	APPROVAL
	66112BN	RELEASE	12-10-63		



QTY REQD	SYMBOL	NOMENCLATURE OR DESCRIPTION	PART OR IDENTIFYING NO.	SPECIFICATION	MATERIAL OR NOTES	CODE IDENT NO.	ITEM NO.

LIST OF MATERIAL OR PARTS LIST

CONTRACT NO.

UNLESS NOTED BREAK CORNERS
OUTSIDE MIN MAX
INSIDE MIN MAX
ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCE ON 2 PLACE DECIMALS 3 PLACE DECIMALS ANGLES
MATL
HARD CASE DEPTH
SURF TREAT

DESIGNED	J. E. Wood	DATE 12-30-63
DESIGN CHECK		1/4/64
DRAWN	MD E&E	12-18-63
DRAWING CHECK		
DESIGN APPROVAL		1-7-64
		1-8-64

INTERNATIONAL BUSINESS MACHINES CORP.
FEDERAL SYSTEMS DIVISION
590 MADISON AVE. NEW YORK 22, N.Y.

TITLE
PRINTED CIRCUIT BOARD ASSY- SC3

CODE IDENT NO.	SIZE	
03640	D	6901358

SCALE NONE WT SHEET 2

Figure 10-55. SC3 Printed Circuit Board Assembly (6901358) (Sheet 2)

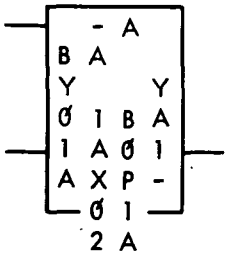
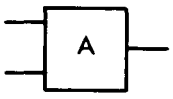
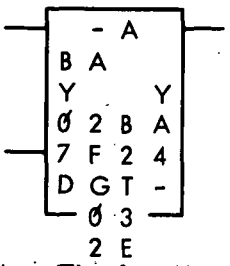
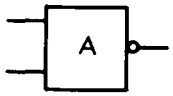
LOGIC SYMBOLS

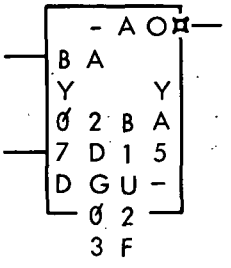
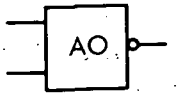
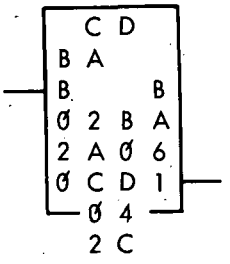
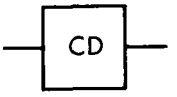
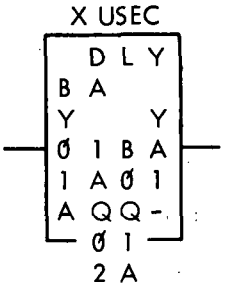
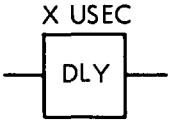
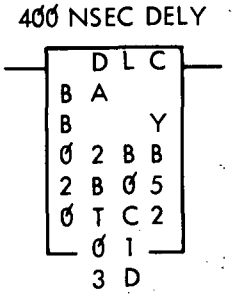
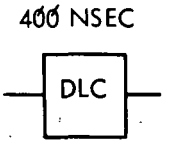
In the list that follows, each type of logic symbol on the LVDCME ALD's is described. Each typical ALD symbol is shown with the corresponding symbol (if any) used in the simplified logic diagrams on figure 10-30; some of the circuits indicated on the ALD's (such as resistive loads and diode clamps) were not indicated on figure 10-30 because they performed no logic function.

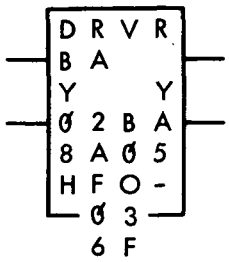
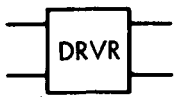
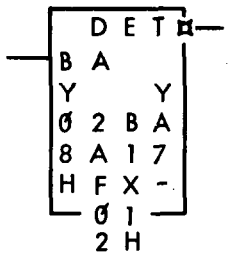
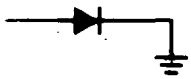
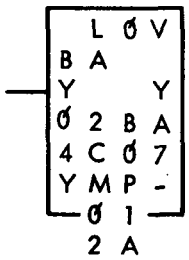
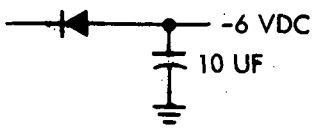
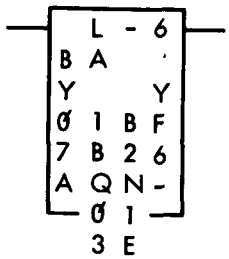
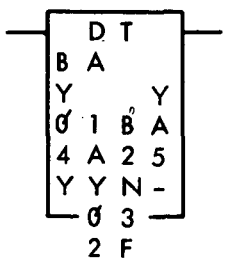
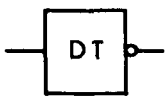
The two letters on the third line of each ALD symbol indicate the nominal levels of input and output voltage for that circuit. The levels represented by these letters are shown in the following table.

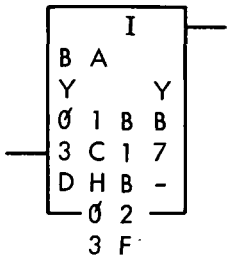
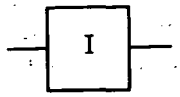
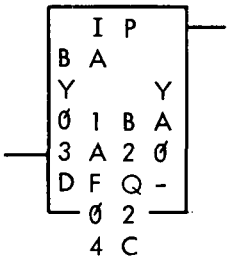
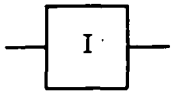
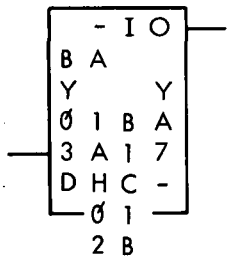
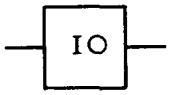
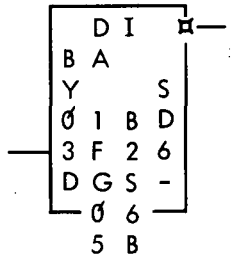
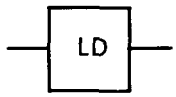
Symbol	Voltage Levels (Nominal)	
	"0" Level	"1" Level
Y	0 VDC	-6 VDC
S	0 VDC	-12 VDC
V	Special	Special
B	Special	Special

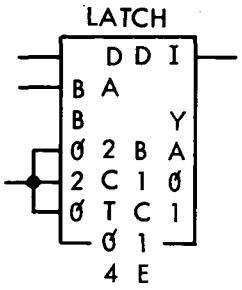
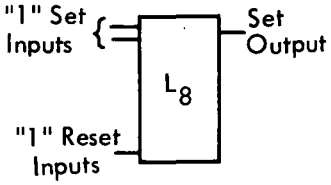
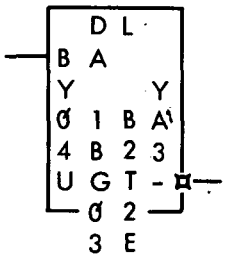
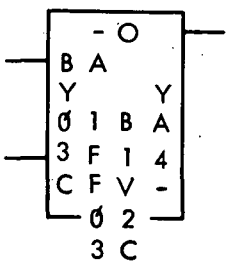
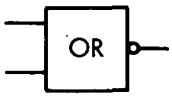
The "Special" levels indicated by B and V are explained in the description of the logic circuits to which they apply; the B notation usually indicates positive logic levels.

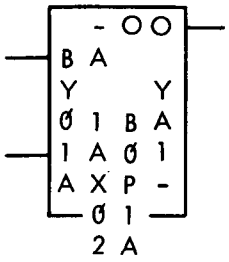
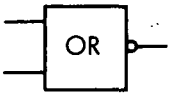
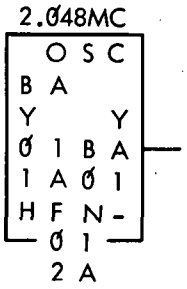
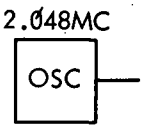
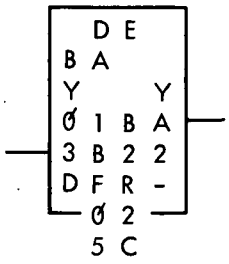
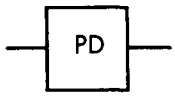
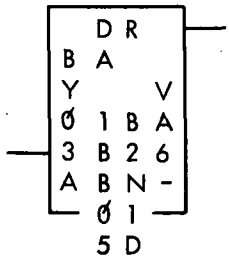
Circuit/Definition	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
1. AND. The output of an AND circuit is the logical AND of its inputs. When all inputs are "1's", the output is a "1"; if any input is a "0", the output is a "0". The AND circuit may have two or more inputs.		
2. AND-INVERTER. This circuit performs the logical AND and INVERT functions. When all inputs are "1's", the output is a "0"; if any input is a "0", the output is a "1". The AND-INVERTER circuit may have two or more inputs.		
	Note: The functional symbol "+O" may be substituted for "-A".	

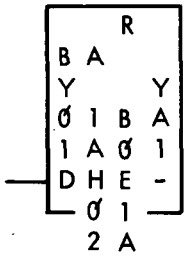
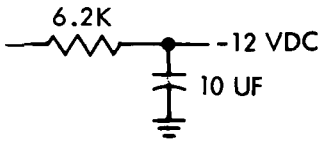
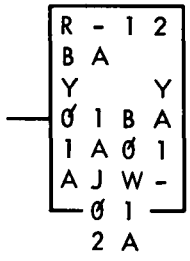
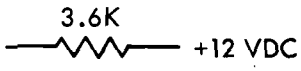
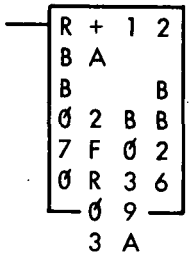
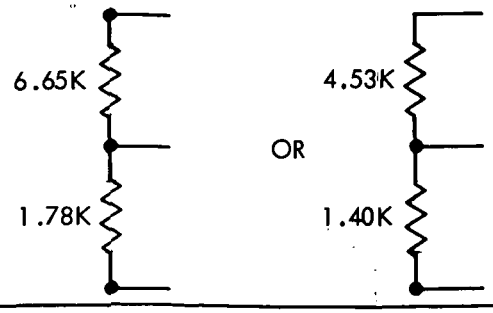
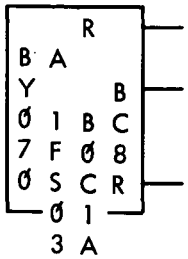
Circuit/Definition	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
3. AND-OR-INVERTER. This circuit performs the logical AND, OR, and INVERT functions. The relation between the inputs and outputs is the same as the AND-INVERTER circuit. However the output transistor of this circuit allows the outputs of several AND-OR-INVERTER circuits to be connected (OR'd) together. A "0" output from any AND-OR-INVERTER circuit of an "OR'd" group of circuits will force a "0" output from the group. The AND-OR-INVERTER circuit may have two or more inputs.	 Note The functional symbol "O O" may be substituted for "-AO".	
4. CLOCK DRIVER. This circuit is used as a level shifter to drive a TRANSLATOR-INVERTER circuit. A low positive voltage input produces a "1" output (+6 VDC); a low negative voltage input produces a "0" output (0 VDC).		
5. DELAY. This circuit delays only the positive transition of its input; a delay occurs only when the input changes from a "1" (-6 VDC) to a "0" (0 VDC). The nominal delay duration is indicated above the symbol. A "1" input causes a "1" output.		
6. DELAY CLOCK MONITOR. This circuit monitors delay line clock pulses; its normal output is a "0". If its input level is not changed from a "1" to a "0" or from a "0" to a "1" during a time of 400 NSEC, its output is forced to a "1" at the end of the 400 NSEC period. Note The sampling period of this circuit is adjustable.		

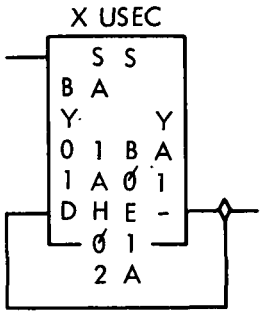
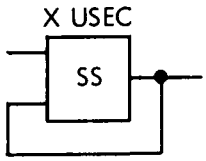
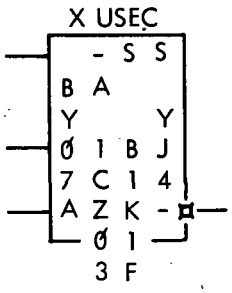
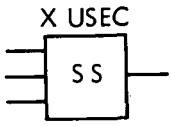
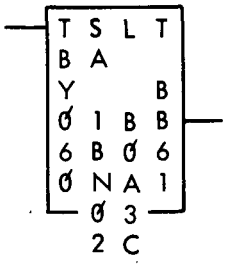
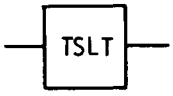
Circuit/Definition	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
7. DELAY LINE DRIVER. This circuit always feeds a DELAY line. A "1" at either input causes a pulse to be emitted at both outputs. The output pulses are tapped from a resistive divider network.		
8. DETECTOR. This circuit senses the outputs from a delay line. A "1" input to the delay line causes the DETECTOR's normally "1" output to become a "0".		
9. DIODE. This circuit is a diode clamped to ground. 		None
10. DIODE. This circuit is a diode clamped to -6 VDC. 		None
11. DRIVER TERMINATOR. This circuit is a signal shaper, inverter, and low impedance matching device.		

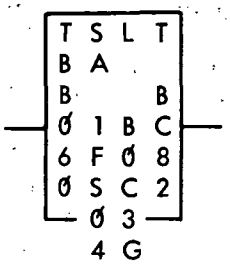
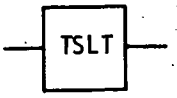
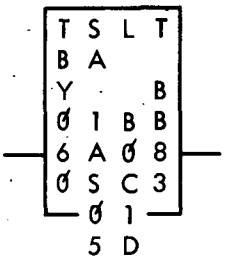
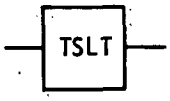
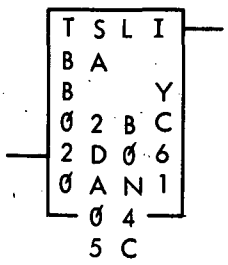
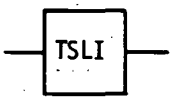
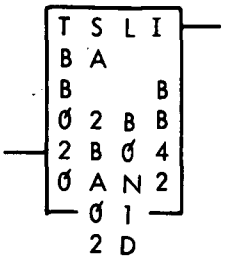
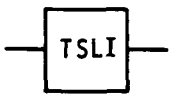
Circuit/Definition	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
12. INVERTER. The output of this circuit is the inverse of its input; a "1" input results in a "0" output and vice versa.		
13. INVERTER (POWER). This circuit performs signal inversion and amplification; a "1" input results in a "0" output and vice versa.		
14. INVERTER-OR. This circuit performs signal inversion; a "1" input results in a "0" output and vice versa. The output transistor of this circuit allows several INVERTER-OR circuits to be connected ("OR'd") together. A "0" output from any INVERTER-OR circuit of an "OR'd" group of circuits will force a "0" output from the group.		
15. LAMP DRIVER. A "1" input causes the LAMP DRIVER to turn on its associated indicator lamp; a "0" input causes the LAMP DRIVER to turn off its associated indicator lamp. The input-output levels are as follows: Input — Output "1" (-6 VDC) — 0 VDC "0" (0 VDC) — -12 VDC Note One side of the indicator lamp is connected to -12 VDC; the other side is connected to the output of the LAMP DRIVER. When the output of the LAMP DRIVER is 0 VDC, the potential	 Note The "DI" functional symbol represents "Driver, Indicator". Some of these blocks do not show the difference between	

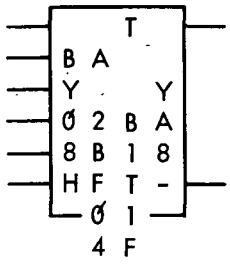
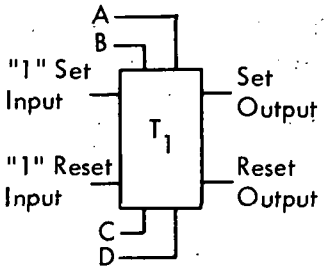
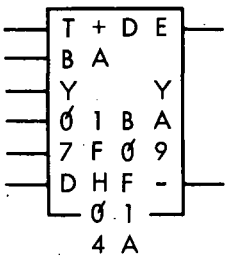
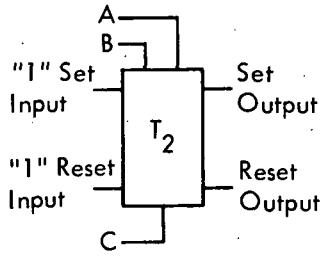
Circuit/Definition	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
Note (cont) difference of 12 volts across the lamp lights the lamp.	Note (cont) the input and output voltage levels; the Y Y notation on these blocks is incorrect.	
16. LATCH 8. This circuit is a bistable device that becomes set when the "1" Set Inputs become "1's"; it is reset when the "1" Reset Input becomes a "1". This circuit also acts as a translator; the nominal input-output levels are as follows: Input — Output "1" (+6 VDC) — "1" (-6 VDC) "0" (0 VDC) — "0" (0 VDC)		
17. LINE DRIVER. This circuit functions as a signal driver and low impedance matching device.	 Note The "DL" functional symbol represents "Driver, Line".	
18. OR-INVERTER. This circuit performs the logical OR and INVERT functions. When all inputs are "0's", the output is a "1"; if any input is a "1", the output is a "0". This circuit may have two or more inputs.		
	Note: The functional symbol "+A" may be substituted for "-O".	

Circuit/Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
19. OR-INVERTER-OR. This circuit functions in the same manner as the OR-INVERTER. The outputs of many OR-INVERTER-OR's may be connected (OR'd) together. A "0" output from any OR-INVERTER-OR circuit of an "OR'd" group of circuits will force a "0" output from the group. This circuit may have two or more inputs.		
20. OSCILLATOR. This circuit generates a square wave signal (0 VDC to -6 VDC) at a 2.048 MC frequency.		
21. POWER DRIVER. This circuit provides circuit matching and power amplification. A "1" input causes a "1" output; a "0" input causes a "0" output.	 Note The "DE" functional symbol represents "Driver, Emitter". The output portion of this circuit is an emitter follower.	
22. RELAY DRIVER. This circuit functions as a level shifter to enable a "1" to energize a relay coil. The input-output relationship is as follows: Input — Output "1" (-6 VDC) — 0 VDC "0" (0 VDC) — -26.5 VDC	 Note: The "DR" functional symbol represents "Driver, Relay".	

Circuit/Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
Note One side of the relay coil is connected to -26.5 VDC; the other side is connected to the output of the RELAY DRIVER. When the output of the RELAY DRIVER is 0 VDC, the potential difference of 26.5 volts across the relay coil energizes the relay coil.		
23. RESISTOR. This circuit is a 1K resistor connected to -12 VDC. 		None
24. RESISTOR. This circuit is a 6.2K resistor connected to -12 VDC. 		None
25. RESISTOR. This circuit is a 3.6K resistor connected to +12 VDC. 		None
26. RESISTOR. This circuit is a resistive divider network. 		None

Circuit/Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
27. SINGLE SHOT. (Dual Input). A negative-going transition at the input causes the SINGLE SHOT to produce a negative output pulse whose negative transition is coincident with the negative transition at the input. The output is fed back to hold the SINGLE SHOT on for the duration of the pulse. The nominal duration of the pulse is shown above the symbol.		
28. SINGLE SHOT (Tri-Input). Any or all three inputs may be connected; an unconnected input (indicated by the absence of that input) is effectively a "1" input. All inputs must be "1's" to trigger the SINGLE SHOT. The negative-going transition of the last input to become a "1" triggers the single shot, forcing it to produce a negative output pulse whose negative transition is coincident with the triggering transition of its input. The nominal duration of the pulse is shown above the symbol.		
29. TRANSLATOR. This circuit is a level shifter that converts the negative logic levels used in the LVDCME logic to the positive levels used in the computer and LVDCME self-check circuitry. A "1" input causes a "1" output, and a "0" input causes a "0" output. The nominal input-output levels are as follows: Input — Output "1" (-6 VDC) — "1" (+6 VDC) "0" (0 VDC) — "0" (0 VDC)	 Note This description also applies to the ϕNA2 TSLT circuit.	

Circuit/Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
30. TRANSLATOR. This level shifter is used only in the LVDCME self-check circuitry. The nominal input-output levels are as follows: Input: "1" (+5 VDC), "0" (0 VDC) Output: "1" (+1 VDC), "0" (-1 VDC) A "1" input causes a "1" output, and a "0" input causes a "0" output.		
31. TRANSLATOR. See Item 30. The nominal input-output levels are as follows: Input: "1" (-6 VDC), "0" (0 VDC) Output: "1" (+8 VDC), "0" (-2 VDC)		
32. TRANSLATOR-INVERTER. This circuit performs level shifting and inversion. This circuit converts the positive logic levels used in the computer and LVDCME self-check circuitry to the negative logic levels used in the LVDCME logic. A "1" input causes a "0" output, and a "0" input causes a "1" output. The nominal input-output levels are as follows: Input: "1" (+6 VDC), "0" (0 VDC) Output: "0" (0 VDC), "1" (-6 VDC)	 Note This description also applies to the ϕAN4 and ϕANM TSLI circuits.	
33. TRANSLATOR-INVERTER. This circuit always feeds a DELAY CLOCK MONITOR circuit. The nominal input-output levels are as follows: Input: "1" (+10 VDC), "0" (0 VDC) Output: "0" (0 VDC), "1" (+6 VDC)		

Circuit/Description	ALD Symbol (typical)	Second Level Logic Symbol (used on figure 10-30)
34. TRIGGER 1. This circuit is a bistable device that becomes set (1) if the "1" Set Input becomes a "1" or, (2) if input A is a "0" and input B changes from a "1" to a "0". Similarly, the circuit becomes reset (1) if the "1" Reset Input becomes a "1" or, (2) if input D is a "0" and input C changes from a "1" to a "0".		
35. TRIGGER 2. This circuit is very similar to the TRIGGER 1. The basic difference is that the circuit becomes reset when input C is a "0" and input B changes from a "1" to a "0". This circuit also provides power amplification.	 Note The functional symbol "T + DE" represents "Trigger and Driver, Emitter".	

GLOSSARY

SYMBOL	DEFINITION
115VACR	115 VOLTS AC TO TAPE READER
115VACR(LT)	115 VOLTS AC RETURN FOR TAPE READER MOTOR.
115VACS	115 VOLTS AC TO SPOOLER.
12 + 14	OPERATION CODES 1 AND 2 OR 1 AND 4.
12 + 24	OPERATION CODES 1 AND 2 OR 2 AND 4.
2BDDTSO NOT	INVERSE 2 BIT DELAY DATA SERIAL OUT.
2BDDTSO	2 BIT DELAY DATA SERIAL OUT.
2 TO EIGHT IND	WORD COUNTER BIT POSITION 2 TO EIGHT, INDICATOR DRIVER OUTPUT.
2 TO EIGHT NOT	INVERSE WORD COUNTER 2 TO EIGHT BIT POSITION.
2 TO ELEVEN IND	WORD COUNTER BIT POSITION 2 TO ELEVEN, INDICATOR DRIVER OUTPUT.
2 TO ELEVEN NOT	INVERSE WORD COUNTER 2 TO ELEVEN BIT POSITION.
2 TO FIVE IND	WORD COUNTER BIT POSITION 2 TO FIVE, INDICATOR DRIVER OUTPUT.
2 TO FOUR IND	WORD COUNTER BIT POSITION 2 TO FOUR, INDICATOR DRIVER OUTPUT.
2 TO NINE IND	WORD COUNTER BIT POSITION 2 TO NINE, INDICATOR DRIVER OUTPUT.
2 TO ONE IND	WORD COUNTER BIT POSITION 2 TO ONE, INDICATOR DRIVER OUTPUT.
2 TO SEVEN IND	WORD COUNTER BIT POSITION 2 TO SEVEN, INDICATOR DRIVER OUTPUT.

SYMBOL	DEFINITION
2 TO SIX IND	WORD COUNTER BIT POSITION 2 TO SIX, INDICATOR DRIVER OUTPUT.
2 TO TEN IND	WORD COUNTER BIT POSITION 2 TO TEN, INDICATOR DRIVER OUTPUT.
2 TO THREE IND	WORD COUNTER BIT POSITION 2 TO THREE, INDICATOR DRIVER OUTPUT.
2 TO TWO IND	WORD COUNTER BIT POSITION 2 TO TWO, INDICATOR DRIVER OUTPUT.
2 TO ZERO IND	WORD COUNTER BIT POSITION 2 TO ZERO, INDICATOR DRIVER OUTPUT.
355AM	LEVEL WHICH PREVENTS HALT UNTIL MULTIPLY, MULTIPLY - HOLD OR DIVIDE OPERATIONS ARE COMPLETE.
3MSSS	3 MILLISECOND SINGLE SHOT.
3 OSC NOT	INVERSE 2.048 MEGACYCLE OSCILLATOR.
3 OSC	2.048 MEGACYCLE OSCILLATOR.
3 OSCS NOT	INVERSE 2.048 MEGACYCLE OSCILLATOR, SHIFTED.
3 OSCS	2.048 MEGACYCLE OSCILLATOR, SHIFTED.
500 CPS MV	500 CYCLE PER SECOND MULTIVIBRATOR. SIMULATES TAPE READER TIMING TRACK IN SELF-CHECK MODE.
50 CPS MV	50 CYCLES PER SECOND MULTIVIBRATOR.
+12 CH1 MOD1 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1, MODULE 1 VOTER CIRCUIT.
+12 CH1 MOD2 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1, MODULE 2 VOTER CIRCUIT.
+12 CH1 MOD3 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1, MODULE 3 VOTER CIRCUIT.

SYMBOL	DEFINITION
+12 CH1 MOD4 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1, MODULE 4 VOTER CIRCUIT.
+12 CH1 MOD5 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1, MODULE 5 VOTER CIRCUIT.
+12 CH1 MOD6 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1 MODULE 6 VOTER CIRCUIT.
+12 CH1 MOD7 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 1 MODULE 7 VOTER CIRCUIT.
+12 CH2 MOD1 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 1 VOTER CIRCUIT.
+12 CH2 MOD2 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 2 VOTER CIRCUIT.
+12 CH2 MOD3 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 3 VOTER CIRCUIT.
+12 CH2 MOD4 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 4 VOTER CIRCUIT.
+12 CH2 MOD5 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 5 VOTER CIRCUIT.
+12 CH2 MOD6 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 6 VOTER CIRCUIT.
+12 CH2 MOD7 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 2, MODULE 7 VOTER CIRCUIT.
+12 CH3 MOD4 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 4 VOTER CIRCUIT.
+12 CH3 MOD5 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 5 VOTER CIRCUIT.

SYMBOL	DEFINITION
+12 CH3 MOD6 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 6 VOTER CIRCUIT.
+12 CH3 MOD7 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 7 VOTER CIRCUIT.
+12 CH 3 MOD 1 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 1 VOTER CIRCUIT.
+12 CH 3 MOD 2 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 2 VOTER CIRCUIT.
+12 CH 3 MOD 3 DR	RELAY DRIVER OUTPUT - ALLOWS 12 VOLTS TO CHANNEL 3, MODULE 3 VOTER CIRCUIT.
+12V CH1 MOD1 THROUGH +12V CH1 MOD7	PLUS 12 VOLTS SWITCHED TO VOTER CIRCUIT FOR CHANNEL 1, MODULES 1 THROUGH 7 SELECTION.
+12V CH2 MOD1 THROUGH +12V CH2 MOD7	PLUS 12 VOLTS SWITCHED TO VOTER CIRCUIT FOR CHANNEL 2, MODULES 1 THROUGH 7 SELECTION.
+12V CH3 MOD1 THROUGH +12V CH3 MOD7	PLUS 12 VOLTS SWITCHED TO VOTER CIRCUIT FOR CHANNEL 3, MODULES 1 THROUGH 7 SELECTION
+6 CH1 OR CH2 MOD1 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 1 VOTER INPUT CIRCUIT.
+6 CH1 OR CH2 MOD2 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 2 VOTER INPUT CIRCUIT.
+6 CH1 OR CH2 MOD3 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 3 VOTER INPUT CIRCUIT.
+6 CH1 OR CH2 MOD4 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 4 VOTER INPUT CIRCUIT.
+6 CH1 OR CH2 MOD5 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 5 VOTER INPUT CIRCUITS.

SYMBOL	DEFINITION
+6 CH1 OR CH2 MOD6 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 6 VOTER INPUT CIRCUIT.
+6 CH1 OR CH2 MOD7 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 2 MODULE 7 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD1 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 1 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD2 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 2 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD3 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 3 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD4 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 4 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD5 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 5 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD6 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 6 VOTER INPUT CIRCUIT.
+6 CH1 OR CH3 MOD7 DR	RELAY DRIVER OUTPUT - ALLOWS 6 VOLTS TO CHANNEL 1 OR CHANNEL 3 MODULE 7 VOTER INPUT CIRCUIT.
+6V CH1 MOD1 THROUGH +6V CH1 MOD7	PLUS 6 VOLTS SWITCHED TO VOTER CIRCUIT FOR CHANNEL 1, MODULES 1 THROUGH 7 SELECTION.
+6V CH2 MOD1 THROUGH +6V CH2 MOD7	PLUS 6 VOLTS SWITCHED TO VOTER CIRCUIT FOR CHANNEL 2, MODULES 1 THROUGH 7 SELECTION.
+6V CH3 MOD1 THROUGH +6V CH3 MOD7	PLUS 6 VOLTS SWITCHED TO VOTER CIRCUIT FOR CHANNEL 3, MODULES 1 THROUGH 7 SELECTION.
A1BO NOT ERR	CHANNEL A1 BUFFER OSCILLATOR NOT ERROR LEVEL.
A1DINN	CHANNEL A1, DATA IN, NAND.

SYMBOL	DEFINITION
A1HOPC1T NOT, A2HOPC1T NOT AND A3HOPC1NOT	INVERSE, TRANSLATED CHANNELS A1, A2 AND A3, HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION, LATCH OUTPUT.
A1INTC	CHANNEL A1, INTERRUPT TO COMPUTER.
A1-3A1V-A9V	CHANNELS A1 THROUGH A3, ONE OUTPUT OF ADDRESS REGISTER LATCHES 1 THROUGH 9, VOTED ON.
A1-3CST NOT	INVERSE CHANNEL A1 THOUGH A3, COMPUTER SINGLE - STEP.
A1-3HLTN	CHANNEL A1 THROUGH A3, HALT NAND.
A1-3HLT	CHANNEL A1 THROUGH A3 HALT.
A1-3 BON ERR	CHANNELS A1 THROUGH A3, INVERSE BUFFER OSCILLATOR ERROR.
A1-3 BON	CHANNELS A1 THROUGH A3, INVERSE BUFFER OSCILLATOR.
A1-3 CSTN	CHANNELS A1 THROUGH A3, INVERSE COMPUTER SINGLE STEP.
A1-3 DIN	CHANNELS A1 THROUGH A3, DATA IN.
A1-3 EAMV	CHANNELS A1 THROUGH A3, ONE OUTPUT OF LATCH WHICH INDICATES AN ERROR IN EVEN MEMORIES, VOTED ON.
A1-3 EBMV	CHANNELS A1 THROUGH A3, ONE OUTPUT OF LATCH WHICH INDICATES ERRORS IN ODD MEMORIES, VOTED ON.
A1-3 G5VN	CHANNELS A1 THROUGH A3, INVERSE BIT GATE GENERATOR LATCH 5, VOTER OUTPUT.
A1-3 HOPC1V	CHANNELS A1 THROUGH A3, ONE OUTPUT OF THE LATCH WHICH GENERATES THE HOP CONSTANT FOR STORAGE DURING AN INTERRUPT OPERATION, VOTED ON.
A1-3 IOREG	CHANNELS A1 THROUGH A3, INPUT - OUTPUT REGISTER (SIMULATES MD-7 --- LATCH IN COMPUTER MULTIPLICAND DIVISOR REGISTER).

SYMBOL	DEFINITION
A1-3 MD7V	CHANNELS A1 THROUGH A3, ONE SIDE OF LATCH IN MULTIPLICAND DIVISOR REGISTER, VOTED ON.
A1-3 MR1V	CHANNELS A1 THROUGH A3, ONE SIDE OF LATCH IN THE MULTIPLIER QUOTIENT, PRODUCT - QUOTIENT REGISTER CONDITIONED BY THE OUTPUT OF THE ACCUMULATOR DURING THE INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE, VOTED ON.
A1-3 OP1V-OP4V	CHANNELS A1 THROUGH A3, ONE OUTPUT OF OPERATION CODE REGISTER LATCHES 1 THROUGH 4, VOTED ON.
A1-3 PBVN	CHANNELS A1 THROUGH A3, INVERSE PHASE B, VOTER OUTPUT.
A1-3 PIOV	CHANNELS A1 THROUGH A3, DECODED PROCESS INPUT OUTPUT OPERATION, VOTER OUTPUT.
A1-3 PROV	CHANNELS A1 THROUGH A3, ONE SIDE OF LATCH CONTAINING THE OLD PARTIAL PRODUCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAINDER DURING DIVIDE, VOTED ON.
A1-3 TER	CHANNELS A1 THROUGH A3, TIMING ERROR RESET.
A1-3 TLCV	CHANNELS A1 THROUGH A3, ONE OUTPUT OF LATCH INDICATING TWO SIMULTANEOUS MEMORY ERRORS (ABORT CONDITION), VOTED ON.
A1-3 TRSV	CHANNELS A1 THROUGH A3, ONE OUTPUT OF TRANSFER REGISTER SERIAL OUTPUT LATCH, VOTED ON.
A1-3 WDA	CHANNELS A1 THROUGH A3, W CLOCK PULSE DRIVER TO DATA ADAPTER •
A1-3 XDA	CHANNELS A1 THROUGH A3, X CLOCK PULSE DRIVER TO DATA ADAPTER •
A1-3 YDA	CHANNELS A1 THROUGH A3, Y CLOCK PULSE DRIVER TO DATA ADAPTER •
A1-3 ZDA	CHANNELS A1 THROUGH A3, Z CLOCK PULSE DRIVER TO DATA ADAPTER

SYMBOL	DEFINITION
A1-3TERN	CHANNEL A1 THROUGH A3, TIMING ERROR RESET INVERTED.
A1-3TER	CHANNEL A1 THROUGH A3, TIMING ERROR RESET.
A1-3V4 MOD1-MOD7	CHANNELS A1 THROUGH A3, PLUS 6 VOLTS SWITCHED TO VOTER CIRCUITS FOR MODULES 1 THROUGH 7 SELECTION (SIMPLEX MODE).
A1-3V5 MOD1-MOD7	CHANNELS A1 THROUGH A3, PLUS 12 VOLTS SWITCHED TO VOTER CIRCUITS FOR MODULES 1 THROUGH 7 SELECTION (SIMPLEX MODE).
A1 ADR CON NOT	INVERSE, CHANNEL A1 ADDRESS CONTROL.
A2BO NOT ERR	CHANNEL A2 BUFFER OSCILLATOR NOT ERROR LEVEL.
A2DINN	CHANNEL A2, DATA IN, NAND.
A2INTC	CHANNEL A2, INTERRUPT TO COMPUTER.
A2 ADR CON NOT	INVERSE, CHANNEL A2 ADDRESS CONTROL.
A3BO NOT ERR	CHANNEL A3, BUFFER OSCILLATOR NOT, ERROR LEVEL
A3DINN	CHANNEL A3, DATA IN, NAND.
A3INTC	CHANNEL A3, INTERRUPT TO COMPUTER.
A3 ADR CON NOT	INVERSE, CHANNEL A3 ADDRESS CONTROL.
AAAAA NOT	INVERSE AAAAA.
AAAAA	TRIS1 OR TRDS1 DURING SELF CHECK AND MEMORY LOAD.
AA NOT	EITHER TAPE READER ADDRESS BIT 8 OR TAPE READER OPERAND ADDRESS BIT 8 DURING MEMORY LOAD.
AA	INVERSE TAPE READER ADDRESS BIT 8 OR INVERSE TAPE READER OPERAND ADDRESS BIT 8 DURING MEMORY LOAD.

SYMBOL	DEFINITION
ABCDEF	INTERMEDIATE CONTROL SIGNAL TO SHIFT CONTROL LATCH.
ADR COMP BB NOT	INVERSE ADDRESS COMPARE FROM PHASE B TO PHASE B, LATCH OUTPUT.
ADR COMP BB	ADDRESS COMPARE FROM PHASE B TO PHASE B, LATCH OUTPUT.
ADR COMP	ADDRESS COMPARE LATCH OUTPUT.
ADRSCW NOT	INVERSE ADDRESS SHIFT - REGISTER CLOCK W (CONTROL).
ADRSCW	ADDRESS SHIFT - REGISTER CLOCK W (CONTROL).
ADRSCX NOT	INVERSE ADDRESS SHIFT - REGISTER CLOCK X (CONTROL).
ADRSCX	ADDRESS SHIFT - REGISTER CLOCK X (CONTROL).
ADRSCY NOT	INVERSE ADDRESS SHIFT REGISTER CLOCK Y (CONTROL).
ADRSCY	ADDRESS SHIFT - REGISTER CLOCK Y (CONTROL).
ADRSCZ NOT	INVERSE ADDRESS SHIFT - REGISTER CLOCK Z (CONTROL).
ADRSCZ	ADDRESS SHIFT - REGISTER CLOCK Z (CONTROL).
ADRSO NOT	INVERSE ADDRESS REGISTER SERIAL OUT.
ADRSO	ADDRESS REGISTER SERIAL OUT.
ADRSRA1-8	ADDRESS SHIFT REGISTER, ADDRESS BITS 1 THROUGH 8.
ADRSRA1 NOT-ADRSRA8 NOT	INVERSE ADDRESS SHIFT REGISTER ADDRESS BITS 1 THROUGH 8.
ADRSRA5D NOT	INVERSE ADDRESS SHIFT - REGISTER ADDRESS BIT 5 DELAYED.
ADRSRA5D	ADDRESS SHIFT - REGISTER ADDRESS BIT 5 DELAYED.
ADRSRA9	ADDRESS SHIFT REGISTER, ADDRESS REGISTER BIT 9.

SYMBOL	DEFINITION
ADRSROP1 NOT-ADRSROP4 NOT	INVERSE ADDRESS SHIFT REGISTER OPERATION CODE BITS 1 THROUGH 4.
ADRSROP1 THROUGH ADRSROP4	ADDRESS SHIFT REGISTER OPERATION CODE BITS 1 THROUGH 4.
ADV=CTR=A=NOT	INVERSE, ADVANCE COUNTER A.
ADV CTR1 NOT	INVERSE ADVANCE WORD COUNTER TO 1.
ADV CTR2 NOT	INVERSE ADVANCE WORD COUNTER TO 2.
ADV CTR3 NOT	INVERSE ADVANCE WORD COUNTER TO 3.
ADV CTR4 NOT	INVERSE ADVANCE WORD COUNTER TO 4.
ADV IND 1 AND 2	ADVANCE TAPE, INDICATOR DRIVER 1 AND 2 OUTPUTS.
ADV TAPE	ADVANCE TAPE LEVEL.
A-14	DATA DISPLAY SHIFT REGISTER CONTROL PULSE. NPHA . NBG14
A-2	DATA DISPLAY SHIFT REGISTER CONTROL PULSE. NPHA . NBG2
A-8 NOT	INVERSE DATA DISPLAY SHIFT REGISTER CONTROL PULSE. (INVERSE NPHA. NBG8)
A-8	DATA DISPLAY SHIFT REGISTER CONTROL PULSE. NPHA . NBG8
ALL CH DR	ALL CHANNELS LEVEL - RELAY DRIVER OUTPUT.
ALL CH IND	GROUND LEVEL TO ALL CHANNELS INDICATOR LAMP WHEN ALL CHANNELS ARE SELECTED.
ALL CH SEL NOT	INVERSE ALL CHANNEL SELECTION LEVEL.
ALL IND	ALL CHANNELS SELECTED, INDICATOR DRIVER OUTPUTS.
ANS	ANSWER.

SYMBOL	DEFINITION
APG	ADVANCE PHASE GENERATOR.
APIO RES	ACCUMULATOR REGISTER PROCESS INPUT/OUTPUT RESET.
AUTO=RELAY=DR=IN	AUTOMATIC MODE, RELAY DRIVER INPUT.
AUTO AND FWD	AUTOMATIC MODE AND FORWARD DRIVE LEVEL.
AUTO A	AUTOMATIC MODE LEVEL, FROM DRIVE SOURCE A.
AUTO B	AUTOMATIC MODE LEVEL, FROM DRIVE SOURCE B.
AUTO C	AUTOMATIC MODE LEVEL, FROM DRIVE SOURCE C.
AUTO IND	AUTOMATIC MODE, INDICATOR DRIVER OUTPUT.
AUTO RELAY COIL	DRIVER OUTPUT TO AUTOMATIC MODE, RELAY COIL.
AUTO R START NOT	INVERSE AUTOMATIC RESTART LEVEL.
AUTO R START	AUTOMATIC RESTART LEVEL.
AUTO RSTART	AUTOMATIC RESTART LEVEL.
BA1-3MR1=NOT	INVERSE, CHANNELS A1 THROUGH A3, BUFFER MR1 LEVEL.
BA1-3MR1	CHANNELS A1 THROUGH A3, BUFFER MR1 LEVEL.
BBBBB NOT	INVERSE BBBBB.
BBBBB	TRIS2 OR TRDS2 DURING SELF CHECK AND MEMORY LOAD.
BB NOT	TAPE READER ADDRESS BIT 7 OR TAPE READER OPERAND ADDRESS BIT 7 DURING MEMORY LOAD.
BB	INVERSE TAPE READER ADDRESS BIT 7 OR INVERSE TAPE READER OPERAND ADDRESS BIT 7 DURING MEMORY LOAD.

SYMBOL	DEFINITION
BCDEFG	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES THE COMPARE ERROR PARALLEL LATCH TO SET.
BG OUT NOT	INVERSE BIT GATE OUTPUT.
BIT SYNC ERR NOT	INVERSE BIT SYNCRONIZATION ERROR.
B-12	DATA DISPLAY SHIFT REGISTER CONTROL PULSE. NPHB . NBG12
B-6	DATA DISPLAY SHIFT REGISTER CONTROL PULSE. NPHB . NBG6
BOE SIM NOT	INVERSE BUFFER OSCILLATOR ERROR, SIMULATED.
BRA14P	BUFFER REGISTER A, BIT 14 (PARITY) - SPECIAL OUTPUT OF MEMORY PARITY BIT FOR TEST EQUIPMENT.
BRB14P	BUFFER REGISTER B, BIT 14 (PARITY) - SPECIAL OUTPUT OF MEMORY PARITY BIT FOR TEST EQUIPMENT.
BSC	GATE SERIAL COMPARE.
BSE IND	BIT SYNC ERROR, INDICATOR DRIVER OUTPUT.
BURBON	LATCH OUTPUT, GATES INSTRUCTION ADDRESS BITS INTO HISTORY MODE.
C2 NOT	INVERSE CYCLE CONTROL 2 PULSE.
C2	CYCLE CONTROL 2 PULSE.
CA1DT NOT	INVERSE CONTROL CHANNEL A1 DATA.
CA1G5 NOT	CONTROL, INVERSE CHANNEL A1, BIT GATE GENERATOR 5.
CA1PB NOT	CONTROL, INVERSE CHANNEL A1, PHASE B.
CA1 THROUGH CA3	CONTROL CHANNEL A1 THROUGH A3.
CA2DT NOT	INVERSE CONTROL CHANNEL A2 DATA.

SYMBOL	DEFINITION
CA2G5 NOT	CONTROL, INVERSE CHANNEL A2, BIT GATE GENERATOR 5.
CA2PB NOT	CONTROL, INVERSE CHANNEL A2, PHASE B.
CA3DT NOT	INVERSE CONTROL CHANNEL A3 DATA.
CA3G5 NOT	CONTROL, INVERSE CHANNEL A3, BIT GATE GENERATOR 5.
CA3PB NOT	CONTROL, INVERSE CHANNEL A3, PHASE B.
CAC1	CONTROL ADDRESS COMPARE 1.
CAC2	CONTROL ADDRESS COMPARE 2.
CAC3	CONTROL ADDRESS COMPARE 3.
CAI3	COMPARE 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR INSTRUCTION CHANNEL OF THE 31 MICRSECOND DELAY LINE.
CB RUN NOT	INVERSE CB RUN LEVEL.
CB RUN	CHARACTER - COUNTER BIT RUN LEVEL. RESET LEVEL FOR SIX OF THE NINE POSITION COUNTER LATCHES.
CCCCC NOT	INVERSE CCCCC.
CCCCC	TRIS3 OR TRDS3 DURING SELF CHECK AND MEMORY LOAD.
CC NOT	TAPE READER ADDRESS BIT 6 OR TAPE READER OPERAND ADDRESS BIT 6 DURING MEMORY LOAD.
CC	INVERSE TAPE READER ADDRESS BIT 6 OR INVERSE TAPE READER OPERAND ADDRESS BIT 6 DURING MEMORY LOAD.
CDEFGH	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES THE COMPARE ERROR PARALLEL LATCH TO SET.
CDRES B3A, B, C AND D	COMPUTER DISPLAY RESET LEVEL FROM DRIVE SOURCES A, B, C AND

SYMBOL	DEFINITION
	D OF GATE B3.
CDRES NOT	INVERSE COMPUTER DISPLAY RESET LATCH OUTPUT.
CDRES	COMPUTER DISPLAY RESET LATCH OUTPUT.
CEADRSRIND	COMPARE ERROR, ADDRESS SHIFT REGISTER, INDICATOR DRIVER OUTPUT.
CEADRSR NOT	INVERSE COMPARE ERROR, ADDRESS SHIFT REGISTER LATCH OUTPUT.
CEADRSR	COMPARE ERROR, ADDRESS SHIFT REGISTER LATCH OUTPUT.
CEAI3 IND	COMPARE ERROR, AI3 INDICATOR DRIVER OUTPUT.
CEAI3 NOT	INVERSE COMPARE ERROR, AI3 LEVEL.
CEAOC IND	COMPARE ERROR, ADDRESS OPERATION CODE, INDICATOR DRIVER OUTPUT.
CEAOC NOT	INVERSE COMPARE ERROR, ADDRESS OPERATION CODE LATCH OUTPUT.
CEAOC	COMPARE ERROR, ADDRESS OPERATION CODE LATCH OUTPUT
CEBR14 IND	COMPARE ERROR, BUFFER REGISTER 14, INDICATOR DRIVER OUTPUT.
CEBR14 NOT	INVERSE COMPARE ERROR, BUFFER REGISTER 14 LATCH OUTPUT.
CEBR14	COMPARE ERROR, BUFFER REGISTER 14 LATCH OUTPUT.
CEHOPC1 IND	COMPARE ERROR, HOP CONSTANT FOR STORAGE DURING INTERRUP OPERATION, INDICATOR DRIVER OUTPUT.
CEHOPC1 NOT	INVERSE COMPARE ERROR, HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION.
CEIADR IND	COMPARE ERROR INSTRUCTION ADDRESS, INDICATOR DRIVER OUTPUT.
CEINSDR IND	COMPARE ERROR INSTRUCTION DISPLAY REGISTER, INDICATOR DRIVER

SYMBOL	DEFINITION
	OUTPUT.
CEINSDR NOT	INVERSE COMPARE ERROR INSTRUCTION DISPLAY REGISTER LATCH OUTPUT.
CEINSDR	COMPARE ERROR INSTRUCTION DISPLAY REGISTER LATCH OUTPUT.
CEPAR IND	COMPARE ERROR RARALLEL, INDICATOR DRIVER OUTPUT.
CEPAR	COMPARE ERROR PARALLEL LATCH OUTPUT.
CEPIOADR IND	COMPARE ERROR PROCESS INPUT - OUTPUT ADDRESS REGISTER, INDICATOR DRIVER OUTPUT.
CEPIOADR NOT	INVERSE COMPARE ERROR PROCESS INPUT - OUTPUT ADDRESS REGISTER LATCH OUTPUT.
CEPIOA IND	COMPARE ERROR PROCESS INPUT/OUTPUT ACCUMULATOR, INDICATOR DRIVER OUTPUT.
CEPIOA NOT	INVERSE COMPARE ERROR PROCESS INPUT/OUTPUT ACCUMULATOR LATCH OUTPUT.
CEPIOM IND	COMPARE ERROR PROCESS INPUT/OUTPUT MEMORY, INDICATOR DRIVER OUTPUT.
CEPIOM NOT	INVERSE COMPARE ERROR PROCESS INPUT/OUTPUT MEMORY LATCH OUTPUT.
CERR NOT	INVERSE COMPARE ERROR OR INVERSE ERROR.
CERR	COMPARE ERROR OR ERROR.
CE NOT	INVERSE COMPARE ERROR.
CE	COMPARE ERROR LEVEL.
CESER IND	COMPARE ERROR SERIAL, INDICATOR DRIVER OUTPUT

SYMBOL	DEFINITION
CESSMBR IND	COMPARE ERROR SECTOR, SYLLABLE, MODULE, BUFFER REGISTER, INDICATOR DRIVER OUTPUT.
CESSMBR NOT	INVERSE COMPARE ERROR SECTOR, SYLLABLE, MODULE, BUFFER REGISTER LATCH OUTPUT.
CESSMBR	COMPARE ERROR, SECTOR, SYLLABLE, MODULE, BUFFER REGISTER LATCH OUTPUT
CESSMDR IND	COMPARE ERROR, SECTOR, SYLLABLE, MODULE DISPLAY REGISTER INDICATOR DRIVER OUTPUT.
CESSMDR NOT	INVERSE COMPARE ERROR, SECTOR, SYLLABLE, MODULE DISPLAY REGISTER LATCH OUTPUT.
CESSMDR	COMPARE ERROR, SECTOR, SYLLABLE MODULE DISPLAY REGISTER LATCH OUTPUT
CESSMSC IND	COMPARE ERROR, SECTOR, SYLLABLE, MODULE, SELF CHECK INDICATOR DRIVER OUTPUT.
CESSMSC NOT	INVERSE COMPARE ERROR, SECTOR, SYLLABLE, MODULE, SELF CHECK LATCH OUTPUT.
CESSMSC	COMPARE ERROR, SECTOR, SYLLABLE, MODULE, SELF CHECK LATCH OUTPUT.
CETRS IND	COMPARE ERROR TRANSFER REGISTER SERIAL, INDICATOR DRIVER OUTPUT.
CETRS NOT	INVERSE COMPARE ERROR TRANSFER REGISTER SERIAL.
CH1=0 CH2=1 IND	GROUND LEVEL ROUTED BY CHANNEL RELAY MATRIX TO CH1=0 CH2=1 INDICATOR LAMP. CAUSES LAMP TO LIGHT AND INDICATES ONE OF TWO METHODS TO SELECT CHANNEL 3.
CH1=0 CH3=1 IND	GROUND LEVEL ROUTED BY CHANNEL RELAY MATRIX TO CH1=0 CH3=1 INDICATOR LAMP. CAUSES LAMP TO LIGHT AND INDICATES ONE OF TWO METHODS TO SELECT CHANNEL 2.

SYMBOL	DEFINITION
CH1=1 CH2=0 IND	GROUND LEVEL ROUTED BY CHANNEL RELAY MATRIX TO CH1=1 CH2=0 INDICATOR LAMP. CAUSES LAMP TO LIGHT AND INDICATES ONE OF TWO METHODS TO SELECT CHANNEL 3.
CH1=1 CH3=0 IND	GROUND LEVEL ROUTED BY CHANNEL RELAY MATRIX TO CH1=1 CH3=0 INDICATOR LAMP. CAUSES LAMP TO LIGHT AND INDICATES ONE OF TWO METHODS TO SELECT CHANNEL 2.
CH2=0 CH3=1 IND	GROUND LEVEL ROUTED BY CHANNEL RELAY MATRIX TO CH2=0 CH3=1 INDICATOR LAMP. CAUSES LAMP TO LIGHT AND INDICATES ONE OF TWO METHODS TO SELECT CHANNEL 1.
CH2=1 CH3=0 IND	GROUND LEVEL ROUTED BY CHANNEL RELAY MATRIX TO CH2=1 CH3=0 INDICATOR LAMP. CAUSES LAMP TO LIGHT AND INDICATES ONE OF TWO METHODS TO SELECT CHANNEL 1.
CHANNEL 1 NOT	INVERSE CHANNEL 1 LEVEL
CHANNEL 1	INVERSE TAPE TRACK 1 LEVEL.
CHANNEL 2 NOT	INVERSE CHANNEL 2 LEVEL.
CHANNEL 2	INVERSE TAPE TRACK 2 LEVEL.
CHANNEL 3 NOT	INVERSE CHANNEL 3 LEVEL.
CHANNEL 3	INVERSE TRACK 3 LEVEL.
CHANNEL 4 NOT	INVERSE CHANNEL 4 LEVEL.
CHANNEL 4	INVERSE TAPE TRACK 4 LEVEL.
CHANNEL 5 NOT	INVERSE CHANNEL 5 LEVEL.
CHANNEL 5	INVERSE TAPE TRACK 5 LEVEL.
CHANNEL 6 NOT	INVERSE CHANNEL 6 LEVEL.

SYMBOL	DEFINITION
CHANNEL 6	INVERSE TAPE TRACK 6 LEVEL.
CHET	OR INPUT - RESULTANT OF CONCURRING SPECIFIC TAPE READER BITS AND SPECIFIC BIT GATES. CONTROLS DATA SERIAL OUT LATCH.
CHRES	CHANNEL RESET.
CH 1 IND	CHANNEL 1 ERROR, INDICATOR DRIVER OUTPUT.
CH 2 IND	CHANNEL 2 ERROR, INDICATOR DRIVER OUTPUT.
CH 3 IND	CHANNEL 3 ERROR, INDICATOR DRIVER OUTPUT.
CH OR MOD SEL	CHANNEL OR MODULE SELECTION LEVEL.
CH RES R	CHANNEL RESET LEVEL FROM RELAY CONTACT.
CH SEL ERR1	CHANNEL SELECTION ERROR 1.
CH SEL ERR2	CHANNEL SELECTION ERROR 2.
CH SEL ERR3	CHANNEL SELECTION ERROR 3.
CH SEL ERR4	CHANNEL SELECTION ERROR 4.
CH SEL ERR5	CHANNEL SELECTION ERROR 5.
CH SEL ERR6	CHANNEL SELECTION ERROR 6.
CH SEL ERR	CHANNEL SELECTION ERROR.
CH SEL IND	GROUND LEVEL APPLIED TO CHANNEL SELECTION INDICATOR LAMP WHE N CHANNEL OR MODULE SELECTION RELAY IS NOT ENERGIZED.
CH SEL	CHANNEL SELECTION LEVEL.
CIR=MDPH=B8=NOT	INVERSE, CIRCULATE MULTIPLY - DIVIDE PAST HISTORY BIT 8. (AL LOWS SYNC TO PAST HISTORY).

SYMBOL	DEFINITION
CIR=MDPH=NOT	INVERSE, CIRCULATE MULTIPLY - DIVIDE PAST HISTORY.
CIR=MDPH	CIRCULATE, MULTIPLY - DIVIDE PAST HISTORY.
CIR NOT	INVERSE CIRCULATE.
CIR	CIRCULATE.
C-10	DATA DISPLAY SHIFT REGISTER CONTROL PULSE - NPHC . NBG10.
C-3 NOT	INVERSE CYCLE CONTROL 3 PULSE.
C-3	CYCLE CONTROL 3 PULSE.
C-4	DATA DISPLAY SHIFT REGISTER CONTROL PULSE - NPHC . NBG4.
CLE IND	CLOCK ERROR, INDICATOR DRIVER OUTPUT.
CLE NOT	INVERSE CLOCK ERROR LATCH OUTPUT.
CLE SIM NOT	INVERSE CLOCK ERROR, SIMULATED.
CLESIM 0	CLOCK ERROR SIMULATED, FAIL TO 0.
CLESIM 1	CLOCK ERROR SIMULATED, FAIL TO 1.
CL DO NOT	RESET LEVEL RESULTING FROM THE ERROR RESET SWITCH.
COMP REF GRD1-2-3	COMPUTER REFERENCE GROUND, TIE POINTS 1, 2, AND 3
CPE NOT	INVERSE COMPUTER PARITY ERROR LEVEL.
CPE	COMPUTER PARITY ERROR.
CPHG NOT	INVERSE PAST HISTORY GATE.
CPHG	PAST HISTORY GATE.
CST ADV IND1	COMPUTER SINGLE - STEP ADVANCE, INDICATOR DRIVER 1 OUTPUT.

SYMBOL	DEFINITION
CST ADV IND2	COMPUTER SINGLE - STEP ADVANCE, INDICATOR DRIVER 2 OUTPUT.
CST OFF IND	COMPUTER SINGLE STEP OFF, INDICATOR DRIVER OUTPUT.
CST ON IND	COMPUTER SINGLE STEP ON, INDICATOR DRIVER OUTPUT.
CSU	CONTROL LEVEL FOR MANUAL ADVANCE OF COMPUTER SINGLE STEP
CTR=GATE	COUNTER GATE.
CTRSA	COMPARE TRANSFER REGISTER SERIAL LEVEL FROM A DRIVE SOURCE.
CTRS NOT	INVERSE COMPARE, TRANSFER REGISTER SERIAL.
CTRS	COMPARE TRANSFER REGISTER SERIAL.
CYC2 AND 3	CYCLE 2 AND 3.
CYC3OR4	CYCLE 3 OR 4.
CYC3 NOT	INVERSE CYCLE 3.
CYC4 NOT	INVERSE CYCLE 4.
CYCL4 NOT	INVERSE CYCLE 4.
CYCO	CYCLE O.
DA COMP IND	DATA ADDRESS COMPARE, INDICATOR DRIVER OUTPUT.
DDA NOT	INVERSE DDA.
DDA	DATA DISPLAY MODE LEVEL FROM A DRIVE SOURCE.
DDCPW	DOUBLE, DELAYED CLOCK PULSE W.
DDDCPW	DELAYED, DELAYED, DELAYED CLOCK PULSE W.

SYMBOL	DEFINITION
DDDDD NOT	INVERSE DDDDD.
DDDDD	TRIS4 OR TRDS4 DURING SELF CHECK AND MEMORY LOAD.
DD IND	DATA DISPLAY MODE INDICATOR DRIVER OUTPUT.
DD NOT	TAPE READER ADDRESS BIT 5 OR TAPE READER OPERAND ADDRESS BIT 5 DURING MEMORY LOAD.
DD RELAY COIL	DATA DISPLAY RELAY COIL (RELAY DRIVER OUTPUT).
DD	INVERSE TAPE READER ADDRESS BIT 5 OR INVERSE TAPE READER OPERAND ADDRESS BIT 5 DURING MEMORY LOAD.
DDSC1	DATA DISPLAY SHIFT - REGISTER, CONTROL 1.
DDSC2 NOT	INVERSE DATA DISPLAY SHIFT - REGISTER CONTROL 2 LATCH OUTPUT.
DDSC2	DATA DISPLAY SHIFT - REGISTER, CONTROL 2.
DEA1EAM	DISAGREEMENT ERROR, CHANNEL A1, ERROR IN EVEN MEMORIES.
DEA1HOPC1 NOT, DEA2HOPC1 NOT AND DEA3HOPC1 NOT	INVERSE DEA1HOPC1, DEA2HOPC1 AND DEA3HOPC1 OUTPUTS.
DEA1HOPC1, DEA2HOPC1 AND DEA3HOPC1	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION.
DEA1MR1 NOT	INVERSE DISAGREEMENT ERROR, CHANNEL A1, MR1.
DEA2EAM	DISAGREEMENT ERROR, CHANNEL A2, ERROR IN EVEN MEMORIES.
DEA2MR1 NOT	INVERSE DISAGREEMENT ERROR, CHANNEL A2, MR1.
DEA3EAM	DISAGREEMENT ERROR, CHANNEL A3, ERROR IN EVEN MEMORIES.
DEA3MR1 NOT	INVERSE DISAGREEMENT ERROR, CHANNEL A3, MR1.

SYMBOL	DEFINITION
DEFGHJ	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES THE COMPARE ERROR PARALLEL LATCH TO SET
DIEADR COMP	DATA INTERFACE EXERCIZER ADDRESS COMPARE.
DIEMAN IND	DATA INTERFACE EXERCIZER MANUAL, INDICATOR DRIVER OUTPUT.
DIEMAN	DATA INTERFACE EXERCIZER MANUAL LEVEL.
DIE A1 IND1 THROUGH DIE A9 IND 1	DATA INTERFACE EXERCIZER ADDRESS REGISTER BIT 1 THROUGH BIT 9, INDICATOR DRIVER 1 OUTPUTS.
DIE A1 IND2 THROUGH DIE A9 IND 2	DATA INTERFACE EXERCIZER ADDRESS REGISTER BIT 1 THROUGH BIT 9, INDICATOR DRIVER 2 OUTPUTS.
DIE A1 NOT THROUGH DIEA9NOT	INVERSE DATA INTERPACE EXERCIZER ADDRESS REGISTER BITS 1 THROUGH 9.
DIE ADR CP	ONE OUTPUT OF THE DATA INTERFACE EXERCISER ADDRESS COMPARE LATCH.
DIE AIL THROUGH DIE A9L	DATA INTERFACE EXERCIZER ADDRESS REGISTER BIT 1 THROUGH BIT 9, LAMP DRIVER INPUTS.
DIE SGC	DATA INTERFACE EXERCIZER, SATURN GUIDANCE COMPUTER LEVEL.
DIES SGC IND	DATA INTERFACE EXERCIZER, SATURN GUIDANCE COMPUTER, INDICATOR DRIVER OUTPUT.
DISAI3 NOT	INVERSE DISPLAY AI3.
DISAI3	DISPLAY AI3.
DISIADR	DISPLAY INSTRUCTION ADDRESS DISPLAY REGISTER.
DIS RPT IND	DISPLAY REPEAT, INDICATOR DRIVER OUTPUT.
DIS SIN IND	DISPLAY SINGLE, INDICATOR DRIVER OUTPUT.

SYMBOL	DEFINITION
DIS SSMDRA	DISPLAY SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER LEVEL FRO M DRIVE SOURCE A.
DIS SSMDRB	DISPLAY SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER LEVEL FRO M DRIVE SOURCE B.
DLY IN	DELAY CIRCUIT INPUT.
DON	OR INPUT - RESULTANT OF CONCURRING SPECIFIC TAPE READER BITS AND SPECIFIC BIT GATES. CONTROLS DATA SERIAL OUT LATCH.
DRIVE LEFT	ONE LEVEL - REVERSE RUN TAPE READER.
DRIVE RIGHT	ONE LEVEL - FORWARD RUN TAPE READER.
DSMC NOT	INVERSE DATA SECTOR MODULE COMPARE.
DSMC	DATA SECTOR MODULE COMPARE.
DSMSO NOT	INVERSE DATA SELECTOR, MEMORY - MODULE SERIAL OUT LATCH OUTP UT.
DSMSO	DATA SELECTOR, MEMORY - MODULE SERIAL OUT LATCH OUTPUT.
DSO=B1	DATA SERIAL OUT, OUTPUT OF GATE B1.
DSOG	DISPLAY SERIAL OUT GATE.
DSO NOT	INVERSE DATA SERIAL OUT.
DTDRB1IND-B25IND	DATA DISPLAY REGISTER BIT 1 THROUGH BIT 25, INDICATOR DRIVER OUTPUTS.
DTDRB1-B25	DATA DISPLAY REGISTER BIT 1 THROUGH BIT 25.
DTDRB1 NOT THROUGH DTDRB25 NOT	INVERSE DATA DISPLAY REGISTER BIT 1 THROUGH B 25.
DTDRCP1A THROUGH DTDRCP4A	DATA DISPLAY REGISTER CLOCK PULSES 1 THROUGH 4 FROM A DRIVE SOURCES.

SYMBOL	DEFINITION
DTDRCP1B THROUGH DTDRCP4B	DATA DISPLAY REGISTER CLOCK PULSES 1 THROUGH 4 FROM B DRIVE SOURCE.
DTDR DATA NOT	INVERSE DATA DISPLAY REGISTER, DATA.
DTDR DATA	DATA DISPLAY REGISTER, DATA.
DTDRSIGN IND	DATA DISPLAY REGISTER SIGN BIT, INDICATOR DRIVER OUTPUT.
DTDRSIGN NOT	INVERSE DATA DISPLAY REGISTER SIGN BIT.
DTDRSIGN	DATA DISPLAY REGISTER SIGN BIT.
DTRPT IND	DATA REPEAT, INDICATOR DRIVER OUTPUT.
DTRPT NOT IND	INVERSE, DATA REPEAT, INDICATOR DRIVER OUTPUT.
DTRPT NOT	INVERSE DATA REPEAT LEVEL.
DTRPT	DATA REPEAT.
DTSO NOT	INVERSE DATA SERIAL OUT LATCH OUTPUT.
DTSO	DATA SERIAL OUT LATCH OUTPUT.
EA19-DP1-3 NOT	INVERSE ERROR LEVEL, CHANNEL A1, ADDRESS REGISTER BIT 9 AND OPERATION CODE BITS 1-3.
EA1A1-4 NOT	INVERSE ERROR LEVEL, CHANNEL A1, ADDRESS REGISTER BITS 1-4.
EA1A1 NOT THROUGH EA1A9 NOT	INVERSE ERROR LEVEL, CHANNEL A1, ADDRESS REGISTER BITS 1 THR OUGH 9.
EA1A5-8 NOT	INVERSE ERROR LEVEL, CHANNEL A1, ADDRESS REGISTER BITS 5-8.
EA1AI3 IND, EA2AI3 IND AND EA3 AI3 IND	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR INSTRUCTION COUNTER CHANNEL OF THE 31 MICROSECOND DELAY LINE, INDICATOR DRIVER OUTPUT.

SYMBOL	DEFINITION
EA1AI3 NOT, EA2AI3 NOT AND EA3 AI3 NOT	INVERSE EA1AI3, EA2AI3 AND EA3AI3 LATCH OUTPUTS.
EA1AI3, EA2AI3 AND EA3AI3	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR INSTRUCTION COUNTER CHANNEL OF THE 31 MICROSECOND DELAY LINE, LATCH OUTPUT
EA1AOC IND	ERROR, CHANNEL A1, ADDRESS AND OPERATION CODE INDICATOR DRIV ER OUTPUT.
EA1BO NOT IND	INVERSE DISAGREEMENT ERROR, CHANNEL A1, BUFFER OSCILLATOR, I NDICATOR DRIVER OUTPUT.
EA1BO NOT NOT	INVERSE INVERTED DISAGREEMENT ERROR, CHANNEL A1, BUFFER OSCI LLATOR.
EA1EAM IND, EA2EAM IND AND EA3 EAM IND	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, ERROR IN EVEN ME MORIES, INDICATOR DRIVER OUTPUT.
EA1EBM IND	ERROR, CHANNEL A1, ERROR IN (B) ODD MEMORIES, INDICATOR DRIV ER OUTPUT.
EA1EBM NOT	INVERSE ERROR, CHANNEL A1, ERROR IN (B) ODD MEMORIES LEVEL.
EA1G5 NOT IND	INVERSE ERROR, BIT GATE GENERATOR LATCH 5, INDICATOR DRIVER OUTPUT.
EA1G5 NOT NOT	INVERSE, INVERTED ERROR, CHANNEL A1 BIT GATE GENERATOR LATCH 5.
EA1G5 NOT	INVERSE ERROR, CHANNEL A1, BIT GATE GENERATOR LATCH 5.
EA1HOPC1 IND, EA2HOPC1 IND AND EA3HOPC1 IND	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION, INDICATOR DRIVER OUTPUT.
EA1HOPC1 NOT, EA2HOPC1 NOT AND EA3HOPC1 NOT	INVERSE DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, HOP CONS TANT FOR STORAGE DURING INTERRUPT OPERATION.

SYMBOL	DEFINITION
EA1HOPC1, EA2HOPC1 AND EA3HOPC 1	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION.
EA1-3	ERROR CHANNELS A1 THROUGH A3.
EA1MD7 IND, EA2MD7 IND AND EA3 MD7 IND	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, MULTIPLICAND - D IVISOR REGISTER LATCH 7, INDICATOR DRIVER OUTPUT.
EA1MD7 NOT, EA2MD7 NOT AND EA3 MD7 NOT	INVERSE EA1MD7, EA2MD7 AND EA3MD7 LATCH OUTPUTS.
EA1MD7, EA2MD7 AND EA3MD7	DISAGREEMENT ERROR, CHANNELS A1, CHANNEL A2 AND CHANNEL A3, MULTIPLICAND - DIVISOR REGISTER LATCH 7.
EA1MR1 IND	ERROR, CHANNEL A1, MR1 INDICATOR DRIVER OUTPUT.
EA1MR1 NOT	INVERSE ERROR, CHANNEL A1, MR1 LATCH OUTPUT.
EA1OP1 NOT THROUGH EA1OP4 NOT	INVERSE ERROR LEVEL, CHANNEL A1, OPERATION CODE BITS 1 THROU GH 4.
EA1PB NOT IND	INVERSE ERROR, CHANNEL A1, PHASE B, INDICATOR DRIVER OUTPUT.
EA1PB NOT NOT	INVERSE INVERTED ERROR, CHANNEL A1, PHASE B, LATCH OUTPUT.
EA1PB NOT	INVERSE ERROR, CHANNEL A1 PHASE B, LATCH OUTPUT.
EA1PRO IND, EA2PRO IND AND EA3 PRO IND	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, OLD PARTIAL PROD UCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD R EMAINDER DURING DIVIDE, INDICATOR DRIVER OUTPUT.
EA1PRO NOT, EA2PRO NOT AND EA3 PRO NOT	INVERSE EA1PRO, EA2PRO AND EA3PRO LATCH OUTPUTS.
EA1PRO, EA2PRO AND EA3PRO	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, OF OLD PARTIAL P RODUCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OL D REMAINDER DURING DIVIDE.
EA1TLC IND	ERROR, CHANNEL A1, TWO SIMULTANEOUS MEMORY ERRORS, INDICATOR

SYMBOL	DEFINITION
	DRIVER OUTPUT.
EA1TRS IND, EA2TRS IND, EA3TRS IND	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, TRANSFER REGISTER SERIAL, INDICATOR DRIVER OUTPUT.
EA1TRS NOT, EA2TRS NOT AND EA3TRS NOT	INVERSE EA1TRS, EA2TRS AND EA3TRS LATCH OUTPUTS.
EA1TRS, EA2TRS AND EA3TRS	DISAGREEMENT ERROR, CHANNELS A1, A2 AND A3, TRANSFER REGISTER SERIAL.
EA2A1-4 NOT	INVERSE ERROR LEVEL, CHANNEL A2, ADDRESS REGISTER BITS 1-4.
EA2A1 NOT THROUGH EA2A9 NOT	INVERSE ERROR LEVEL, CHANNEL A2, ADDRESS REGISTER BITS 1 THROUGH 9.
EA2A5-8 NOT	INVERSE ERROR LEVEL, CHANNEL A2, ADDRESS REGISTER BITS 5-8.
EA2A9-OP1-3 NOT	INVERSE ERROR LEVEL, CHANNEL A2, ADDRESS REGISTER BIT 9 AND OPERATION CODE BITS 1-3.
EA2AOC IND	ERROR, CHANNEL A2, ADDRESS AND OPERATION CODE INDICATOR DRIVER OUTPUT.
EA2BO NOT IND	INVERSE DISAGREEMENT ERROR, CHANNEL A2, BUFFER OSCILLATOR, INDICATOR DRIVER OUTPUT.
EA2BO NOT NOT	INVERSE INVERTED DISAGREEMENT ERROR, CHANNEL A2, BUFFER OSCILLATOR LEVEL.
EA2EBM IND	ERROR, CHANNEL A2, ERROR IN (B) ODD MEMORIES, INDICATOR DRIVER OUTPUT.
EA2EBM NOT	INVERSE ERROR, CHANNEL A2, ERROR IN (B) ODD MEMORIES LEVEL.
EA2G5 NOT IND	INVERSE ERROR, BIT GATE GENERATOR LATCH 5, INDICATOR DRIVER OUTPUT.
EA2G5 NOT NOT	INVERSE INVERTED ERROR, CHANNEL A2, BIT GATE GENERATOR LATCH

SYMBOL	DEFINITION
	5.
EA2G5 NOT	INVERSE ERROR, CHANNEL A2, BIT GATE GENERATOR LATCH 5
EA2MR1 IND	ERROR, CHANNEL A2, MR1 INDICATOR DRIVER OUTPUT.
EA2MR1 NOT	INVERSE ERROR, CHANNEL A2, MR1 LATCH OUTPUT.
EA2OP1 NOT THROUGH EA2OP4 NOT	INVERSE ERROR LEVEL, CHANNEL A2, OPERATION CODE BITS 1 THROU GH 4.
EA2PB NOT IND	INVERSE ERROR, CHANNEL A2, PHASE B, INDICATOR DRIVER OUTPUT.
EA2PB NOT NOT	INVERSE INVERTED ERROR, CHANNEL A2 PHASE B, LATCH OUTPUT.
EA2PB NOT	INVERSE ERROR, CHANNEL A2 PHASE B, LATCH OUTPUT.
EA2TLC IND	ERROR, CHANNEL A2, TWO SIMULTANEOUS MEMORY ERRORS, INDICATOR DRIVER OUTPUT.
EA3A1-4 NOT	INVERSE ERROR LEVEL, CHANNEL A3, ADDRESS REGISTER BITS 1-4.
EA3A1 NOT THROUGH EA3A9 NOT	INVERSE ERROR LEVEL, CHANNEL A3, ADDRESS REGISTER BITS 1 THR OUGH 9.
EA3A5-8 NOT	INVERSE ERROR LEVEL, CHANNEL A3, ADDRESS REGISTER BITS 5-8.
EA3A9-OP1-3 NOT	INVERSE ERROR LEVEL, CHANNEL A3, ADDRESS REGISTER BIT 9 AND OPERATION CODE BITS 1-3.
EA3AOC IND	ERROR, CHANNEL A3, ADDRESS AND OPERATION CODE INDICATOR DRIV ER OUTPUT.
EA3BO NOT IND	INVERSE DISAGREEMENT ERROR, CHANNEL A3, BUFFER OSCILLATOR, I NDICATOR DRIVER OUTPUT.
EA3BO NOT NOT	INVERSE, INVERTED DISAGREEMENT ERROR, CHANNEL A3, BUFFER OSC ILLATOR LEVEL.

SYMBOL	DEFINITION
EA3EBM IND	ERROR, CHANNEL A3, ERROR IN (B) ODD MEMORIES, INDICATOR DRIVER OUTPUT.
EA3EBM NOT	INVERSE ERROR, CHANNEL A3, ERROR IN (B) ODD MEMORIES LEVEL.
EA3G5 NOT IND	INVERSE ERROR, BIT GATE GENERATOR LATCH 5, INDICATOR DRIVER OUTPUT.
EA3G5 NOT NOT	INVERSE INVERTED ERROR, CHANNEL A3, BIT GATE GENERATOR LATCH 5.
EA3G5 NOT	INVERSE ERROR, CHANNEL A3, BIT GATE GENERATOR LATCH 5.
EA3MR1 IND	ERROR, CHANNEL A3, MR1 INDICATOR DRIVER OUTPUT.
EA3MR1 NOT	INVERSE ERROR, CHANNEL A3, MR1 LATCH OUTPUT.
EA3OP1 NOT THROUGH EA3OP4 NOT	INVERSE ERROR LEVEL, CHANNEL A3, OPERATION CODE BITS 1 THROUGH 4.
EA3PB NOT IND	INVERSE ERROR, CHANNEL A3, PHASE B, INDICATOR DRIVER OUTPUT.
EA3PB NOT NOT	INVERSE INVERTED ERROR, CHANNEL A3, PHASE B, LATCH OUTPUT.
EA3PB NOT	INVERSE ERROR, CHANNEL A3, PHASE B, LATCH OUTPUT.
EA3TLC IND	ERROR, CHANNEL A3, TWO SIMULTANEOUS MEMORY ERRORS, INDICATOR DRIVER OUTPUT.
EARLY IND1	MEMORY CLOCK EARLY, INDICATOR DRIVER 1 OUTPUT.
EARLY IND2	MEMORY CLOCK EARLY, INDICATOR DRIVER 2 OUTPUT.
EDDI1	ERROR DISAGREEMENT DETECTOR INVERTED OUTPUT 1.
EDDI2	ERROR DISAGREEMENT DETECTOR INVERTED OUTPUT 2.
EEEEE NOT	INVERSE EEEEE.

SYMBOL	DEFINITION
EEEEE	TRSYLO OR TRDX DURING SELF CHECK AND MEMORY LOAD.
EE NOT	TAPE READER ADDRESS BIT 4 OR TAPE READER OPERAND ADDRESS BIT 4 DURING MEMORY LOAD.
EE	INVERSE TAPE READER ADDRESS BIT 4 OR INVERSE TAPE READER OPERAND ADDRESS BIT 4 DURING MEMORY LOAD.
EFGHJK	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES THE COMPARE ERROR PARALLEL LATCH TO SET.
EOP	END OF PROGRAM BIT.
EP15	ERROR PULSE 15.
EP2-3	ERROR PULSES 2 THROUGH 13.
ERCEIL	INVERTED GATE OUTPUT WHOSE INPUTS ARE ERROR NOT + COMPARE ERROR NOT + ILLEGAL PATH NOT.
ERR1 B2	ERROR LEVEL 1, OUTPUT OF GATE B2.
ERR1 B7	ERROR 1, GATE B7 OUTPUT.
ERR1	ERROR 1
ERR2 B2	ERROR LEVEL 2, OUTPUT OF GATE B2.
ERR2	ERROR 2
ERR 1B OR 4B NOT	INVERSE ERR 1B OR 4B LEVEL.
ERR 1B OR 4B	ERROR 1B OR 4B - MISSING CLOCK DETECTOR LATCH. CAUSES STOP CLOCK WHEN CLOCKS 1 OR 4 ARE MISSING.
ERR 2B OR 4A NOT	INVERSE ERROR 2B OR 4A LEVEL.
ERR 2B OR 4A	ERROR 2B OR 4A - MISSING CLOCK DETECTOR LATCH. CAUSES STOP CLOCK WHEN CLOCKS 2 OR 4 ARE MISSING.

SYMBOL	DEFINITION
ERR NOT	INVERSE ERROR LEVEL.
ERR RESET NOT	INVERTED ERROR RESET LEVEL.
ERR RES B4A	ERROR RESET, OUTPUT FROM GATE B4, DRIVE SOURCE A.
ERR RES B4	ERROR RESET LEVEL, OUTPUT FROM GATE B4.
ERR RES B7	ERROR RESET, OUTPUT FROM GATE B7.
ERR RES IA	ERROR RESET LEVEL, OUTPUT OF INVERTER A.
ERR RES IB	ERROR RESET LEVEL, OUTPUT OF INVERTER B.
ERR RES NOT B6	INVERSE ERROR RESET - INPUT TOGATE B6.
ERR RES NOT	INVERSE, ERROR RESET LEVEL.
ERR RES	ERROR RESET. RESULTS FROM ERROR RESET SWITCH, RESETS ERROR DEVICES.
ERR	ERROR
ERR TEST B4A	ERROR TEST LEVEL, OUTPUT FROM GATE B4 DRIVE SOURCE A.
ERR TEST B4	ERROR TEST, INPUT TO GATE B4.
ERR TEST B7	ERROR TEST, OUTPUT FROM GATE B7.
ERR TEST NOT	INVERSE ERROR TEST LEVEL.
ERR TEST	ONE OUTPUT OF ERROR TEST LATCH.
ESR	ERROR STOP READER.
ESSMBR	ERROR, SECTOR, SYLLABLE, MODULE BUFFER REGISTER
ETI1	ERROR TEST LEVEL, INVERTER 1 OUTPUT.

SYMBOL	DEFINITION
ETI2	ERROR TEST LEVEL, INVERTER 2 OUTPUT.
ETI3	ERROR TEST LEVEL, INVERTER 3 OUTPUT.
EVEN	EVEN, DATA TRANSFER CONTROL LEVEL.
FEED TRACK	TAPE SPROCKET HOLES FROM WHICH TAPE READER TIMING IS DERIVED . THE TIME BETWEEN HOLES IS 2000 + 60 MICROSECONDS BASED ON A TAPE SPEED OF 50 INCHES PER SECOND AND 10 DRIVE HOLES PER INCH.
FF NOT	TAPE READER ADDRESS BIT 3 OR TAPE READER OPERAND ADDRESS BIT 3 DURING MEMORY LOAD.
FF	INVERSE TAPE READER ADDRESS BIT 3 OR INVERSE TAPE READER OPE RAND ADDRESS BIT 3 DURING MEMORY LOAD.
FGHJKL	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUS ES THE COMPARE ERROR PARALLEL LATCH TO SET.
FIR WO NOT	INVERSE FIRST WORD LATCH OUTPUT.
FIRWO	ONE OUTPUT OR FIRST WORD LATCH.
FREE RUN SS	FREE RUN SINGLE SHOT
FRR NOT	INVERSE FREE RUN REGISTER.
FRR	FREE RUN REGISTER.
FRSS 50	FREE RUN SINGLE SHOT AND 50 CYCLES PER SECOND MULTIVIBRATOR.
FRTR IND	FREE RUN TAPE READER, INDICATOR DRIVER OUTPUT.
F RUN	FORWARD RUN TAPE READER.
F START	FORWARD START LEVEL.

SYMBOL	DEFINITION
FWD A	FORWARD A. TAPE MOTION CONTROL LEVEL FROM A DRIVE SOURCE.
FWD IND	FORWARD, INDICATOR DRIVER OUTPUT.
G1 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 1.
G1	ONE OUTPUT BIT GATE GENERATOR LATCH 1.
G2 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 2.
G2	ONE OUTPUT BIT GATE GENERATOR LATCH 2
G3 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 3.
G3	ONE OUTPUT BIT GATE GENERATOR LATCH 3.
G4 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 4
G4	ONE OUTPUT BIT GATE GENERATOR LATCH 4.
G5 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 5.
G5	ONE OUTPUT BIT GATE GENERATOR LATCH 5.
G6 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 6.
G6	ONE OUTPUT BIT GATE GENERATOR LATCH 6.
G7 NOT	ZERO OUTPUT BIT GATE GENERATOR LATCH 7.
G7	ONE OUTPUT BIT GATE GENERATOR LATCH 7
GACISS	GATE, ADVANCE COMPUTER ONE INSTRUCTION DURING SINGLE STEP.
GG NOT	TAPE READER ADDRESS BIT 2 OR TAPE READER OPERAND ADDRESS BIT 2 DURING MEMORY LOAD.
GG	INVERSE TAPE READER ADDRESS BIT 2 OR INVERSE TAPE READER OPERAND ADDRESS BIT 2 DURING MEMORY LOAD.

SYMBOL	DEFINITION
GHJKLM	LOGIC TIE POINT - THE OR OUTPUT COMPARE ERROR LEVEL WHICH CA USES THE COMPARE ERROR PARALLEL LATCH TO SET.
GMDO	GATE, MULTIPLY - DIVIDE OUT.
GMMH	GATE MULTIPLY MULTIPLY HOLD.
GPHMMD	GATE, PAST HISTORY, MULTIPLY, MULTIPLY - DIVIDE.
GRD SP1	ACME GROUND LEVEL TO SPARE PROBE 1.
GRD SP2	ACME GROUND LEVEL TO SPARE PROBE 2.
HADR	HISTORY ADDRESS REGISTER.
HELP NOT	INVERSE ERROR ENABLE LEVEL IN SELF CHECK MODE.
HH NOT	TAPE READER ADDRESS BIT 1 OR TAPE READER OPERAND ADDRESS BIT 1 DURING MEMORY LOAD.
HH	INVERSE TAPE READER ADDRESS BIT 1 OR INVERSE TAPE READER OPE RAND ADDRESS BIT 1 DURING MEMORY LOAD.
HISIA	ONE OUTPUT, HISTORY INSTRUSTION ADDRESS LATCH
HISTMD7	HISTORY LATCH 7 OF MULTIPLICAND DIVISOR REGISTER.
HIST AI3	HISTORY, 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR INSTR UCTION CHANNEL OF THE 31 MICROSECOND DELAY LINE.
HIST MR1	HISTORY OF LATCH IN MULTIPLIER, QUOTIENT, PRODUCT - QUOTIENT REGISTER CONDITIONED BY THE OUTPUT OF THE ACCUMULATOR DURIN G THE INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUO TIENT BITS DURING DIVIDE.
HIST PP1	HISTORY, PARTIAL PRODUCT 1.
HIST TRS	HISTORY, TRANSFER REGISTER SERIAL LATCH.

SYMBOL	DEFINITION
HJKLMN	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES COMPARE ERROR, SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER LATCH TO SET.
HLT AUTO IND	HALT AUTOMATIC, INDICATOR DRIVER OUTPUT.
HLT IND1	HALT, INDICATOR DRIVER 1 OUTPUT.
HLT IND2	HALT, INDICATOR DRIVER 2 OUTPUT.
HLT MAN IND	HALT MANUAL, INDICATOR DRIVER OUTPUT.
HWC EVEN	HISTORY WORD COUNTER EVEN - LATCH OUTPUT - WORD COUNTER CONTROL LEVEL.
HWC ODD	HISTORY WORD COUNTER ODD - LATCH OUTPUT - WORD COUNTER CONTROL LEVEL.
IAA1 IND-IAA8 IND	INSTRUCTION ADDRESS, ADDRESS BITS 1 THROUGH 8, INDICATOR DRIVER OUTPUTS.
IAC NOT	INVERSE INSTRUCTION ADDRESS COMPARE.
IAC	INSTRUCTION ADDRESS COMPARE.
IADRA1 NOT-IADRA8 NOT	INVERSE INSTRUCTION ADDRESS DISPLAY REGISTER ADDRESS BITS 1 THROUGH 8.
IA COMP IND	INSTRUCTION ADDRESS COMPARE, INDICATOR DRIVER OUTPUT.
IA RELAY COIL	DRIVER OUTPUT TO INSTRUCTION ADDRESS RELAY COIL.
ILLEGAL PATH IND	ILLEGAL PATH, INDICATOR DRIVER OUTPUT.
INHIBIT	PLUS 4 VOLT LEVEL ROUTED THROUGH NORMALLY OPENED READER INHIBIT RELAY (01A9K15) CONTACTS. INHIBITS LEFT OR RIGHT DRIVE AND LEFT OR RIGHT BRAKE ON TAPE READER AND SPOOLER.

SYMBOL	DEFINITION
INSBRAB	INSTRUCTION BUFFER REGISTER A, FROM B DRIVE SOURCE.
INSBRA IND	INSTRUCTION BUFFER REGISTER A, INDICATOR DRIVER OUTPUT.
INSBRB IND	INSTRUCTION BUFFER REGISTER B, INDICATOR DRIVER OUTPUT.
INSDROA1-8	INSTRUCTION DISPLAY REGISTER OPERAND ADDRESS 1 THROUGH 8.
INSDROA1 NOT -8 NOT	INVERSE INSTRUCTION DISPLAY REGISTER OPERAND ADDRESS BITS 1 THROUGH 8.
INSDROA9 NOT	INVERSE INSTRUCTION DISPLAY REGISTER OPERAND ADDRESS BIT 9.
INSDROA9	INSTRUCTION DISPLAY REGISTER OPERAND ADDRESS BIT 9.
INSDROP1-4	INSTRUCTION DISPLAY REGISTER OPERATION CODE BITS 1 THROUGH 4 .
INSDROP1 NOT-4 NOT	INVERSE INSTRUCTION DISPLAY REGISTER OPERATION CODE BITS 1 T HROUGH 4.
INSOA1 IND-INSOA9 IND	INSTRUCTION OPERAND ADDRESS 1 THROUGH 9, INDICATOR DRIVER OU TPUTS.
INSOP1 IND-INSOP4 IND	INSTRUCTION OPERATION CODE BITS 1 THROUGH 4, INDICATOR DRIVE R OUTPUTS.
INSSO NOT	INVERSE INSTRUCTION SERIAL OUT LATCH OUTPUT.
INSSO	INSTRUCTION SERIAL OUT LATCH OUTPUT.
INTERC	INTERRUPT, OUTPUT FROM C DRIVE SOURCE.
INTER IND1AND2	INTERRUPT, IND DRIVER 1 AND 2 OUTPUTS.
INTER L	INTERRUPT LAMP DRIVER INPUT.
INTER NOT	INVERSE INTERRUPT.

SYMBOL	DEFINITION
INV ERR IND	INVERT ERROR, INDICATOR DRIVER OUTPUT.
INV ERR	INVERT ERROR LEVELS, CHECKS ERROR CHECK CIRCUITS IN SELF CHECK MODE.
ISSC NOT	INVERSE INSTRUCTION, SYLLABLE, SECTOR COMPARE.
ISSC	INSTRUCTION, SYLLABLE, SECTOR COMPARE.
JKLMNP	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES COMPARE ERROR, SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER LATCH TO SET.
KLMNPQ	LOGIC TIE POINT - THE OR OUTPUT COMPARE ERROR LEVEL WHICH CAUSES COMPARE ERROR, SECTOR, SYLLABLE, MODULE DISPLAY REGISTER LATCH TO SET.
KSSMD NOT	INVERSE KEEP SECTOR, SYLLABLE, MODULE, DISPLAY.
KWIAF NOT	RESULTS FROM THE PRESENCE OF START SS LEVEL OR ANY OF THE TAPE READER CHARACTER COUNTER BITS. IT GUARANTEES A FULL COMPLIMENT OF TAPE CHARACTERS, AND ALLOWS CLOCK PULSES 3 AND 4 WHILE IN THE MANUAL MODE.
LACH 1 THRU 6	LATCH 1 THROUGH 6 OUTPUT. MANUAL TAPE READER READ - OUT CONTROL LATCH.
LACH 7 NOT	INVERSE LATCH 7.
LACH 7	LATCH 7 - CONTROLS MANUAL SELECTION OF TAPE READER REGISTER.
LAI3	LOAD, 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION CHANNEL OF THE 31 MICROSECOND DELAY LINE.
LAMP TEST 1-6	LAMP TEST, LINES 1 THROUGH 6.
LAMP TEST INT	LAMP TEST INTERNAL-GROUND LEVEL, PREVENTS LAMP TEST WHILE RUNNING TAPE READER.

SYMBOL	DEFINITION
LARE	LATCH RESET.
LAST	LATCH SET.
LATE IND1	MEMORY CLOCK LATE, INDICATOR DRIVER 1 OUTPUT.
LATE IND2	MEMORY CLOCK LATE, INDICATOR DRIVER 2 OUTPUT.
LC NOT	INVERT LATCH C LEVEL
LC	LATCH C - CONTROL LEVEL FOR NINE POSITION COUNTER LE - LM.
LDIV	LAST DIVIDE.
LD	LATCH D - CONTROL LEVEL PER LATCH C.
LEDCST NOT	INVERSE, LEADING EDGE OF COMPUTER SINGLE - STEP LEVEL.
LEDCST	LEADING EDGE OF COMPUTER SINGLE - STEP LEVEL
LEMMON I	CONTROL LEVEL - ALLOWS SELECTION OF BRA14P OR BRB14P IN SELF CHECK MODE.
LE NOT	ZERO OUTPUT OF LATCH E.
LE	ONE OUTPUT OF LATCH E. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LF NOT	ZERO OUTPUT OF LATCH F.
LF	ONE OUTPUT OF LATCH F. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LG NOT	ZERO OUTPUT OF LATCH G.
LG	ONE OUTPUT OF LATCH G. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LH NOT	ZERO OUTPUT OF LATCH H.

SYMBOL	DEFINITION
LH	ONE OUTPUT OF LATCH H. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LI NOT	ZERO OUTPUT OF LATCH I.
LI	ONE OUTPUT OF LATCH I. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LJ NOT	ZERO OUTPUT OF LATCH J.
LJ	ONE OUTPUT OF LATCH J. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LK NOT	ZERO OUTPUT OF LATCH K.
LK	ONE OUTPUT OF LATCH K. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LL NOT	ZERO OUTPUT OF LATCH L.
LL	ONE OUTPUT OF LATCH L. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.
LMA	LATCH M (LM) OUTPUT, FROM DRIVE SOURCE A.
LMD	LATCH MD - A BUFFER LATCH IN THE NINE POSITION COUNTER.
LMMH	LATCH OUTPUT, MULTIPLY, MULTIPLY HOLD.
LMNPQR	LOGIC TIE POINT - THE OR OUTPUT COMPARE ERROR LEVEL WHICH CAUSES COMPARE ERROR INSTRUCTION DISPLAY REGISTER LATCH TO SET.
LM NOT	ZERO OUTPUT OF LATCH M.
LM	ONE OUTPUT OF LATCH M. ONE OF NINE POSITION COUNTER WHOSE OUTPUT IS A GATING LEVEL FOR A CHARACTER COUNTER BIT.

SYMBOL	DEFINITION
LTRS NOT	INVERSE LOAD, TRANSFER REGISTER SERIAL.
LTRS	LOAD, TRANSFER REGISTER SERIAL.
LT	LAMP TEST LEVEL.
MANCH NOT	INVERSE MANUAL CHANNEL LEVEL.
MANCH	MANUAL CHANNEL LEVEL (LATCH OUTPUT).
MANCH SET A	MANUAL CHANNEL SET LEVEL FROM DRIVE SOURCE A.
MAN A	MANUAL MODE LEVEL FROM DRIVE SOURCE A.
MAN B	MANUAL MODE LEVEL FROM DRIVE SOURCE B.
MAN CH ERR GEN	MANUAL CHANNEL ERROR GENERATE LEVEL.
MAN GATE	MANUAL GATE.
MAN IND	MANUAL MODE, INDICATOR DRIVER OUTPUT.
MAN OR RUN NOT	MANUAL MODE LEVEL.
MCL	MEMORY CLOCK LATE.
MCNN	INVERSE MEMORY CLOCK NORMAL
MCN	MEMORY CLOCK NORMAL.
MDANS	MULTIPLY DIVIDE ANSWER.
MDC1-1	MULTIPLY - DIVIDE COUNTER 1, FROM DRIVE SOURCE 1.
MDC1 NOT THROUGH MDC9 NOT	INVERSE MULTIPLY - DIVIDE COUNTER 1 THROUGH 9.
MDC2-1	MULTIPLY - DIVIDE COUNTER 2, FROM DRIVE SOURCE 1.
MDC8-1	MULTIPLY - DIVIDE COUNTER 8, FROM DRIVE SOURCE 1.

SYMBOL	DEFINITION
MDCA NOT, -CB NOT, -CC NOT, -CD NOT, -CE NOT, -CF NOT, -CG N	INVERSE MULTIPLY - DIVIDE COUNTER A, B, C, D, E, F, G AND H LATCH OUTPUTS.
MDCA, -CB, -CC, -CD, -CE AND CF	MULTIPLY - DIVIDE COUNTER A, B, C, D, E AND F LATCH OUTPUTS.
MDCG	MULTIPLY DIVIDE COUNTER G LATCH OUTPUT.
MDCH	MULTIPLY DIVIDE COUNTER H LATCH OUTPUT.
MDCP1 AND MDCP2	MULTIPLY - DIVIDE CLOCK PULSES 1 AND 2.
MDDIS	MULTIPLY - DIVIDE DISPLAY.
MD INH NOT	INVERSE, MULTIPLY - DIVIDE INHIBIT.
MEM SIM IND	MEMORY SIMULATE, INDICATOR DRIVER OUTPUT.
MEM SIM NOT	INVERSE MEMORY SIMULATE MODE LEVEL.
MEM SIM RELAY COIL	MEMORY SIMULATE RELAY COIL (RELAY DRIVER OUT-PUT).
MEM SIM	ONE OUTPUT OF MEMORY SIMULATE LATCH.
MGMR1	MULTIPLY GATE MR1.
MKA	OR INPUT - COMPARE ERROR LEVEL.
ML78 NOT	INVERSE MEMORY LOAD, OUTPUT LEVEL TO SWITCH 78.
ML78	MEMORY LOAD, OUTPUT LEVEL TO SWITCH 78.
MLA NOT	INVERSE MEMORY LOAD, OUTPUT FROM DRIVE SOURCE A.
MLA	MEMORY LOAD LEVEL FROM A DRIVE SOURCE.
MLB4	MEMORY LOAD, OUTPUT FROM GATE B4.

SYMBOL	DEFINITION
ML B5A AND B	MEMORY LOAD, OUTPUT LEVEL FROM GATE B5, DRIVE SOURCES A AND B.
ML B6	MEMORY LOAD INPUT TO GATE B6.
ML IND	MEMORY LOAD MODE, INDICATOR DRIVER OUTPUT.
ML NOTB4	INVERSE MEMORY LOAD, OUTPUT FROM GATE B4.
MMHD NOT	INVERSE MULTIPLY, MULTIPLY HOLD, DIVIDE.
MMHD	MULTIPLY - MULTIPLY HOLD DIVIDE.
MNPQRS	LOGIC TIE POINT - AN OR INPUT COMPARE ERROR LEVEL WHICH CAUSES COMPARE ERROR INSTRUCTION DISPLAY REGISTER LATCH TO SET
MOD1 A GRD IND THROUGH MOD7 A GRD IND	GROUND LEVEL ROUTED BY MODULE SWITCHING RELAYS TO MODULES 1 THROUGH 7, CHANNEL 3, INDICATOR LAMPS
MOD1 B GRD IND THROUGH MOD7 B GRD IND	GROUND LEVEL ROUTED BY MODULE SWITCHING RELAYS TO MODULES 1 THROUGH 7, CHANNEL 1, INDICATOR LAMPS.
MOD1 CH1 IND-12 THROUGH MOD7 CH1 IND-12	MINUS 12 VOLTS ROUTED BY MODULE SWITCHING RELAYS TO MODULES 1 THROUGH 7, CHANNEL 1, INDICATOR LAMPS
MOD1 CH2 IND-12 THROUGH MOD7 CH2 IND-12	MINUS 12 VOLTS ROUTED BY MODULE SWITCHING RELAYS TO MODULES 1 THROUGH 7, CHANNEL 2, INDICATOR LAMPS
MOD1 CH3 IND-12 THROUGH MOD7 CH3 IND-12	MINUS 12 VOLTS ROUTED BY MODULE SWITCHING RELAYS TO MODULES 1 THROUGH 7, CHANNEL 3, INDICATOR LAMPS
MOD1 C GRD IND THROUGH MOD7 C GRD IND	GROUND LEVEL ROUTED BY MODULE SWITCHING RELAYS TO MODULES 1 THROUGH 7, CHANNEL 2, INDICATOR LAMPS.
MOD SEL ERR	MODULE SELECTION ERROR.
MOD SEL IND	GROUND LEVEL APPLIED TO MODULE SELECTION INDICATOR LAMP WHEN CHANNEL OR MODULE SELECTION RELAY IS ENERGIZED

SYMBOL	DEFINITION
MOD SEL	MODULE SELECTION LEVEL.
MPIO RES	MEMORY REGISTER PROCESS INPUT/OUTPUT RESET.
MTA1-3WDA, MTA1-3XDA, MTA1-3YDA AND MTA1-3ZDA	MISSING TRANSLATED CHANNEL A1 THROUGH A3, W,X,Y AND Z CLOCK PULSE DRIVERS TO DATA ADAPTER.
NA1-3DIN	NAND, CHANNELS A1 THROUGH A3, DATA IN.
NA1 NOT THROUGH NA9 NOT	NAND, INVERSE ADDRESS SELECTION BITS 1 THROUGH 9.
NA1 THROUGH NA9	NAND, ADDRESS SELECTION BITS 1 THROUGH 9.
NAI1 NOT	NAND, INVERSE OUTPUT OF 1ST DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION CHANNEL OF 31 MICROSECOND DELAY LINE.
NAI1	NAND, OUTPUT OF 1ST DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION CHANNEL OF 31 MICROSECOND DELAY LINE.
NAI3A	NAND, OUTPUT FROM A DRIVE SOURCE OF THE THIRD DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION COUNTER CHANNEL OF THE 31 MICROSECOND DELAY LINE.
NAI3 B6	NAND OUTPUT OF 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR INSTRUCTION CHANNEL OF THE 31 MICROSECOND DELAY LINE. INPUT TO GATE B6.
NAI3 NOT	NAND, INVERSE OUTPUT OF 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION CHANNEL OF THE 31 MICROSECOND DELAY LINE.
NBG10B NOT	NAND, INVERSE BIT GATE 10, FROM B DRIVE SOURCE.
NBG10 B5	NAND BIT GATE 10, OUTPUT FROM GATE B5.
NBG10 B7	NAND, BIT GATE 10, GATE B7 OUTPUT.
NBG10	NAND BIT GATE 10 LEVEL.

SYMBOL	DEFINITION
NBG11B NOT	NAND, INVERSE BIT GATE 11, FROM B DRIVE SOURCE.
NBG11 B4	NAND, BIT GATE 11, OUTPUT FROM GATE B4.
NBG11 B5	NAND, BIT GATE 11, OUTPUT FROM GATE B5.
NBG11 B7	NAND, BIT GATE 11, GATE B7 OUTPUT
NBG12B NOT	NAND, INVERSE BIT GATE 12, FROM B DRIVE SOURCE.
NBG12 B5	NAND, BIT GATE 12, OUTPUT FROM GATE B5.
NBG12 B7	NAND, BIT GATE 12, GATE B7 OUTPUT.
NBG13B NOT	NAND, INVERSE BIT GATE 13, FROM B DRIVE SOURCE.
NBG13 B4	NAND BIT GATE 13, OUTPUT FROM GATE B4.
NBG13 B5	NAND, BIT GATE 13, OUTPUT FROM GATE B5.
NBG13	NAND, BIT GATE 13.
NBG14B NOT	INVERSE, NAND, BIT GATE 14 FROM DRIVE SOURCE B.
NBG1=B1	NAND, BIT GATE 1, INPUT TO GATE B1.
NBG1A NOT THROUGH NBG14A NOT	NAND, INVERSE BIT GATE 1 THROUGH 14, FROM A DRIVE SOURCES.
NBG1C	NAND, BIT GATE 1 FROM DRIVE SOURCE C.
NBG1 B3 THROUGH NBG14 B3	NAND BIT GATE 1 THROUGH BIT GATE 14, OUTPUT OF GATE 02, B3 TIMING DRIVERS.
NBG1 B4 THROUGH NBG14 B4	NAND, BIT GATE 1 THOUGH NAND, BIT GATE 14, OUTPUTS FROM GATE B4.
NBG1 B5	NAND, BIT GATE 1, OUTPUT FROM GATE B5.

SYMBOL	DEFINITION
NBG1 B6 THROUGH NBG14 B6	NAND, BIT GATE 1 THROUGH 14 INPUTS TO GATE B6.
NBG1 B7	NAND, BIT GATE 1, OUTPUT FROM GATE B7.
NBG1 THROUGH 14	NAND, BIT GATE 1 THROUGH 14.
NBG2=B1	NAND, BIT GATE 2, INPUT TO GATE B1.
NBG2B4 AND NBG5B4	NAND, BIT GATES 2 AND 5 OUTPUTS OF GATE B4.
NBG2B NOT	NAND, INVERSE BIT GATE 2, FROM B DRIVE SOURCE.
NBG2C NOT, -3CNOT, -4CNOT, -6C NOT, -8CNOT, -9CNOT AND -13CNO	NAND, INVERSE, BIT GATES 2,3,4,6,8,9, AND 13 FROM C DRIVE SO URCE.
NBG2C	NAND, BIT GATE 2 FROM DRIVE SOURCE C.
NBG2 B5	NAND, BIT GATE 2, OUTPUT FROM GATE B5.
NBG2 B7	NAND, BIT GATE 2, OUTPUT FROM GATE B7.
NBG3B NOT	NAND, INVERSE BIT GATE 3, FROM B DRIVE SOURCE.
NBG3 B4	NAND, BIT GATE 3, OUTPUT FROM GATE B4.
NBG3 B5	NAND, BIT GATE 3, OUTPUT FROM GATE B5.
NBG3 B7	NAND, BIT GATE 3, GATE B7 OUTPUT.
NBG4B NOT	NAND, INVERSE BIT GATE 4, FROM B DRIVE SOURCE.
NBG4C	NAND, BIT GATE 4 FROM DRIVE SOURCE C.
NBG4 B5	NAND, BIT GATE 4, OUTPUT FROM GATE B5.
NBG4 B7	NAND, BIT GATE 4, GATE B7 OUTPUT.
NBG5B NOT	NAND, INVERSE BIT GATE 5, FROM B DRIVE SOURCE.

SYMBOL	DEFINITION
NBG5C NOT	INVERSE, NAND, BIT GATE 5 FROM DRIVE SOURCE C.
NBG5C	NAND, BIT GATE 5 FROM DRIVE SOURCE C.
NBG5 B5	NAND, BIT GATE 5, OUTPUT FROM GATE B5.
NBG5 B7	NAND, BIT GATE 5, GATE B7 OUTPUT.
NBG6B NOT	NAND, INVERSE BIT GATE 6, FROM B DRIVE SOURCE.
NBG6 B5	NAND, BIT GATE 6, OUTPUT FROM GATE B5.
NBG7B NOT	INVERSE, NAND, BIT GATE 7, FROM B DRIVE SOURCE.
NBG7 B7	NAND, BIT GATE 7, GATE B7 OUTPUT.
NBG8B NOT	NAND, INVERSE BIT GATE 8, FROM B DRIVE SOURCE.
NBG8 B7	NAND, BIT GATE 8, GATE B7 OUTPUT.
NBG9B NOT	INVERSE, NAND, BIT GATE 9, FROM B DRIVE SOURCE.
NBG9 B4	NAND, BIT GATE 9, OUTPUT FROM GATE B4.
NBG9 B7	NAND, BIT GATE 9, GATE B7 OUTPUT.
NBG1B NOT	NAND, INVERSE BIT GATE 1, FROM B DRIVE SOURCE.
NBG1C NOT	INVERSE, NAND, BIT GATE 1 FROM DRIVE SOURCE C.
NCPFE NOT	NAND, INVERSE CLOCK PULSE X FROM F DRIVE SOURCE.
NCPW1 NOT	NAND, INVERSE CLOCK PULSE W FROM DRIVE SOURCE 1.
NCPW2 NOT	NAND, INVERTED CLOCK PULSE W FROM DRIVE SOURCE 2.
NCPWB NOT	NAND, INVERSE CLOCK PULSE W, FROM B DRIVE SOURCE.
NCPWC NOT	NAND, INVERSE CLOCK PULSE W FROM C DRIVE SOURCE.

SYMBOL	DEFINITION
NCPWD NOT	NAND, INVERSE W CLOCK PULSE DELAYED.
NCPWE1	NAND, CLOCK PULSE W, FROM DRIVE SOURCES E, 1.
NCPWE2	NAND, CLOCK PULSE W, FROM DRIVE SOURCES E, 2.
NCPWE NOT	NAND, INVERSE CLOCK PULSE W FROM E DRIVE SOURCE.
NCPWF1	NAND, CLOCK PULSE W FROM DRIVE SOURCES F, 1.
NCPWF NOT	NAND, INVERSE CLOCK PULSE W FROM F DRIVE SOURCE.
NCPWG	NAND, CLOCK PULSE W FROM G DRIVE SOURCE.
NCPWH	NAND, CLOCK PULSE W FROM H DRIVE SOURCE.
NCPW B3	NAND, CLOCK PULSE W, OUTPUT OF GATE 02, B3 TIMING DRIVER.
NCPW B4	NAND, CLOCK PULSE W, OUTPUT FROM GATE B4.
NCPW B4, -XB4, -YB4 AND -ZB4 -	NAND CLOCK PULSES W,X,Y AND Z, OUTPUTS FROM GATE B4.
NCPW B6	NAND, CLOCK PULSE W INPUT TO GATE B6.
NCPW F2	NAND, CLOCK PULSE W, FROM DRIVE SOURCES F, 2.
NCPW,X,YAND Z	NAND, CLOCK PULSES W, X, Y AND Z.
NCPX1 NOT	NAND INVERTED CLOCK PULSE X FROM DRIVE SOURCE 1.
NCPX2 NOT	NAND INVERTED CLOCK PULSE X FROM DRIVE SOURCE 2.
NCPXB NOT	NAND, INVERSE CLOCK PULSE X, FROM B DRIVE SOURCE.
NCPXC NOT	NAND, INVERSE CLOCK PULSE X FROM C DRIVE SOURCE.
NCPXD NOT	NAND, INVERSE X CLOCK PULSE DELAYED.

SYMBOL	DEFINITION
NCPXE NOT	NAND, INVERSE CLOCK PULSE X FROM E DRIVE SOURCE.
NCPXE	NAND, CLOCK PULSE X, FROM DRIVE SOURCE E.
NCPXF	NAND, CLOCK PULSE X FROM DRIVE SOURCE F.
NCPXG	NAND, CLOCK PULSE X FROM G DRIVE SOURCE.
NCPXH	NAND, CLOCK PULSE X FROM H DRIVE SOURCE.
NCPX B3	NAND, CLOCK PULSE X, OUTPUT OF GATE 02, B3 TIMING DRIVER.
NCPX B6	NAND CLOCK PULSE X INPUT TO GATE B6.
NCPY1 NOT	NAND, INVERTED CLOCK PULSE Y FROM DRIVE SOURCE 1.
NCPY2 NOT	NAND INVERTED CLOCK PULSE Y FROM DRIVE SOURCE 2.
NCPYB NOT	NAND, INVERSE CLOCK PULSE Y, FROM B DRIVE SOURCE.
NCPYC NOT	NAND, INVERSE CLOCK PULSE Y FROM C DRIVE SOURCE.
NCPYD NOT	NAND, INVERSE Y CLOCK PULSE DELAYED.
NCPYE1	NAND, CLOCK PULSE Y, FROM DRIVE SOURCES E, 1.
NCPYE2	NAND, CLOCK PULSE Y, FROM DRIVE SOURCES E, 2.
NCPYE NOT	NAND, INVERSE CLOCK PULSE Y FROM E DRIVE SOURCE.
NCPYF1	NAND, CLOCK PULSE Y FROM DRIVE SOURCES F, 1.
NCPYF2	NAND, CLOCK PULSE Y FROM DRIVE SOURCES F, 2.
NCPYF NOT	NAND, INVERSE CLOCK PULSE Y FROM F DRIVE SOURCE.
NCPYF	NAND, CLOCK PULSE Y FROM DRIVE SOURCE F.
NCPYG	NAND, CLOCK PULSE Y FROM G DRIVE SOURCE.

SYMBOL	DEFINITION
NCPY B3	NAND, CLOCK PULSE Y, OUTPUT OF GATE 02, B3 TIMING DRIVER.
NCPY B4A	NAND, CLOCK PULSE Y, OUTPUT FROM GATE B4, DRIVE SOURCE A.
NCPY B4	NAND, CLOCK PULSE Y, OUTPUT FROM GATE B4.
NCPY B6	NAND CLOCK PULSE Y INPUT TO GATE B6.
NCPZ1 NOT	NAND, INVERTED CLOCK PULSE Z FROM DRIVE SOURCE 1.
NCPZ2 NOT	NAND, INVERTED CLOCK PULSE Z FROM DRIVE SOURCE 2.
NCPZB NOT	NAND, INVERSE CLOCK PULSE Z, FROM B DRIVE SOURCE.
NCPZC NOT	NAND, INVERSE CLOCK PULSE Z FROM C DRIVE SOURCE.
NCPZD NOT	NAND, INVERSE Z CLOCK PULSE DELAYED.
NCPZE1	NAND, CLOCK PULSE Z, FROM DRIVE SOURCES E, 1.
NCPZE2	NAND, CLOCK PULSE Z, FROM DRIVE SOURCES E, 2.
NCPZE NOT	NAND, INVERSE CLOCK PULSE Z FROM E DRIVE SOURCE.
NCPZF NOT	NAND, INVERSE CLOCK PULSE Z FROM F DRIVE SOURCE.
NCPZF	NAND, CLOCK PULSE Z FROM DRIVE SOURCE F.
NCPZ B3	NAND, CLOCK PULSE Z, OUTPUT OF GATE 02, B3 TIMING DRIVER.
NCPZ B4	NAND, CLOCK PULSE Z, OUTPUT FROM GATE B4.
NCPZ B6	NAND CLOCK PULSE Z INPUT TO GATE B 6.
NCST1 NOT	NAND, INVERSE COMPUTER SINGLE - STEP LEVEL FROM DRIVE SOURCE 1.
NCST1	NAND, COMPUTER SINGLE - STEP LEVEL FROM DRIVE SOURCE 1

SYMBOL	DEFINITION
NCST NOT	NAND, INVERSE COMPUTER SINGLE STEP CONTROL.
NCST	NAND, COMPUTER SINGLE - STEP.
NDIV NOT	NAND, INVERSE DIVIDE LATCH OUTPUT.
NDIV	NAND, DIVIDE LATCH OUTPUT.
NDLP	NO DELAY LINE PROCESSION.
NEAM IND	NAND, ERROR IN EVEN MEMORIES, INDICATOR DRIVER OUTPUT.
NEAM	NAND, ERROR IN EVEN MEMORIES LEVEL.
NEBM IND	NAND, ERROR IN (B) ODD MEMORIES, INDICATOR DRIVER OUTPUT.
NEBM	NAND, ERROR IN ODD MEMORIES LEVEL.
NEP13 IND1	NAND, ERROR PULSE 13, INDICATOR DRIVER 1 OUTPUT.
NEP13 IND2	NAND ERROR PULSE 13, INDICATOR DRIVER 2 OUTPUT.
NEP15 IND	NAND, ERROR PULSE 15, INDICATOR DRIVER OUTPUT.
NEP15	NAND, ERROR PULSE 15. (GENERATED ON LOGIC PAGE 15).
NEP2 IND THROUGH NEP13 IND	NAND, ERROR PULSE 2 THROUGH 13, INDICATOR DRIVER OUTPUTS.
NEP2 THROUGH NEP13	NAND, ERROR PULSE 2 THROUGH 13. (GENERATED ON LOGIC PAGES 2 THROUGH 13)
NERR RES1-3	NAND, ERROR RESET, LINES 1 THROUGH 3.
NERR TEST 1-3	NAND, ERROR TEST, LINES 1 THROUGH 3.
NG5 NOT	NAND, INVERSE OUTPUT OF BIT GATE GENERATOR LATCH 5.
NG5	NAND, ONE OUTPUT OF BIT GATE GENERATOR LATCH 5.

SYMBOL	DEFINITION
NHLT NOT	NAND, INVERSE HALT.
NHLT	NAND, HALT LEVEL.
NHOPC1 NOT	NAND, INVERSE HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION, LATCH OUTPUT.
NHOPC1	NAND, LATCH OUTPUT WHICH GENERATES THE HOP CONSTANT FOR STORAGE DURING AN INTERRUPT OPERATION.
NMCNN	INVERSE, MEMORY CLOCK NOMINAL, NAND.
NMD7 B6	NAND, LATCH 7 OUTPUT OF MULTIPLICAND - DIVISOR REGISTER - INPUT TO GATE B6.
NMD7 NOT B6	NAND, INVERSE LATCH 7 OUTPUT OF MULTIPLICAND - DIVISOR REGISTER - INPUT TO GATE B6.
NMD7 NOT	NAND, INVERSE LATCH 7 OUTPUT OF MULTIPLICAND - DIVISOR REGISTER.
NMD7	NAND, LATCH 7 OUTPUT OF MULTIPLIPLICAND - DIVISOR REGISTER
NMMH NOT	NAND, INVERSE MULTIPLY, MULTIPLY HOLD LATCH OUTPUT.
NMMH	NAND, MULTIPLY, MULTIPLY HOLD LATCH OUTPUT.
NMR1 NOT	NAND, ZERO LATCH OUTPUT IN THE MULTIPLIER - QUOTIENT, PRODUCT QUOTIENT REGISTER CONDITIONED BY THE OUTPUT OF THE ACCUMULATOR DURING THE INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE.
NMR1	NAND, OUTPUT OF LATCH IN MULTIPLIER, QUOTIENT, PRODUCT - QUOTIENT REGISTER CONDITIONED BY THE OUTPUT OF THE ACCUMULATOR DURING THE INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE.
NOP1 NOT THROUGH NOP4 NOT	INVERSE, NAND, OPERATION CODE BITS 1 THROUGH 4.

SYMBOL	DEFINITION
NOP1 THROUGH NOP4	NAND, OPERATION CODE BITS 1 THROUGH 4
NORMAL IND1	MEMORY CLOCK NORMAL, INDICATOR DRIVER 1 OUTPUT.
NORMAL IND2	MEMORY CLOCK NORMAL, INDICATOR DRIVER 2 OUTPUT.
NPB NOT	NAND, INVERSE PHASE B.
NPB	NAND, PHASE B, VOTED OUTPUT OF COMPUTER.
NPHAA NOT	NAND, INVERSE PHASE A, FROM DRIVE SOURCE A.
NPHAB NOT	NAND, INVERSE PHASE A, FROM B DRIVE SOURCE.
NPHAC NOT,NPHBC NOT ANDNPHCC NOT	NAND, INVERSE, PHASE A, B AND C FROM C DRIVE SOURCE.
NPHAC	NAND, PHASE A FROM C DRIVE SOURCE.
NPHA B3	NAND, PHASE A, OUTPUT OF GATE 02, B3 TIMING DRIVER.
NPHA B4A	NAND, PHASE A, OUTPUT OF GATE B4 DRIVE SOURCE A.
NPHA B4, -BB4 AND -CB4	NAND PHASES A, B AND C OUTPUTS FROM GATE B4.
NPHA B5	NAND, PHASE A, OUTPUT FROM GATE B5.
NPHA B6A AND B	NAND, PHASE A INPUT TO GATE B6 FROM A AND B DRIVE SOURCES.
NPHA B7	NAND, PHASE A, GATE B7 OUTPUT.
NPHBA NOT	NAND, INVERSE PHASE B, FROM DRIVE SOURCE A.
NPHBB NOT	NAND, INVERSE PHASE B, FROM B DRIVE SOURCE.
NPHBC	NAND, PHASE B FROM DRIVE SOURCE C.
NPHB B3	NAND, PHASE B, OUTPUT OF GATE 02, B3 TIMING DRIVER.

SYMBOL	DEFINITION
NPHB B4A	NAND, PHASE B, OUTPUT OF GATE B4 DRIVE SOURCE A.
NPHB B4	NAND, PHASE B OUTPUT OF GATE B4.
NPHB B5	NAND PHASE B, OUTPUT FROM GATE B5.
NPHB B6A AND B	NAND, PHASE B INPUT TO GATE B6 FROM A AND B DRIVE SOURCES.
NPHB B7	NAND, PHASE B, GATE B7 OUTPUT.
NPHCA NOT	NAND, INVERSE PHASE C, FROM DRIVE SOURCE A.
NPHCB NOT	INVERSE, NAND, PHASE C, FROM B DRIVE SOURCE.
NPHC AND NBG11	NAND, PHASE C AND NAND, BIT GATE 11.
NPHC B3	NAND, PHASE C, OUTPUT OF GATE 02, B3 TIMING DRIVER.
NPHC B4A	NAND, PHASE C, OUTPUT OF GATE B4 DRIVE SOURCE A
NPHC B5	NAND, PHASE C, OUTPUT FROM GATE B5.
NPHC B6	NAND, PHASE C INPUT TO GATE B6.
NPHC B7	NAND, PHASE C, GATE B7 OUTPUT.
NPIO	NAND, DECODED PROCESS INPUT/OUTPUT OPERATION.
NPQRST	LOGIC TIE POINT - COMPARE ERROR LEVEL WHICH CAUSES THE COMPARE ERROR BUFFER REGISTER 14 LATCH TO BE SET AT CYCLE 4 AND NAND BIT GATE 6 TIME.
NPRO B6	NAND, OUTPUT OF LATCH CONTAINING THE OLD PARTIAL PRODUCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAINDER DURING DIVIDE. INPUT TO GATE B6.
NPRO NOT	NAND, INVERSE OLD PARTIAL PRODUCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAINDER DURING DIVIDE, LATCH

SYMBOL	DEFINITION
	OUTPUT.
NPRO	NAND, OUTPUT OF LATCH CONTAINING THE OLD PARTIAL PRODUCT DUR ING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAINDE R DURING DIVIDE.
NSCA1BO NOT	INVERSE, NAND, SELF CHECK, CHANNEL A1, BUFFER OSCILLATOR.
NSCA1EAM	NAND, SELF CHECK, CHANNEL A1, ERROR IN (A) EVEN MEMORIES.
NSCA1EBM	NAND, SELF CHECK, CHANNEL A1, ERROR IN (B) ODD MEMORIES.
NSCA1G5 NOT	NAND, INVERSE, SELF CHECK, CHANNEL A1, BIT GATE GENERATOR 5.
NSCA1-3A1-9	NAND, SELF CHECK CHANNELS A1 THROUGH A3, ADDRESS BITS 1 THRO UGH 9.
NSCA1-3OP1-4	NAND, SELF CHECK CHANNELS A1 THROUGH A3, OPERATION CODE BITS 1 THROUGH 4.
NSCA1PB NOT	NAND, INVERSE SELF CHECK, CHANNEL A2, PHASE B.
NSCA1TLC	NAND, SELF CHECK, CHANNEL A1, TWO SIMULTANEOUS MEMORY ERRORS (AN ABORT CONDITION).
NSCA1TRS	NAND, SELF CHECK, CHANNEL A1, TRANSFER REGISTER SERIAL
NSCA1WDA	NAND, SELF CHECK, CHANNEL A1, W CLOCK PULSE DRIVER TO DATA A DAPTER
NSCA1XDA	NAND, SELF CHECK, CHANNEL A1, X CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA1YDA	NAND, SELF CHECK, CHANNEL A1, Y CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA1ZDA	NAND, SELF CHECK, CHANNEL A1, Z CLOCK PULSE DRIVER TO DATA A DAPTER.

SYMBOL	DEFINITION
NSCA2AI3	NAND, SELF CHECK, CHANNEL A2, AI3 LEVEL.
NSCA2BO NOT	INVERSE, NAND, SELF CHECK, CHANNEL A2, BUFFER OSCILLATOR.
NSCA2EAM	NAND, SELF CHECK, CHANNEL A2, ERROR IN (A) EVEN MEMORIES.
NSCA2EBM	NAND, SELF CHECK, CHANNEL A2, ERROR IN (B) ODD MEMORIES.
NSCA2G5 NOT	NAND, INVERSE SELF CHECK, CHANNEL A2, BIT GATE GENERATOR 5.
NSCA2PB NOT	NAND, INVERSE SELF CHECK, CHANNEL A2, PHASE B.
NSCA2TLC	NAND, SELF CHECK, CHANNEL A2, TWO SIMULTANEOUS MEMORY ERRORS (AN ABORT CONDITION).
NSCA2TRS	NAND, SELF CHECK, CHANNEL A2, TRANSFER REGISTER SERIAL.
NSCA2WDA	NAND, SELF CHECK, CHANNEL A2, W CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA2XDA	NAND, SELF CHECK, CHANNEL A2, X CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA2YDA	NAND, SELF CHECK, CHANNEL A2, Y CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA2ZDA	NAND, SELF CHECK, CHANNEL A2, Z CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA3AI3	NAND, SELF CHECK, CHANNEL A3, AI3 LEVEL.
NSCA3BO NOT	INVERSE, NAND, SELF CHECK, CHANNEL A3, BUFFER OSCILLATOR.
NSCA3EAM	NAND, SELF CHECK, CHANNEL A3, ERROR IN (A) EVEN MEMORIES.
NSCA3EBM	NAND, SELF CHECK, CHANNEL A3, ERROR IN (B) ODD MEMORIES.
NSCA3G5 NOT	NAND, SELF CHECK, CHANNEL A3, BIT GATE GENERATOR 5.

SYMBOL	DEFINITION
NSCA3PB NOT	NAND, INVERSE SELF CHECK, CHANNEL A3, PHASE B.
NSCA3TLC	NAND, SELF CHECK, CHANNEL A3, TWO SIMULTANEOUS MEMORY ERRORS (AN ABORT CONDITION).
NSCA3TRS	NAND, SELF CHECK, CHANNEL A3, TRANSFER REGISTER SERIAL.
NSCA3WDA	NAND, SELF CHECK, CHANNEL A3, W CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA3XDA	NAND, SELF CHECK, CHANNEL A3, X CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA3YDA	NAND, SELF CHECK, CHANNEL A3, Y CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCA3ZDA	NAND, SELF CHECK, CHANNEL A3, Z CLOCK PULSE DRIVER TO DATA A DAPTER.
NSCBRA14P	NAND, SELF CHECK, BUFFER REGISTER A, BIT 14. (SPECIAL PARITY BIT).
NSCBRB14P	NAND, SELF CHECK, BUFFER REGISTER B, BIT 14. (SPECIAL PARITY BIT).
NSP1 NOT	NAND, INVERSE SPARE PROBE 1.
NSP2 NOT	NAND, INVERSE SPARE PROBE 2.
NSTO NOT	NAND, INVERSE STORE INSTRUCTION.
NTLC IND	NAND, TWO SIMULTANEOUS MEMORY ERRORS, INDICATOR DRIVER OUTPUT.
NTLC	NAND, TWO SIMULTANEOUS MEMORY ERRORS LEVEL.
NTRS B6	NAND, OUTPUT OF TRANSFER REGISTER SERIAL LATCH. INPUT TO GATE B6.

SYMBOL	DEFINITION
NTRS NOT	NAND, INVERSE TRANSFER REGISTER SERIAL LATCH OUTPUT.
NTRS	NAND, TRANSFER REGISTER SERIAL LATCH OUTPUT
NUT	SAMPLE ERROR GATE FOR THE CEPIOA LATCH.
OAC NOT	INVERSE OPERAND ADDRESS COMPARE.
OAC	OPERAND ADDRESS COMPARE.
ODD	ODD, DATA TRANSFER CONTROL LEVEL
OLIVE	ERROR SIGNAL ASSOCIATED WITH DATA TRANSFER DURING MEMORY LOAD PREVENTS SPARE PROBE TURN ON OF DISPLAY SHIFT REGISTER.
ONE NOT OR FOUR NOT	TAPE READER OPERATION CODE BIT 1 AND TAPE READER OPERATION CODE BIT 4 DECODED.
ONE NOT OR TWO NOT	TAPE READER OPERATION CODE BIT 1 AND TAPE READER OPERATION CODE BIT 2 DECODED.
OPA1	OPERATION CODE, CHANNEL A1 CONTROL.
OPA2	OPERATION CODE, CHANNEL A2 CONTROL.
OPA3	OPERATION CODE, CHANNEL A3 CONTROL.
OPC	OPERATION CODE COMPARE.
OPER R	OPERATE ADDRESS SERIALIZER PARITY BIT LATCH.
OPER (R)	OPERATE POWER --- A ONE LEVEL WHEN POWER IS UP.
OPER(R) NOT	INVERSE OPERATE POWER.
OVERRIDE IND1	OVER RIDE ERROR, INDICATOR DRIVER 1.
OVERRIDE IND2	OVERRIDE ERROR, INDICATOR DRIVER 2.

SYMBOL	DEFINITION
PAST IND	PAST, INDICATOR DRIVER OUTPUT.
PHASE OUT NOT	INVERTED PHASE OUT - SYNC LEVEL FOR SPARE PROBE ON - OFF.
PHASE OUT	PHASE OUT - SYNC LEVEL FOR SPARE PROBE ON - OFF.
PHB BG6 CPX	PHASE B AND BIT GATE 6 AND CLOCK PULSE X.
PHG	PAST HISTORY GATE.
PHI NOT	INVERSE PAST HISTORY INHIBIT LEVEL.
PHM=A=NOT	INVERSE, PAST HISTORY MODE, FROM A DRIVE SOURCE.
PHMDC=EV	PAST HISTORY MULTIPLY - DIVIDE COUNTER EVEN.
PHMDC=INH=NOT	INVERSE PAST HISTORY MULTIPLY - DIVIDE COUNTER INHIBIT.
PHMDCA NOT	INVERSE A OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCA	A OUTPUT OF THE PAST HISTORY, MULTIPLY - DIVIDE COUNTER .
PHMDCC NOT	INVERSE, C OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCC	C OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCD NOT	INVERSE, D OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCD	D OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCE NOT	INVERSE, E OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCE	E OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDCF NOT	INVERSE F OUTPUT OF THE PAST HISTORY MULTIPLY DIVIDE COUNTER

SYMBOL	DEFINITION
PHMDCF	F OUTPUT OF THE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDC NOT	INVERSE PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMDC	PAST HISTORY MULTIPLY - DIVIDE COUNTER.
PHMMHD	PAST HISTORY, MULTIPLY - MULTIPLY HOLD DIVIDE.
PHM NOT	INVERSE PAST HISTORY MODE.
PHM	PAST HISTORY MODE
PHS SYNC ERR NOT	INVERSE PHASE SYNC ERROR.
PIO1 THROUGH PIO3	PROCESS INPUT - OUTPUT LEVEL FROM DRIVE SOURCES 1 THROUGH 3.
PIO AB13D NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR BIT 13 DELAYED.
PIO AB13D	PROCESS INPUT/OUTPUT ACCUMULATOR BIT 13 DELAYED.
PIO AB18 NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR REGISTER BIT 18.
PIO AB1 IND. THROUGH PIO AB25 IND	PROCESS INPUT OUTPUT ACCUMULATOR REGISTER BIT 1 THROUGH BIT 25, INDICATOR DRIVER OUTPUT.
PIO AB1 THROUGH B25	PROCESS INPUT/OUTPUT ACCUMULATOR REGISTER BIT 1 THROUGH BIT 25.
PIO AB22D NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR BIT 22 DELAYED.
PIO AB22D	PROCESS INPUT/OUTPUT ACCUMULATOR BIT 22 DELAYED.
PIO AB25D NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR BIT 25 DELAYED.
PIO AB25D	PROCESS INPUT/OUTPUT ACCUMULATOR BIT 25 DELAYED.
PIO AB4D NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR BIT 4 DELAYED.

SYMBOL	DEFINITION
PIO AB4D	PROCESS INPUT/OUTPUT ACCUMULATOR BIT 4 DELAYED.
PIO AB9 NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR REGISTER BIT 9.
PIO ABD	PROCESS INPUT/OUTPUT ACCUMULATOR BITS DELAYED.
PIO A SIGN IND	PROCESS INPUT/OUTPUT ACCUMULATOR REGISTER SIGN BIT, INDICATO R DRIVER OUTPUT.
PIO A SIGN NOT	INVERSE PROCESS INPUT/OUTPUT ACCUMULATOR REGISTER SIGN BIT L EVEL.
PIO A SIGN	PROCESS INPUT/OUTPUT ACCUMULATOR SIGN BIT LEVEL.
PIO MB13D NOT	INVERSE PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 13 DELAYED.
PIO MB13D	PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 13 DELAYED.
PIO MB1A	PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 1 FROM A DRIVE SOUR CE.
PIO MB1 IND THROUGH PIO MB25 I ND	PROCESS INPUT OUTPUT MEMORY REGISTER BIT 1 THROUGH BIT 25, I NDICATOR DRIVER OUTPUT.
PIO MB1 NOT THROUGH B25 NOT	INVERSE PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 1 THROUGH B IT 1 THROUGH BIT 25.
PIO MB1 THROUGH B25	PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 1 THROUGH BIT 25.
PIO MB22D NOT	INVERSE PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 22 DELAYED.
PIO MB22D	PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 22 DELAYED.
PIO MB25D NOT	INVERSE PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 25 DELAYED.
PIO MB25D	PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 25 DELAYED.
PIO MB4D NOT	INVERSE PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 4 DELAYED.

SYMBOL	DEFINITION
PIO MB4D	PROCESS INPUT/OUTPUT MEMORY REGISTER BIT 4 DELAYED.
PIO MBD	PROCESS INPUT/OUTPUT MEMORY REGISTER BITS DELAYED.
PIO M SIGNA	PROCESS INPUT/OUTPUT MEMORY REGISTER SIGN BIT FROM A DRIVE SOURCE.
PIO M SIGN IND	PROCESS INPUT/OUTPUT MEMORY REGISTER SIGN BIT, INDICATOR DRIVER OUTPUT.
PIO M SIGN NOT	INVERSE PROCESS INPUT/OUTPUT MEMORY REGISTER SIGN BIT.
PIO M SIGN	PROCESS INPUT/OUTPUT MEMORY REGISTER SIGN BIT.
PIO RES NOT	INVERSE PROCESS INPUT/OUTPUT RESET.
PLUS 6 SP1	ACME PLUS 6 VOLTS TO SPARE PROBE 1.
PLUS 6 SP2	ACME PLUS 6 VOLTS TO SPARE PROBE 2.
PODC	CONTROL GATE DURING CORRECT HISTORY WORD WHICH ALLOWS SPARE PROBE TURN ON OF DISPLAY SHIFT REGISTER.
PPQ1 THROUGH PPQ12	PARTIAL PRODUCT - QUOTIENT 1 THROUGH 12.
PRESENT IND	PRESENT, INDICATOR DRIVER OUTPUT.
PSE IND	PHASE SYNC ERROR, INDICATOR DRIVER OUTPUT.
PTGWD	PULSE TO GENERATE W DELAYED CLOCK
PTGW	PULSE TO GENERATE W CLOCK.
PTGXD	PULSE TO GENERATE X DELAYED CLOCK.
PTGX	PULSE TO GENERATE X CLOCK.
PTGYD	PULSE TO GENERATE Y DELAYED CLOCK

SYMBOL	DEFINITION
PTGY	PULSE TO GENERATE Y CLOCK
PTGZD	PULSE TO GENERATE Z DELAYED CLOCK.
PTGZ	PULSE TO GENERATE Z CLOCK
PWR HLT	POWER HALT.
QQ NOT	INVERSE LEVEL - (LOGIC FUNCTION - ACCUMULATOR DISPLAY REGENERATION GATE AND INVERSE PAST HISTORY INHIBIT).
RAY NOT	INVERSE LATCH OUTPUT, CONTROL LEVEL FOR SIMULATING HOP CONSTANT DURING SELF CHECK.
RDL1	READ DELAY LINE 1.
RDL2	READ DELAY LINE 2.
RDL3	READ DELAY LINE 3.
REGGATE	ACCUMULATOR DISPLAY REGENERATION GATE.
RESET=MDCTR=2	RESET MULTIPLY - DIVIDE COUNTER 2.
RESET HWC	RESET HISTORY WORD COUNTER.
RESET MDCTR2	RESET MULTIPLY/DIVIDE COUNTER 2.
RESINSDR	RESET INSTRUCTION DISPLAY REGISTER.
RES PB	RESET PARITY BIT.
RES RT NOT	INVERSE RESET DATA AND ADDRESS SERIALIZER PARITY BIT LATCHES.
RES SSMBRA	RESET, SECTOR, SYLLABLE, MODULE, BUFFER REGISTER LEVEL FROM DRIVE SOURCE A.

SYMBOL	DEFINITION
RES SSMBRB	RESET, SECTOR, SYLLABLE, MODULE, BUFFER REGISTER LEVEL FROM DRIVE SOURCE B.
REWIND FWD	REWIND FORWARD.
REWIND REV	REWIND REVERSE.
RMDIS	RESET ON MR1 DURING DIVIDE, CONTROL LEVEL.
R NOT	INVERSE ADDRESS SERIALIZER PARITY BIT LATCH OUTPUT.
R RUN	REVERSE RUN TAPE READER.
R	ADDRESS SERIALIZER PARITY BIT LATCH OUTPUT.
RTROP3 NOT	INVERSE RESET TAPE READER OPERATION BIT 3.
RTROP3	RESET TAPE READER OPERATION BIT 3.
RUN-A, B AND C	AND C DENOTES DRIVE SOURCES. TAPE READER RUN LEVEL. (ONE OUTPUT LEVEL OF A TRATCH. A, B
RUN NOT	INVERSE TAPE READER RUN LEVEL.
RVS A	REVERSE LEVEL FROM A DRIVE SOURCE.
RVS IND	REVERSE, INDICATOR DRIVER OUTPUT.
S0	STEERING LEVEL 0 - CONTROL LEVEL FOR PHASE A GENERATION.
S1	STEERING LEVEL 1 - CONTROL LEVEL FOR PHASE B GENERATION.
S2	STEERING LEVEL 2 - CONTROL LEVEL FOR PHASE C GENERATION.
S78ABX3G	SWITCH 78, DECK A, POLE BX, PIN 3 CONTROL GROUND WHICH ALLOW S SWITCHING AI3 DATA.
S78AXG	SWITCH 78, DECK A, POLE X, CONTROL GROUND WHICH ALLOWS SERIA L REGISTER TRANSFER.

SYMBOL	DEFINITION
S78CXXG	SWITCH 78, DECK C POLE XX, CONTROL GROUND WHICH ALLOWS CERTA IN SWITCH INFORMATION.
SA1DT	SELF - CHECK, CHANNEL A1, DATA LEVEL.
SA1-3CST NOT	SHIELD, INVERSE CHANNEL A1 THROUGH A3 COMPUTER SINGLE - STEP .
SA1-3HLT	SHIELD, CHANNEL A1 THROUGH A3 HALT.
SA1-3TER	SHIELD, CHANNEL A1 THROUGH A3, TIMING ERROR RESET.
SA2DT	SELF - CHECK, CHANNEL A2, DATA LEVEL.
SA3DT	SELF - CHECK, CHANNEL A3, DATA LEVEL.
SALLY	LEVEL CAUSES TAPE POWER RELEASE GROUND IF TAPE DOES NOT STOP WITHIN 50 MILLISECOND.
SAM ERRS	SAMPLE ERRORS LEVEL.
SA 1A	SHIFT ACCUMULATOR PULSE A FROM DRIVE SOURCE 1.
SA 1B	SHIFT ACCUMULATOR PULSE B FROM DRIVE SOURCE 1.
SA 1C	SHIFT ACCUMULATOR PULSE C FROM DRIVE SOURCE 1.
SA 1D	SHIFT ACCUMULATOR PULSE D FROM DRIVE SOURCE 1.
SA 2A	SHIFT ACCUMULATOR PULSE A FROM DRIVE SOURCE 2.
SA 2B	SHIFT ACCUMULATOR PULSE B FROM DRIVE SOURCE 2.
SA 2C	SHIFT ACCUMULATOR PULSE C FROM DRIVE SOURCE 2.
SA 2D	SHIFT ACCUMULATOR PULSE D FROM DRIVE SOURCE 2.
SBI	SWITCH BOUNCE INHIBIT.

SYMBOL	DEFINITION
SCA1A1N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 1
SCA1A2N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 2
SCA1A3N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 3
SCA1A4N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 4
SCA1A5N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 5
SCA1A6N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 6
SCA1A7N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 7
SCA1A8N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 8
SCA1A9N	SELF CHECK, CHANNEL A1, INVERSE ADDRESS - SELECTION BIT 9.
SCA1HOPC1N	SELF CHECK, CHANNEL A1, INVERSE SIMULATED HOP CONSTANT.
SCA1-3A1V-A9V	SELF CHECK, CHANNELS A1 THROUGH A3, ADDRESS REGISTER BITS 1 THROUGH 9, VOTED ON.
SCA1-3 A13V	SELF CHECK, CHANNELS A1 THROUGH A3, ONE OUTPUT FROM THE THIR D DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION CO UNTER CHANNEL OF THE 31 MICRSECOND DELAY LINE, VOTED ON.
SCA1-3 BON	SELF CHECK, CHANNELS A1 THROUGH A3, INVERSE BUFFER OSCILLATO R
SCA1-3 EAMV	SELF CHECK, CHANNELS A1 THROUGH A3, ERROR IN EVEN MEMORIES L EVEL, VOTED ON.
SCA1-3 EBMV	SELF CHECK, CHANNELS A1 THROUGH A3, LATCH INDICATING ERRORS IN ODD MEMORY, VOTED ON.
SCA1-3 G5VN	SELF CHECK, CHANNELS A1 THROUGH A3, INVERSE BIT GATE GENERAT OR LATCH 5, VOTER OUTPUT

SYMBOL	DEFINITION
SCA1-3 HOPC1	SELF CHECK, CHANNELS A1 THROUGH A3, ONE OUTPUT OF LATCH WHIC H GENERATES THE HOP CONSTANT FOR STORAGE DURING AN INTERRUPT OPERATION.
SCA1-3 MD7	SELF CHECK, MODULES A1 THROUGH A3, ONE OUTPUT OF LATCH IN MU LTIPLICAND DIVISOR REGISTER.
SCA1-3 MD7V	SELF CHECK, CHANNELS A1 THROUGH A3, MULTIPLICAND - DIVISOR R EGISTER LATCH, VOTED ON.
SCA1-3 MR1V	SELF CHECK, MODULES A1 THROUGH A3, ONE SIDE OF THE LATCH IN THE MULTIPLIER - QUOTIENT REGISTER CONDITIONED BY THE OUTPUT OF THE ACCUMULATOR DURING THE INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE, VOTED ON.
SCA1-3 OP1V-4V	SELF CHECK, CHANNELS A1 THROUGH A3, ONE OUTPUT OPERATION COD ES 1 THROUGH 4, VOTED ON.
SCA1-3 PBVN	SELF CHECK, CHANNELS A1 THROUGH A3, INVERSE PHASE B, VOTER O UTPUT.
SCA1-3 PIOV	SELF CHECK, CHANNELS A1 THROUGH A3, DECODED PROCESS INPUT - OUTPUT OPERATION, VOTER OUTPUT.
SCA1-3 TLCV	SELF CHECK, CHANNELS A1 THROUGH A3, LATCH INDICATING TWO SIM ULTANEOUS MEMORY ERRORS (AN ABORT CONDITION), VOTED ON.
SCA1-3 TRSV	SELF CHECK, CHANNELS A1 THROUGH A3, TRANSFER REGISTER SERIAL LATCH, VOTED ON.
SCA1-3 WDA	SELF CHECK, CHANNELS A1 THROUGH A3, W CLOCK PULSE DRIVER TO DATA ADAPTER.
SCA1-3 XDA	SELF CHECK, CHANNELS A1 THROUGH A3, X CLOCK PULSE DRIVER TO DATA ADAPTER.
SCA1-3 YDA	SELF CHECK, CHANNELS A1 THROUGH A3, Y CLOCK PULSE DRIVER TO DATA ADAPTER

SYMBOL	DEFINITION
SCA1-3 ZDA	SELF CHECK, CHANNELS A1 THROUGH A3, Z CLOCK PULSE DRIVER TO DATA ADAPTER.
SCA1MR1N	SELF CHECK, CHANNEL A1, INVERSE OUTPUT OF LATCH IN THE MULTIPLIER, QUOTIENT, PRODUCT - QUOTIENT REGISTER CONDITIONED BY OUTPUT OF ACCUMULATOR DURING INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE.
SCA1OP1N	SELF CHECK, CHANNEL A1, INVERSE OPERATION CODE BIT 1.
SCA1OP2N	SELF CHECK, CHANNEL A1, INVERSE OPERATION CODE BIT 2.
SCA1OP3N	SELF CHECK, CHANNEL A1, INVERSE OPERATION CODE BIT 3.
SCA1OP4N	SELF CHECK, CHANNEL A1, INVERSE OPERATION CODE BIT 4.
SCA1PION	SELF CHECK, CHANNEL A1, INVERSE PROCESS INPUT - OUTPUT LEVEL .
SCA1 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 1.
SCA2A1N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 1.
SCA2A2N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 2.
SCA2A3N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 3.
SCA2A4N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 4.
SCA2A5N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 5.
SCA2A6N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 6.
SCA2A7N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 7.
SCA2A8N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 8.
SCA2A9N	SELF CHECK, CHANNEL A2, INVERSE ADDRESS SELECTION BIT 9.

SYMBOL	DEFINITION
SCA2HOPC1N	SELF CHECK, CHANNEL A2, INVERSE SIMULATED HOP CONSTANT.
SCA2MR1N	SELF CHECK, CHANNEL A2, INVERSE OUTPUT OF LATCH IN THE MULTIPLIER, QUTIENT, PRODUCT ← QUOTIENT REGISTER CONDITIONED BY OUTPUT OF ACCUMULATOR DURING INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE.
SCA2OP1N	SELF CHECK, CHANNEL A2, INVERSE OPERATION CODE BIT 1
SCA2OP2N	SELF CHECK, CHANNEL A2, INVERSE OPERATION CODE BIT 2
SCA2OP3N	SELF CHECK, CHANNEL A2, INVERSE OPERATION CODE BIT 3
SCA2OP4N	SELF CHECK, CHANNEL A2, INVERSE OPERATION CODE BIT 4
SCA2PION	SELF CHECK, CHANNEL A2, INVERSE PROCESS INPUT - OUTPUT LEVEL .
SCA2 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 2.
SCA3A1N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 1.
SCA3A2N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 2.
SCA3A3N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 3.
SCA3A4N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 4.
SCA3A5N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 5.
SCA3A6N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 6.
SCA3A7N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 7.
SCA3A8N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 8.
SCA3A9N	SELF CHECK, CHANNEL A3, INVERSE ADDRESS SELECTION BIT 9.

SYMBOL	DEFINITION
SCA3HOPC1N	SELF CHECK, CHANNEL A3, INVERSE SIMULATED HOP CONSTANT.
SCA3MR1N	SELF CHECK, CHANNEL A3, INVERSE OUTPUT OF LATCH IN THE MULTIPLIER, QUOTIENT, PRODUCT - QUOTIENT REGISTER CONDITIONED BY OUTPUT OF ACCUMULATOR DURING INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE.
SCA3OP1N	SELF CHECK, CHANNEL A3, INVERSE OPERATION CODE BIT 1.
SCA3OP2N	SELF CHECK, CHANNEL A3, INVERSE OPERATION CODE BIT 2.
SCA3OP3N	SELF CHECK, CHANNEL A3, INVERSE OPERATION CODE BIT 3.
SCA3OP4N	SELF CHECK, CHANNEL A3, INVERSE OPERATION CODE BIT 4.
SCA3PION	SELF CHECK, CHANNEL A3, INVERSE PROCESS INPUT - OUTPUT LEVEL.
SCA3 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 3.
SCA4 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 4.
SCA5 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 5.
SCA6 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 6.
SCA7 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 7.
SCA8 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 8.
SCA9 NOT	SELF CHECK, INVERSE SIMULATED ADDRESS SELECTION BIT 9.
SCAI3 NOT	INVERSE SELF CHECK LEVEL OF 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR - INSTRUCTION CHANNEL OF THE 31 MICROSECOND DELAY LINE.
SCBG11	SELF CHECK, BIT GATE 11.
SCBG12	SELF CHECK, BIT GATE 12.

SYMBOL	DEFINITION
SCBG13	SELF CHECK, BIT GATE 13.
SCBG14 NOT	INVERSE SELF CHECK, BIT GATE 14.
SCBG3	SELF CHECK, BIT GATE 3.
SCBG4	SELF CHECK, BIT GATE 4.
SCBG6 NOT	INVERSE SELF CHECK, BIT GATE 6.
SCBG7	SELF CHECK, BIT GATE 7.
SCBRA14P	SELF CHECK, BUFFER REGISTER A, BIT 14 (PARITY). SPECIAL MEMORY PARITY BIT FOR TEST EQUIPMENT.
SCBRB14P	SELF CHECK, BUFFER REGISTER B, BIT 14 (PARITY). SPECIAL MEMORY PARITY BIT FOR TEST EQUIPMENT.
SCCYC2 AND 3	SELF CHECK CYCLE 2 AND 3.
SCEP10N	SELF CHECK, INVERSE ERROR PULSE 10
SCEP11N	SELF CHECK, INVERSE ERROR PULSE 11
SCEP12N	SELF CHECK, INVERSE ERROR PULSE 12
SCEP13N	SELF CHECK, INVERSE ERROR PULSE 13
SCEP15	SELF CHECK, ERROR PULSE 15.
SCEP1N	SELF CHECK, INVERSE ERROR PULSE 1
SCEP2-13	SELF CHECK, ERROR PULSES 2 THROUGH 13.
SCEP2N	SELF CHECK, INVERSE ERROR PULSE 2
SCEP3N	SELF CHECK, INVERSE ERROR PULSE 3

SYMBOL	DEFINITION
SCEP4N	SELF CHECK, INVERSE ERROR PULSE 4
SCEP5N	SELF CHECK, INVERSE ERROR PULSE 5
SCEP6N	SELF CHECK, INVERSE ERROR PULSE 6
SCEP7N	SELF CHECK, INVERSE ERROR PULSE 7
SCEP8N	SELF CHECK, INVERSE ERROR PULSE 8
SCEP9N	SELF CHECK, INVERSE ERROR PULSE 9
SCETRS NOT	INVERSE SERIAL COMPARE ERROR TRANSFER REGISTER SERIAL.
SCG1 NOT	SELF CHECK, INVERSE SIMULATED BIT GATE GENERATOR LATCH 1.
SCG1	SELF CHECK, SIMULATED BIT GATE GENERATOR LATCH 1.
SCG2 NOT	SELF CHECK, INVERSE SIMULATED BIT GATE GENERATOR LATCH 2.
SCG3	SELF CHECK, SIMULATED BIT GATE GENERATOR LATCH 3.
SCG4 NOT	SELF CHECK, INVERSE SIMULATED BIT GATE GENERATOR LATCH 4.
SCG4	SELF CHECK, SIMULATED BIT GATE GENERATOR LATCH 4.
SCG5 NOT	SELF CHECK, INVERSE SIMULATED BIT GATE GENERATOR LATCH 5.
SCG5	SELF CHECK, SIMULATED BIT GATE GENERATOR LATCH 5.
SCG6 NOT	SELF CHECK, INVERSE SIMULATED BIT GATE GENERATOR LATCH 6.
SCG6	SELF CHECK, SIMULATED BIT GATE GENERATOR LATCH 6.
SCG7 NOT	SELF CHECK, INVERSE SIMULATED BIT GATE GENERATOR LATCH 7.
SCG7	SELF CHECK, SIMULATED BIT GATE GENERATOR LATCH 7.
SCIA	SELF CHECK, INSTRUCTION ADDRESS CONTROL.

SYMBOL	DEFINITION
SCIEC	SELF CHECK INVERT ERROR CONTROL.
SC-61	ONE OUTPUT OF LATCH SET BY SC6 AND RESET BY SC14.
SCMCL	SELF CHECK, MEMORY CLOCK LATE.
SCMCN	SELF CHECK, MEMORY CLOCK NORMAL.
SCOA	SELF CHECK, OPERAND ADDRESS CONTROL.
SCOP1 NOT	SELF CHECK, SIMULATED INVERSE OPERATION CODE BIT 1.
SCOP2 NOT	SELF CHECK, SIMULATED INVERSE OPERATION CODE BIT 2.
SCOP3 NOT	SELF CHECK, SIMULATED INVERSE OPERATION CODE BIT 3.
SCOP4 NOT	SELF CHECK, SIMULATED INVERSE OPERATION CODE BIT 4.
SCOP 2	SELF CHECK, SIMULATED OPERATION CODE BIT 2.
SCOP 4	SELF CHECK, SIMULATED OPERATION CODE BIT 4.
SCOP	SELF CHECK, OPERATION CODE CONTROL.
SCPA	SELF CHECK PHASE A.
SCPB	SELF CHECK PHASE B.
SCPC	SELF CHECK PHASE C.
SC EVEN	SELF CHECK, EVEN, LATCH OUTPUT.
SC ODD	SELF CHECK, ODD, LATCH OUTPUT.
SCTHERM 1	SELF CHECK, SIMULATED THERMISTER (RESISTOR) CONNECTION POINT (1) TO BRIDGE NETWORK.
SCTHERM 2	SELF CHECK, SIMULATED THERMISTER (RESISTOR) CONNECTION POINT

SYMBOL	DEFINITION
	(2) TO BRIDGE NETWORK.
SCTHERM 2S	A LOGIC POINT, WHICH WHEN SWITCH - SHORTED TO SCTHERM 2 ALLOWS A RESISTOR TO BE PLACED IN PARALLEL WITH A NORMAL TEMPERATURE RESISTOR THEREBY SIMULATING A HIGH TEMPERATURE CONDITION.
SCTHERM 3	SELF CHECK, SIMULATED THERMISTER (RESISTOR) CONNECTION POINT (3) TO BRIDGE NETWORK.
SCTHERM 4	SELF CHECK, SIMULATED THERMISTER (RESISTOR) CONNECTION POINT (4) TO BRIDGE NETWORK.
SCTHERM 4S	A LOGIC POINT, WHICH WHEN SWITCH - SHORTED TO SCTHERM 3 ALLOWS A RESISTOR TO BE PLACED IN PARALLEL WITH A NORMAL TEMPERATURE RESISTOR THEREBY SIMULATING A HIGH TEMPERATURE CONDITION.
SCTO NOT	INVERSE SET COUNTER TO 0 LATCH OUTPUT.
SCTO	SET COUNTER TO 0 LATCH OUTPUT.
SCTRS NOT	INVERSE SHIFT COUNTERS.
SCW NOT	SELF CHECK, INVERSE SIMULATED W CLOCK.
SCW	SELF CHECK, SIMULATED W CLOCK.
SCX NOT	SELF CHECK, INVERSE SIMULATED X CLOCK.
SCY NOT	SELF CHECK, INVERSE SIMULATED Y CLOCK.
SCY	SELF CHECK, SIMULATED Y CLOCK.
SCZ NOT	SELF CHECK, INVERSE SIMULATED Z CLOCK.
SCZ	SELF CHECK, SIMULATED Z CLOCK.
SDT	SELECT DATA

SYMBOL	DEFINITION
SE1 IND	SEQUENCE ERROR 1 INDICATOR.
SE1 NOT	INVERSE SEQUENCE ERROR 1 LEVEL.
SE1	SEQUENCE ERROR 1 LEVEL.
SE2 IND	SEQUENCE ERROR 2 INDICATOR.
SE2 RES INH	SEQUENCE ERROR 2 RESET INHIBIT.
SE2	SEQUENCE ERROR 2 LEVEL.
SECK	SELF CHECK MODE.
SEL=ADR	SELECT ADDRESS.
SEL=CTR	SELECT COUNTER.
SELA1	SELECT CHANNEL A1.
SELA2	SELECT CHANNEL A2.
SELA3	SELECT CHANNEL A3.
SELAI3 DATA	SELECT AI3 DATA.
SELAI3	SELECT 3RD DELAY LATCH AT THE END OF THE ACCUMULATOR INSTRUCTION CHANNEL OF THE 31 MICROSECOND DELAY LINE.
SELHOPC1	SELECT LATCH WHICH GENERATES THE HOP CONSTANT FOR STORAGE DURING AN INTERRUPT OPERATION.
SELMD7	SELECT MULTIPLICAND - DIVISOR REGISTER LATCH 7.
SELMR1	SELECT, LATCH IN MULTIPLIER, QUOTIENT, PRODUCT - QUOTIENT REGISTER CONDITIONED BY THE OUTPUT OF THE ACCUMULATOR DURING THE INITIATION OF EITHER MULTIPLY OPERATION AND BY THE QUOTIENT BITS DURING DIVIDE.

SYMBOL	DEFINITION
SELPH	SELECT PHASE.
SELPRO	SELECT THE OLD PARTIAL PRODUCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAINDER DURING DIVIDE.
SEL CPW	SELECT CLOCK PULSE W.
SEL CPX	SELECT CLOCK PULSE X.
SEL CPY	SELECT CLOCK PULSE Y.
SEL CPZ	SELECT CLOCK PULSE Z.
SEL CTR IND	SELECT WORD COUNTER, INDICATOR DRIVER OUTPUT.
SEL CTR	SELECT WORD COUNTER.
SELSP	SELECT SPARE PROBE.
SELTRS NOT	INVERSE, SELECT TRANSFER REGISTER SERIAL
SELTRS	SELECT, TRANSFER REGISTER SERIAL.
SEPIAD	SET PIO ADDRESS REGISTER LEVEL.
SEQ BIT	SEQUENCE BIT (CHARACTER 9, CHANNEL 7 BIT).
SER PB IND1	SERIAL PARITY BIT, INDICATOR DRIVER 1 OUTPUT.
SER PB IND2	SERIAL PARITY BIT INDICATOR DRIVER 2 OUTPUT.
SER PB NOT	INVERSE SERIAL PARITY BIT.
SER PB	SERIAL PARITY BIT
SETIADR	SET INSTRUCTION ADDRESS DISPLAY REGISTER.
SETINSDR	SET INSTRUCTION DISPLAY REGISTER.

SYMBOL	DEFINITION
SET SSMBRA	SET SECTOR, SYLLABLE, MODULE, BUFFER REGISTER LEVEL FROM DRIVE SOURCE A.
SET SSMBRB	SET SECTOR, SYLLABLE, MODULE, BUFFER REGISTER LEVEL FROM DRIVE SOURCE B.
SET SSMDRA	SET SECTOR SYLLABLE MODULE DISPLAY REGISTER LEVEL FROM DRIVE SOURCE A.
SF STOP	DOT OR ED WITH STOP NOT
SGCEL	SATURN GUIDANCE COMPUTER ERROR LAMP DRIVER INPUT.
SGCE IND1 AND 2	SATURN GUIDANCE COMPUTER ERROR, INDICATOR DRIVER 1 AND 2 OUTPUTS.
SGCE NOT	INVERSE SATURN GUIDANCE COMPUTER ERROR.
SIGNAL GRD	SIGNAL GROUND.
SKIP FIRST NOT	INVERSE SKIP FIRST LEVEL.
SKIP FIRST	ONE OUTPUT OF SKIP FIRST SEQUENCE BIT LATCH.
SLE (SET LE)	SET LATCH E - ONE OUTPUT OF LATCH WHICH SETS NINE POSITION COUNTER TO POSITION ONE (E) WHEN TAPE READER IS NOT RUNNING AND IN FORWARD MODE.
SLL NOT (SET LL NOT)	INVERT SET LATCH L LEVEL.
SLL (SET LL)	SET LATCH L - ONE OUTPUT OF LATCH WHICH SETS NINE POSITION COUNTER TO POSITION EIGHT (L) WHEN TAPE READER IS NOT RUNNING AND IN REVERSE MODE.
SLTE	SET LATCH EVEN.
SLTO	SET LATCH ODD.

SYMBOL	DEFINITION
SMCL	SHIELD, MEMORY CLOCK LATE.
SMCN	SHIELD,MEMORY CLOCK NORMAL
SM 1A	SHIFT MEMORY REGISTER PULSE A FROM DRIVE SOURCE 1.
SM 1B	SHIFT MEMORY REGISTER PULSE B FROM DRIVE SOURCE 1.
SM 1C	SHIFT MEMORY REGISTER PULSE C FROM DRIVE SOURCE 1.
SM 1D	SHIFT MEMORY REGISTER PULSE D FROM DRIVE SOURCE 1.
SM 2A	SHIFT MEMORY REGISTER PULSE A FROM DRIVE SOURCE 2.
SM 2B	SHIFT MEMORY REGISTER PULSE B FROM DRIVE SOURCE 2.
SM 2C	SHIFT MEMORY REGISTER PULSE C FROM DRIVE SOURCE 2.
SM 2D	SHIFT MEMORY REGISTER PULSE D FROM DRIVE SOURCE 2.
SP1	ACME SPARE PROBE 1
SP2	SPARE PROBE 2.
SPBG	SPARE PROBE, 1 BIT GATE.
SPB	SERIALIZER PARITY BIT.
SPDM2 NOT	INVERSE SPARE PROBE DELAY MINUS 2 BIT TIMES, LATCH OUTPUT.
SPDM2	SPARE PROBE DELAY MINUS 2 BIT TIMES, LATCH OUTPUT.
SPD	SPARE PROBE DELAYED.
SPE IND	SERIAL PARITY ERROR, INDICATOR DRIVER OUTPUT.
SPE NOT	INVERSE SET PARITY ERROR LATCH.
SPE	SET PARITY ERROR LATCH.

SYMBOL	DEFINITION
SPOFF	SPARE PROBE, TURN OFF DISPLAY SHIFT REGISTER
SPON	SPARE PROBE, TURN ON DISPLAY SHIFT REGISTER
SRPT NOT	SET REPEAT.
SSMBRD-S NOT	INVERSE SECTOR, SYLLABLE, MODULE, BUFFER REGISTER DUPLEX - SIMPLEX LATCH OUTPUT.
SSMBRD-S	SECTOR, SYLLABLE, MODULE, BUFFER REGISTER DUPLEX - SIMPLEX LATCH OUTPUT.
SSMBRDS1-4	SECTOR, SYLLABLE, MODULE, BUFFER REGISTER DATA SECTOR 1 THROUGH 4 LATCH OUTPUTS.
SSMBRDS1 NOT -4 NOT	INVERSE SECTOR, SYLLABLE, MODULE, BUFFER REGISTER DATA SECTOR 1 THROUGH 4 LATCH OUTPUTS.
SSMBRIS1-4	SECTOR SYLLABLE MODULE BUFFER REGISTER INSTRUCTION SECTOR 1 THROUGH 4 LATCH OUTPUTS.
SSMBRIS1 NOT -4 NOT	INVERSE SECTOR, SYLLABLE, MODULE BUFFER REGISTER INSTRUCTION SECTOR 1 THROUGH 4 LATCH OUTPUTS.
SSMBRMM1-3	SECTOR, SYLLABLE, MODULE, BUFFER REGISTER MEMORY MODULE 1 THROUGH 3 LATCH OUTPUTS.
SSMBRMM1 NOT -3 NOT	INVERSE SECTOR, SYLLABLE, MODULE BUFFER REGISTER MEMORY MODULE 1 THROUGH 3 LATCH OUTPUTS.
SSMBRSYLC1 NOT	INVERSE SECTOR, SYLLABLE, MODULE, BUFFER REGISTER SYLLABLE C1 LATCH OUTPUT.
SSMBRSYLC1	SECTOR, SYLLABLE, MODULE, BUFFER REGISTER SYLLABLE C1 LATCH OUTPUT.
SSMDRD-S NOT	INVERSE - SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER DUPLEX - SIMPLEX LATCH OUTPUT.

SYMBOL	DEFINITION
SSMDRD-S	SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER DUPLEX - SIMPLEX LATCH OUTPUT.
SSMDRDS1-4	SECTOR, SYLLABLE MODULE, DISPLAY REGISTER DATA SECTOR 1 THRO UGH 4 LATCH OUTPUTS.
SSMDRDS1 NOT -4 NOT	INVERSE SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER DATA SECT OR 1 THROUGH 4 LATCH OUTPUTS.
SSMDRIS1-4	SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER INSTRUCTION SECTO R 1 THROUGH 4 LATCH OUTPUTS.
SSMDRIS1 NOT -4 NOT	INVERSE SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER INSTRUCTI ON SECTOR 1 THROUGH 4 LATCH OUTPUTS.
SSMDRMM1-3	SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER MEMORY MODULE 1 T HROUGH 3 LATCH OUTPUTS.
SSMDRMM1 NOT -3 NOT	INVERSE SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER MEMORY MO DULE 1 THROUGH 3 LATCH OUTPUTS.
SSMDRSYLC1 NOT	INVERSE SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER SYLLABLE C1 LATCH OUTPUT.
SSMDRSYLC1	SECTOR, SYLLABLE, MODULE, DISPLAY REGISTER SYLLABLE C1 LATCH OUTPUT.
SSMDS1 IND -4 IND	SECTOR, SYLLABLE, MODULE, DATA SECTOR 1 THROUGH 4 INDICATOR DRIVER OUTPUTS.
SSMDX IND	SECTOR, SYLLABLE, MODULE, DUPLEX INDICATOR DRIVER OUTPUT.
SSMIS1 IND -4 IND	SECTOR, SYLLABLE, MODULE, INSTRUCTION SECTOR 1 THROUGH 4 IND DRIVER OUTPUTS.
SSMMM1 IND -3 IND	SECTOR, SYLLABLE, MODULE, MEMORY MODULE 1 THROUGH 3, INDICAT OR DRIVER OUTPUTS.

SYMBOL	DEFINITION
SSMSCW	SECTOR, SYLLABLE, MODULE, SHIFT CLOCK W CONTROL PULSE.
SSMSCX	SECTOR, SYLLABLE, MODULE, SHIFT CLOCK X CONTROL PULSE.
SSMSCYA	SECTOR, SYLLABLE, MODULE, SHIFT CLOCK Y CONTROL PULSE FROM D RIVE SOURCE A.
SSMSCY	SECTOR, SYLLABLE, MODULE, SHIFT CLOCK Y CONTROL PULSE.
SSMSCZ	SECTOR, SYLLABLE, MODULE, SHIFT CLOCK Z CONTROL PULSE.
SSMSO NOT	INVERSE SECTOR SYLLABLE MODULE SERIAL OUT.
SSMSO	SECTOR, SYLLABLE, MODULE, SERIAL OUT.
SSMSRD-S	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER DUPLEX - SIMPLEX LA TCH OUTPUT.
SSMSRDS1-SSMSRDS4	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER DATA SECTOR 1 THROU GH 4 LATCH OUTPUTS.
SSMSRIS1-4	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER INSTRUCTION SECTOR 1 THROUGH 4 LATCH OUTPUTS.
SSMSRIS2 NOT	INVERSE SECTOR, SYLLABLE, MODULE, SHIFT REGISTER INSTRUCTION SECTOR 2 LATCH OUTPUT.
SSMSRMM1	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER MEMORY MODULE 1 LAT CH OUTPUT.
SSMSRMM2 NOT	INVERSE SECTOR, SYLLABLE, MODULE, SHIFT REGISTER MEMORY MODU LE 2 LATCH OUTPUT.
SSMSRMM2	SECTOR, SYLLABLE MODULE, SHIFT REGISTER MEMORY MODULE 2 LATC H OUTPUT.
SSMSRMM3	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER MEMORY MODULE 3 LAT CH OUTPUT.

SYMBOL	DEFINITION
SSMSR DATA NOT	INVERSE SECTOR, SYLLABLE, MODULE SHIFT REGISTER DATA LATCH OUTPUT.
SSMSR DATA	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER DATA LATCH OUTPUT.
SSMSRSYLC1	SECTOR, SYLLABLE, MODULE, SHIFT REGISTER SYLLABLE C1 LATCH OUTPUT.
SSMSX IND	SECTOR, SYLLABLE, MODULE, SIMPLEX INDICATOR DRIVER OUTPUT.
SSMSYL0 IND	SECTOR, SYLLABLE, MODULE, SYLLABLE 0 INDICATOR DRIVER OUTPUT.
SSMSYL1 IND	SECTOR, SYLLABLE, MODULE, SYLLABLE 1 INDICATOR DRIVER OUTPUT.
SSOT NOT	INVERSE, CONTROL SYLLABLE ON TRANSFER.
SSR IND	SINGLE STEP READER, INDICATOR DRIVER OUTPUT.
START IND 1 AND 2	START, INDICATOR DRIVER 1 AND 2 OUTPUTS.
START SS NOT	INVERSE START SINGLE SHOT LEVEL.
START SS	START SINGLE SHORT
STOP IND 1 AND 2	STOP, INDICATOR DRIVER 1 AND 2 OUTPUTS.
STOP NOT	INVERSE STOP LEVEL.
STOP	ONE OUTPUT OF STOP LATCH, TAPE MOVEMENT CONTROL LEVEL.
STROP3	SET TAPE READER OPERATION BIT 3.
ST CYC1	START CYCLE 1.
ST CYC	START CYCLE.
SW=SSR	SWITCH, SINGLE STEP READER.

SYMBOL	DEFINITION
SW=TR=RESR	SWITCH, TAPE READER RESET REGISTER.
SWA1	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 1.
SWA2	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 2.
SWA3	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 3.
SWA4	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 4.
SWA5	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 5.
SWA6	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 6.
SWA7	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 7.
SWA8	SWITCH FOR MANUAL SELECTION OF MEMORY ADDRESS BIT 8.
SWANS NOT	SWITCH, INVERSE ANSWER.
SWIA NOT	SWITCH, INVERSE INSTRUCTION ADDRESS.
SWIA	SWITCH, INSTRUCTION ADDRESS.
SWIS1	SWITCH FOR MANUAL SELECTION OF MEMORY INSTRUCTION SECTOR, BIT 1.
SWIS2	SWITCH FOR MANUAL SELECTION OF MEMORY INSTRUCTION SECTOR, BIT 2.
SWIS3	SWITCH FOR MANUAL SELECTION OF MEMORY INSTRUCTION SECTOR, BIT 3.
SWIS4	SWITCH FOR MANUAL SELECTION OF MEMORY INSTRUCTION SECTOR, BIT 4.
SWMM1	SWITCH FOR MANUAL SELECTION OF MEMORY MODULE BIT 1.

SYMBOL	DEFINITION
SWMM2	SWITCH FOR MANUAL SELECTION OF MEMORY MODULE BIT 2.
SWMM3	SWITCH FOR MANUAL SELECTION OF MEMORY MODULE BIT 3.
SWOP1	SWITCH FOR MANUAL INSERTION OF OPERATION CODE BIT 1.
SWOP2	SWITCH FOR MANUAL INSERTION OF OPERATION CODE BIT 2.
SWOP3	SWITCH FOR MANUAL INSERTION OF OPERATION CODE BIT 3.
SWOP 4	SWITCH FOR MANUAL INSERTION OF OPERATION CODE BIT 4.
SWPPQ1 NOT THROUGH SWPPQ12 NOT	SWITCHES, INVERSE PARTIAL PRODUCT - QUOTIENT 1 THROUGH 12.
SW A1BOE0 NOT	SWITCH, CHANNEL A1, INVERSE BUFFER OSCILLATOR ERROR, FAIL TO 0.
SW A1BOE1 NOT	SWITCH, CHANNEL A1, INVERSE BUFFER OSCILLATOR ERROR, FAIL TO 1.
SW A1W0 NOT	SWITCH, CHANNEL A1, INVERSE CLOCK W, FAIL TO 0.
SW A1W1 NOT	SWITCH, CHANNEL A1, INVERSE CLOCK W, FAIL TO 1
SW A1X0 NOT	SWITCH, CHANNEL A1, INVERSE CLOCK X, FAIL TO 0.
SW A1X1 NOT	SWITCH, CHANNEL A1, INVERSE CLOCK X, FAIL TO 1.
SW A1Y0 NOT	SWITCH, CHANNEL A1, INVERSE CLOCK Y, FAIL TO 0.
SW A1Y1 NOT	SWITCH, CHANNEL A1 INVERSE CLOCK Y, FAIL TO 1.
SW A1Z0 NOT	SWITCH, INVERSE CHANNEL A1, CLOCK Z, FAIL TO 0.
SW A1Z1 NOT	SWITCH, CHANNEL A1, INVERSE CLOCK Z, FAIL TO 1.
SW A2BOE0 NOT	SWITCH, CHANNEL A2, INVERSE BUFFER OSCILLATOR ERROR, FAIL TO 0.

SYMBOL	DEFINITION
SW A2B0E1 NOT	SWITCH, CHANNEL A2, INVERSE BUFFER OSCILLATOR ERROR, FAIL TO 1.
SW A2W0 NOT	SWITCH, CHANNEL A2, INVERSE CLOCK W, FAIL TO 0.
SW A2W1 NOT	SWITCH, CHANNEL A2, INVERSE CLOCK W, FAIL TO 1.
SW A2X0 NOT	SWITCH, CHANNEL INVERSE A2, CLOCK X, FAIL TO 0.
SW A2X1 NOT	SWITCH, CHANNEL A2, INVERSE CLOCK X, FAIL TO 1.
SW A2Y0 NOT	SWITCH, CHANNEL INVERSE A2, CLOCK Y, FAIL TO 0.
SW A2Y1 NOT	SWITCH, CHANNEL A2, INVERSE CLOCK Y, FAIL TO 1.
SW A2Z0 NOT	SWITCH, CHANNEL A2, INVERSE CLOCK Z, FAIL TO 0.
SW A2Z1 NOT	SWITCH, CHANNEL A2, INVERSE CLOCK Z, FAIL TO 1.
SW A3B0E0 NOT	SWITCH, CHANNEL A3, INVERSE BUFFER OSCILLATOR ERROR, FAIL TO 0.
SW A3B0E1 NOT	SWITCH, CHANNEL A3, INVERSE BUFFER OSCILLATOR ERROR, FAIL TO 1.
SW A3W0 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK W, FAIL TO 0.
SW A3W1 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK W, FAIL TO 1.
SW A3X0 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK X, FAIL TO 0.
SW A3X1 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK X, FAIL TO 1
SW A3Y0 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK Y, FAIL TO 0.
SW A3Y1 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK Y, FAIL TO 1.
SW A3Z0 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK Z, FAIL TO 0.

SYMBOL	DEFINITION
SW A3Z1 NOT	SWITCH, CHANNEL A3, INVERSE CLOCK Z, FAIL TO 1.
SW ADV NOT	SWITCH, INVERSE ADVANCE TAPE.
SW ADV	SWITCH, ADVANCE TAPE.
SW AI3 DATA NOT	SWITCH, INVERSE AI3 DATA.
SW AI3 NOT	SWITCH, INVERSE AI3.
SW APIO1 NOT THROUGH 25 NOT	SWITCH, ACCUMULATOR REGISTER, PROCESS INPUT/OUTPUT BIT 1 THROUGH BIT 25 SELECTOR
SW APIO RES NOT	SWITCH, INVERSE ACCUMULATOR REGISTER PROCESS INPUT/OUTPUT RESET.
SW APIOSIGN NOT	SWITCH, ACCUMULATOR REGISTER, PROCESS INPUT/OUTPUT SIGN BIT SELECTOR.
SW AUTO	SWITCH, AUTOMATIC MODE.
SW B10	SWITCH FOR MANUAL INSERTION OF BIT 10, DATA BIT.
SW B11	SWITCH FOR MANUAL INSERTION OF BIT 11, DATA BIT.
SW B12	SWITCH FOR MANUAL INSERTION OF BIT 12, DATA BIT.
SW B13	SWITCH FOR MANUAL INSERTION OF BIT 13, DATA BIT.
SW B14	SWITCH FOR MANUAL INSERTION OF BIT 14, DATA BIT.
SW B15	SWITCH FOR MANUAL INSERTION OF BIT 15, DATA BIT.
SW B16	SWITCH FOR MANUAL INSERTION OF BIT 16, DATA BIT.
SW B17	SWITCH FOR MANUAL INSERTION OF BIT 17, DATA BIT.
SW B18	SWITCH FOR MANUAL INSERTION OF BIT 18, DATA BIT.

SYMBOL	DEFINITION
SW B19	SWITCH FOR MANUAL INSERTION OF BIT 19, DATA BIT.
SW B1	SWITCH FOR MANUAL INSERTION OF BIT 1, DATA BIT.
SW B20	SWITCH FOR MANUAL INSERTION OF BIT 20, DATA BIT.
SW B21	SWITCH FOR MANUAL INSERTION OF BIT 21, DATA BIT.
SW B22	SWITCH FOR MANUAL INSERTION OF BIT 22, DATA BIT.
SW B23	SWITCH FOR MANUAL INSERTION OF BIT 23, DATA BIT.
SW B24	SWITCH FOR MANUAL INSERTION OF BIT 24, DATA BIT.
SW B25	SWITCH FOR MANUAL INSERTION OF BIT 25, DATA BIT.
SW B2	SWITCH FOR MANUAL INSERTION OF BIT 2, DATA BIT.
SW B3	SWITCH FOR MANUAL INSERTION OF BIT 3, DATA BIT.
SW B4	SWITCH FOR MANUAL INSERTION OF BIT 4, DATA BIT.
SW B5	SWITCH FOR MANUAL INSERTION OF BIT 5, DATA BIT.
SW B6	SWITCH FOR MANUAL INSERTION OF BIT 6, DATA BIT.
SW B7	SWITCH FOR MANUAL INSERTION OF BIT 7, DATA BIT.
SW B8	SWITCH FOR MANUAL INSERTION OF BIT 8, DATA BIT.
SW B9	SWITCH FOR MANUAL INSERTION OF BIT 9, DATA BIT.
SW BG14P NOT	SWITCH, INVERSE BIT GATE 14.
SW BG1 THROUGH 14	SWITCH, BIT GATES 1 THROUGH 14.
SW BG1T13P NOT	SWITCH, INVERSE BIT GATE 1 TO 13.
SW CDRES NOT	SWITCH INVERSE COMPUTER DISPLAY RESET.

SYMBOL	DEFINITION
SW CD RES	SWITCH COMPUTER DISPLAY RESET.
SW CH1 MOD 1 NOT	SWITCH, CHANNEL 1 MODULE 1 SELECTION.
SW CH1 MOD 2 NOT	SWITCH, CHANNEL 1 MODULE 2 SELECTION.
SW CH1 MOD 3 NOT	SWITCH, CHANNEL 1 MODULE 3 SELECTION.
SW CH1 MOD 4 NOT	SWITCH, CHANNEL 1 MODULE 4 SELECTION.
SW CH1 MOD 5 NOT	SWITCH, CHANNEL 1 MODULE 5 SELECTION.
SW CH1 MOD 6 NOT	SWITCH, CHANNEL 1 MODULE 6 SELECTION.
SW CH1 MOD 7 NOT	SWITCH, CHANNEL 1 MODULE 7 SELECTION.
SW CH1 NOT	SWITCH, CHANNEL 1 SELECTION.
SW CH2 MOD1 NOT	SWITCH, CHANNEL 2 MODULE 1 SELECTION.
SW CH2 MOD2 NOT	SWITCH CHANNEL 2 MODULE 2 SELECTION.
SW CH2 MOD3 NOT	SWITCH, CHANNEL 2 MODULE 3 SELECTION.
SW CH2 MOD4 NOT	SWITCH, CHANNEL 2 MODULE 4 SELECTION.
SW CH2 MOD5 NOT	SWITCH, CHANNEL 2 MODULE 5 SELECTION.
SW CH2 MOD6 NOT	SWITCH, CHANNEL 2 MODULE 6 SELECTION.
SW CH2 MOD7 NOT	SWITCH, CHANNEL 2 MODULE 7 SELECTION.
SW CH 2 NOT	SWITCH CHANNEL 2 SELECTION.
SW CH 3 MOD 1 NOT	SWITCH, CHANNEL 3 MODULE 1 SELECTION.
SW CH 3 MOD 2 NOT	SWITCH, CHANNEL 3 MODULE 2 SELECTION.

SYMBOL	DEFINITION
SW CH 3 MOD 3 NOT	SWITCH, CHANNEL 3 MODULE 3 SELECTION.
SW CH 3 MOD 4 NOT	SWITCH, CHANNEL 3 MODULE 4 SELECTION.
SW CH 3 MOD 5 NOT	SWITCH, CHANNEL 3 MODULE 5 SELECTION.
SW CH 3 MOD 6 NOT	SWITCH, CHANNEL 3 MODULE 6 SELECTION.
SW CH 3 MOD 7 NOT	SWITCH, CHANNEL 3 MODULE 7 SELECTION.
SW CH 3 NOT	SWITCH, CHANNEL 3 SELECTION.
SW CH ALL NOT	SWITCH, INVERSE ALL CHANNEL SELECTION.
SW CH NOT	SWITCH, INVERSE CHANNEL.
SW CH	SWITCH, CHANNEL.
SW CH SEL	SWITCH, CHANNEL SELECTION.
SW CPW NOT	SWITCH, INVERSE CLOCK PULSE W.
SW CPX NOT	SWITCH, INVERSE CLOCK PULSE X.
SW CPY NOT	SWITCH, INVERSE CLOCK PULSE Y.
SW CPZ NOT	SWITCH, INVERSE CLOCK PULSE Z.
SW CST ADV NOT	SWITCH, INVERSE COMPUTER SINGLE - STEP ADVANCE.
SW CST NOT	SWITCH, INVERSE COMPUTER SINGLE - STEP.
SW CST	SWITCH, COMPUTER SINGLE STEP.
SW DD	SWITCH, DATA DISPLAY MODE.
SW DIE MAN	SWITCH, DATA INTERFACE EXERCIZER MANUAL.
SW DIE SGC	SWITCH, DATA INTERFACE EXERCIZER, SATURN GUIDANCE COMPUTER.

SYMBOL	DEFINITION
SW DIR NOT	SWITCH, INVERSE DIRECTION.
SW DIR	SWITCH, DIRECTION (CONTROLS TAPE FORWARD-REVERSE MOTION).
SW DIS RPT NOT	SWITCH, INVERSE DISPLAY REPEAT.
SW DIS RPT	SWITCH, DISPLAY REPEAT.
SW DS1	SWITCH FOR MANUAL SELECTION OF DATA SELECTOR BIT 1.
SW DS2	SWITCH FOR MANUAL SELECTION OF DATA SELECTOR BIT 2.
SW DS3	SWITCH FOR MANUAL SELECTION OF DATA SELECTOR BIT 3.
SW DS4	SWITCH FOR MANUAL SELECTION OF DATA SELECTOR BIT 4.
SW DX	SWITCH FOR MANUAL SELECTION OF DUPLEX MODE.
SW EARLY	SWITCH, MEMORY CLOCK EARLY.
SW ERR TEST	SWITCH, ERROR TEST.
SW E RES	SWITCH, ERROR RESET.
SW FRSS NOT	SWITCH, INVERSE FREE RUN SINGLE SHOT.
SW FRSS	SWITCH, FREE RUN SINGLE SHOT.
SW FRTR	SWITCH, FREE RUN TAPE READER.
SW HLT NOT	SWITCH, INVERSE HALT.
SW HLT RPT NOT	SWITCH, INVERSE HALT REPEAT.
SW HLT RPT	SWITCH, HALT REPEAT.
SW HOPC1 NOT	SWITCH, INVERSE LEVEL WHICH GENERATES HOP CONSTANT FOR STORAGE DURING AN INTERRUPT OPERATION.

SYMBOL	DEFINITION
SW INTER NOT	SWITCH, INVERSE INTERRUPT.
SW INTER	SWITCH, INTERRUPT
SW LAMP TEST 01-A2	GROUND LEVEL FROM LAMP TEST SWITCH (FRAME 01 PANEL A2) WHICH CAUSES LAMP TEST RELAY 01A9K7 TO BE ENERGIZED.
SW LAMP TEST 02-A1	GROUND LEVEL FROM LAMP TEST SWITCH (FRAME 02, PANEL A1) WHIC H CAUSES LAMP TEST RELAY 01A9K5 TO BE ENERGIZED.
SW LAMP TEST 02-A2	GROUND LEVEL FROM LAMP TEST SWITCH (FRAME 02, PANEL A2) WHIC H CAUSES LAMP TEST RELAY 01A9K6 TO BE ENERGIZED.
SW LATE	SWITCH, MEMORY CLOCK LATE.
SW MAN	SWITCH, MANUAL MODE.
SW MD7 NOT	SWITCH, INVERSE MULTIPLICAND - DIVISOR LATCH 7.
SW MEM SIM NOT	SWITCH, INVERSE MEMORY SIMULATE
SW MEM SIM	SWITCH, MEMORY SIMULATE.
SW ML	SWITCH, MEMORY LOAD.
SW MOD 1 NOT	SWITCH, INVERSE MODULE 1 SELECTION.
SW MOD 1	SWITCH, MODULE 1 SELECTION.
SW MOD 2 NOT	SWITCH, INVERSE MODULE 2 SELECTION.
SW MOD 2	SWITCH, MODULE 2 SELECTION
SW MOD 3 NOT	SWITCH, INVERSE MODULE 3 SELECTION.
SW MOD 3	SWITCH, MODULE 3 SELECTION.
SW MOD 4 NOT	SWITCH, INVERSE MODULE 4 SELECTION.

SYMBOL	DEFINITION
SW MOD 4	SWITCH, MODULE 4 SELECTION.
SW MOD 5 NOT	SWITCH, INVERSE MODULE 5 SELECTION.
SW MOD 5	SWITCH, MODULE 5 SELECTION.
SW MOD 6 NOT	SWITCH, INVERSE MODULE 6 SELECTION.
SW MOD 6	SWITCH, MODULE 6 SELECTION.
SW MOD 7 NOT	SWITCH, INVERSE MODULE 7 SELECTION.
SW MOD 7	SWITCH, MODULE 7 SELECTION.
SW MOD SEL	SWITCH, MODULE SELECTION
SW MPIO1 NOT THROUGH 25 NOT	SWITCH, INVERSE MEMORY REGISTER PROCESS INPUT/OUTPUT BITS 1 THROUGH 25.
SW MPIO1 THROUGH 25	SWITCH, MEMORY REGISTER PROCESS INPUT/OUTPUT BITS 1 THROUGH 25.
SW MPIO RES NOT	SWITCH, INVERSE MEMORY REGISTER PROCESS INPUT/OUTPUT RESET.
SW MPIO SIGN NOT	SWITCH, INVERSE MEMORY REGISTER PROCESS INPUT/OUTPUT SIGN BIT.
SW MPIO SIGN	SWITCH, MEMORY REGISTER PROCESS INPUT/OUTPUT SIGN BIT.
SW MR1 NOT	SWITCH, INVERSE MR1 LEVEL.
SW NORMAL	SWITCH, MEMORY CLOCK NORMAL.
SW NO BG	SWITCH, NO BIT GATE.
SW NO CP NOT	SWITCH, INVERSE NO CLOCK PULSE.
SW NO PH	SWITCH, NO PHASE.

SYMBOL	DEFINITION
SW OA1	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 1.
SW OA2	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 2.
SW OA3	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 3.
SW OA4	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 4.
SW OA5	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 5.
SW OA6	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 6.
SW OA7	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 7.
SW OA8	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 8.
SW OA9	SWITCH FOR MANUAL INSERTION OF OPERAND ADDRESS BIT 9.
SW OVERRIDE NOT	SWITCH, INVERSE ERROR OVERRIDE.
SW OVERRIDE	SWITCH, ERROR OVERRIDE.
SW OVRICST NOT	SWITCH, INVERSE OVERIDE COMPUTER SINGLE - STEP.
SW PAPR NOT	SWITCH, INVERSE PAST - PRESENT.
SW PAPR	SWITCH, PAST - PRESENT.
SW PHA	SWITCH, PHASE A.
SW PHB	SWITCH, PHASE B.
SW PHC	SWITCH, PHASE C.
SW PRO NOT	SWITCH, INVERSE LEVEL DESIGNATING THE OLD PARTIAL PRODUCT DU RING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAIND ER DURING DIVIDE.

SYMBOL	DEFINITION
SW RESET 1	SWITCH, RESET 1 - RESETS ALL ERROR DEVICES TO NO ERROR CONDITION BEFORE INFORMATION TRANSFER CAN TAKE PLACE. THE SWITCH IS LOCATED ON PANEL A1.
SW RESET 2	SWITCH, RESET 2 - SAME FUNCTION AS SW RESET 1. THE SWITCH IS IS LOCATED ON PANEL A2.
SW RPT NOT	SWITCH, INVERSE REPEAT.
SW RPT	SWITCH, REPEAT.
SW SEL ADR	SWITCH SELECT ADDRESS.
SW SEL CTR	SWITCH, SELECT WORD COUNTER.
SW SGC RES	SWITCH SATURN GUIDANCE COMPUTER RESET.
SW SGDTC NOT	SWITCH, INVERSE SINGLE GATE DATA TO COMPUTER.
SW SGDTC	SWITCH, SINGLE GATE DATA TO COMPUTER.
SW SIGN	SWITCH FOR MANUAL INSERTION OF SIGN, DATA BIT.
SW SP1 NOT	SWITCH, INVERSE SPARE PROBE 1.
SW SP2 NOT	SWITCH, INVERSE SPARE PROBE 2.
SW START NOT	SWITCH, INVERSE START TAPE READER.
SW START	SWITCH, START TAPE READER.
SW START SS	SWITCH, START SINGLE SHOT
SW STOP	SWITCH, STOP TAPE READER.
SW SYL	SWITCH, SYLLABLE.
SW TAADR1	SWITCH FOR MANUAL INSERTION OF TAPE ADDRESS BIT 1.

SYMBOL	DEFINITION
SW TAADR2	SWITCH FOR MANUAL INSERTION OF TAPE ADDRESS BIT 2.
SW TAADR3	SWITCH FOR MANUAL INSERTION OF TAPE ADDRESS BIT 3.
SW TAADR4	SWITCH FOR MANUAL INSERTION OF TAPE ADDRESS BIT 4.
SW TAADR5	SWITCH FOR MANUAL INSERTION OF TAPE ADDRESS BIT 5.
SW TA PWR	SWITCH, TAPE POWER.
SW T-0	SWITCH, THIS (PRESENT) WORD (-) MINUS 0.
SW T-10	SWITCH, THIS (PRESENT) WORD (-) MINUS 10.
SW T-11	SWITCH, THIS (PRESENT) WORD (-) MINUS 11.
SW T-12	SWITCH, THIS (PRESENT) WORD (-) MINUS 12.
SW T-1	SWITCH, THIS (PRESENT) WORD (-) MINUS 1.
SW T-2	SWITCH, THIS (PRESENT) WORD (-) MINUS 2.
SW T-3	SWITCH, THIS (PRESENT) WORD (-) MINUS 3.
SW T-4	SWITCH, THIS (PRESENT) WORD (-) MINUS 4.
SW T-5	SWITCH, THIS (PRESENT) WORD (-) MINUS 5.
SW T-6	SWITCH, THIS (PRESENT) WORD (-) MINUS 6.
SW T-7	SWITCH, THIS (PRESENT) WORD (-) MINUS 7.
SW T-8	SWITCH, THIS (PRESENT) WORD (-) MINUS 8.
SW T-9	SWITCH, THIS (PRESENT) WORD (-) MINUS 9.
SW TRCB1	SWITCH, TAPE READER CHARACTER - COUNTER BIT 1.
SW TRCB2	SWITCH, TAPE READER CHARACTER - COUNTER BIT 2.

SYMBOL	DEFINITION
SW TRCB3	SWITCH, TAPE READER CHARACTER - COUNTER BIT 3.
SW TRCB4	SWITCH, TAPE READER CHARACTER - COUNTER BIT 4.
SW TRCB5	SWITCH, TAPE READER CHARACTER - COUNTER BIT 5.
SW TRCB6	SWITCH, TAPE READER CHARACTER - COUNTER BIT 6.
SW TRCB7	SWITCH, TAPE READER CHARACTER - COUNTER BIT 7.
SW TRCB8	SWITCH, TAPE READER CHARACTER - COUNTER BIT 8.
SW TRCB9	SWITCH, TAPE READER CHARACTER - COUNTER BIT 9.
SW TRCH1-02 THROUGH SW TRCH6-02	SWITCHES, TAPE READER CHANNELS 1 THROUGH 6 (PANEL 02)
SW TRCH 1-01 THRU SW TRCH 5-01	SWITCHES, TAPE READER CHANNEL 1 THROUGH 5 (PANEL 01).
SW TR RES	SWITCH, TAPE READER RESET.
SW TRS NOT	SWITCH, INVERSE TRANSFER REGISTER SERIAL LEVEL.
SW T NOT	SWITCH, INVERSE THIS (PRESENT) WORD.
SWVER ONLY NOT	SWITCH, INVERSE VERIFY ONLY.
SWVER ONLY	SWITCH, VERIFY ONLY.
SYL1BRAB	SYLLABLE 1, BUFFER REGISTER A, FROM B DRIVE SOURCE.
SYL1BRA IND	SYLLABLE 1, BUFFER REGISTER A, INDICATOR DRIVER OUTPUT.
SYL1BRA NOT	INVERSE SYLLABLE 1, BUFFER REGISTER A, LATCH OUTPUT.
SYL1BRA	SYLLABLE 1, BUFFER REGISTER A, LATCH OUTPUT.
SYL1BRB IND	SYLLABLE 1, BUFFER REGISTER B, INDICATOR DRIVER OUTPUT.

SYMBOL	DEFINITION
SYL1BRB NOT	INVERSE SYLLABLE 1 BUFFER REGISTER B LATCH OUTPUT
SYL1BRB	SYLLABLE 1 BUFFER REGISTER B LATCH OUTPUT.
SYLOBRAB	SYLLABLE 0, BUFFER REGISTER A, FROM B DRIVE SOURCE
SYLOBRA IND	SYLLABLE 0 BUFFER REGISTER A, INDICATOR DRIVER OUTPUT.
SYLOBRA NOT	INVERSE SYLLABLE 0 BUFFER REGISTER A LATCH OUTPUT.
SYLOBRA	SYLLABLE 0 BUFFER REGISTER A LATCH OUTPUT.
SYLOBRB IND	SYLLABLE 0 BUFFER REGISTER B, INDICATOR DRIVER OUTPUT.
SYLOBRB NOT	INVERSE SYLLABLE 0 BUFFER REGISTER B LATCH OUTPUT.
SYLOBRB	SYLLABLE 0 BUFFER REGISTER B LATCH OUTPUT.
SYNC NOT	INVERTED SYNC LEVEL.
SYNC OUTPUT	OSCILOSCOPE SYNC, EVERY ADDRESS COMPARE.
SYNC	STARTS ACME PHASE GENERATOR - CAUSED BY COMPUTER PHASE B.
TA1A1 NOT THROUGH TA1A9 NOT	INVERSE TRANSLATED CHANNEL A1 ADDRESS REGISTER BITS 1 THROUGH 9.
TA1AI3 NOT	TRANSLATED, CHANNEL A1, AI3 INVERTED.
TA1EAM NOT, TA2EAM NOT AND TA3EAM NOT	INVERSE TRANSLATED CHANNELS A1, A2, A3 LATCH OUTPUTS WHICH INDICATES AN ERROR IN EVEN MEMORIES
TA1EBM NOT	TRANSLATED, INVERSE CHANNEL A1, ERROR IN ODD MEMORIES LEVEL.
TA1G5	TRANSLATED, CHANNEL A1, BIT GATE GENERATOR LATCH 5 OUTPUT.
TA1-3HOPC1V	TRANSLATED CHANNELS A1 THROUGH A3, HOP CONSTANT FOR STORAGE DURING INTERRUPT OPERATION.

SYMBOL	DEFINITION
TA1MD7, NOT TA2MD7 NOT AND TA3 MD7 NOT	INVERSE TRANSLATED, CHANNELS A1, A2, AND A3, MULTIPLICAND - DIVISOR REGISTER LATCH 7.
TA1MR1I	TRANSLATED, CHANNEL A1 MR1 INVERTED
TA1MR1 NOT	INVERSE TRANSLATED, CHANNEL A1, MR1 LATCH OUTPUT.
TA1MR1	TRANSLATED, CHANNEL A1, MR1 LATCH OUTPUT.
TA1OP1 NOT THROUGH TA1OP4 NOT	INVERSE TRANSLATED CHANNEL A1 OPERATION CODE BITS 1 THROUGH 4.
TA1PB	TRANSLATED, CHANNEL A1 PHASE B.
TA1PIO NOT	INVERSE TRANSLATED CHANNEL A1 PROCESS INPUT/OUTPUT.
TA1PRO NOT, TA2PRO NOT AND TA3 PRO NOT	INVERSE TRANSLATED OLD PARTIAL PRODUCT DURING EITHER MULTIPLY OPERATION OR FOUR TIMES THE OLD REMAINDER DURING DIVIDE.
TA1TLC NOT	TRANSLATED, INVERSE CHANNEL A1, TWO SIMULTANEOUS MEMORY ERRORS LEVEL.
TA1TRS NOT, TA2TRS NOT AND TA3 TRS NOT	INVERSE TRANSLATED CHANNELS A1, A2 AND A3, TRANSFER REGISTER SERIAL LATCH.
TA1WDA, TA1XDA, TA1YDA AND TA1 ZDA	TRANSLATED CHANNEL A1, W,X,Y AND Z CLOCK PULSE DRIVERS TO DATA ADAPTER.
TA2A1 NOT THROUGH TA2A9 NOT	INVERSE TRANSLATED CHANNEL A2 ADDRESS REGISTER BITS 1 THROUGH 9.
TA2AI3 NOT	TRANSLATED, CHANNEL A2, AI3 INVERTED.
TA2EBM NOT	TRANSLATED, INVERSE CHANNEL A2, ERROR IN ODD MEMORIES LEVEL.
TA2G5	TRANSLATED, CHANNEL A2, BIT GATE GENERATOR LATCH 5 OUTPUT.
TA2MR1 NOT	INVERSE TRANSLATED, CHANNEL A2, MR1 LATCH OUTPUT.

SYMBOL	DEFINITION
TA2MR1	TRANSLATED, CHANNEL A2, MR1 LATCH OUTPUT.
TA2MR1T	TRANSLATED, CHANNEL A2 MR1 INVERTED
TA2OP1 NOT THROUGH TA2OP4 NOT	INVERSE TRANSLATED CHANNEL A2 OPERATION CODE BITS 1 THROUGH 4.
TA2PB	TRANSLATED, CHANNEL A2 PHASE B.
TA2PIO NOT	INVERSE TRANSLATED CHANNEL A2 PROCESS INPUT/OUTPUT.
TA2TLC NOT	TRANSLATED, INVERSE CHANNEL A2, TWO SIMULTANEOUS MEMORY ERRORS LEVEL.
TA2WDA, TA2XDA, TA2YDA AND TA2ZDA	TRANSLATED CHANNEL A2, W,X,Y AND Z CLOCK PULSE DRIVERS TO DATA ADAPTER
TA3A1 NOT THROUGH TA3A9 NOT	INVERSE TRANSLATED CHANNEL A3 ADDRESS REGISTER BITS 1 THROUGH 9.
TA3AI3 NOT	TRANSLATED, CHANNEL A3, AI3 INVERTED.
TA3EBM NOT	TRANSLATED, INVERSE CHANNEL A3, ERROR IN ODD MEMORIES LEVEL.
TA3G5	TRANSLATED, CHANNEL A3, BIT GATE GENERATOR LATCH 5 OUTPUT.
TA3MR1I	TRANSLATED, CHANNEL A3 MR1 INVERTED
TA3MR1 NOT	INVERSE TRANSLATED, CHANNEL A3, MR1 LATCH OUTPUT.
TA3MR1	TRANSLATED, CHANNEL A3, MR1 LATCH OUTPUT.
TA3OP1 NOT THROUGH TA3OP4 NOT	INVERSE TRANSLATED CHANNEL A3 OPERATION CODE BITS 1 THROUGH 4.
TA3PB	TRANSLATED, CHANNEL A3 PHASE B.
TA3PIO NOT	INVERSE TRANSLATED CHANNEL A3 PROCESS INPUT/OUTPUT LEVEL.

SYMBOL	DEFINITION
TA3TLC NOT	TRANSLATED INVERSE, CHANNEL A3, TWO SIMULTANEOUS ERRORS LEVEL.
TA3WDA, TA3XDA, TA3YDA AND TA3ZDA	TRANSLATED CHANNEL A3, W,X,Y AND Z CLOCK PULSE DRIVERS TO DATA ADAPTER.
TA=PWR=OFF=IND	TAPE POWER OFF, INDICATOR DRIVER OUTPUT
TA=PWR=ON=IND	TAPE POWER ON, INDICATOR DRIVER OUTPUT
TAADR1 THRU TAADR5 IND	TAPE ADDRESS SELECTION BITS 1 THROUGH 5, INDICATOR DRIVER OUTPUTS.
TADR	TRANSLATED ADDRESS LEVEL.
TAPAR ERR	TAPE PARITY ERROR LEVEL.
TAPB NOT	INVERSE TAPE PARITY BIT LEVEL.
TA ADR1 NOT	ZERO OUTPUT OF TAPE ADDRESS BIT 1 LATCH.
TA ADR1	ONE OUTPUT OF TAPE ADDRESS BIT 1 LATCH.
TA ADR2 NOT	ZERO OUTPUT OF TAPE ADDRESS BIT 2 LATCH.
TA ADR2	ONE OUTPUT OF TAPE ADDRESS BIT 2 LATCH.
TA ADR3 NOT	ZERO OUTPUT OF TAPE ADDRESS BIT 3 LATCH.
TA ADR3	ONE OUTPUT OF TAPE ADDRESS BIT 3 LATCH.
TA ADR4 NOT	ZERO OUTPUT OF TAPE ADDRESS BIT 4 LATCH.
TA ADR4	ONE OUTPUT OF TAPE ADDRESS BIT 4 LATCH.
TA ADR5 NOT	ZERO OUTPUT OF TAPE ADDRESS BIT 5 LATCH.
TA ADR5	ONE OUTPUT OF TAPE ADDRESS BIT 5 LATCH.

SYMBOL	DEFINITION
TA PWR ERR INT	TAPE POWER ERROR INTERLOCK.
TA PWR RELAY GRD	TAPE POWER RELAY GROUND.
TA PWR REL GRD	TAPE POWER RELAY GROUND. IT BECOMES THE TA PWR GROUND LEVEL WHEN THERE IS NO TAPE POWER ERROR AND TAPE POWER ON PUSHBUTT ON IS PRESSED.
TA PWR	TAPE POWER GROUND LEVEL - ALLOWS TAPE POWER RELAY 01B5K2 TO BE ENERGIZED
TATC	TRANSFER ADDRESS TO COMPUTER.
TBRA14P NOT	INVERSE, TRANSLATED BUFFER REGISTER A, BIT 14 - PARITY.
TBRB14P NOT	INVERSE, TRANSLATED BUFFER REGISTER B, BIT 14 - PARITY.
TBRB14P	TRANSLATED, BUFFER REGISTER B, BIT 14 - PARITY.
TCIR	GROUND LEVEL FROM INHIBIT READER CONTROL SWITCH WHICH CAUSES READER INHIBIT RELAY 01A9K15 TO BE ENERGIZED.
TDTTC	TRANSFER DATA TO COMPUTER.
TEMPHIGHIND	TEMPERATURE HIGH, INDICATOR DRIVER OUTPUT.
TEMP ERR1	TEMPERATURE ERROR 1.
TEMP ERR2	TEMPERATURE ERROR 2.
TEMP NORM IND	TEMPERATURE NORMAL, INDICATOR DRIVER OUTPUT.
TE ERR ARRAY IND	TEMPERATURE ERROR ARRAY, INDICATOR DRIVER OUTPUT.
TE ERR PAGE IND	TEMPERATURE ERROR PAGE, INDICATOR DRIVER OUTPUT.
TE PWR SEQ OFF	TEMPERATURE ERROR, POWER SEQUENCE OFF.

SYMBOL	DEFINITION
TE RES	TEMPERATURE RESET.
TIME SEL	TIME SELECT.
TIMING MARKER	OSCILOSCOPE SYNC --- ANY SELECTED CLOCK, BIT GATE AND PHASE.
TNOT	INVERSE DATA SERIALIZER PARITY BIT LATCH OUTPUT.
TOM	INVERSE ERROR RESET (NOT OR'D WITH ERROR RESET.).
TPE IND	TAPE PARITY ERROR, INDICATOR DRIVER OUTPUT.
TP GND	TEST POINT GROUND.
TRA1 IND	TAPE READER ADDRESS SELECTION BIT 1, INDICATOR DRIVER OUTPUT.
TRA1 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 1 LATCH.
TRA1	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 1 LATCH.
TRA2 IND	TAPE READER ADDRESS SELECTION BIT 2, INDICATOR DRIVER OUTPUT.
TRA2 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 2 LATCH.
TRA2	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 2 LATCH.
TRA3 IND	TAPE READER ADDRESS SELECTION BIT 3, INDICATOR DRIVER OUTPUT.
TRA3 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 3 LATCH.
TRA3	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 3 LATCH.
TRA4 IND	TAPE READER ADDRESS SELECTION BIT 4, INDICATOR DRIVER OUTPUT.
TRA4 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 4 LATCH.

SYMBOL	DEFINITION
TRA4	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 4 LATCH.
TRA5 IND	TAPE READER ADDRESS SELECTION BIT 5, INDICATOR DRIVER OUTPUT
TRA5 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 5 LATCH.
TRA5	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 5 LATCH.
TRA6 IND	TAPE READER ADDRESS SELECTION BIT 6, INDICATOR DRIVER OUTPUT
TRA6 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 6 LATCH.
TRA6	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 6 LATCH.
TRA7 IND	TAPE READER ADDRESS SELECTION BIT 7, INDICATOR DRIVER OUTPUT
TRA7 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 7 LATCH.
TRA7	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 7 LATCH.
TRA8 IND	TAPE READER ADDRESS SELECTION BIT 8, INDICATOR DRIVER OUTPUT
TRA8 NOT	ZERO OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 8 LATCH.
TRA8	ONE OUTPUT OF TAPE READER ADDRESS SELECTION, BIT 8 LATCH.
TRACK 1	TAPE TRACK 1 - ZERO LEVEL FOR A SENSED BIT.
TRACK 2	TAPE TRACK 2 - ZERO LEVEL FOR A SENSED BIT.
TRACK 3	TAPE TRACK 3 - ZERO LEVEL FOR A SENSED BIT.
TRACK 4	TAPE TRACK 4 - ZERO LEVEL FOR A SENSED BIT.

SYMBOL	DEFINITION
TRACK 5	TAPE TRACK 5 - ZERO LEVEL FOR A SENSED BIT.
TRACK 6	TAPE TRACK 6 - ZERO LEVEL FOR A SENSED BIT.
TRACK 8	OUTPUT OF TRACK 8 TAPE READER PARITY CHANNEL.
TRANS INH NOT	INVERSE TRANSFER INHIBIT LEVEL.
TRA NOT	INVERSE TRANSFER.
TRA PB	TRANSFER PARITY BIT.
TRA	TRANSFER.
TRCB1	TAPE READER CHARACTER - COUNTER BIT 1
TRCB2	TAPE READER CHARACTER - COUNTER BIT 2
TRCB3	TAPE READER CHARACTER - COUNTER BIT 3
TRCB4	TAPE READER CHARACTER - COUNTER BIT 4
TRCB5	TAPE READER CHARACTER - COUNTER BIT 5
TRCB6	TAPE READER CHARACTER - COUNTER BIT 6
TRCB7	TAPE READER CHARACTER - COUNTER BIT 7
TRCB8	TAPE READER CHARACTER - COUNTER BIT 8.
TRCB9	TAPE READER CHARACTER - COUNTER BIT 9.
TRCB-1 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 1 LATCH.
TRCB-1	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 1 LATCH.
TRCB-2 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 2 LATCH.
TRCB-2	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 2 LATCH.

SYMBOL	DEFINITION
TRCB-3 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 3 LATCH.
TRCB-3	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 3 LATCH.
TRCB-4 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 4 LATCH.
TRCB-4	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 4 LATCH.
TRCB-5 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 5 LATCH.
TRCB-5	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 5 LATCH.
TRCB-6 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 6 LATCH.
TRCB-6	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 6 LATCH.
TRCB-7 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 7 LATCH.
TRCB-7	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 7 LATCH.
TRCB-8 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 8 LATCH.
TRCB-8	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 8 LATCH.
TRCB-9 NOT	ZERO OUTPUT OF TAPE READER CHARACTER COUNTER BIT 9 LATCH.
TRCB-9	ONE OUTPUT OF TAPE READER CHARACTER COUNTER BIT 9 LATCH.
TRCH1A NOT	INVERSE TAPE READER CHANNEL 1, FROM DRIVE SOURCE A.
TRCH1A	TAPE READER CHANNEL 1, FROM DRIVE SOURCE A.
TRCH2A NOT	INVERSE TAPE READER CHANNEL 2, FROM DRIVE SOURCE A.
TRCH2A	TAPE READER CHANNEL 2, FROM DRIVE SOURCE A.
TRCH3A NOT	INVERSE TAPE READER CHANNEL 3, FROM DRIVE SOURCE A.

SYMBOL	DEFINITION
TRCH3A	TAPE READER CHANNEL 3, FROM DRIVE SOURCE A.
TRCH4A NOT	INVERSE TAPE READER CHANNEL 4, FROM DRIVE SOURCE A.
TRCH4A	TAPE READER CHANNEL 4, FROM DRIVE SOURCE A.
TRCH5A NOT	INVERSE TAPE READER CHANNEL 5, FROM DRIVE SOURCE A.
TRCH5A	TAPE READER CHANNEL 5, FROM DRIVE SOURCE A.
TRCH6A NOT	INVERSE TAPE READER CHANNEL 6, FROM DRIVE SOURCE A.
TRCH6A	TAPE READER CHANNEL 6, FROM DRIVE SOURCE A.
TRCLA NOT	INVERSE TAPE READER CLEAR AND ADD LEVEL.
TRCP1A	TAPE READER CLOCK PULSE 1 FROM A DRIVE SOURCE.
TRCP1B	TAPE READER CLOCK PULSE 1 FROM B DRIVE SOURCE.
TRCP1C	TAPE READER CLOCK PULSE 1 FROM C DRIVE SOURCE.
TRCP2A	TAPE READER CLOCK PULSE 2 FROM A DRIVE SOURCE.
TRCP2B	TAPE READER CLOCK PULSE 2 FROM B DRIVE SOURCE.
TRCP3A	TAPE READER CLOCK PULSE 3 FROM A DRIVE SOURCE.
TRCP4	TAPE READER CLOCK PULSE 4
TRCP ERR DLY	TAPE READER CLOCK PULSE ERROR DELAY.
TRCP ERR NOT	INVERSE TRCP ERR LEVEL.
TRCP ERR	ONE OUTPUT OF THE TAPE READER CLOCK PULSE ERROR LATCH. SET WHEN A CLOCK FAILS TO A CONSTANT ONE.
TRCP GEN	TAPE READER CLOCK PULSE GENERATOR.

SYMBOL	DEFINITION
TRDA PB NOT	INVERSE TAPE READER DATA PARITY BIT.
TRDA PB	TAPE READER DATA PARITY BIT.
TRDA RES	TAPE READER DATA RESET.
TRDS1 IND	TAPE READER DATA SELECTOR BIT 1, INDICATOR DRIVER OUTPUT.
TRDS2 IND	TAPE READER DATA SELECTOR BIT 2, INDICATOR DRIVER OUTPUT.
TRDS3 IND	TAPE READER DATA SELECTOR BIT 3, INDICATOR DRIVER OUTPUT.
TRDS4 IND	TAPE READER DATA SELECTOR BIT 4, INDICATOR DRIVER OUTPUT.
TRDX	TAPE READER, DUPLEX MODE.
TRG CLOCK1	TRIGGER INPUT, CLOCK 1.
TRG CLOCK2	TRIGGER INPUT, CLOCK 2.
TRIA PB NOT	INVERSE TAPE READER INSTRUCTION - ADDRESS PARITY BIT.
TRIA PB	TAPE READER INSTRUCTION - ADDRESS PARITY BIT.
TRIA RES	TAPE READER INSTRUCTION ADDRESS RESET.
TRIS1 IND	TAPE READER INSTRUCTION SECTOR BIT 1, INDICATOR DRIVER OUTPUT.
TRIS1 NOT	ZERO OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 1 LATCH.
TRIS1	ONE OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 1 LATCH.
TRIS2 IND	TAPE READER INSTRUCTION SECTOR BIT 2, INDICATOR DRIVER OUTPUT.
TRIS2 NOT	ZERO OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 2 LATCH.
TRIS2	ONE OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 2 LATCH.

SYMBOL	DEFINITION
TRIS3 IND	TAPE READER INSTRUCTION SECTOR BIT 3, INDICATOR DRIVER OUTPUT.
TRIS3 NOT	ZERO OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 3 LATCH.
TRIS3	ONE OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 3 LATCH.
TRIS4 IND	TAPE READER INSTRUCTION SECTOR BIT 4, INDICATOR DRIVER OUTPUT.
TRIS4 NOT	ZERO OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 4 LATCH.
TRIS4	ONE OUTPUT OF TAPE READER INSTRUCTION SECTOR BIT 4 LATCH.
TRMM1 IND	TAPE READER MEMORY MODULE BIT 1, INDICATOR DRIVER OUTPUT.
TRMM1 NOT	ZERO OUTPUT OF TAPE READER MEMORY MODULE BIT 1 LATCH.
TRMM1	ONE OUTPUT OF TAPE READER MEMORY MODULE BIT 1 LATCH.
TRMM2 IND	TAPE READER MEMORY MODULE BIT 2, INDICATOR DRIVER OUTPUT.
TRMM2 NOT	ZERO OUTPUT OF TAPE READER MEMORY MODULE BIT 2 LATCH.
TRMM2	ONE OUTPUT OF TAPE READER MEMORY MODULE BIT 2 LATCH.
TRMM3 IND	TAPE READER MEMORY MODULE BIT 3, INDICATOR DRIVER OUTPUT.
TRMM3 NOT	ZERO OUTPUT OF TAPE READER MEMORY MODULE BIT 3 LATCH.
TRMM3	ONE OUTPUT OF TAPE READER MEMORY MODULE BIT 3 LATCH.
TROA1 IND	TAPE READER OPERAND ADDRESS BIT 1, INDICATOR DRIVER OUTPUT.
TROA1 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 1 LATCH.
TROA1	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 1 LATCH.

SYMBOL	DEFINITION
TROA2 IND	TAPE READER OPERAND ADDRESS BIT 2, INDICATOR DRIVER OUTPUT.
TROA2 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 2 LATCH.
TROA2	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 2 LATCH.
TROA3 IND	TAPE READER OPERAND ADDRESS BIT 3, INDICATOR DRIVER OUTPUT.
TROA3 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 3 LATCH.
TROA3	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 3 LATCH.
TROA4 IND	TAPE READER OPERAND ADDRESS BIT 4, INDICATOR DRIVER OUTPUT.
TROA4 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 4 LATCH.
TROA4	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 4 LATCH.
TROA5 IND	TAPE READER OPERAND ADDRESS BIT 5, INDICATOR DRIVER OUTPUT.
TROA5 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 5 LATCH.
TROA5	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 5 LATCH.
TROA6 IND	TAPE READER OPERAND ADDRESS BIT 6, INDICATOR DRIVER, OUTPUT.
TROA6 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 6 LATCH.
TROA6	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 6 LATCH.
TROA7 IND	TAPE READER OPERAND ADDRESS BIT 7, INDICATOR DRIVER OUTPUT.
TROA7 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 7 LATCH.
TROA7	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 7 LATCH.
TROA8 IND	TAPE READER OPERAND ADDRESS BIT 8, INDICATOR DRIVER OUTPUT.
TROA8 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 8 LATCH.

SYMBOL	DEFINITION
TROA8	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 8 LATCH.
TROA9 IND	TAPE READER OPERAND ADDRESS BIT 9, INDICATOR DRIVER OUTPUT.
TROA9 NOT	ZERO OUTPUT OF TAPE READER OPERAND ADDRESS BIT 9 LATCH.
TROA9	ONE OUTPUT OF TAPE READER OPERAND ADDRESS BIT 9 LATCH.
TROP1 IND	TAPE READER OPERATION CODE BIT 1, INDICATOR DRIVER OUTPUT.
TROP1 NOT	ZERO OUTPUT OF TAPE READER OPERATION CODE BIT 1 LATCH.
TROP1	ONE OUTPUT OF TAPE READER OPERATION CODE BIT 1 LATCH.
TROP2 IND	TAPE READER OPERATION CODE BIT 2, INDICATOR DRIVER OUTPUT.
TROP2 NOT	ZERO OUTPUT OF TAPE READER OPERATION CODE BIT 2 LATCH.
TROP2	ONE OUTPUT OF TAPE READER OPERATION CODE BIT 2 LATCH.
TROP3 IND	TAPE READER OPERATION CODE BIT 3, INDICATOR DRIVER OUTPUT.
TROP3 NOT	ZERO OUTPUT OF TAPE READER OPERATION CODE BIT 3 LATCH.
TROP3	ONE OUTPUT OF TAPE READER OPERATION CODE BIT 3 LATCH.
TROP4 IND	TAPE READER OPERATION CODE BIT 4, INDICATOR DRIVER OUTPUT.
TROP4 NOT	ZERO OUTPUT OF TAPE READER OPERATION CODE BIT 4 LATCH.
TROP4	ONE OUTPUT OF TAPE READER OPERATION CODE BIT 4 LATCH.
TR B10 IND	TAPE READER BIT 10, INDICATOR DRIVER OUTPUT.
TR B10 NOT	ZERO OUTPUT OF TAPE READER BIT 10 LATCH.
TR B10	ONE OUTPUT OF TAPE READER BIT 10 LATCH.

SYMBOL	DEFINITION
TR B11 IND	TAPE READER BIT 11, INDICATOR DRIVER OUTPUT.
TR B11 NOT	ZERO OUTPUT OF TAPE READER BIT 11 LATCH.
TR B11	ONE OUTPUT OF TAPE READER BIT 11 LATCH.
TR B12 IND	TAPE READER BIT 12, INDICATOR DRIVER OUTPUT.
TR B12 NOT	ZERO OUTPUT OF TAPE READER BIT 12 LATCH.
TR B12	ONE OUTPUT OF TAPE READER BIT 12 LATCH.
TR B13 IND	TAPE READER BIT 13, INDICATOR DRIVER OUTPUT.
TR B13 NOT	ZERO OUTPUT OF TAPE READER BIT 13 LATCH.
TR B13	ONE OUTPUT OF TAPE READER BIT 13 LATCH.
TR B14 IND	TAPE READER BIT 14, INDICATOR DRIVER OUTPUT.
TR B14 NOT	ZERO OUTPUT OF TAPE READER BIT 14 LATCH.
TR B14	ONE OUTPUT OF TAPE READER BIT 14 LATCH.
TR B15 IND	TAPE READER BIT 15, INDICATOR DRIVER OUTPUT.
TR B15 NOT	ZERO OUTPUT OF TAPE READER BIT 15 LATCH.
TR B15	ONE OUTPUT OF TAPE READER BIT 15 LATCH.
TR B16 IND	TAPE READER BIT 16, INDICATOR DRIVER OUTPUT.
TR B16 NOT	ZERO OUTPUT OF TAPE READER BIT 16 LATCH.
TR B16	ONE OUTPUT OF TAPE READER BIT 16 LATCH.
TR B17 IND	TAPE READER BIT 17, INDICATOR DRIVER OUTPUT.
TR B17 NOT	ZERO OUTPUT OF TAPE READER BIT 17 LATCH.

SYMBOL	DEFINITION
TR B17	ONE OUTPUT OF TAPE READER BIT 17 LATCH.
TR B18 IND	TAPE READER BIT 18, INDICATOR DRIVER OUTPUT.
TR B18 NOT	ZERO OUTPUT OF TAPE READER BIT 18 LATCH.
TR B18	ONE OUTPUT OF TAPE READER BIT 18 LATCH.
TR B19 IND	TAPE READER BIT 19, INDICATOR DRIVER OUTPUT.
TR B19 NOT	ZERO OUTPUT OF TAPE READER BIT 19 LATCH.
TR B19	ONE OUTPUT OF TAPE READER BIT 19 LATCH.
TR B1 IND	TAPE READER BIT 1, INDICATOR DRIVER OUTPUT.
TR B1 NOT	ZERO OUTPUT OF TAPE READER BIT 1 LATCH.
TR B1	ONE OUTPUT OF TAPE READER BIT 1 LATCH.
TR B20 IND	TAPE READER BIT 20, INDICATOR DRIVER OUTPUT.
TR B20 NOT	ZERO OUTPUT OF TAPE READER BIT 20 LATCH.
TR B20	ONE OUTPUT OF TAPE READER BIT 20 LATCH.
TR B21 IND	TAPE READER BIT 21, INDICATOR DRIVER OUTPUT.
TR B21 NOT	ZERO OUTPUT OF TAPE READER BIT 21 LATCH.
TR B21	ONE OUTPUT OF TAPE READER BIT 21 LATCH.
TR B22 IND	TAPE READER BIT 22, INDICATOR DRIVER OUTPUT.
TR B22 NOT	ZERO OUTPUT OF TAPE READER BIT 22 LATCH.
TR B22	ONE OUTPUT OF TAPE READER BIT 22 LATCH.

SYMBOL	DEFINITION
TR B23 IND	TAPE READER BIT 23, INDICATOR DRIVER OUTPUT.
TR B23 NOT	ZERO OUTPUT OF TAPE READER BIT 23 LATCH.
TR B23	ONE OUTPUT OF TAPE READER BIT 23 LATCH.
TR B24 IND	TAPE READER BIT 24, INDICATOR DRIVER OUTPUT.
TR B24 NOT	ZERO OUTPUT OF TAPE READER BIT 24 LATCH.
TR B24	ONE OUTPUT OF TAPE READER BIT 24 LATCH.
TR B25 IND	TAPE READER BIT 25, INDICATOR DRIVER OUTPUT.
TR B25 NOT	ZERO OUTPUT OF TAPE READER BIT 25 LATCH.
TR B25	ONE OUTPUT OF TAPE READER BIT 25 LATCH.
TR B2 IND	TAPE READER BIT 2, INDICATOR DRIVER OUTPUT.
TR B2 NOT	ZERO OUTPUT OF TAPE READER BIT 2 LATCH.
TR B2	ONE OUTPUT OF TAPE READER BIT 2 LATCH.
TR B3 IND	TAPE READER BIT 3, INDICATOR DRIVER OUTPUT.
TR B3 NOT	ZERO OUTPUT OF TAPE READER BIT 3 LATCH.
TR B3	ONE OUTPUT OF TAPE READER BIT 3 LATCH.
TR B4 IND	TAPE READER BIT 4, INDICATOR DRIVER OUTPUT.
TR B4 NOT	ZERO OUTPUT OF TAPE READER BIT 4 LATCH.
TR B4	ONE OUTPUT OF TAPE READER BIT 4 LATCH.
TR B5 IND	TAPE READER BIT 5, INDICATOR DRIVER OUTPUT.
TR B5 NOT	ZERO OUTPUT OF TAPE READER BIT 5 LATCH.

SYMBOL	DEFINITION
TR B5	ONE OUTPUT OF TAPE READER BIT 5 LATCH.
TR B6 IND	TAPE READER BIT 6, INDICATOR DRIVER OUTPUT.
TR B6 NOT	ZERO OUTPUT OF TAPE READER BIT 6 LATCH.
TR B6	ONE OUTPUT OF TAPE READER BIT 6 LATCH.
TR B7 IND	TAPE READER BIT 7, INDICATOR DRIVER OUTPUT.
TR B7 NOT	ZERO OUTPUT OF TAPE READER BIT 7 LATCH.
TR B7	ONE OUTPUT OF TAPE READER BIT 7 LATCH.
TR B8 IND	TAPE READER BIT 8, INDICATOR DRIVER OUTPUT.
TR B8 NOT	ZERO OUTPUT OF TAPE READER BIT 8 LATCH.
TR B8	ONE OUTPUT OF TAPE READER BIT 8 LATCH.
TR B9 IND	TAPE READER BIT 9, INDICATOR DRIVER OUTPUT.
TR B9 NOT	ZERO OUTPUT OF TAPE READER BIT 9 LATCH.
TR B9	ONE OUTPUT OF TAPE READER BIT 9 LATCH.
TR DATA RESET	TAPE READER DATA RESET.
TR DATA RES	TAPE READER DATA RESET LEVEL.
TR DS1 NOT	ZERO OUTPUT OF TAPE READER DATA SELECTOR BIT 1 LATCH.
TR DS1	ONE OUTPUT OF TAPE READER DATA SELECTOR BIT 1 LATCH.
TR DS2 NOT	ZERO OUTPUT OF TAPE READER DATA SELECTOR BIT 2 LATCH.
TR DS2	ONE OUTPUT OF TAPE READER DATA SELECTOR BIT 2 LATCH.

SYMBOL	DEFINITION
TR DS3 NOT	ZERO OUTPUT OF TAPE READER DATA SELECTOR BIT 3 LATCH.
TR DS3	ONE OUTPUT OF TAPE READER DATA SELECTOR BIT 3 LATCH.
TR DS4 NOT	ZERO OUTPUT OF TAPE READER DATA SELECTOR BIT 4 LATCH.
TR DS4	ONE OUTPUT OF TAPE READER DATA SELECTOR BIT 4 LATCH.
TR DX IND	TAPE READER DUPLEX MODE, INDICATOR DRIVER OUTPUT.
TR IA RES	TAPE READER INSTRUCTION ADDRESS LEVEL.
TR RESR	TAPE READER, RESET REGISTER.
TR SIGN IND	TAPE READER SIGN BIT, INDICATOR DRIVER OUTPUT.
TR SIGN NOT	ZERO OUTPUT OF TAPE READER SIGN BIT LATCH.
TR SIGN	ONE OUTPUT OF TAPE READER SIGN BIT LATCH.
TR SX IND	TAPE READER SIMPLEX MODE, INDICATOR DRIVER OUTPUT.
TR SYL 1 IND	TAPE READER SYLLABLE 1, INDICATOR DRIVER OUTPUT.
TR SYL 1 PB	TAPE READER SYLLABLE 1 PARITY BIT. CHANNEL 6 OF TAPE CHARACTER 9 IS PARITY BIT FOR SYLLABLE 1.
TR SYL OPB	TAPE READER SYLLABLE 0 PARITY BIT. CHANNEL 1 OF TAPE CHARACTER 8 IS PARITY BIT FOR SYLLABLE 0.
TR SYL 0 IND	TAPE READER SYLLABLE 0, INDICATOR DRIVER OUTPUT.
TR SYL 0	TAPE READER SYLLABLE 0.
TRSTO	DECODED TAPE READER STORE.
TRSX	TAPE READER, SIMPLEX MODE.
TRSYL1 PB IND	TAPE READER SYLLABLE 1 PARITY BIT, INDICATOR DRIVER OUTPUT.

SYMBOL	DEFINITION
TRSYL1 PB NOT	INVERSE TAPE READER SYLLABLE 1 PARITY BIT.
TRSYLO PB IND	TAPE READER SYLLABLE 0 PARITY BIT INDICATOR DRIVER OUTPUT.
TRSYLO PB NOT	INVERSE TAPE READER SYLLABLE 0 PARITY BIT.
TRTT	TAPE READER TIMING TRACK. DRIVES TAPE READER CLOCK GENERATOR
T NOT	INVERSE, DATA SERIALIZER PARITY BIT LATCH OUTPUT.
T PE ERR NOT	INVERSE TAPE PARITY ERROR.
T	DATA SERIALIZER PARITY BIT LATCH OUTPUT.
TSP1-2	TRANSLATED SPARE PROBE 1 AND 2.
TWO NOT OR FOUR NOT	TAPE READER OPERATION CODE BIT 2 AND TAPE READER OPERATION C ODE BIT 4 DECODED.
VER ONLY IND 1 AND 2	VERIFY ONLY, INDICATOR DRIVER 1 AND 2 OUTPUTS.
WDL1G	WRITE DELAY LINE 1, DRIVER PIN G OUTPUT.
WDL1H	WRITE DELAY LINE 1, DRIVER PIN H OUTPUT.
WDL2G	WRITE DELAY LINE 2, DRIVER PIN G OUTPUT.
WDL2H	WRITE DELAY LINE 2, DRIVER PIN H OUTPUT.
WDL3G	WRITE DELAY LINE 3, DRIVER PIN G OUTPUT.
WDL3H	WRITE DELAY LINE 3, DRIVER PIN H OUTPUT.
WD CTR A NOT THROUGH F NOT	INVERSE WORD COUNTER A THROUGH F.
WD CTR A	WORD COUNTER A.
WD CTR B	WORD COUNTER B.

SYMBOL	DEFINITION
WD CTR C	WORD COUNTER C.
WD CTR D	WORD COUNTER D
WD CTR E	WORD COUNTER E.
WD CTR F	WORD COUNTER F.
WINE	LATCH OUTPUT, GATES DATA ADDRESS BITS INTO HISTORY MODE.
W AND A NOT	BIT COUNTER CONTROL LEVEL - RESULT OF COMBINED CLOCK W AND INVERTED STEERING LATCH A OUTPUT.
W AND A	BIT COUNTER CONTROL LEVEL - RESULT OF COMBINED CLOCK W AND STEERING LATCH A OUTPUT.
ZERO COUNT2 NOT	INVERSE, ZERO COUNT OF MULTIPLY/DIVIDE COUNTER 2.

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