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ON THE EXTRAPOLATION OF ACCELERATED STRESS CONDITIONS TO NORMAL STRESS CONDITIONS OF GERMANIUM TRANSISTORS

by
Jayne Partridge

September 1963

MIT INSTRUMENTATION LABORATORY
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ON THE EXTRAPOLATION OF ACCELERATED STRESS CONDITIONS TO NORMAL STRESS CONDITIONS OF GERMANIUM TRANSISTORS

ABSTRACT

Accelerated stressing has become a popular method of evaluating high reliability devices in short periods of testing time However, the convenience of accelerated testing should not be the prime factor for its use. The modes of failure generated by normal (within rating) and accelerated (exceeding rating) stressing should be compared before failure rates created by accelerated stressing are accepted as valid

It has been found for moisture gettered PNP germanium mesa transistors that the predominant modes of failure created during accelerated stressing are different from the predominant modes of failure created during normal stressing During accelerated unpowered thermal stressing, parameter changes are exactly opposite to parameter changes during normal unpowered thermal stressing The direction and irreversibility of parameter changes, the dependance of amount of parameter change on the stabilization bake temperature and internal package vapor pressure, and a good fit of h_{FE} decay to Wallmark's equation.

$$\frac{1}{h_{FE}} = C_1 e^{-\frac{C_2}{T}} t^{\frac{1}{3}} + C_3 ,$$

all point to oxidation of the germanium surface. The activation energy as determined from the above equation is discussed Oxidation of the germanium surface is negligible at temperatures

less than stabilization bake temperatures.

Accelerated powering produced several predominant failure modes not observed during normal power stressing. Electrical overstressing characterized by lead wire melting and junction shorting were first order failures. Failures by junction shorting through the bulk were reverse collector voltage dependant as well as power dependant. The failures were attributed to operation in a negative resistance mode During lower voltage accelerated power stressing, parameter degradation identical to parameter degradation created during accelerated unpowered thermal stressing was observed at the emitter junction only. As has been found with normal stressing, unpowered thermal stresses in general do not create the same failure modes or parameter changes as the combination of reverse voltage and power. Only as reverse bias is decreased do parameter changes approach those of pure thermal stresses

by Jayne Partridge
November 1963

TABLE OF CONTENTS

	Page
Introduction	7
Section	
1. Parameter Changes During Normal Stress . . .	7
2. Parameter Changes During Accelerated Temperature Stress	8
3. Activation Energies Of Accelerated Temperature Reaction	15
4. Non-Predominant Failure Modes Created During Accelerated Step Stress	16
5. Parameter Changes During Accelerated Power Stressing	19
6. General Discussion	27
List of Symbols	33
List of References	35

LIST OF ILLUSTRATIONS

		Page
Fig 1	Variation of h_{FE} with accelerated temperature stress, time, and stabilization bake. Indicated temperatures are for transistors stabilize baked at 175°C . .	11
Fig. 2	Variation of $1V_{CBO}$ with accelerated temperature stress, time, and stabilization bake Indicated temperatures are for transistors stabilize baked at 175°C. .	13
Fig. 3	Schematic representation of types of collector reverse of collector reverse diode characteristics created during accelerated temperature stress .	14
Fig. 4	Variation of h_{FE} of molecular sieve dessicated transistors with temperature stress and moisture content Stress interval, 24 hours. Sample size, 9 per curve Stabilize baked at 150°C . . .	17
Fig 5	Variation of h_{FE} of $BaCO_3$ + Ni (1:2) dessicated transistors with temperature stress Stress interval, 24 hours. Sample size 35 Stabilize baked at 150°C. .	18
Fig 6a	h_{FE} vs accumulated time on stress for lots (A) 1, 2, and 3 of Table I (B) 9, 10, and 11 of Table IV. . .	25
Fig. 6b	h_{FE} accumulated time on stress for lots (A) 1, 2, and 3 of Table I (B) 9, 10, and 11 of Table IV (Cont) . . .	26
Fig. 7	Comparison of the h_{FE} decay of a 5v, 400 mw life test with the 225°C life test of Table III Both groups stabilize baked at 150°C.	29

ON THE EXTRAPOLATION OF ACCELERATED STRESS CONDITIONS TO NORMAL STRESS CONDITIONS OF GERMANIUM TRANSISTORS

Introduction

The increased demand for high reliability devices has created the necessity of using large samples of devices exposed to long term stresses so that reliable failure rate data may be generated. As a result, the application of accelerated stress conditions has been proposed as a means of accumulating failure rate data. Accelerated life testing has the advantage of shorter stress time using small samples.

A method of accelerated testing was proposed by Peck[(1)*] and further studied by Howard and Dodson.[(2, 3)] By their step stress technique a small sample of transistors or diodes is subjected to temperature or power in excess of rated temperature or power in steps of increasing magnitude while time under stress is held constant. Early failures are then forced. A plot of log failure rate vs. reciprocal temperature was shown to give a straight line. Extrapolation of the line to a given stress condition within the rating of the device will hopefully give the failure rate at that stress. This technique would certainly be valid if the predominant mechanism causing failure or parameter change at the accelerated stress is identical or a least similar in behavior and dependancy to the predominant mechanism causing failure or parameter change within rated stress. This assumption must be critically viewed before failure rate data generated by the step stress method can be accepted as a realistic prediction.

1. Parameter Changes During Normal Stress

Normal stressing is defined as subjecting transistors to temperature, voltage and power equal to or less than the rated temperature, voltage and power conditions of the transistor. The primary parameter changes of germanium transistors during normal stressing have been previously reported[(4)] and will be briefly reviewed.

*Superscript numerals refer to similarly numbered documents in the list of references.

Normal temperature stressing of germanium PNP transistors whose initial surface is accumulated shows that h_{FE} increases, I_{CBO} or I_{EBO} decreases and BV_{CBO} or BV_{EBO} decreases Breakdown voltage "sweepout" increases. If the initial surface is sufficiently inverted, h_{FE} will decrease and no change in BV_{CBO} or BV_{EBO} will be observed The direction of these parameter changes indicates that the surface has become more accumulated during normal temperature stressing [5] Reverse biasing of the diodes shows the exact opposite changes indicating the surface becomes more inverted during reverse voltage stressing These described parameter changes are completely reversible with long time constants

2. Parameter Changes During Accelerated Temperature Stressing

Accelerated temperature stressing is defined as subjecting transistors to temperatures in excess of the rated temperatures of the devices

During accelerated temperature stressing of germanium PNP transistors with initially accumulated or slightly inverted surfaces, it was found that h_{FE} decreased and I_{CBO} and I_{EBO} increased. High current BV_{CBO} or BV_{EBO} increased if the surface was originally accumulated or exhibited no change if the surface was slightly inverted. Low current breakdown voltage will decrease, but this is, in effect, a change in leakage current. [5] These parameter changes are not reversible At this point, it can be concluded that curves determined from accelerated temperature stressing of germanium transistors cannot be extrapolated to normal stressing temperatures because of the occurrence of a predominant new mode of failure However, further study of this new predominant failure mode is required

In addition to the parameter changes described above, it was also observed that the rate of parameter degradation depended strongly on stabilization bake temperature. The direction of parameter change indicates that the surface becomes more

inverted during accelerated temperature stress [5] For a PNP transistor this implies that the surface is receiving a source of negative charge, thus driving the surface of the base region p type. The irreversibility of the parameter change might indicate the occurrence of a chemical reaction A reaction which would fit all these symptoms is the further oxidation of the germanium surface.

Wallmark[6] developed an equation relating the h_{FE} of a germanium PNP transistor to the temperature-time dependance of the oxidation of the transistor surface at low temperatures The equation has the form

$$\frac{1}{h_{FE}} = C_1 e^{-C_2/T} t^{1/3} + C_3 \quad (1)$$

In order to determine if the h_{FE} decrease with time and accelerated temperature would fit the above equation, the tests outlined in Tables I to III were performed using the Syl 2017 transistor The Syl 2017 is a germanium mesa,, PNP, diffused base, alloyed emitter transistor in a JEDEC TO-18 package. The variation of the median normalized h_{FE} is shown in Fig 1. Using only the data generated by the test described in Table I, a fit to Eq. 1 was attempted. The best fit found was

$$\frac{1}{h_{FE}} = e^{14\ 8} e^{-11,000/T} t^{1/3} + 0.01 \quad (2)$$

Note that the theoretical curves of Fig. 1 intersect the step stress lots and that the fit is good except for the 300°C, 240 hour point (Lot 3) Failure analysis of the devices after the 300°C, 240 hour exposure indicated electrical overstress because the gold lead wires were melted and some splattered, junctions were completely shorted. This could have easily occured during the 15 V I_{CBO} measurement which was read prior to h_{FE} .

Table I

Syl-2017 Temperature Step Stress Tests. Stabilization Bake, 175°C For 170 Hours.

Lot #	Sample Size	Time Intervals	Initial Temp.	Temp. Steps
1	100	5 hrs.	275°C	25°C
2	100	72 hrs.	250°C	25°C
3	100	240 hrs.	225°C	25°C

Table II

Syl-2017 Temperature Life Tests. Stabilization Bake, 175°C For 170 Hours.

Lot #	Sample Size	Life Test Temperature
4	100	225°C
5	100	275°C
6	100	300°C

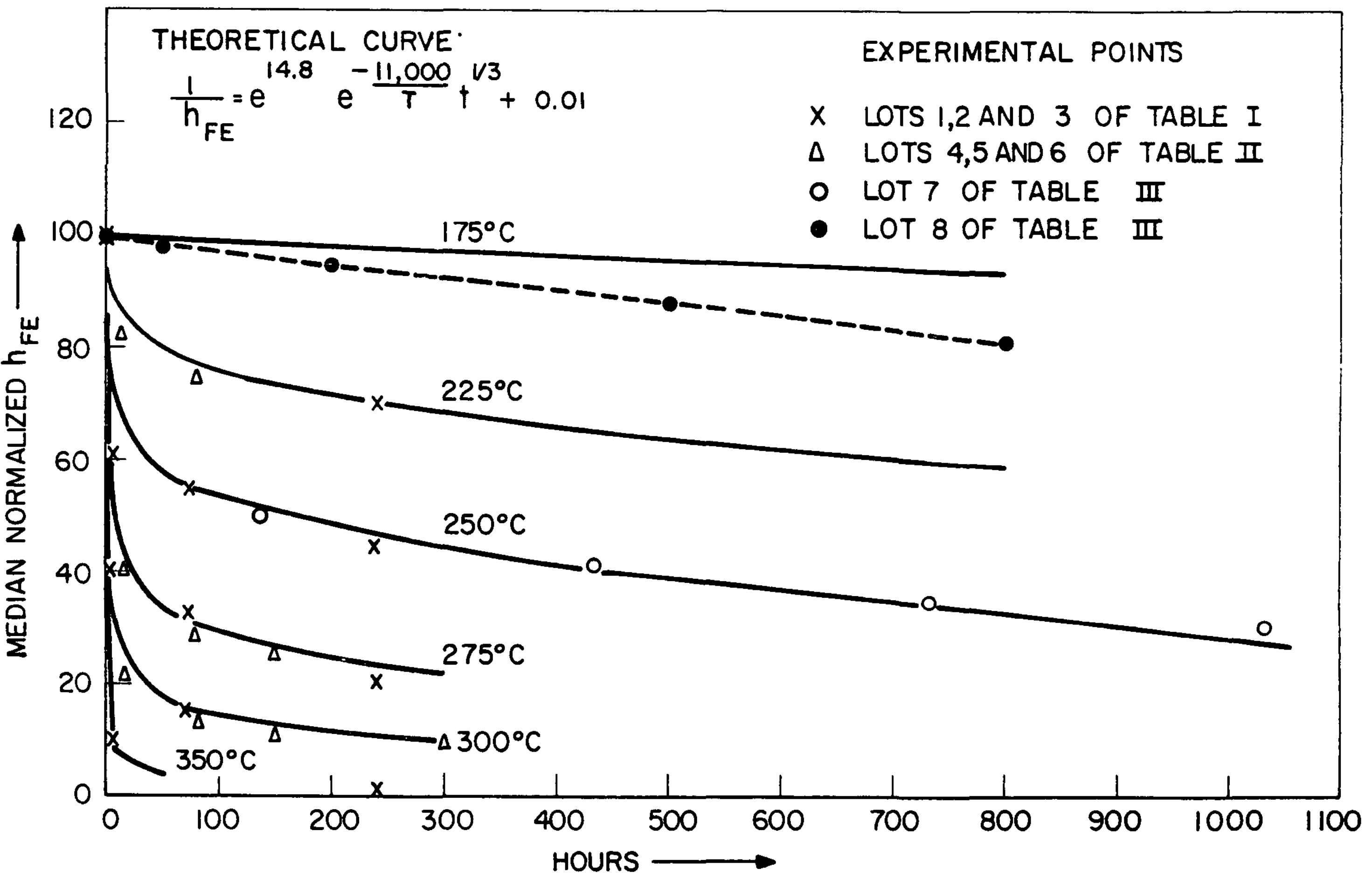
Table III

Syl-2017 Temperature Life Tests. Stabilize Baked For 170 Hours.

Lot#	Sample Size	Stabilization Bake	Life Test Temperature
7	400	150°C	225°C
8	10	225°C	225°C

Fig 1

VARIATION OF h_{FE} WITH ACCELERATED TEMPERATURE STRESS, TIME, AND STABILIZATION BAKE. INDICATED TEMPERATURES ARE FOR TRANSISTORS STABILIZE BAKED AT 175°C.



If care was not taken in the measurement of 15 V I_{CBO}, the extremely high reverse junction currents (in the order of milliamps at 15 V) which developed during the very high temperature baking were sufficient to cause damage. For this reason, only h_{FE} was measured during the test described in Table II.

Lots 4, 5 and 6 of Table II show that, when temperature is constant and time is varied, a good fit to the theoretical curve is established. The 150 hour reading of lot 4 was not plotted since the oven temperature increased from 225°C to 280°C for 28 hours during the last 72 hour interval. However, it was interesting to note that, using the value of h_{FE} created during the last 72 hour interval and knowing the amount of time in which the oven ran away, the temperature of the oven could be calculated using Eq. 2. The lot 5 life test was extended to 300 hours to verify the 300°C maverick point of lot 3.

The dependance of the median normalized h_{FE} decay on stabilization bake temperature is also shown in Fig. 1 by lots 7 and 8 of Table III. These two lots can be compared with the lots stabilize baked at 175°C and life tested at 225°C. It is seen that increasing the stabilization bake temperature decreases the severity of h_{FE} decay during accelerated temperature stressing. All the transistors used in this study were stabilize baked for 170 hours.

The median normalized 1 V I_{CBO} change with time and temperature for lots 1, 2, 3, 7 and 8 is shown in Fig. 2. The types of collector reverse diode curves created during accelerated temperature stress are schematically shown in Fig. 3. If a catastrophic limit is placed on $h_{FE} \leqq 10$, curve 2 of Fig. 3 corresponds to the collector reverse diode when a catastrophic h_{FE} failure has occurred. If a catastrophic limit is placed on 15 V $I_{CBO} \geqq 500\ \mu a$, curves 3 - 6 represent various types of I_{CBO} failures. I_{EBO} at 5 V also increased, but a slower rate than the 15 V I_{CBO} increase until a surface collector to emitter short was created with pinch-off voltages[7] of 1 - 5 V (curve 4 of Fig. 3). Then the rate of I_{CBO}

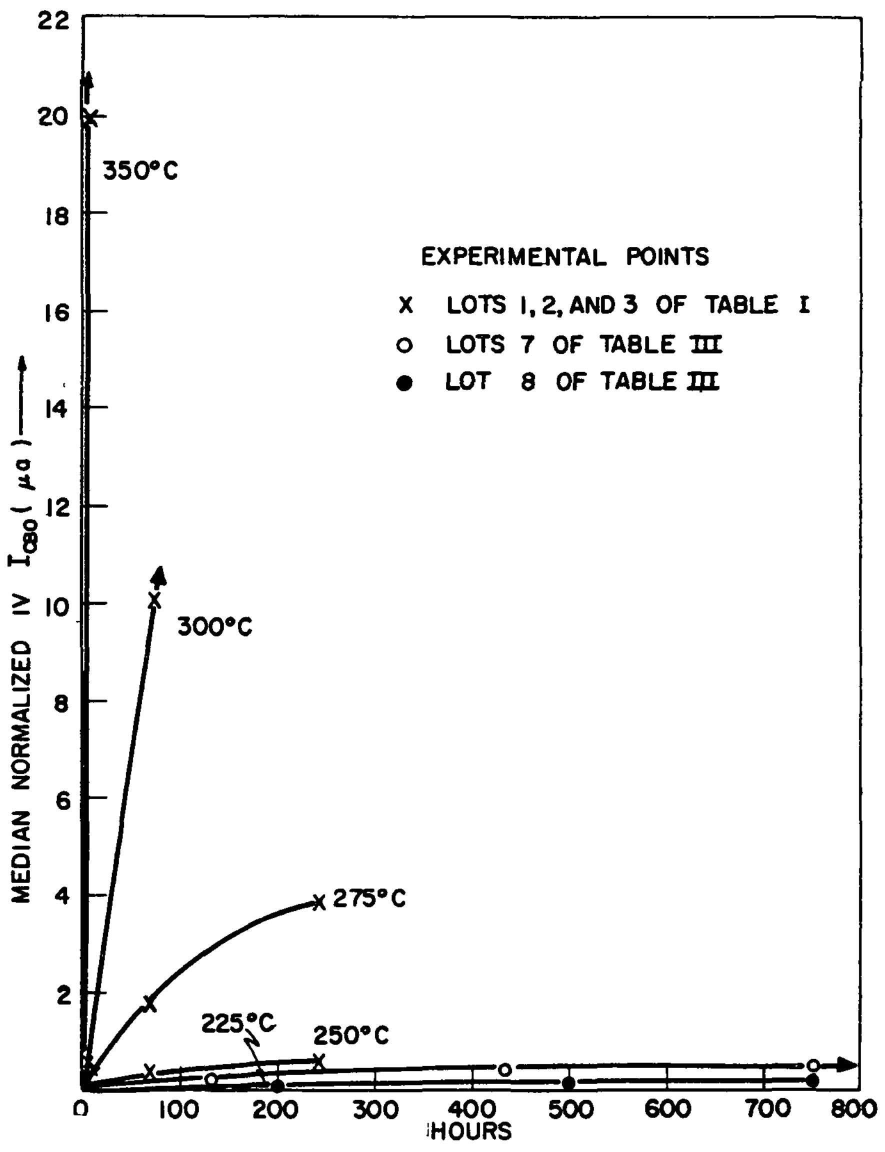
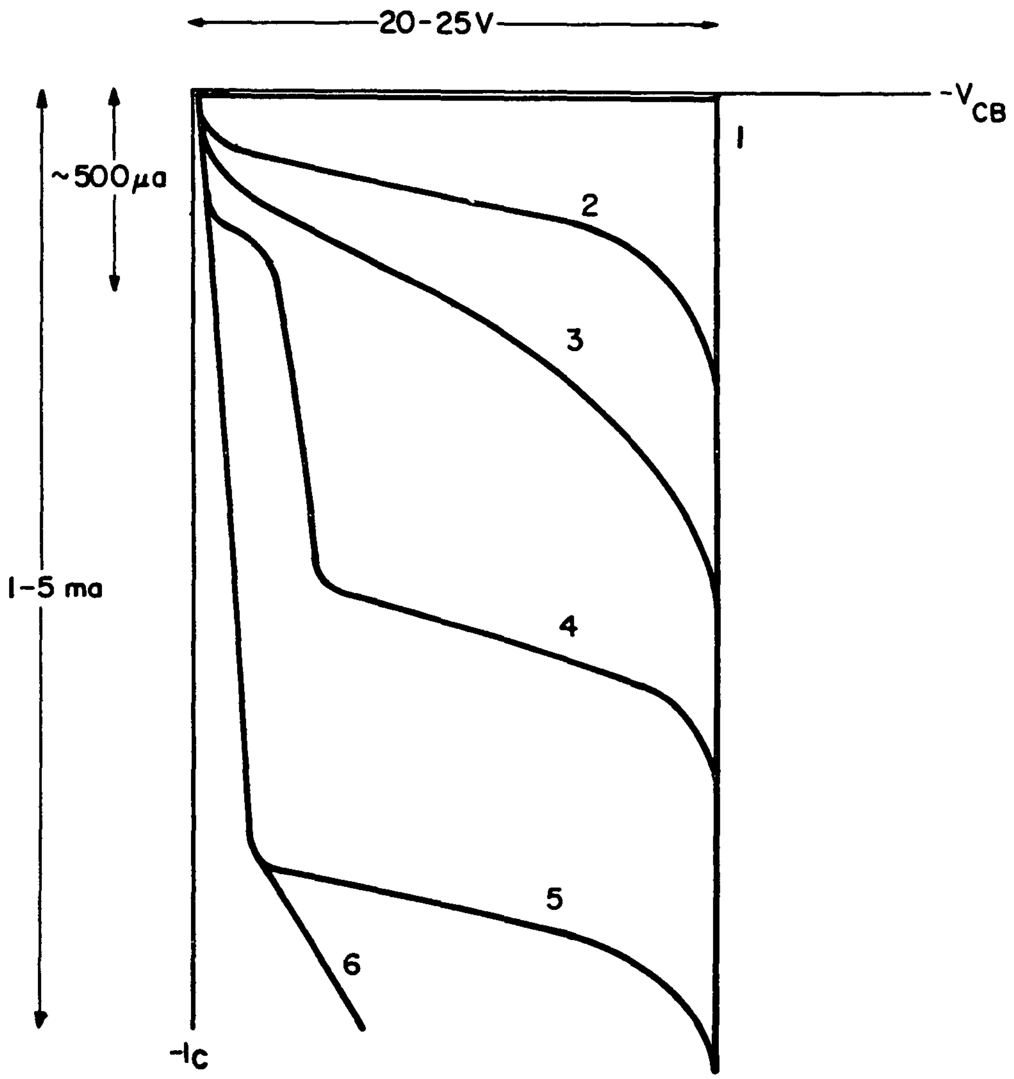


Fig. 2

VARIATION OF IV_{CBO} WITH ACCELERATED TEMPERATURE STRESS, TIME, AND STABILIZATION BAKE. INDICATED TEMPERATURES ARE FOR TRANSISTORS STABILIZE BAKED AT 175°C.

Fig. 3

SCHEMATIC REPRESENTATION OF TYPES OF COLLECTOR REVERSE DIODE CHARACTERISTICS CREATED DURING ACCELERATED TEMPERATURE STRESS.



and I_{EBO} increase was identical.

A blue film was observed on the surface of some of the devices stressed at 350°C. The intensity of the blue color varied from device to device and over the surface The color appeared to be deeper blue around the emitter junctions, the collector junctions were not observed. After exposure to room air, the blue color faded and eventually was no longer observed The observation of such a colored film during oxidation of a germanium surface has been previously reported [8]

3. Activation Energies Of Accelerated Temperature Reaction

The constant C_2 of Eq. 1 is related to the activation energy of the reaction causing h_{FE} decay For the transistors stabilize baked at 175°C, the median activation energy is 21 7 ± 1.2 Kcal/mole or 0.9 ± 0.1 ev. This is in agreement with the activation energies found by Dodson[3], but it is approximately three times higher than the activation energy determined by Wallmark[6] However, Wallmark studied the oxidation reaction at temperatures of 125°C or less, using transistors not exposed to a prebake. Ligenza[9] shows that the logarithmic oxidation rate can be derived by assuming that the activation energy changes linearly with extent of coverage Therefore transistors exposed to pre-bakes must exhibit higher activation energies when exposed to bakes thereafter, due to a thicker initial oxide film.

Ligenza determined that the maximum activation energy for the logarithmic rate of oxidation is 19 kcal/mole, and the logarithmic rate holds up to several minutes exposure at 250°C. The value of activation energy determined by h_{FE} decay is 14% higher and the logarithmic rate appears to be satisfied at least up to 300 hours at 350°C. Variations of oxygen pressure and processing of the germanium surface could account for some of the discrepancy An extremely important dependance of the activation energy of oxidation is the water vapor pressure of the surrounding ambient The dependance of oxidation effects on water vapor pressure is so

strong that measured variations in oxygen uptake among those studying oxidation of germanium is usually ascribed to water vapor pressure variations Figure 4 shows a dependance of the median normalized h_{FE} decay with package water vapor pressure. With increasing stress temperature, roughly in excess of stabilization bake temperature, h_{FE} decreases more rapidly with increasing package vapor pressure The package vapor pressure was varied from less than 10^{-4} to 10^{-2} mm Hg at 25°C by varying the water loading of molecular sieve mixed in an inert fluid base[4] Note that at temperatures less than the stabilization bake temperature, the usual increase of h_{FE} is observed except for the wettest lot The same test was performed using $BaCO_3$ + Ni (1·2) as the dessicant in an air ambient of - 95°F dew point The result is shown in Fig 5 The package water vapor pressure created by the $BaCO_3$ + Ni dessicant is not known, but it is suspected that the water vapor pressure is less than the driest group of Fig 4 This suspicion is based on the facts that the $BaCO_3$ + Ni dessicated group had the lowest absolute initial h_{FE} , showed the largest percentage increase at temperatures less than the stabilization bake temperature, and showed the least median normalized h_{FE} change at temperatures greater than the stabilization bake temperature

4. Non-Predominant Failure Modes Created During Accelerated Step Stress

Although what appears to be oxidation of the germanium surface is the predominant failure mechanism during accelerated temperature stress, other failures are occurring which are not attributable to surface oxidation One of the non-predominant failure modes is the occurrence of open emitters due to the formation of the $AuAl_2$ intermetallic compound[10] commonly referred to as "purple plague" For example, the incidence of open emitters for lots 1, 2 and 3 were 2, 4 and 10% respectively Thirteen out of a total of 16 open emitters occurred at the 275°C step At the step at which open emitters occurred, a discountinuity in the h_{FE} vs time curve for the given unit is observed The study of the "purple plague" formation on

Fig. 4

VARIATION OF h_{FE} OF MOLECULAR SIEVE DESSICATED TRANSISTORS WITH TEMPERATURE STRESS AND MOISTURE CONTENT. STRESS INTERVAL, 24 HOURS. SAMPLE SIZE, 9 PER CURVE. STABILIZE BAKED AT 150°C.

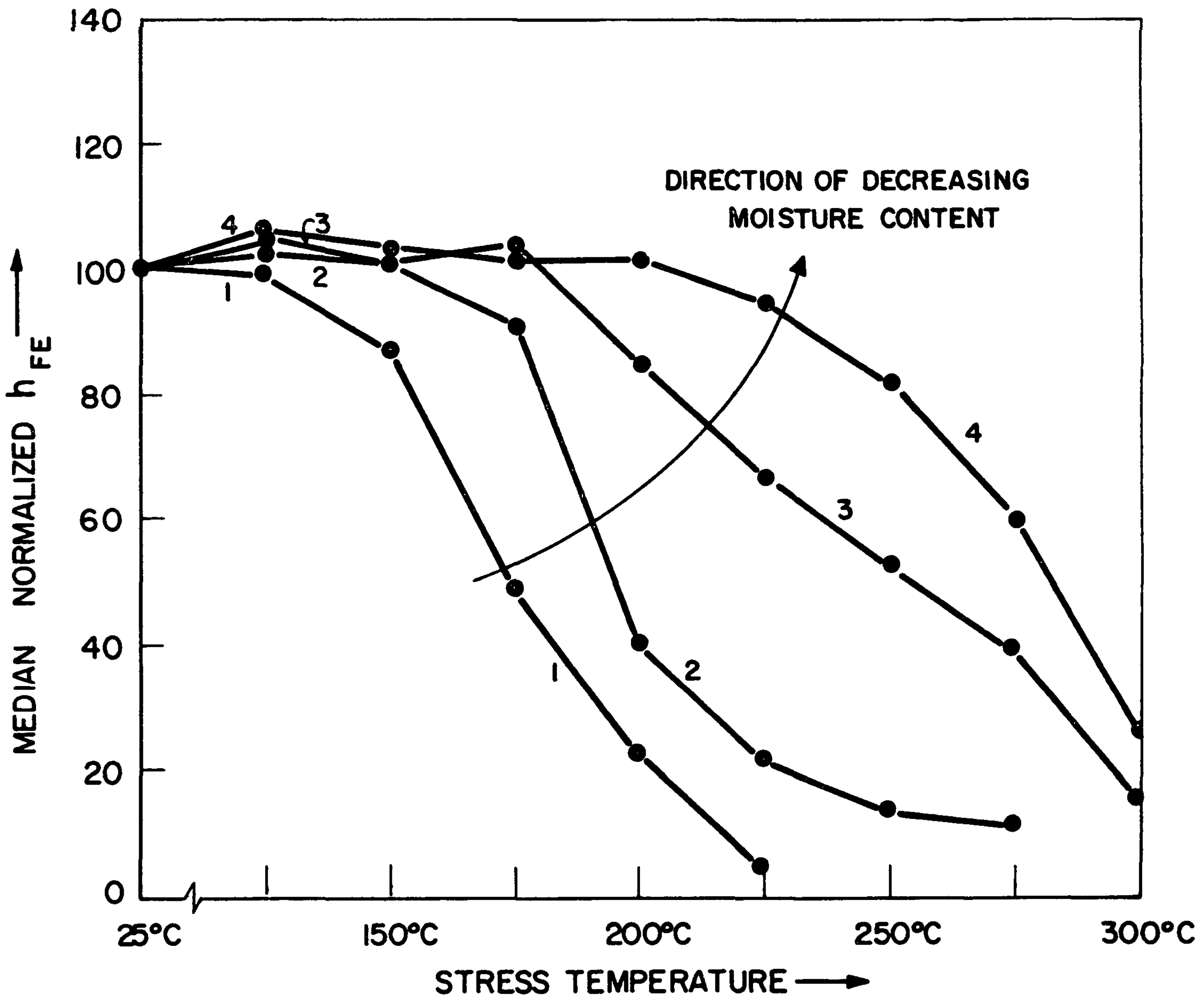
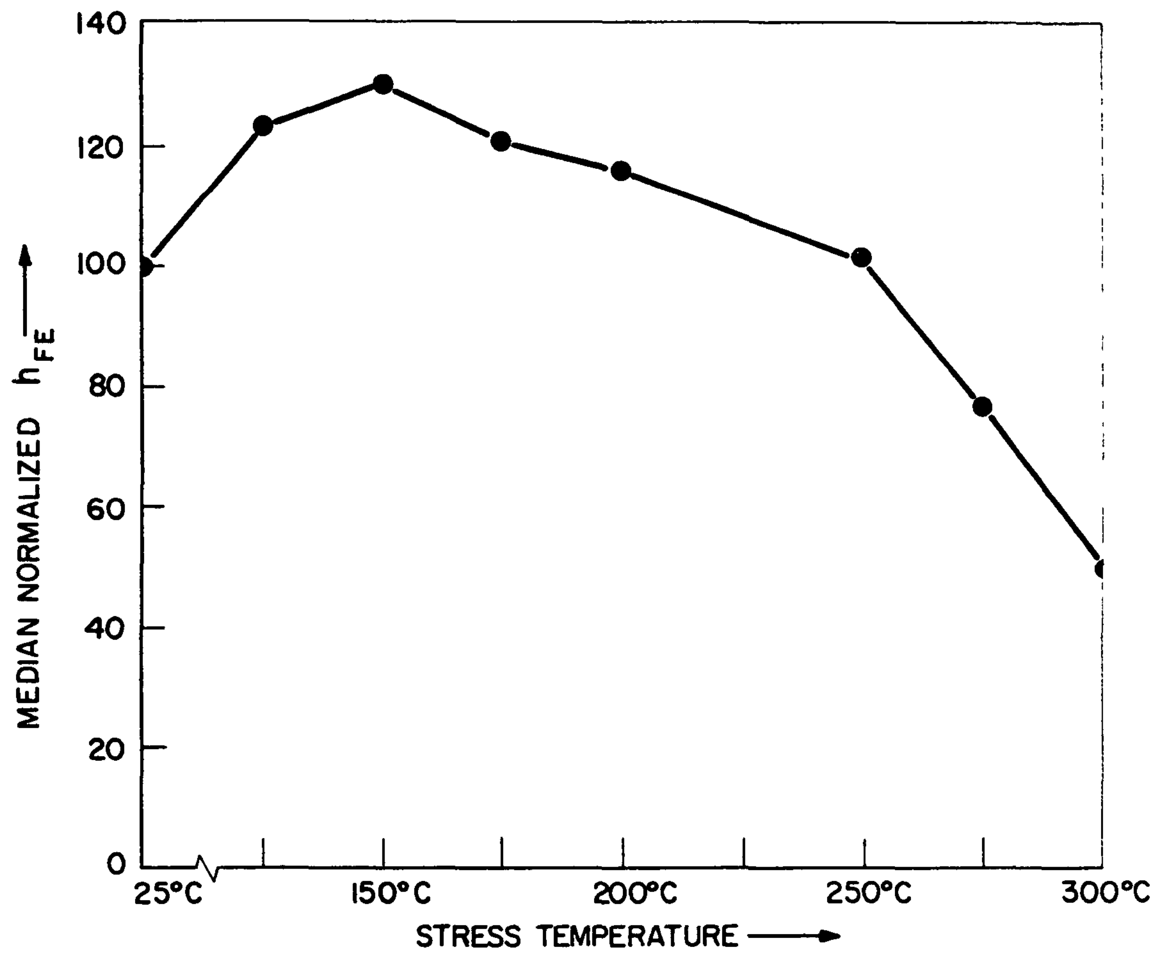


Fig. 5

VARIATION OF h_{FE} OF Ba CO_3 + Ni (1:2) DESSICATED TRANSISTORS WITH TEMPERATURE STRESS. STRESS INTERVAL, 24 HOURS. SAMPLE SIZE 35. STABILIZE BAKED AT 150°C.



parameter change other than actual open emitters is difficult due to other predominant mechanisms causing parameter change both at accelerated and normal temperature stressing. The problem is further complicated by the fact that open emitters due to the "purple plague" formation or poor bonding without "purple plague" can be temporarily or even permanently closed by the application of reverse bias as little as 5V in some cases. Measurements of emitter leakage currents or constant current emitter breakdown voltage may readily heal open emitters. Thus, if these parameters are read prior to h_{FE} or input voltage, the created open emitter goes undetected.

Electrical overstressing during parameter measurement is a constant problem, particularly when reverse junction currents in the order of milliamps are created Electrical overstressing is considered an error rather than a failure mode, but it can be confused with surface changes, especially when only partial damage occurs[11]. Increased activation energies result.

If sufficiently high temperatures are reached or a sufficient amount of time at high temperature is spent the oxidation mechanism takes a new form[9]. The activation energy becomes temperature dependant. This may give some the false impression that a new failure mode is occurring

5. Parameter Changes During Accelerated Power Stressing

Step stress tests as outlined in Tables IV and V were performed. A common base circuit with constant voltage supplies was used. The 5 V circuit was equipped with constant emitter and collector series resistances of 150 and 50 ohms respectively. The 15 V circuit had a 300 ohm emitter series resistance and a 150 ohm collector series resistance

Unlike accelerated temperature stressing, several predominant failure modes were found during accelerated power stressing The major failure modes occurring during the 5 V power step

Table IV

Syl-2017 5V, V_{CB} Power Step Stress Tests. Stabilization Bake, 175^{0}C For 170 Hours.

Lot #	Sample Size	Time on Stress	Initial Power	Power Steps	Final Power
9	100	5 hrs.	250 mw	50 mw up to 700 mw; 100 mw, thereafter	1200 mw
10	100	72 hrs.	250 mw	50 mw up to 500 mw; 100 mw, thereafter	1000 mw
11	100	240 hrs.	200 mw	50 mw up to 300 mw; 100 mw, thereafter	800 mw

Table V

Syl-2017 15V, V_{CB} Power Step Stress Test. Stabilization Bake, 175^{0}C for 170 Hours.

Lot #	Sample Size	Time of Stress	Initial Power	Power Steps	Final Power
12	100	5 hrs.	250 mw	50 mw	350 mw
13	100	72 hrs.	250 mw	50 mw	400 mw
14	100	240 hrs.	200 mw	50 mw	350 mw

stressing were

1 The creating of open emitters by lead wire melting during the last steps of lots 9 and 10

2 The occurrence of collector to emitter shorts through the bulk

3 Parameter degradation similar to parameter degradation during accelerated temperature stress

The only failure mode of lot 12 and the predominant failure mode of lots 13 and 14 of the 15 V power step stressing was the occurrence of collector to emitter shorts through the bulk Lots 13 and 14 also showed parameter degradation

The melting of the thin gold lead wires is expected when power in excess of one watt is applied to a transistor designed for a maximum rating of 150 mw. This mode of failure is not considered a problem

The collector to emitter shorts created during power step stressing were different from the collector to emitter shorts created during temperature step stressing Temperature stressing caused surface shorts with low pinch-off voltages, and etching of the surface caused improvement Power stressing caused bulk collector to emitter shorts such that the emitter and collector diodes were identical. In some cases the emitter diodes were not degraded, in other cases they were completely shorted. Failure analysis of these shorted devices disclosed alloying through the base region similar to that found by Schafft and French[12] When alloying of the aluminum through the base region was not observed, physical bulk damage was found [11].

These collector to emitter shorts are explained by the fact that, during accelerated power stressing, the transistors were operated in a negative resistance region This was determined by the fact that the voltage drop across the emitter series resistance was greater than the emitter voltage supply. The excess voltage

was coming from the collector voltage supply. All of the devices on the 15 V power step stress test were in negative resistance operation, while, during the 5 V power step stress, negative resistance operation was just beginning at 400 mw. Curve tracing of the transistors indicate that, at the power levels attained, the devices were being operated in secondary breakdown Schafft and French[12] have shown that operation of transistors into secondary breakdown causes bulk collector to emitter shorts

For operation in the negative resistance region, power and voltage levels were difficult to control. As a result, a distribution of power and voltage for each step was measured For the 15 V power step stressed transistors in which the collector to emitter bulk shorting was the predominant failure mode, a median power-voltage relation to the number of failures is shown in Table VI.

Another interesting correlation was found for collector to emitter bulk shorting during the 15 V power step stressing The transistors with the highest turn on time and lowest storage time values in the initial distributions were the earliest failures During a 15 V, 250 mw life test for 1000 hours, a decreasing failure rate with time was observed The catastrophic failures were again bulk collector to emitter shorts Of a total of 19 catastrophic failures out of a sample size of 400, all but one were in the upper 50% of the turn on time initial distribution and all but two were in the lower 50% of the storage time initial distribution. No such correlation to switching times was found with 5 V power stressing. This might be explained by the fact that other major failure modes are working during 5 V power stressing In any event, the relation of collector to emitter shorting to switching times must be subjected to further study before concrete conclusions can be drawn However, it has been found that transistors with higher frequency characteristics have invariably lower secondary breakdown power ratings [13]

Parameter degradation was another failure mode occurring during accelerated power stressing It has been previously shown[4]

TABLE VI

(a) Relation of Failures to Median Power and V_{CB}

	Lot#	200 mw	250 mw	300 mw	350 mw	400 mw
	12	-	1	56	14	-
(a)	13	-	2	38	3	42
	14	10	2	50	28	-
	12	-	286 mw	486 mw	580 mw	-
(b)	13	-	281 mw	387 mw	374 mw	690 mw
	14	276 mw	300 mw	431 mw	690 mw	-
	12	-	14.5V	14.5V	14.5V	-
(c)	13	-	14.5V	14.5V	14.5V	14.5V
	14	16.5V	15.5V	14.5V	13.5V	-

that normal circuit operation with a forward biased emitter and a reverse biased collector imposes a thermal stress on the emitter junction while the collector receives a combination of voltage and thermal stresses. Assuming that the same conditions exist during accelerated power stressing, an attempt to generate curves as in Fig. 1, using power rather than temperature as a parameter, was made for the 5V power step stress test This proved to be impossible for the following reasons

1 During the first two steps h_{FE} increased rather than decreased

2. Distributions of power existed for each step rather than a single power level The median power was usually in excess of the programmed power

3 Power steps were increased from 50 mw to 100 mw as shown in Table IV. This was done because failures of more than 70% of the sample were taking too long

As a result, another method of comparing h_{FE} decay was used as shown in Fig 6 Figure 6a shows the continuous normalized h_{FE} decay for the temperature stressed lots 1, 2, and 3 versus accumlated time on stress Figure 6b shows the normalized median h_{FE} change for the power stressed lots 9, 10, and 11 versus accumulated time on stress It is seen that h_{FE} changes during 5 V power step stressing occur in three separate modes The first is an initial increase indicating that applied 5 V power of less than 300 mw does not create an effective temperature at the emitter junction up to 175°C (stabilization bake temperature). In the final steps, junction shorting and lead wire melting predominate In the middle, the region of continuous h_{FE} decay appears similar to the temperature stressed h_{FE} decay However, I_{CBO} behaves differently during temperature and power stressing For example, when h_{FE} decreased an average of 50% during temperature stressing, 15 V I_{CBO} increased an average of 330% During 5 V power step stressing an average h_{FE} decrease of 50% was accompanied

Fig. 6a

h_{FE} VS ACCUMULATED TIME ON STRESS FOR LOTS (A) 1, 2, AND 3 OF TABLE I (B) 9, 10, AND 11 OF TABLE IV.

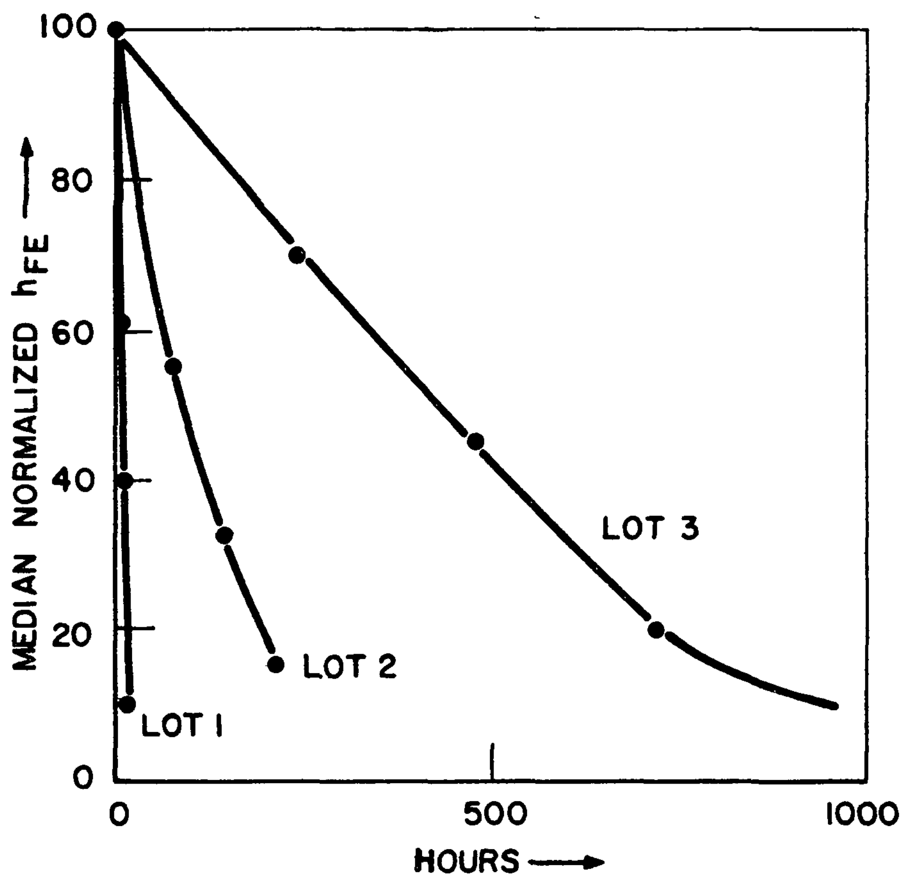
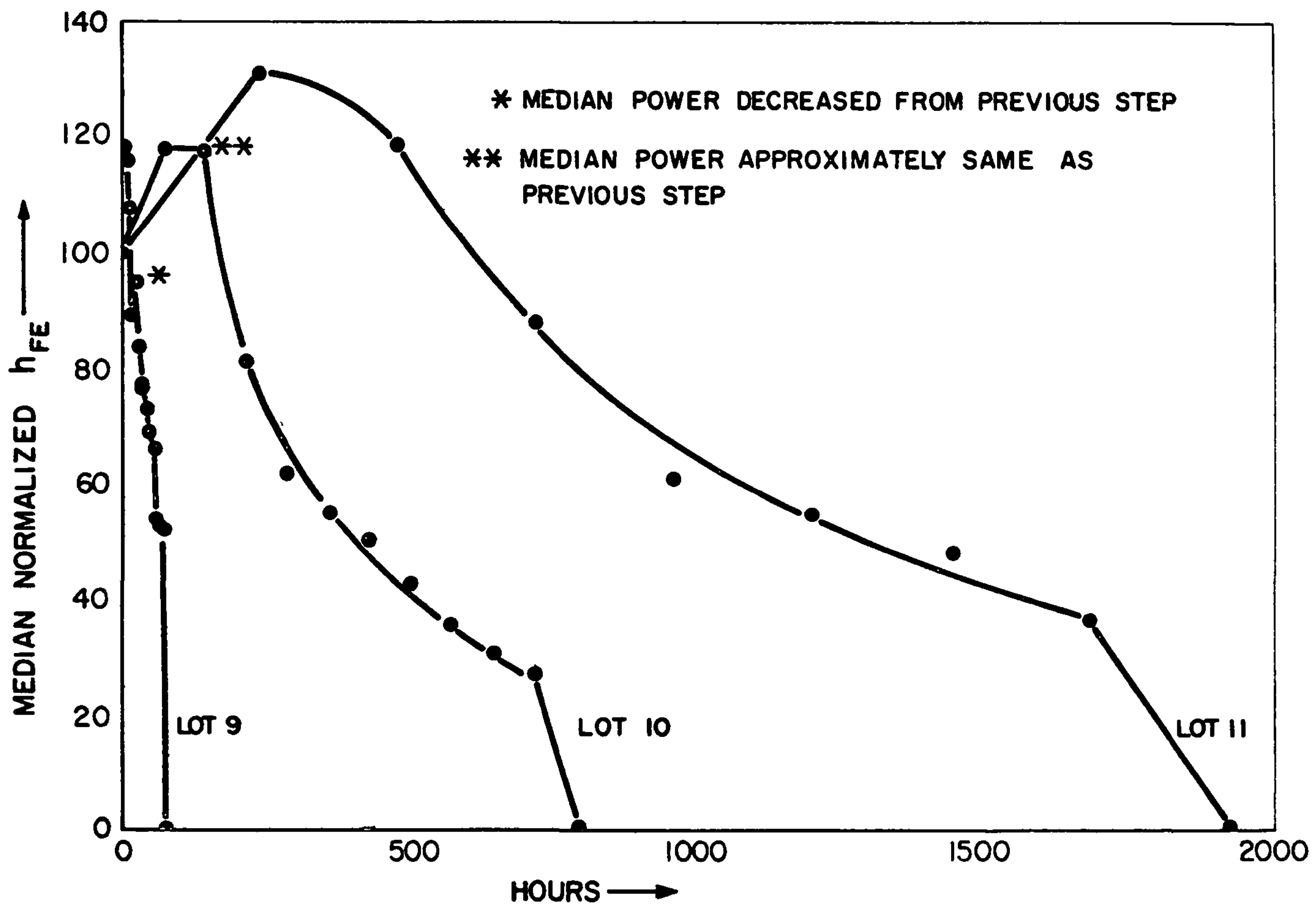


Fig. 6b

h_{FE} VS ACCUMULATED TIME ON STRESS FOR LOTS (A) 1, 2, AND 3 OF TABLE I (B) 9, 10, AND 11 OF TABLE IV. (CONT.)



by an average increase of 15 V I_{CBO} of 40% When h_{FE} has decreased by an average of 65%, 5 V power stressing showed an average increase of 15 V I_{CBO} of 250%, but temperature step stressing showed 15 V I_{CBO} increasing by a factor of more than two orders of magnitude. It might then appear that the continuous h_{FE} decay occurring during power stressing is not due to the same mechanism as the decay during temperature stressing This is shown not to be the case by the data of Fig. 7 and Table VII. The comparison of a sample of 400 transistors life tested during 1000 hours of 5 V, 400 mw constant power with a temperature life tested sample (lot 7) is shown in Fig. 7 Both lots were stabilize baked at 150°C for 170 hours It is seen that the h_{FE} decay during 5 V, 400 mw life testing is of the same form as the 225°C life testing, but that the temperature at the emitter junction generated by 400 mw is somewhere less than 225°C. Table VII shows that, for a 50% decrease of h_{FE}, the increase of 5 V I_{EBO} is comparable, but the change in I_{CBO} is significantly different. These data lead to the conclusion that the reverse field at the collector junction causes a different type of I_{CBO} change than a pure temperature stress would cause

The 15 V power step stressing of Table V showed similar results to the 5 V power stressing except that collector to emitter shorting began to dominate the distribution early in the test Lot 12 showed no change in I_{CBO} or h_{FE} before collector to emitter shorting began to dominate the distribution Lot 13 showed a 12% h_{FE} change accompanied by a 20% 15 V I_{CBO} change before collector to emitter shorting dominated the distribution. Lot 14 showed a 50% h_{FE} change with a 22% 15 V I_{CBO} change before collector to emitter shorting dominated the distribution

6. General Discussion

It has been established that, during accelerated temperature stressing of germanium transistors, a new predominant mode of failure is created. The evidence points strongly to the fact

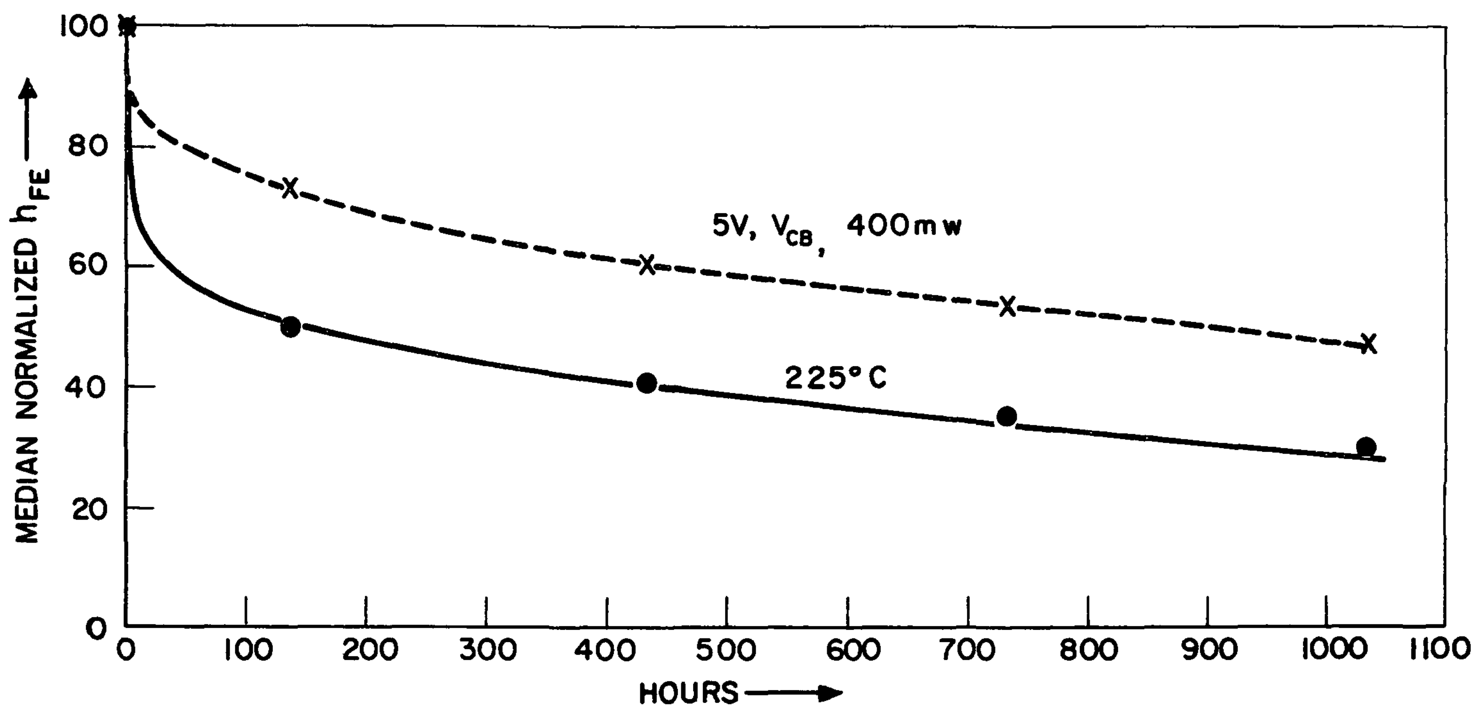
TABLE VII

Comparison of Average Parameter Change for an Equal h_{FE} Change During 225°C Life Test and 5V, V_{CB}, 400 mw Life Test. Stabilization Bake = 150°C for 170 Hours.

Parameter	225°C Life Test (Lot 7)	5V, 400 mw Life Test
h_{FE}	50% decrease	50% decrease
5V I_{EBO}	80% increase	75% increase
15V I_{CBO}	100% increase	40% increase
1V I_{CBO}	100% increase	25% increase

Fig. 7

COMPARISON OF THE h_{FE} DECAY OF A 5V, 400 MW LIFE TEST WITH THE 225^{0}C LIFE TEST OF TABLE III. BOTH GROUPS STABILIZE BAKED AT 150^{0}C.



that this new mode of failure is the oxidation of the germanium surface. If germanium transistors are stabilize baked at temperatures exceeding the maximum temperature rating of the device, the effect of subsequent oxidation on parameter change is negligible within temperature ratings For example, we see from Eq. 2 that it will take more than 10^3 years before a 1% decrease in h_{FE} due to oxidation is observed for PNP transistors stabilize baked at 175°C Increases of h_{FE} much greater than 1% are usually observed for PNP devices life tested at 100°C.

Accelerated power stressing is found to create the same form of parameter change as accelerated temperature stressing, but at the emitter junctions only It appears that either oxidation is inhibited by the high reverse fields at the surface collector junction or a different, field dependent mechanism causing parameter change is occurring As reverse voltage is increased during accelerated power stressing, electrical overstress becomes a predominant failure mode However, electrical overstress should not really be considered a failure mode, but rather abusive use or power circuit design

Since new failure modes are caused during accelerated power temperature stressing, extrapolation of reciprocal temperature or power versus log failure rate or time curves to normal conditions is not vaild for germanium transistors

The accelerated stressing method of reliability testing may have more successful results with heavily oxidized silicon planar transistors where the oxidation mechanism is expected to be negligible However, silicon devices usually have temperature ratings up to 300°C. As a result, only temperatures exceeding 300°C can be considered accelerated stress Accelerated power stressing of silicon devices will run into the same pitfalls that germanium devices have if excessive reverse voltage or power is applied In general, before accelerated stress can be accepted as a failure rate predication tool, it must be proven that the same mode of failure is created at the accelerated stresses as would be

created at the normal stresses.

Accelerated step stressing has some very useful applications not previously considered. They are:

1. A method of determining realistic temperature, power, and voltage ratings.
2. A method of determining when the realistic temperature, power, and voltage ratings have varied because of process changes.
3. A method of determining when different modes of failure from those occurring at normal stress have been initiated. This provides an excellent failure analysis tool for inadvertently overstressed devices.
4. A method of picking out some process changes. However, the reader must again be cautioned. Process changes causing failures at accelerated stress may not affect reliability at normal stresses and, in some cases, may even aid reliability at normal stresses.

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LIST OF SYMBOLS

BV_{CBO}	Reverse collector to base breakdown voltage with emitter open.
BV_{EBO}	Reverse emitter to base breakdown voltage with collector open.
h_{FE}	Common emitter current gain. Always measured at $V_{CE} = 3\,V$ and $I_C = 50$ ma . 30 msec pulse.
I_C	Collector current.
I_{CBO}	Reverse collector to base current with emitter open.
I_{EBO}	Reverse emitter to base current with collector open.
ma	Milliamps
mw	Milliwatts
T	Temperature in ^{o}K
t	Time in hours
V	Volts
V_{CB}	Reverse collector to base voltage.
V_{CE}	Reverse collector to emitter voltage.
μa	Microamps

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LIST OF REFERENCES

1 Peck, D. S., "A Mesa Transistor Reliability Program", The Solid State Journal, pp 25-30, Nov/Dec, 1960.

2. Howard, B. T. and Dodson, G A., "A Method for the Rapid Evaluation of the Reliability of Semiconductor Devices", Bell Telephone Engineering Services on Transistors, 2nd Interim Report, Contract DA36-039 SC85352, pp 17-27, 20 Nov 1960.

3. Dodson, G. A., "Step-Stress Aging of Diffused Germanium Transistors - A Process Study", Bell Telephone Engineering Services on Transistors, 3rd Interim Report, Contract DA36-039 SC85352, pp 12-22, 28 Feb 1961.

4 Partridge, J. and Borofsky, A J., "Some Reversible and More Permanent Effects of Moisture on the Electrical Characteristics of Germanium Transistors - Following Stress", presented at the Symposium on Cleaning and Materials Processing for Electronics and Space Apparatus ASTM, 4th Pacific Area National Meeting, Los Angeles, Oct 1962.

5. Forster, J. H. and Veloric, H. S., "Effect of Variations in Surface Potential on Junction Characteristics", Journal of Applied Physics, Vol. 30, pp 906-914, June 1959.

6. Wallmark, J. T, "Influence of Surface Oxidation on $Alpha_{cb}$ of Germanium PNP Transistors", RCA Review, pp 255-271, June 1957.

7. Brown, W. L., "n-Type Surface Conductively on p-Type Germanium", Physical Review, Vol. 91, pp 518-527, August 1, 1953.

8 Bernstein, R. B and Cubicciotti, D., "The Kinetics of the Reaction of Germanium and Oxygen", J Amer. Chem. Soc., Vol 73, pp 4112-4114, 1951

9. Ligenza, J. R, "The Initial Stages of Oxidation of Germanium", Journal of Physical Chemistry, Vol. 64, pp 1017-1022, August 1960.

10. Bernstein, L, Warren, W. B, and Bender, B. G., "Physical Metallurgy in Semiconductor Device Fabrication", presented at the Electrochemical Society Spring Meeting, May 1960.

11 Borofsky, A J. and Partridge, J., "Achieving More Accurate Judgements of the Reliability of Germanium Transistors", presented at the Symposium on Cleaning and Materials Processing for Space Apparatus, ASTM, 4th Pacific Area National Meeting, Los Angeles, October 1962.

12. Schafft, H. A and French, J. C, "Second Breakdown in Transistors", IRE Transactions on Electron Devices, pp 129-136, March 1962.

13. Chang, Z. F. and Turner, C. R., "Characterization of Second Breakdown in Silicon Power Transistors", RCA Application Note SMA-21.

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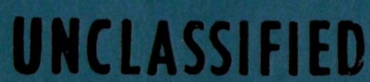
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