file AGC Blk II testing

RAYTHEON

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Delco Electronics Division
General Motors Corporation
Oak Creek Plant
Milwaukee, Wisconsin 53201

Attention: Mr. G. Dumke

Subject: Effects of ACE Equipment Supplying ± 40 Volts onto W-910, W-911 Power Control Lines to AGC

Gentlemen:

This letter is of particular interest to Mr. J. Weber

Introduction

During a review at North American Rockwell, Mr. S. Snipes of NASA/MSC requested an analysis as to what effect a failure in the ACE equipment DAC's (resulting in supplying ± 40 volts onto W-910, W-911 Power Control Lines) has on the AGC.

Specifications

1. The specification governing the interface signals W-910, W-911 for the Command Module is ICD #MH01-01390-200. The specification for these control lines is ± 30 VDC. The command identification for these signals is:

   KG7020 - CGC 4V Stimuli
   KG7021 - CGC 14V Stimuli

2. The Apollo AGC Specification PS 2016007 defines the safety voltage limits in the Voltage Variation Program Fail Test-JDC 5370.

   The safety limits are:

   +4VDC 2.5 to 5.0 VDC
   +14VDC *9.0 to 17.0 VDC

   Each voltage limit has a tolerance of ± 0.2 VDC

   *Not Critical

Analysis

An analysis performed on the power supply circuits indicates that no overstress condition will occur; however, the supplies will saturate.

The outputs at these extremes empirically are:

Control Input	Supply	Output Voltage	
+40	+4VDC	+5.3VDC	(High)
-40	+4VDC	+0.5VDC	(Low)
+40	+14VDC	+17.9VDC	(High)
-40	+14VDC	+3.0VDC	(Low)

Each extreme is analyzed as a single failure.

1. +4VDC - High

   The worst case safe limit is +5.2VDC; however, the supply saturates at +5.3VDC. Under this condition a possible overstress condition can exist in the B-9, B10 modules. Transistor Q3, P/N 2004184-001. SCD 1006323 can see a reverse bias condition between emitter and base of the voltage indicated. The emitter base breakdown voltage B_{Vebo} is specified as 5V min with I_E = 100μa and I_c = 0μa However, on a lot sample basis these transistors received a 48 hours reverse bias burn-in at 6VDC and no reverse bias failures were recorded. Therefore, this condition does not appear to cause overstress.

2. +4VDC - Low

   The myclamp circuit inhibits memory operation if the +4VDC falls below +2.0 $\pm$ 0.1 VDC. No overstress condition would exist.

3. +14VDC - High

   A. The transistors in the Tray B circuits are specified to have a V_{CE} of 35 V max; therefore, no overstress.

   B. The EL voltage is the other concern. The condition under which a DAC failure can occur is during a Voltage Margin Test. However, it is a field procedure to turn the intensity control to minimum per NASA direction. (Also reference - Apollo System Support Technical Bulletin Vol. I, Issue 40, Date 5/22/68.) If this direction is followed, the maximum EL voltage of 300 VRMS, as specified by SCD 1006315, will not be exceeded. Therefore, no overstress will exist.

4. +14V - Low

Erratic operation will occur but is not critical in an overstress sense.

5. The AGC may not execute a program properly due to race conditions established by the voltage extremes.

Conclusion

It is concluded that the AGC will not be overstressed if a failure in the ACE equipment results in supplying ± 40 volts onto W-910, W-911 Power Control Lines. This analysis is also applicable to the ACE-LM interface.

Recommendation

It is recommended that, if possible, protection be provided by the ACE equipment in order to avoid these extremes because of possible tolerance built-ups and to prevent possible program alarms. The safety limits are specified in Item 2 of the specification. The DAC limits would be:

+4V Stimuli	-7.5 to +9 VDC
+14V Stimuli	-16 to +16.5 VDC

Should you have any questions regarding this matter, please contact the undersigned.

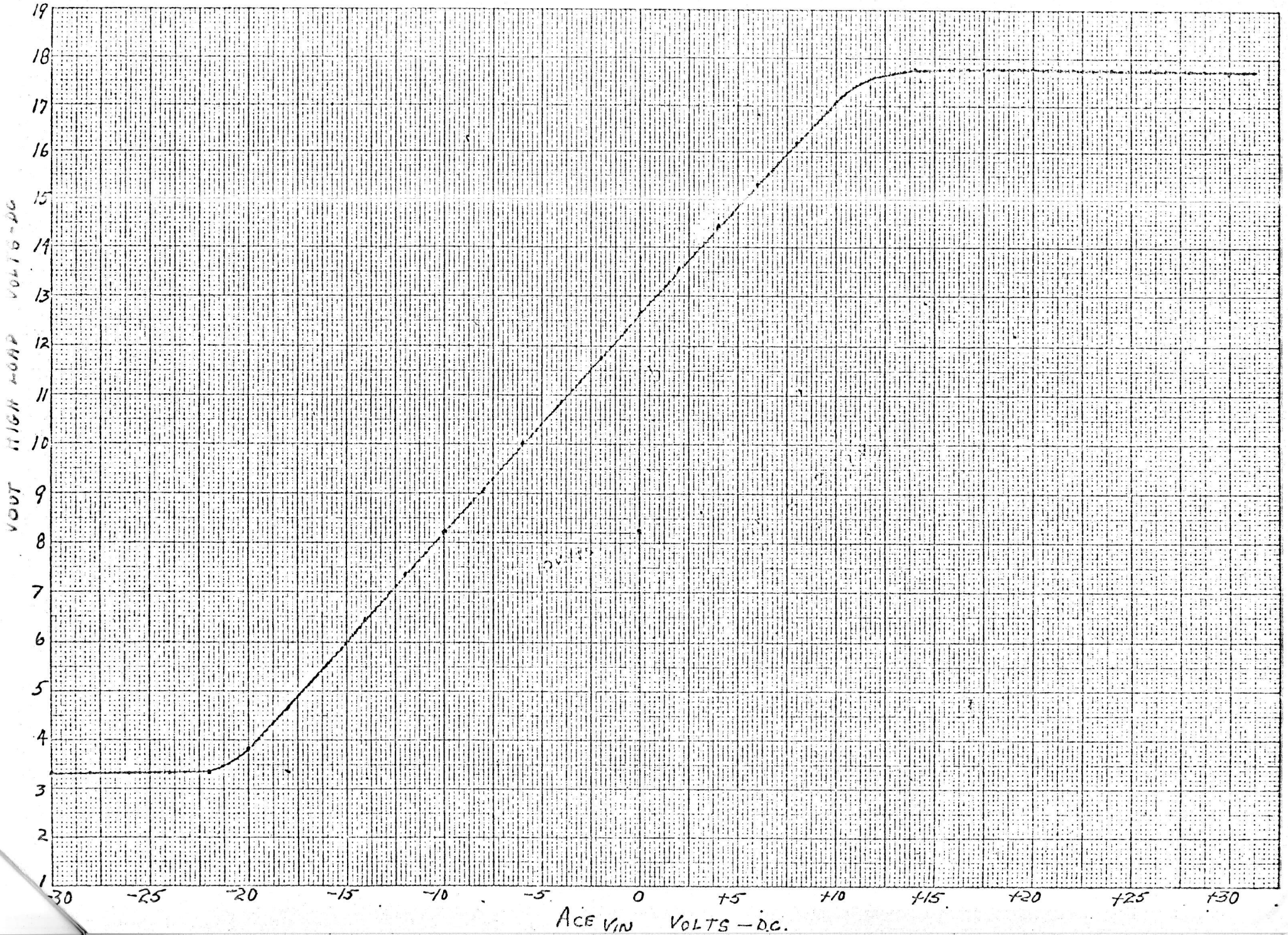
Very truly yours,

RAYTHEON COMPANY

RJS:dmc

Robert J. Storella, Manager
Apollo Contracts

CC: C. Benes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