SINGLE COPY ONLY

Apollo

GUIDANCE COMPUTER AND ASSOCIATED GROUND SUPPORT EQUIPMENT [U]

MONTHLY TECHNICAL REPORT
NO. 10
FR-3-60

RAYTHEON COMPANY
SPACE AND INFORMATION SYSTEMS DIVISION
RAYTHEON

MONTHLY TECHNICAL REPORT NO. 10

FR-3-60

Reporting Period

1 April 1963 - 30 April 1963

Prepared by

RAYTHEON COMPANY
SPACE AND INFORMATION SYSTEMS DIVISION
Sudbury, Massachusetts

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

CONTRACT NAS9-498

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

SECTION I
INTRODUCTION

SECTION I
INTRODUCTION

1.1 GENERAL

This is Monthly Technical Report No. 10 issued in accordance with Work Statement for Industrial Support E-1097, and covers the period 1 April through 30 April 1963. Eighty-eight Technical Directives have been received to date; seventy-three have been accepted; twenty-one have been completed; fifty-two remain active.

To supplement the Master Summary Schedule issued on 20 March 1963, and for the purpose of the monthly report, Raytheon has prepared an Apollo Project Plan which is shown in figure 1-1. This plan is prepared in the NASA format and lists the important milestones of the Apollo Project. This plan will be updated on a monthly basis.

A PERT integration meeting was held on April 4 and 5 at the NASA Manned Spacecraft Center, Houston, Texas. At this meeting, interfaces between the Raytheon fragnets and those of other Guidance and Navigation System contractors were established. Guidance and Navigation System contractors were also requested by NASA to include and identify NASA milestones on their PERT fragnets. These NASA milestones, as well as the interfaces, have been incorporated into the Raytheon fragnets and are currently being reported to NASA.

During this reporting period, a new PERT network for the AGC Oscillator was written and submitted to MIT/IL. The PERT network for the dc-dc converter (now called the Switching Regulator) has been revised to reflect current thinking on this unit and submitted to MIT/IL. New

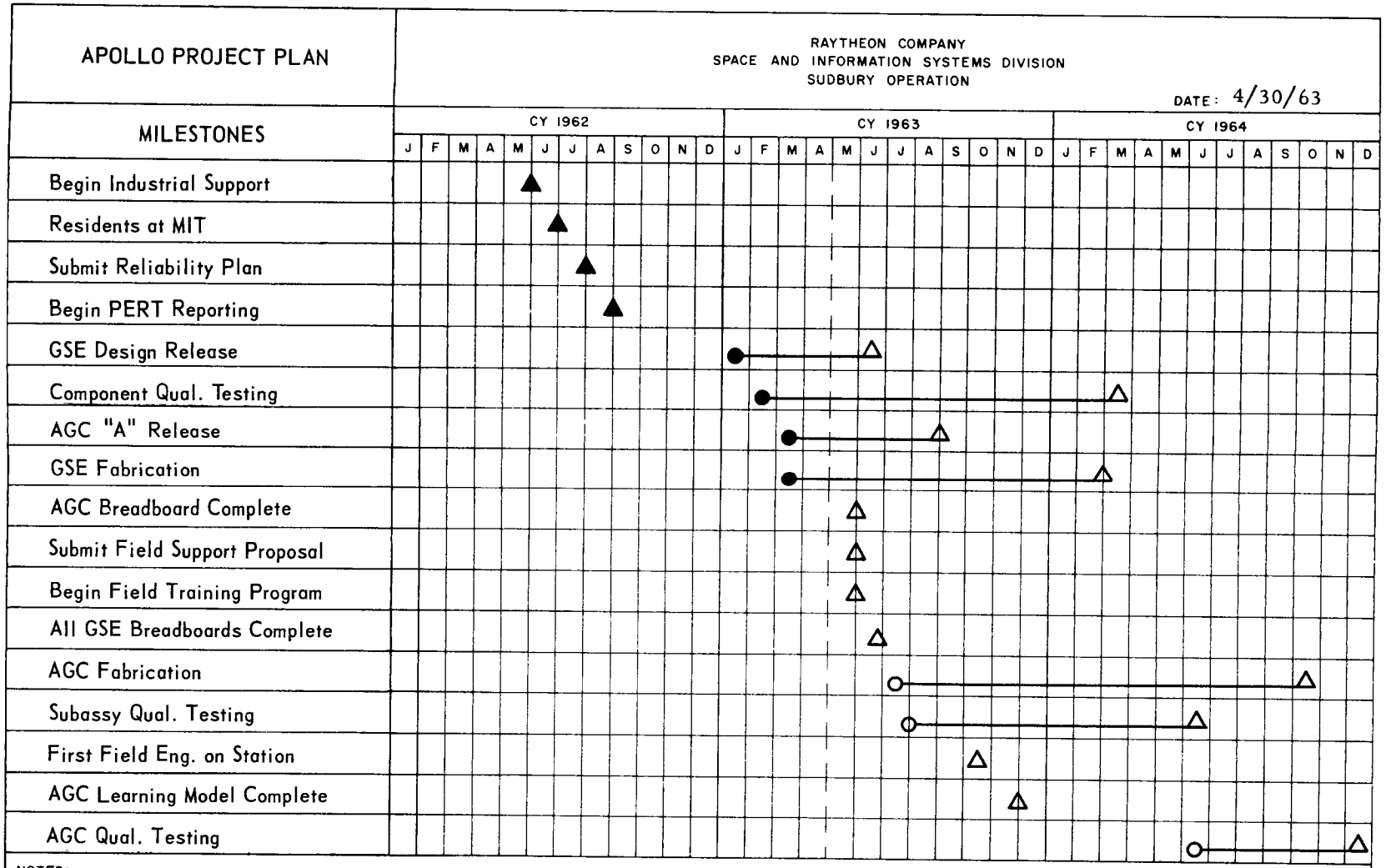

Figure 1-1. Raytheon Apollo Milestone Chart

fragnets are presently being written for: AGC 4B; AGC 7, 8, and 20; and the remaining units of GSE. These fragnets will be submitted to MIT/IL in May.

SECTION II
APOLLO GUIDANCE COMPUTER

SECTION II
APOLLO GUIDANCE COMPUTER

2.1 INTRODUCTION

The Apollo Guidance Computer (AGC) is a special design general-purpose parallel-operated digital control computer. Wired-in programs carry out specific control actions automatically. Access to the computer is through the Display and Keyboard which allows the astronaut to control computing actions.

2.2 GENERAL DESCRIPTION

The computer characteristics are as follows:

(1)	Word Length	16 bits (15 + parity)
(2)	Number System	ONEs complement with overflow correction
(3)	Wired-in Memory (core-rope)	12,288 words
(4)	Erasable Memory (coincident-current core)	1008 words
(5)	Clock Rate (Action rate)	1 Mpps
(6)	Regular Instructions	11
(7)	Involuntary Instructions (interrupt increment)	8
(8)	Interrupt Options	5
(9)	Memory Cycle Time (MCT)	11.7 μsec
(10)	Add Time	23 μsec
(11)	Double Precision Add (X + x) + (Y + y) = (Z + z)	23$\frac{1}{2}$ μsec
(12)	Multiply Time	93 μsec

(13)	Double Precision Multiply	780 μsec
(14)	Number of Counters (input data)	20
(15)	Aggregate Input Rate (instructions of 1/2 speed)	43 kpps
(16)	Input Lines (1 bit per line)	60
(17)	Output Lines for Display	18
(18)	Output (pulsed) Lines for Control	22
(19)	Telemetry	Single error correcting pulse train asynchronous to computer timing

With the exception of the storage portion, all logic flow in the AGC is performed by combinations of three-input NOR gates. The computer uses positive logic, which means that a positive voltage level at the output of the storage elements represents a binary ONE stored.

AGC storage is divided into three types: fixed, erasable, and temporary. See figure 2-1.

Fixed storage consists of three "core-rope" memory elements. A core-rope is a unique method of storage in which the pattern of wiring determines the word stored. Since the pattern of wiring is, necessarily, electrically unchangeable, fixed memory always contains the same words for read-out. The total capacity of fixed memory is 12,288 words, each of which is given an address in octal notation. The S register in conjunction with the Bank (BNK) register is used for memory addressing. The Selection Logic (SL) network decodes the contents of S and BNK to read out the desired word.

Erasable storage by definition is destructive on read-out and consists of a coincident-current core matrix with a total usable capabity of 1008

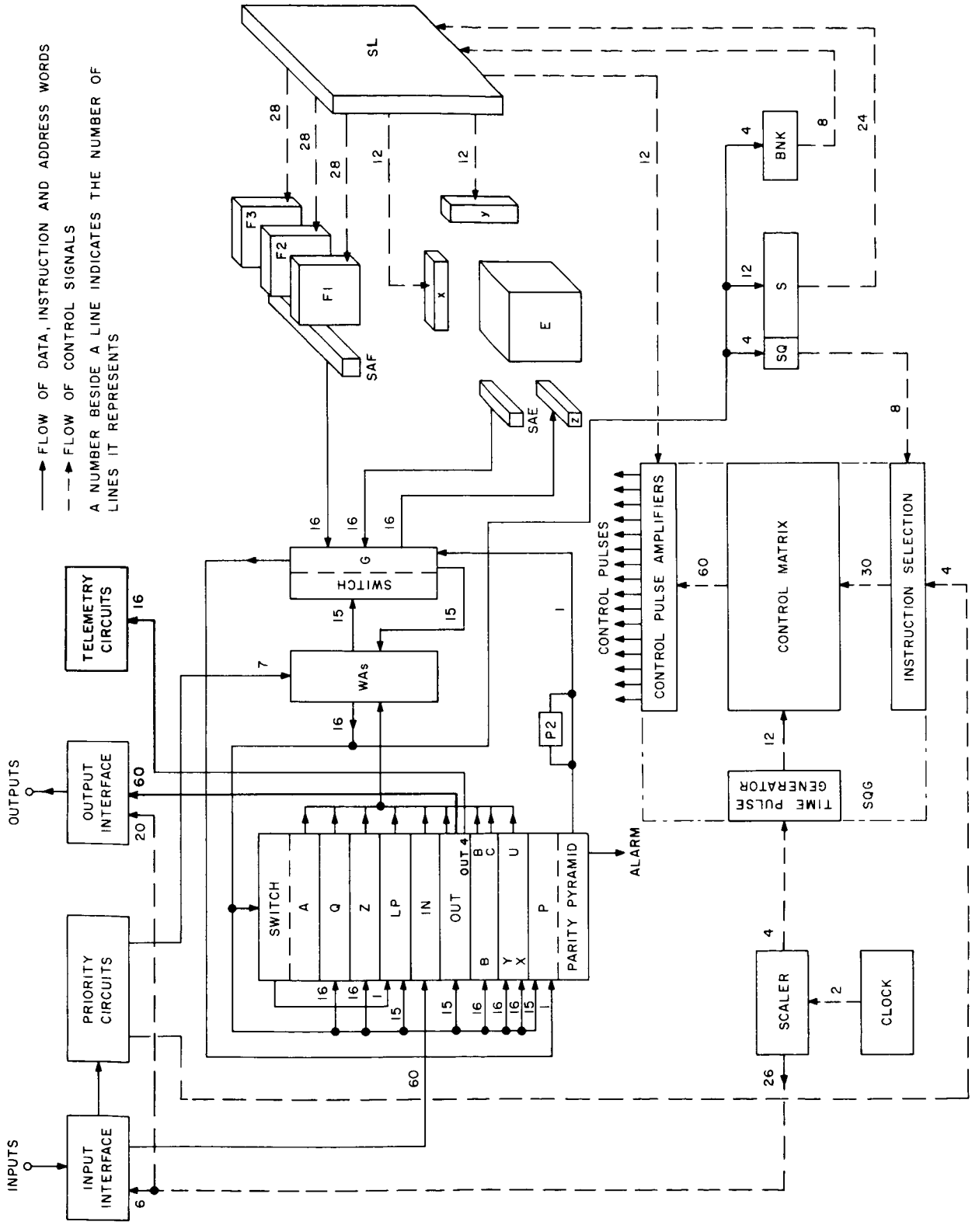

Figure 2-1. AGC General Block Diagram

words. Only the S register is required to address the erasable memory. As before, the S contents are decoded on SL to provide access to the desired word.

Temporary storage consists of 20 flip-flop central registers which make up the operational portion of the computer. The particular functions of the central registers (A, Q, Z, etc.) will be explained later. As a group the central registers are used to carry out mathematical operations. They have the quality of nondestructive read-out and therefore can be used as temporary storage locations. In fact 14 of these central registers are addressable via the S register.

The addressable central registers are A, Q, Z, LP, BNK, all Inputs, and all Outputs. The nonaddressable central registers are B, X, Y, SQ, S, G, and P.

2.2.1 SEQUENCE GENERATOR

The function of the sequence generator is to carry out a multi-instruction program with proper timing. In other words the memories and the central registers must be written into and read out of in the proper sequence to insure that correct results are obtained. The sequence generator consists of an Instruction Selection network which decodes the contents of the SQ register to determine the order code of the instruction to be executed, a control matrix which ANDs in instruction with the time pulse train to produce the read, write, and test pulses required for execution of the instruction.

2.2.2 CLOCK

The crystal-controlled clock oscillator operates at 2.048 mc with an

accuracy of about 1 part in 10^7. The clock rate is one binary division of 2.048 mc (1.024 mc) and provides the time reference for the entire spacecraft. The clock rate is used as a reference for an elapsed time indicator, drives the scaler which controls the output drive rates, and references the Timing Pulse Generator which determines the action times for sequence generator operation.

2.2.3 INPUT-OUTPUT INTERFACES

The input-output interfaces are the only connection that the computer has with the spacecraft. The interfaces route the input data, which may be either incremental or discrete binary digits, to the proper locations. Thirty input lines are provided for incremental input data which must be counted on one of 20 incremental counters located in the erasable memory. Some incremental input pulses require positive incrementing, some negative, and some a shift (or a shift and add one). Each input pulse is stored in the priority circuits which automatically address the proper counter and cause the sequence generator to increment, decrement, or shift the contents of that counter (depending upon the input requirement) as soon as permissible (the interruption of an instruction is not allowed). If more than one such input is present, the priority chain decides upon the sequence of handling.

Binary input digits go directly to the IN registers via 60 lines. Some are fed to the interrupt priority circuits to interrupt a program being executed in favor of a program of higher priority. The outputs from OUT 0 through OUT 3 consist of 60 signal lines of which 40 are used; 18 are discrete outputs for display, and 22 are for pulsed control outputs under program control. Such outputs as ± PIPA (X, Y, and Z) drive rates are supplied from the output registers. Telemetry data is generated as a sixteen bit word in register OUT 4 which is coupled directly to the telemetry programer.

2.2.4 WRITE AMPLIFIERS

Communication, within the computer, is accomplished on sixteen write amplifiers which are multi-input NOR gates connected to all input and output sides of all registers. Each write amplifier carries one bit from point to point in the process of READING a register or WRITING into a register. Shifting of words within a register is accomplished by different connections of the write amplifiers and special enable gates. By definition, a positive voltage state on the input to the write amplifiers represents a binary data bit with value ONE.

2.2.5 POWER

Power is supplied to the AGC by three internal power supplies; a 13 vdc supply for the clock, a 3 vdc (A) supply for the scaler and other timing circuits, and a 3 vdc (B) supply which powers the main logic system within the computer. By turning off the 3 vdc (B) supply when the computer is not required to perform problem solution (such as during midcourse) the timing can still be maintained and a large amount of power drain can be avoided. Total power drain on the three supplies is about 100 watts.

2.2.6 PHYSICAL CONFIGURATION

Physically, the AGC is mounted in a frame structure which is about 9 inches high, 20 inches wide, and 25 inches deep. The logic circuitry is constructed in "stick" form, with 120 micrologic units in each stick, and a plug on the bottom. The sticks plug into pull out drawers, called trays which, in turn, plug into the frame structure. The frame structure is set into the control panel in such a manner, that the astronaut may remove trays for possible stick replacement.

2.2.7 DSKY

The only unit which is actually part of the AGC yet mounted externally is the Display and Keyboard (DSKY). The display portion gives the operator visual indications of various malfunctions such as parity error, power fail, etc. The Keyboard allows the operator to insert order codes and addresses (VERBS) and/or data (NOUNS) thereby allowing him to start the computer on a desired fixed program or to insert a small program in erasable memory. The MARK on the Optics Panel and the ENTER button on the DSKY allow Keyboard use. If either button is pressed, the computer automatically stores all relevant information about the present program and then gives control to the Keyboard. The program stored remains on "hold" until the operator releases control of the Keyboard.

An abstract representation of the machine organization is given in figure 2-2.

2.3 BREADBOARD COMPUTER AGC 4A

Construction of the AGC 4A breadboard is proceeding on schedule. Thirty-five logic sticks have been constructed, tested, and installed in the cabinets. Wiring of the interconnection panels, and testing of the fixed and erasable memory cycle timing has been completed. Tests are presently being conducted on the sequence generator.

The memory section of the breadboard computer is being designed and circuits for the memory sticks are being fabricated. Each fixed memory stick will contain two quarter ropes. Erasable memory sticks will be fabricated as soon as the necessary information becomes available.

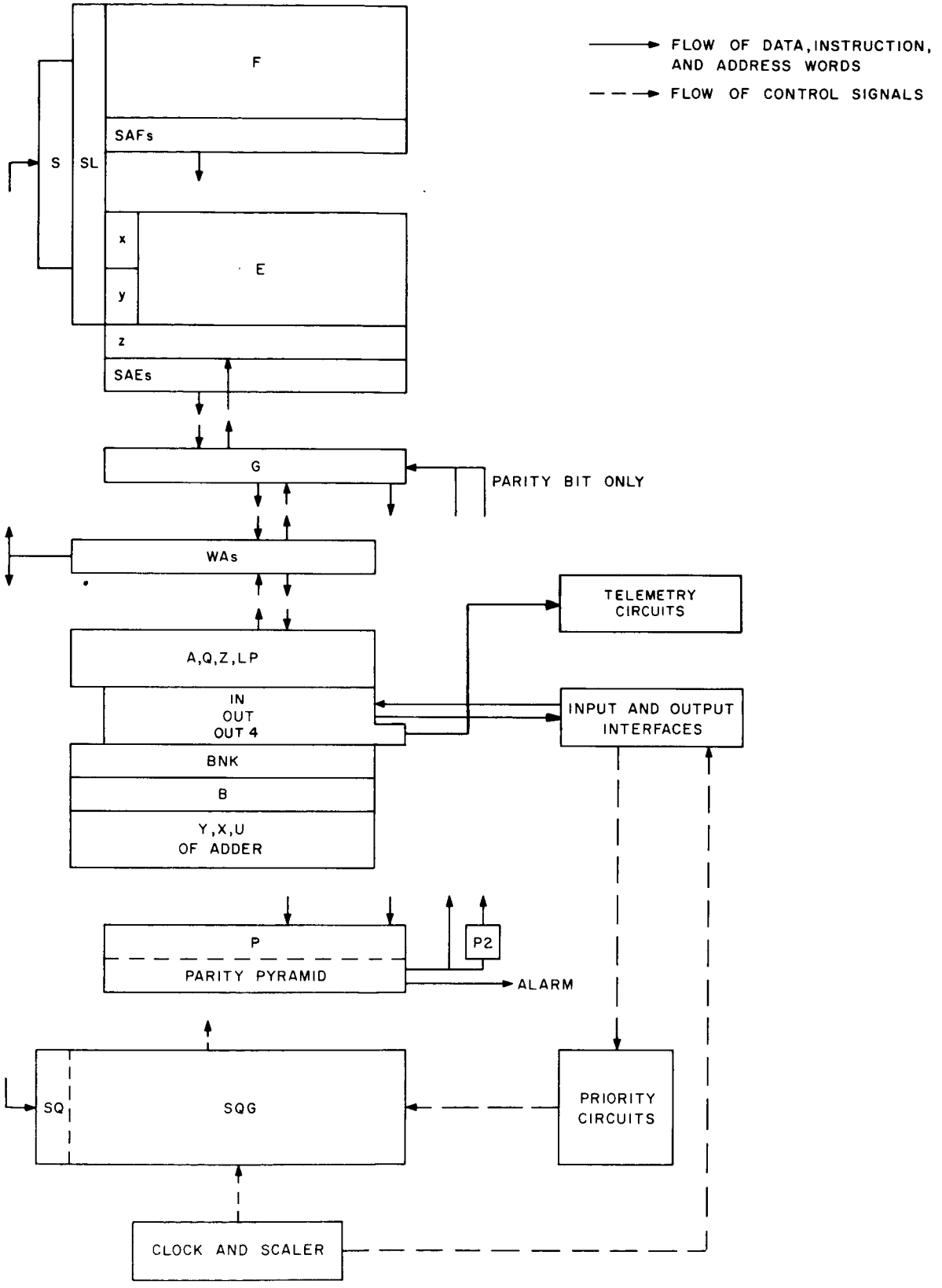

Figure 2-2. Machine Organization

Fabrication of a monitor for communication with the AGC4A breadboard has been completed. The monitor will provide the capability to write into or read out of any addressable register, monitor the write lines at any action time, and monitor any desired output from the breadboard. The monitor will be used to perform functional tests on the breadboard computer until the Computer Test Set is checked-out.

The combined diagnostic and exercising program for the AGC 4A breadboard has been corrected and modified. The program is formulated in a series of separate flow charts, each flow chart being an independent program in itself. Each independent program can be joined to another independent program or arranged to loop within itself. The flow charts are presently being coded and the programs will be used as a means to checkout the breadboard computer.

2.4 PROTOTYPE COMPUTER AGC 4B

The first prototype Apollo Guidance Computer, AGC 4B, will be functionally identical with AGC 4A, and will be packaged as described in Apollo Quarterly Technical Report No. 3. Originally intended as a learning model it is now scheduled to be shipped to support AGE 5 until AGC 5 is completed. The prototype will be updated periodically as more information becomes available on the final configuration.

At present, sixteen arithmetic and some driver sticks are being fabricated for AGC 4B. All electrical and mechanical parts for stick fabrication have been received, with the exception of the header housing assembly.

2.5 MATRIX FABRICATION EQUIPMENT

All matrix fabrication equipment has been refined to incorporate the twelve-channel matrix capability. A statistical analysis of weld settings and weld strengths is being conducted to determine optimum weld settings which furnish the most consistent and reliable welds in compliance with Apollo standards. Several test matrices will be fabricated for this evaluation.

2.6 IN-PROCESS WELD MONITOR

A breadboard version of an In-Process Weld monitor has been constructed. The basic principle of the monitor is to provide weld energy checks at three points on the welding discharge curve to ensure that the energy delivered to a weld is within certain predetermined limits. The breadboard version performed satisfactorily and as a result a go/no-go read-out device has been designed and is presently being assembled. This device will provide an automatic weld evaluation capability for use with all automatic welding equipment.

SECTION III
GROUND SUPPORT EQUIPMENT

SECTION III
GROUND SUPPORT EQUIPMENT

3.1 INTRODUCTION

The Ground Support Equipment for the AGC which is being designed and fabricated by Raytheon must meet the following requirements: (1) independently checkout the AGC, (2) enable performance of open loop tests on IMU, CDU, and PSA, (3) check the AGC oscillator, and (4) check the AGC, when operating as part of the G & N system, prior to installation in the spacecraft. In order to implement the above requirements, Raytheon has designed the Computer Test Set, Computer Simulator, and Computer Calibration Equipment. With these three pieces of equipment it will be possible to perform diagnostic tests on the AGC system during subsystem and system tests, and analyze any malfunction which might occur.

3.2 COMPUTER TEST SET

The Computer Test Set (CTS) consists of a two-bay console and an auxiliary single-bay console. The two-bay console houses twelve units of test equipment as well as three power supplies and is used to evaluate dynamic operation of the AGC during system tests. The CTS will operate in conjunction with the System Checkout Equipment to perform system tests on the Guidance and Navigation System. It will connect to the AGC and Guidance and Navigation System through appropriate interface circuitry and will provide direct program control for monitoring the special and central registers of the AGC and for some key logic functions associated with the AGC internal program control.

The single-bay console contains two Display and Keyboard panels (DSKY), a power control panel, temperature control plate, and a 28 vdc power supply. Self-operating, this console is capable of performing some subsystem tests.

The AGC will be mounted on the temperature control plate which simulates the temperature variations of the computer in flight. The dc power supply provides the operating voltages for the AGC under test. The power control panel provides means of selecting operating voltages and temperatures of the temperature control plate. Since the two Display and Keyboard panels operate in conjunction with the computer during flight, all three are tested simultaneously during system and subsystem tests.

The single-bay console when combined with the two-bay console is capable of performing complete subsystem tests on the AGC. The CTS will provide the logic, hardware, and commercial equipment required for loading programs or data into the AGC, provide for signals into the AGC inputs, and provide for complete test of AGC operation.

The breadboard computer test set is being fabricated in four cabinets. Two cabinets will house commercial equipment and the remaining two will house logic plates and interconnection wiring. The test set will contain ten logic plates and two interconnection plates. Programs for wirewrapping the logic plates have been written; four have been completed. Two logic plates have been wirewrapped and successfully tested. All commercial equipment has been installed in the cabinets and components are being mounted on front panels. Three hundred breadboard modules have been fabricated to date; four hundred are in process and are expected to be completed in May. Testing of the breadboard test set will begin as soon as possible.

3.3 COMPUTER SIMULATOR

The Computer Simulator is a compact, slide-mounted logic drawer, containing three vertically-mounted logic plate assemblies, a vertically-mounted dc power supply assembly, a hinged interconnection plate, and a hinged front panel. The basic structure, designed to fit into a standard 19-inch rack, consists of a wrap-around chassis 17 inches wide, 10 inches high, and 24 inches deep, exclusive of front panel. The front panel is 12-1/4 inches high and 19 inches wide and provides radio frequency interference (RFI) shielding. Ducts are provided in the base of the chassis to permit cooling of the drawer contents.

The Computer Simulator produces drive rates identical with those of the AGC by generating a bi-phase clock frequency, dividing it, and modifying the results of the division to produce the desired outputs. The simulator contains circuits for the selection of inputs to the Guidance and Navigation (G & N) Subsystem. These circuits utilize the pulse trains generated by modifying the clock output to provide one of three specialized input signals to the G & N Subsystem. The choice of which one of the three to be used is the decision of the operator and is manually selected through front panel switches. Provisions are also included to permit operation of the simulator from a remote location.

The breadboard Computer Simulator and Computer Simulator No. 3 have been revised to reflect the earlier changes required by MIT/IL. New changes received from MIT/IL regarding Computer Simulator No. 3 require changes to the wiring, front panel, and power supply. Appropriate drawings of the simulator have been revised to incorporate these changes.

Assembly of the prototype Computer Simulator is in process. The majority of the cables have been fabricated. Modules for the simulator are being constructed. To ease the processing problems encountered in welding to beryllium-copper, connector blades with a brazed-on nickel section at the module end are being used to allow nickel-nickel welds. Over-all module reliability also results. Testing of the modules and the prototype simulator will begin shortly.

3.4 COMPUTER CALIBRATION EQUIPMENT

The Apollo Guidance Computer Calibration Equipment consists of five units of test equipment capable of accurately calibrating the AGC crystal oscillator frequency to within 1 part in 10^9. The Calibration Equipment consists of a modular-constructed single rack console mounted on casters. Rack-mounted in the console is a digital recorder, counter assembly, control and interface panel, VLF comparison receiver, and an oscillator. An antenna mounted on the top of the console has been replaced with a loop antenna external to the console to increase the RF signals for the VLF receiver.

An 18 kc or 20 kc signal is detected by the receiver and sent to a frequency synthesizer which produces a 100 kc signal that is fed to the phase comparator. A frequency standard of 1 mc is divided down to 100 kc, fed through the resolver and then to the phase comparator. These two 100 kc signals are compared for phase relationship. If there is a phase error, a signal is produced that activates the servomotor to drive the resolver. This resolver drives a digital recorder that indicates how much error there is in the phase of the standard. When an error exists, it is corrected by means of a manual control located on the frequency standard. It is assumed that the incoming 18 kc signal is much more accurate than the signal from the frequency standard;

therefore, any error signal produced is due to the standard unit changing frequency. The 1 mc output of the calibrated standard is used as the time base of an eight stage counter. The AGC oscillator output (2.048 mc) is fed into this counter. The output of the counter is fed through a printer that records the frequency of the AGC oscillator. Thus, by calibrating the frequency standard with the 18 kc or 20 kc standard, the frequency and aging characteristics of the AGC oscillator can be determined.

Fabrication of the Computer Calibration Equipment has been completed. Debugging is in process and will be completed shortly. Test specifications are in the process of being written.

SECTION IV
FACTORY TEST EQUIPMENT

SECTION IV
FACTORY TEST EQUIPMENT

4.1 INTRODUCTION

Various tests are required during fabrication of subassemblies and assemblies for AGC and GSE equipments. To satisfy all test situations, it was necessary to design factory test equipment. For this reason Raytheon instituted a Factory Test Plan Board. The purpose of this board was to generate a plan depicting the sequential testing from the component level through the final acceptance test of AGC and GSE.

The GSE Factory Test Plan (figure 4-1) specifies the inspection and electrical tests required during the manufacturing process, including incoming inspection. It provides the basis for fabricating the test equipment and generating test procedures necessary for the implementation of the Factory Test Plan.

The AGC Factory Test Plan (figure 4-2) specifies the inspection and electrical tests required during incoming inspection, screening and burn-in and assembly. It also defines the test stations and provides the basis for fabricating the test equipment and generating test procedures necessary for the implementation of the Factory Test Plan. The Factory Test Plans will be continually updated under the control of the Factory Test Plan Review Board, insuring that the Factory Test Plans will be effective planning documents.

4.2 SENSE AMPLIFIER TESTER

The Sense Amplifier Tester has been modified to facilitate measurement

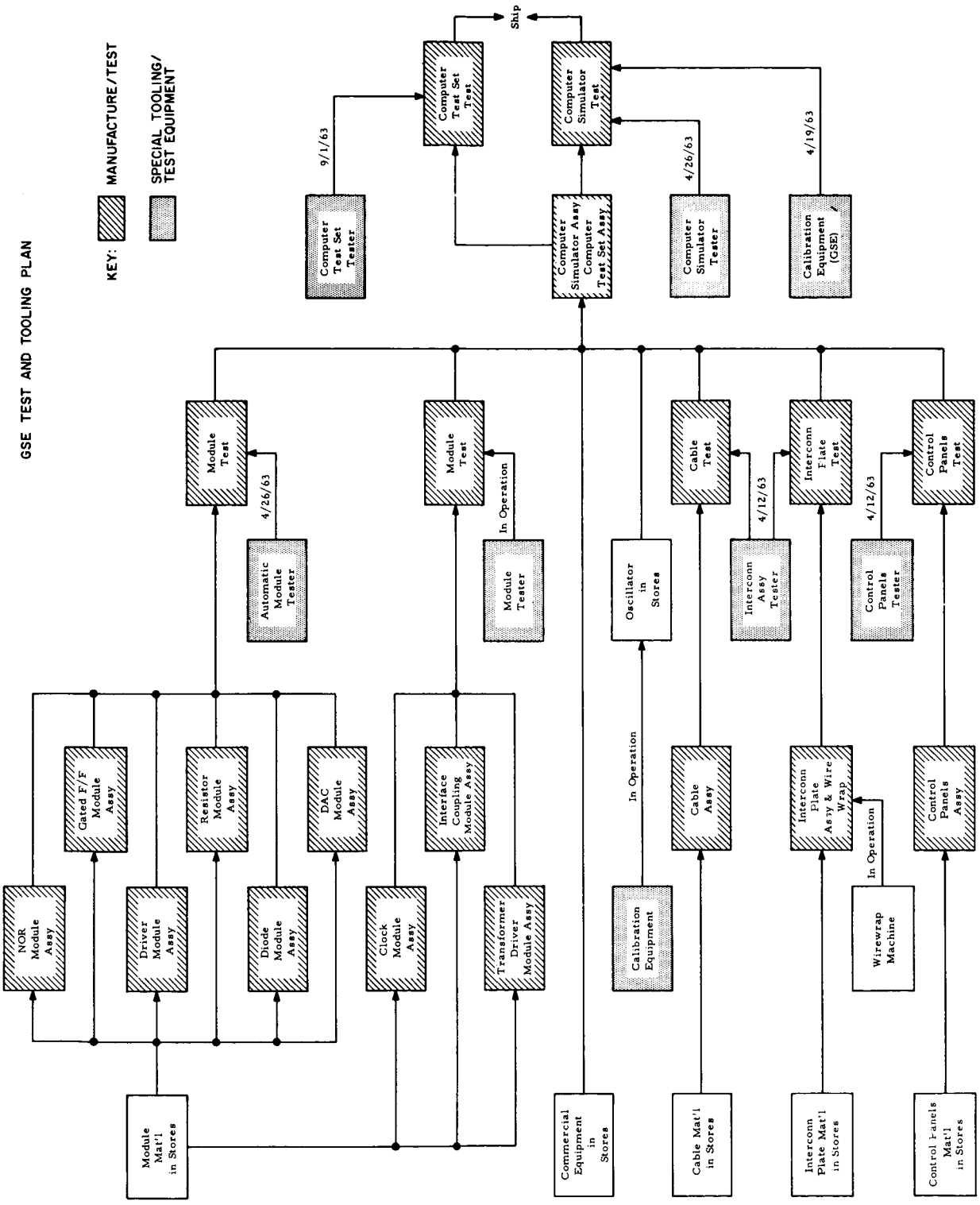

Figure 4-1. GSE Factory Test Plan

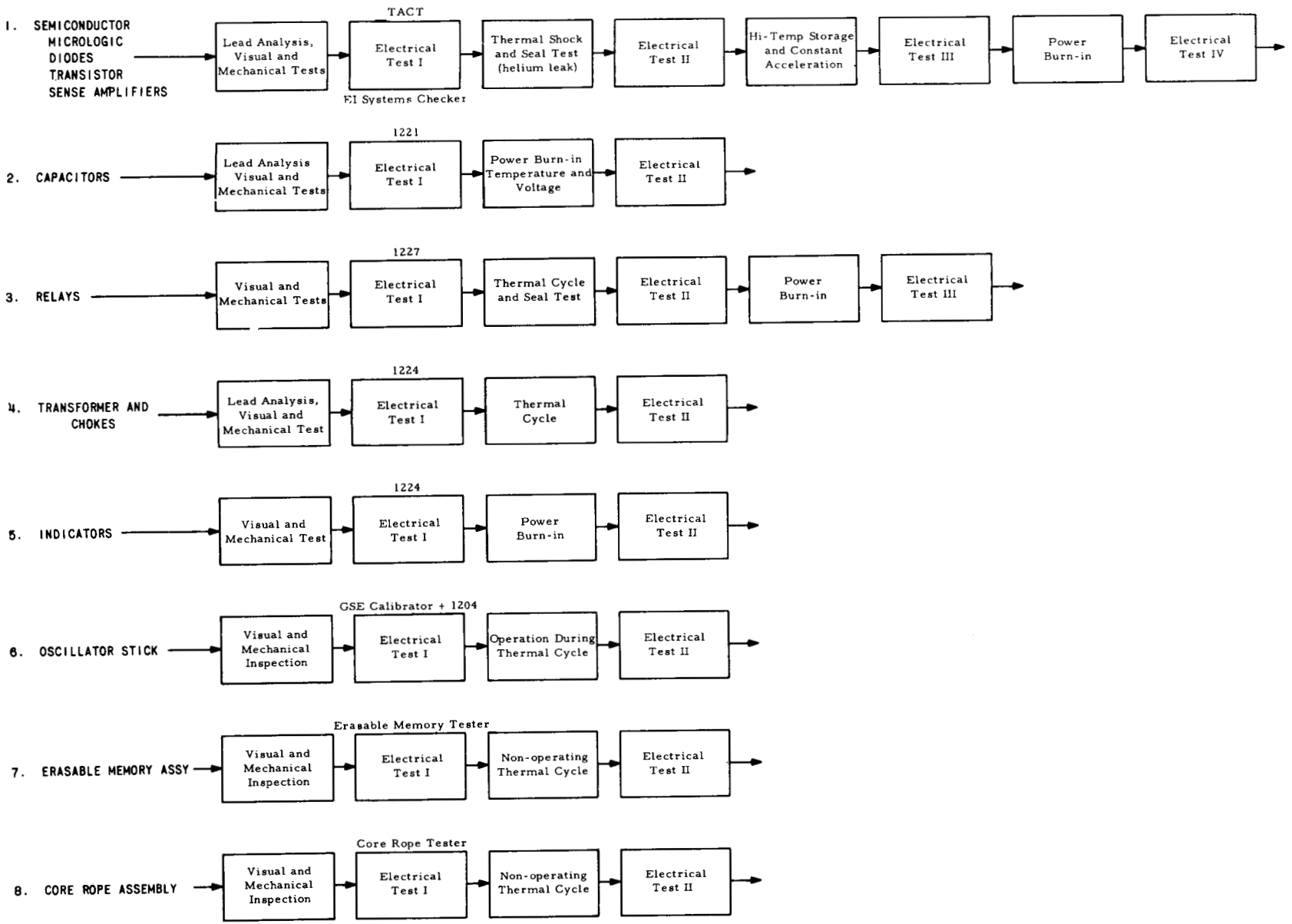

Figure 4-2. AGC Factory Test Plan (Sheet 1 of 2)

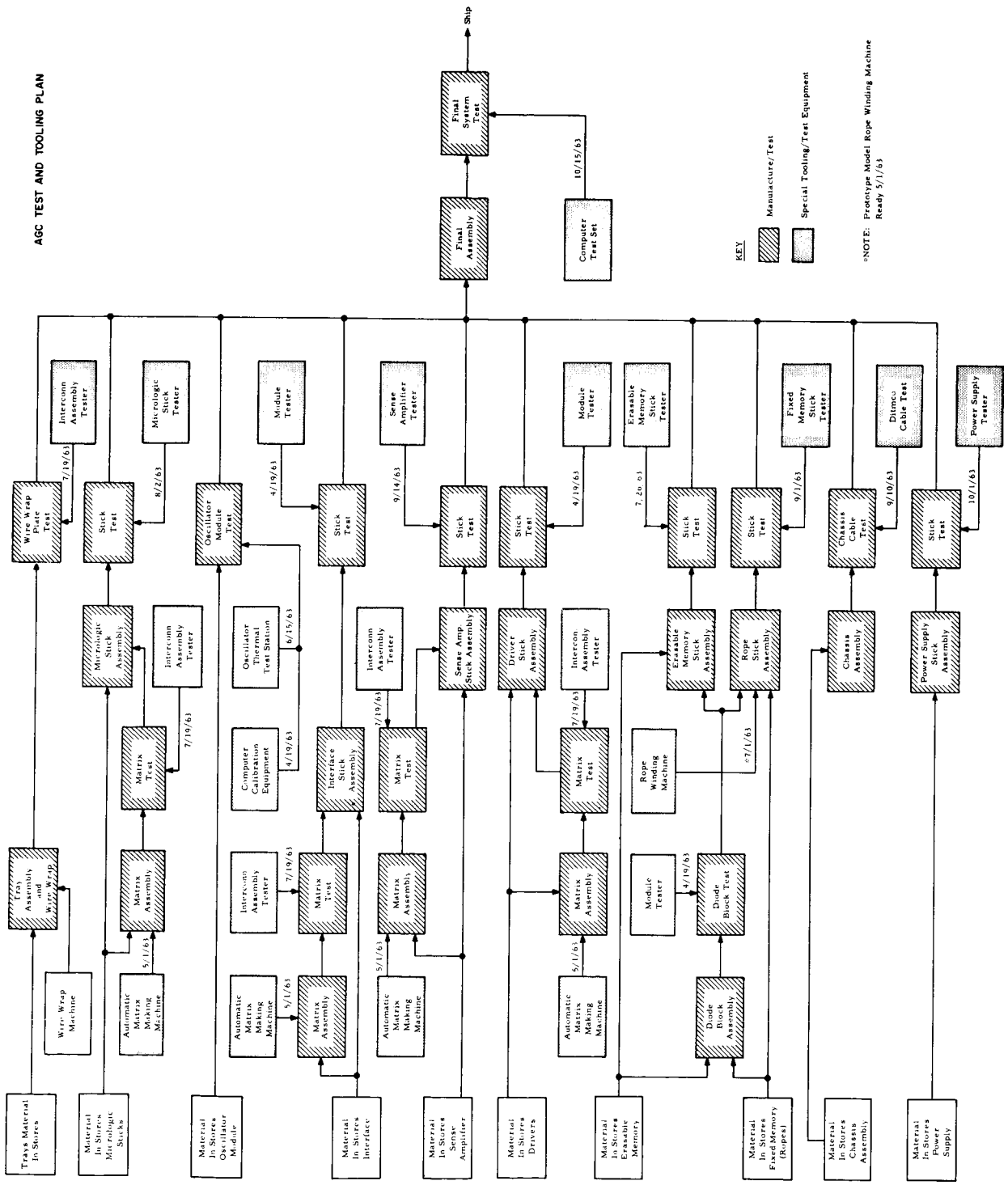

Figure 4-2. AGC Factory Test Plan (Sheet 2 of 2)

of differential gain, resolution, propagation delay, and linearity of integrated sense amplifiers. Efforts are being made to establish a procedure for measuring the temperature coefficient of sense amplifiers in order to obtain information regarding the design of sense amplifier voltage sources.

4.3 CORE ROPE SIMULATOR

The purpose of the Core Rope Simulator (CRS) is to provide a practical tool for the development of AGC programs from subsystem and system test routines to actual in-flight mission programs. The CRS will provide a means of performing a final checkout of programs before implementation as core ropes.

The CRS will be basically a 4096 word erasable memory which will be substituted for and simulate one of the three core ropes contained in the Apollo Guidance Computer. The selection of the core for removal will be a function of the over-all program space allotment and the particular test to be performed.

The CRS will be contained in a 6 foot high by 19 inch wide rack-type enclosure. It will consist of an operator's keyboard, a tape reader and spooler, five module drawers (one of which will contain an erasable core stack), a power input and control panel, and associated dc power supplies.

Electrical design of the CRS has been completed and fabrication begun. All components have been received. The simulator will have five drawers of associated circuitry, each drawer containing an upper and lower section. Wiring of these sections is in process.

SECTION V
RELIABILITY AND QUALITY ASSURANCE

SECTION V
RELIABILITY AND QUALITY ASSURANCE

5.1 GENERAL

Raytheon and MIT/IL have initiated an evaluation and formal qualification program for the three-input NOR gates. Vendors capable of producing this item were notified of this program. Sample NOR gates have been submitted by the vendors and are being used in evaluation tests which stress interchangeability and ability to meet electrical requirements at all system temperature extremes. Formal vendor qualification will commence in June.

The high power diode used in the AGC power supply is being evaluated and a life test rack for this item is being constructed. Capacitors used in the AGC power supply have been evaluated for series resistance.

Incoming, screening, and burn-in equipment planning for the AGC Oscillator has begun. The majority of semi-conductor screening and burn-in equipment has been ordered; some of the equipment has already been received.

During this reporting period, Design Review Committee meetings were held on AGC and GSE documents. As a result of reviews conducted on the AGC Power Supplies and AGC Oscillator, components have been standardized and derating practices improved.

Two mechanical test sets, an abrasion tester and an insulation tester, have been designed and fabricated for magnet wire evaluation tests. Stringent evaluation tests will be performed on the magnet wire to establish limits of acceptability.

SECTION VI
DOCUMENTATION

SECTION VI
DOCUMENTATION

6.1 FAMILIARIZATION MANUAL

The Familiarization Manual will present a physical and functional description of the Apollo Guidance System and Subsystems. The scope and depth of the information is planned for use by engineers already trained in one of the three Apollo Program Subsystems. Because this manual will be used primarily for indoctrination and training at an engineering level, no maintenance information will be included. Detailed theory necessary to support the maintenance and logistics plan will be included in the theory section of the Operation and Maintenance Manual.

Two meetings have been held to date to submit requirements for the Familiarization Manual.

The first meeting was held on 24 April 1963 at MIT/IL. All participating contractors were present. AC Spark Plug's outline was reviewed by the participating contractors. In addition, initial outline requirements were assigned at this meeting.

On 28 April 1963, the second meeting was held at Raytheon between Raytheon and ACSP representatives to establish a level of presentation for the Familiarization Manual.

Raytheon efforts on the Familiarization Manual (figure 6-1) will consist of integrating information into Chapter 2 (Functional Analysis of AGE), Chapter 6 (Ground Support Equipment), and complete effort on Chapter 5 (Computer Subsystem).

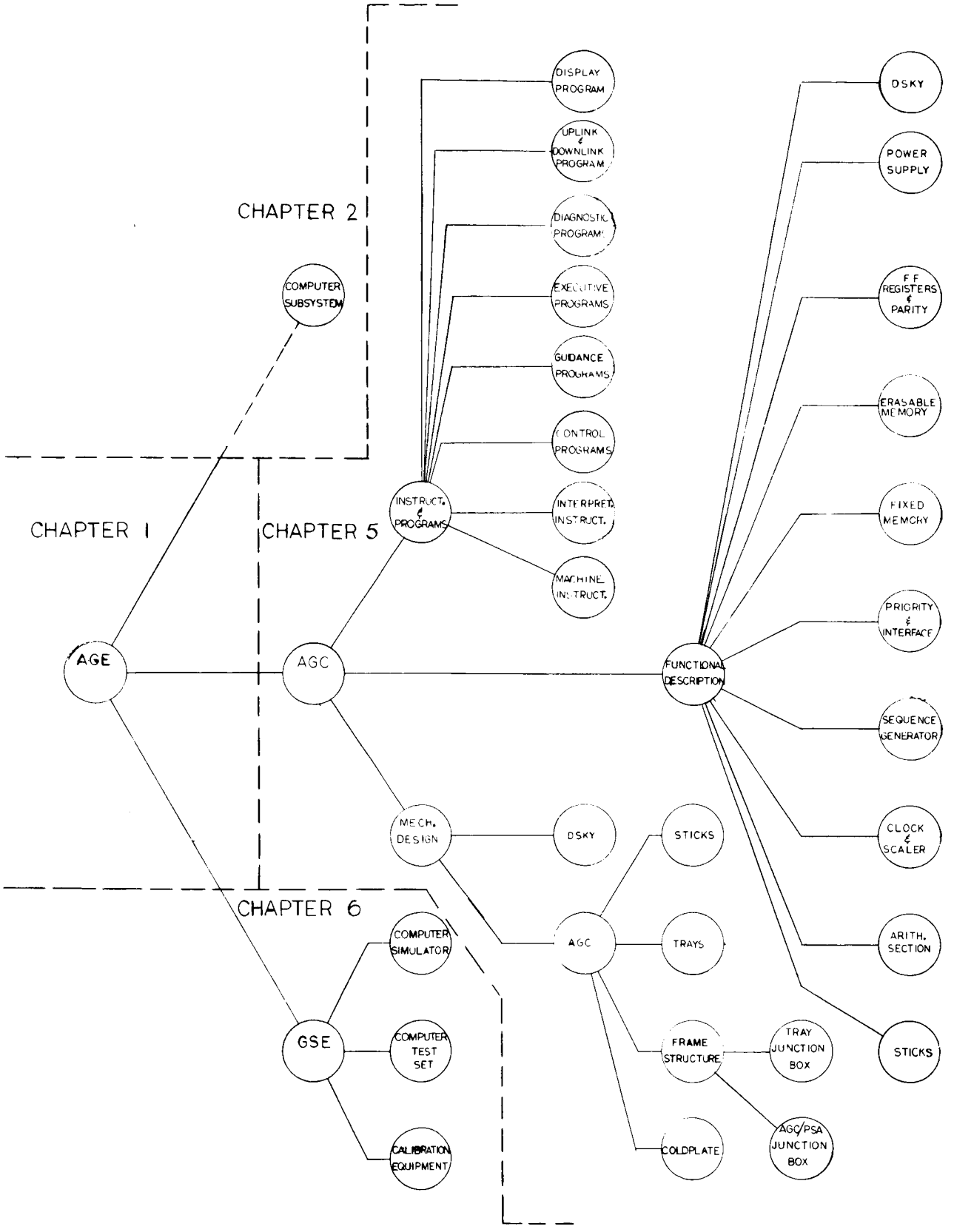

Figure 6-1. AGC Portion of Familiarization Manual

A functional analysis in general terms of the computer will be provided sufficient in scope to support a general block diagram of the AGC. Inputs and outputs will be discussed by type and function but not as specific signals. The type and general character of the memory, the arithmetic unit, control of the computer, and programs will also be discussed.

The information supplied by Raytheon for Chapter 6 will include a physical and functional description of the Computer Test Set, Apollo Guidance Computer Simulator, and the Computer Calibration Equipment. The information included will not contain theory or operating instructions. This chapter will consist of organization and operation, instructions and programs, display programs, functional descriptions, mechanical configuration, and the basic description of the Apollo Guidance Computer.

6.2 AGC INFORMATION SERIES

Reports entitled "AGC Information Series" (AGCIS) are being prepared by Raytheon Company to inform members of the technical staff at MIT and Raytheon about the Apollo Guidance Computer and the Apollo Guidance and Navigation System. Each report will deal with a separate subject and will be released as soon as possible. Although the organization of the series will be as follows, the issues will not necessarily be released in this order.

Apollo Guidance Computer

General Description

Instructions and Programs

Machine Instructions

Interpretive Instructions

Control Programs

Guidance Programs

Executive Programs

- Diagnostic Programs
- Uplink and Downlink Programs
- Display Program

Functional Description

- Logic Sticks
- Display and Keyboard
- Power Supply
- Flip-Flop Registers and Parity
- Erasable Memory
- Fixed Memory
- Priority and Interface
- Sequence Generator
- Clock and Scaler
- Arithmetic Section

Mechanical Design

- Mechanical Design of AGC
- Mechanical Design of Display and Keyboard

Guidance and Navigation System

- AGC Interface and Apollo Subsystems
- Guidance Equations and Programs
- Control Programs

Ground Support Equipment

- Computer Test Set
- Calibration Equipment
- Computer Simulator

Issue 3, Issue 4, and Errata Sheet No. 4 of the AGCIS have been distributed. Issue 3 is the first of the series describing the logic flow of individual Logic Sticks and deals with the Arithmetic Stick. Issue 4 provides a detailed description of the characteristics and operation of the Erasable Memory as a subsystem of the AGC. Errata Sheet No. 4

was issued to include a physical description of the AGC as part of Issue 1, and to update Issues 1 and 2. Issue 5 concerning Logic Sticks A, B, C, and D, and Issue 6 concerning Interpretive Instructions are presently being prepared.

6.3 SPECIFICATION CONTROL DRAWINGS

Three hundred and sixty requests for Specification Control Drawings (SCDs) have been received to date; two hundred and forty-eight have been completed, thirty-eight have been cancelled, and seventy-four are in process. During this reporting period, five special process specifications were started.

6.4 DOCUMENTATION SCHEDULE

The Apollo Documentation Schedule Chart is included as figure 6-2. This schedule summarizes the documentation effort and is based on Revision 1 of the Documentation Plan dated 1 December 1962.

ND NO.	TYPE I SPECIAL PROCESS DOCUMENTS	IN PREPARATION	APPROVED
1002017	SPECIAL TEST REQUIREMENTS FOR SENSE AMPL		CLASS B
1002019	PROCESS FOR GENERAL MARKING	X	
1002025	STD. WELD REPAIRS PROCEDURES IN ELEC-ASS'YS	X	
1002026	INSPECTION CRITERIA OF WELDS IN ELEC-ASS'YS	X	
1002027	WIRE STRIPPING, MAGNETIC	X	
1002028	CORE REPLACEMENT	X	
1002029	FIXED MEMORY WIRING	X	
1002030	MATRIX BONDING	X	
1002031	WIRE WRAPPING	X	
1002032	FAB. OF WIRING HARNESS IN WIRED ASS'YS	X	
1002107	PROCUREMENT SPEC. FOR WIRE-WRAP WIRE	X	
1002116	PROCUREMENT SPEC. FOR NYLON COATED MAG. WIRE	X	
1002119	PROC. FOR ENCAP. SCOTCH CAST #8	X	
1002121	INSTALLATION OF KEENSERTS	X	
1002126	EMBEDDING WITH EPOXY RESIN	X	

TYPE I SPECIFICATION CONTROL DRAWINGS	TOTAL REQUESTS RECEIVED	IN PROCESS	COMPLETED
AGC	69	17	43
GSE	121	53	57.
PSA	170	4	148

PLANS	TYPE	IN PREPARATION	COMPLETED
DOCUMENTATION PLAN	II		X
DEVELOPMENT PLAN	II		X
FACTORY TEST PLAN	III	X	
MASTER SUMMARY SCHEDULE	III	X	

MANUALS	TYPE	IN PREPARATION	COMPLETED
INFORMATION SERIES (AGC)	III	X	
FAMILIARIZATION MANUAL	I	X	
AGC OPERATIONS & MAINTENANCE	I		
GSE OPERATIONS & MAINTENANCE	I		
CHECKOUT MANUAL	*		
LAUNCH OPERATIONS	*		
FLIGHT OPERATION	*		

REPORTS	TYPE	IN PREPARATION	COMPLETED
MONTHLY TECHNICAL PROGRESS	II		Each Month
QUARTERLY TECHNICAL PROGRESS	II		Each Quarter
STILL PHOTOS (Total of 300)	II	X	II
MOTION PICTURE (20 min. total)	II		Partial
TECHNICAL DIRECTIVE STATUS	II		Each Month
EMERGENCY ACTION	II		AR
FAILURE DATA	II		
QUALIFICATION TEST	I		

DOCUMENTS: FINAL ACCEPTANCE TEST PROCEDURE TYPE I	IN-PROCESS INSPECTION PROCEDURE TYPE III	IN-PROCESS TEST PROCEDURE TYPE III	PROCUREMENT SPECIFICATIONS TYPE I	INTERFACE SPECIFICATIONS TYPE I	PERFORMANCE SPECIFICATIONS TYPE I	TOP ASSEMBLY DRAWING NUMBER TYPE I	TITLE	SCHEDULE: UNITS REQUIRED PER ASSEMBLY	PERFORMANCE SPECIFICATIONS	INTERFACE SPECIFICATIONS	PROCUREMENT SPECIFICATIONS	IN-PROCESS TEST PROCEDURE	IN-PROCESS INSPECTION PROCEDURE	FINAL ACCEPTANCE TEST PROCEDURE
✓	NR	NR	*	1002076	*	✓	COMPUTER - AGC	1	8/30/63	7/30/63	1/30/64	NR	NR	12/30/63
✓	✓	✓	NR	NR	NR	✓	FRAME & END CONN	1	NR	NR	NR	11/30/63	11/30/63	11/30/63
✓	✓	✓		NR	NR	✓	TRAY I	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	NR	NR	NR	✓	WIREWRAP PLATE & FRAME	1	NR	NR	NR	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ARITHMETIC	16	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	G SERVICE	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ERASABLE MEMORY ADDER	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	TELEMETRY	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ROPE ADDER	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	PARITY	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	RUPT	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	BANK	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	INTERFACE	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
✓	✓	✓	*	NR	NR	✓	TRAY II	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	NR	NR	NR	✓	WIREWRAP PLATE & FRAME	1	NR	NR	NR	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	SCALER & MEMORY TIMING	2	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	SEQUENCE GENERATOR	5	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	RING & IT. & TR.	2	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	RATES	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ALARMS	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	COUNTERS	3	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	CATCHALL	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	TEST CONN.	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	INTERFACE	2	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
✓	✓	✓	*	NR	NR	✓	TRAY III	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	NR	NR	NR	✓	WIREWRAP PLATE & FRAME	1	NR	NR	NR	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	SENSE AMPLIFIER	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	READ DRIVER	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	Z INHIBIT	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	CURRENT SWITCH	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ROPE INHIBIT DRIVER	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ROPE GATES	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ROPE SENSE AMPLIFIER	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	STRAND SELECTOR	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	ERASABLE MEMORY		NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	POWER SUPPLY	3	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	OSCILLATOR	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	OVERFLOW ST.	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
✓	✓	✓	*	NR	NR	✓	TRAY IV	1	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
*	*	*	NR	NR	NR	✓	WIREWRAP PLATE & FRAME	1	NR	NR	NR	11/30/63	11/30/63	11/30/63
*	*	*	*	NR	NR	✓	FIXED MEMORY	12	NR	NR	12/30/63	11/30/63	11/30/63	11/30/63
✓	✓	✓	*	1002076	NR	✓	COMPUTER DISPLAY	1	NR	7/30/62	12/30/63	11/30/63	11/30/63	11/30/63
✓	✓	✓	*	✓	NR	✓	COMPUTER TEST SET (GSE)	1	NR	7/30/62	9/30/63	8/30/63	8/30/63	9/30/63
✓	✓	✓	*	✓	NR	✓	COMPUTER SIMULATOR (GSE)	1	NR	6/30/62	7/1/63	7/1/63	7/1/63	7/10/63
NR	NR	NR	NR	NR	NR	✓	COMPUTER CALIBRATION EQUIP. (GSE)	1	NR	NR	NR	NR	NR	NR

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	ADDED LATEST INFORMATION	5/10/63	E.V.

NOTES:

1. * INDICATES THAT THIS DOCUMENT IS NOT INCLUDED IN OUR PRESENT CONTRACT.
2. ✓ THE NUMBERS FOR THESE DOCUMENTS WILL BE ASSIGNED AT A LATER DATE.
3. (NR) INDICATES "NOT REQUIRED".
4. THIS DOCUMENTATION SCHEDULE IS BASED ON THE DOCUMENTATION PLAN REV. 1 DATED 1 DEC. 1962.

RAYTHEON CO. LEXINGTON, MASS.	MANNED SPACECRAFT CENTER HOUSTON, TEXAS	
DWG NO / CONTRACT		
DRAWN R.P. Russell DATE 3/4/63	APOLLO DOCUMENTATION SCHEDULE	
CHECKED		
APPROVAL J.R. Antaya 3/4/63		
APPROVAL		
NASA APPROVAL	CODE IDENT NO.	SIZE C / NASA DRAWING NO. 1010517
MIT APPROVAL	SCALE	WT / SHEET OF

Figure 6-2. Apollo Documentation Schedule Chart