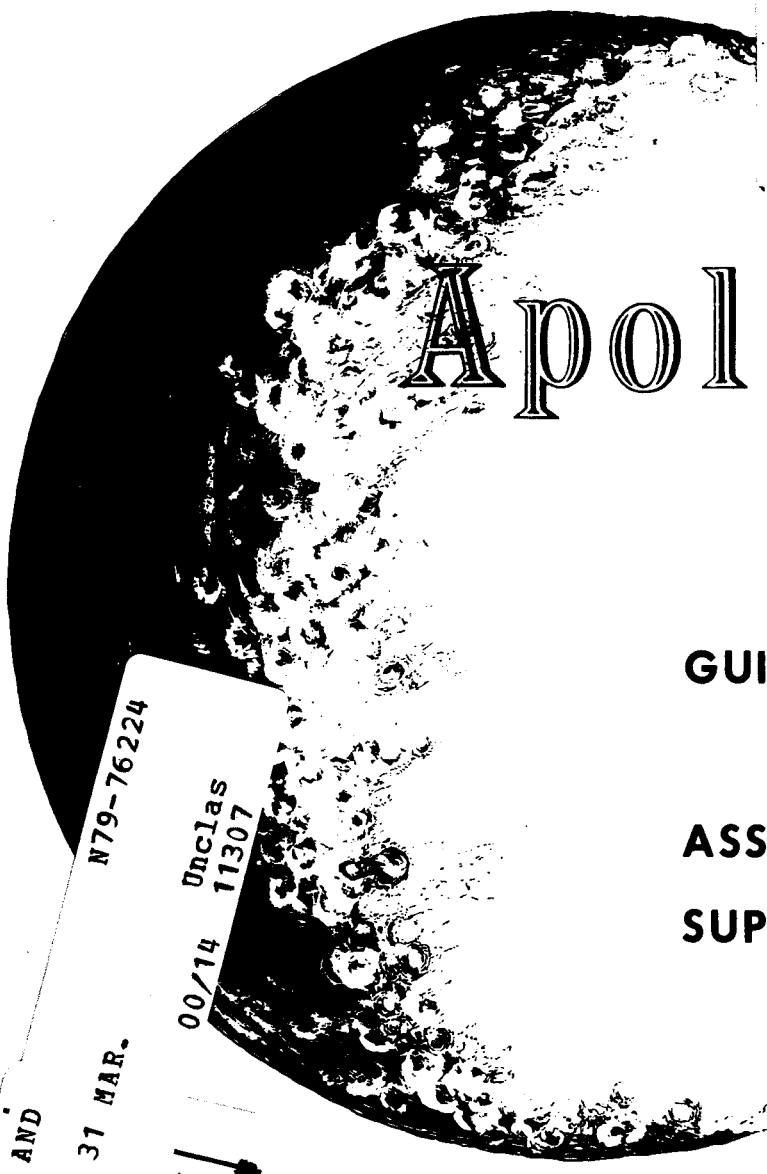

GUIDANCE COMPUTER AND ASSOCIATED GROUND SUPPORT EQUIPMENT(U)

QUARTERLY TECHNICAL REPORT
NO. 3
FR-3-53

RAYTHEON COMPANY
SPACE AND INFORMATION SYSTEMS DIVISION

RAYTHEON

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QUARTERLY TECHNICAL REPORT NO. 3

FR-3-53

Period Covered

1 January 1963 - 31 March 1963

Prepared by

RAYTHEON COMPANY
SPACE AND INFORMATION SYSTEMS DIVISION
Sudbury, Massachusetts

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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INTRODUCTION

1.1 GENERAL

This is Quarterly Technical Report No. 3 issued in lieu of Monthly Technical Report No. 9 in accordance with Work Statement for Industrial Support, E-1097. A monthly report is not required when a quarterly report is issued. The next monthly report issued will be Monthly Technical Report No. 10. Information which would normally be contained in report No. 9 is included in this report.

This Quarterly Technical Report covers the period 1 January 1963 through 31 March 1963. Sixty-nine Technical Directives have been received and accepted to date; fifteen have been completed and fifty-four remain active.

Raytheon has assigned resident engineers to MIT/IL to: (1) aid in the development of requirements for computer check-out, GSE functions, and PACE (2) provide assistance in generating the Logistic Support Plan, including maintenance analysis, and (3) assist GSE design, development test, and liaison effort, and conduct a study on Computer Simulator output interface signal distortion.

Raytheon issued the "Master Summary Schedule - Apollo Guidance Computer and Associated Ground Support Equipment" on 20 March 1963. This schedule consists of a program summary showing technical milestones and plans for the design, release, fabrication, and delivery of hardware.

To supplement the Master Summary Schedule, and for the purpose of the monthly report, an Apollo Project Plan has been prepared and included in this report as figure 1-1. This plan is prepared in the NASA format and lists the important milestones of the Apollo Project. This plan will be updated on a monthly basis.

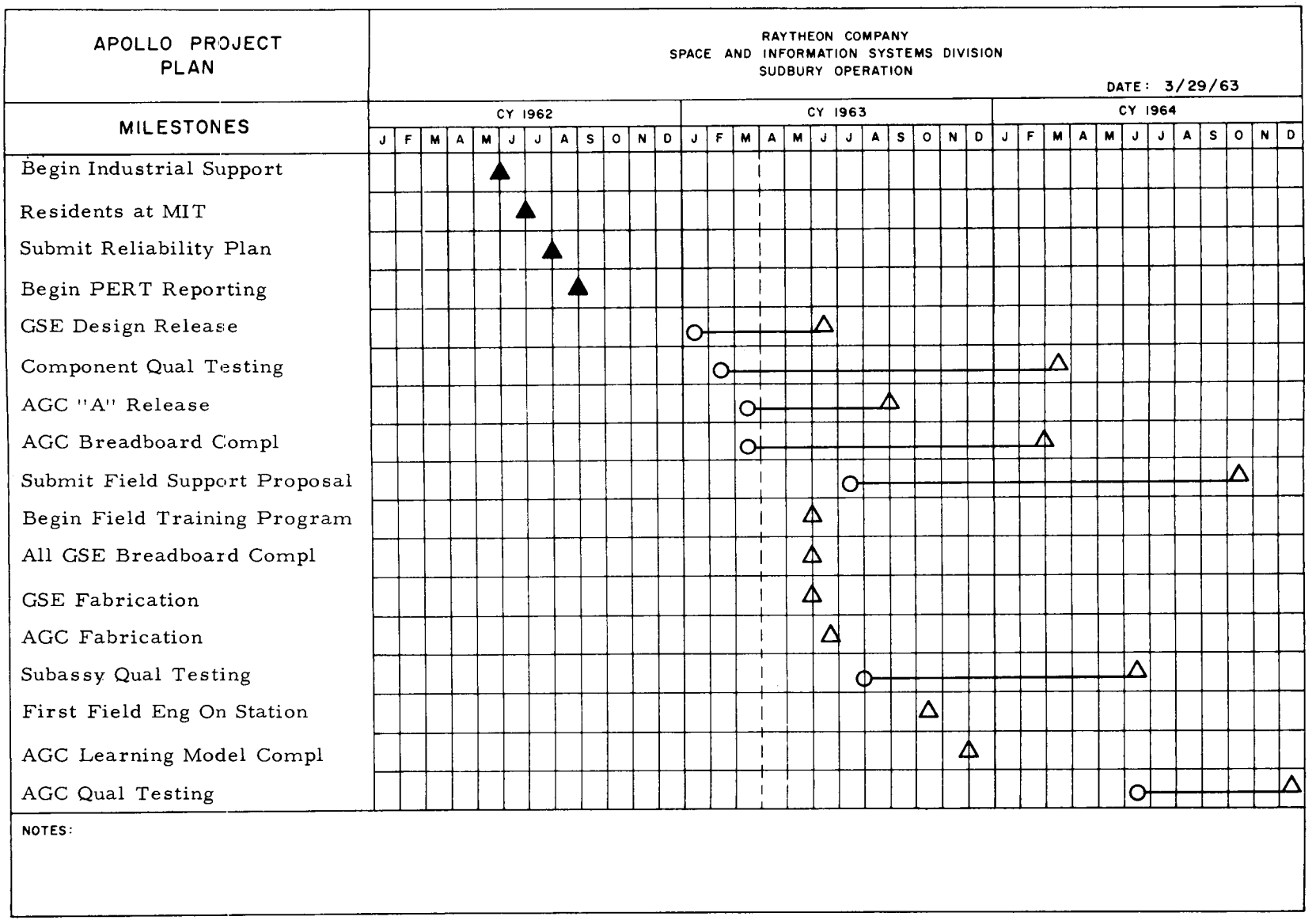


Figure 1-1. Raytheon Apollo Milestone Chart

Raytheon and MIT/IL held several meetings during this reporting period to more closely coordinate and integrate schedules and definitions of both Class A and Class B releases for the AGC. The PERT fragnets were revised to reflect the results of these discussions. The Raytheon fragnet for AGC 6 now includes the subassemblies for AGC 5 to be delivered to MIT/IL. A fragnet for AGC 4A and AGC 4B has been prepared and a fragnet for the AGC oscillator effort is in preparation. These fragnets will be submitted to MIT/IL shortly.

SECTION II
APOLLO GUIDANCE COMPUTER

SECTION II
APOLLO GUIDANCE COMPUTER

2.1 INTRODUCTION

The AGC system consists of three major physical parts; the AGC which is located in the lower equipment bay of the Command Module; a Display and Keyboard Unit (DSKY) also located in the lower equipment bay; and a DSKY located in the Main Display Panel. Figure 2-1 shows the location of these units.

The AGC (figure 2-2) consists of five trays housed in a frame structure which contains a tray junction box assembly and an AGC/PSA junction box. The frame structure is bolted to the AGC coldplate which provides installation mounting and heat transfer media. The trays are designated A through E and contain plug-in sticks. The end connectors of the trays connect to the tray junction box assembly which contains the female Malco miniwasp connector pins. The underside of the connector pins are wirewrapped to provide interconnections between the five trays. Connections from the tray junction box assembly to the AGC/PSA junction box are made with a cable mounted to the frame structure. The AGC/PSA junction box distributes signal and power connections between the trays, the PSA, and the outside world. A cable connecting the AGC to the Guidance and Navigation System is plugged into the front of the AGC/PSA junction box, and a cable connecting AGC and PSA is plugged into the back of the box.

The AGC occupies a volume of 1.9 cubic feet. In general, the frame, tray, and stick structural members are hard-anodized magnesium alloy and the hardware is corrosion-resistant antimagnetic stainless steel. The sticks are urethane foam potted. Each loaded tray occupies a volume of approximately 0.26 cubic feet.

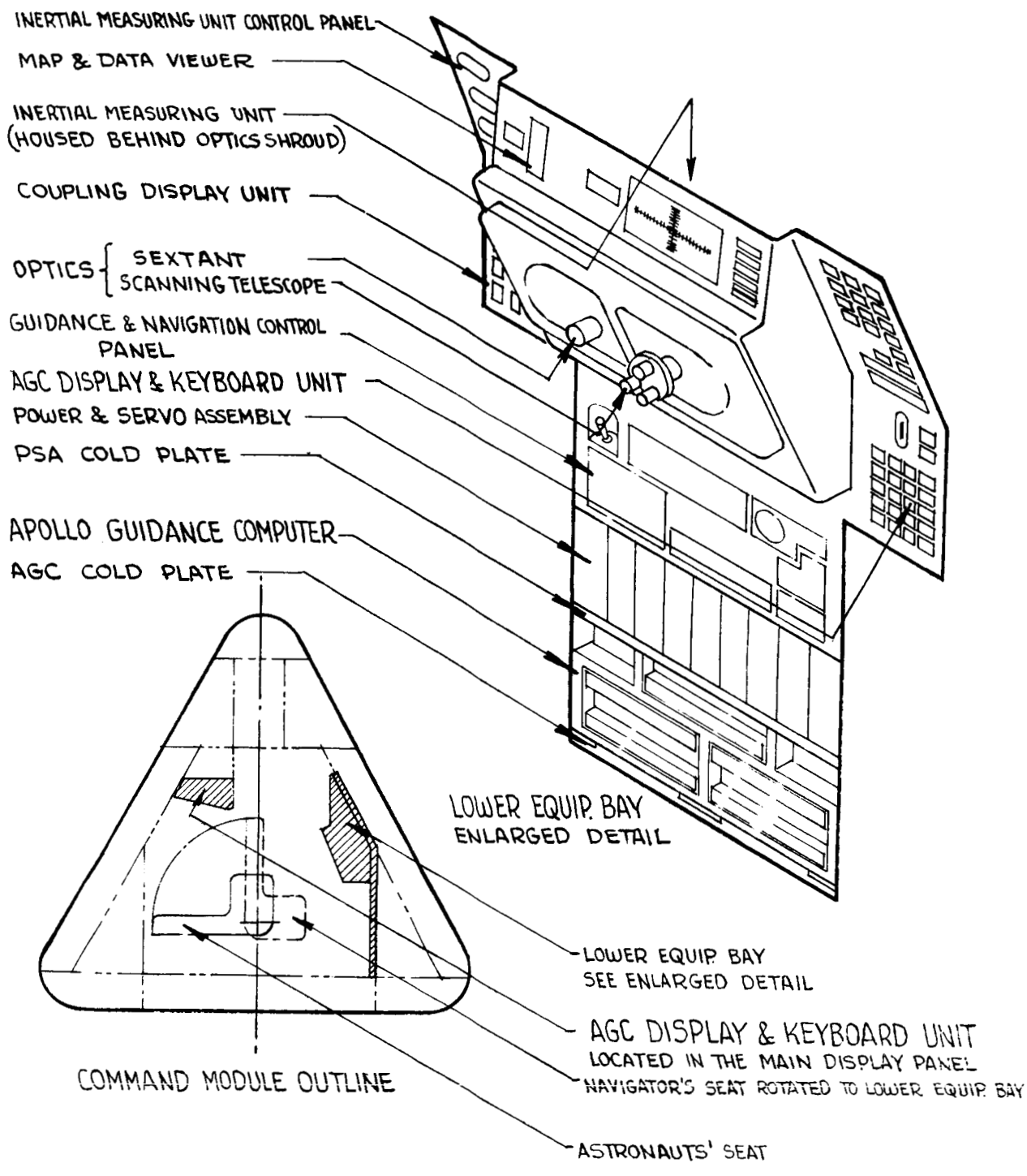


Figure 2-1. Apollo Command Module G & N System

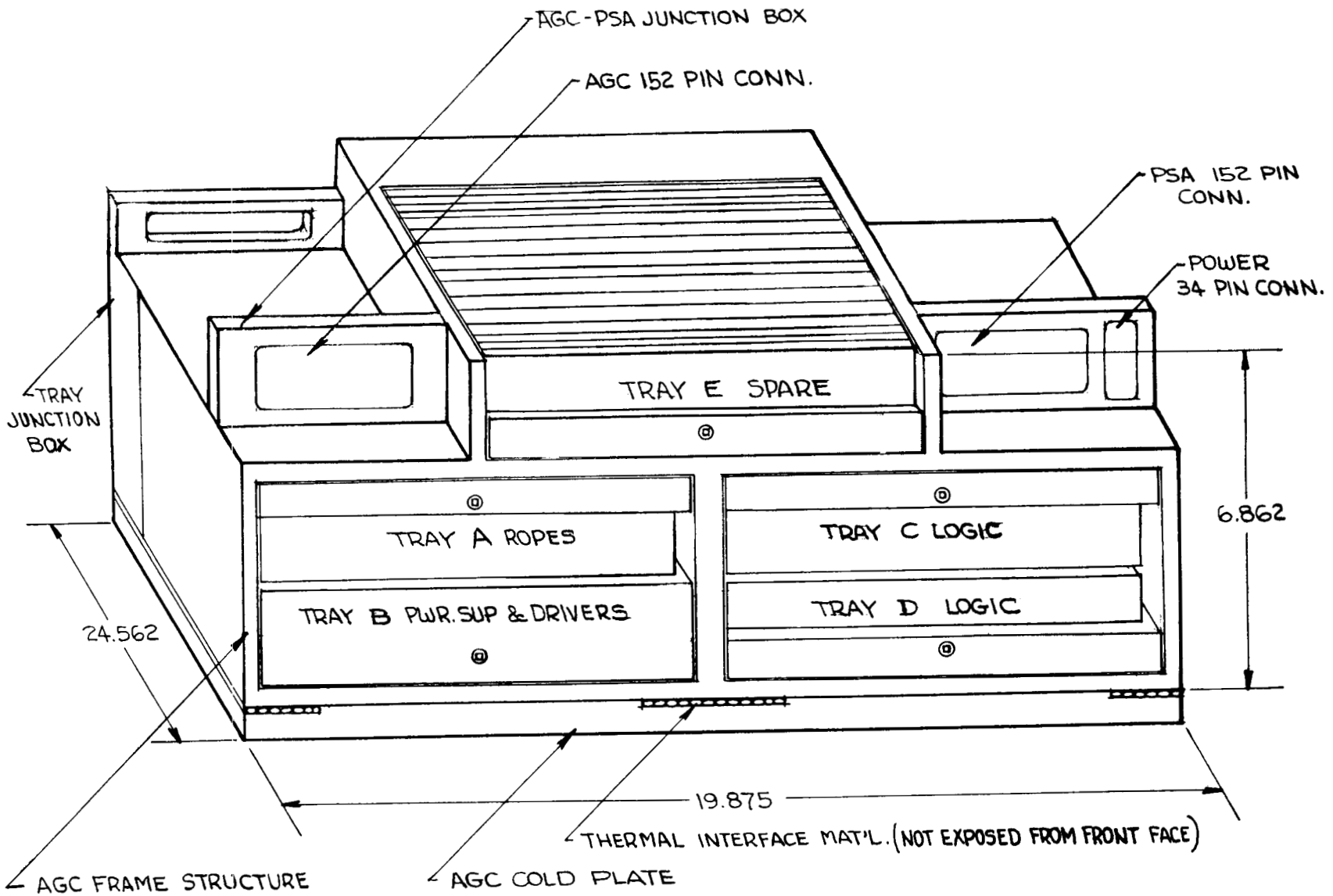


Figure 2-2. Apollo Guidance Computer

The AGC frame structure is designed, and the trays are placed in the frame, in such a manner as to provide optimum-balanced thermal design. The power consumption of the computer is approximately 200 watts. The heat dissipation of approximately 177 watts is distributed as follows:

a. Trays C and D (Logic Trays) located on the right side of the frame, each contain 24 Sticks with a dissipation of 1.8 watts per stick (a total of 86 watts).

b. Tray B (Power Supply and Driver Tray), located on the left hand bottom section of the frame, dissipates a total of 91 watts.

c. Tray A (Rope Tray) located directly above Tray B and the Spare Tray E contribute little or no heat dissipation.

The frame structure is made up of two cast-magnesium channel-type sections bolted together, plus a junction box subassembly. The frame contains worm-gear plates and wedge-pin mechanisms to secure the trays in compressive contact with the structure, providing a thermal path through the frame which in turn is bolted to the AGC coldplate. The coldplate is an aluminum-alloy liquid-cooled honeycomb structure designed to provide the interface thermal conductance media to handle the heat dissipation generated by the AGC while maintaining a constant interface temperature of approximately 25°C during the operation phase of the computer. The AGC frame structure is connected to the coldplate through inset strips of thermal interface material (copper foil helically wound on rubber tubing) to afford maximum conductance.

The AGC trays are wrap-around frame structures which house and give rigidity to the plug-in sticks. Each tray contains the female Malco miniwasp connector pins, the underside of which are wirewrapped, providing multi-interconnections between the sticks and to the end connector of the tray. The wirewrapped underside of the tray is urethane foam potted leaving the ends of the connector pins exposed for test points. The sticks are bolted to the tray with captive jack screws. The tray has a worm gear and wedging mechanism

which affords the means of locking the tray into the frame structure to insure positive end connector engagement to the frame structure junction box and provides the necessary thermal conductive path between the sticks and the frame structure.

The five AGC trays are of identical design with a capacity of 24 single module sticks each of 12 double sticks each or a combination of both. The tray contents and distribution are as follows:

a. Tray A (Rope Tray) contains 3 Ropes (J, S, and R) of 4 double sticks each as shown in figure 2-3. Tray A is located in the upper left section of the frame.

b. Tray B (Power Supply and Driver Tray) contains the power supplies, oscillator, the rope drivers and strand select, the erasable memory drivers, current switches and sense amplifiers, and several unassigned sticks as shown in figure 2-4. Tray B is located in the lower left section of the frame.

c. Tray C (Logic Tray C) contains 16 arithmetic sticks, G and A service, parity, bank, interrupt priority, erasable memory and rope address, telemetry, and input-output sticks as shown in figure 2-5. Tray C is located in the upper right section of the frame.

d. Tray D (Logic Tray D) located in the lower right section of the frame contains test connectors, central control units, ring counter, scalers, control pulses and pulse counter, SQ complex, instruction decode, counter priority and service, rate circuits, alarms, input-output, and several unassigned sticks as shown in figure 2-6.

e. Tray E (Spare Tray) situated in the top center section of the frame contains the unassigned and spare module sticks shown in figure 2-7.

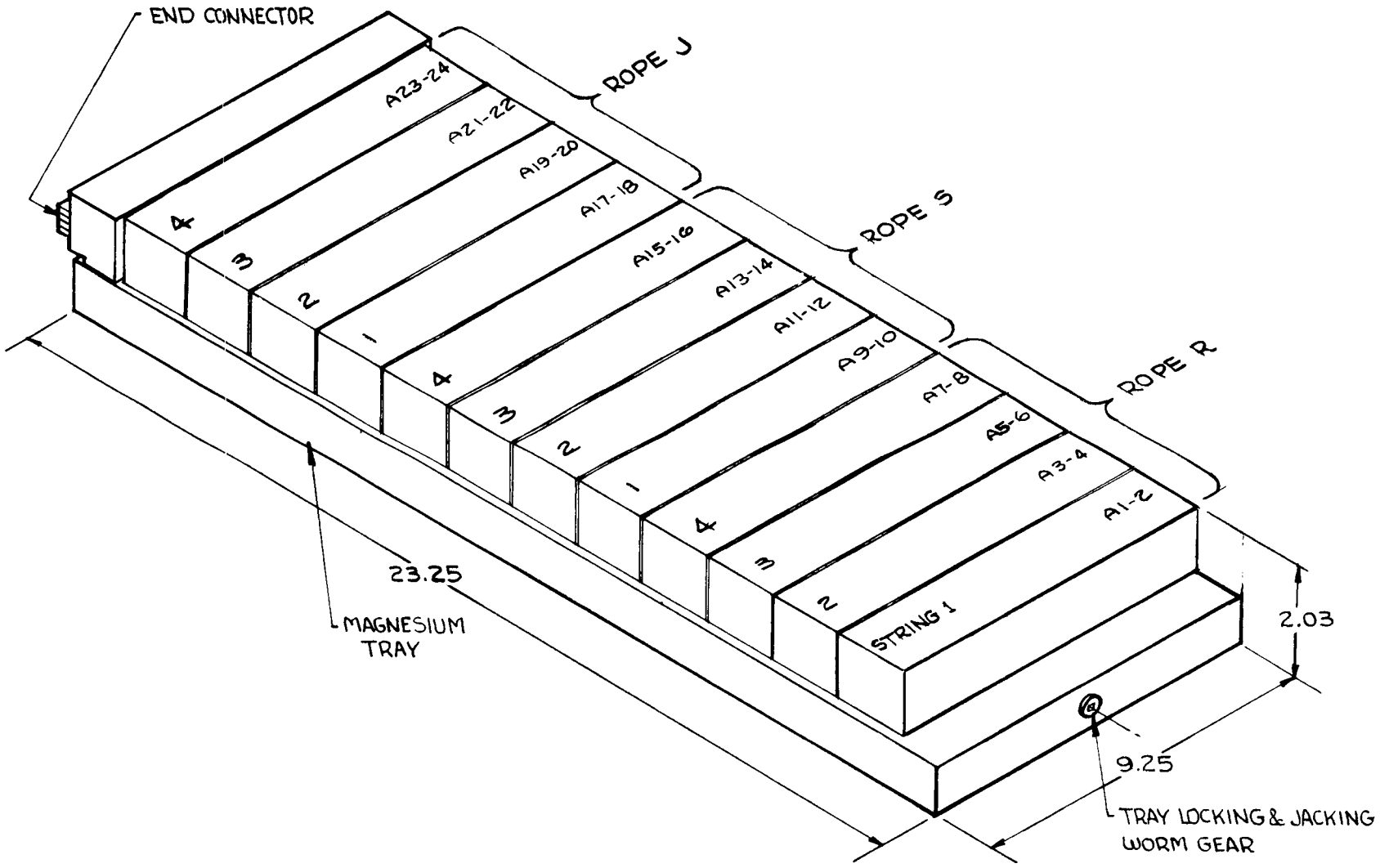


Figure 2-3. AGC Rope Tray A

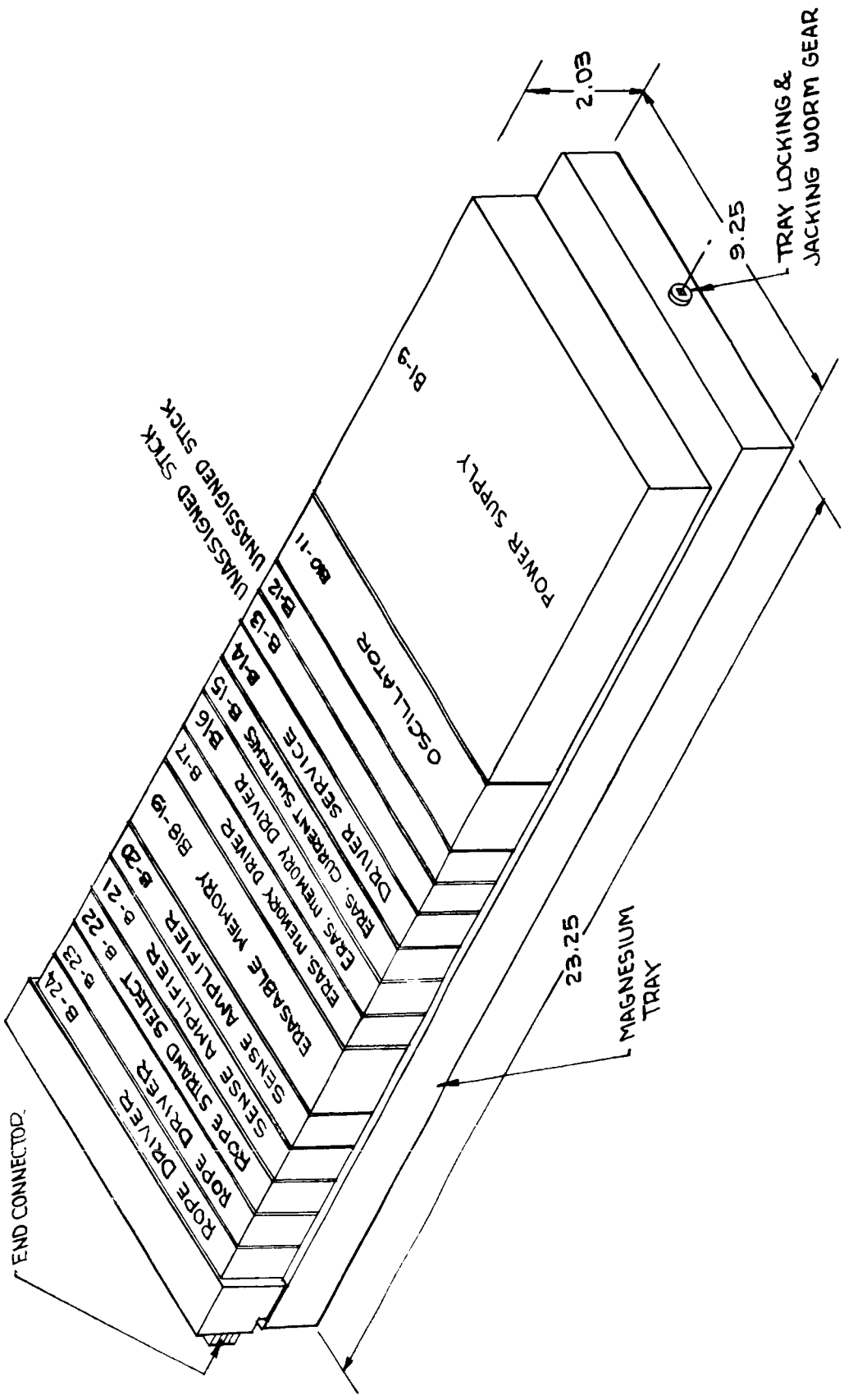


Figure 2-4. AGC Power Supply and Driver Tray B

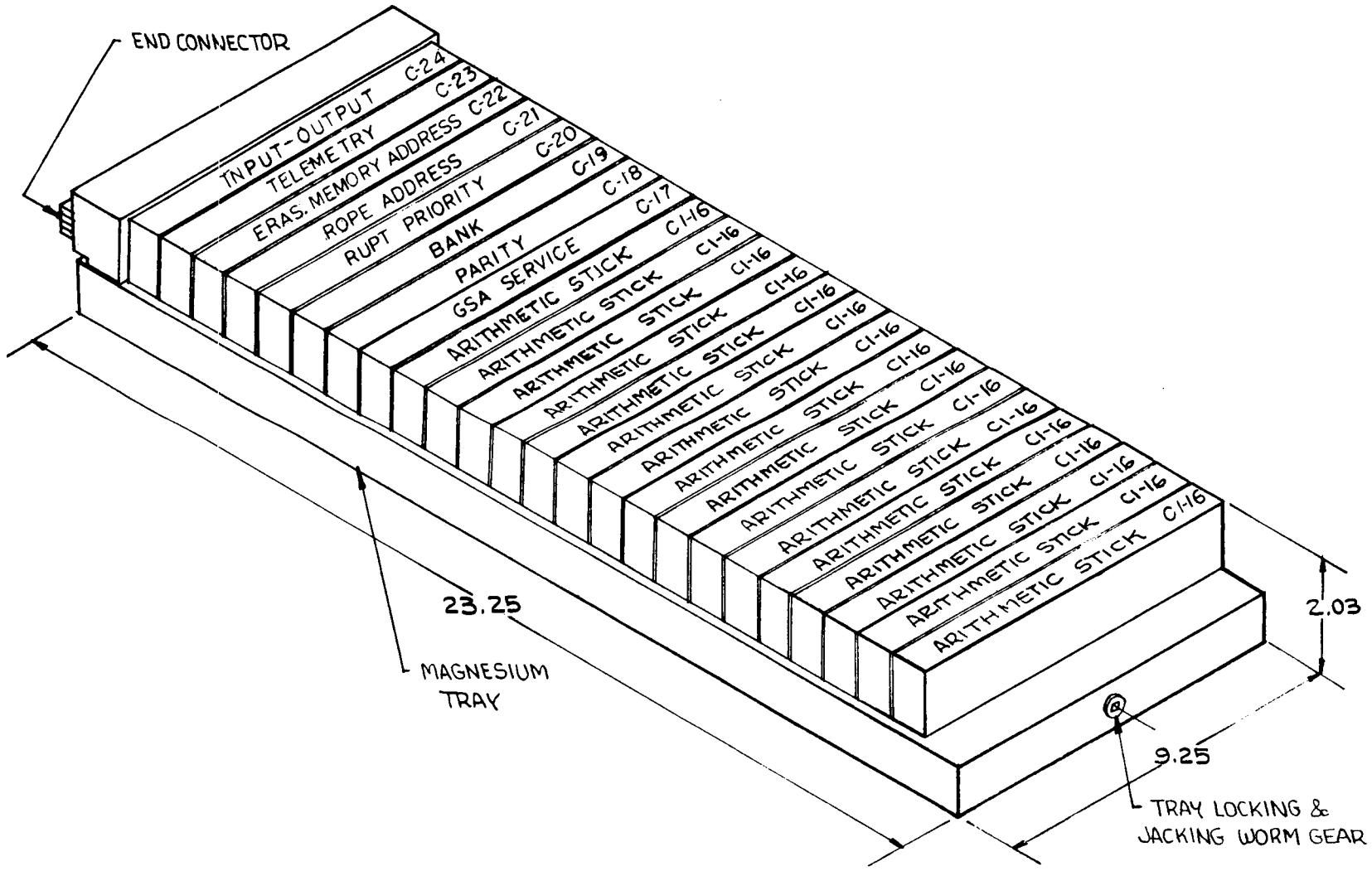


Figure 2-5. AGC Logic Tray C

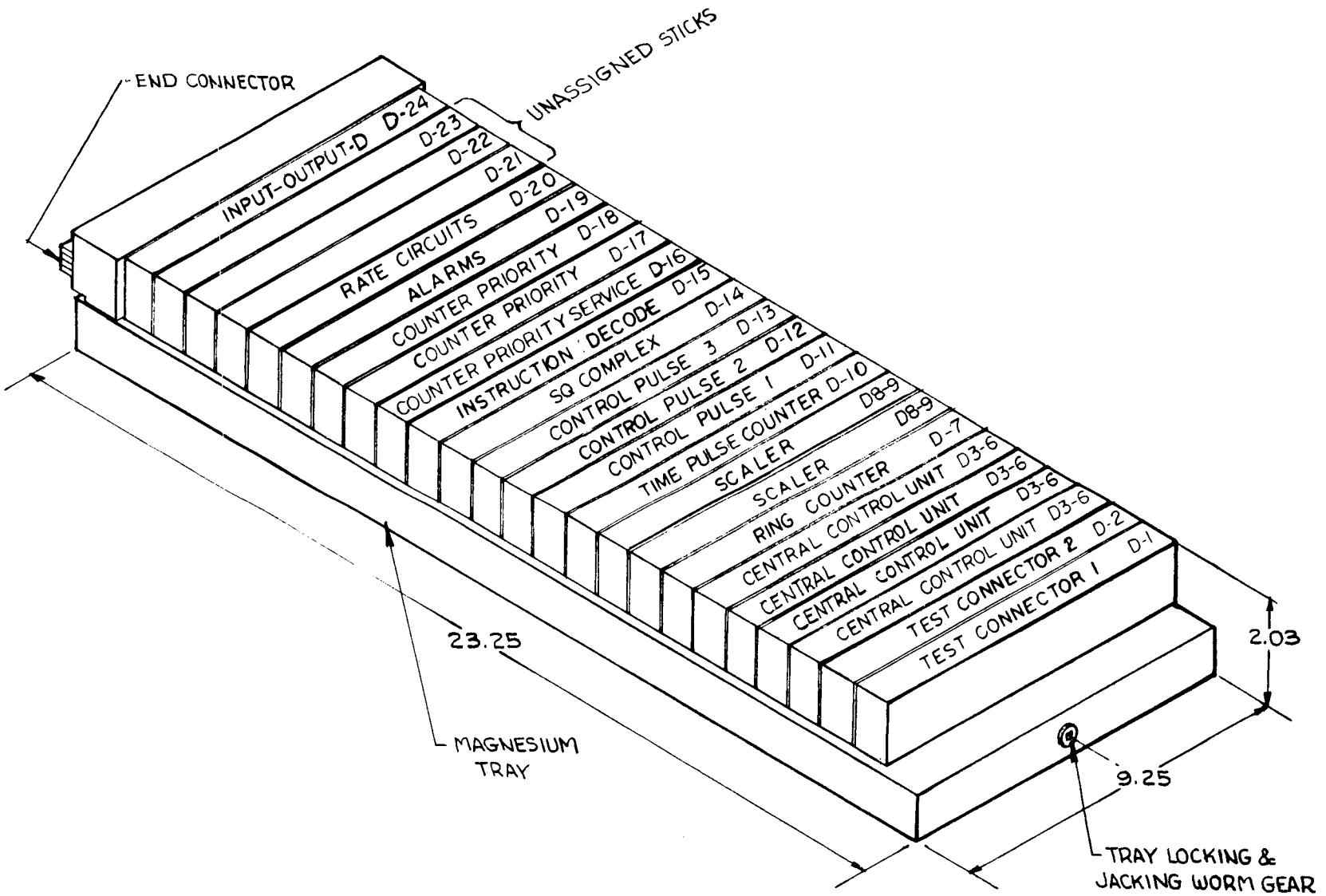


Figure 2-6. AGC Logic Tray D

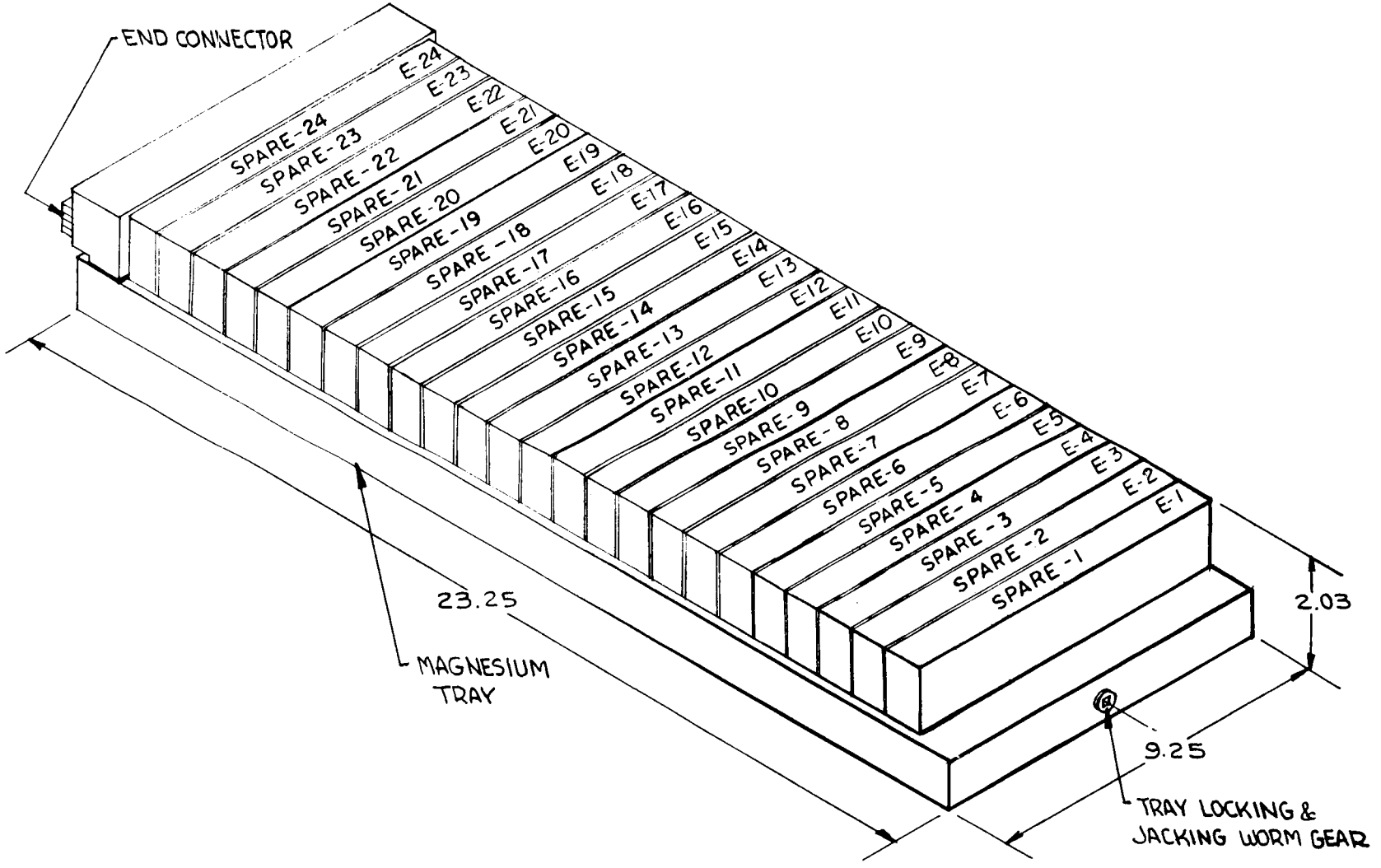


Figure 2-7. AGC Spare Tray E

A typical integrated NOR gate or single stick, as shown in figure 2-8, is 0.825" wide, 1.550" high and 9.150" long. The basic structural element is the hard-anodized magnesium alloy "I" beam header dividing the stick into two separate sections and containing 142 Malco miniwasp male connector pins on 0.125 centers. Each section houses 2 plastic loading forms which seat 30 integrated NOR gates in TO-47 cans for a total of 120 per stick. The gates are interconnected by means of a folded matrix and connected to the header connector pins through a flat inner matrix. The completed assembly is urethane foam potted.

A double stick such as those which constitute the fixed memory ropes are erasable memory units are of similar design to the integrated NOR gate stick comprising a 142 Malco pin header. The double stick is 1.700" wide, 1.550" high and 9.150" long.

The oscillator also comprises a double stick in exterior dimension but is of somewhat peculiar design inherent in the difficult requirements imposed by the quartz crystal and associated circuitry.

2.2 ROPE WINDER

There are two basic problems encountered when fabricating ropes. These problems are: (1) thread through the cores with a delicate wire without breaking, kinking, or stripping the insulation from the wire and, (2) provide convenient storage for the wire during the process. Several methods have been closely examined and the most feasible, a spinning-reel technique, was pursued.

An engineering model of a rope winder has been constructed to prove the concept of the spinning-reel. This rope winder is illustrated on figure 2-9. This technique employs two manually-operated, identically-constructed reels

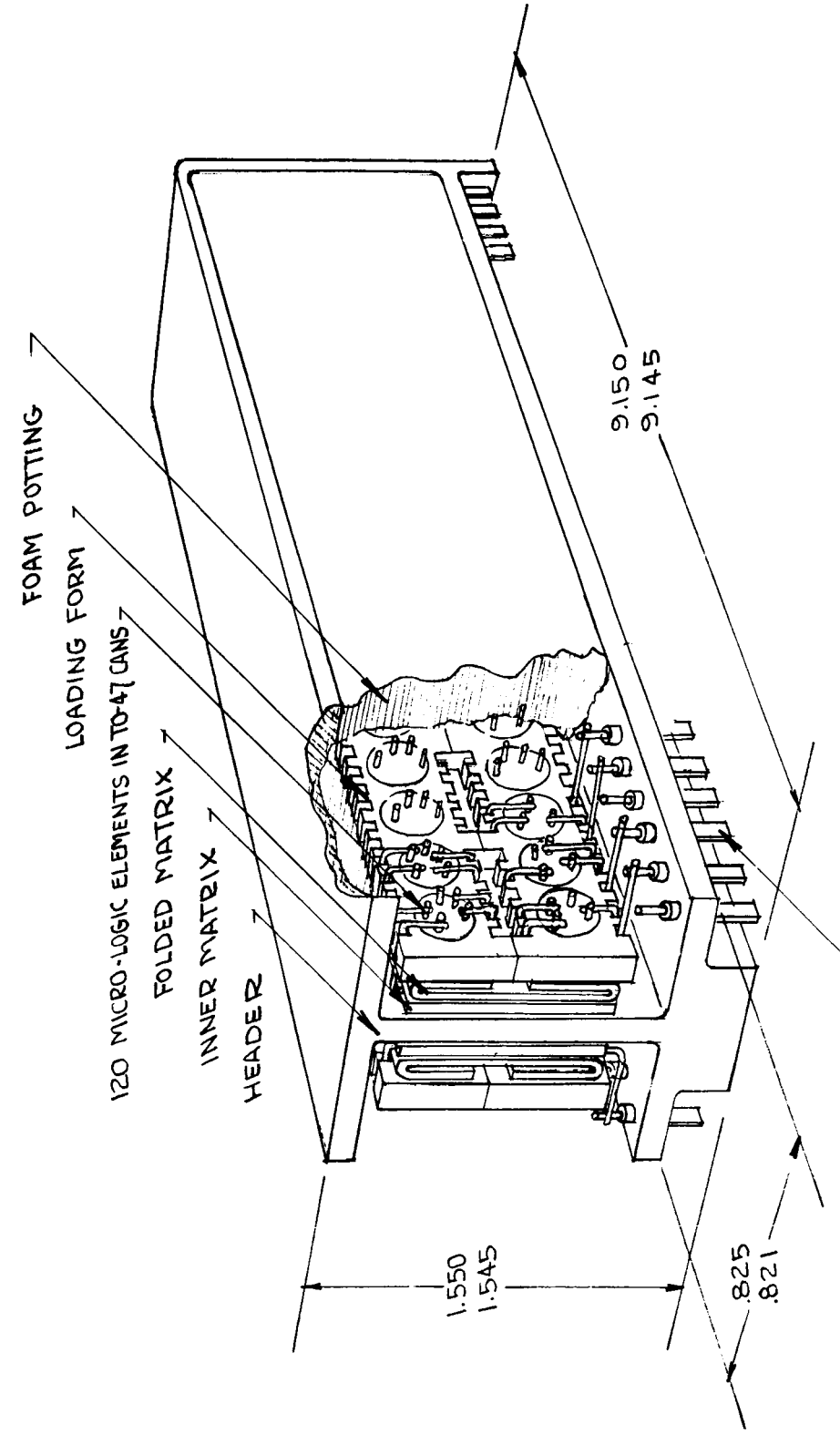


Figure 2-8. Typical Micrologic Stick Construction

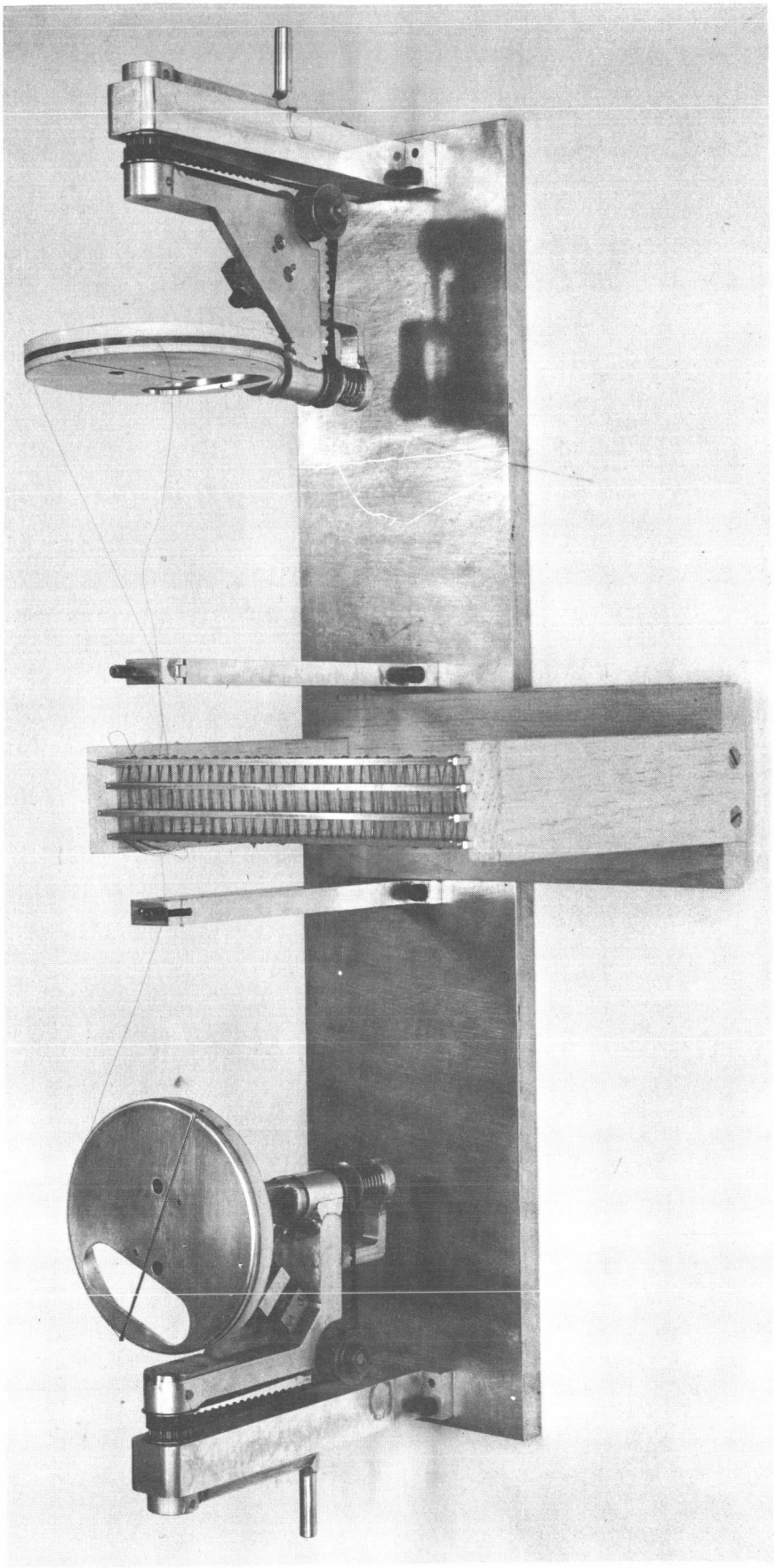


Figure 2-9. Rope Winder

mounted on the same center line, approximately 27 inches apart. Each reel has provisions for either vertical or horizontal spool alignment. Slots are provided on the top of each spool to accomodate a threading needle. This needle attaches to the leading end of the wire and facilitates the threading of the cores. A temporary rack supports the cores to be wired and is mounted in the center between the two reels, providing symmetry to the device.

Wire is initially stored on the vertically aligned spool. The wire is unwound from this spool, threaded through the proper cores, and rewound, top to bottom in the form of a helix, on the horizontally aligned spool. Guides on the rack support allow the wire to pass freely through the inner diameter of the cores. As the wire is unwound from the vertically aligned spool, a torsion wind is produced on the wire. This torsion wind is removed by orbiting the second spool while rewinding the wire. Spool alignment is then reversed and the threading cycle takes place in the reverse direction. Several dummy ropes have been wired utilizing this technique and the results were favorable. Further efforts are being made to refine the device for greater efficiency, with semi-automatic operation being the long-term objective.

2.3 MINIATURE WIREWRAP

A miniature wirewrap technique was originally investigated in order to provide, in conjunction with the use of micrologic, an increase in over-all computer packaging density. In order to prove the miniature wirewrap (miniwrap) concept, Raytheon modified a Pratt and Whitney Tape-O-Matic drill. After extensive testing, Raytheon demonstrated that miniwrap techniques would be low in cost and provide the quality, accuracy, and reliability required.

The Pratt and Whitney drill is a versatile wirewrap tool that is numerically controlled and supplemented by powered vertical motion, an automatic repeat cycle, a tape reader, and a data display unit. (See figure 2-10.) A fixture

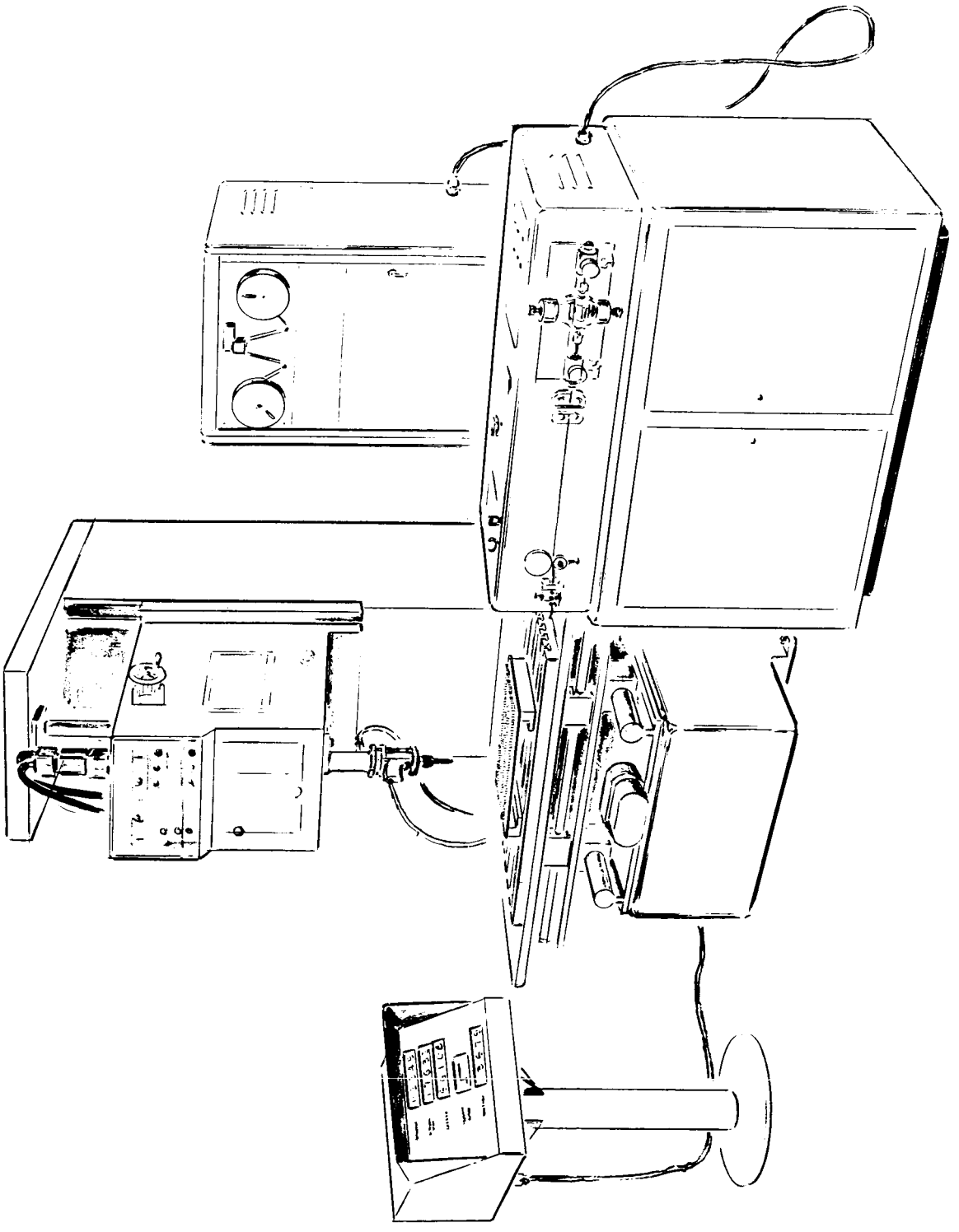


Figure 2-10. Semi-automatic Miniature Wirewrap Machine

has been designed to hold a hand wrapping tool that will accomodate 30 through 16 gauge wire and will adapt to the drill of the Pratt and Whitney machine. A back pressure valve is provided on this fixture which can be manually adjusted to vary the weight of the wrapping tool depending on the characteristics of the wire used. By proper adjustment of the pressure, a reliable gas-tight wrap can be made.

Machine stimulus is provided by a punched paper tape program that furnishes data display and machine instructions in two modes of operation; semi-automatic and automatic. Programing the punched tape is achieved by utilizing process sheets that have a Friden Flexowriter tab-sequential format that allows the programer to easily record dimensional information and wiring patterns that are taken from interconnection diagrams. From this information wires are precut and prestripped by the operator and arranged according to the tape program. At the present time, efforts are being made to obtain a programable wire stripper and cutter which will be commanded by the wire length display information. This device will eliminate the storage of precut and prestripped random lengths of wire.

The programer chooses a zero reference point that allows only positive machine instructions. This minimizes programing errors and directs the machine to operate in the first quadrant only. Plus signs and leading zeros may be deleted and any axis dimensions eliminated if that dimension is unchanged in the succeeding instructions. Wires can be grouped by length, pattern, or sequence to make optimum use of machine positioning speed, to simplify tape preparation, and to conserve tape length.

The data display unit will be mounted on a pedestal on the opposite side of the wirewrap tool from the control console. It will have additional logic for sensing, decoding, and driving the unit as well as facilities for the following four special displays: wire sequence, X and Y table coordinates, wire length, and

wire pattern. Display lights and pushbuttons are provided on the control panel to aid the operator in performing the proper sequence of programed events. The color of the lights may be programed to signify a change in the program or a Z level (wire density) code.

In the semi-automatic mode, a wrapost is positioned each time the advance button is activated by the operator. The vertical and rotational motions of the wrapping tool are also pushbutton controlled. The data display unit provides a pictorial presentation of the wire pattern and a numerical read-out of wire length and table coordinates. The operator inserts the prescribed length of wire into the wrapping quill as designated by the display unit. The quill is depressed until it reaches a positive stop where the rotational motion of the wrapping tool is energized. The quill then retracts to the nominal rest position.

The automatic mode requires no additional programing. The table is positioned from the instructions on the tape. Upon reaching the commanded position, a set light is energized that activates the down-feed of the quill. Before the quill is depressed, the operator must insert the prescribed wire. Safety factors are being studied for this phase of the operation to maximize operator safety. The remaining steps of the operation are the same as those for semi-automatic. The tape is automatically advanced to the next instruction after retraction of the tool.

In order to minimize human error, all sorting and sequencing of tape processing information will be performed by IBM tabulating equipment. To provide more reliability in the final tape program, the following sequence of steps are provided for the programer:

a. Find the interconnection path and assign Z level notation, pattern, machine coordinates, wire lengths, etc. in any logical order and transfer this information to IBM cards.

b. Sort the cards to sequence criteria for operator, program, and machine efficiency.

c. Insert post processor cards (rewind instructions, etc.) and assign sequence number using tab equipment.

d. Sort the cards to generate a verification sheet. This sheet will be a print-out of the signal name and sequence number at each command position or representative coordinates of the wire-wrap board.

e. Sort the cards by sequence number and generate the program tape.

This system of processing the tape information minimizes human error during processing, provides the opportunity to check for errors by using the verification sheet, provides a flexible medium for making engineering changes, is a source of test cards for any continuity tester that operates from cards, and is a source of reports for costing, purchasing, etc. The same program tape may be used to drill the holes for the connector plate, to wirewrap the conductor or components, and to locate pins for trouble shooting, visual inspection, and electrical tests.

2.4 RESISTANCE WELDING

The resistance welding study program being conducted by Raytheon is complete with the exception of operating life tests. These life tests are presently in process. Preliminary data evaluation indicated that, within the limits of test equipment repeatability, welding environments had no significant affect on collector-base leakage, emitter-base leakage, base-emitter saturation, and collector-emitter saturation. Test equipment repeatability for DC current gain was found to be poor, however, no unexplainable catastrophic failures were detected in post-weld testing. The affects that welding has on DC current gain will be clarified further after testing a confirmation group.

Two techniques for testing the quality of welds have been surveyed; infrared sensing and heat pulse checking. Infrared sensing employs an infrared detector which scans current-carrying welds and wires in search of hot spots. The intensity of the hot spots indicates welds with cross sections below some acceptable value, or wires with reduced cross sections due to adjacent burned welds. The second technique, which seems the more feasible, employs a heat pulse applied at some point on the wire close to a weld. The decay of the pulse through the weld is compared to the decay of the pulse on the continuation of the incident wire. The quality of the weld is determined by comparing the energy passing through the weld to that passing down the incident wire. Further verification of this technique is needed to insure that all bad welds will be found.

2.5 EVALUATION OF MICROLOGIC CIRCUITS

A micrologic element is a logic-function integrated in a single microminiature transistor-like device that can be interconnected to perform the logic required in digital computers. The Apollo Guidance Computer utilizes direct-coupled-transistor-logic (DCTL) micrologic elements since they most closely meet the Apollo program requirements of high reliability, low power consumption, high speed, and minimum components. The micrologic elements used operate over a temperature range of -55°C to +125°C, with an average delay of 50 nsec, and an average dissipation power of 15 mw. Each element can drive up to 5 other micrologic loads in parallel. The miniaturization achieved using micrologic, in particular the high-density packaging and low power consumption, is of significant value to the AGC.

Raytheon Company has instituted, and is currently engaged in, an exhaustive evaluation program on micrologic units. A considerable number of tests have been designed and performed to reveal the characteristics of these devices. These tests have been grouped to completely evaluate the following conditions of operation:

a.	Hold-on	A condition in which the element (or circuit) is maintained in the ON state
b.	Hold-off	A condition in which the element (or circuit) is maintained in the OFF state
c.	Turn-on delay	The length of time between application of input signal and attainment of a saturated condition (OFF to ON)
d.	Turn-off delay	The length of time required to change from the saturated condition to OFF (ON to OFF).

The arrangement of the various parameters that affect these four conditions and the organization of the test groups are shown in figures 2-11 and 2-12. Turn-on and hold-on are covered by the same group of tests; the same is true for turn-off and hold-off.

The basic micrologic circuit used in the AGC is the NOR gate shown schematically in figure 2-13. The circuit is a relatively simple one consisting of a transistor for each input and a single collector resistor. Two worst-case types of the micrologic element are defined as follows:

a. Easy-on: an element which readily saturates and presents maximum load to its driving stage. An easy-on element is characterized by:
   1. minimum R_B
   2. minimum V_{BE} threshold
   3. maximum h_{fe}
   4. maximum R_L
   5. minimum V_{CE} sat

b. Easy-off: an element characterized by parameters exactly opposite to those of the easy-on element.

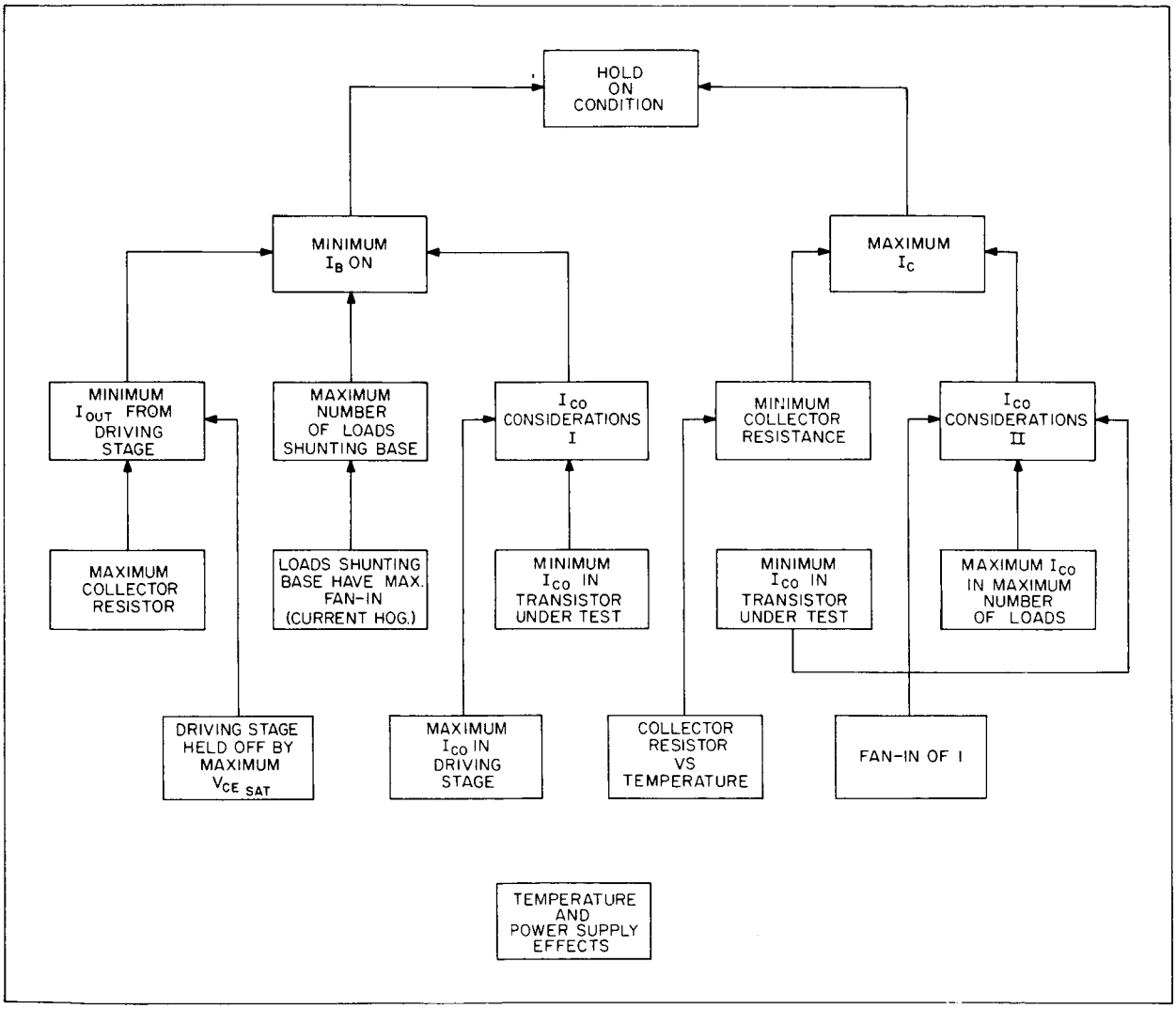


Figure 2-11 - Hold-on Parameters

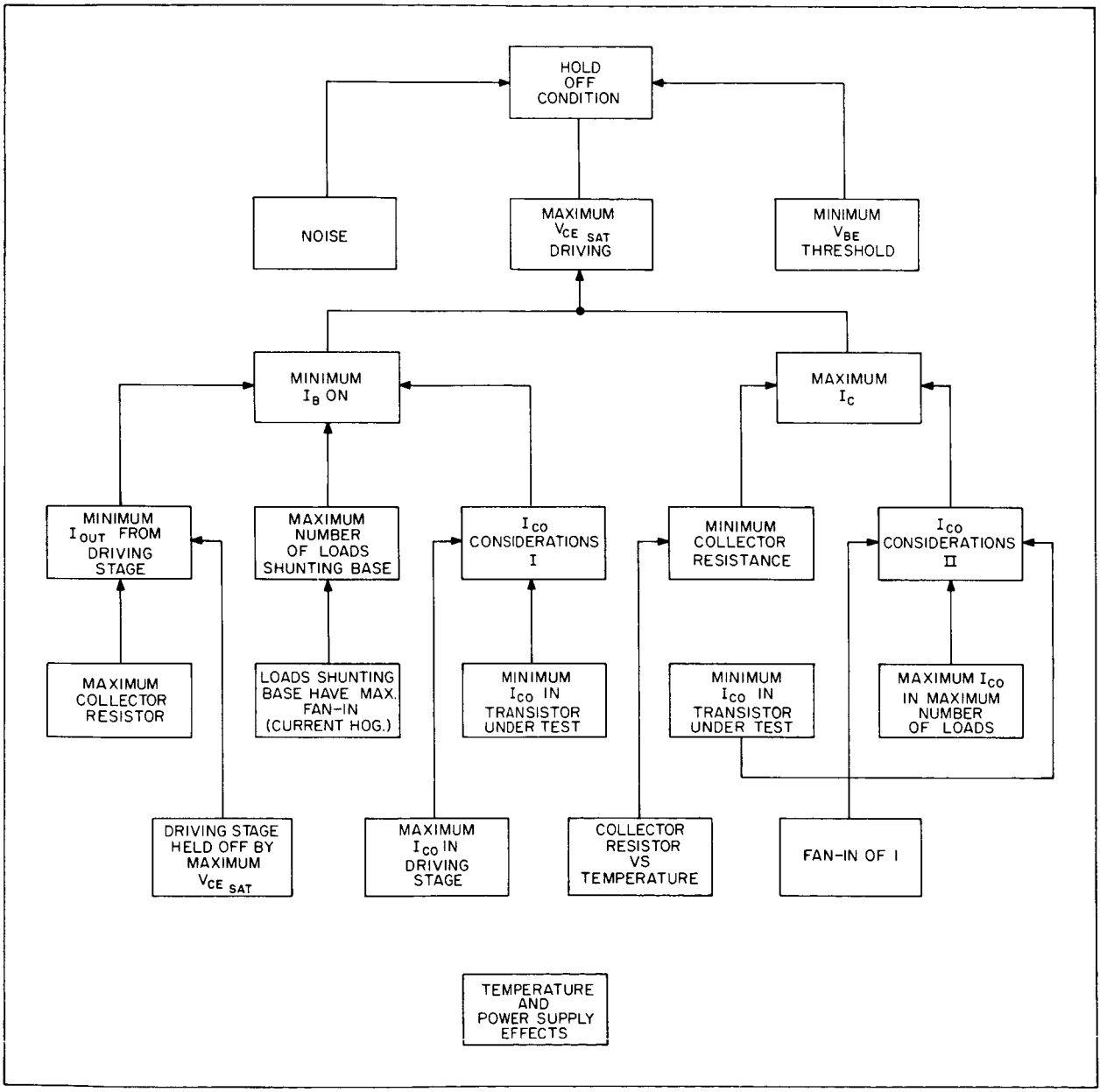


Figure 2-12 - Hold-off Parameters

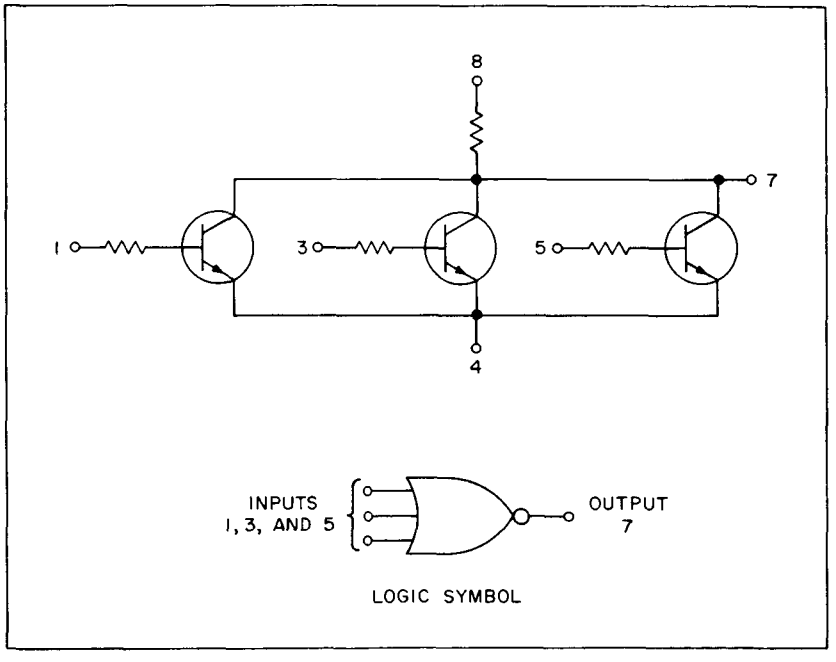


Figure 2-13 - Basic NOR Gate, Schematic Diagram

R_B, R_L, and V_{BE} are not independent parameters. The individual components within the element which contribute to these parameters are simultaneously diffused during the manufacturing process. Usually they will be on the same side of the tolerance specification.

A relatively simple circuit (figure 2-14) can be used which represent simultaneously worst-case conditions for both ON and OFF states. The worst-case condition for hold-on requires a maximum I_c, minimum I_b and an easy-off element. To accomplish this in unit 2 an easy-off type element is required. To obtain maximum I_c, the loads (units 1 and 3; S1 is closed) must exhibit maximum I_{cbo} while I_{cbo} in unit 2 must be a minimum. Collector resistor R_{L2} must also be a minimum value. I_o from unit 1 must be a minimum for minimum base current. Therefore, R_{L1} must be a maximum value and the base of unit 1 must be only slightly biased off with a maximum "zero" which unit 2 supplies via the feedback loop. To complete the condition for minimum I_b in unit 2 the base must be shunted by a maximum number of loads each having a fan-in of three.

The worst-case condition for hold-off requires an easy-on element and an easy-off element with minimum I_b driving the base. Conditions already described satisfy these requirements.

The worst-case condition for turn-on delay requires maximum I_c, minimum I_b, an easy-off element, and maximum capacitance at input and output. Conditions already described satisfy these requirements. The capacitance is supplied by approximately 30 mmf connected to the circuit.

The worst-case condition for turn-off delay requires minimum I_c, maximum $\frac{I_{b_{on}}}{I_{b_{off}}}$, an easy-on element, and maximum capacitance. In the test circuit, S1 must be open and unit 3 must be considered. Minimum I_c here requires a

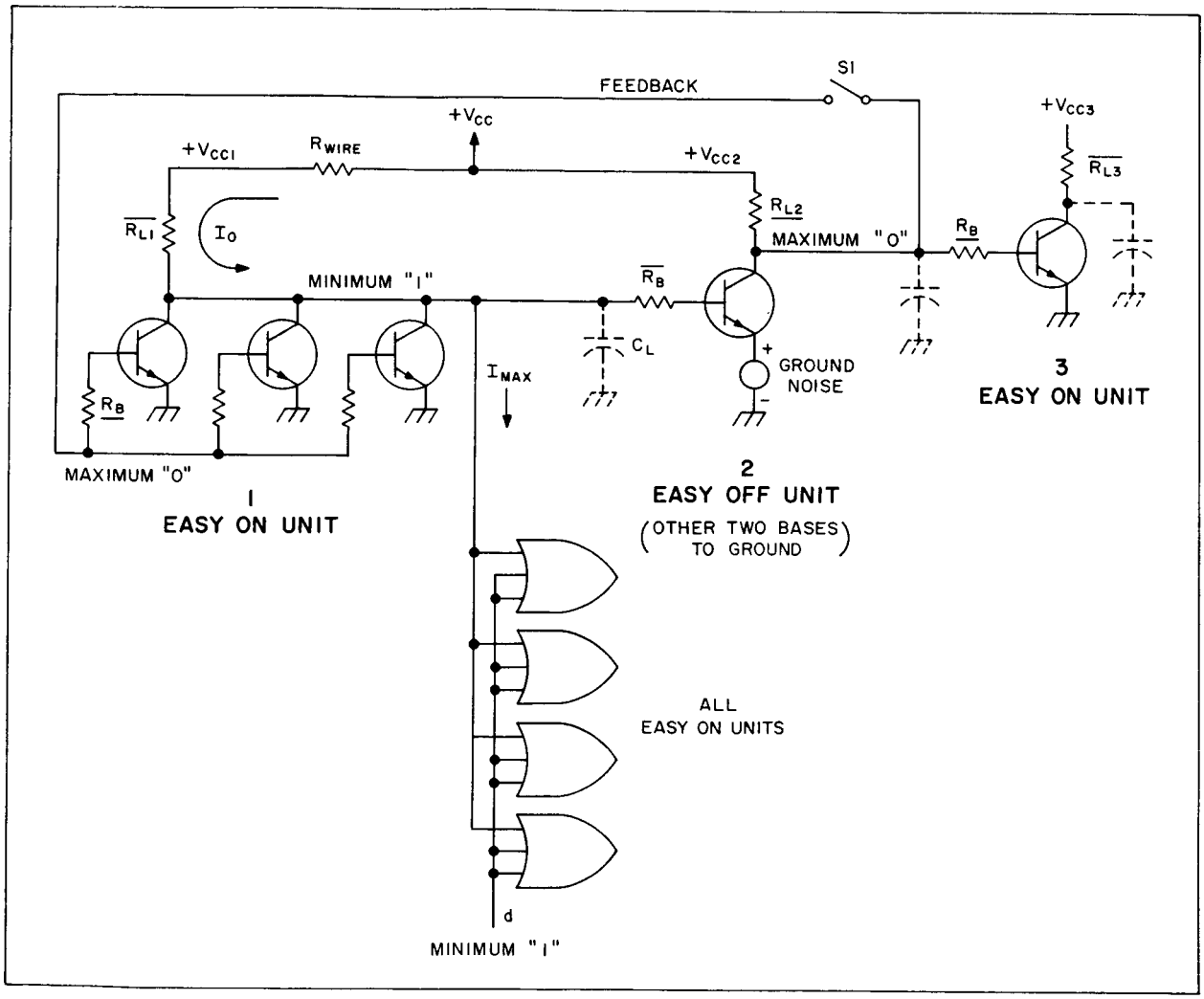


Figure 2-14 - Model Circuit

maximum value for R_{L3}. The only remaining significant parameter is the ratio $\frac{I_{b_{on}}}{I_{b_{off}}}$. Conditions already discussed provide a maximum $I_{b_{on}}$. Base current in the reverse direction must be applied to the saturated base to move unit 3 out of saturation. This current is supplied through the ON collector driving the base of unit 3. Unit 3 will be "starved" for turn-off base current because the collector current from unit 2 is already restricted to a minimum value. A meaningful turn-off delay measurement requires a worst-case element in unit 2 so that no excess collector current is available to discharge unit 3.

In the process of manufacturing a micrologic NOR gate element, a resistance, commonly called the collector resistance, is diffused into the silicon chip. Boron is used as the diffusing impurity in a high-temperature diffusing process. The basic NOR gate element utilizes a common collector resistor which has the most influence on the element in the hold-on condition. An extensive investigation was conducted on this resistor to verify its known characteristics as well as to gain insight into how and why the resistor influences hold-on.

2.5.1 MAXIMUM COLLECTOR RESISTOR

The maximum collector resistor parameter affects the minimum Iout parameter from the driving stage. This parameter, in turn, affects the minimum $I_{b_{on}}$ parameter which directly affects the hold-on condition as shown in figure 2-11.

The maximum resistance as calculated from NASA specification 1006771 is 651 ohms. Any resistance greater than 651 ohms will limit the available current supplying the bases connected to the collector node. If the available current to these bases is limited by a value of R_C higher than 651 ohms then some or all of these bases may be forced out of saturation. Thus, the

hold-on status of any stages connected to an OFF collector node is directly affected by the value of the collector resistor at that node.

2.5.2 MINIMUM COLLECTOR RESISTANCE

The minimum collector resistance affects the maximum I_C parameter which directly affects the hold-on condition as shown in figure 2-11. The minimum collector resistance value has been established by NASA specification as 510 ohms. A minimum R_C causes a maximum I_C. The increased collector current will cause the internal base-emitter voltage drop of the stage being driven to increase due to R_e. If a transistor has its base clamped by other bases that are attached to the same collector node then, the current into that base will decrease. If this transistor is an "easy-off" unit then it may be forced out of saturation. This situation only occurs under certain logic conditions; namely, when an "easy-off" unit is base connected back to a collector node which is connected to several other bases. This configuration is used often and therefore becomes an important consideration.

2.5.3 COLLECTOR RESISTANCE VERSUS TEMPERATURE

Two procedures were used to determine the resistance change with temperature. Under the first, each of the collector resistances of chosen sampling of elements was monitored with a General Radio Impedance Bridge. The second method tested the same resistances under voltage-current conditions. Comparison of the data taken by both methods indicates that within the dissipation range of 7.1 to 21.8 mw the resistors were of the same value. Any differences can be attributed mainly to instrumentation tolerances. The resistance change is approximately 0.5 ohms/^{o}C for the -55^{o}C to 0^{o}C and +70^{o}C to 100^{o}C ranges, and 1 ohm/^{o}C for the 0^{o}C to +70^{o}C range. These values are determined from the slope of the curves in figures 2-15 and 2-16.

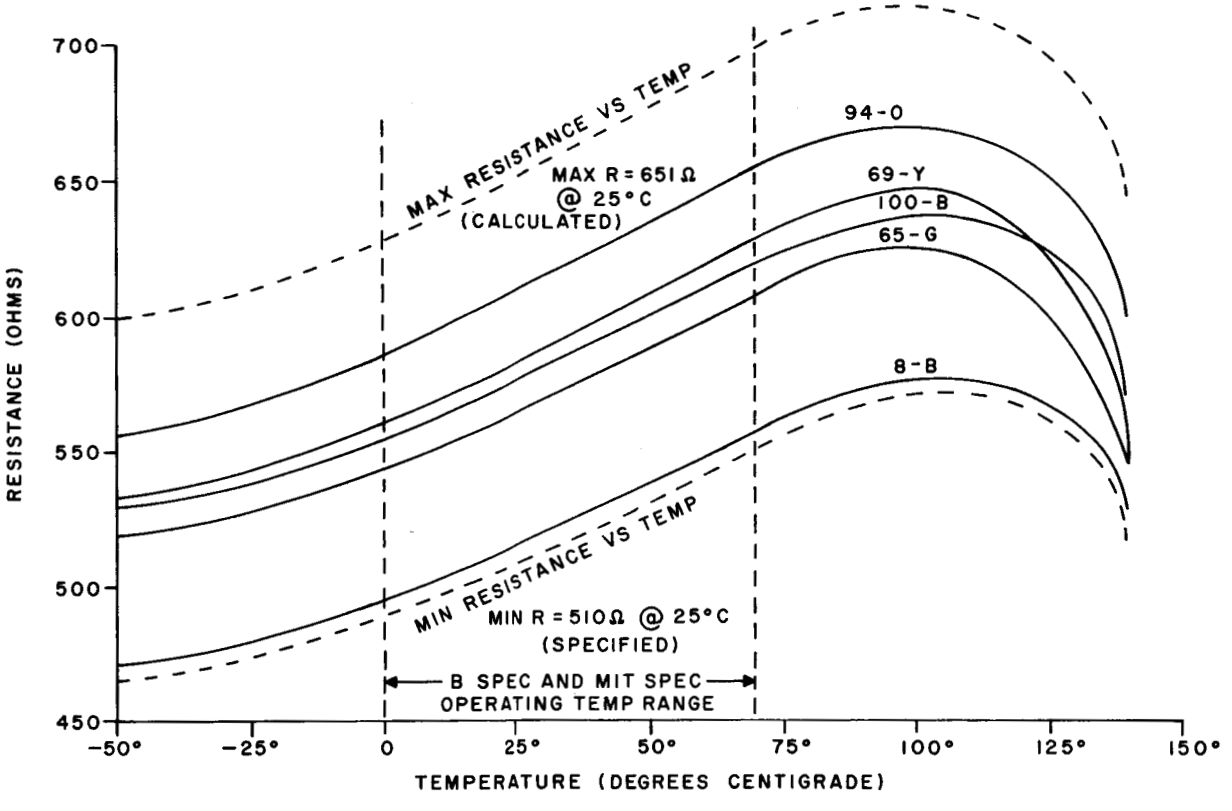


Figure 2-15. Collector Resistance vs Temperature (Monitored by GR Bridge)

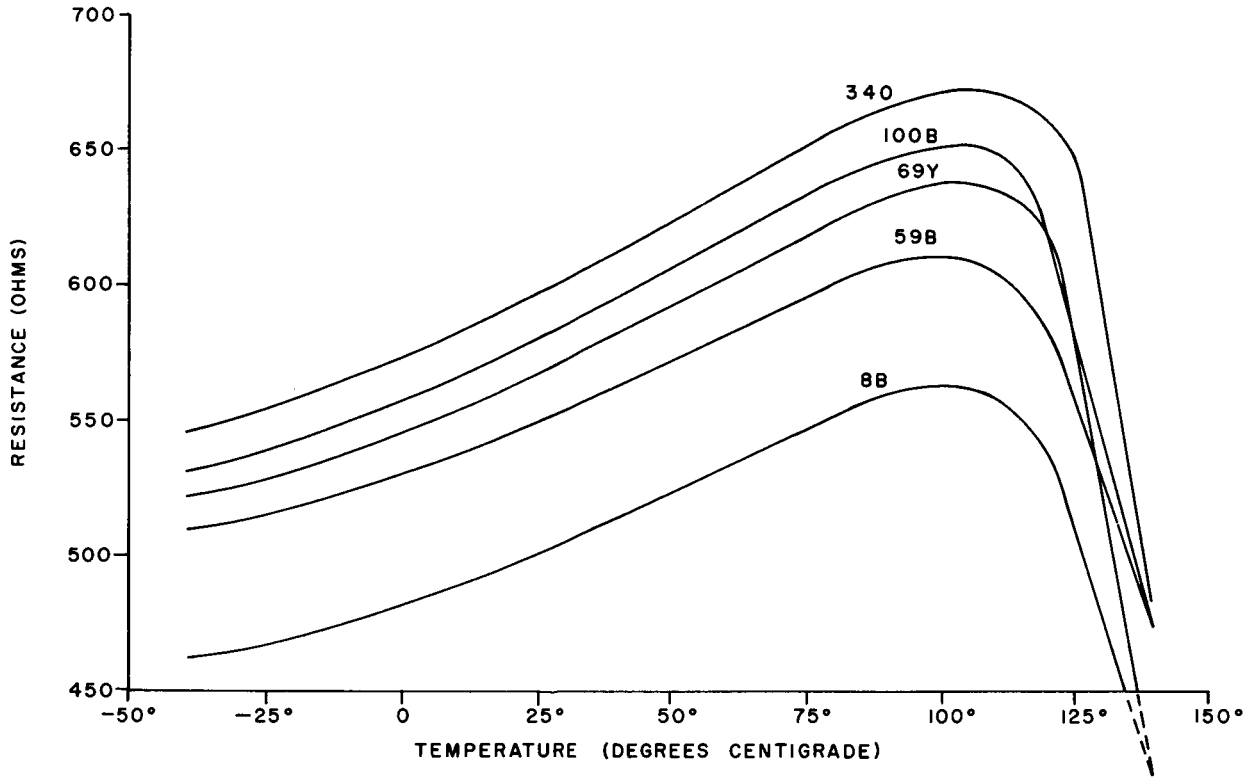


Figure 2-16. Collector Resistance vs Temperature (Calculated)

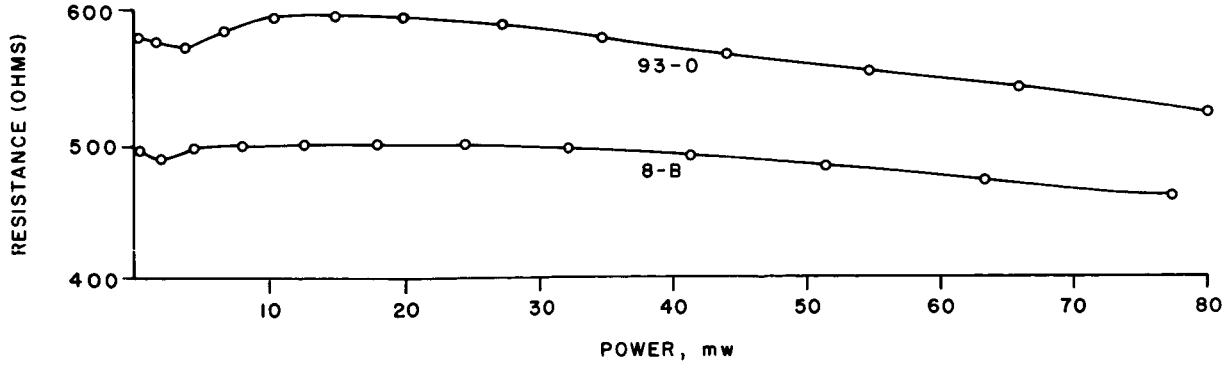


Figure 2-17. Collector Resistance vs Power Dissipation

With regard to the temperature range specification of 0°C to +70°C, the maximum worst-case value of R_c occurs at +70°C (figure 2-15). Effects of aging this resistance will be investigated shortly. The worst-case minimum resistance, disregarding aging, occurs when the minimum acceptable value of R_c of 510 ohms is operating at 0°C, within the maximum worst-case dissipation limit of 21.8 mw. Its value is then 485 ohms. The worst-case maximum resistance, disregarding aging, occurs when the maximum acceptable value of R_c of 651 ohms is operating at 70°C, within the maximum worst-case dissipation limit of 21.8 mw. Its value is then 696 ohms.

2.5.4 COLLECTOR RESISTANCE VERSUS DISSIPATION

During the test of collector resistance change vs power dissipation, the voltage across the collector resistors of two units was varied and the current measured. The resistance value was then calculated and plotted as shown in figure 2-17.

Under actual operation, the typical dissipation of the "G" element is about 15 mw. For a typical case, the collector current might be 4.6 ma, and the saturation voltage might be 0.330V. The R_c dissipation is then 12.3 mw. The remaining 2.7 mw is being dissipated by the transistors biased ON within the "G" element.

It can be seen from figure 2-17 that the resistance changes very little over the 7.1 to 21.8 mw power range. This provides justification for the 7.1 mw minimum and 21.8 mw maximum worst-case R_c dissipation limits.

2.5.5 MAXIMUM AND MINIMUM WORST-CASE COLLECTOR RESISTOR POWER DISSIPATION

The following is a calculation of the worst-case maximum and minimum P_{Rc} figures.

a. Maximum P_{Rc} occurs under the following conditions:

1. Supply voltage, maximum worst-case = 3.35 vdc
2. R_c at 25°C, minimum = 510 ohms
3. Temperature, minimum = 0°C
4. Saturation voltage, V_{ces}, minimum at 0°C = 0.096 vdc

Worst-case P_{Rc} maximum is then

$$\frac{(3.35 - 0.096)^2}{510-25} = 21.8 \text{ mw}$$

b. Minimum P_{Rc} occurs under the following conditions:

1. Supply voltage, minimum worst-case = 2.65 vdc
2. R_c at 25°C maximum = 651 ohms
3. Temperature, maximum = +70°C
4. Saturation voltage, V_{ces}, maximum = 0.40 vdc at 25°C
   0.423 vdc at 70°C

Worst-case P_{Rc} minimum is then

$$\frac{(2.65 - 0.423)^2}{651 + 45} = 7.1 \text{ mw}$$

2.6 BREADBOARD COMPUTER AGC 4A

Fabrication of the AGC 4A breadboard computer is proceeding on schedule. The breadboard is illustrated on figure 2-18. A preliminary diagnostic and exercising program for the breadboard computer has been written. The program consists of two parts; an instruction check which occupies 259 memory locations, and an erasable memory check which occupies 118 memory locations. In addition, 30 locations are necessary to store temporary data and constants. The program is formulated in a series of separate flow charts tc keep it as flexible as possible, each flow chart being an independent program in itself. Each independent program can be joined to another independent program or arranged to loop within itself.

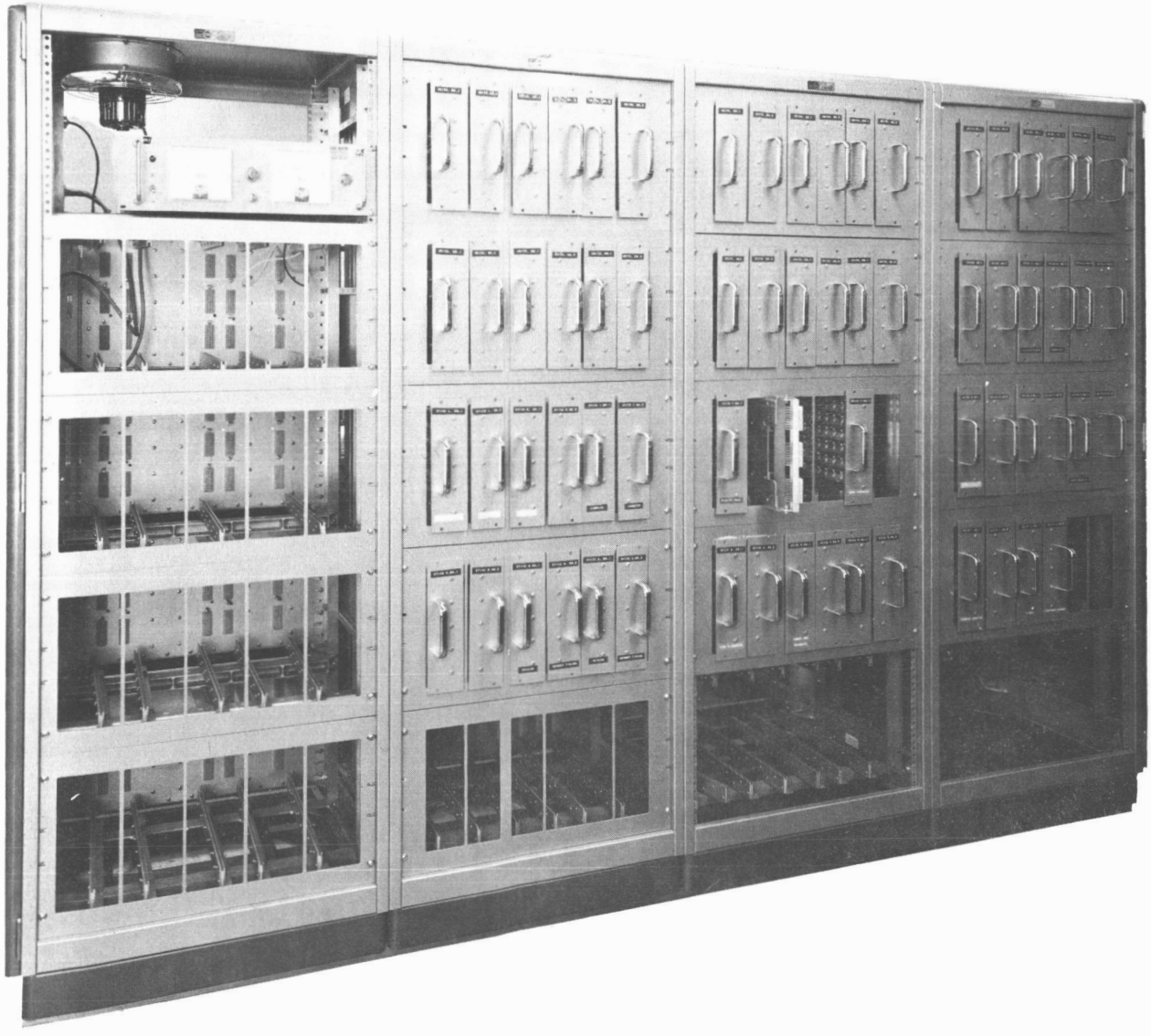


Figure 2-18. AGC 4A Breadboard Computer

A ONEs check program and an ADD loop program, shown in figures 2-19 and 2-20 respectively, are examples of the type of programs used. The ONEs check program provides a means of checking that all ONEs can be written into and read out of all erasable memory locations. The ADD loop program utilizes the AD instruction to propagate all ones from the least significant bit to the most significant bit. Provisions are incorporated in these and the other programs to stop on error. If testing is performed with the Computer Test Set, the operator may arbitrarily designate an address at which to stop. If an error is detected during a program cycle, testing will be halted at that address, regardless of where it occurs in the program cycle. A means will be provided in the checkout equipment to determine the location of the error. Depending on the type of error and where it occurred, various techniques will be performed to isolate and correct the malfunction.

The ideal place to enter the erasable memory check portion of the program is in fixed memory. In addition, if this memory check program is wired into a core rope it could serve the dual function of debugging the logic of the breadboard computer as well as testing the circuitry of the rope. If the entire program is entered into erasable memory, it will occupy approximately 40 percent of the locations. This will not provide an adequate check of the memory since only 60 percent of the locations are available for checking. If only the erasable memory check portion of the program plus the temporary data and constants are entered into erasable memory, 90 percent of the locations would be available for checking.

The diagnostic and exercising program can also be used as an exercising routine for the breadboard computer. After the breadboard computer has been checked-out, diagnostic programs can be run during "open" time (the time when no computations are being performed) to provide a check on the seldom used logic of the computer to insure that no error failure has occurred in the logic. The program in its present form may require some modification

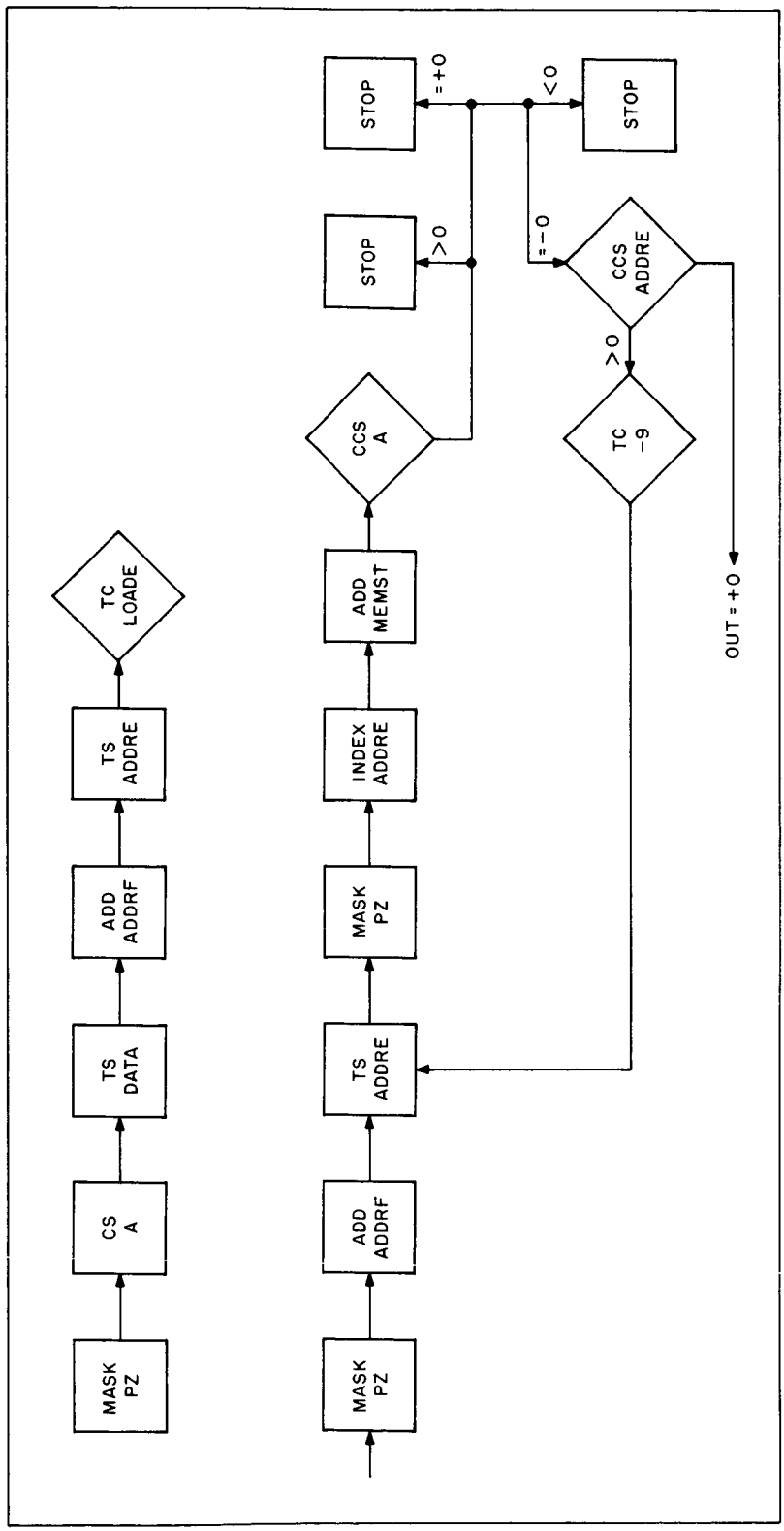


Figure 2-19 - ONEs Check Program

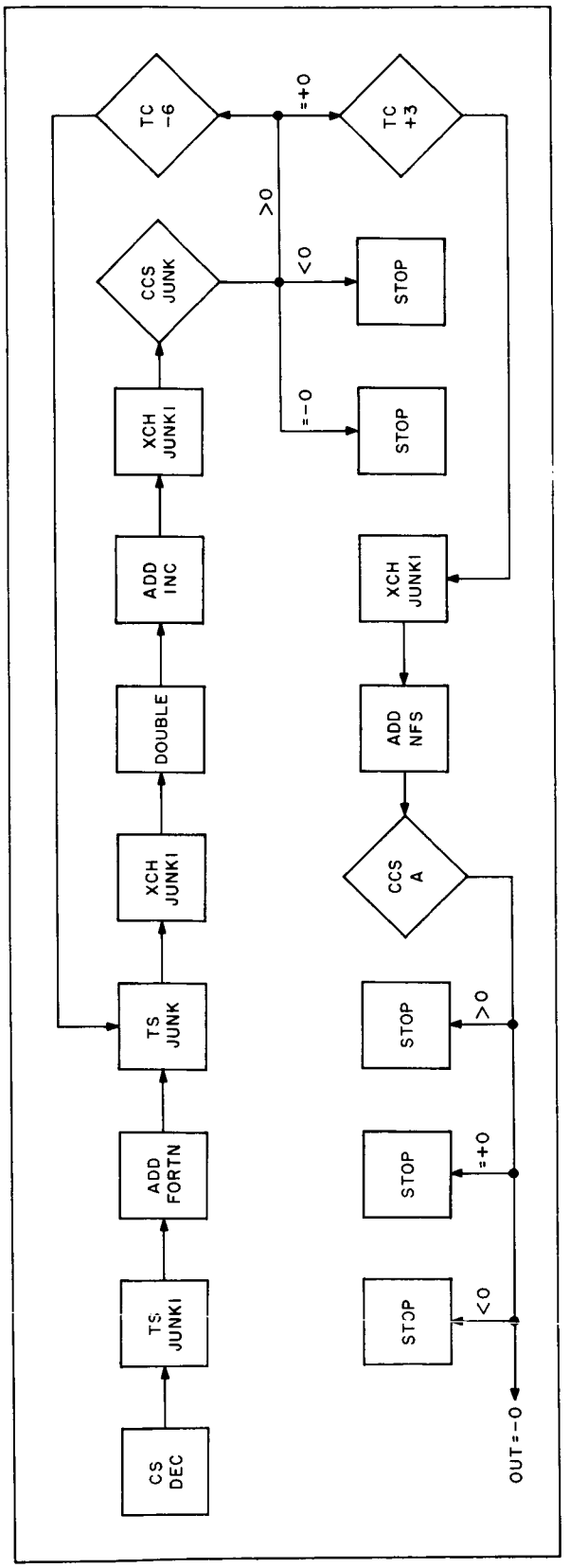


Figure 2-20 - ADD Loop Program

as computer operation becomes more and more defined, however, it is anticipated that it will, in whole or in part, be one of the tools utilized to check-out the AGC 4A breadboard computer.

SECTION III
GROUND SUPPORT EQUIPMENT

SECTION III
GROUND SUPPORT EQUIPMENT

3.1 INTRODUCTION

The responsibility for the design and fabrication of Ground Support Equipment for the AGC was presented to Raytheon by MIT/IL. The equipment had to be designed to meet the following requirements: (1) independently checkout the AGC, (2) enable performance of open loop tests on IMU, CDU, and PSA, (3) check the AGC oscillator, and (4) check the AGC, when operating as part of a G & N system, prior to installation in the Spacecraft. In order to implement the above requirements, Raytheon has designed the Computer Test Set, Computer Simulator, and Computer Calibration Equipment. With these three pieces of equipment it will be possible to perform diagnostic tests on the AGC system during subsystem and system tests, and analyze any malfunction which might occur.

3.2 COMPUTER TEST SET

The Computer Test Set (CTS) will be a self-contained test set used to evaluate dynamic operation of the AGC. The CTS will automatically or manually simulate conditions encountered by the AGC, evaluate computer response to these conditions, and check the integral computer circuits required to generate proper response. The CTS will perform subsystem and system tests and generate signals to perform self-tests.

The CTS (figure 3-1) will consist of a two-bay console containing twelve units of test equipment and four DC power supplies. In addition, a caster-mounted single-bay console (not shown) will contain two Display and Control panels and provisions for supporting the AGC and coldplate during subsystem tests.

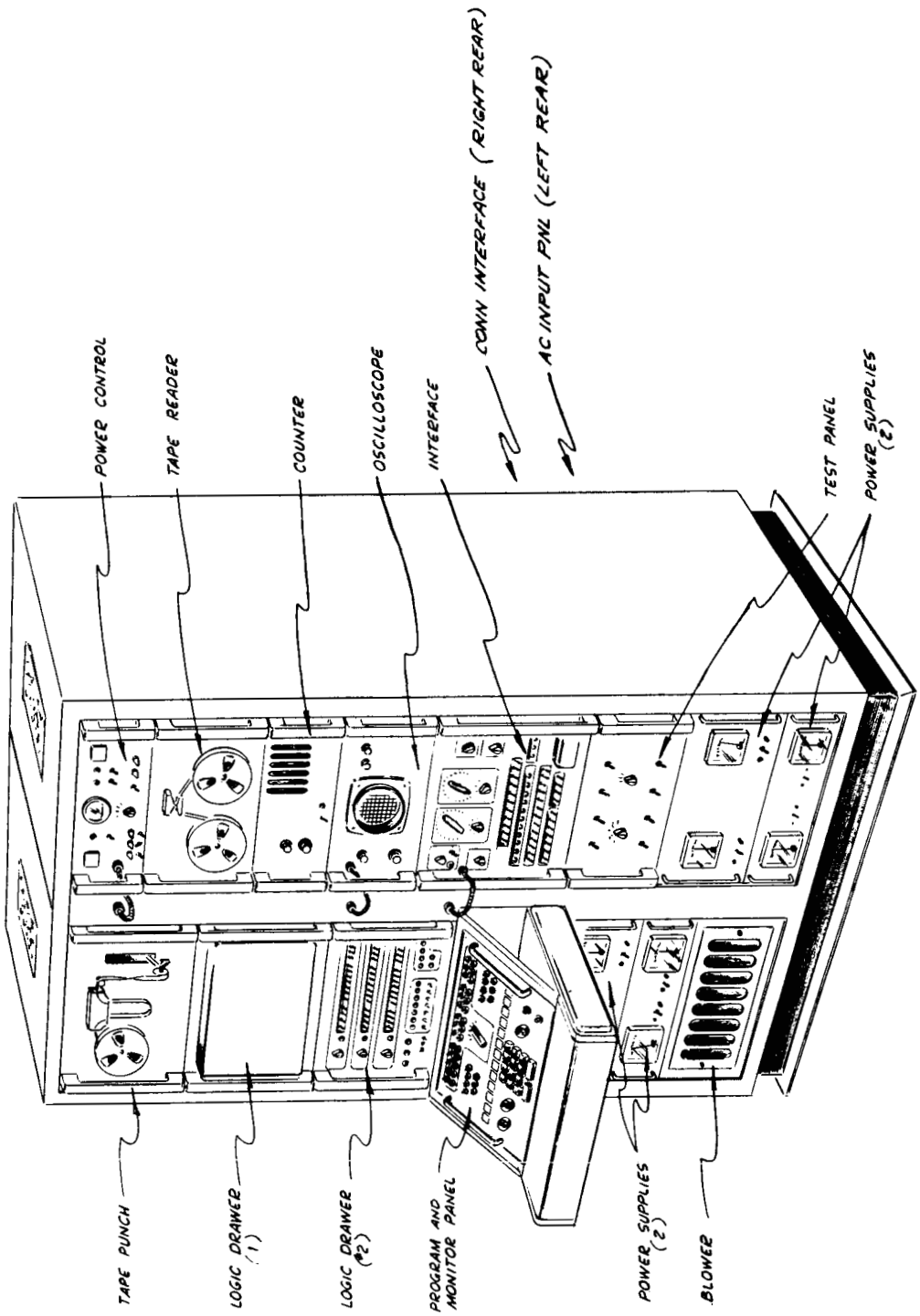


Figure 3-1. Computer Test Set

The CTS will be capable of the following:

a. Provide mounting, power, and cooling for a production type AGC during subsystem test.

b. Provide mounting for the two associated production type AGC D and C panels during subsystem test.

c. Provide interconnection between the AGC and the two D and C panels.

d. Provide means for direct program control, including stopping or stepping a program.

e. Provide continuous or sampled monitoring of the special and central registers of the AGC, or monitoring of selected memory locations.

f. Provide monitoring of key AGC program functions.

g. Provide dummy loading for AGC outputs.

h. Provide the logic, hardware, and commercial equipment required for loading programs or data into the AGC, provide for signals into the AGC inputs, and provide for complete test of AGC operation.

i. Provide means to generate or duplicate paper tape for loading the AGC.

j. Provide a means of communication with the AGC during system test external to the Spacecraft, formatting and recording digital data by tape punch, converting and recording analog data on channels of a strip chart recorder (not provided), and displaying the contents of selected addresses.

k. Self test.

The CTS will operate in conjunction with the System Checkout Equipment to perform system tests on the Guidance and Navigation System. It will connect to the AGC and the Guidance and Navigation System through appropriate interface circuitry and will provide direct program control for monitoring the

special and central registers of the AGC and for some key logic functions associated with AGC internal program control.

Ordinarily, an AGC stop is forbidden during system test. If a stop is permitted, the CTS can load programs into erasable memory or perform troubleshooting functions. Since loading of erasable memory is performed in the stop mode, the Display and Control panels will normally be used for small changes (changing constants, scale factors, etc.) during system tests and for reading and displaying the contents of a selected location in erasable memory after loading.

Fabrication of the breadboard Computer Test Set (figure 3-2) has begun. The logic design has been completed, with the exception of the self-test feature. Wrapost plates and interconnection plates have been installed in racks and the AC wiring is in progress. Modules and interconnection cables are being fabricated. To date, two-hundred modules have been completed. Tests on these modules will begin shortly. All commercial equipment for the breadboard computer test set has been ordered.

3.3 COMPUTER SIMULATOR

The purpose of the Computer Simulator is to provide drive rates, identical with those of the AGC, for use by inertial systems equipment. The simulator is not intended to replace the AGC during systems tests however.

The Computer Simulator is a compact, slide-mounted logic drawer, containing three vertically mounted logic plate assemblies, a vertically mounted DC power supply assembly, a hinged interconnection plate, and a hinged front panel. The basic structure, designed to fit into a standard 19-inch rack, consists of a wrap-around chassis 17 inches wide, 10 inches high, and 24 inches deep, exclusive of front panel. The front panel is 12-1/4 inches highes and 19 inches

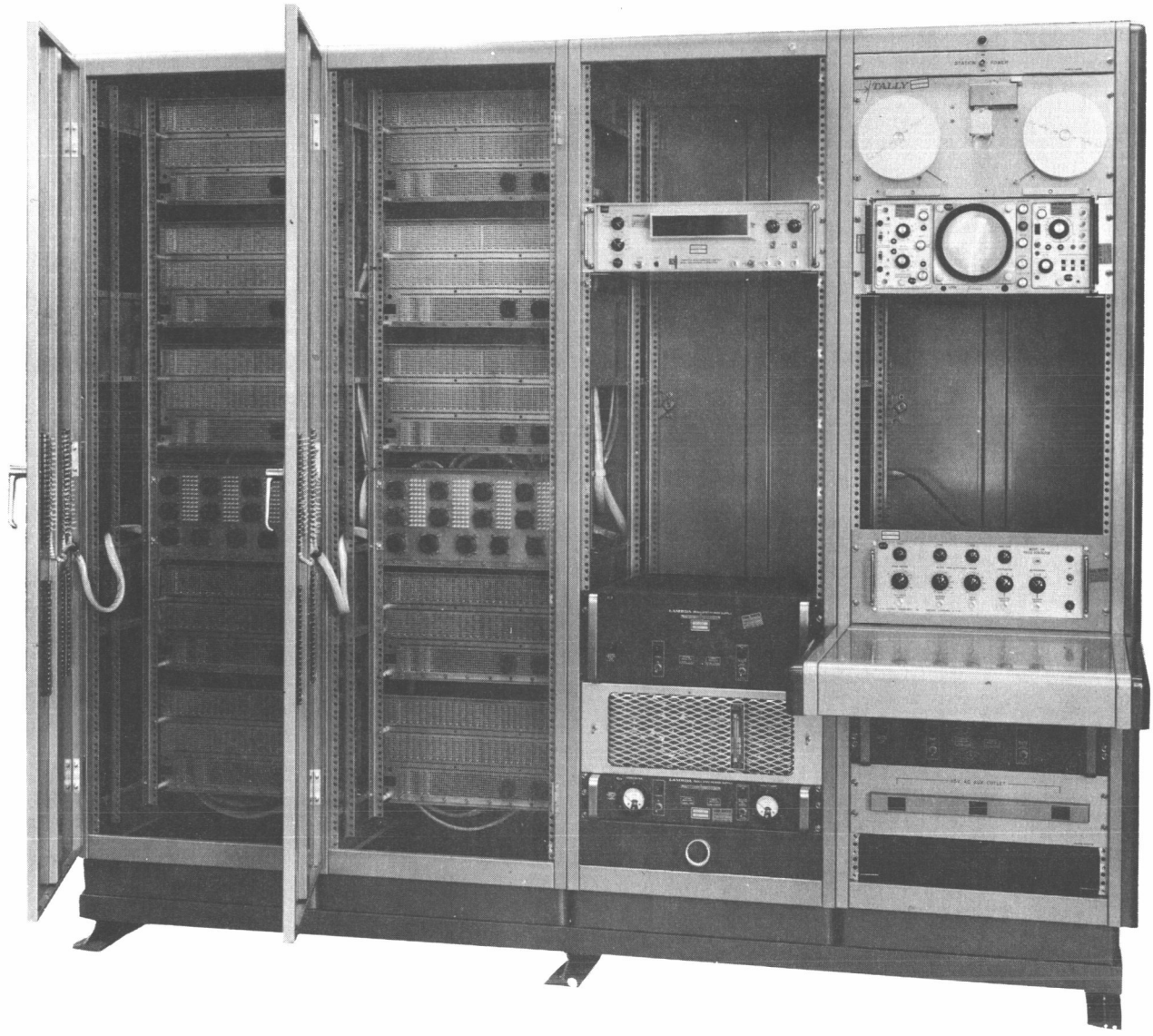


Figure 3-2. Breadboard Computer Test Set

wide and provides radio frequency interference (FRI) shielding. Ducts are provided in the base of the chassis to permit cooling of the drawer contents.

The logic plates are slide-mounted in the chassis and are fastened at each end by captive screws. Each logic plate is capable of holding 64 GSE modules and 2 cable assembly plugs, each of which is three module spaces wide. Interconnections between the logic plate assemblies, DC power supply assembly, front panel, and external connectors are provided by cable assemblies and the wire-wrapped interconnection plate. A logic plate, fully loaded, weighs approximately 15 pounds. These logic plates can be raised to permit servicing when the drawer is fully extended.

There are seven types of GSE modules used in the Computer Simulator: NOR (AC), interface coupling (CR), gated flip-flop (KH), diode (HF), resistor (FD), driver (MK), and transformer driver (DA). Modules are plugged into one side of the logic plate assemblies and are fastened with captive screws. Interconnections within the modules are resistance spot welded. Wirewrap, on the underside of the logic plate assemblies, provides interconnections between modules. Interconnections to other circuits are provided by a moulded connector, containing 20 feed-through pins, that raises the height of the modules on the circuit side of the connector. The module structure provides wrap-around protection for the circuits. Notches are provided on the modules to permit the use of an extracting tool.

The DC power supply assembly occupies the amount of space normally allotted to two logic plates in a standard GSE logic drawer. The assembly consists of two modular regulated power supplies and two crystal-can relays, mounted in inverted positions. Input to the assembly is 115 vac, single phase, 60 cps. A single cable assembly connects the DC power supply assembly to the interconnection plate which distributes power throughout the simulator.

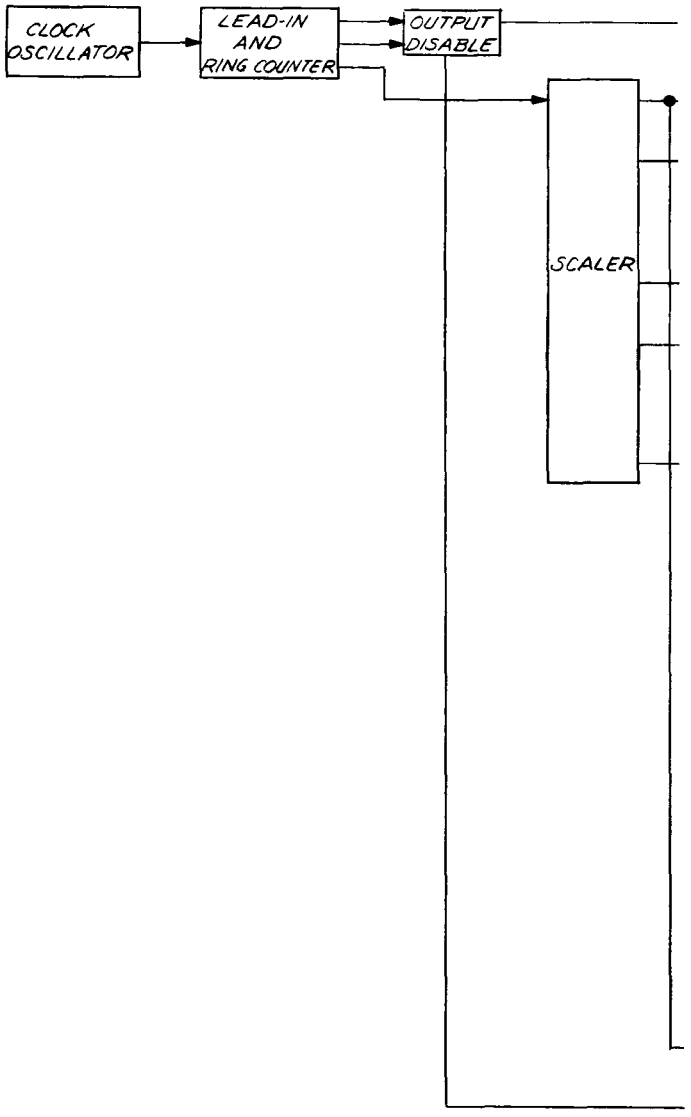
The interconnection plate is identical in size and general construction to the logic plates. The interconnection plate is hinged at the bottom and attached at the top by captive screws. The plate tilts forward to permit easy access to the inside of the drawer, cables, and internal connectors. Stops are provided on the side of the chassis structure to prevent the interconnection plate from coming in contact with the front panel.

The front panel assembly is attached to the chassis structure by hinges at each bottom corner and at the top by captive screws. The captive screws are only accessible from the rear of the panel. The simulator must be withdrawn from the rack before the front panel can tilt forward to permit access to the interconnection plate and drawer contents. Handles on the panel facilitate removal of the simulator from the rack. All the controls and indicators necessary to operate the simulator are mounted on the front panel.

The Computer Simulator produces drive rates identical with those of the AGC by generating a bi-phase clock frequency, dividing it, and modifying the results of the division to produce the desired outputs.

The simulator contains circuits for the selection of inputs to the Guidance and Navigation Subsystem. A block diagram of the simulator is shown in figure 3-3. These circuits utilize the pulse trains generated by modifying the clock output to provide one of three specialized input signals to the G & N. The choice of which one of the three to be used is the decision of the operator and is manually selected through front panel switches. Provisions are also included to permit operation of the simulator from a remote location.

The logic diagrams for the prototype Computer Simulator have been completed. Changes have been made to the prototype simulator to incorporate the latest requirements outlined by MIT/IL. Further refinements are being made to the simulator which include provisions for buffering from the CDU encoder, optics



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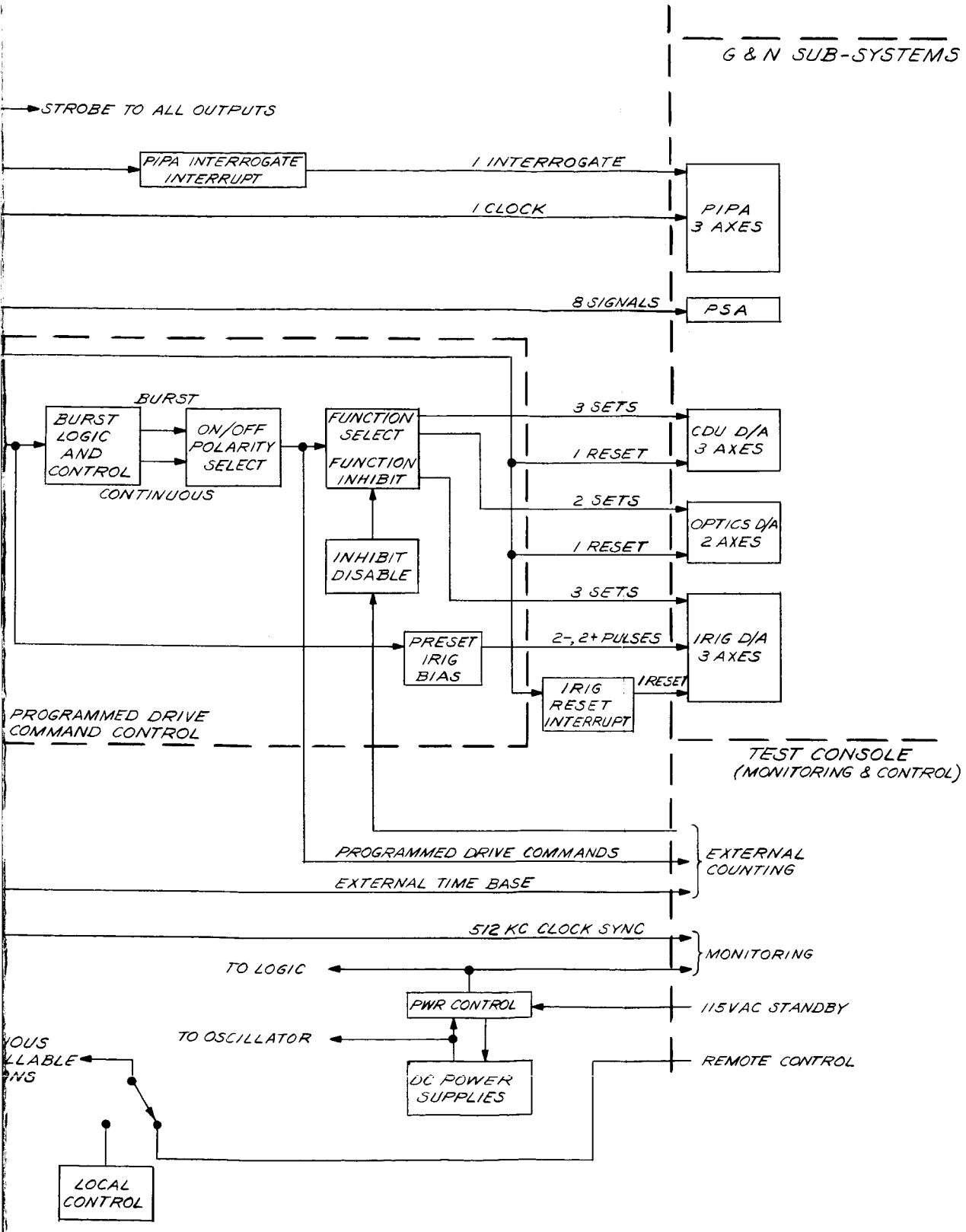

Figure 3-3. Computer Simulator Block Diagram

encoder, and PIPA as well as provisions for additional time bases. The former necessitated the design of a new module to provide the simulated AGC input. The breadboard simulator (figure 3-4) is also being revised to incorporate all of the above changes.

3.4 COMPUTER CALIBRATION EQUIPMENT

The Apollo Guidance Computer Calibration Equipment (figure 3-5) consists of five units of test equipment and is used to calibrate the AGC crystal oscillator. The Calibration Equipment consists of a modular-constructed, single rack console, approximately 53 inches high and 24 inches wide, mounted on casters. Rack-mounted in the console and constituting the calibration system is a digital recorder, counter assembly, control and interface panel, VLF comparison receiver, and an oscillator. An antenna, mounted on the top left of the console, provides facilities for receiving RF signals for the VLF receiver. AC power is supplied to the system through an AC input panel located at the rear of the console.

A block diagram of the technique used to check the AGC oscillator is shown in figure 3-6. An 18 kc signal is detected by the receiver and sent to a frequency synthesizer which produces a 100 kc signal that is fed to the phase comparator. A frequency standard of 1 mc is divided down to 100 kc, fed through the resolver and then to the phase comparator. These two 100 kc signals are compared for phase relationship. If there is a phase error, a signal is produced that activates the servomotor to drive the resolver. This resolver drives a digital recorder that indicates how much error there is in the phase of the standard. When an error exists, it is corrected by means of a manual control located on the frequency standard. It is assumed that the incoming 18 kc signal is much more accurate than the signal from the frequency standard; therefore, any error signal produced is due to the standard unit changing frequency.

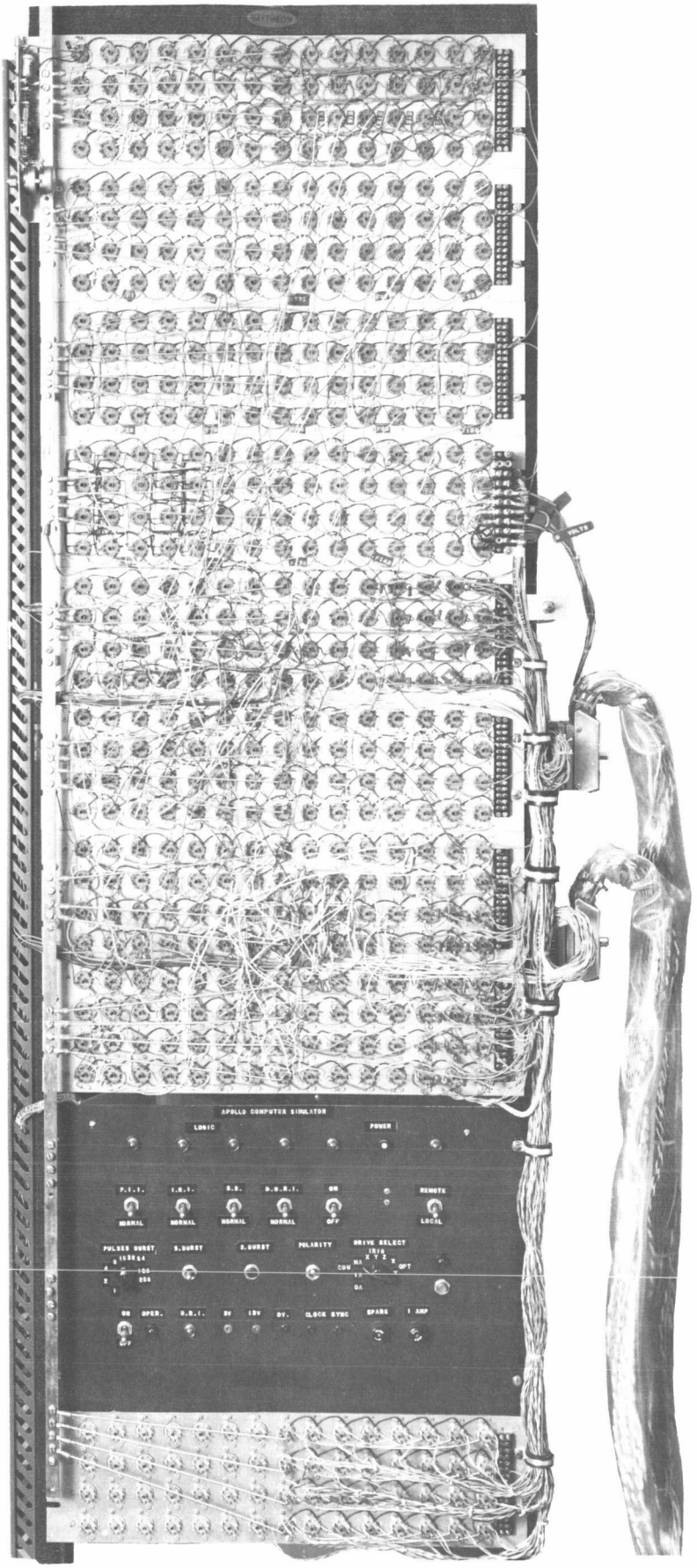

Figure 3-4. Breadboard Computer Simulator

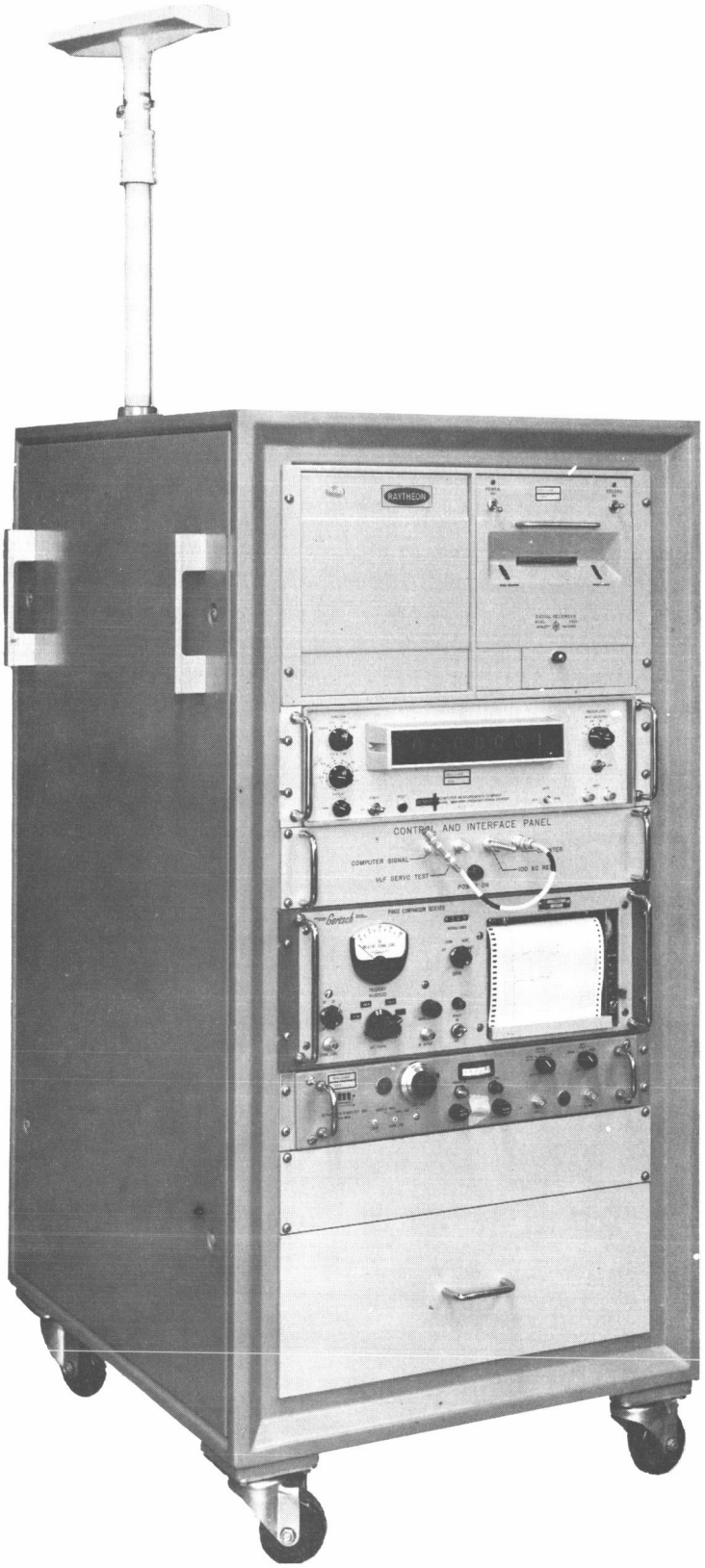

Figure 3-5. Computer Calibration Equipment

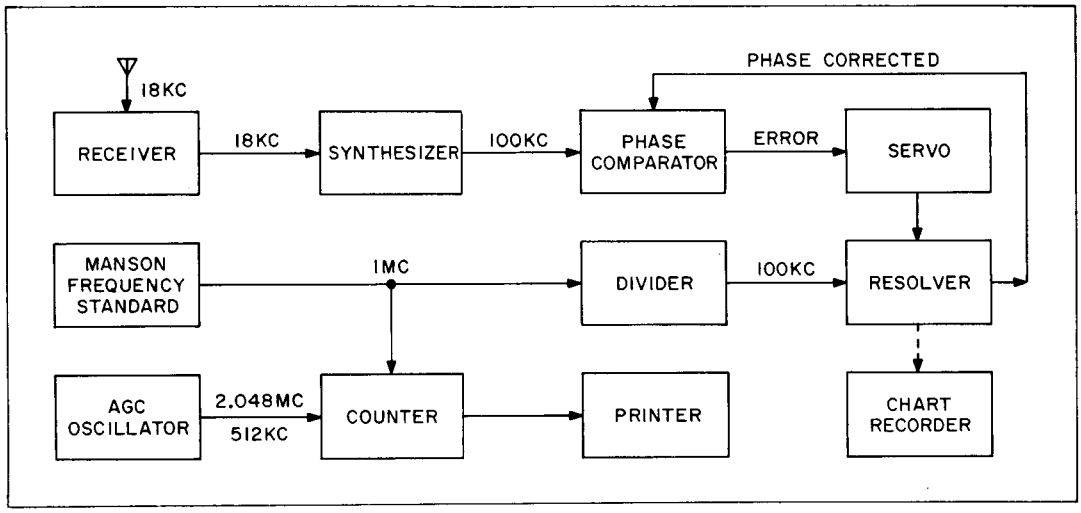

Figure 3-6 - Technique Used to Measure AGC Oscillator Characteristics

The 1 mc output of the calibrated standard is used as the time base of an eight stage counter. The AGC oscillator output (2.048 mc) is fed into this counter. The output of the counter is fed through a printer that records the frequency of the AGC oscillator. Thus, by calibrating the frequency standard with the 18 kc standard, the frequency and aging characteristics of the AGC oscillator can be determined.

Fabrication of the Computer Calibration Equipment has begun. Construction of all cable assemblies has been completed and the commercial equipment is presently being installed in racks. Complete fabrication is anticipated in early April.

SECTION IV
FACTORY TEST EQUIPMENT

SECTION IV
FACTORY TEST EQUIPMENT

4.1 INTRODUCTION

Various tests are required during fabrication of subassemblies and assemblies for AGC and GSE equipments. To satisfy all test situations, it was necessary to design factory test equipment. For this reason Raytheon instituted a Factory Test Plan Board. The purpose of this board was to generate a plan depicting the sequential testing from the component level through the final acceptance test of AGC and GSE.

The GSE Factory Test Plan (figure 4-1) specifies the inspection and electrical tests required during the manufacturing process, including incoming inspection. It provides the basis for fabricating the test equipment and generating test procedures necessary for the implementation of the Factory Test Plan.

The AGC Factory Test Plan (figure 4-2) specifies the inspection and electrical tests required during incoming inspection, screening and burn-in, and assembly. It also defines the test stations and provides the basis for fabricating the test equipment and generating test procedures necessary for the implementation of the Factory Test Plan. The Factory Test Plans will be continually updated under the control of the Factory Test Plan Review Board, insuring that the Factory Test Plans will be effective planning documents.

Some of the equipment being designed to meet the requirements of the Factory Test Plan Board are discussed in the following paragraphs.

4.2 CORE ROPE SIMULATOR

The purpose of the Core Rope Simulator is to provide a practical tool for the

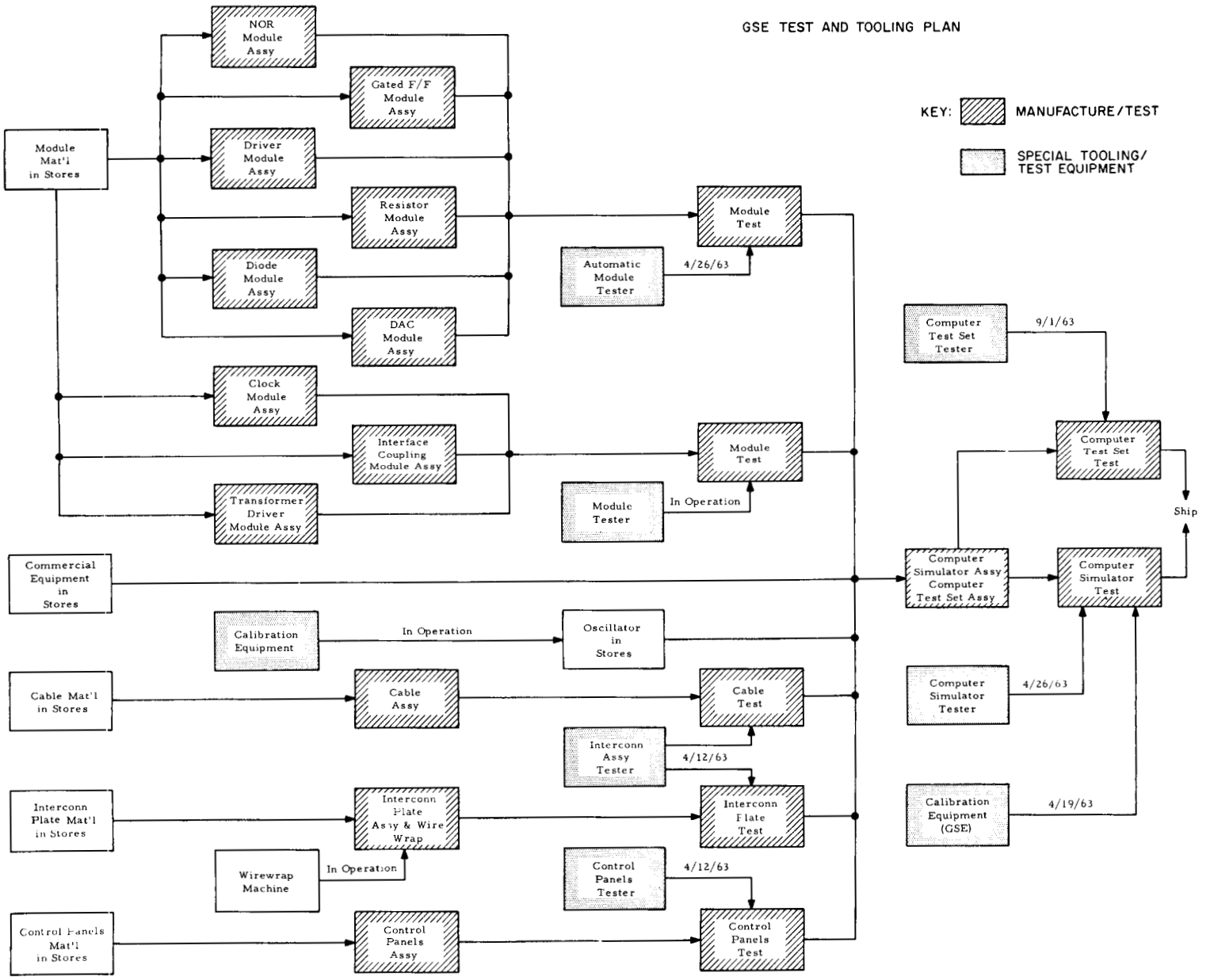

Figure 4-1. GSE Factory Test Plan

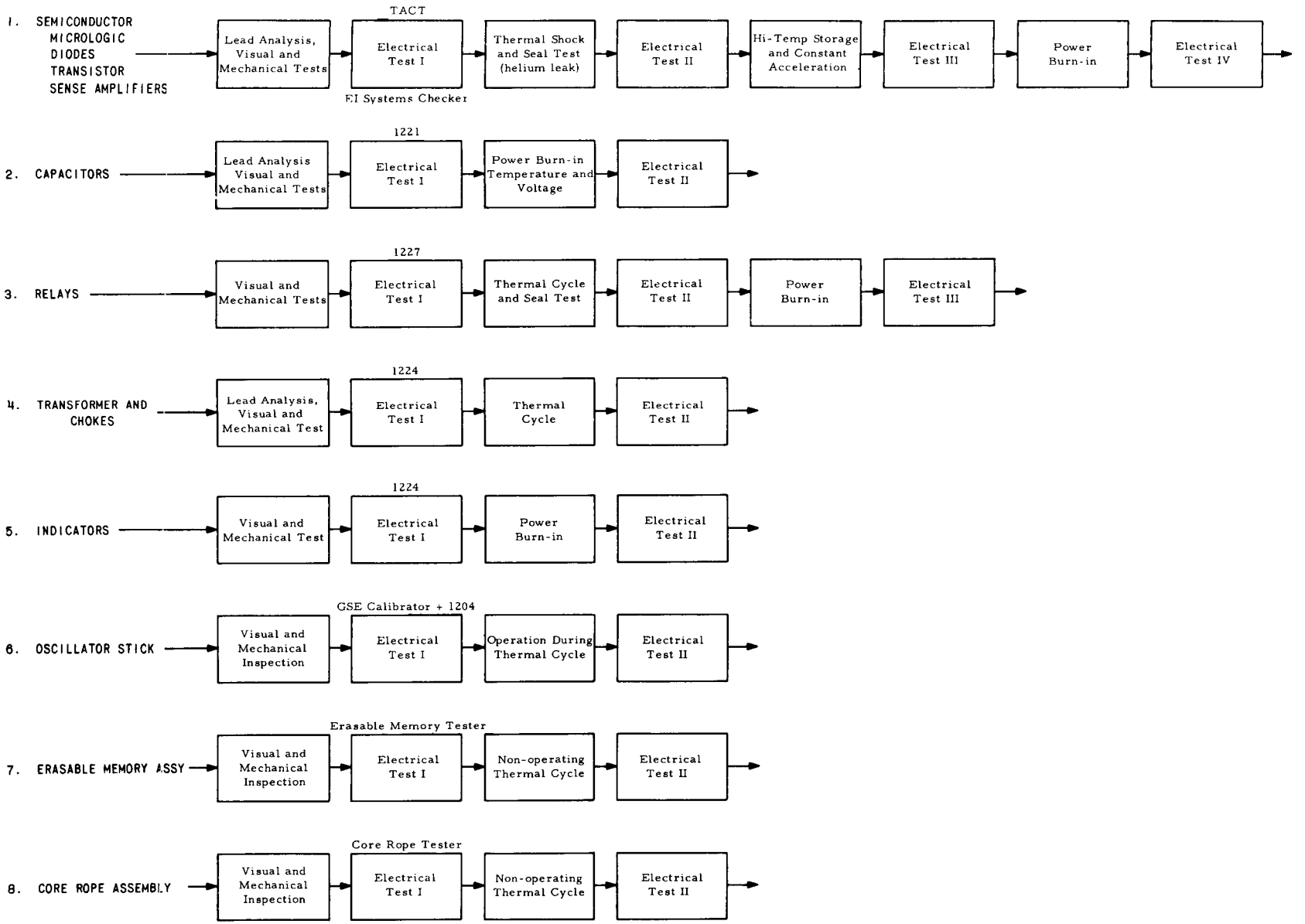

Figure 4-2. AGC Factory Test Plan (Sheet 1 of 2)

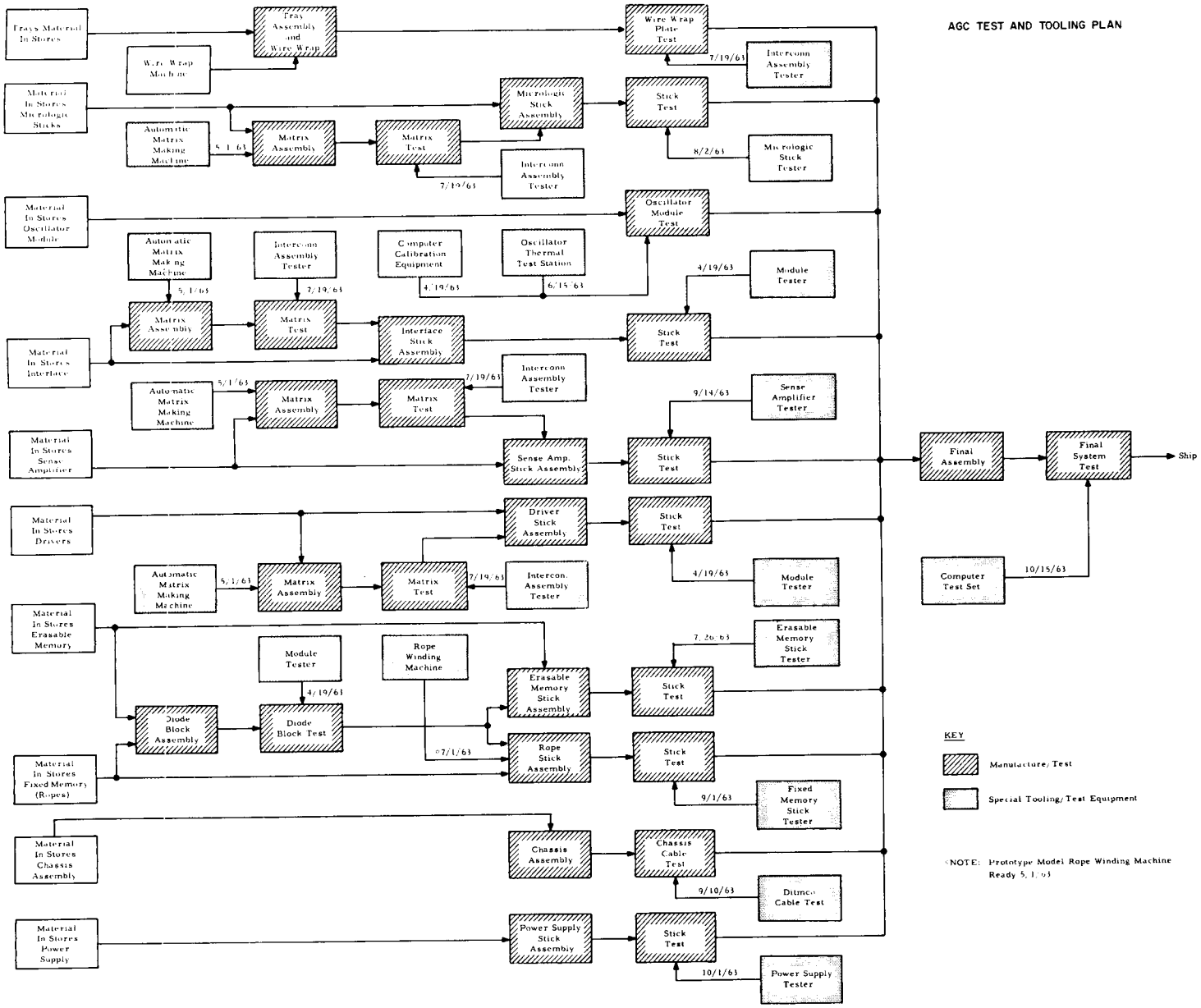

Figure 4-2. AGC Factory Test Plan (Sheet 2 of 2)

development of AGC programs from subsystem and system test routines to actual in-flight mission programs. The Core Rope Simulator (CRS) will provide a means of performing a final checkout of programs before implementation as core ropes.

The CRS will be basically a 4096 word erasable memory which will be substituted for and simulate one of the three core ropes contained in the Apollo Guidance Computer. The selection of the core for removal will be a function of the over-all program space allotment and the particular test to be performed.

The CRS will be contained in a six foot high by nineteen-inch wide rack-type enclosure. It will consist of an operator's keyboard, a tape reader and spooler, five module drawers (one of which will contain an erasable core stack), power input and control panels, and associated DC power supplies. The keyboard is illustrated on figure 4-3.

Provisions will be included to permit loading the core stack within the simulator either manually by keyboard, or automatically by paper tape.

During manual operation address selection is accomplished by means of twelve address keys on the keyboard. The word to be written into a particular address is selected by means of fifteen data keys. Indicator lamps adjacent to the keys, indicate the word and address being loaded into the memory.

During tape loading the data keys will be inoperative and the address may be selected by either keys or tape. Loading the memory by tape can be accomplished at a rate of 100 bits per second. Provisions will also be included to allow writing into the memory from tape one word at a time. The content of any address may be read out as indications on the lamps adjacent to the keys and rewritten into the memory. Parity checks will also be available.

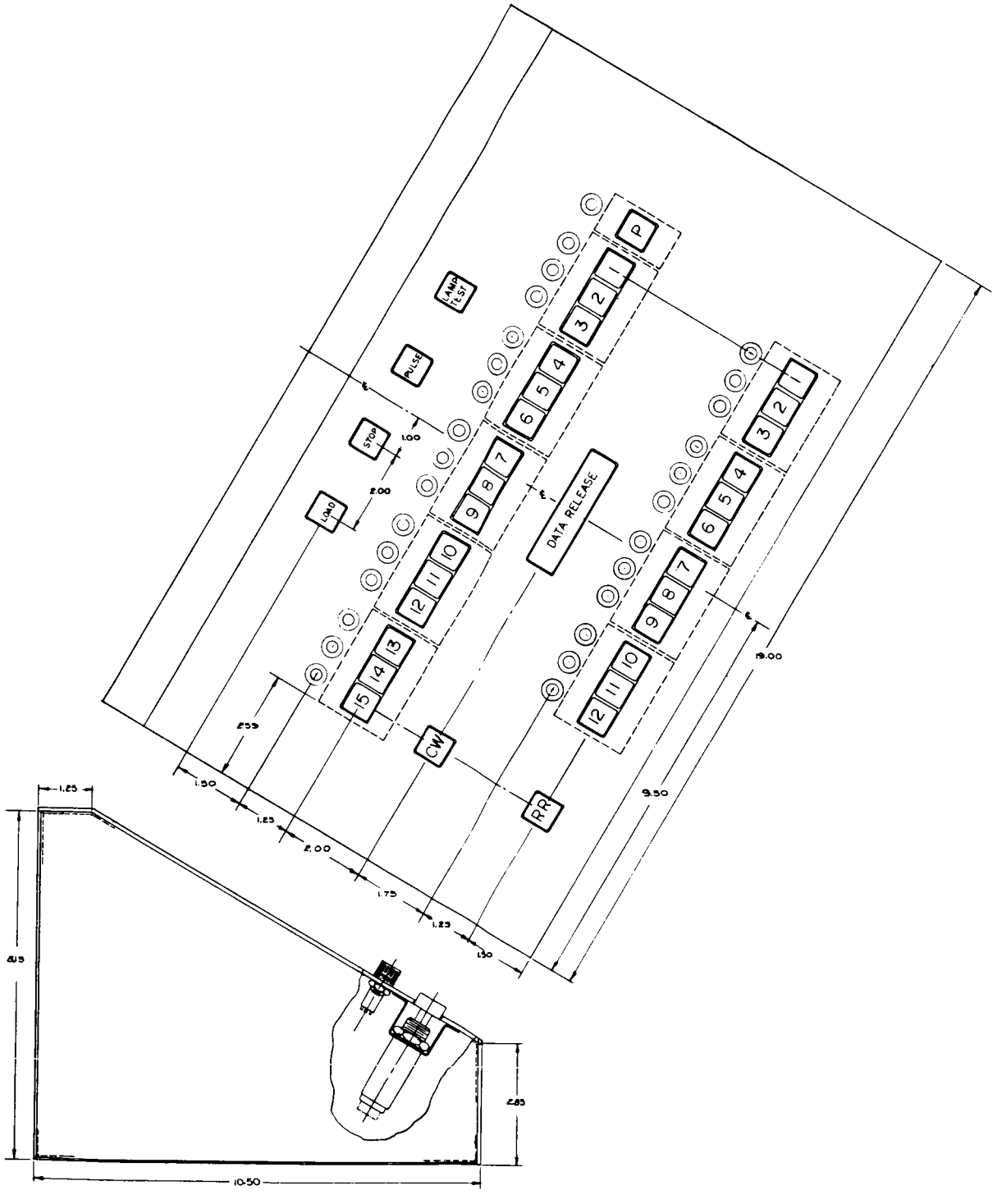

Figure 4-3. Core Rope Simulator Keyboard

4.3 CONTROL PANEL TEST STATION

The Control Panel Test Station will consist of a holding and test fixture, test probe, terminal board, and one unit of test equipment. The test station will be capable of measuring wiring resistance between components and connector pins.

4.4 COMPUTER SIMULATOR TEST STATION

The Apollo Computer Simulator Test Station will be an upright console for rack mounted equipment. It will contain an oscilloscope with a four input preamplifier, a frequency counter, and a test selector and power control panel. The test station will be capable of measuring phase relationship, pulse width, rise time, fall time, droop, amplitude, frequency, period, time interval, and frequency ratios, all of which are required for testing the Computer Simulator. The test selector and power control panel will contain switching functions identical with those of the Computer Simulator with the exception of the local/remote switch. No computer simulator displays will be duplicated on the test station. A bank of five rotary switches will be utilized to switch computer simulator outputs to the oscilloscope. In addition, three rotary switches will be utilized to control the frequency counter inputs. A DC voltmeter will be provided with test probes. Dummy loads will be included on the control panel to simulate 1 mv equipment inputs. Power control for the test station will be provided by a switch on the station power panel and a circuit breaker on the AC power input panel.

4.5 PULSE TRANSFORMER TEST STATION

The Pulse Transformer Test Station is capable of testing pulse transformers for inductance, leakage inductance, coupling capacitance, input capacitance, polarity, resistance, insulation breakdown, pulse duration, rise time, and

peak to peak voltages. The test station contains a "Q" meter, inductance and capacitance meter, oscilloscope, resistance bridge, insulation breakdown tester, pulse generator and a pulse transformer test fixture.

4.6 POWER SUPPLY TEST STATION

The Power Supply Test Station will consist of five units of test equipment, a mercury wetted contact relay, and four variable resistors. The test station will be capable of performing static and dynamic line and load regulation tests. In addition, the test station will check power supplies for overload, insulation, and ripple.

4.7 RELAY TEST STATION

The Relay Test Station will consist of five units of test equipment and two test fixtures. The test station will be capable of measuring pull-in and drop-out voltages, and contact and coil resistances of non-latching relays. In addition it will be capable of measuring the amplitude, polarity, and width of pulse generator outputs, and assure the absence of false pulses when testing one-shot relays.

4.8 RESISTOR TEST STATION

The Resistor Test Station will be capable of testing resistors for body dimensions, diameter of leads, cracks, chips, lead pull and bends, and ohmic value. The test station will contain a resistance bridge, weight and pull devices, a micrometer, and go/no-go gauges.

4.9 AGC MICROLOGIC STICK TESTER

An AGC Micrologic Stick Tester has been proposed which will be capable of

testing twenty-three micrologic stick types, one test cycle being completed within 15 minutes. The stick tester will be capable of by-passing an existing error during a test cycle, locating an error automatically, and diagnosing an error to the smallest possible micrologic element. In addition, the tester will adjust for stick design changes automatically, and perform tests which will incorporate voltage level discrimination and AC measurements.

SECTION V
RELIABILITY AND QUALITY ASSURANCE

SECTION V
RELIABILITY AND QUALITY ASSURANCE

5.1 INTRODUCTION

Raytheon has conducted an extensive evaluation program on the Fairchild micrologic NOR gate. In an attempt to obtain statistically sound information concerning the distribution of parameters, many electrical tests were performed on large samples of the device; two such tests are included in this report. Modifications were made to Raytheon's Automatic Systems Checker, located in the Environmental Test Facility at the Sudbury complex, to accomplish this task. Data from these tests was processed on a computer and certain meaningful parameters were plotted as composite frequency histograms.

5.2 MICROLOGIC EVALUATION

The first series of tests were performed on 1600 NOR gates (TO-47 case size) that were purchased to ND 1006771, Revision C, for use in the breadboard computers at Raytheon and MIT/IL. These devices were broken down into two groups; group A contained 600 NORs and group B contained 1000 NORs. Test conditions for groups A and B are listed in Tables 5-1 and 5-2, respectively. The "cull" limits for group A were established to select marginal units for evaluation by circuit designers. The cull and reject limits for group B were identical. Composite frequency histograms of certain meaningful parameters for group A are shown on figures 5-1 through 5-5; those for group B are shown on figures 5-6 through 5-10. An evaluation of these histograms show a normal distribution, that is centered on the specification limits.

The second series of tests were performed on 2000 NOR gates (TO-5 case size) that were purchased to ND 1006985, Revision A, for use in breadboard GSE and Factory Test Equipment. These devices were broken down into two

groups, A and B, each group containing 1000 NORs. Test conditions for groups A and B, listed in Tables 5-3 and 5-4, respectively, differ only in the load resistor used in the "current available" test and the limits associated with that test. Composite frequency histograms of certain meaningful parameters for group A are shown in figures 5-11 through 5-14; those for group B are shown in figures 5-15 through 5-18. The majority of these histograms show normal distributions that are centered on the specification limits, with few exceptions. It is interesting to note in figures 5-12, 5-13, 5-16, and 5-17 that the center portions of the distributions are noticeably reduced. This indicates that the vendor had probably selected units for another customer from the test groups. The truncated distribution shown in figure 5-14 may be the result of the diffusion process.

In the majority of the cases, the number of units in a test and the number reported were unequal. This is a result of the wrong lead configuration on the unit, the wrong leads clipped from the header, micrologic flip-flops received from the vendor instead of NOR gates, and spoiled data. The automatic tape punch introduced errors into the data handling system. These errors were detected and removed; but the data was not used in the statistical analysis.

Raytheon has also performed a series of special evaluation tests on the micrologic NOR gate to establish performance characteristics of the device as well as to provide an aid in determining its quality and reliability. Both the original configuration and the new mask of the NOR gate were used in the evaluation. The following tests were performed:

a. "S" Curve - The Automatic System Checker was used to plot base voltage versus collector voltage of a properly loaded NOR gate. A sample of 200 units were tested to establish margins for turn-on and output voltages for the Specification Control Drawing.

b. Temperature - A sample of 200 units were tested at 0°C, room temperature, and +70°C. Results of these tests indicated that adequate design margins exist at both extremes of the temperature range.

c. Radiographic Examination - During initial stages of testing NOR gates, an intermittent short was discovered in an input circuit. X-Ray examination revealed a large conducting particle which was found to be an extra solder preform used to attach the silicon chip to the header. Three-hundred units were then subjected to x-ray examination and no further defects were found. It was recommended that if this situation occurs again, 100 percent examination should be performed in the screening and burn-in program.

d. Case Leakage - Ten samples of TO-47 case size NOR gates were submitted to helium leak checks. Six had leak rates greater than 1×10^{-6} cc/atm/min. The specification presently establishes 1×10^{-8} cc/atm/min as the maximum limit.

e. Humidity Life Test - It has been demonstrated that a large number of NOR gates in the possession of Raytheon and MIT/IL had defective cases. This, however, is probably not a serious problem since the chip is surface-passivated with silicon dioxide which protects the critical junction interfaces. High-humidity life tests have been performed on 60 units from known defective lots to determine if it was a sound engineering decision to use these units in non-critical hardware. The life tests consisted of two phases: a 500-hour run at a Vcc of 3 volts, and a 500-hour run at a Vcc of 6 volts. Resulting data is being examined for degradation failures.

f. High Temperature Storage - During specification negotiations with Fairchild, it became apparent that there was a basic difference between integrated circuits and planar-passivated silicon

transistors in their ability to withstand high temperature storage. The standard 300°C high temperature storage test for transistors "will guarantee the development of purple plague in micrologic". Twenty-five of the original micrologic configuration and twenty-five of the new mask units were submitted to a step-stress test. Fairchild recommended that these micrologic units should not be subjected to temperatures greater than 150°C. Raytheon's testing began at 200°C storage for 72 hours, followed by 72 hours storage at 250°C and at 300°C respectively. Electrical tests were performed before and after each step. Following the 300°C bake, the units were subjected to 20,000 g's constant acceleration in the y direction. No catastrophic failures or degradation was noted after testing.

g. Emitter Lead Pull Test - During testing it was noted that the emitter lead on two units had separated from the case. The emitter lead is brazed or welded directly to the case and is different from the other five leads. All leads pass through the header and are insulated from the case by glass eyelets. Emitter leads on five units were pulled to the breaking point. Average break strength was 20 pounds and the dispersion was good. Pull tests will be performed in the screening and burn-in program.

TABLE 5-1

TEST CONDITIONS, GROUP A, TEST 1

TEST NO.	PARAMETER	INPUTS						CULLING LIMITS		SPEC LIMITS	
		1	3	4	5	7	8	MIN	MAX	MIN	MAX
1	BASE CURRENT IB1	.79	.79	GND	.79	—	3V	250μA	550μA	—	680μA
2	BASE CURRENT IB2	.79	.79	GND	.79	—	3V	250μA	550μA	—	680μA
3	BASE CURRENT IB3	.79	.79	GND	.79	—	3V	250μA	550μA	—	680μA
4	OUTPUT VOLTAGE VCE1	.79	—	GND	—	—	3V	200mv	350mv	—	400mv
5	OUTPUT VOLTAGE VCE2	—	.79	GND	—	—	3V	200mv	350mv	—	400mv
6	OUTPUT VOLTAGE VCE3	—	—	GND	.79	—	3V	200mv	350mv	—	400mv
7	SATURATION VOLTAGE VCES1	1.2	—	GND	—	—	3V	200mv	300mv	—	350mv
8	SATURATION VOLTAGE VCES2	—	1.2	GND	—	—	3V	200mv	300mv	—	350mv
9	SATURATION VOLTAGE VCES3	—	—	GND	1.2	—	3V	200mv	300mv	—	350mv
10	CURRENT AVAILABLE	.54	.54	GND	.54	230 Ω	3V	800mv	950mv	3.4MA	—
11	ICEO	—	—	GND	—	5.0	—	—	100μA	—	100μA
12	IEBO	GND	GND	6.5	GND	—	—	—	1.0MA	—	1.0MA
13	ICBO	GND	GND	—	GND	8.0	—	—	1.0MA	—	1.0MA
14	BVCEO	—	—	GND	—	100μA	—	7.0V	40V	—	—
15	BVEBO	GND	GND	100μA	GND	—	—	5.0V	20V	—	—
16	BVCBO	GND	GND	—	GND	100μA	—	7.0V	40V	—	—

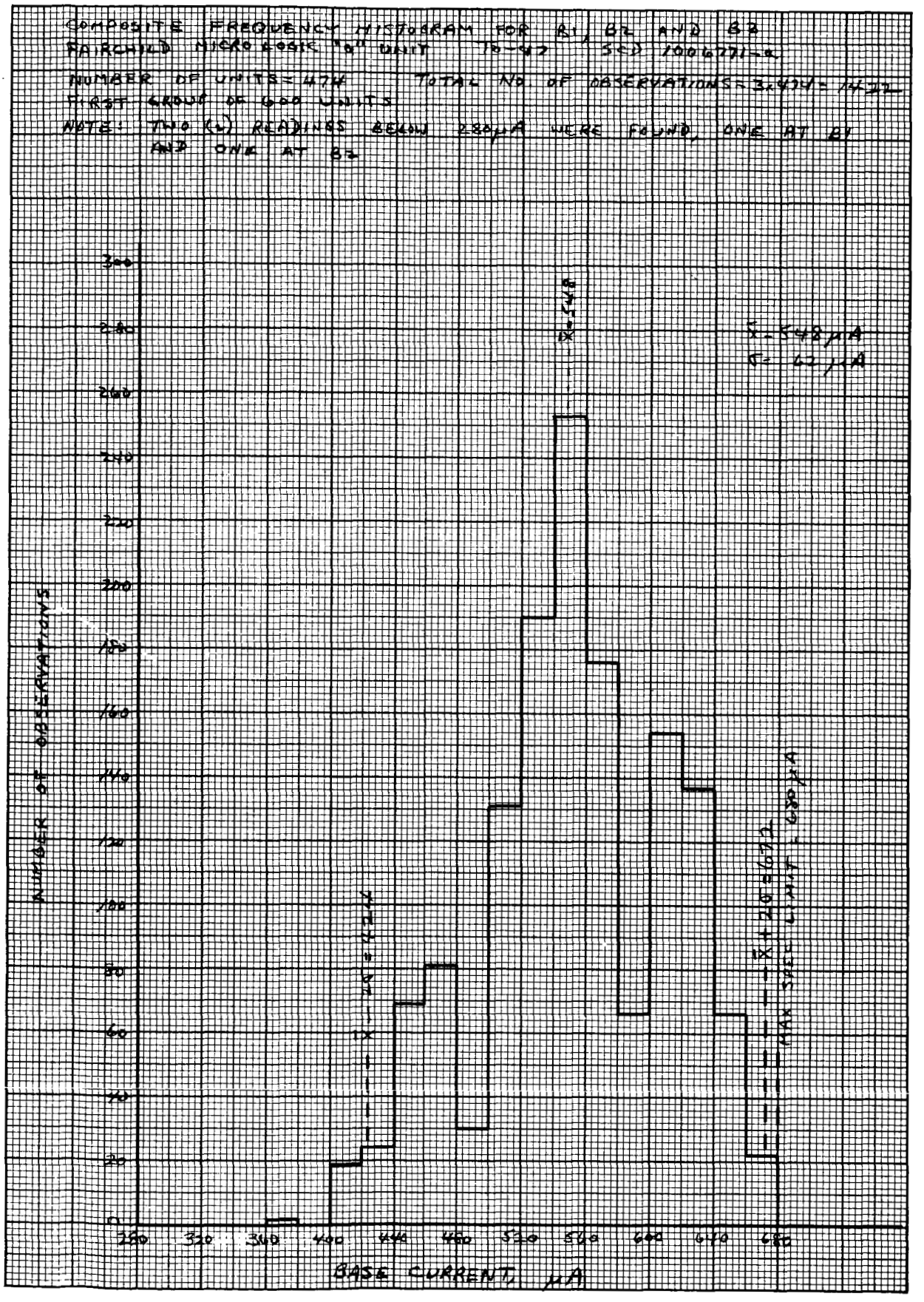

Figure 5-1. Base Current Data, Group A, Test 1

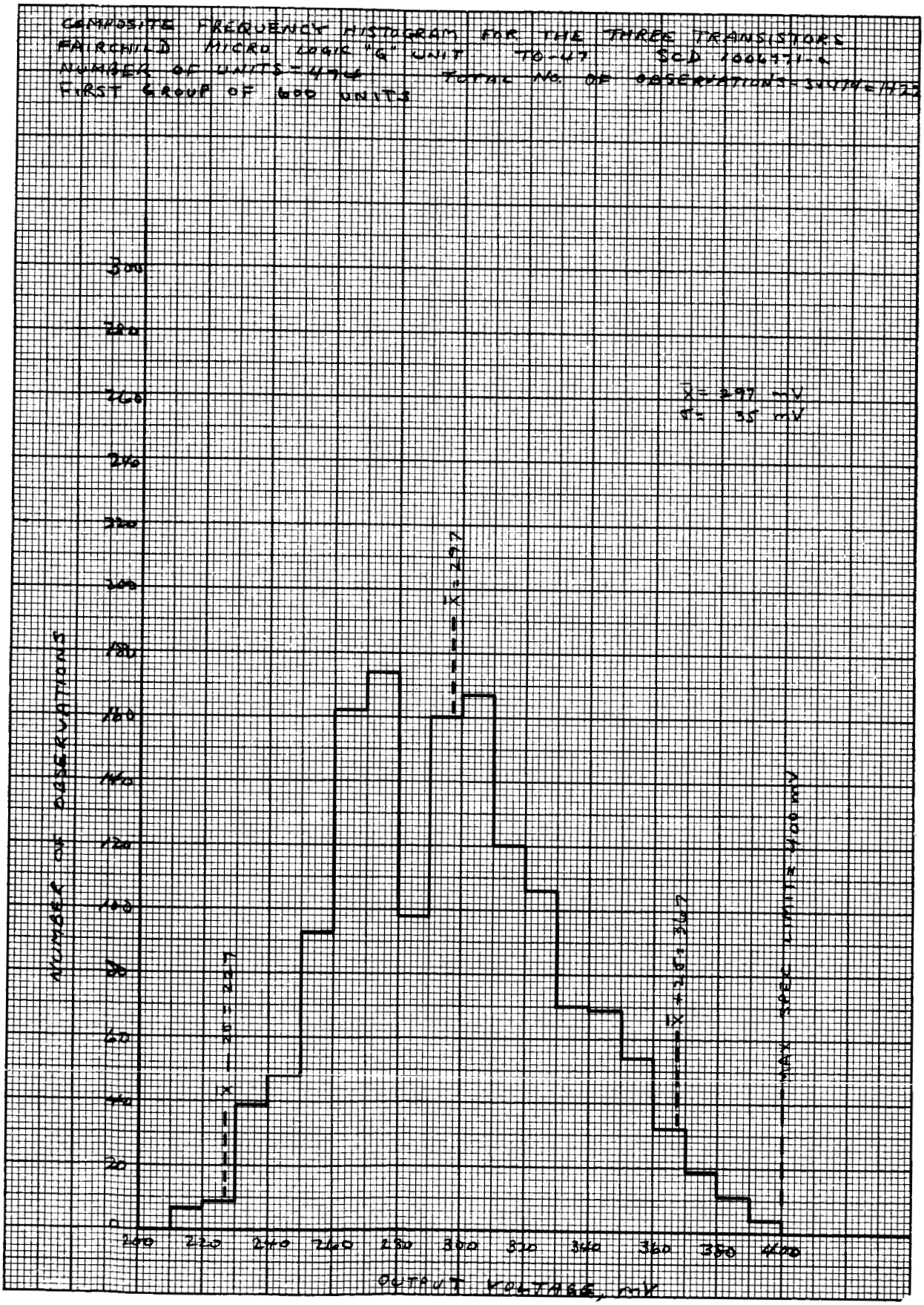

Figure 5-2. Output Voltage Data, Group A, Test 1

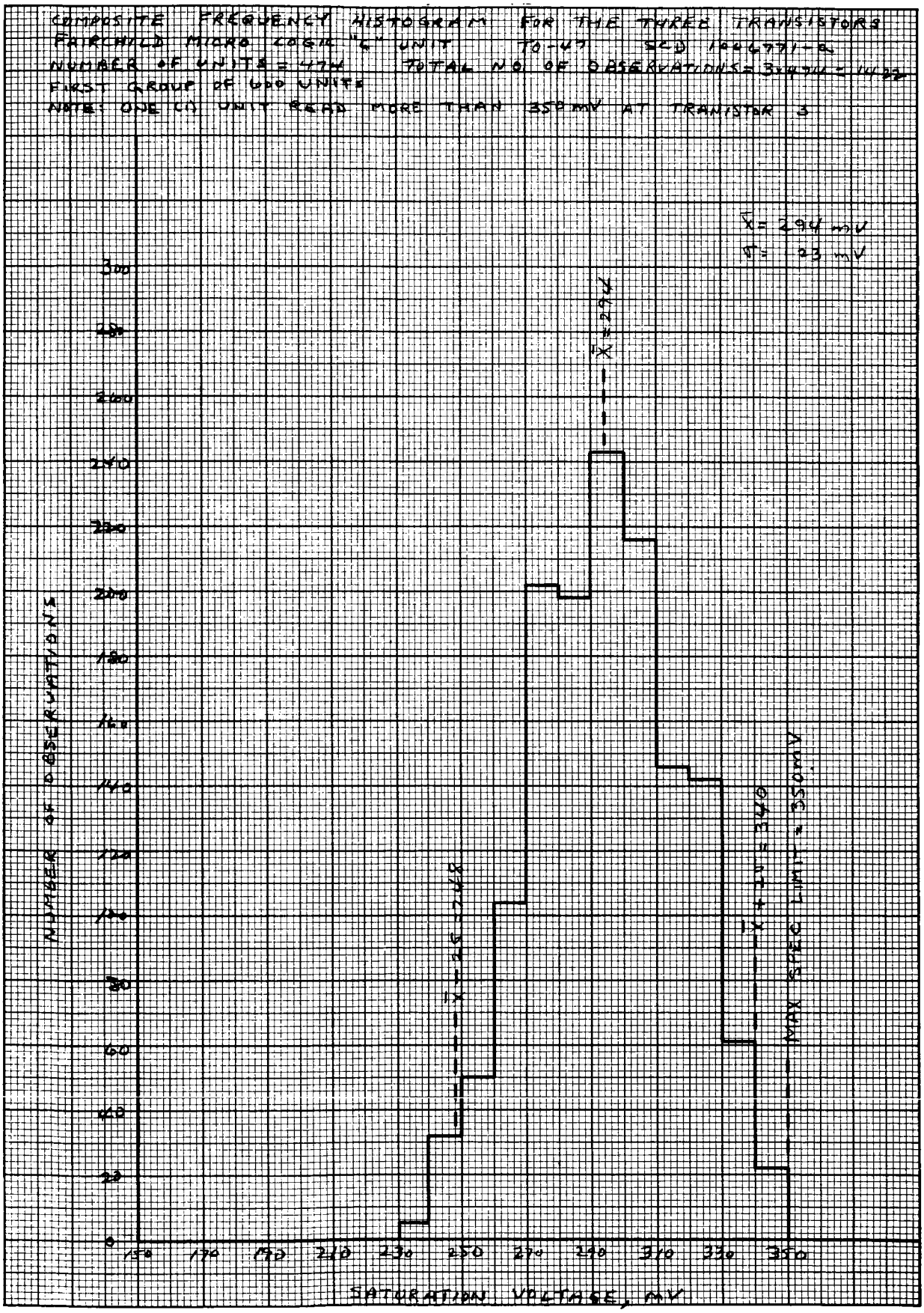

Figure 5-3. Saturation Voltage, Group A, Test 1

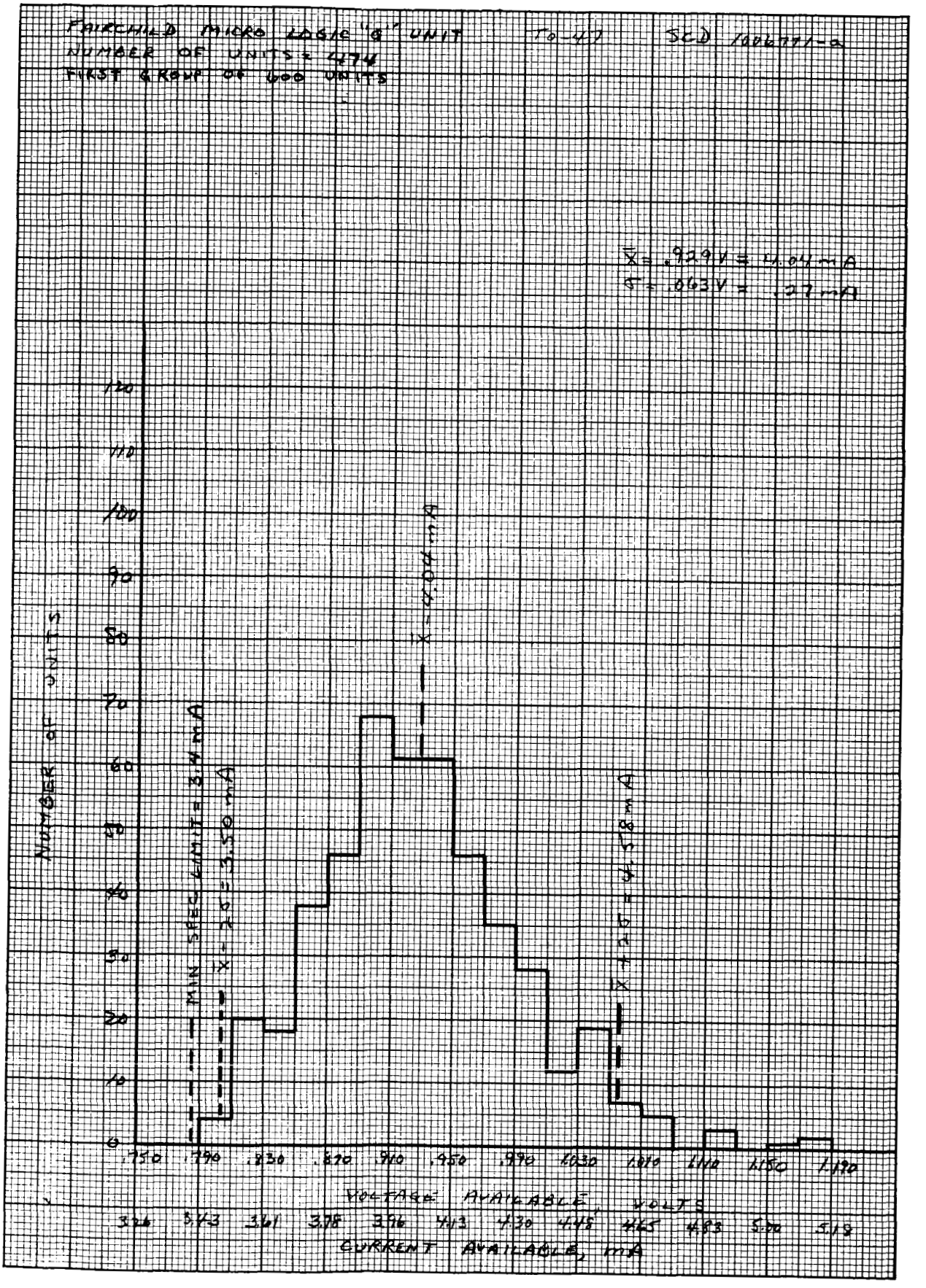

Figure 5-4. Current Available, Group A, Test 1

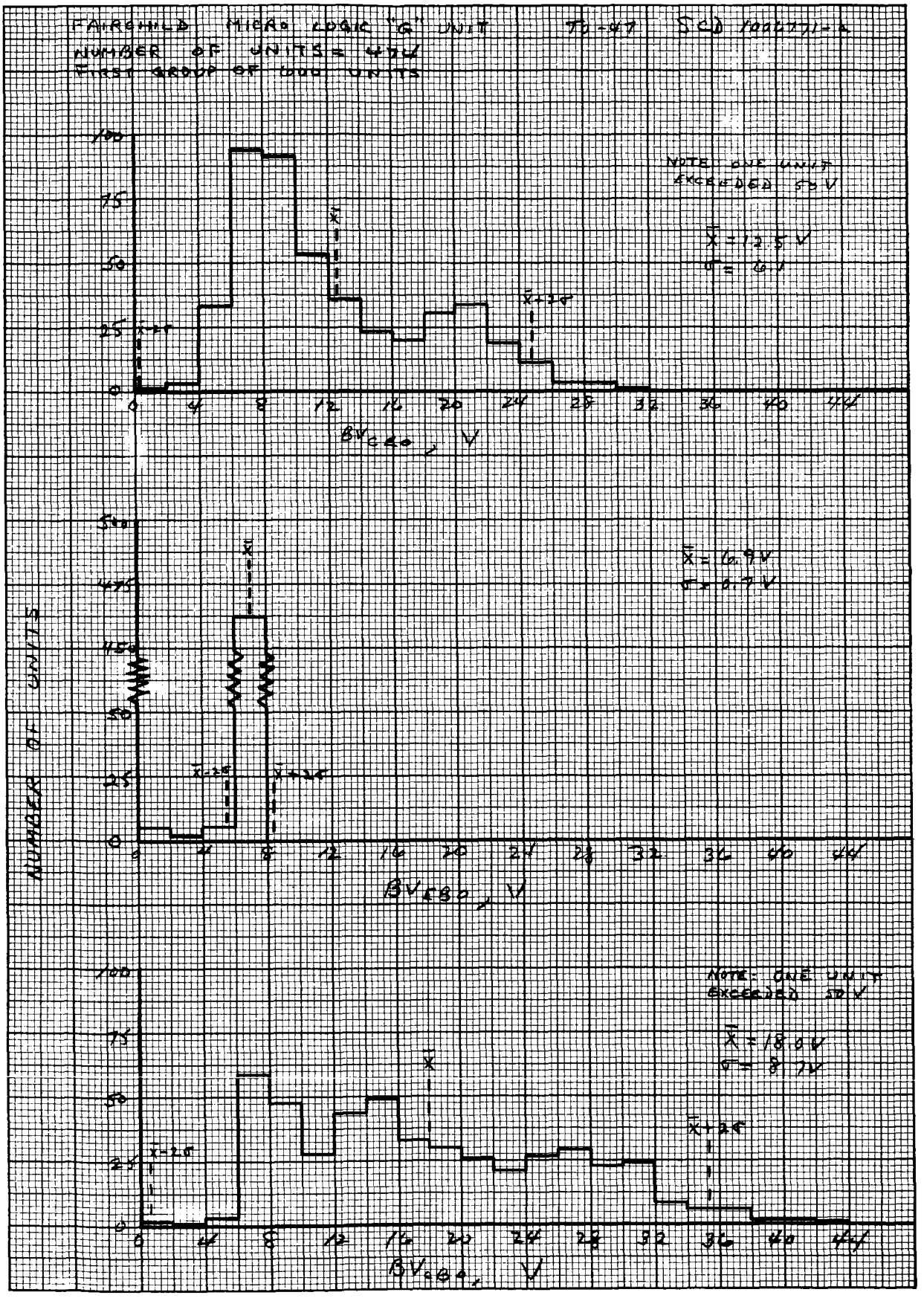

Figure 5-5. Breakdown Voltages, Group A, Test 1

TABLE 5-2
TEST CONDITIONS, GROUP B, TEST 1

TEST NO.	PARAMETER	INPUTS						CULLING LIMITS		SPEC LIMITS	
		1	3	4	5	7	8	MIN	MAX	MIN	MAX
1	BASE CURRENT IB1	.79	.79	GND	.79	—	3V	420μA	680μA	—	680μA
2	BASE CURRENT IB2	.79	.79	GND	.79	—	3V	420μA	680μA	—	680μA
3	BASE CURRENT IB3	.79	.79	GND	.79	—	3V	420μA	680μA	—	680μA
4	OUTPUT VOLTAGE VCE1	.79	—	GND	—	—	3V	200mv	370mv	—	400mv
5	OUTPUT VOLTAGE VCE2	—	.79	GND	—	—	3V	200mv	370mv	—	400mv
6	OUTPUT VOLTAGE VCE3	—	—	GND	.79	—	3V	200mv	370mv	—	400mv
7	SATURATION VOLTAGE VCES1	1.2	—	GND	—	—	3V	200mv	340mv	—	350mv
8	SATURATION VOLTAGE VCES2	—	1.2	GND	—	—	3V	200mv	340mv	—	350mv
9	SATURATION VOLTAGE VCES3	—	—	GND	1.2	—	3V	200mv	340mv	—	350mv
10	CURRENT AVAILABLE	.54	.54	GND	.54	230Ω	3V	800mv	—	3.4MA	—
11	ICEO	—	—	GND	—	5.0	—	—	100μA	—	100μA
12	IEBO	GND	GND	6.5	GND	—	—	—	1.0MA	—	1.0MA
13	ICBO	GND	GND	—	GND	8.0	—	—	1.0MA	—	1.0MA
14	BVCEO	—	—	GND	—	100μA	—	5.0V	40V	—	—
15	BVEBO	GND	GND	100μA	GND	—	—	5.0V	20V	—	—
16	BVCBO	GND	GND	—	GND	100μA	—	5.0V	40V	—	—

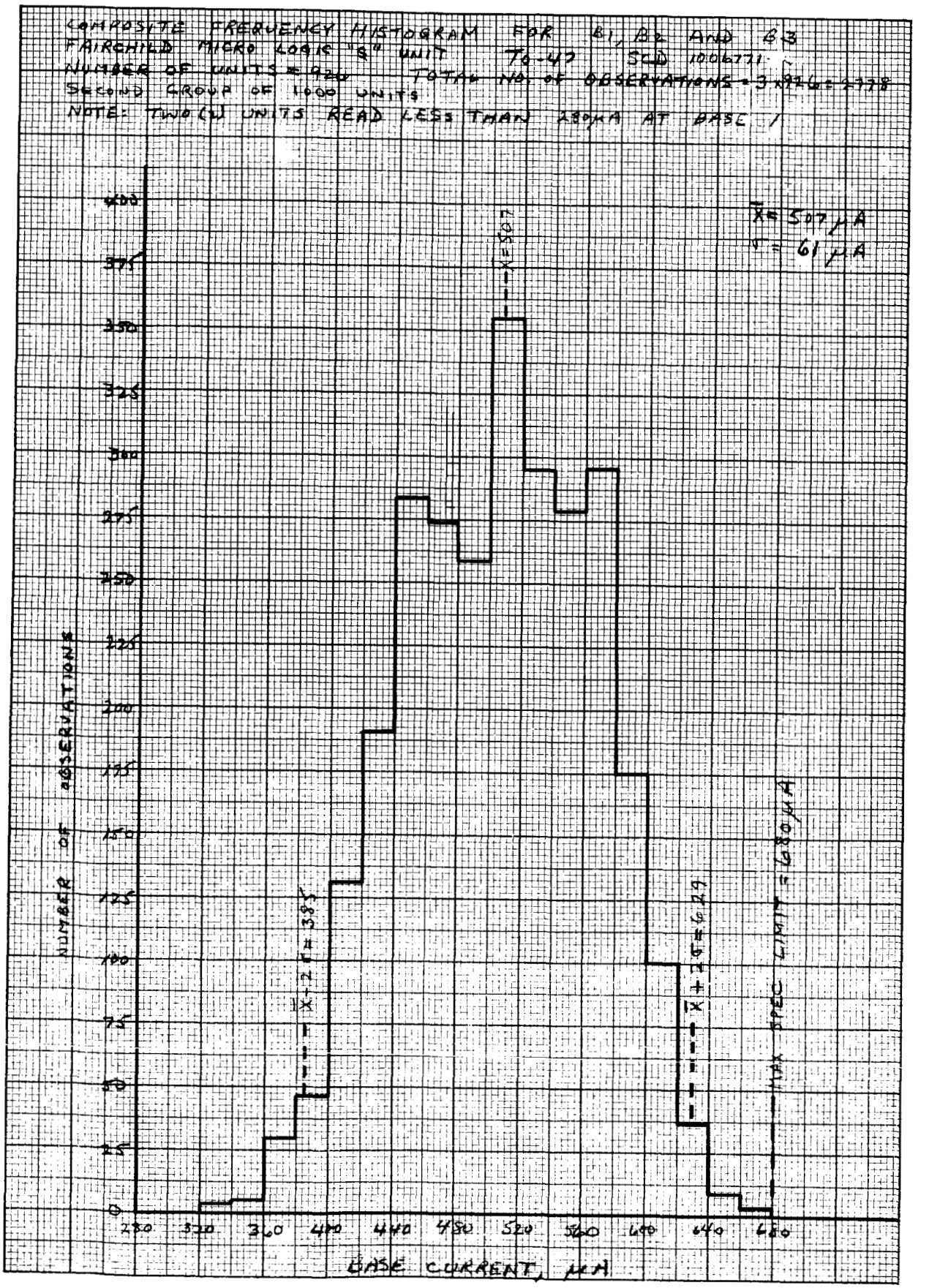

Figure 5-6. Base Current Data, Group B, Test 1

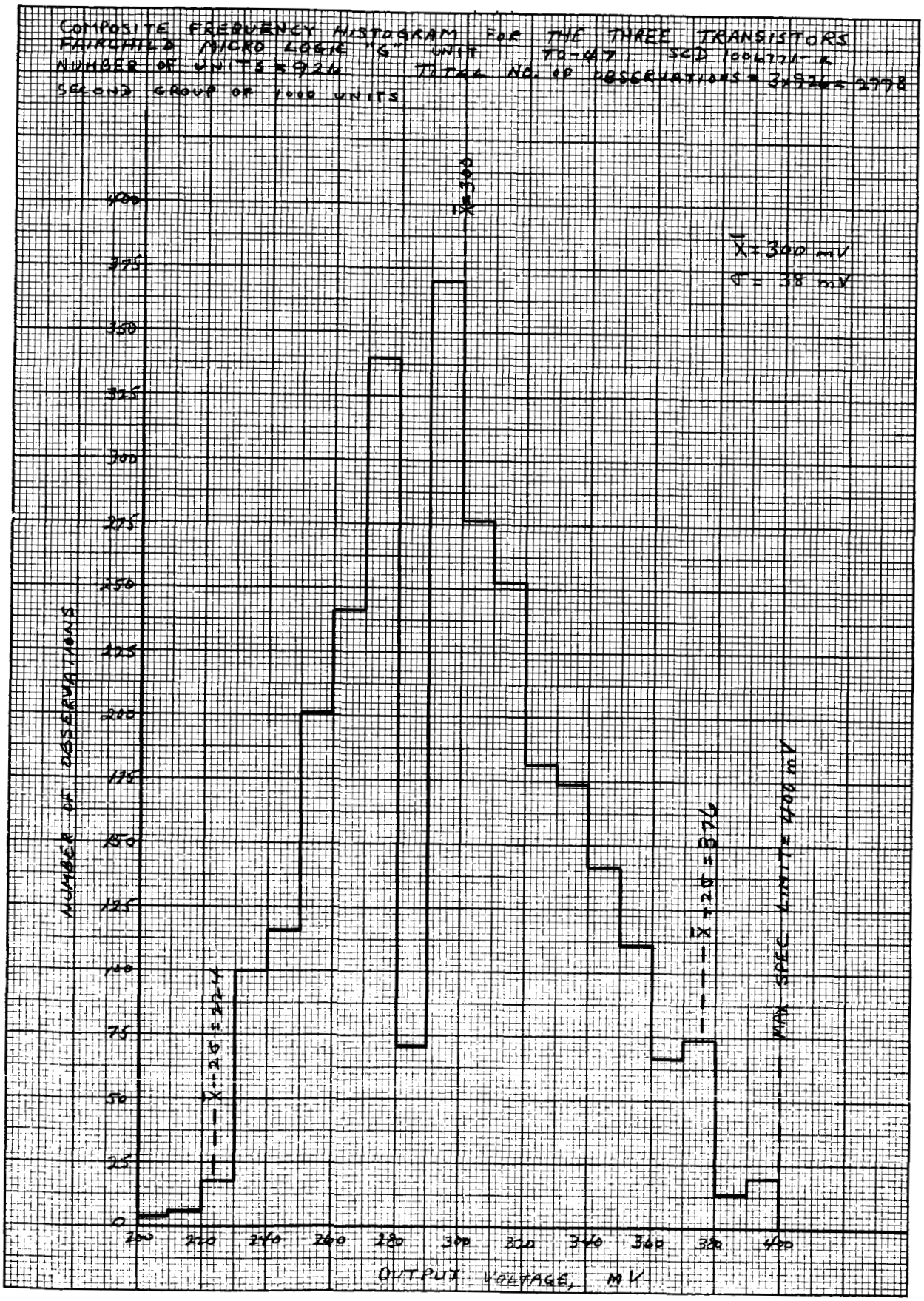

Figure 5-7. Output Voltage Data, Group B, Test 1

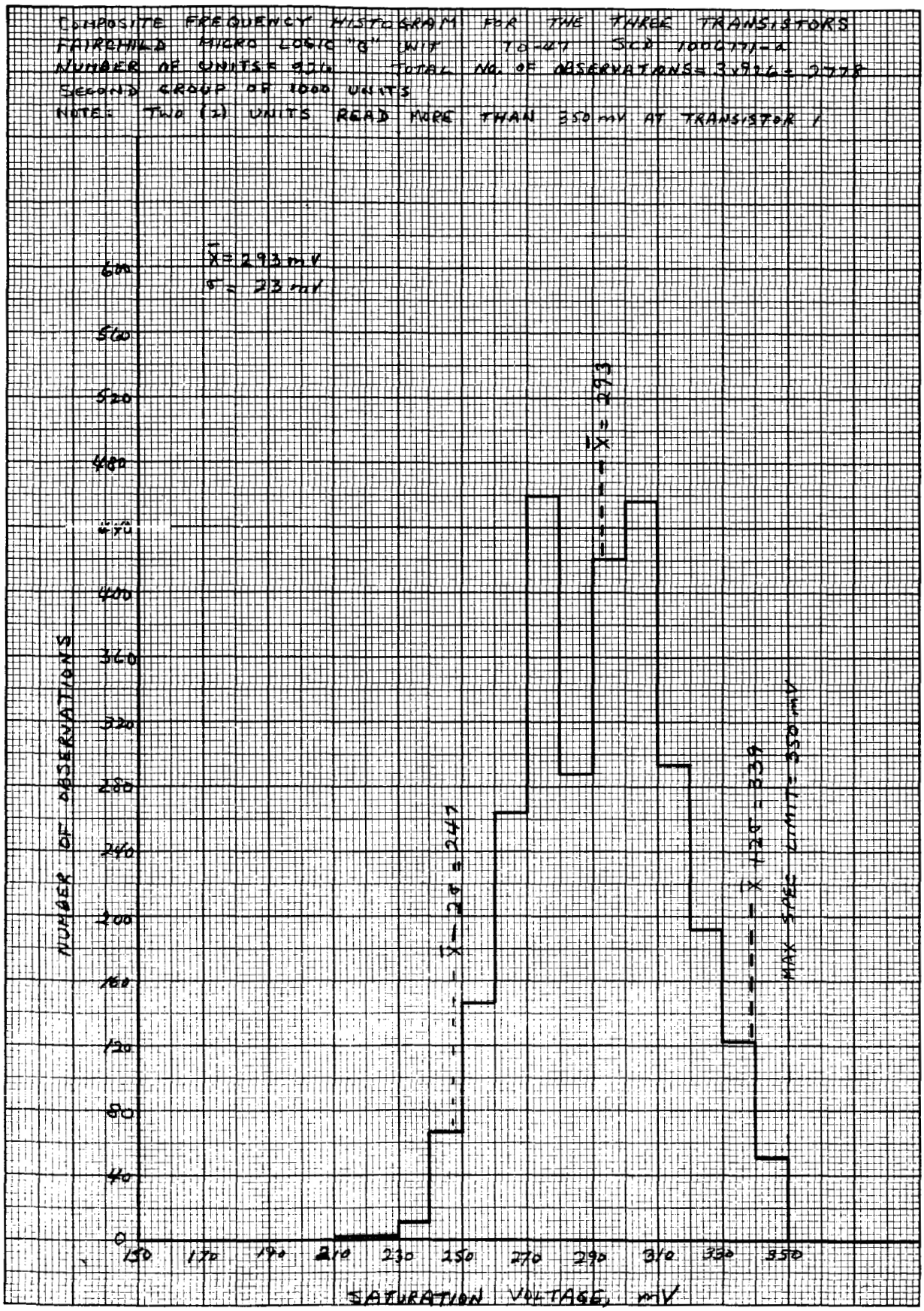

Figure 5-8. Saturation Voltage, Group B, Test 1

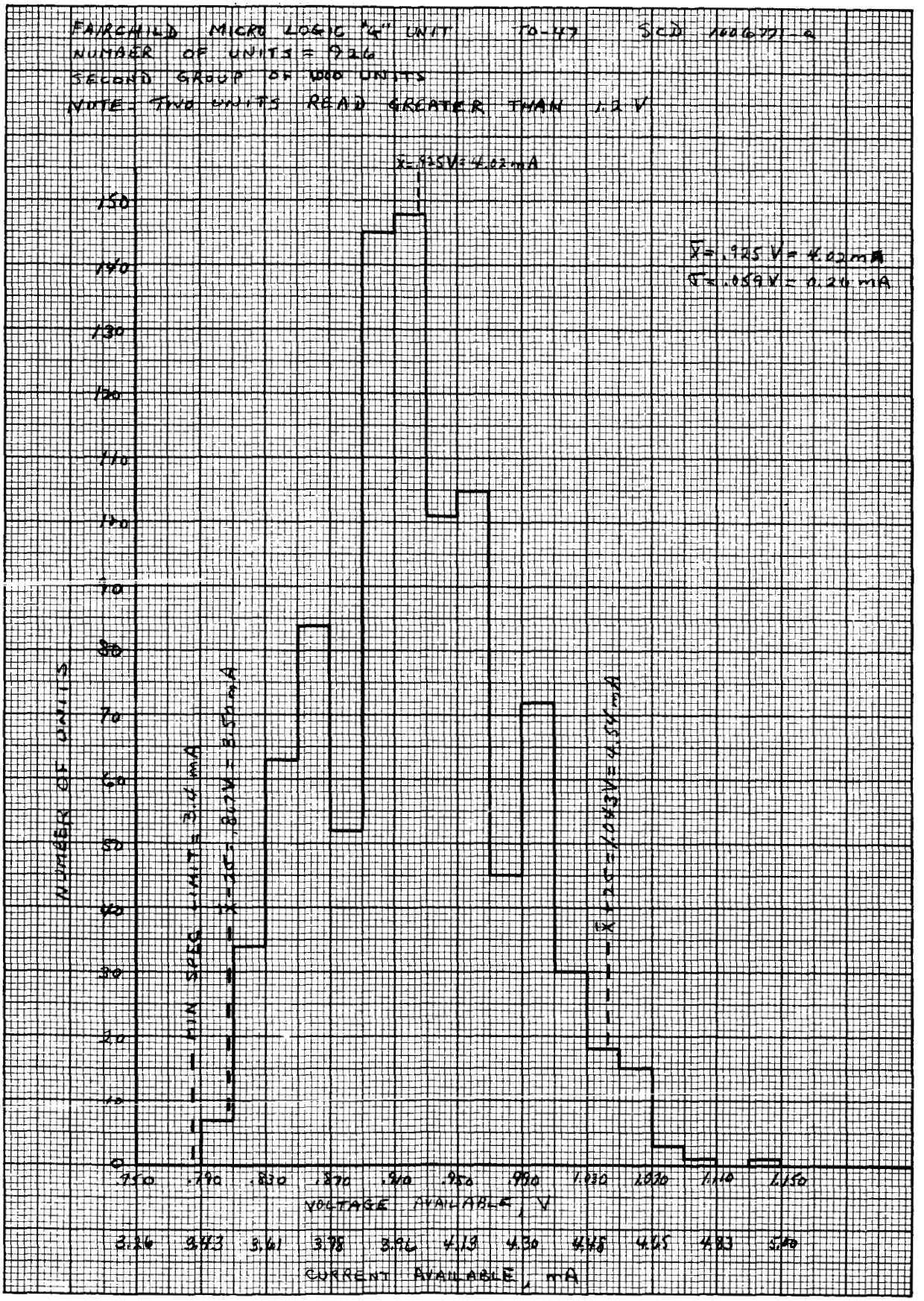

Figure 5-9. Current Available, Group B, Test 1

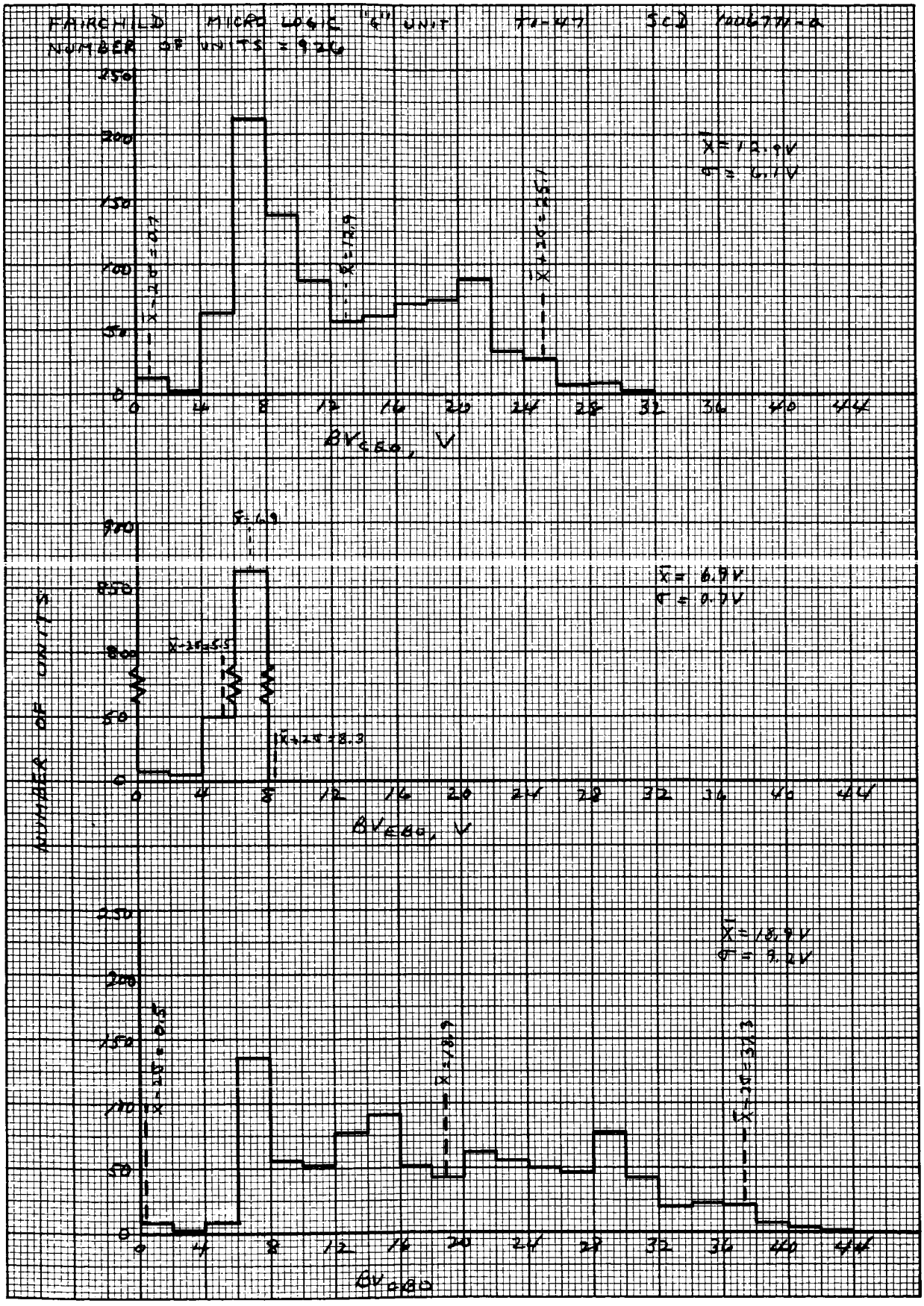

Figure 5-10. Breakdown Voltages, Group B, Test 1

TABLE 5-3
TEST CONDITIONS, GROUP A, TEST 2

TEST NO.	PARAMETER	INPUTS						CULLING LIMITS		SPEC LIMITS	
		1	3	4	5	6	8	MIN	MAX	MIN	MAX
1	BASE CURRENT IB1	.79	.79	GND	.79	—	3V	250μA	800μA	—	—
2	BASE CURRENT IB2	.79	.79	GND	.79	—	3V	250μA	800μA	—	680μA
3	BASE CURRENT IB3	.79	.79	GND	.79	—	3V	250μA	800μA	—	680μA
4	OUTPUT VOLTAGE VCE1	.79	—	GND	—	—	3V	200mv	400mv	—	400mv
5	OUTPUT VOLTAGE VCE2	—	.79	GND	—	—	3V	200mv	400mv	—	400mv
6	OUTPUT VOLTAGE VCE3	—	—	GND	.79	—	3V	200mv	400mv	—	400mv
7	SATURATION VOLTAGE VCES1	1.2	—	GND	—	—	3V	200mv	350mv	—	350mv
8	SATURATION VOLTAGE VCES2	—	1.2	GND	—	—	3V	200mv	350mv	—	350mv
9	SATURATION VOLTAGE VCES3	—	—	GND	1.2	—	3V	200mv	350mv	—	350mv
10	CURRENT AVAILABLE	.54	.54	GND	.54	245Ω	3V	785mv	—	3.2MA	—
11	ICEO	—	—	GND	—	—	—	—	1.0MA	—	100μA
12	IEBO	GND	GND	6.5	GND	—	—	—	1.0MA	—	1.0MA
13	ICBO	GND	GND	—	GND	—	—	—	1.0MA	—	1.0MA

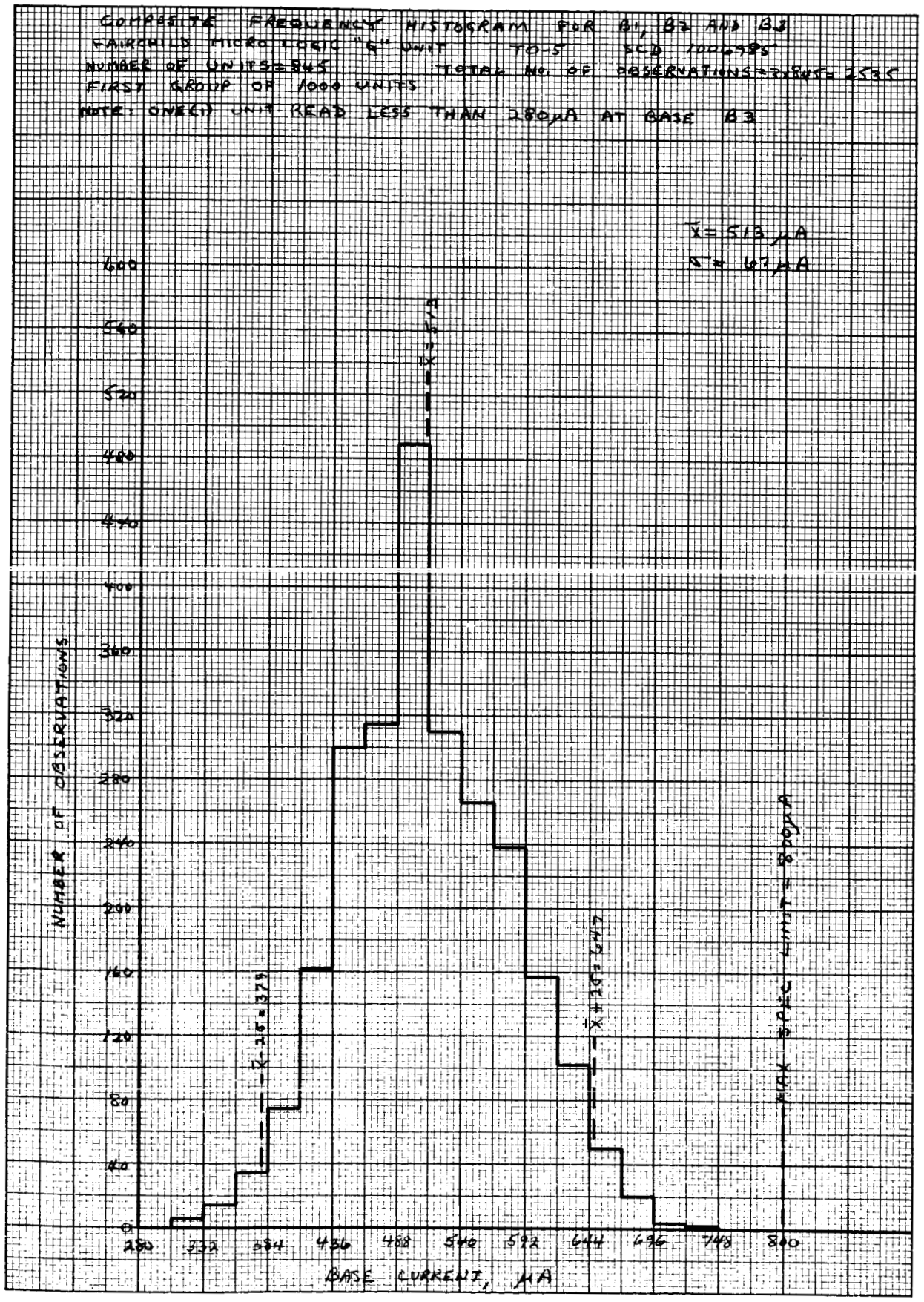

Figure 5-11. Base Current Data, Group A, Test 2

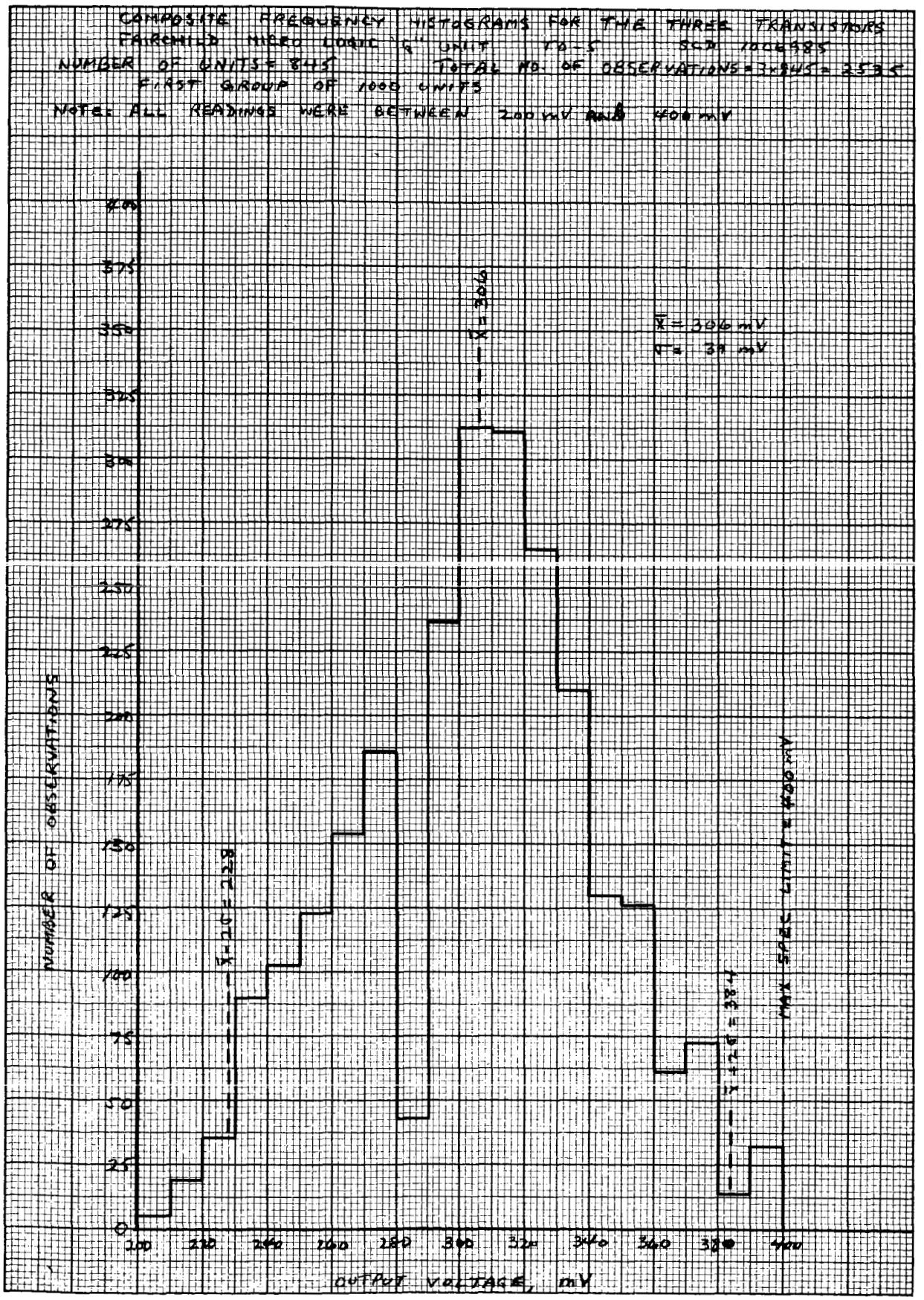

Figure 5-12. Output Voltage Data, Group A, Test 2

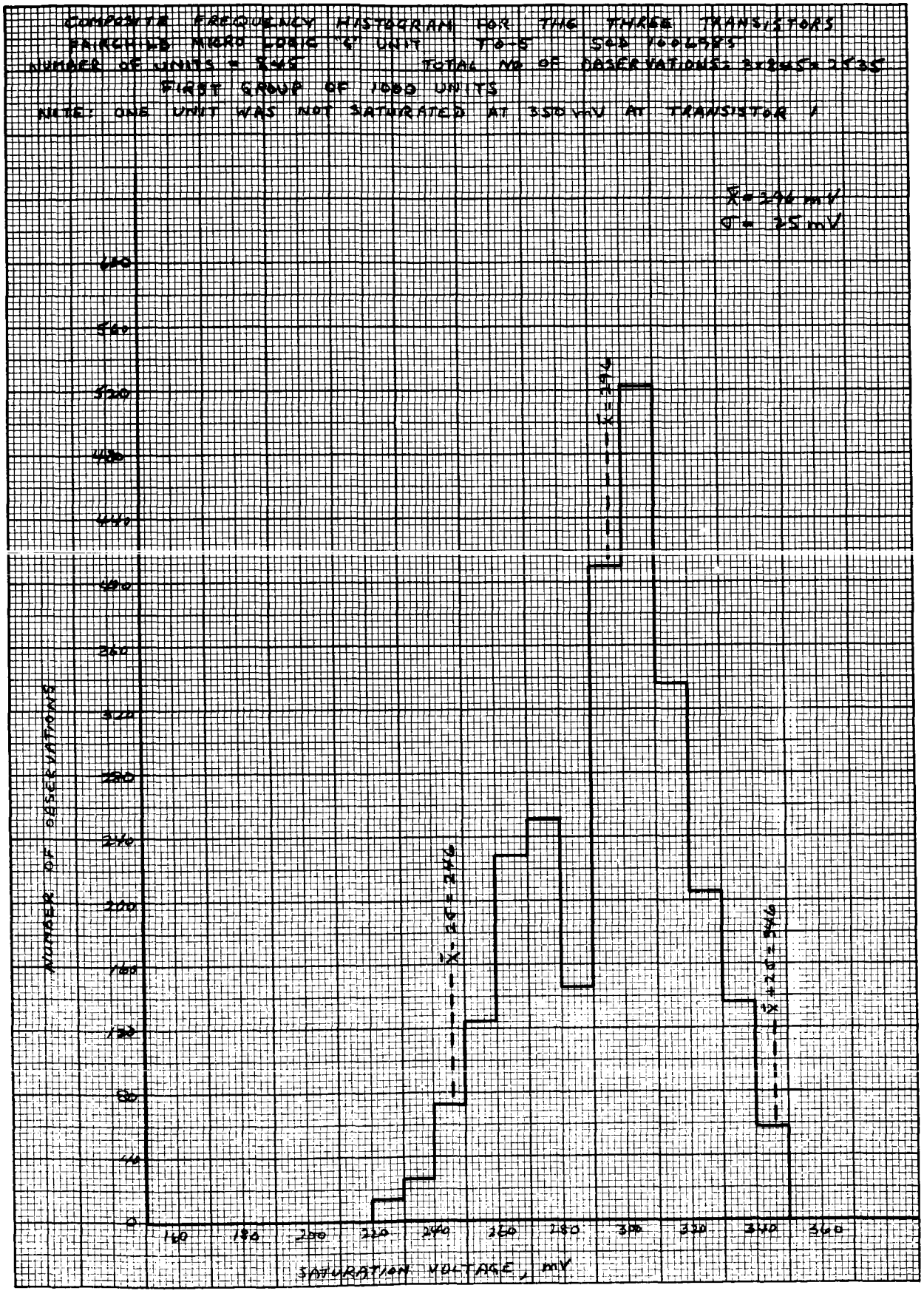

Figure 5-13. Saturation Voltage, Group A, Test 2

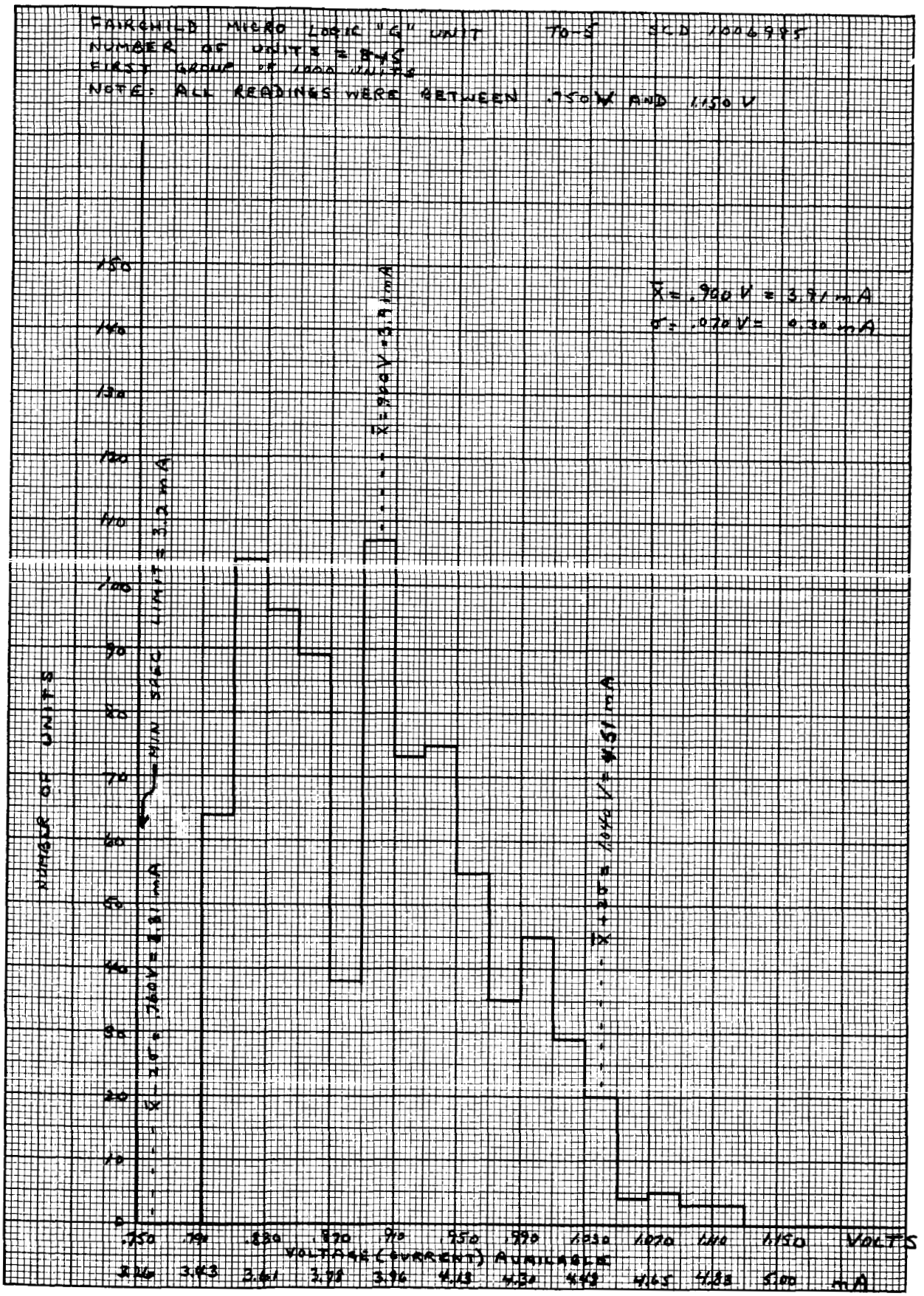

Figure 5-14. Current Available, Group A, Test 2

TABLE 5-4
TEST CONDITIONS, GROUP B, TEST 2

TEST NO.	PARAMETER		INPUTS						CULLING LIMITS		SPEC LIMITS	
			1	3	4	5	6	8	MIN	MAX	MIN	MAX
1	BASE CURRENT	IB1	.79	.79	GND	.79	—	3V	250μA	800μA	—	800μA
2	BASE CURRENT	IB2	.79	.79	GND	.79	—	3V	250μA	800μA	—	800μA
3	BASE CURRENT	IB3	.79	.79	GND	.79	—	3V	250μA	800μA	—	800μA
4	OUTPUT VOLTAGE	VCE1	.79	—	GND	—	—	3V	200mv	400mv	—	400mv
5	OUTPUT VOLTAGE	VCE2	—	.79	GND	—	—	3V	200mv	400mv	—	400mv
6	OUTPUT VOLTAGE	VCE3	—	—	GND	.79	—	3V	200mv	400mv	—	400mv
7	SATURATION VOLTAGE	VCES1	1.2	—	GND	—	—	3V	200mv	350mv	—	—
8	SATURATION VOLTAGE	VCES2	—	1.2	GND	—	—	3V	200mv	350mv	—	—
9	SATURATION VOLTAGE	VCES3	—	—	GND	1.2	—	3V	200mv	350mv	—	—
10	CURRENT AVAILABLE		.54	.54	GND	.54	230Ω	3V	735mv	—	3.2MA	—
11	ICEO		—	—	GND	—	—	—	—	1.0MA	—	—
12	IEBO		GND	GND	6.5	GND	—	—	—	1.0MA	—	—
13	ICBO		GND	GND	—	GND	—	—	—	1.0MA	—	—

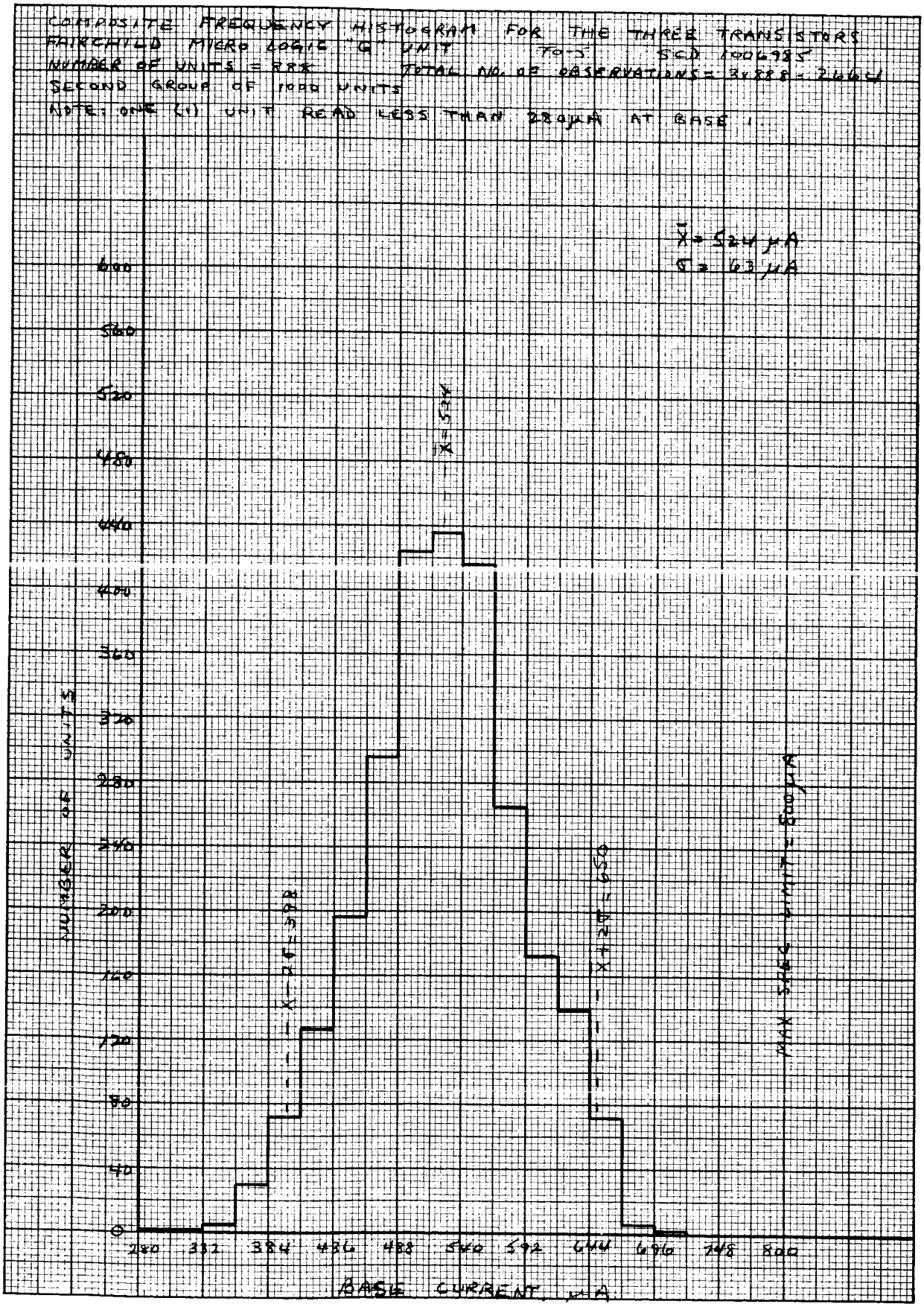

Figure 5-15. Base Current Data, Group B, Test 2

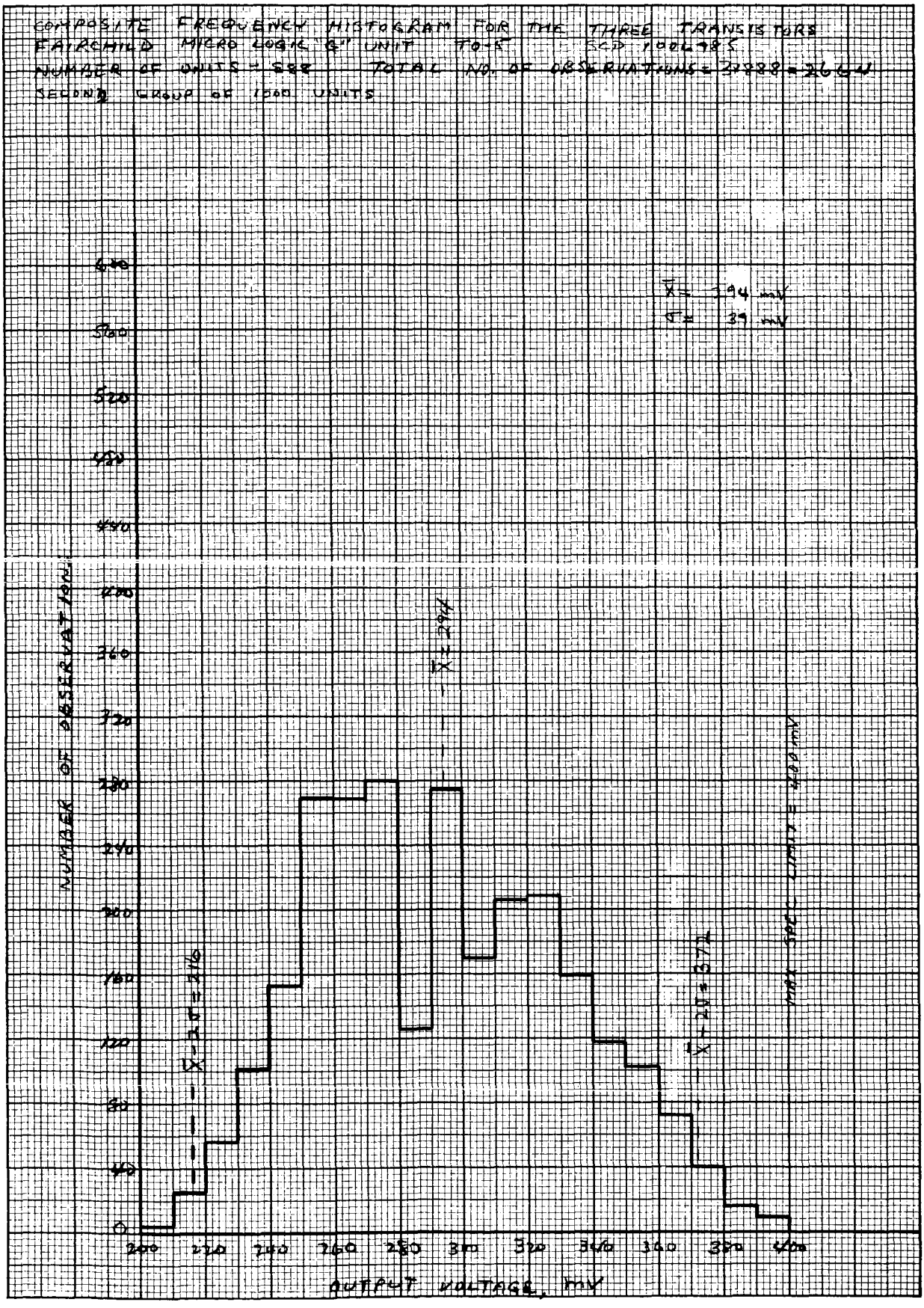

Figure 5-16. Output Voltage Data, Group B, Test 2

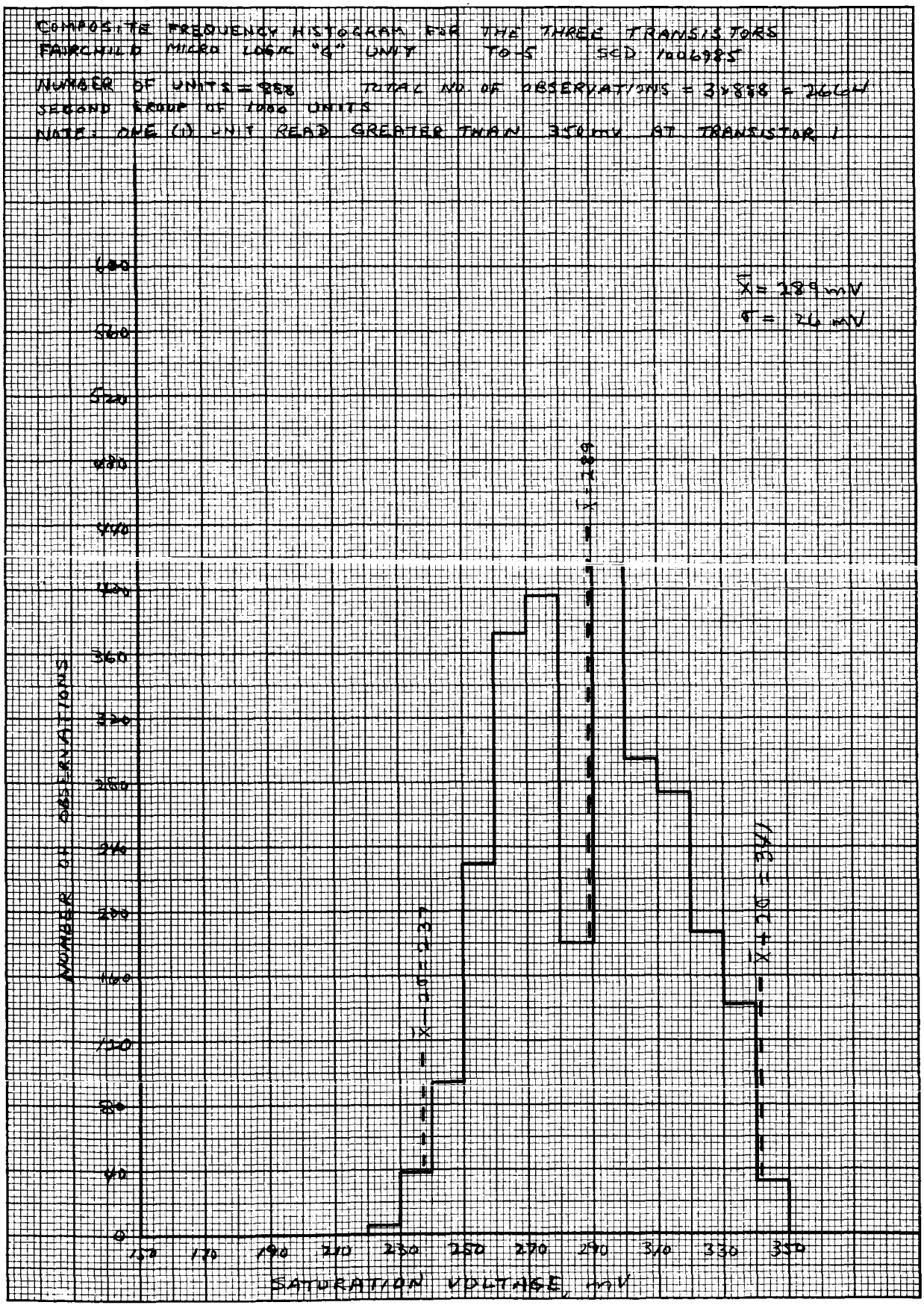

Figure 5-17. Saturation Voltage, Group B, Test 2

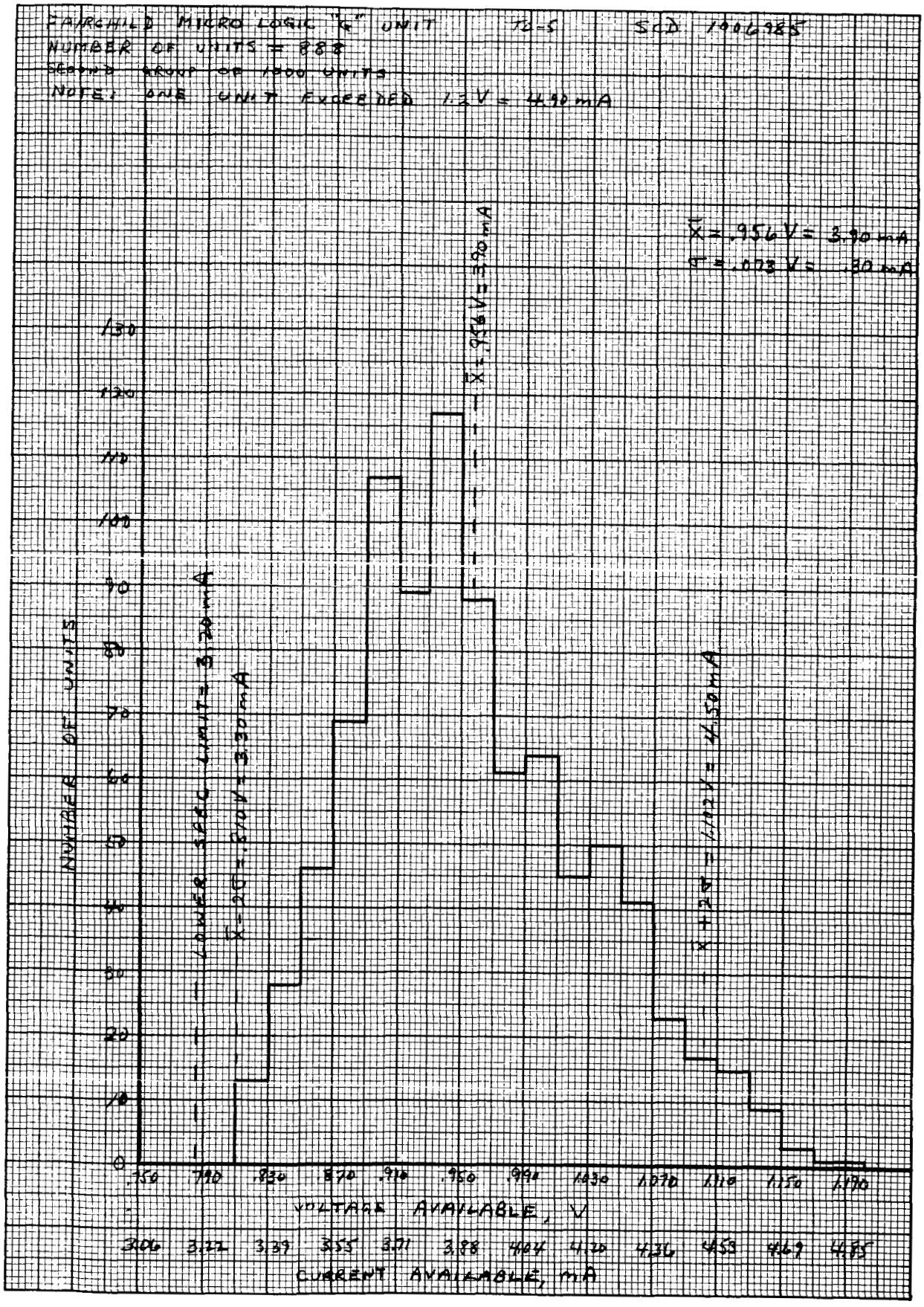

Figure 5-18. Current Available, Group B, Test 2

SECTION VI
DOCUMENTATION

SECTION VI
DOCUMENTATION

6.1 GENERAL

Issue 2 of the AGCIS has been distributed. Issues 3 and 4, concerning the Arithmetic Stick and Erasable Memory, respectively, are presently undergoing engineering review. These issues will be distributed as soon as possible. Issues concerning Interpretive Instructions and Logic Sticks B and C are in process. Errata Sheet No. 4, which adds a physical description of the AGC to Issue 1, will be distributed by mid-April.

Two-hundred and ninety requests for Specification Control Drawings (SCDs) have been received to date; two-hundred and thirty-one have been completed; fifty-nine are in process.

Revision 4 of the Documentation Plan is illustrated on figure 6-1. During this reporting period, Raytheon received Technical Directive Numbers 72 and 78 concerning the Core Rope Simulator and AGC Familiarization Manual, respectively. Raytheon has assigned a resident engineer to MIT/IL to assist in SCD coordination. An unedited motion picture has been submitted to MIT/IL in compliance with Technical Directive No. 43.

ITEM	TASK	DESCRIPTION	TYPE GROUP	TD NO.	QTY	STATUS
1.0	DEVELOPMENT PLAN MANUFACTURING SUPPORT FACILITIES	RAYTHEON FORMAT	II	TDR-2	1	COMPLETED SEPT 1962
2.0	SPECIFICATIONS AGC INTERFACE GSE INTERFACE SPECIAL PROCESS AND MATERIALS SCD'S	NO SIMILAR TO OD'S	I I I I	TDR-66 TDR-39 TDR-3/44	1 1 20 200	IN PREPARATION 5 COMPLETE 231 COMPLETED
3.0	FACTORY TEST PLANS AGC GSE	RAYTHEON FORMAT	III	TDR-11	 1 1	IN PREPARATION
4.0	PROCEDURES IN PROCESS TESTS IN PROCESS INSPECTION IN PROCESS ASSY FINAL ACCEPTANCE TESTS	RAYTHEON FORMAT NO SIMILAR TO OD'S	 III III III I			
5.0 5.1	REPORTS PROGRAM PROGRESS TD REPORT PROGRAM PLANNING MANAGEMENT	RAYTHEON FORMAT		TDR-43	MONTHLY	
5.2	TECHNICAL DATA & ANALYSIS		II	TDR-29	AR	
5.3	FAILURE DATA REPORT		II	TDR-43	AR	
5.4	EMERGENCY ACTION REPORT		II	TDR-43	AR	
5.5	MONTHLY TECHNICAL PROGRESS REPORT		II	TDR-21	MONTHLY	
5.6	QUARTERLY TECHNICAL PROGRESS REPORT		II	TDR-21	QUARTERLY	
5.7	RELIABILITY AND QUALITY CONTROL REPORTS		II			
5.8	QUALIFICATION TEST REPORTS		I			
5.9	MOTION PICTURE REPORT (TOTAL 20 MIN.)	20 MIN. TOTAL	II	TDR-43		UNEDITED MOVIE TO MIT/IL
5.10	STILL PHOTOS	300 SHOTS {(2 NEGATIVES & 3 PRINTS OF EACH)	II	TDR-43	300	11 SUBMITTED TO MIT/IL
6.0	INFORMATION SERIES			TDR-30		
7.0	MANUALS					
7.1	AGC FAMILIARIZATION		I	TDR-78		
7.2	AGC OPERATION & MAINTENANCE		I			
7.3	GSE OPERATION & MAINTENANCE 1. COMPUTER TEST SET 2. COMPUTER SIMULATOR 3. CALIBRATION EQUIPMENT		I			
7.4	CORE ROPE SIMULATOR		II	TDR-72		
8.0	DOCUMENTATION ADMINISTRATION			TDR-26		
9.0	SCD RESIDENT ENG			TDR-36		
10.0	ASST. RESIDENT SCD ENG			TDR-77		
11.0	DOCUMENTATION SCHEDULE		II	TDR-27		

AR = AS REQUIRED

Figure 6-1. Documentation Plan, Revision 4