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ERASABLE FERRITE MEMORY-

MOD 3C COMPUTER

by

D. Shansky

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ERASABLE FERRITE MEMORY - MOD 3C COMPUTER

ABSTRACT

The operation of a ferrite core memory system, with a capacity of 512 - 16 bit words, is described with reference to its application to the Mod 3C computer.

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TABLE OF CONTENTS

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Introduction

A memory whose capacity will be 512 - 16 bit words has been specified for Mod 3C. The memory will be capable of operation over a temperature range in excess of 0^{o} to 85^{o}C with ± 20% power supply environment and will consume approximately 3 w of power.

A number of different storage schemes were evaluated to fulfill this specification. Among these were a 2 core/bit constant flux memory, an externally selected memory, and a coincident current memory. The coincident current memory was chosen for detailed design because of economy of equipment and power.

At the time of the start of this development, two core vendors, R.C.A. and Ampex, introduced a new ferrite core material that is characterized by an extremely low coefficient of temperature vs coercive force (~0.1%/^{o}C). Unfortunately, this insensitivity to heat is obtained at the cost of increased drive current (~ 1 amp turn for full switch). These cores typically switch in less than 1 μ sec under coincident current excitation.

A block schematic of the proposed memory system is shown on Fig. 1.

In the interest of reducing the number of active drivers and keeping the active element count down, metal tape switch

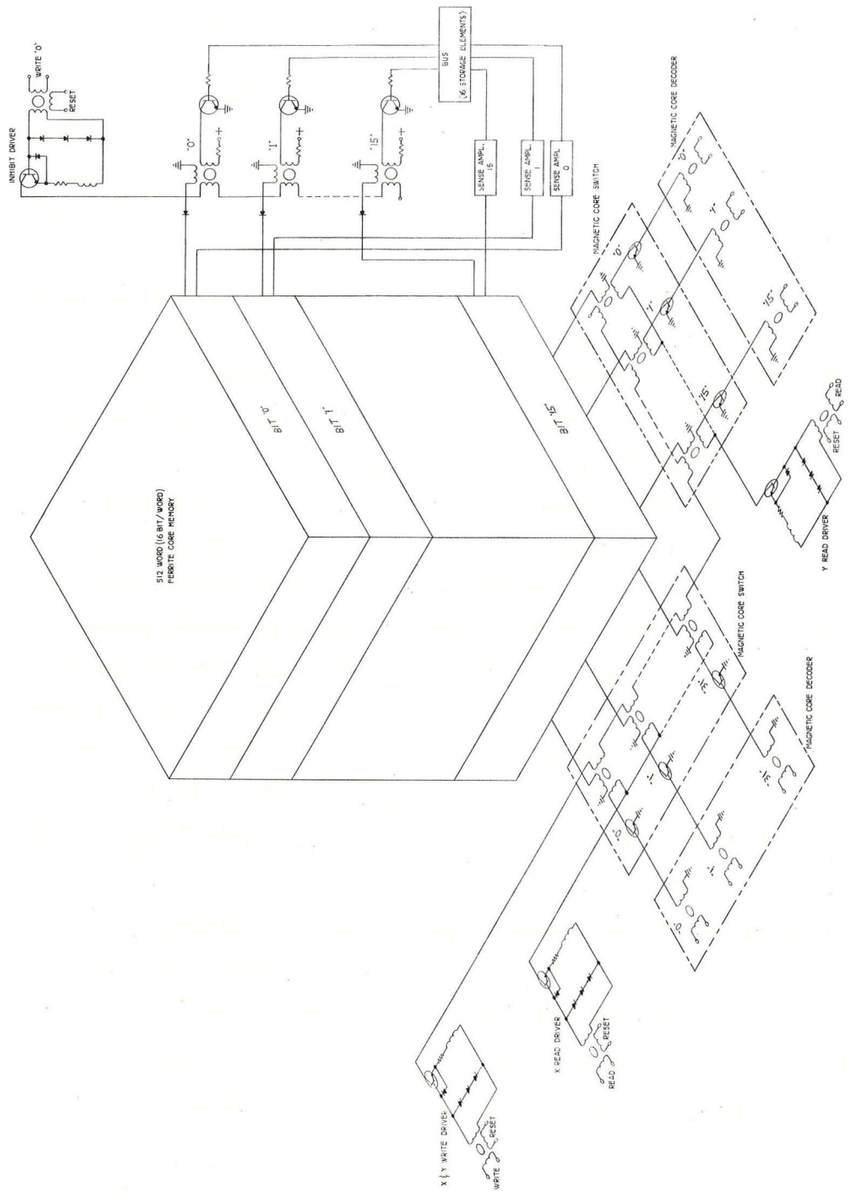

Fig. 1 Ferrite core memory

cores will be used both for DRIVE and ADDRESS selection on all 3 axes of the memory. It will be noted that there are only four current sources in the memory: two READ DRIVERS, one WRITE DRIVER and one INHIBIT DRIVER.

Operation of the Memory

Decoding of the X and Y coordinates will be done by means of a magnetic core matrix switch. Each of the cores in the decoder will be equipped with a multi-turn winding connected to the base-emitter diode of a silicon transistor such as the 2N1613. The core will be arranged such that it switches under constant voltage conditions and hence presaturates 2 of the 1613's (one in X and one in Y). A short time after the cores begin to switch (to avoid effects of noise), the two driver cores in question will be pulsed by a constant current source, thus driving the switch cores to the "1" state and consequently furnishing 1/2 amplitude READ current pulses down the X and Y selection lines. Within 3/4 of a μ sec from the start of the current pulses on X and Y, an output will appear on each of the 16 sense lines. This output will be sensed by an amplifier similar to that presently employed in the fixed memory and its output will condition a latch circuit, 16 of which comprise the WRITE BUSES. Connected to the WRITE BUSES will be 16 transistors whose purpose it will be to write a "1" into any of the switch cores connected to the INHIBIT lines in the memory. A zero will be written into the memory when the INHIBIT DRIVER is actuated driving all of the preset switch cores from "1" to "0".

The WRITE current pulse is generated by resetting all of the coordinate (X and Y) selecting cores to zero with a constant current source during the WRITE portion of the cycle.

One of the parameters of the switch core which varies as a function of temperature is the coercive force. With metal

tape cores this variation is of the order of 0.05%/^{o}C. Tracking over the temperature range appears to be about 20% with run-of-the-mill cores. Since the coercive force appears as a shunt resistance in the equivalent circuit, some attempt will be made to secure better tracking by selection. The result of an increase in temperature will be a lowering of the effective coercive force (increase in shunt resistance) thus increasing the memory current at high temperatures -- an undesirable direction. The transistor current driver, on the other hand, suffers a decrease in current of the order of 0.4%/^{o}C, resulting in a condition which tends towards compensation over the temperature range. The current could be made to exactly compensate by a choice of the appropriate switch core material, temperature sensing references in the transistor current drivers, or the choice of the appropriate storage core material. Of the three, the most promising course of action seems to be the third course, that is, specifying the appropriate storage core. In order to exactly compensate for the drivers, the variation in coercive force with temperature would have to be specified to be of the order of 0.3%/^{o}C or a factor of 3 poorer than existing materials. Compliance with this specification would result in a lowering of coercive force and hence a decrease in drive current and power -- from our standpoint, a favorable development. It should be emphasized that the variation of current with temperature in the drivers results naturally from the simple circuit we propose to employ.

The proposed transistor driver circuit is shown on Fig. 2. The switch core is overdriven so that its switching time is constrained and determined by the voltage drop appearing across the three forward biased silicon diodes: D_1, D_2, and D_3 ($N\Delta\Phi$ = et). Diode D_4 prevents breakdown in the base-emitter diode when the core is reset. The constant voltage drop dictated by these diodes causes a constant voltage to appear across the series combination of the base-emitter diode, the resistor R, and the inductor L. If V_{eb} is assumed constant, R will determine the steady state

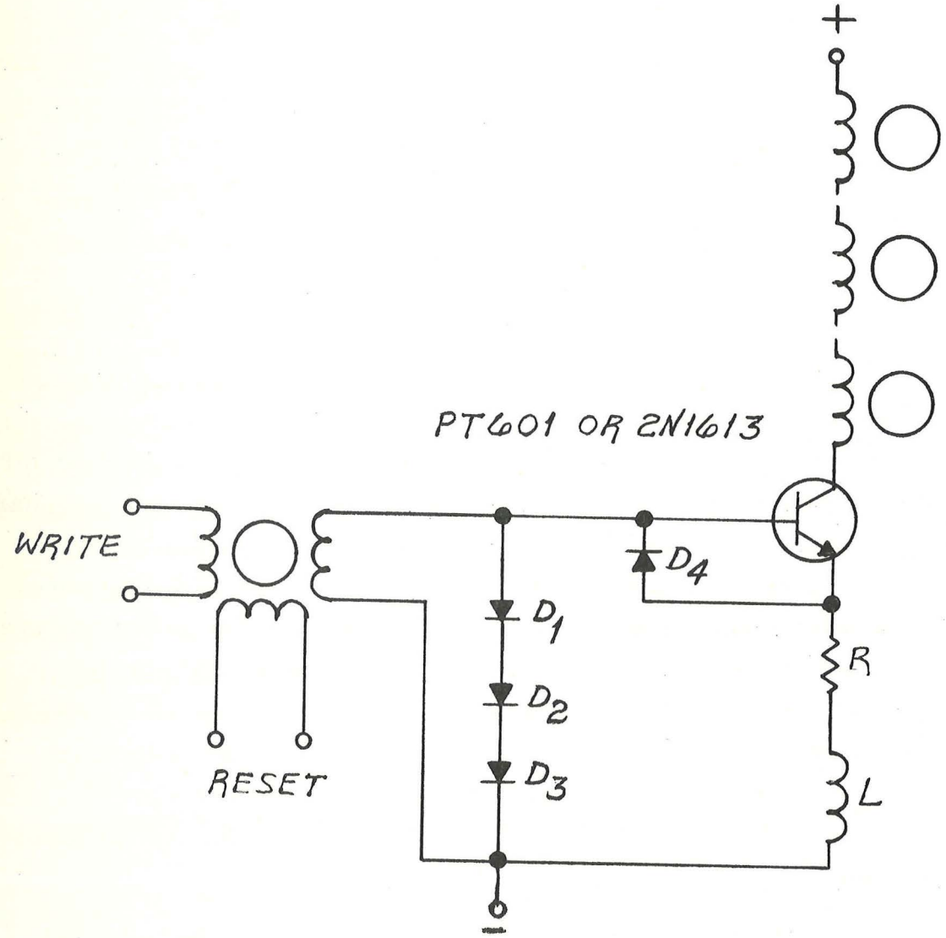

Fig. 2 Pulsed current source

current and L will dictate the $\frac{di}{dt}$. The collector supply voltage will be adjusted so that the transistor remains out of saturation thus presenting a driving point impedance equal to R_{cc} shunted by C_c. In this manner a current pulse source with controlled rise time, controlled duration and output current (over a specified range) independent of load and supply voltage can be made. Since the values of R and L are of the order of 2 Ω and 1μh, respectively, both resistance and inductance could conceivably be purchased as a single wire-wound resistance. The above circuit would be used for all the required current sources, with only component values and transistor types changing to meet the needs of the various differing current and load requirements.

The actual line drivers (X, Y, and INHIBIT), as indicated on the block schematic, will be metal tape (Mo Perm) switch cores. A tentative switch core design has been completed and experimental work to verify the calculation is in progress. The required secondary $N\Delta\Phi$ is obtained by summing the flux changes necessary to drive the line resistance, inductance, shuttle flux of non-switching cores and flux change in switching cores. The number of primary ampere-turns is adjusted so that $NI_{pri} = NI_{load} + NI_o$, where NI_o is the coercive force and other primary loss terms.

Design Details

Upon the assumption that 512 words could be packaged in a 1" x 1" x 2" volume, the resistance, and inductance of representative X, Y, and INHIBIT lines were computed. The shuttle flux and switching flux change of a few of the cores to be used as memory cells were measured and these values were used to determine switch-core load. This computation led to the following flux change requirements for the various lines

X = 188.5 maxwells
Y = 127.1 maxwells
Z = 400.5 maxwells .

It should be noted that wire resistance in the memory is in all cases

the dominating portion of the load. In the case of the Z axis, the series silicon diode, which disconnects the switch core from the line during reset time, completely overshadows the remaining load components.

The number of primary turns will be adjusted so that compatibility with expected power supplies and transistor driver capability exists.

Of the 512 words which will be furnished, only 464 will be addressable and the remaining 48 words will be used as emergency spares in the event of a bit failure in any word. The 48 words which have been set aside will be supplied as modified C-16 packages. It is expected that the sense windings in the C-16 will simply be series connected with the corresponding sense lines in the Ferrite memory resulting in the saving of 16 sense amplifiers. This connection is possible because there is the same flux capacity in the C-16 core as in the ferrite storage core.