OPTIONAL FORM NO. 10
5010-104

UNITED STATES GOVERNMENT

Memorandum

AUG 11 Rec'd
Pal 8-101

3.2.2.4

TO : EG/Chief, Guidance and Control Division

DATE: August 10, 1965

In reply refer to:
EG44-362-65

FROM : EG44/Deputy Manager, Apollo G&N Project Office

SUBJECT: Block II computer design deficiency

Summary - August 2, MIT/IL discovered that the Block II computer might not work due to excessive signal propagation time in the micrologic interconnect matrix. This was caused by more capacitance than allowed for in the logic design. August 4 MIT was confident that the computer would not operate without major changes and they notified MSC. After a meeting August 6 with MIT/IL, ACED, and Raytheon, it appears that the only way to maintain the present spacecraft schedules, with an operating computer, is to change from the multilayer nickel ribbon interconnect to a multilayer circuit board. With this change, and some modifications to early breadboard system ribbon interconnects, it appears that required deliveries can be met at an increase in program cost of less than $500,000.

Problem - In the Block II computer MIT/IL based the design on a matrix capacitance of 100 picofarads. This is the measured value of the matrix of the Block I computer. However, the matrix fabrication was changed from a welded wire interconnect to a very dense nickel ribbon approach. Figure 1 is a cross section of the matrix. MIT/IL did not anticipate any increase in the matrix capacitance over the Block I design.

When the first tall logic sticks were delivered to MIT/IL the signal propagation time was so great, due to the high matrix capacitance, that the computer would not operate at design speed. The measured times, for the longest run length, are as follows:

a. $T_u + T_m + T_o$ = 650 nano sec. (computer will not operate at design speed)

b. $T_m + T_o$ = 600 nano sec.

c. $T_u + T_o$ = 350 nano sec.

d. T_o = 300 nano sec.

T_u = delay in the unscrambler matrix (unique to the tall logic computers and not present in the flight configuration)

T_m = delay in the punched nickel ribbon interconnect matrix

T_o = delay in four parallel gates plus the tray wiring

INDEXING DATA

DATE	OPR	#	T	PGM	SUBJECT	SIGNATOR	LOC
08-10-65	MSC	EG44-362-65	M	GN	(Above)	FRASIER	065-65

As can be seen, the delay that is unique to tall logic configuration (T_u) is 50 nano seconds and the interconnect matrix delay is 300 nano seconds. The design value for the matrix delay was approximately 60 nano seconds.

To make the computer operate, with these propagations times, would require an entire logic redesign which would decrease the computer speed. MIT/IL estimates that the decrease might be as much as 50%.

Possible Solutions - The changes which could be made to make the computer operate are listed below:

a. Redesign the logic to accommodate the delay times. This would result in a six month to one year schedule slip and would probably produce a computer that will not meet the Apollo requirements.

b. Increase the micrologic power by a factor of 2. This is done by decreasing the output resistor which requires a change in fabrication masks and a requalification program.

c. Decrease the capacitance in the present matrix by optimizing the layout, decreasing the ribbon width, increasing the insulation thickness, and changing the insulation material.

d. Change from a nickel ribbon matrix to a multilayer board interconnect.

Solution "a" is the least desirable.

If the micrologic power is doubled, the computer power consumption will increase by 15 to 20 watts. The agreement to allow a change, from Block I, to low power micrologic was conditioned by the requirement to design the computer to accept high power (Block I) logic in the event of difficulty. However, this has not been observed by MIT/IL. Therefore, the ability of the power supply to supply additional energy and the adequacy of the thermal design are questionable for higher power logic. The design will not accommodate the high power Block I logic. MIT/IL is currently investigating the impact of doubling the logic power. The most serious impact of increasing the power is estimated to be the availability of logic elements. It is estimated that it would require at least seven weeks to obtain higher power gates, in flat packs, or transistor cans, as engineering prototypes. Allowing two weeks for welding the gates to boards, the first computer could not be operating until October 11, 1965. Since the logic design cannot be confirmed until after a complete computer is operational, the design could not be frozen until approximately November.

This would cause a one month schedule slip throughout the program. A more serious impact would be caused by the availability of gates for pre-production systems. The low power gates for pre-production computers are purchased and in stock. The production buy is approximately five weeks into the procurement cycle. A requirement to change the logic would slip the delivery of all systems at least two months since early prototypes are in fabrication now. It would also result in scrapping approximately $180,000 worth of micrologic (6 computers at $30,000 each) and increased cost due to the mask change.

It may not be possible to sufficiently decrease the capacitance in the present matrix by a redesign. The amount of reduction possible by optimizing the layout, within the space available, is completely unknown. It is only possible to decrease the ribbon width by changing the manufacturing process from stamping to chemical etching. This change would increase the matrix fabrication difficulties and increase the computer cost. MIT/IL does not think it is possible to increase the insulation thickness significantly in the present logic module mechanical design. Changes in insulation do not result in dramatic decreases in the capacitance. For example, mylar is 3.2 while the best material available is paraffin with K=2.1. The only way to determine the effect of all these changes is to actually design, manufacture, and measure the delay times.

If the computer is changed from a nickel ribbon to a multilayer board (MLB) interconnect, the delay time in the matrix is reduced from 300 nano seconds to 100 nano seconds. This is based on tests run at MIT/IL with multilayer boards manufactured as a parallel development to the ribbon interconnect. MIT/IL personnel think that this is enough reduction to make the computer work. They are currently getting micrologic put on a complete set of boards (by Raytheon) and expect to have the majority of a computer operating by August 18. The reduction in delay is primarily due to the narrower (0.020) conductors and the 0.008 in spacing between layers. The use of the multilayer boards would also allow further increase in the insulation thickness, and a further reduction in delay, if the interconnections between thicker layers can be made reliably. There is adequate room in the present logic modules to increase the thickness of the boards. However, without further reduction in the MLB capacitance, the margin in the design appears to be inadequate. If certain changes discussed below are made to some of the pre-production computers, the MLB's can be incorporated without impacting the system availability dates. The change to MLB's would cause some scrap but would result in a lower production cost.

Recommended Action - To minimize cost, risk, and schedule delays it is recommended that you and Dr. Shea approve the use of multilayer logic interconnect boards and medium power micrologic (if required) for all Block II computers. With this approval, the following actions will be taken:

a. Immediate procurement of multilayer boards to the latest logic design. Fortunately, MIT/IL has kept the masters at Mel Par updated on a continuous basis. Specifically, Mel Par boards would be procured by Raytheon for computers PC-1, PC-2, PC-3, PC-4, 200 R, 601 and subsequent production. MIT/IL has two sets of boards in-house which will be used for 200 M and 600 M. After my approval, MIT/IL initiated procurement for 3 sets of boards from Mel Par, August 6. This will result in an expenditure of approximately $30,000 and will be within their current contract cost and scope (per L. Larson). Two sets will be used for MIT/IL evaluation and the third set to update 200 M to a 600 F configuration or to use for 200 C.

b. Modify the nickel ribbon matrix of computers 200 C, PC-1, PC-2 and possibly PC-3, to the four wide configuration, with teflon insulation, shown in figure 2. It is estimated that this will reduce the capacitance by a factor of 3.9 or more. Raytheon is fabricating an experimental matrix to demonstrate this approach. This will result in a combined unscrambler and interconnect matrix delay, in the tall stack configuration, which is slightly more than that obtained in a flight type computer with multilayer boards. This approach is necessary to provide easily modified breadboard computers which can be manufactured while the computer design is being verified. By using this method, the only computer delivery that will be delayed is 200 C which is a Raytheon system for PAC (core rope simulator) and FTM program checkout. Multilayer boards will also be procured for PC-1, PC-2, and 200 C in the event the changed ribbon matrix does not work. To provide a multilayer board backup, it is also recommended that tall logic and ribbon interconnect be provided, in parallel, for PC-3. This design cannot be used in flight type computers due to space limitations.

c. Review the adequacy of the computer design to handle the higher power (by a factor of 2) micrologic and modify the power supply and thermal design if required.

d. Have AC Electronics initiate procurement, immediately, for enough medium power micrologic for two computers. This will initiate the procurement of the medium power logic early enough to allow its incorporation into PC-2 and 601 (for LTA-1) in the event there is not enough time margin with the low power logic. The margin available should be indicated by September 1 and demonstrated by October 1. With the tooling available, from the initial order, there is adequate time to expand production for all subsequent systems. It should be pointed out that this is a hedge against the unknown effect of the change to multilayer boards. Due to the large investment that will exist in low power logic in the near future, it is mandatory that the correct design be determined as soon as possible.

e. Have AC Electronics thoroughly investigate all available multilayer board fabrication techniques and establish a second source as soon as possible to insure reliable board production. MIT/IL has agreed to provide duplicate masters (and whatever else is needed to establish a second source rapidly) to AC Electronics from Mel Par.

f. Install micrologic on the multilayer boards for PC-1. This is necessary to insure a computer for the GAEC flight control integration which operates exactly like the flight computers.

Estimated Cost - A rough cut estimate of the cost of implementing the recommended changes is outlined below:

a.	Multilayer board procurement	
	MIT/IL 3 sets (in scope)	$30,000
	Raytheon 3 sets (the necessary headers are currently under contract)	30,000
	TOTAL	$60,000
b.	Modify the nickel ribbon interconnects	
	200 C	$50,000
	PC-1 and PC-2 are in scope	
	Tall logic for PC-3	19,000
	TOTAL	$69,000
c.	The cost of adapting the computers for medium power logic	unknown
d.	Medium power micrologic for two computers (without extensive quality control)	$90,000
e.	Establish a second source for multilayer boards and purchase two sets for evaluation	$90,000
f.	Additional micrologic to fabricate the logic for PC-1 on multilayer boards in parallel with the tall logic configuration	$40,000
	TOTAL	$349,000

It is estimated that part of this can be either negotiated as in scope or recovered later due to the lower computer costs resulting from the use of multilayer boards.

Schedule - If the above recommendations are followed, the primary G&N can support the current spacecraft schedules. However, certain changes to the requirements are necessary. GAEC has requested two breadboard computers, one for use in flight control integration (FCI) and one in rendezvous radar integration (RRI). Both of these computers require a core rope simulator (PAC) for operation. Since GAEC is only scheduled for one PAC, and the computers are much smaller than a PAC, only one breadboard computer is being alloaated for FCI and RRI.

NAA has requested a computer for electrical compatibility testing by February 1 and a complete system for House Spacecraft 1 on April 1. In addition, they have requested the following:

a. computer for CSDV 1 3/1

b. complete system for CSDV II 9/1

c. computer for mission evaluators 8/1

To meet these requirements, the following system allocation is proposed (and required to meet all G&N system availability requirements):

a. Furnish system 201 to NAA on 2/1 for electrical compatibility testing. Transfer this system to the house spacecraft for futher integration 4/1.

b. Deliver computer PC-3 on 3/1 for CSDV part I testing. Transfer PC-3 to the mission evaluator 8/1. This is the scheduled completion date of CSDV part I and the evaluator required date.

c. Deliver a complete systems, less optics, with computer PC-5 to NAA on 9/1 to support that required date.

This meets NAA's needs at I understand them. Computer PC-4 would be available for MSFC simulations 6/1/65.

To avoid any schedule impacts, it is mandatory to obtain MSC approval of the entire recovery program no later than August 10, 1965.

Cline W. Frasier

Enclosure
cc:
EG42/G. Rice EG/R. Chilton
EG43/H. Croyts
PA/J. Shea
PA/W. Lee
PS/O. Maynard

EG44:CFrasier:caj 8-11-65

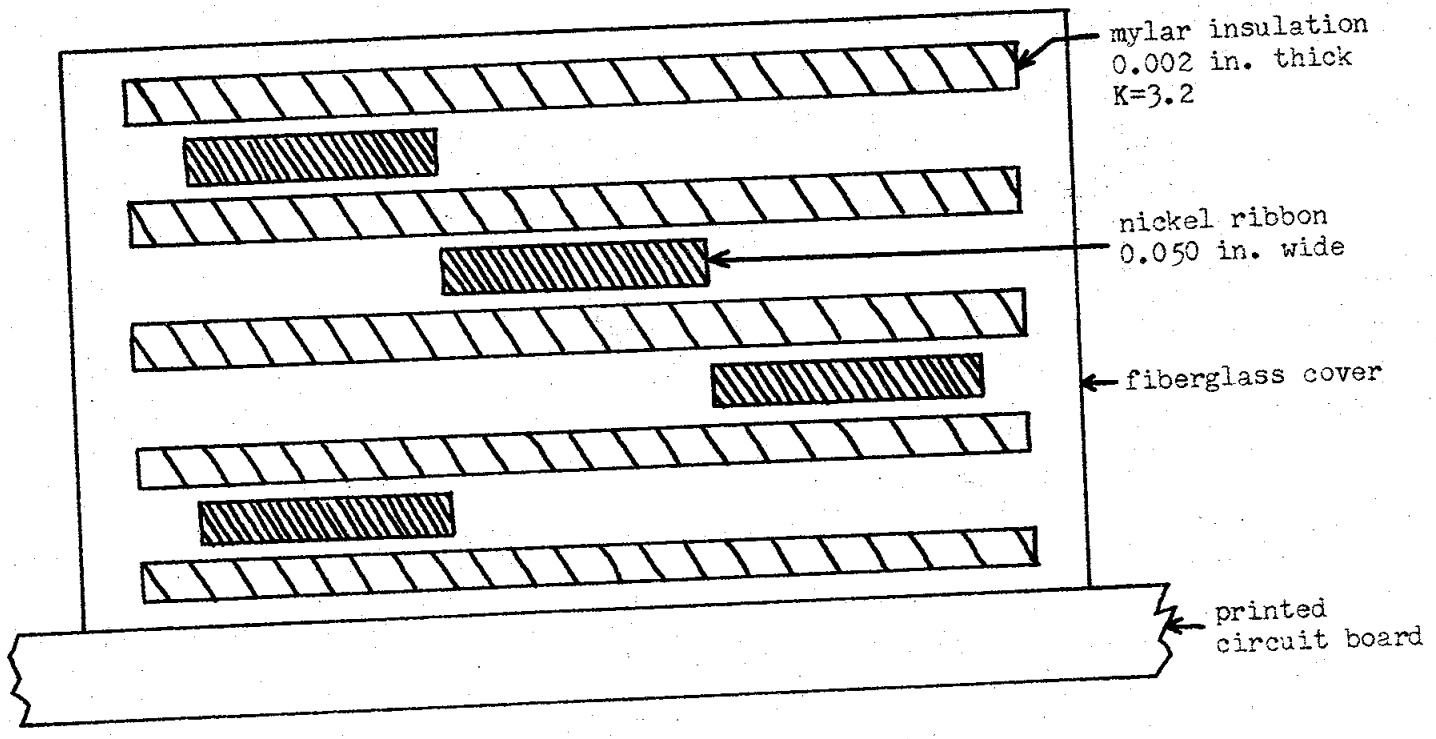
mylar insulation
0.002 in. thick
K=3.2
nickel ribbon
0.050 in. wide
fiberglass cover
printed
circuit board

Figure 1

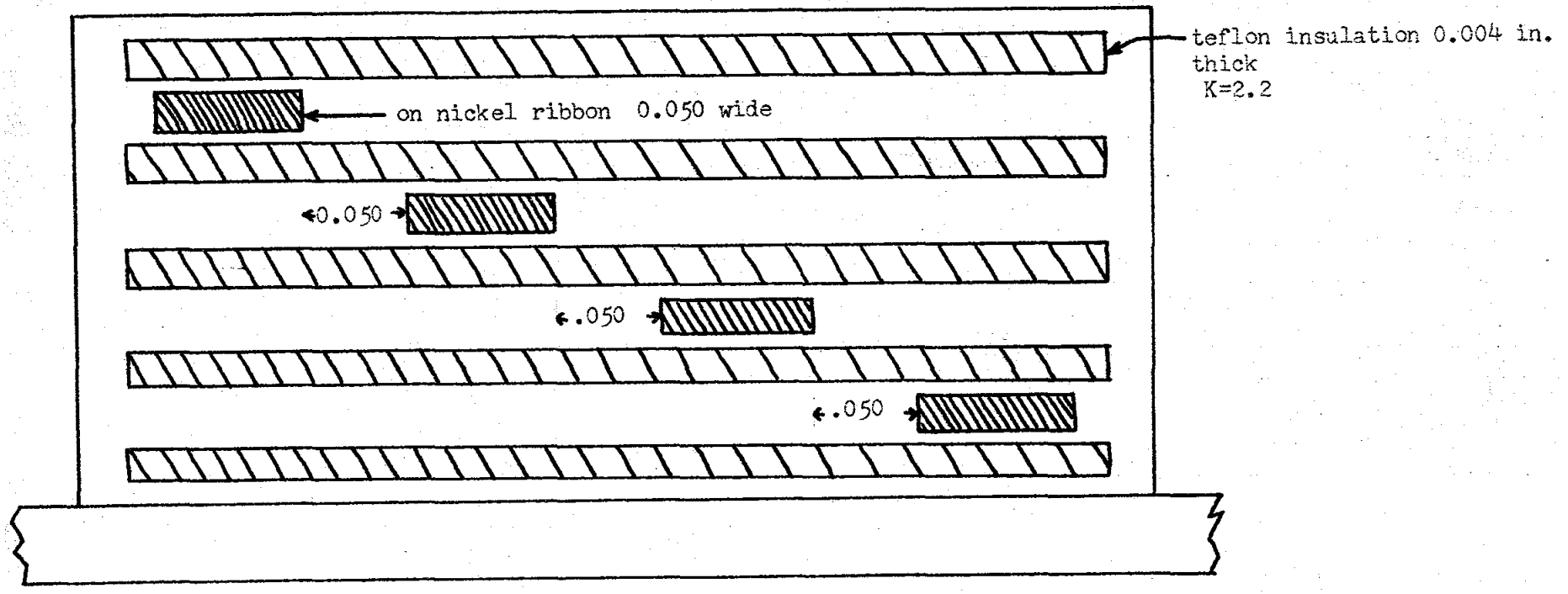
teflon insulation 0.004 in. thick
K=2.2
on nickel ribbon 0.050 wide
0.050
.050
.050

Figure 2