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PREPARED BY	TITLE	DATE
Stanley S. Pachulski Raytheon Co.	Technical Writer	5-27-64

EXAMINED BY	TITLE	DATE
Edwin A. Rogers	Design Engineer	5/27/64
J. Isenmark Raytheon Co.	Engineer	5/27/64

APPROVED BY	TITLE	DATE
Kenneth Bowen Raytheon Co.	Proj Eng	5/28/64

APPROVED BY	TITLE	DATE
Charles Sperling MIT/IL	Staff Engineer	7/5/64

APPROVED BY	TITLE	DATE
Elda C Hall MIT/IL		7/8/64

APPROVED BY	TITLE	DATE
W. Bagnall NASA/MSC		7/21/64

CONFIGURATION CONTROL BOARD RELEASE BY

Walter S. Kupfer — 21 July 1964

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LIST OF EFFECTIVE PAGES

THE TOTAL NUMBER OF PAGES IN THIS PUBLICATION IS 218 , CONSISTING OF THE FOLLOWING:

Page Number	Revision	Page Number	Revision
i	A	4-13	A
ii	Original	4-14 thru 4-15	Original
iii thru v	A	4-16 thru 4-21	A
vi thru vii	Original	4-22	Original
viii	A	4-23 thru 4-24	A
ix thru x	Original	5-1	Original
1-1	A	5-2	A
1-2	Original	5-3	Original
1-3	A	5-4 thru 5-7	A
1-4	Original	6-1	Original
1-5	A	6-2	A
1-6	Original	6-3	Original
1-7	A	6-4 thru 6-5	A
1-8	Original	7-1	Original
1-9	A	A-1 thru A-2	A
1-10	Original	B-1	A
1-11	A		
1-12	Original		
2-1 thru 2-2	A		
2-3	Original		
3-1 thru 3-2	A		
4-1 thru 4-3	A		
4-4	Original		
4-5	A		
4-6 thru 4-8	Original		
4-9 thru 4-10	A		
4-11 thru 4-12	Original		

All JDC's listed in Appendix A including data sheets are part of this manual (151 pages)

CONTENTS

CONTENTS (cont)

CONTENTS (cont)

ILLUSTRATIONS

TABLES

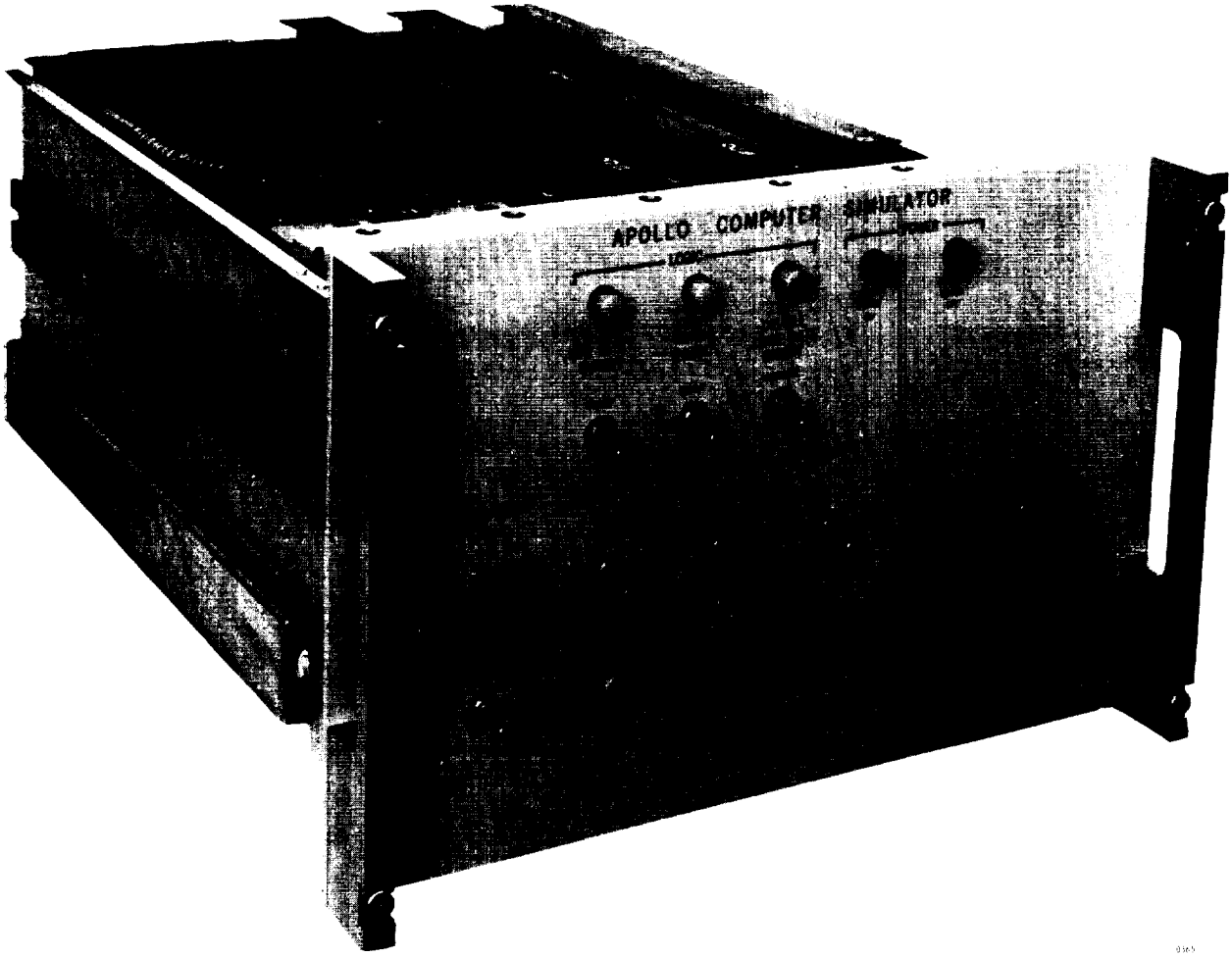

Figure 1-1. Apollo Guidance Computer Simulator

Chapter 1

DESCRIPTION AND LEADING PARTICULARS

1-1 INTRODUCTION

This technical manual contains a description of the operation, theory, calibration, and maintenance of the Apollo Guidance Computer (AGC) Simulator, Part Number 1014061. The AGC Simulator (figure 1-1) is a part of the Ground Support Equipment (GSE) designed and fabricated by Raytheon Company, Space and Information Systems Division, Sudbury Operation, Sudbury, Massachusetts, as part of ACSP Subcontract FNP 12775.

1-2 PURPOSE OF THE AGC SIMULATOR

The purpose of the AGC Simulator is to produce drive rate outputs identical to those of the AGC for use during optics-inertial subsystem tests. The simulator is not intended to replace the AGC in these tests. Rather, it is intended for use in open-loop tests of various guidance and navigation subsystems, singly or in combination. The Simulator is part of the Optics-Inertial System Analyzer (1900005-011). (Refer to ND 1021035 for information on the analyzer.)

1-3 DESCRIPTION

The AGC Simulator is a compact, self-contained unit designed for installation in a standard 19-inch rack. The unit is fabricated with rack slides to facilitate access to the interior without removing the unit from the rack. It consists of a logic drawer containing three logic plate assemblies, a d-c power supply assembly, a hinged interconnection plate, and a hinged front panel. The simulator, exclusive of the front panel, is approximately 17 inches wide, 10 inches high, and 24 inches deep. The front panel, approximately 12 inches high and 19 inches wide, provides radio frequency interference (RFI) shielding.

Sixteen normal AGC inputs are accepted by the simulator buffer circuits. They are IMU and optics CDU encoder outputs and Δv's from the PIPA's. All of the pulse rates generated by the AGC for the CDU's, IRIG's, PIPA's, optics, and PSA are available with essentially the same options as in the AGC, although manually controlled.

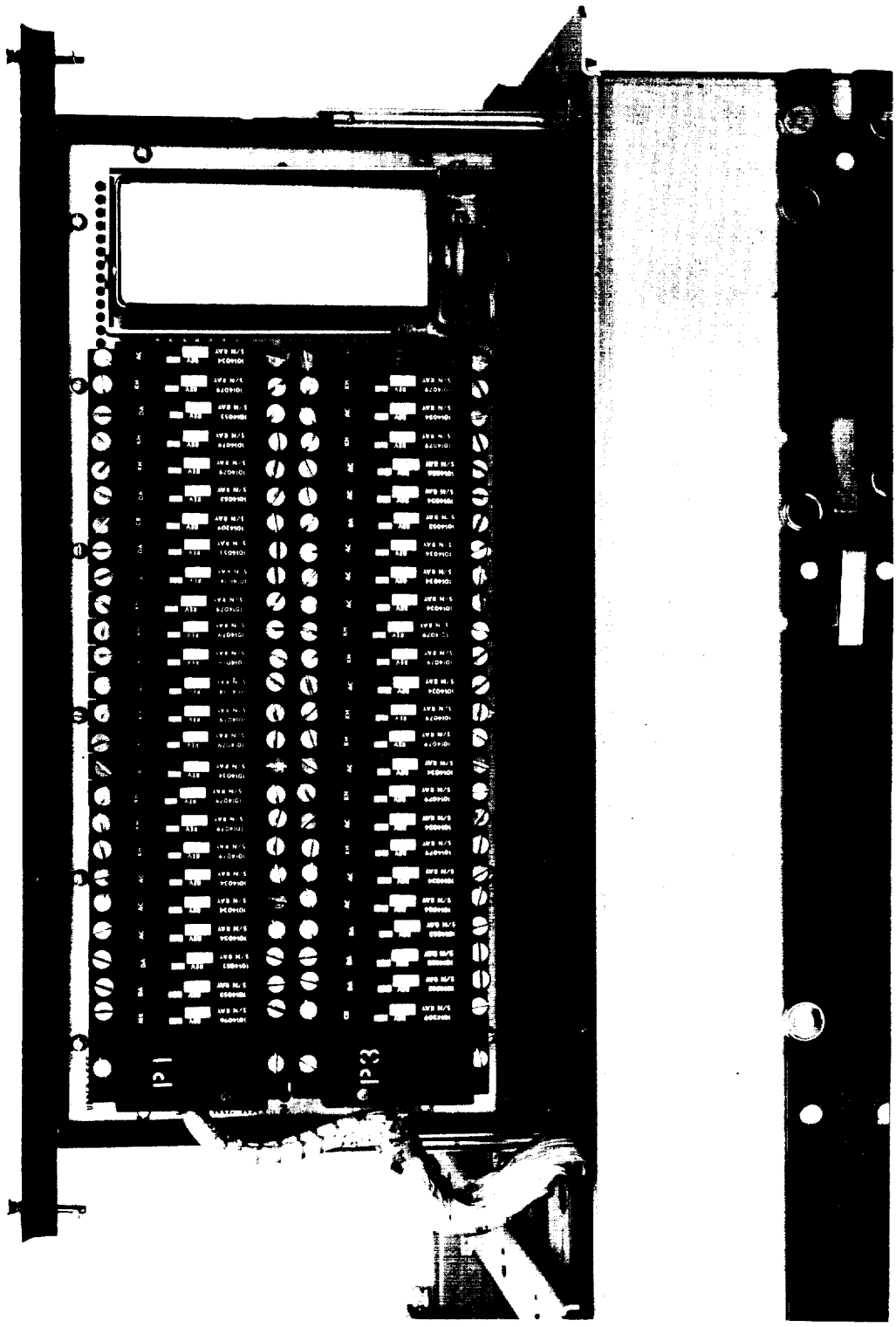

Figure 1-2. Logic Plate Assembly

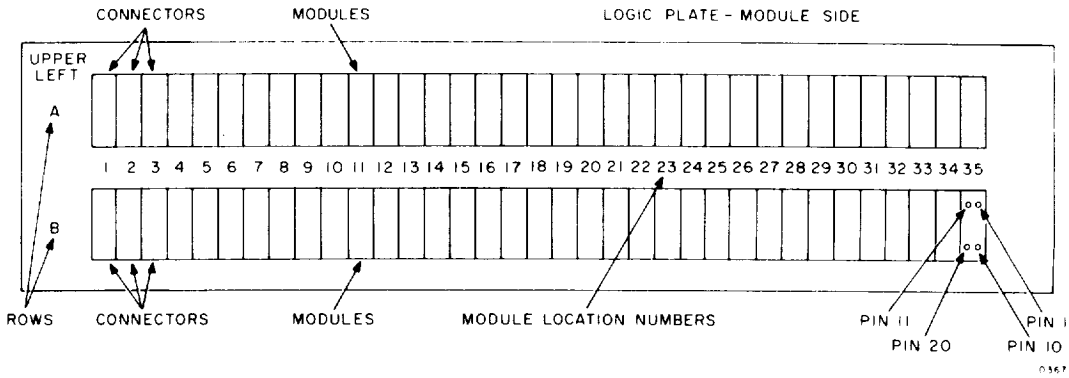

Figure 1-3. Logic Plate, Connector and Module Layout

1-3.1 LOGIC PLATE ASSEMBLIES. The logic modules for the simulator are contained in three logic plate assemblies. (See figure 1-2.) Each logic plate has a maximum capacity of 64 modules. A completely filled logic plate assembly weighs approximately 15 pounds. The modules are arranged in two rows, designated A and B. (See figure 1-3.) Each row is divided into 35 segments, the first three segments of each are occupied by a 60-pin connector. The remaining segments accommodate the modules. Interconnections between the modules are made on each plate assembly via the wirewrap technique. Interconnections between assemblies and output connectors are made in the interconnection plate by wirewrap.

The logic plates are slide-mounted and can be withdrawn to an access position and locked for inspection or troubleshooting purposes without removing the interconnection plugs. Logic plates are secured to the drawer with captive screws, one at each end.

1-3.1.1 Modules. Seven different GSE modules are required to perform the logic functions for the simulator. The modules are: NOR(AC), transformer (DA), resistor (FD), diode (HF), gated flip-flop (KH), interface coupling (CR), and driver (MK) modules. Connections within the modules are resistance-spot welded. A typical logic module is illustrated on figure 1-4.

The modules are secured to the logic plate by a pair of captive screws. Modules are keyed by an indexing receptacle under the captive screws. Encapsulation of the components provides wrap-around protection for the circuit components. The two notched areas at the end farthest from the connector accommodate a module extraction tool (figure 1-4). All modules are labelled

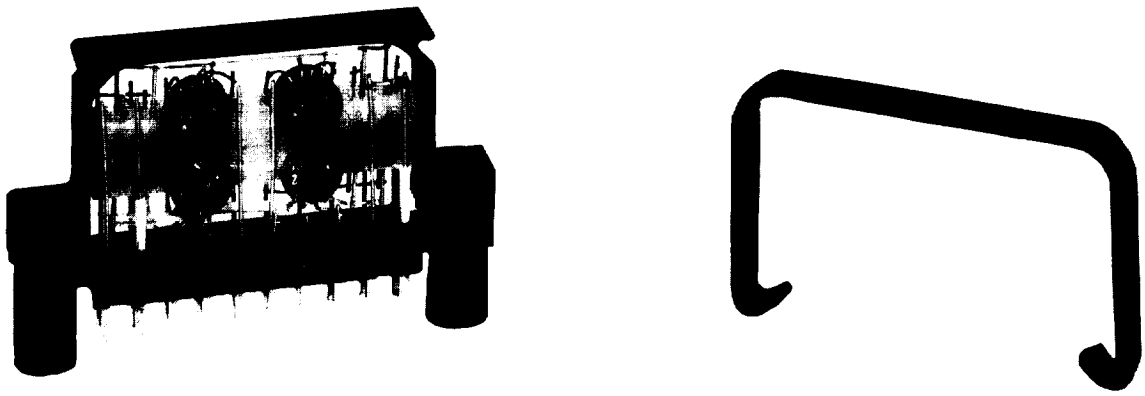

Figure 1-4. Logic Module and Extraction Tool

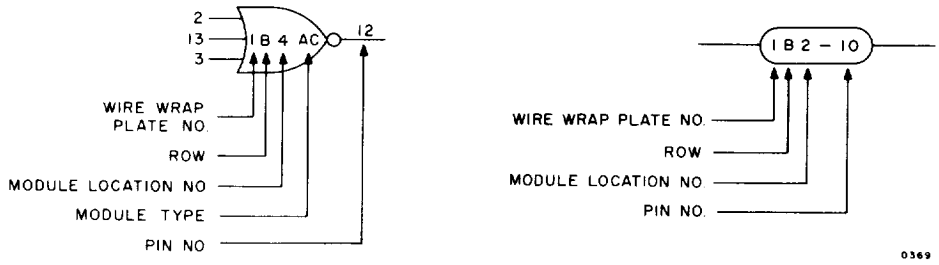

Figure 1-5. Module and Connector Identification

on the logic diagrams with a code to aid in location and identification. Figure 1-5 is an illustrated description of how to use this code on modules as well as connector pins within the simulator.

The basic logic-function circuit element contained in the modules is a NOR gate. A NOR gate is an integrated circuit composed of a resistor and three NPN transistors. The combination of four NOR gates is a NOR module. A gated flip-flop module contains eight such NOR gates.

Output interface between the simulator and the G and N is accomplished through the use of transformer-coupled common-emitter stages. Two of these stages are combined to form one transformer driver module.

Two modules are used to provide "steering" and current-limiting functions for the logic circuits. The steering function is provided with a diode module containing four two-input diode gates and two single-input diode gates. Current limiting is accomplished with a resistor module which contains nine separate resistors.

Input interface between the simulator and the G and N is provided by a transformer coupled interface circuit. Four of these circuits are combined to form one interface coupling module.

Current gain for the illumination of three indicator lamps on the front panel is provided by driver circuits. Four of these circuits make up one driver module.

1-3.2 D-C POWER SUPPLY ASSEMBLY. The d-c power supply assembly (figure 1-6) is mounted in the space normally allotted to logic plates 4 and 5

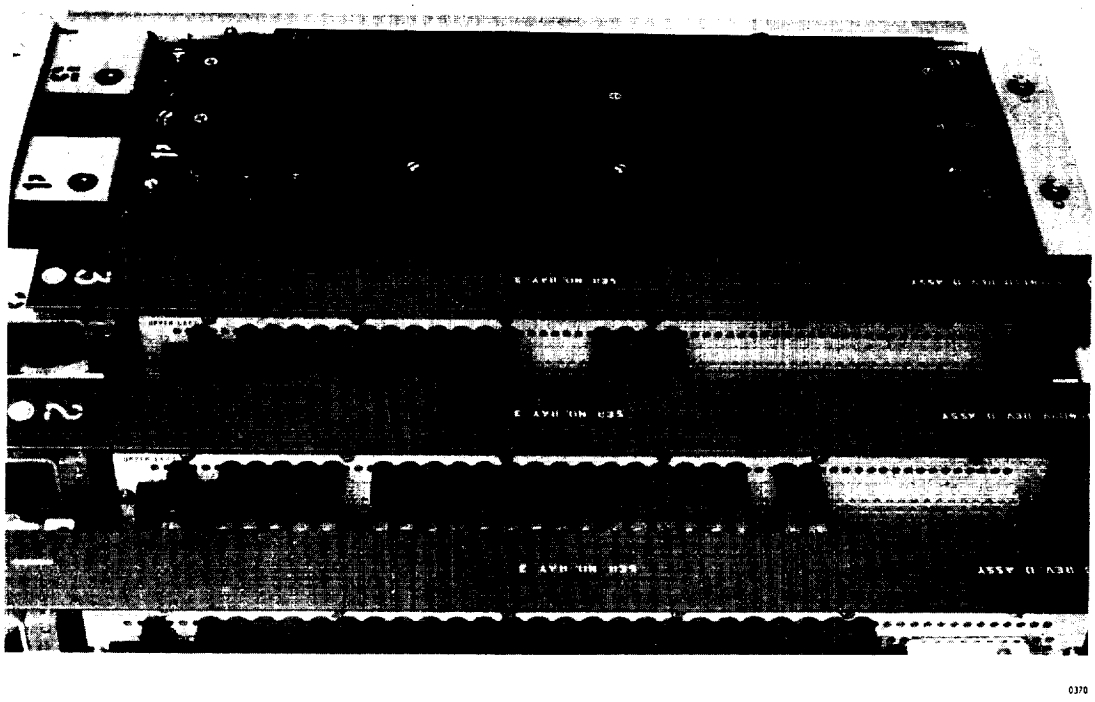

Figure 1-6. D-C Power Supply Assembly

in a standard GSE logic drawer. The assembly is composed of two modular power supplies (+3 vdc and +13 vdc) and two encapsulated relays, all mounted in inverted positions. The undersides of the supplies and relays are protected by a cover which acts as a heat sink and is easily removed to facilitate servicing. Two holes in the cover provide access to power supply output voltage adjustments. Monitor jacks for these adjustments are located on the cover. The input to the d-c power supply assembly is 115 vac, single phase, 60 cps. A single cable assembly connects the supply to the interconnection plate, where the power is distributed throughout the simulator. The LOGIC POWER switch is located on the d-c power supply assembly also.

1-3.3 INTERCONNECTION PLATE. The interconnection plate (figure 1-7) is similar in size and general construction to a logic plate. The plate is

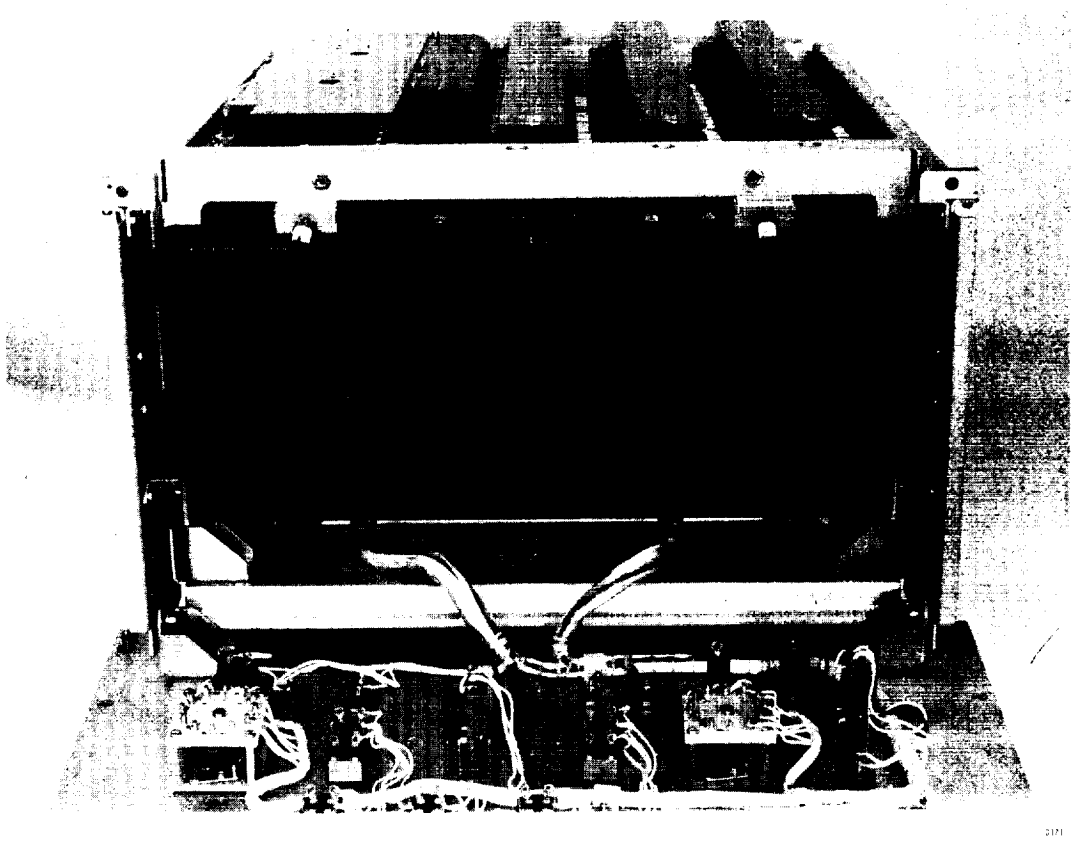

Figure 1-7. Interconnection Plate

hinged at the bottom and fastened to the chassis structure at the top with captive screws. The plate tilts forward to provide access to the cables and internal connectors inside the chassis structure. Stops on each side of the chassis hold the plate away from contact with the inside of the front panel.

1-3.4 FRONT PANEL ASSEMBLY. The front panel assembly (figure 1-8) is attached to the chassis structure by a pivot at each bottom corner and by captive screws at each top corner. The captive screws are accessible only from the rear of the panel. Therefore, the simulator must be withdrawn from the rack before the front panel can be tilted forward to provide access to the interconnection plate. Handles at each end of the front panel facilitate removal of the simulator from the rack. All controls and indicators required to operate the simulator are mounted on the front panel.

1-4 LEADING PARTICULARS

1-4.1 EQUIPMENT SUPPLIED. The equipment supplied as part of the AGC Simulator is listed in table 1-I.

1-4.2 POWER REQUIREMENTS. The AGC Simulator requires a source of 115-vac, 60-cps, single-phase power capable of sustaining a current drain of approximately 1 ampere.

1-4.3 INSTALLATION REQUIREMENTS. The AGC Simulator is designed for use in the Optics-Inertial System Analyzer (1900005-011). It can be mounted in any standard 19-inch rack that can accommodate the 24-inch depth and 12-1/4-inch front panel height of the simulator.

1-4.4 COOLING REQUIREMENTS. The AGC Simulator requires approximately 60 cfm of cooling air at a static pressure of 0.1 inch H_2O.

1-4.5 OPERATING CONTROLS AND INDICATORS. The operating controls and indicators for the AGC Simulator are shown on figures 1-6 and 1-8 and are listed in table 1-II.

1-4.6 EQUIPMENT HISTORY. The original part number for the Computer Simulator was 1014061. However, as a result of NECP R-00003 (RIB No. 0104003), which incorporated a logic power failure circuit to enable an external sync signal, from the ACSP Optics-Inertial Analyzer, to be supplied to the power supply circuits in the PSA in the event of a Computer Simulator power supply failure, the part number was changed to 1014061-011. Any simulator that does not have this change has the part number 1014061-000.

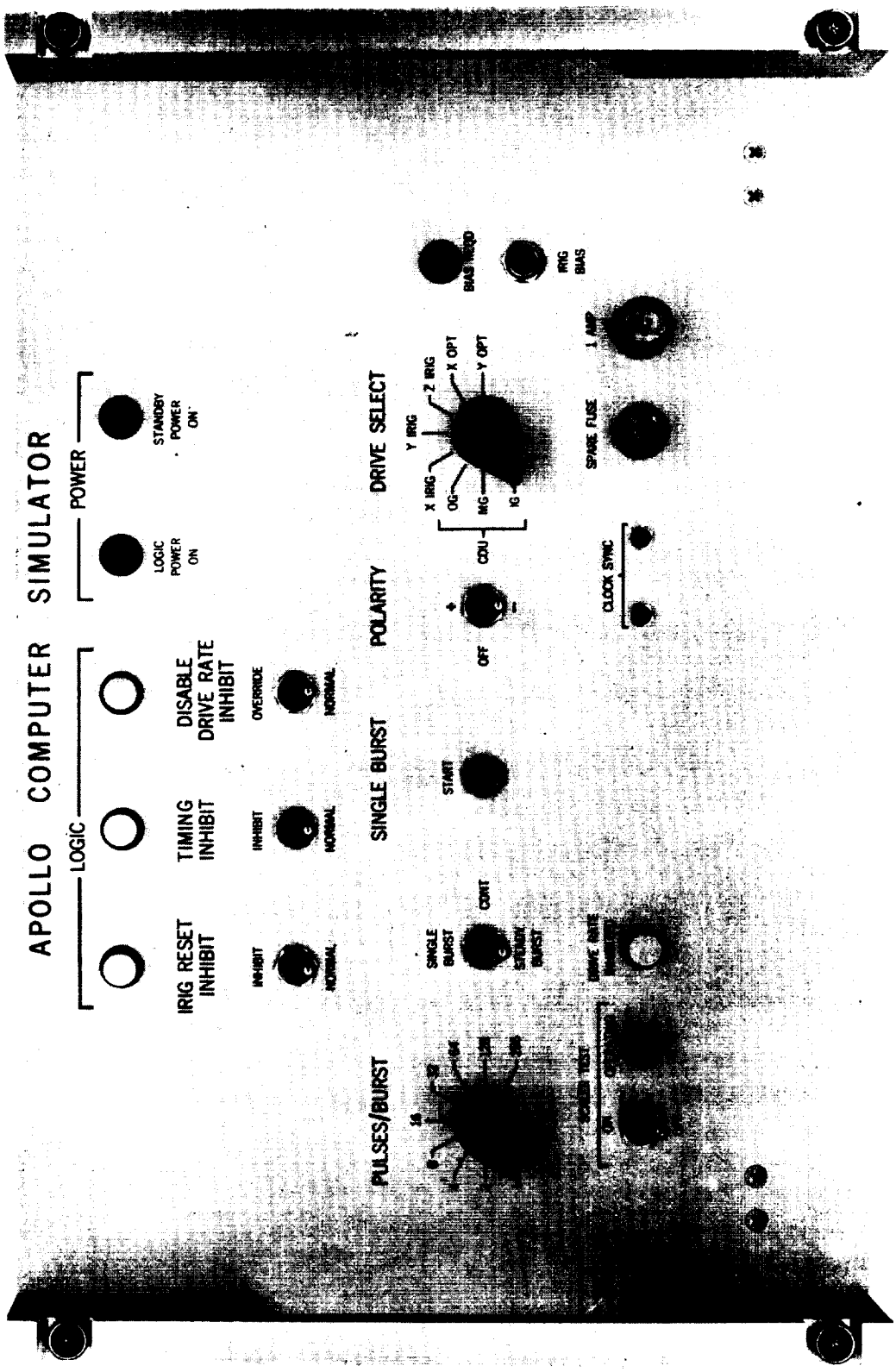

Figure 1-8. Front Panel Assembly

Table 1-I. Equipment Supplied

Description	Part Number
Frame support	1014007
Retainer screw	1014013
Frame	1014014-2
Cable bracket	1014017
Channel, bottom RT	1014027
Channel, bottom LT	1014028
Chassis structure	1014045-8
Cable assembly W1	1014046-1
Cable assembly W2	1014046-2
Cable assembly W3	1014046-3
Support bracket	1014081
Chassis assembly, dc power supply	1014084
Logic plate 1	1014090
Connector bracket	1014094
Logic plate 2	1014099
Front panel	1014106
Logic plate 3	1014110
Cable assembly W6	1014112-1
Cable assembly W7	1014112-2
Cable assembly W8	1014112-3
Cable assembly W9	1014112-4
Interconnection plate	1014113
Cable assembly W4	1014120

Table 1-II. Operating Controls and Indicators

Control or Indicator	Functions
Power Functions	
STANDBY POWER ON light	Indicates that +13 vdc is applied to the crystal oscillator and oven. Indicates 115 vac is applied to the simulator.
LOGIC POWER ON switch (1)	Controls application of d-c voltages to logic plates.
LOGIC POWER ON light	Indicates application of d-c voltages to logic plates.
Program Functions	
DRIVE SELECT switch	Enables simulator output logic for one of eight axes (IG CDU, MG CDU, OG CDU, X IRIG, Y IRIG, Z IRIG, X OPT, and Y OPT).
Mode switch	Establishes the type of pulse rate (SINGLE BURST, CONT, or STEADY BURST) to be applied to the selected unit axis.
SINGLE BURST START switch	Initiates one burst of drive rate pulses.
PULSES/BURST switch	Selects pulse content of any burst in nonadditive binary steps of 1, 2, 4, 8, 16, 32, 64, 128, or 256 pulses per burst.
POLARITY switch	Enables either the positive or negative side of the unit axis selected by the DRIVE SELECT switch. Inhibits drive rate logic in the OFF position.
(1) On d-c power supply assembly.	

Table 1-II. Operating Controls and Indicators (cont)

Control or Indicator	Function
Program Functions (cont)	
IRIG BIAS switch	Provides biasing pulses to IRIG's and is operated in conjunction with BIAS REQD light.
BIAS REQD light	Indicates bias pulses are required for IRIG's, when lighted.
Inhibit Functions	
IRIG RESET INHIBIT switch and light	Inhibits IRIG reset function and indicates inhibiting action.
TIMING INHIBIT switch and light	Inhibits all outputs and indicates inhibiting action.
DISABLE DRIVE RATE INHIBIT switch and light	Disables externally generated drive rate inhibit signal and indicates disabling action.
Monitor Function	
DRIVE RATE INHIBITED light	Detects presence of externally generated drive rate inhibit signal.
Test Functions	
SCALER TEST OPERATING light and SCALER TEST ON/OFF switch	Provides indication of scaler operation. Switch in ON position causes light to flash at a 12.5-cps rate. Steady on or off indicates scaler is malfunctioning or TIMING INHIBIT switch is set to INHIBIT.
+3 VDC jack (1)	Provides test point for +3 vdc.
(1) On d-c power supply assembly.	

Table 1-II. Operating Controls and Indicators (cont)

Control or Indicator	Function
Test Functions (cont)	
+13 VDC jack (1)	Provides test point for +13 vdc.
0 VDC jack (1)	Provides test point for 0 vdc.
3 VOLT ADJUST control (1)	Controls output of 3-vdc supply.
13 VOLT ADJUST control (1)	Controls output of 13-vdc supply.
CLOCK SYNC jacks	Provides test points for 512-kc clock sync signal.
Fuses	
1 AMP blown fuse indicator	Provides 115-vac circuit protection indication.
SPARE FUSE holder	Provides storage for one spare fuse.
(1) On d-c power supply assembly.	

Chapter 2

TEST EQUIPMENT AND SPECIAL TOOLS

2-1 TEST EQUIPMENT

The test equipment required for maintenance or operation of the AGC Simulator is listed in table 2-I.

Table 2-I. Test Equipment Required

Equipment	Manufacturers' Part or Model Number	Application
AGC calibration system (see figure 2-1)	NASA 1014217	Clock oscillator calibration
Oscilloscope	Type 545A or equivalent; Tektronix, Inc., Beaverton, Oregon.	Waveform analysis
4-channel trace preamplifier	Type M or equivalent; Tektronix, Inc., Beaverton, Oregon.	Waveform analysis
Scope probes (4)	Type P6000 x 10; Tektronix, Inc., Beaverton, Oregon.	Waveform analysis
Precision DC differential voltmeter	Model 803B or equivalent; John Fluke Mfg. Co., Inc., Seattle, Washington	Power supply calibration
+13 vdc power supply	Model 855B or equivalent; Harrison Labs, Inc., Berkley Hgts, N. J.	Checkout

Table 2-I. Test Equipment Required (cont)

Equipment	Manufacturers' Part or Model Number	Application
Electronic counter	Model 6146 or equivalent, with extender, Model 602; Beckman Instruments Inc., Berkley Div., Richmond, Col.	Frequency and time interval measurements
Bendix connector pins, male and female crimp (25)	Bendix Corp, Scintilla Div., Sidney, New York	
Malco connector pins, female crimp (25)	Malco Mfg. Co., Chicago, Ill.	
Coaxial cable (BNC - test prods)		
Resistors, 200 ohm ± 5% (25)		

2-2 SPECIAL TOOLS

The special tools required for maintenance of the AGC Simulator are listed in table 2-II.

Table 2-II. Special Tools Required

Tool	Part Number	Application
Module extraction tool (see figure 1-4)	NASA 1014018	Logic module extraction

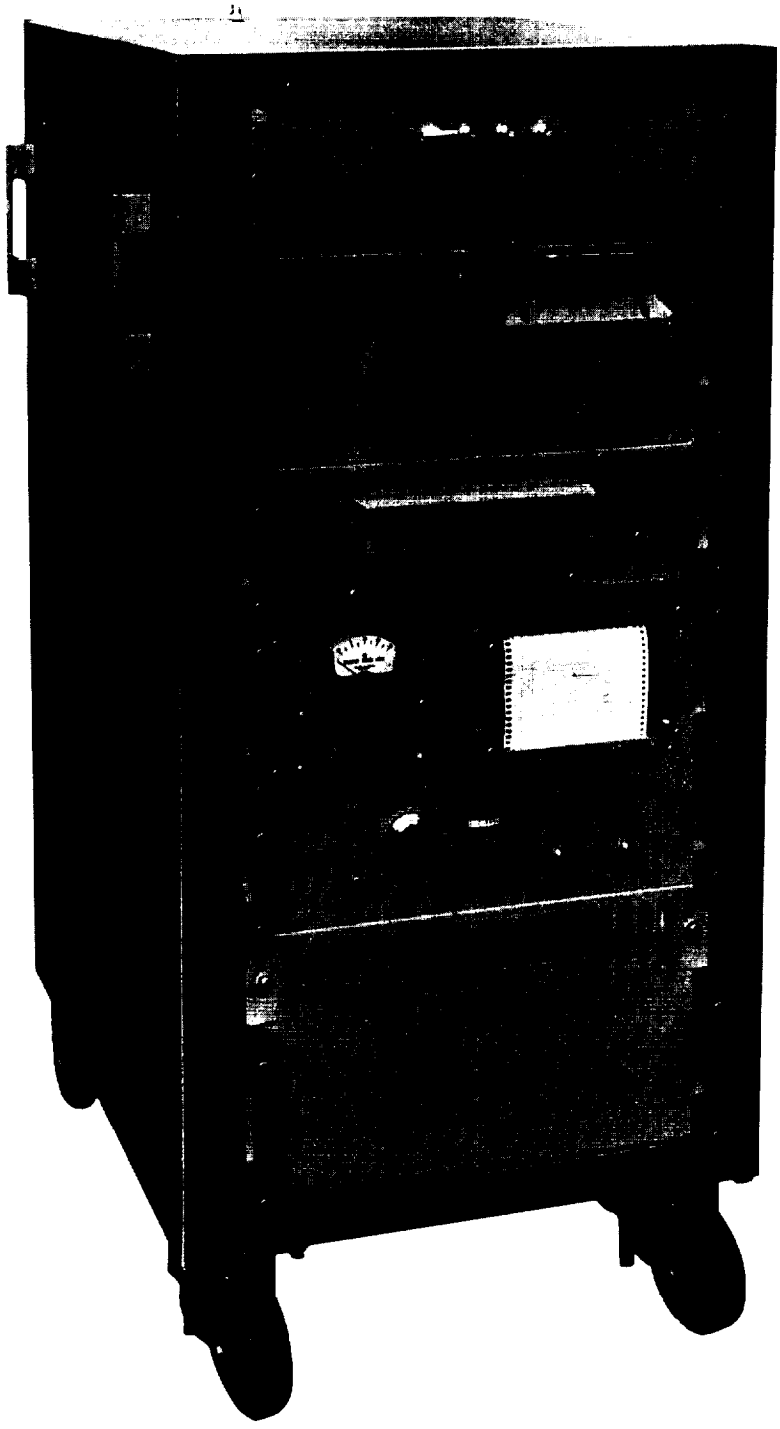

Figure 2-1. AGC Calibration System

Chapter 3

PREPARATION FOR USE AND RESHIPMENT

3-1 INTRODUCTION

This section contains information necessary to prepare the AGC Simulator for use by operating personnel. Instructions for reshipment are included also.

3-2 PREPARATION FOR USE

Preparation for use entails the performance of the tasks described in the following paragraphs.

3-2.1 INSTALLATION. The AGC Simulator is designed for installation in the Optics Inertial Analyzer. Refer to ND 1021035 for physical location for simulator. Slides for slide mounting the simulator are supplies. Installation of the slides should be performed according to good workshop practices.

The simulator can be installed in any 19-inch rack and requires 24-1/2 inches of space behind the front panel and 12-1/4 inches of vertical panel space. Slide travel is 30 inches. Logic plates extend 7 inches above the top of the front panel when withdrawn. The front panel extends 7-5/8 inches beyond the original position when lowered. The interconnection plate can be lowered to a position approximately 37 degrees from the vertical.

WARNING

Exercise care when lowering logic plates. Serious injury to fingers is possible if plate is dropped.

3-2.2 INTERCONNECTIONS. All external connections to the G and N system are made through two cables connected to jacks J1 and J2 (figure 3-1). Connections to display and test equipment are made through jacks J3 and J4. The jacks are located at the rear of the simulator. The plugs and jacks are keyed in such a manner that only the correct plug can be inserted into the mated jack.

3-2.3 COOLING. The AGC Simulator requires approximately 60 cfm of cooling air at a static pressure of 0.1 inch H_2O. It is designed to work at an ambient temperature of 0 to 50 degrees centigrade.

3-3 RESHIPMENT

Reship the AGC Simulator in accordance with procedure in JDC 19533.

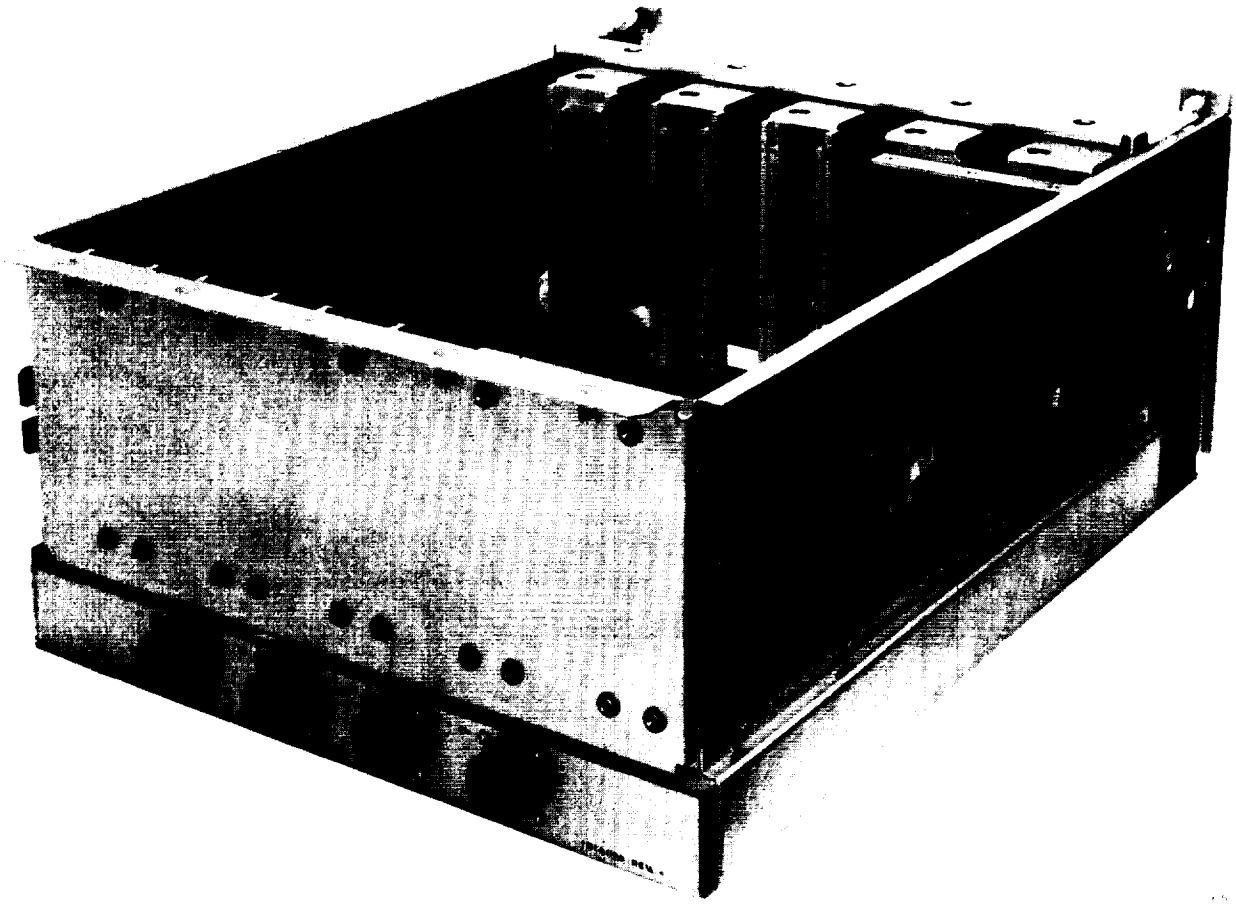

Figure 3-1. Computer Simulator Drawer

Chapter 4

THEORY OF OPERATION

4-1 INTRODUCTION

This chapter contains a discussion of the functional theory of operation of the AGC Simulator. The discussion is carried on at a block-diagram and simplified-logic-diagram level with supporting illustrations depicting waveforms generated in the different circuits. Detailed analysis is given only for circuits unique to the AGC Simulator. Since the primary function of the simulator is to produce drive rate outputs, the discussion is divided into the seven basic circuits required to produce the outputs. Included is a short discussion of the theory of operation of the power and control circuit.

4-2 GENERAL THEORY

The prime function of the AGC Simulator, shown in block-diagram form on figure 4-1, is to produce drive rate outputs identical to those of the Apollo Guidance Computer for the optics-inertial subsystem tests. This is accomplished by generating a clock frequency and by dividing and modifying the clock output to produce the drive rate outputs.

The logic used in the simulator can be divided into seven groups for discussion purposes. The groups are: (1) the clock and scaler, (2) drive rate, (3) reset, (4) PIPA, (5) PSA, (6) external time base, and (7) buffer circuits.

4-2.1 CLOCK AND SCALER. The clock and scaler circuit (figure 4-2) generates the basic timing pulses for the simulator and the G and N system. It consists of a lead-in section, ring counter, and scaler.

4-2.1.1 Lead-In Section. The lead-in section is made up of a highly stable oscillator and binary frequency division circuits. The oscillator has a long-term aging characteristic of ± 4 pp10^7 per week and produces a 2.048-Mc output (± 2 pp 10^8), which is fed through two NOR gates to produce Ωa and Ωb, two 2.048-Mc square wave signals delayed 180 degrees from each other. Next follows the binary frequency division of Ωa and Ωb in two divide-by-two stages. The outputs provided by the second of these two divide-by-two stages are C2, Wa, and Wb.

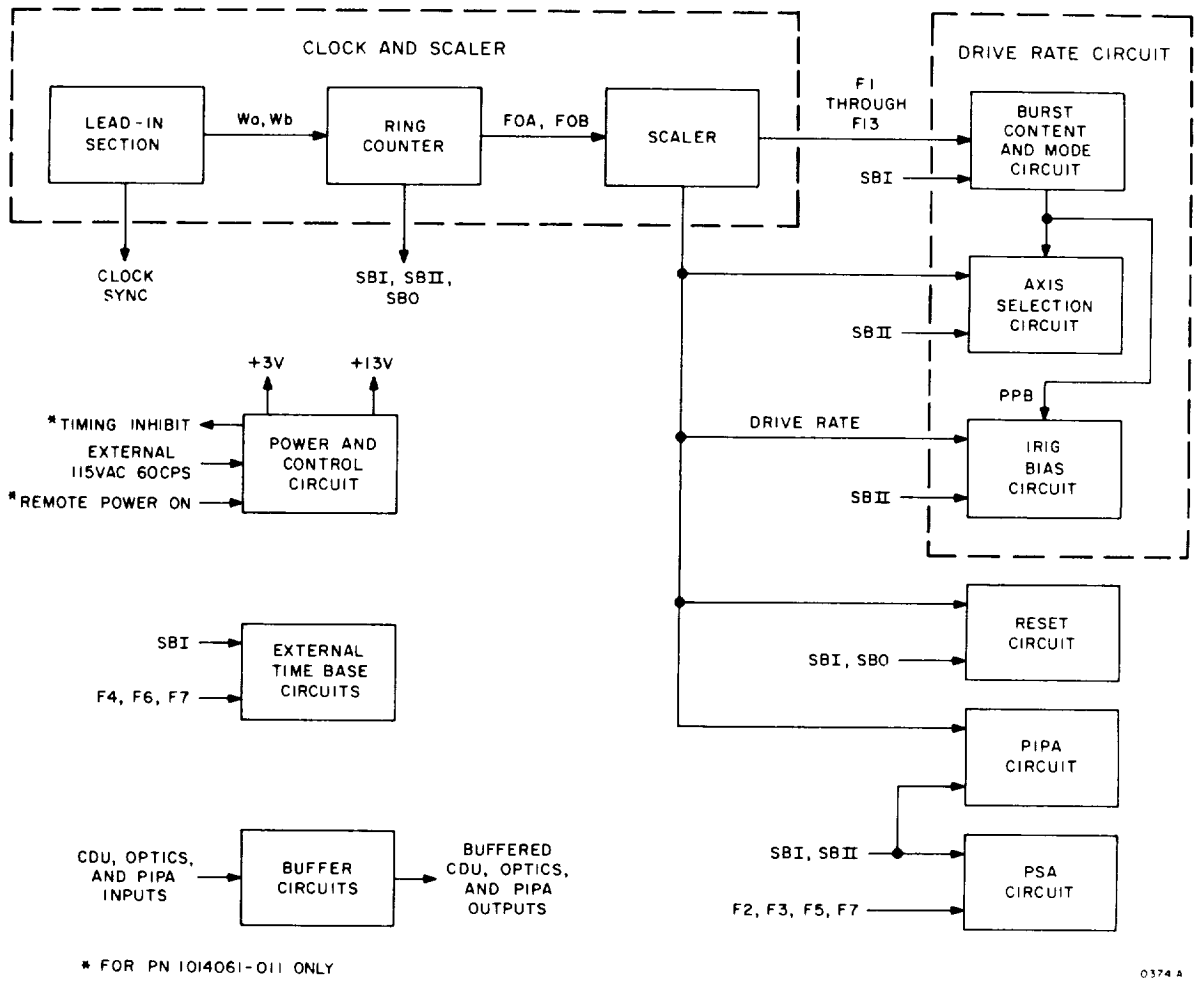

Figure 4-1. AGC Simulator, Functional Block Diagram

Output C2, a 512-kc square wave, is applied to a NOR gate controlled by the TIMING INHIBIT function of switch S3 on the front panel. Setting S3 to INHIBIT forward-biases a steering diode to permit the application of approximately 1 vdc at one input of the NOR gate, which effectively inhibits the transmission of C2 to the output circuit.

Setting S3 to NORMAL removes the fixed voltage from the NOR gate and permits the gate to act as an inverter for C2. The output of the NOR gate, $\overline{C2}$, is coupled to the G and N output circuit through a transformer driver module. $\overline{C2}$ is connected also to J4 and J5 on the front panel and labelled CLOCK SYNC.

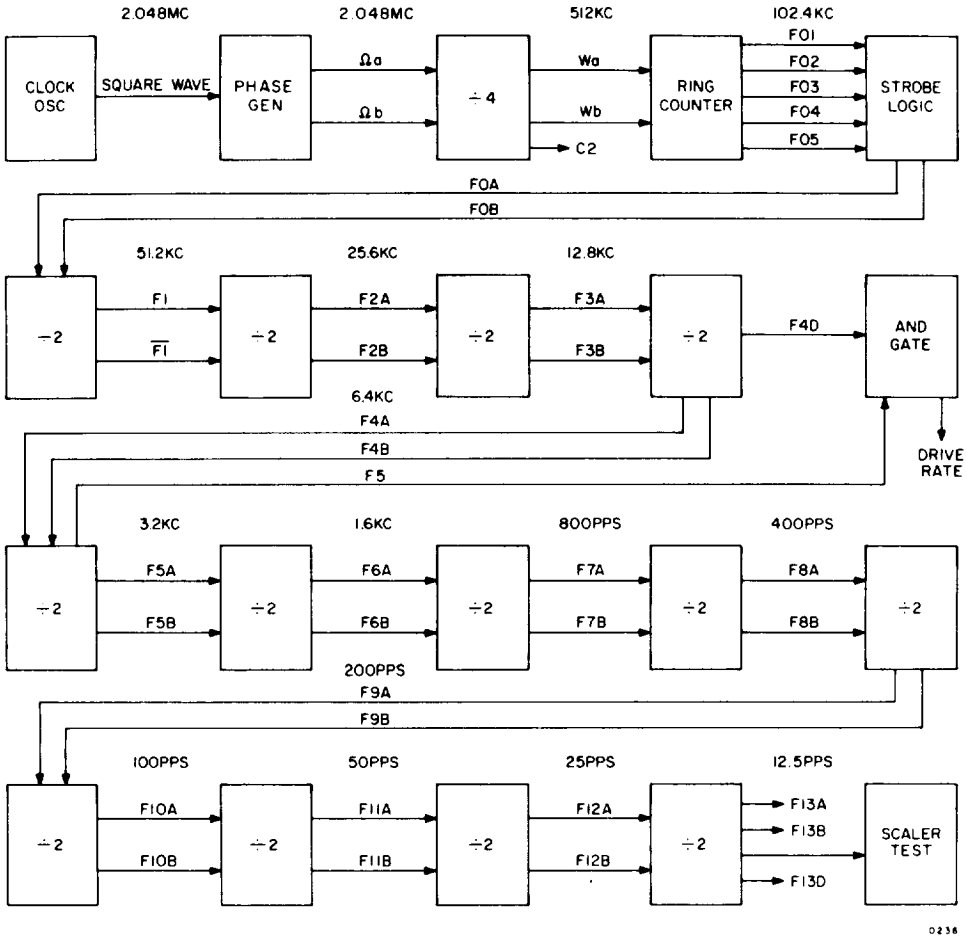

Figure 4-2. Clock and Scaler, Functional Block Diagram

4-2.1.2 Ring Counter. The ring counter (figure 4-3) accepts nonoverlapping ZERO pulse trains at 512 kc (Wa and Wb) from the lead-in section as gating signals. Since the number of flip-flop elements and the desired frequency division are odd numbers (five), each level of gating has both Wa and Wb in it. For example, if the top gate has Wa as its strobing signal, the bottom gate will have Wb applied, and vice versa.

The ring counter generates five phases of 102.4-kc square waves. Three strobe outputs (SBI, SBII, and SB0) and two phases (FOA and FOB) are derived from these square waves. FOA and FOB are used to trigger the succeeding 13 stages of binary division.

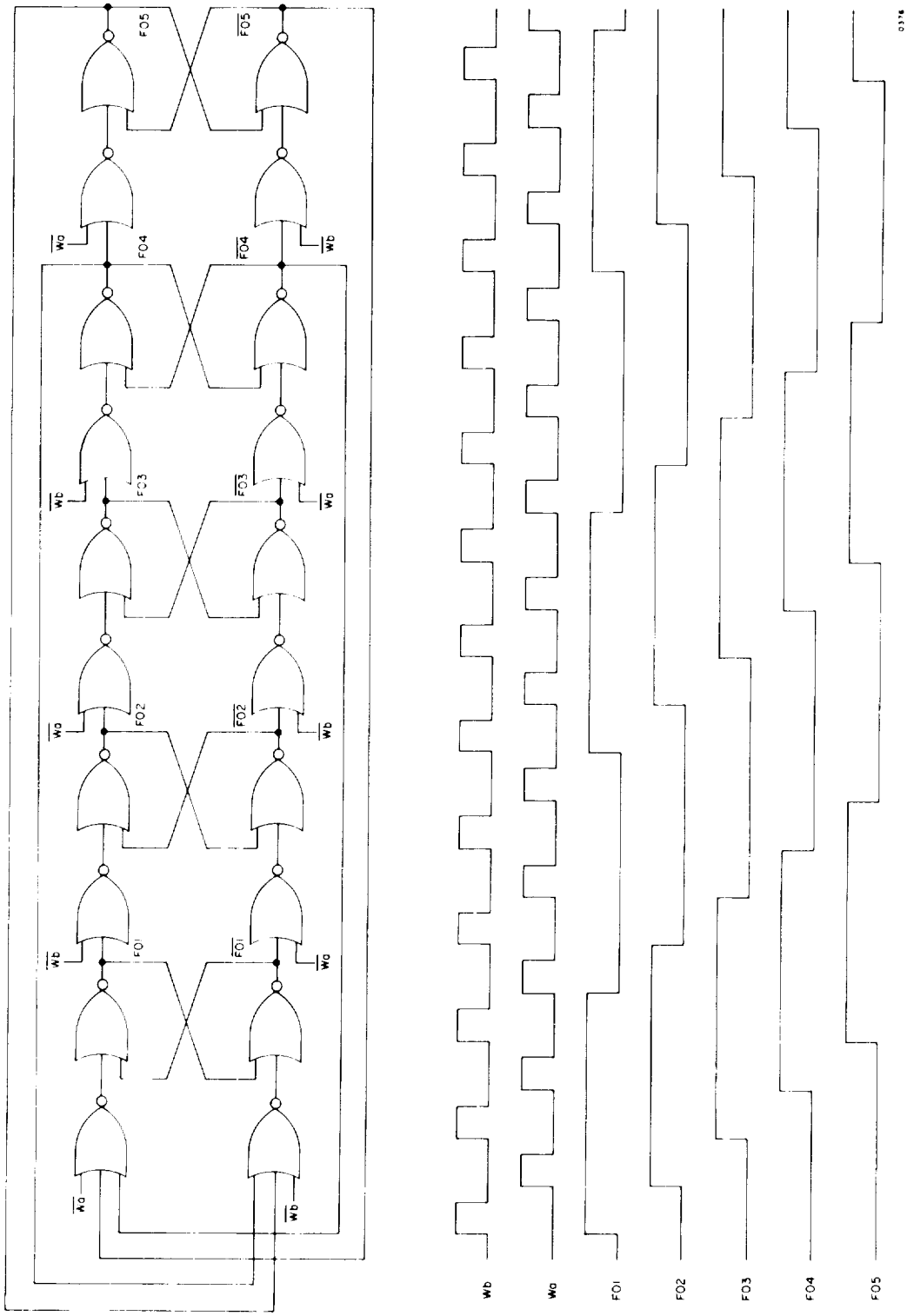

Figure 4-3. Ring Counter, Logic Diagram

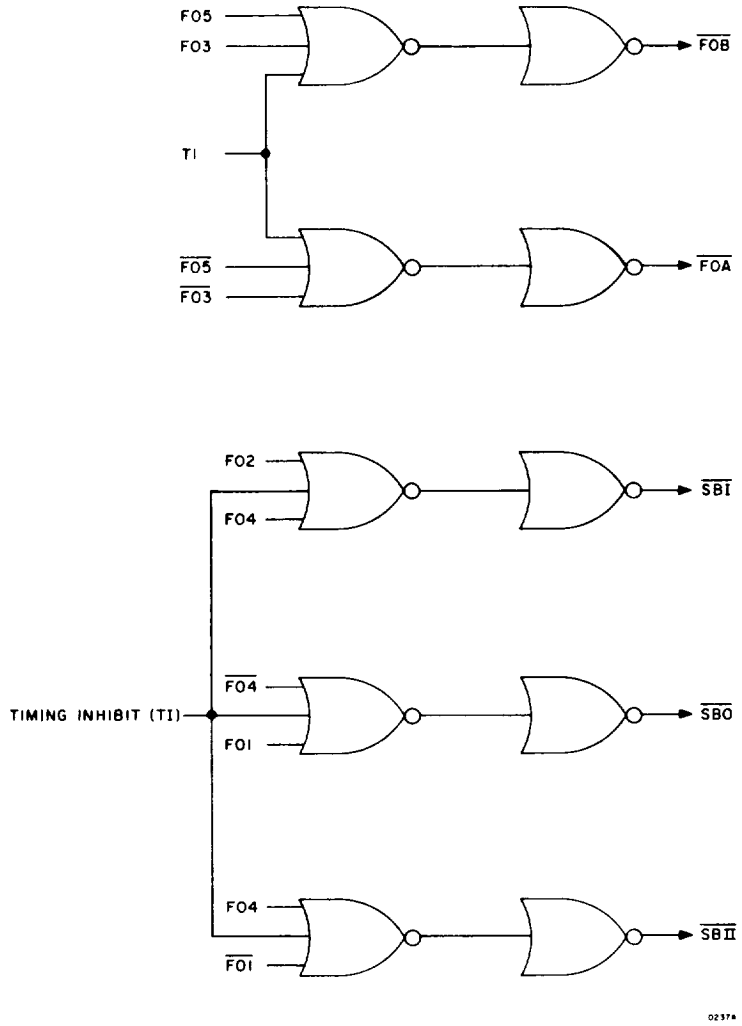

Figure 4-4. Strobe Generator, Logic Diagram

The strobe generator (figure 4-4) combines pairs of ring counter outputs to produce signals SBI, SBII, and SB0, where

$$SBI = \overline{FO2} \cdot \overline{FO4} \cdot \overline{TI}$$

$$SBII = FO1 \cdot \overline{FO4} \cdot \overline{TI}$$

$$SB0 = \overline{FO1} \cdot FO4 \cdot \overline{TI}.$$

The four NOR gates with inputs in parallel provide an increased "fan-out" capability. The four outputs of these gates are identical in time, amplitude,

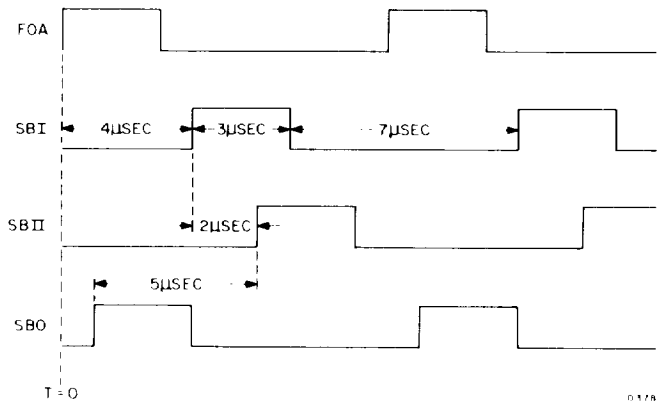

Figure 4-5. Strobe Waveforms

and frequency. The strobe pulses (figure 4-5) are 3 μsec wide at a frequency of 102.4 kc.

4-2.1.3 Scaler. The scaler (figure 4-2) consists of 13 binary counter stages similar to those shown in figure 4-3. The stages are cascaded, so frequency division is successive. The first stage is driven from two strobe-like pulses, $\overline{FOA}$ and $\overline{FOB}$ (figure 4-4) where

$$FOA = FO5 \cdot FO3 \cdot \overline{TI}$$

$$FOB = \overline{FO5} \cdot \overline{FO3} \cdot \overline{TI}.$$

Flip-flop outputs F1 and $\overline{F1}$ are 51.2-kc square waves, 180 degrees out of phase. These outputs are used as timing signals for stage 2, causing the duration of F2A and F2B to be approximately 10 μsec. Stage 2 uses the feed-forward principle to inhibit sneak pulses. These sneak pulses are the result of an untimely coincidence of ZERO's caused by propagation delay of the inverse square wave.

The inversions of F2A and F2B are used to operate stage 3 so that the resultant widths of the 25.6-kc signals, F3A and F3B, are the same as that of F2, or 10 μsec. This process of inversion and insertion is used from stage 3 through stage 12 with the result that all pulses from F2A on down are basically of the same width (10 μsec). (Refer to figure 4-6 for timing diagram.)

A scaler operating indicator circuit is built into the AGC Simulator so

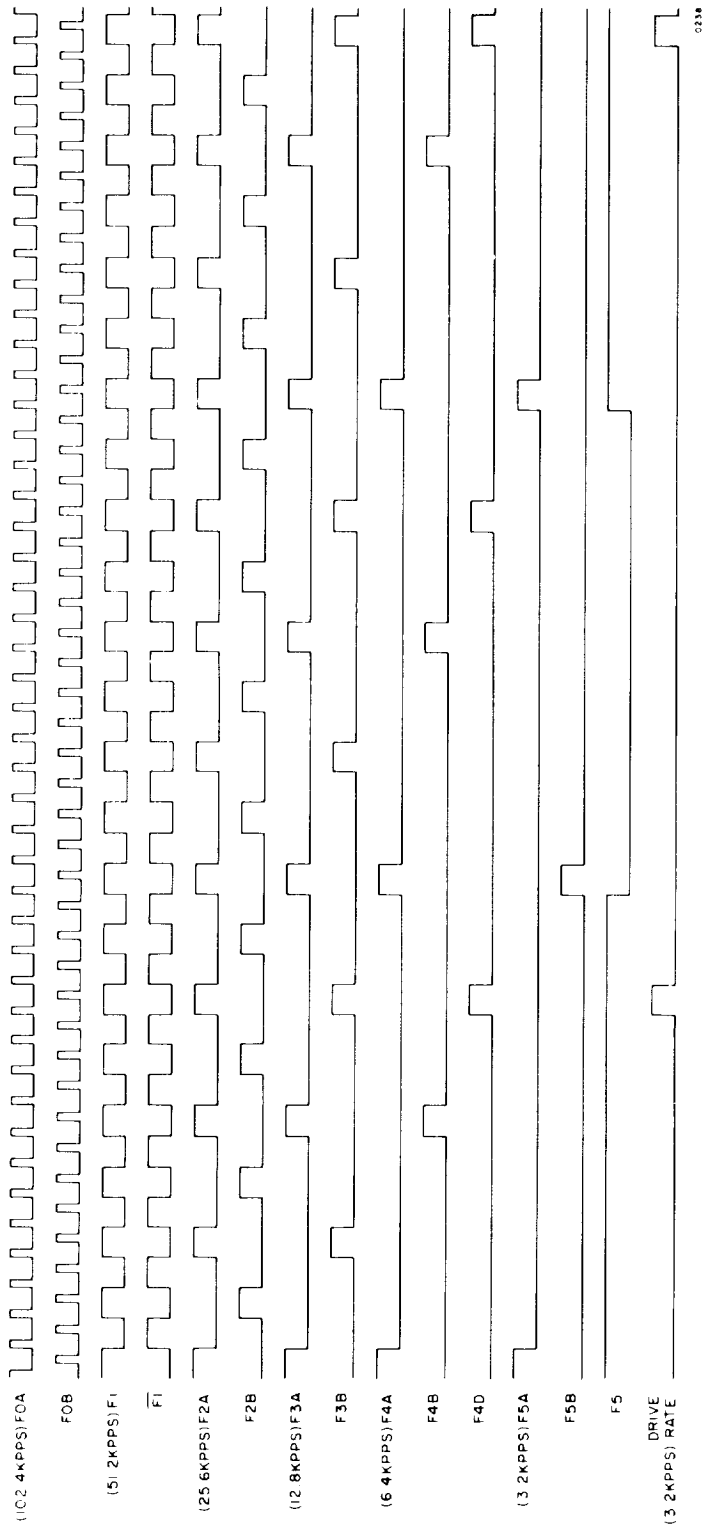

Figure 4-6. Timing Waveforms (Sheet 1 of 2)

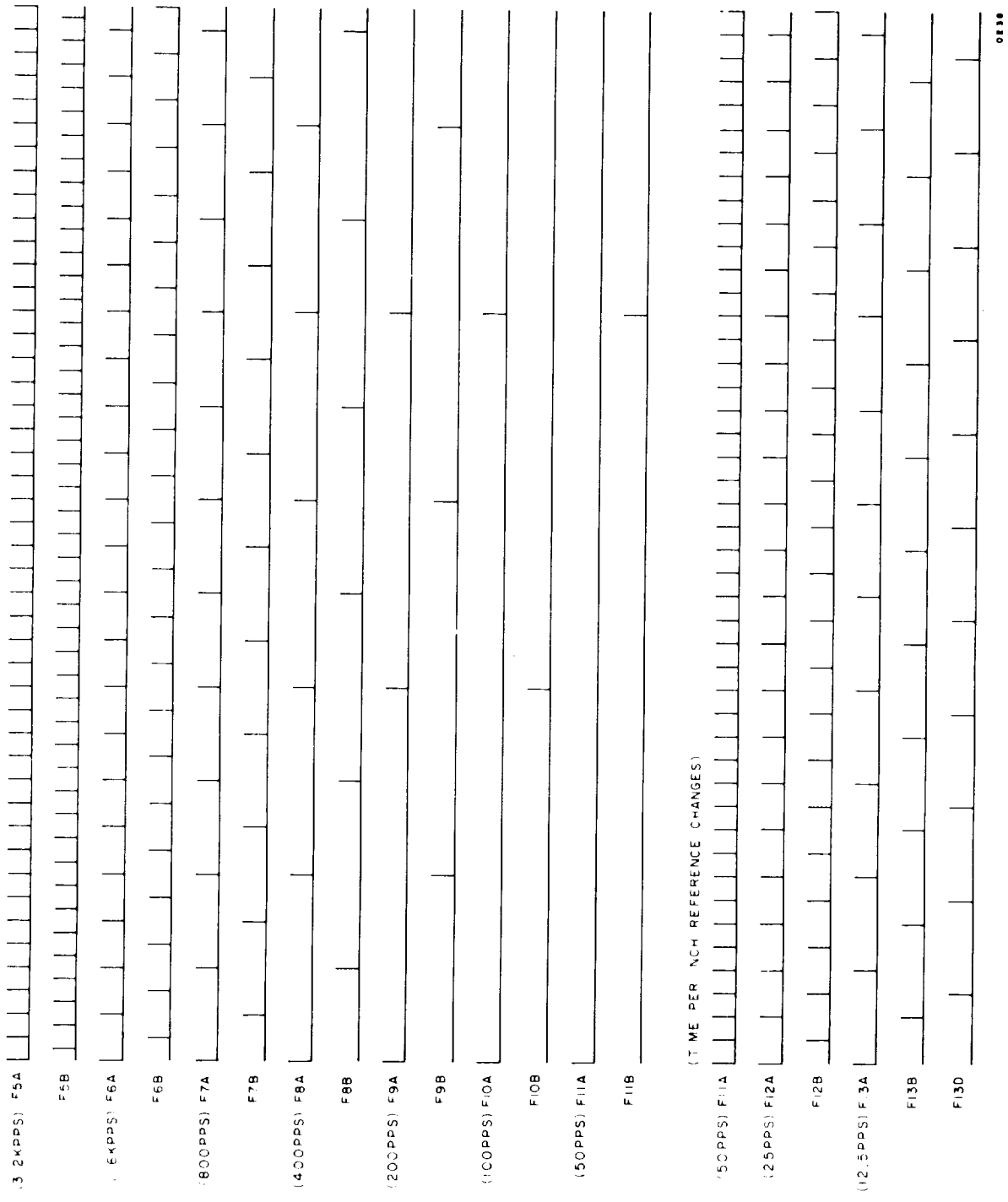

Figure 4-6. Timing Waveforms (Sheet 2 of 2)

that the clock and scaler may be checked quickly for correct operation. This is done by closing SCALER TEST switch S13 on the front panel and observing that the SCALER TEST OPERATING light flashes at a rate of approximately 12 cps. If the light is either steady on or steady off, the clock and scaler circuit is not functioning properly or the TIMING INHIBIT switch is set to INHIBIT.

4-2.2 DRIVE RATE CIRCUIT. The drive rate used throughout the simulator is formed by "anding" two scaler outputs. This signal is then strobed according to the requirements of the desired outputs. The equation is

$$\text{DRIVE RATE} = \text{F4D} \cdot \text{F5} \ .$$

This signal is 3200 pps applied directly and continuously to the PIPA clock, PIPA interrogate, and reset outputs, where it is strobed (by strobe I, II, or 0) before being coupled out. The IMU CDU's, IRIG's, and optic CDU's receive this rate in one of three configurations controlled by the burst content and mode circuit. (See figure 4-7.)

4-2.2.1 Burst Content and Mode Circuit. The burst content and mode circuit (figure 4-8) permits three modes of operation: steady burst, continuous, or single burst. Selection of any of the three modes is accomplished manually with a front panel switch. Continuous drive is achieved by logically "not" selecting either of the burst modes. This permits the drive rate to be strobed and continuously applied to the axis-selecting logic. Selection of the steady-burst mode enables the drive rate to the axis-selecting logic for up to 80 msec maximum once every 240 msec. This function is controlled by the burst content logic.

Single-burst selection inhibits the drive rate until a start pulse is received from the SINGLE BURST START pushbutton switch. The duration of a burst so initiated is also controlled by the burst content logic.

4-2.2.1.1 Burst Content Logic. The principal element of the burst content logic is a flip-flop defined by its input equations as follows:

$$\text{SET} = \text{F13A} \cdot \text{GO SIGNAL} \cdot \text{STROBE I} \cdot \text{PHA} \cdot \text{BURST ENABLE} \cdot (\text{SBST} + \text{STBSEL})$$

$$\text{RESET} = (1\ \text{PPB SEL})(\text{F6B}) + (2\ \text{PPB SEL})(\text{F7B}) + (4\ \text{PPB SEL})(\text{F8B}) + (8\ \text{PPB SEL})(\text{F9B}) + (16\ \text{PPB SEL})(\text{F10B}) + (32\ \text{PPB SEL})(\text{F11B}) + (64\ \text{PPB SEL})(\text{F12B}) + (128\ \text{PPB SEL})(\text{F13B}) + (256\ \text{PPB SEL})\overline{(\text{PHA})}$$

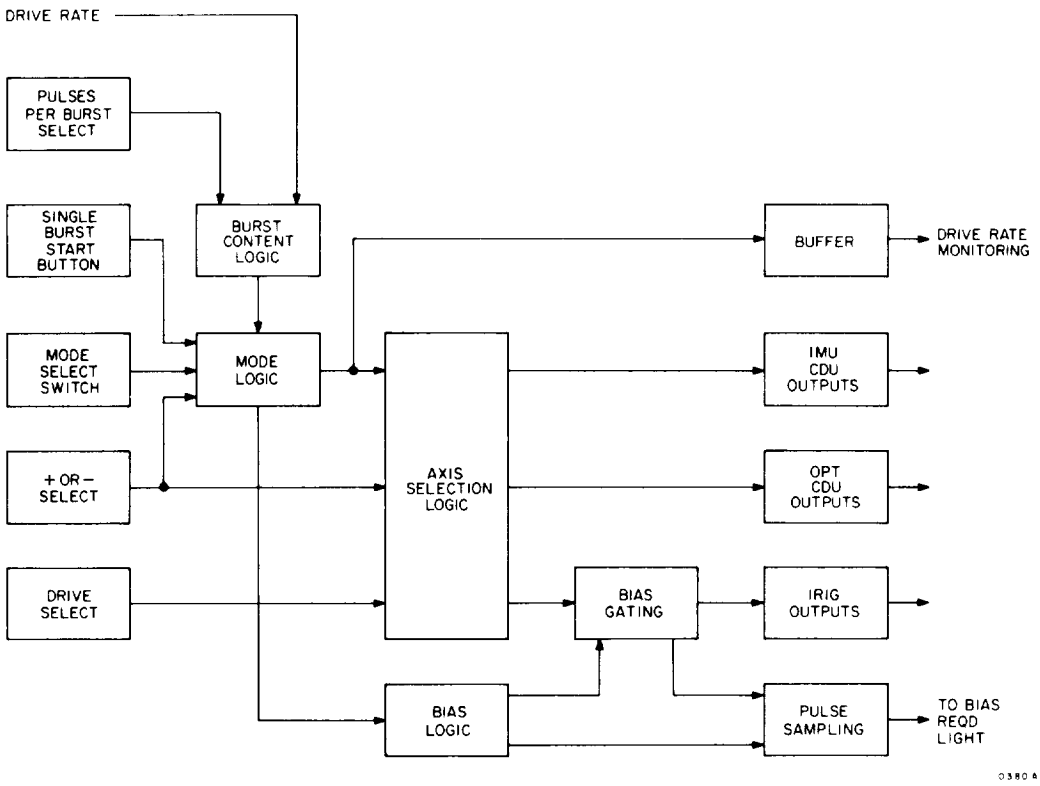

Figure 4-7. Drive Rate Circuit, Functional Block Diagram

This flip-flop controls the duration of the burst, which consequently establishes the pulse content of a given burst or train of bursts. The terms used in the SET and RESET equations are defined as follows:

1. F6B, F7B, F8B, F9B, F10B, F11B, F12B, F13B, and F13A are scaler frequencies having 10-μsec pulse durations.
2. 1 through 256 PPBSEL, GO SIGNAL, and STBSEL are d-c enabling levels selected by front panel controls.
3. PHA and $\overline{\text{PHA}}$ are opposite polarity signals taken from the first stage of a 3-bit shift register. (Refer to drawing 1014063, sheet 5, gate 3B17AC-12.)
4. STROBE I is a continuous train of 3-μsec pulses occurring at a 102.4-kpps rate.
5. BURST ENABLE is the output of a burst control flip-flop. (Refer to drawing 1014063, sheet 5, flip-flop 3A22AC-14/16.)

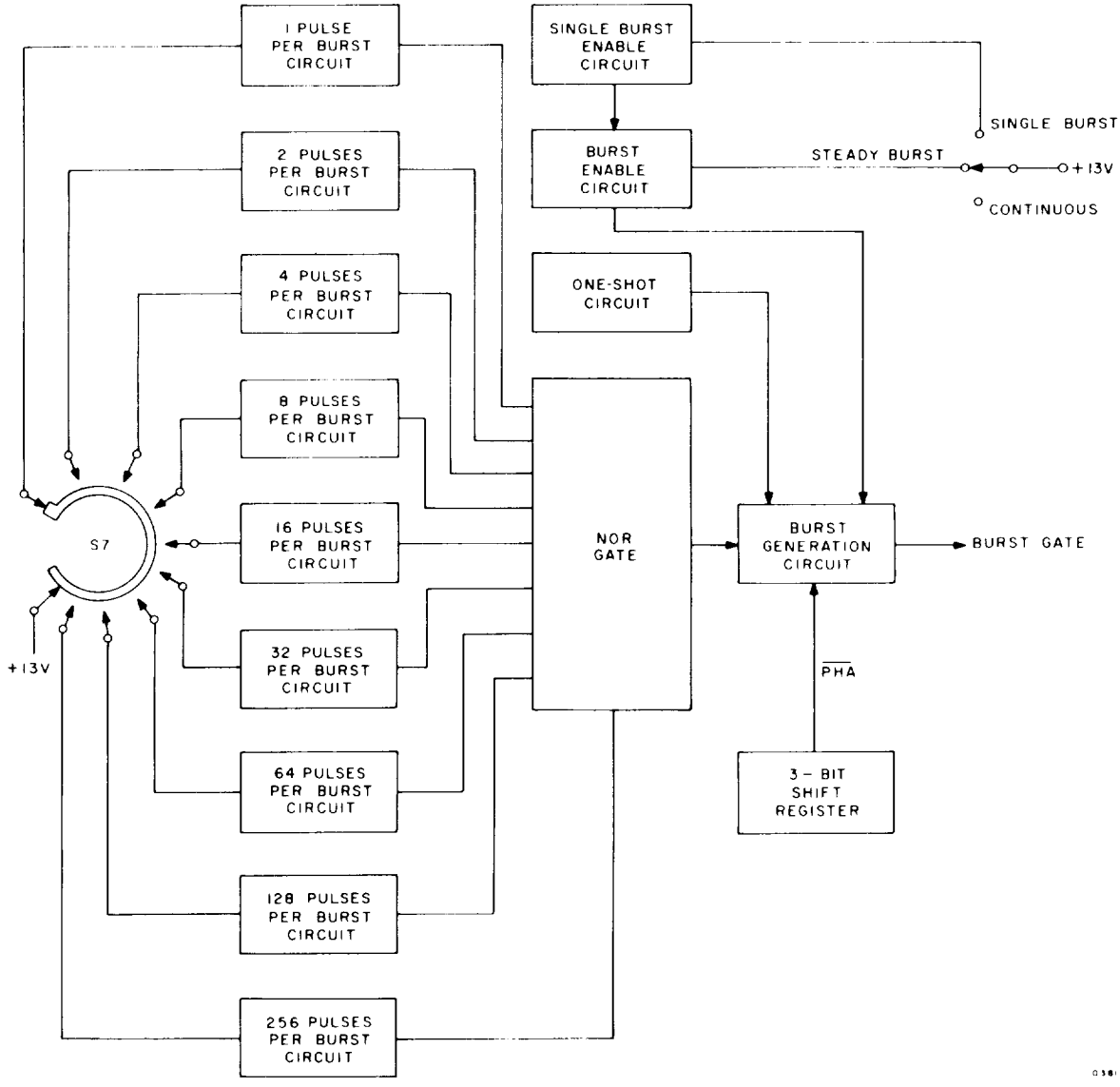

Figure 4-8. Burst Content and Mode Circuit, Functional Block Diagram

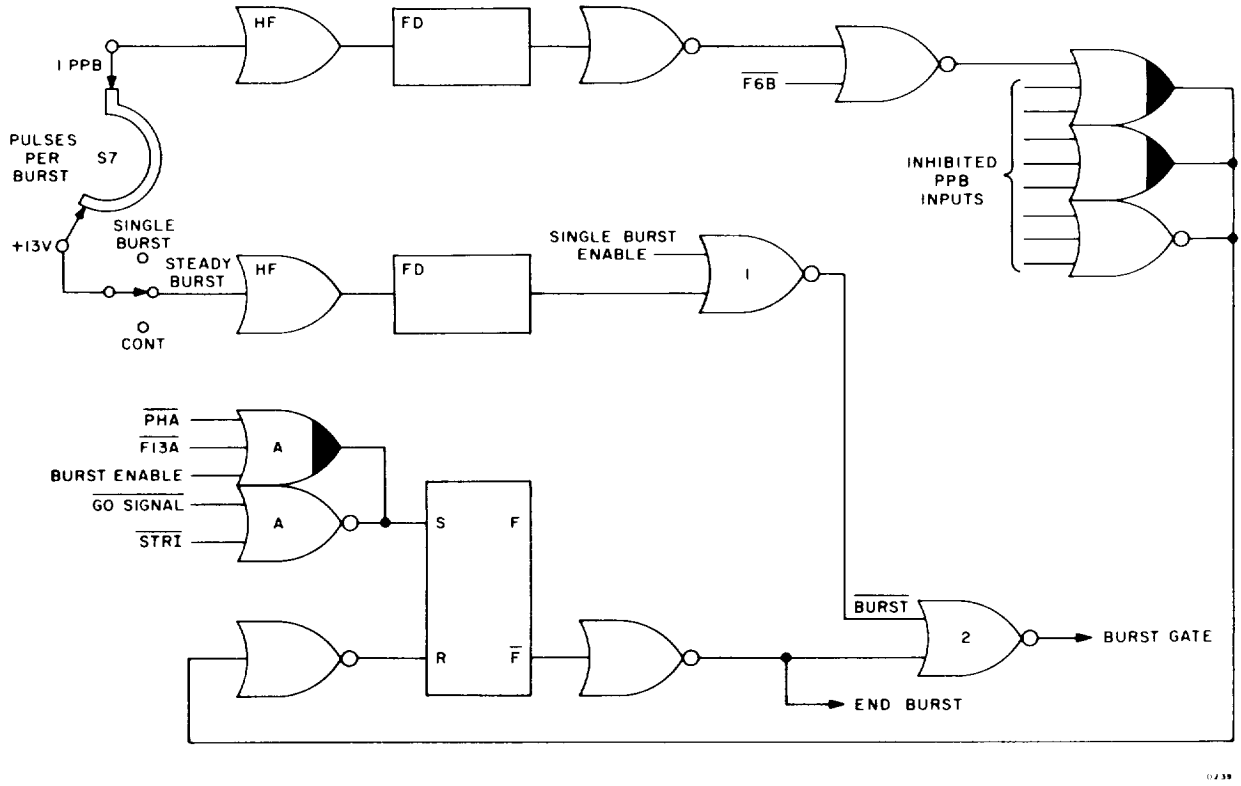

Figure 4-9. Pulses per Burst Selection Circuit, Logic Diagram

6. SBST is a single pulse generated by a one-shot pushbutton switch.
7. GO SIGNAL is a d-c enabling level selected by the ± POLARITY front panel control.

Figure 4-9 is a simplified logic diagram of that part of the burst content logic used during steady burst operation. The 1 PPB position was chosen for discussion. Operation of the circuit is as follows.

Plus 13 vdc is applied to a diode-resistor network with PULSES/BURST switch S7 in the 1 PPB position. The diode acts as a passive OR gate and is used for isolation. The resistor is a current limiter which provides approximately 1 volt to the input of the NOR gate. The presence of a ONE at the input of the NOR gate enables the following NOR gate. All other NOR gates prior to the increased-fan-in NOR gate are inhibited as a result of the absence of the enable level. The NOR output is then F6B.

$\overline{F6B}$ appears at the input to the NOR gate at the reset input of the flip-flop. $\overline{PHA}$, $\overline{F13A}$, $\overline{GO\ SIGNAL}$, SBI, and BURST ENABLE appear at the NOR gate set input. $\overline{PHA}$ has the longest duration as a pulse, an 80-msec ZERO period and a 160-msec ONE period. $\overline{F13A}$ is a 10-μsec ZERO occurring 12.5 times per second. The $\overline{GO\ SIGNAL}$ is a logic ZERO when either + or - is selected. It is a logic ONE when neither + nor - is selected. SBI is a series of 3-μsec ZERO's occurring every 10 μsec. BURST ENABLE is the reset output of a burst enable and duration control flip-flop (not shown).

The increased-fan-in NOR gate (A) at the set input of the flip-flop provides an AND function. When the four inputs are in ZERO coincidence, the flip-flop is set, and a ZERO is present at the $\overline{F}$ output. This occurs approximately four times per second regardless of the position of PULSES/BURST switch S7.

Since the train of pulses present at the reset input of the flip-flop are B pulses and are not in coincidence with the A pulses of the set input, F6B causes the flip-flop to reset approximately 312 μsec after the set.

Another enable level is furnished by setting the mode switch to STEADY BURST. This applies +13 vdc to a diode-resistor network which provides a ONE to NOR gate 1. The output of NOR gate 1, a ZERO, enables NOR gate 2, which allows the burst duration determined by the flip-flop to be applied to the DRIVE RATE strobing gate.

Operation in the other positions of S7 is identical to the one discussed except that a different B scaler frequency is used for the reset gate of the flip-flop so that an enable burst gate that doubles in duration for each advance of S7 is produced.

Single-burst operation is similar to that of continuous burst in every way but one. No burst gate is present at the output of NOR gate 2 until a single-shot switch is depressed on the front panel. The switch contains a one-shot generator that produces an approximate 12-volt output that is reduced to approximately 1 volt through a resistor module, which, in turn, triggers a flip-flop to set the burst gate flip-flop (figure 4-9). From this point, operation is identical to the steady-burst mode.

4-2.2.1.2 Shift Register and Comparator. A 3-bit shift register (refer to drawing number 1014063, sheet 5) triggered by $\overline{F13A}$ and $\overline{F13B}$ generates three outputs: PHA, PHB, and PHC. PHA is the only one of the three used in the simulator. PHB and PHC along with PHA are used within the shift register circuit to maintain operation in the desired mode.

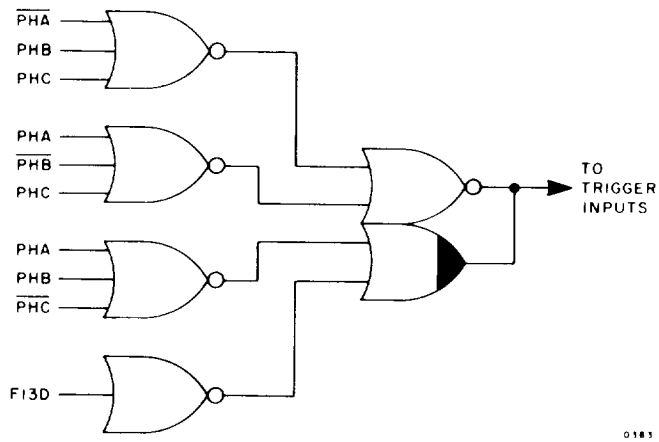

Figure 4-10. 3-Bit Shift Register Comparator Circuit, Logic Diagram

Since a 3-bit register can assume eight different modes, restrictions must be imposed to provide the desired three modes. This is accomplished with the comparator circuit shown on figure 4-10. As long as the inputs to the NOR gates are as shown, the input to the trigger input circuit is a ZERO. However, the presence of a combination other than 100, 010, or 001 presents all ZERO's at the input of the increased-fan-in NOR gate. This applies a ONE to the trigger circuit of the shift register, which resets the register to 100. The insertion of F13D into the circuit permits the completion of a combination; thus, the comparator cannot act on partial information.

4-2.2.2 Axis-Selection Logic. Once the drive rate mode has been selected, it is necessary to direct it to its proper destination. This is done by selecting the proper axis and polarity on the front panel.

There are sixteen combinations of the DRIVE SELECT and POLARITY switches. A typical example is +OG CDU. When both + and OG CDU are selected, the output gate of that particular axis is enabled and allows the strobed drive rate to be coupled to the external electronics. A seventeenth output, PROGRAMMED SIGNAL, monitors the drive rate continually, regardless of which axis is selected.

Since the circuits for axis selection are similar, only the +OG CDU selection circuit is discussed. A simplified logic diagram of the +OG CDU selection circuit is shown on figure 4-11. Setting DRIVE SELECT switch S11

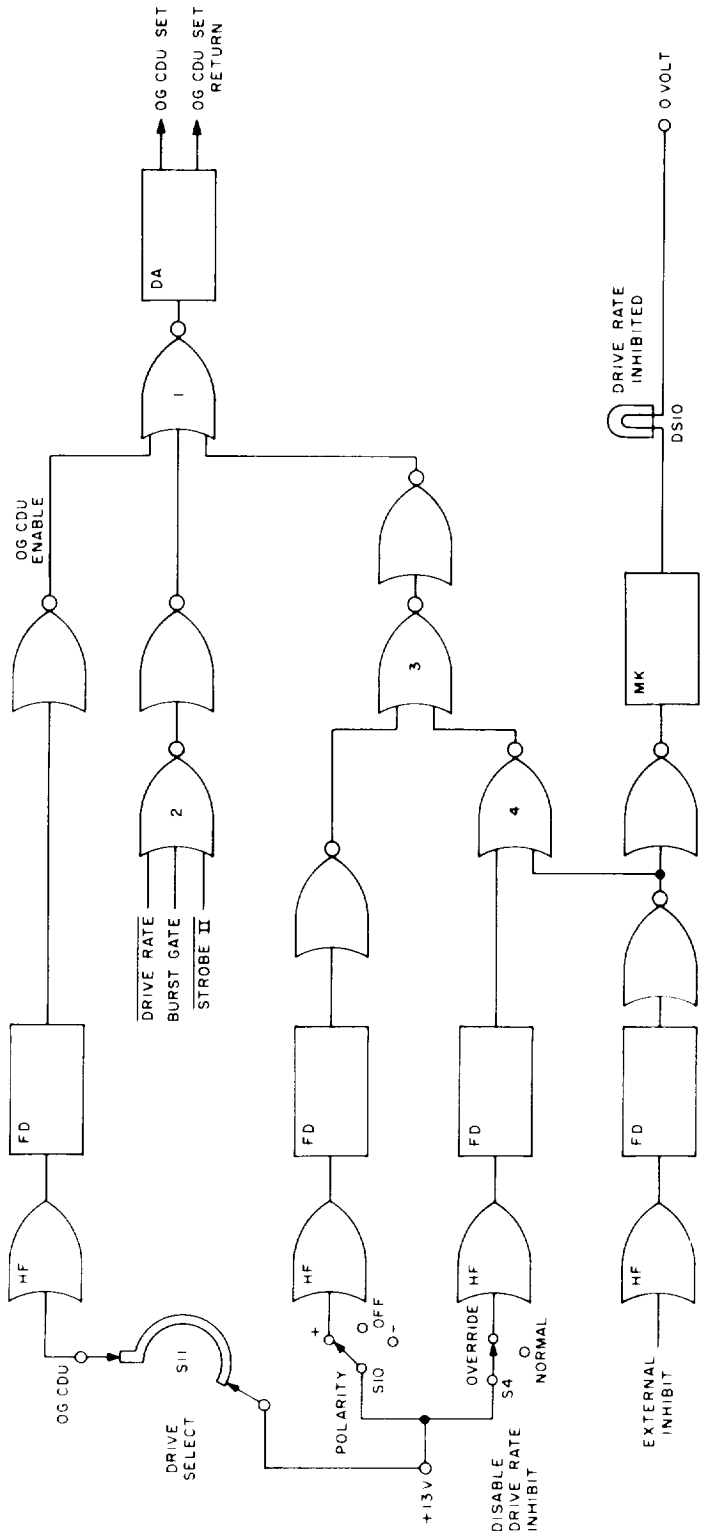

Figure 4-11. +OG CDU Selection Circuit, Logic Diagram

to OG CDU provides a path for +13 vdc to forward-bias a passive diode gate. This voltage is reduced to approximately 1 vdc by a resistor module, which provides a logic ONE input to a NOR gate. The output of the NOR gate is a ZERO and is present at the input of gate 1.

A second input to gate 1 is provided by gate 2 in conjunction with a NOR gate. The input to gate 2 is $\overline{\text{DRIVE RATE}}$, BURST GATE, and $\overline{\text{STROBE II}}$.

Gate 2 is one of the standard NOR gates used as an AND gate. It performs the AND function by providing the desired output only during a coincidence of ZERO's at the input. This coincidence of ZERO's provides a ONE output, which is inverted and applied to gate 1.

The third input to gate 1 is derived from gate 3 and associated logic. The state of gate 3 is determined by POLARITY switch S10, DISABLE DRIVE RATE INHIBIT switch S4, and the external inhibit signal.

When switch S10 is set to the + position, +13 vdc are applied to the same type of circuit that is used in conjunction with DRIVE SELECT switch S11. The result is that a ZERO is present at one of the inputs to gate 3.

The other input to gate 3 is controlled by DISABLE DRIVE RATE INHIBIT switch S4. A ONE is applied to the input of gate 4 with S4 in the OVERRIDE position, as shown on figure 4-11. The external inhibit command is present at the input of gate 4 as a ZERO. Since a ONE is already present at the input of gate 4 (provided by S4), the external drive rate inhibit command is effectively blocked.

A DRIVE RATE INHIBITED indicator lamp is provided to inform the operator that a drive rate inhibit command is being applied to gate 4 from the external electronics. A driver module, preceded by a NOR gate, amplifies the inhibit command to a current level adequate to cause the lamp to glow.

With a coincidence of ZERO's present at the input of gate 3, a simultaneous coincidence of ZERO's occurs at the input of gate 1. Two of the inputs at gate 1 are enable levels. The required commands in the form of "n" strobed pulses of drive rate per burst (controlled by PULSES/BURST switch S7) are then applied to the input of a transformer driver module for impedance matching, isolation, and amplification to the external electronics.

One other circuit for discussion in the area of axis-selection logic is the programmed signal circuit (figure 4-12). This circuit is used to monitor the drive rate continually, regardless of which axis is selected. (This is true

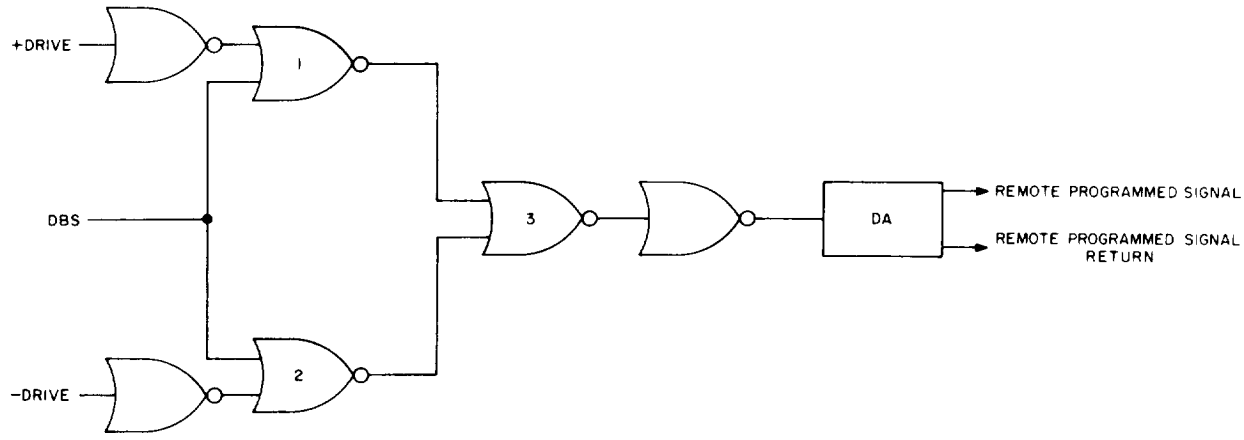

Figure 4-12. Programmed Signal Circuit, Logic Diagram

only when the POLARITY switch is not set to OFF.)

Assume that the POLARITY switch is set to +. This applies an enable signal (a ZERO) to gate 1 through its associated inverter. (The routing of DBS through gate 2 is inhibited by the presence of a ONE at the input gate 2.) This permits the passage of DBS to gate 3.

NOTE: DBS = $\overline{\text{DRIVE RATE}}$ + BURST GATE + $\overline{\text{STROBE II}}$

Gate 3 acts as an inverter because of the steady ZERO level present from gate 2.

4-2.2.3 IRIG Bias Circuit. The IRIG bias circuit (figure 4-13) is used to "normalize" the IRIG's when they have been driven on their negative axes or when the AGC Simulator is initially turned on. This is done by simultaneously supplying two pulses on all three negative axes and then two on all three positive axes. (Since the operation of the IRIG circuits is identical, only the +X IRIG circuit is discussed.)

To initiate this action, flip-flop 4 is set by a one-shot pulse from the BIAS pushbutton switch on the front panel. This assumes that gate 7 has a ZERO for an output, BIAS PERMISS.

The BIAS PERMISS circuit consists of gates 5, 6, and 7 and their associated NOR gates. In the continuous or steady-burst modes the $\overline{\text{GO SIGNAL}}$ and

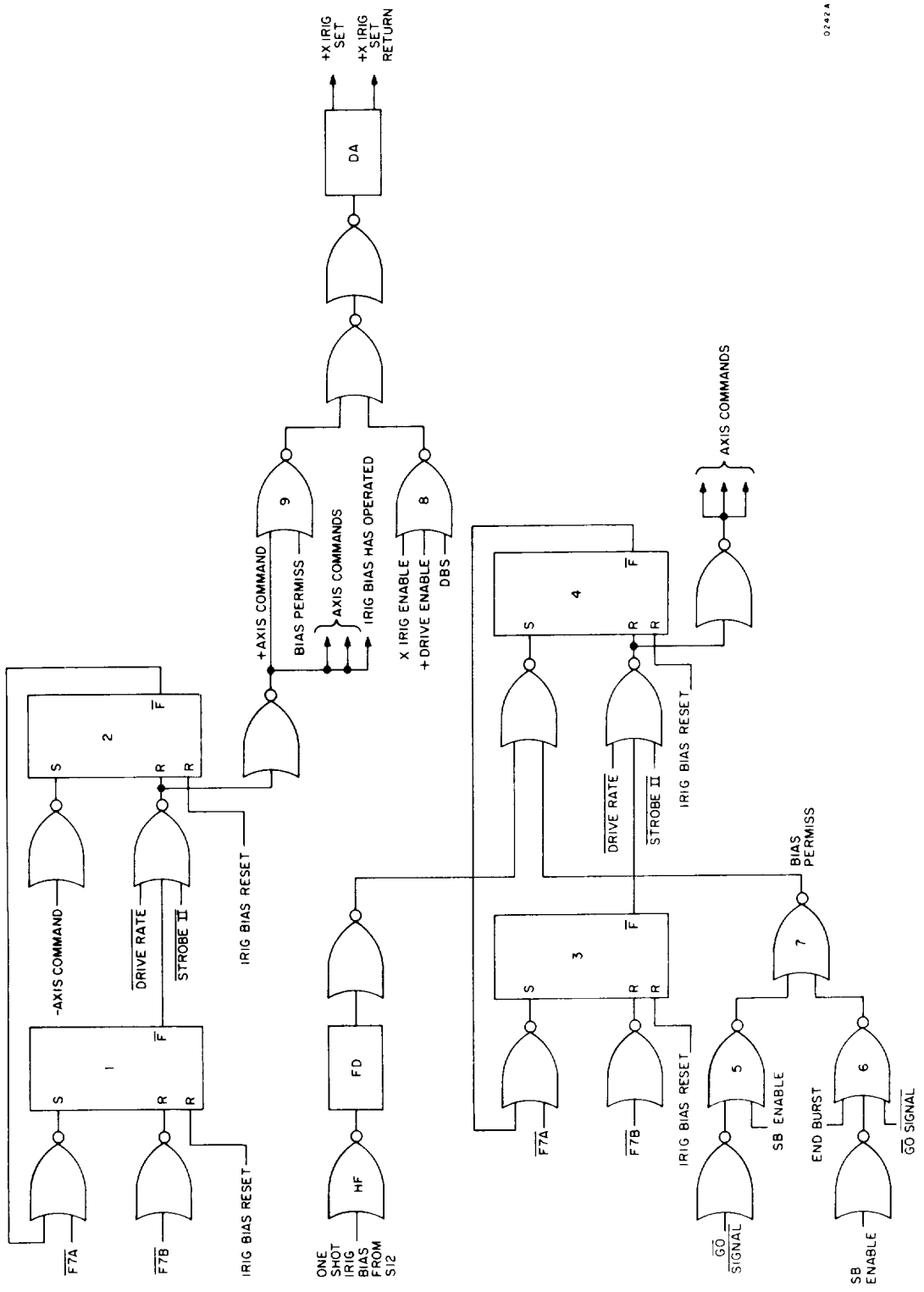

Figure 4-13. +X IRIG Bias Circuit, Logic Diagram

the SINGLE BURST ENABLE are ZERO's; therefore, the output of gate 7 is a ZERO, which always enables the set gate of flip-flop 4. In the single-burst mode, however, SINGLE BURST ENABLE is a ONE and the GO SIGNAL, a ZERO. Therefore, the set gate of flip-flop 4 is enabled only when the END BURST is a ZERO.

Resuming the discussion at the point where flip-flop 4 is set, $\overline{F}$ output is a ZERO, and a ZERO is present also at the input to the set gate for flip-flop 3. When $\overline{F7A}$ goes to a ZERO for 10 μsec (normal pulse width for scaler outputs), flip-flop 3 is set. The $\overline{F}$ output is then a ZERO and is present at the input of the reset gate for flip-flop 4. This enables the passage of two drive rate pulses (the first of which resets flip-flop 4) through the gate to a NOR gate for distribution to the minus IRIG logic bias circuits. The drive rate pulses are strobed by $\overline{STR\ II}$ to a 3-μsec pulse width to compensate for transit time within the AGC Simulator.

Since flip-flop 4 is now reset, a ONE is present at the $\overline{F}$ output of flip-flop 4 and the input of the set gate for flip-flop 3. This inhibits $\overline{F7A}$ from having any further effect on the circuit.

After a period of time, $\overline{F7B}$ resets flip-flop 3 which causes a ONE at $\overline{F}$. This ONE inhibits the reset gate of flip-flop 4 and thus limits the minus axis command to two pulses of drive rate.

The first pulse of minus axis command from the reset gate of flip-flop 4 sets flip-flop 2 also. This causes flip-flops 1 and 2 to function exactly as flip-flops 3 and 4. The result is that two pulses of + AXIS COMMAND are generated and applied to gate 9. At first glance it would seem that there is a conflict. A conflict between the AXIS COMMAND pulses and the DBS from gate 8 never occurs, since the axis command generation circuit is inhibited during burst operation by END BURST at the input of gate 6.

The generation of the AXIS COMMAND pulses is neither random nor automatic. The IRIG BIAS switch is depressed by the operator when a BIAS REQD indicator lamp glows on the front panel. The bias check circuit is shown on figure 4-14.

Four separate signals cause the BIAS REQD indicator lamp to glow. IRIG BIAS RESET is a 3-volt, 5-msec pulse that occurs at turn-on. It is generated by relay K2 in the d-c power supply section. The pulse (a ONE) sets the flip-flop shown on figure 4-14. With the flip-flop set, the F output is a ONE, which, in turn, permits the BIAS REQD indicator to glow. The indicator glows until

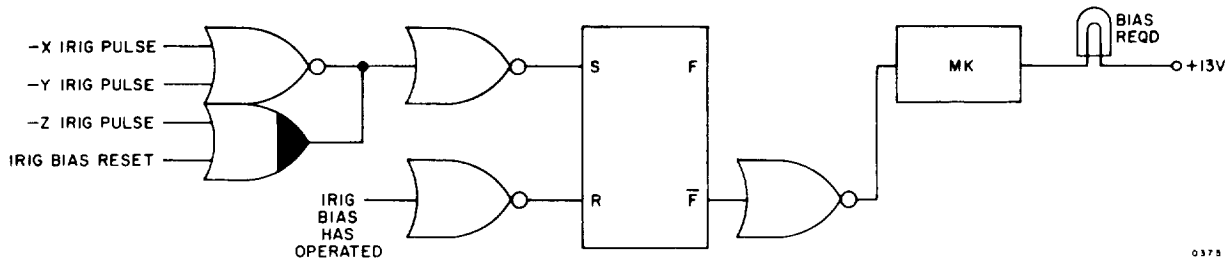

Figure 4-14. Bias Check Circuit, Logic Diagram

the operator depresses the IRIG BIAS pushbutton switch to initiate the generation of axis commands. One + AXIS COMMAND pulse from the IRIG bias circuit resets the flip-flop, and the indicator is extinguished.

The presence of pulses on any one of the three minus IRIG axes produces a ONE at the input of the increased fan-in NOR gate of figure 4-14. The minus IRIG axis pulses are all derived in the same manner and operate the bias check circuit in the same way as the IRIG BIAS RESET pulse.

4-2.3 RESET CIRCUIT. The reset pulses applied to the IMU CDU's and optics CDU's are identical. They are continuous pulses of the drive rate frequency strobed with STROBE I. (See figure 4-15.) Any reset pulse occurs approximately 310 μsec after a preceding set pulse with this logic. The equation describing this is

$$\text{CDU RESETS} = \text{F4D} \cdot \text{F5} \cdot \text{STROBE I} \ .$$

The IRIG reset is of the same frequency but requires STROBE 0; thus, an IRIG reset pulse occurs approximately 307 μsec after the preceding set pulse. This signal may be inhibited by the use of a front panel switch. The inhibit function is indicated by a front panel indicator lamp. The equation for this signal is

$$\text{IRIG RESET} = \text{F4D} \cdot \text{F5} \cdot \text{STROBE 0} \cdot \overline{\text{RST INH}} \ .$$

4-2.4. PIPA CIRCUIT. The PIPA circuit (figure 4-16) generates two outputs: PIPA INTERROGATE, and PIPA CLOCK. PIPA CLOCK is a direct and continuous output. The equations are as follows:

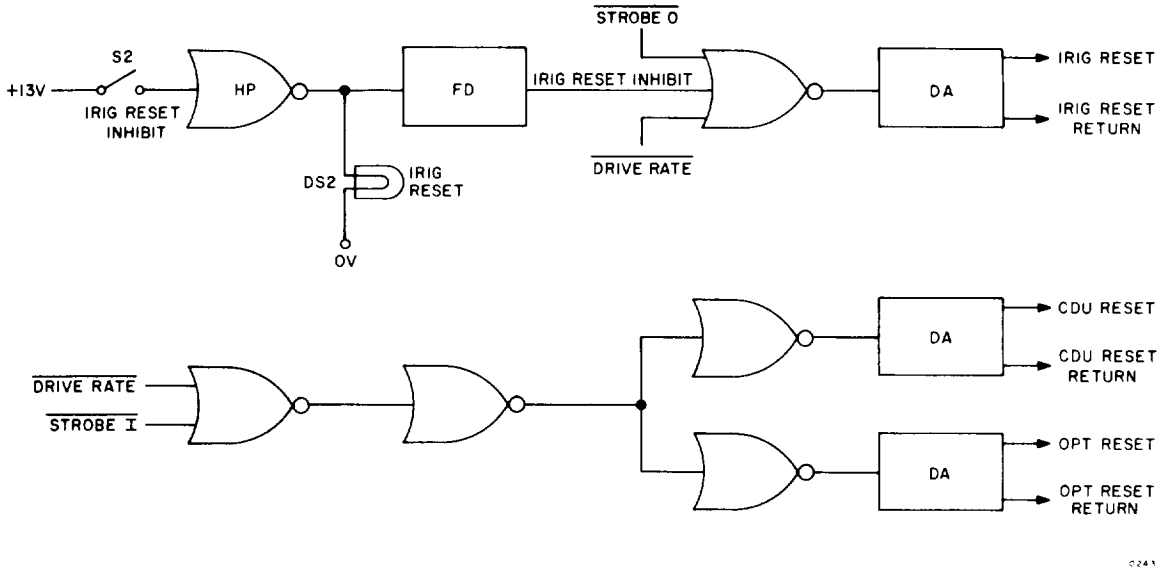

Figure 4-15. Reset Circuit, Logic Diagram

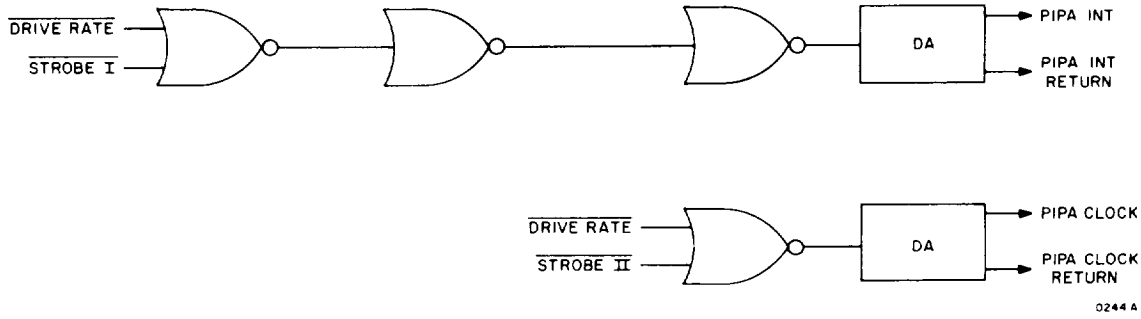

Figure 4-16. PIPA Circuit, Logic Diagram

$$\text{PIPA CLOCK} = \text{F4D} \cdot \text{F5} \cdot \text{STROBE II}$$

$$\text{PIPA INTERROGATE} = \text{F4D} \cdot \text{F5} \cdot \text{STROBE I.}$$

4-2.5 PSA CIRCUIT. The PSA circuit (figure 4-17) provides strobing of the

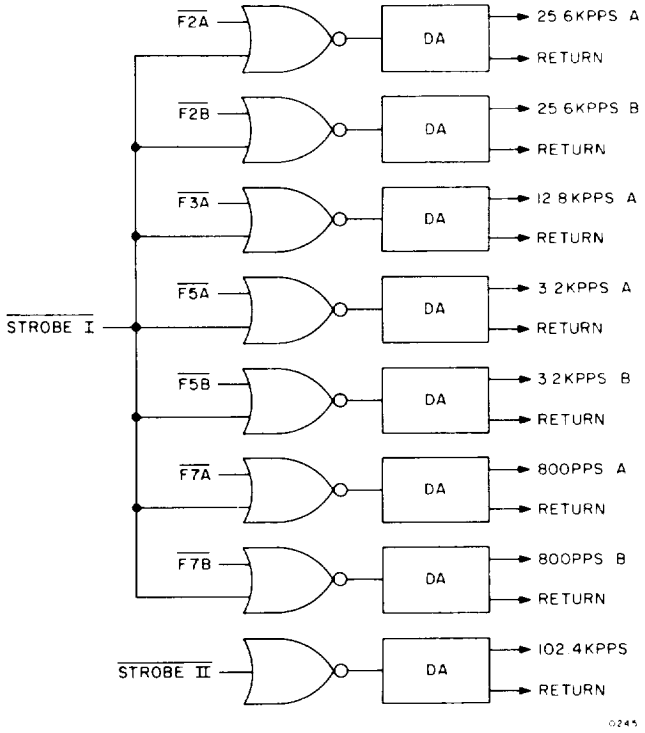

Figure 4-17. PSA Circuit, Logic Diagram

scaler rates going to the PSA electronics. The outputs are continuous and are defined by the following equations:

$$25.6 \text{ kpps A} = F2A \cdot SB\ I$$

$$25.6 \text{ kpps B} = F2B \cdot SB\ I$$

$$12.8 \text{ kpps A} = F3A \cdot SB\ I$$

$$3.2 \text{ kpps A} = F5A \cdot SB\ I$$

$$3.2 \text{ kpps B} = F5B \cdot SB\ I$$

$$800 \text{ pps A} = F7A \cdot SB\ I$$

$$800 \text{ pps B} = F7B \cdot SB\ I$$

$$102.4 \text{ kpps} = SB\ II\ .$$

4-2.6 EXTERNAL TIME BASES. Three external time base outputs have

direct, nonprogrammable logic circuits associated with them. The equations that describe these outputs are:

$$\text{EXT TB 1} = \text{F4D} \cdot \text{F5} \cdot \text{SBI} \qquad (3.2 \text{ kpps})$$

$$\text{EXT TB 2} = \text{F6B} \cdot \text{SBI} \qquad (1.6 \text{ kpps})$$

$$\text{EXT TB 3} = \text{F7B} \cdot \text{SBI} \qquad (800 \text{ pps})$$

4-2.7 BUFFER CIRCUITS. The G and N system provides several inputs to the AGC Simulator. These are the inputs normally applied to the AGC and require some operation. Since the AGC Simulator is incapable of performing any operations on these inputs and the inputs have to be routed through the simulator to the subsystem check-out equipment, buffer circuits are furnished to route these inputs. The buffers are an interface coupling circuit into a transformer driver and provide loading for the inputs as well as isolation.

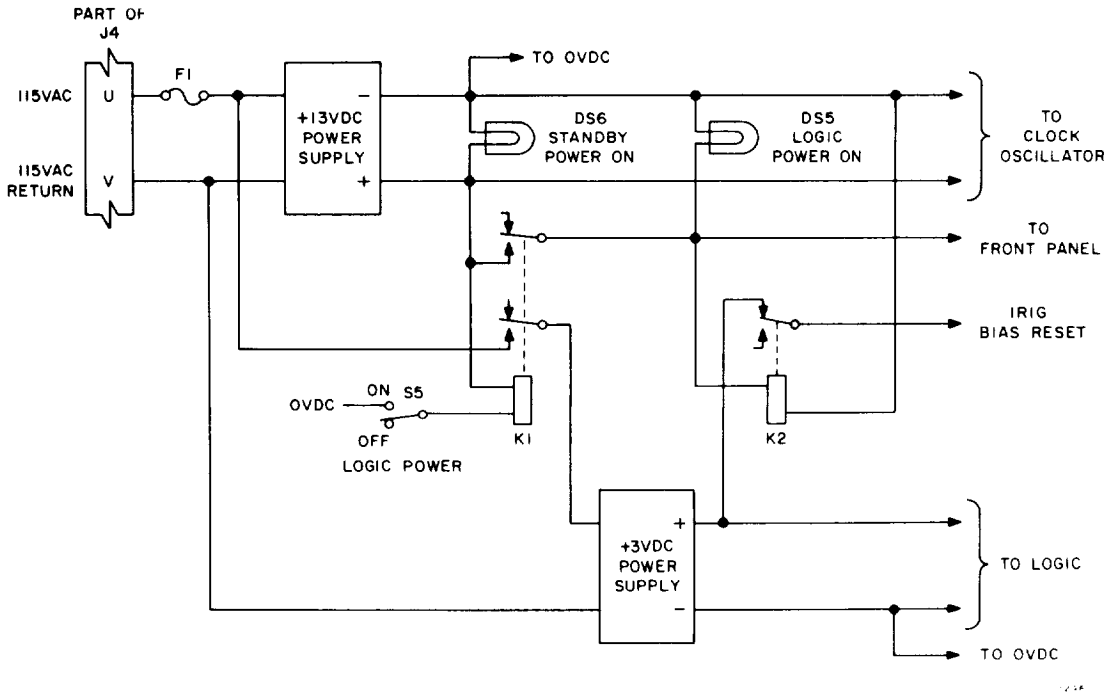

Figure 4-18. Power and Control Circuit for Part Number 1014061-000, Simplified Schematic Diagram

4-2.8 POWER AND CONTROL CIRCUIT. The power and control circuit for part number 1014061-000, (figure 4-18) supplies the two voltages required by the AGC Simulator for operation. These voltages are +3 and +13 vdc.

The clock oscillator remains energized regardless of the positions of any of the front panel switches as long as 115 vac is available to the input of the +13-vdc power supply. STANDBY POWER ON indicator lamp DS6 glows to indicate the presence of +13-vdc at the input to the oscillator.

LOGIC POWER switch S5 controls the application of +3 and +13 vdc to simulator circuits other than the clock oscillator. Switch S5 provides a path for the +13-volt return to the winding of relay K1.

The +3-vdc power supply is furnished with primary power when relay K1 is energized. The period of time between the application of primary power to the supply and the availability of +3 volts at the output of the supply is utilized by relay K2 to produce the IRIG BIAS RESET pulse.

The power and control circuit, for part number 1014061-011 (figure 4-19) is slightly different. The +3 and +13 vdc supplies are on with the application

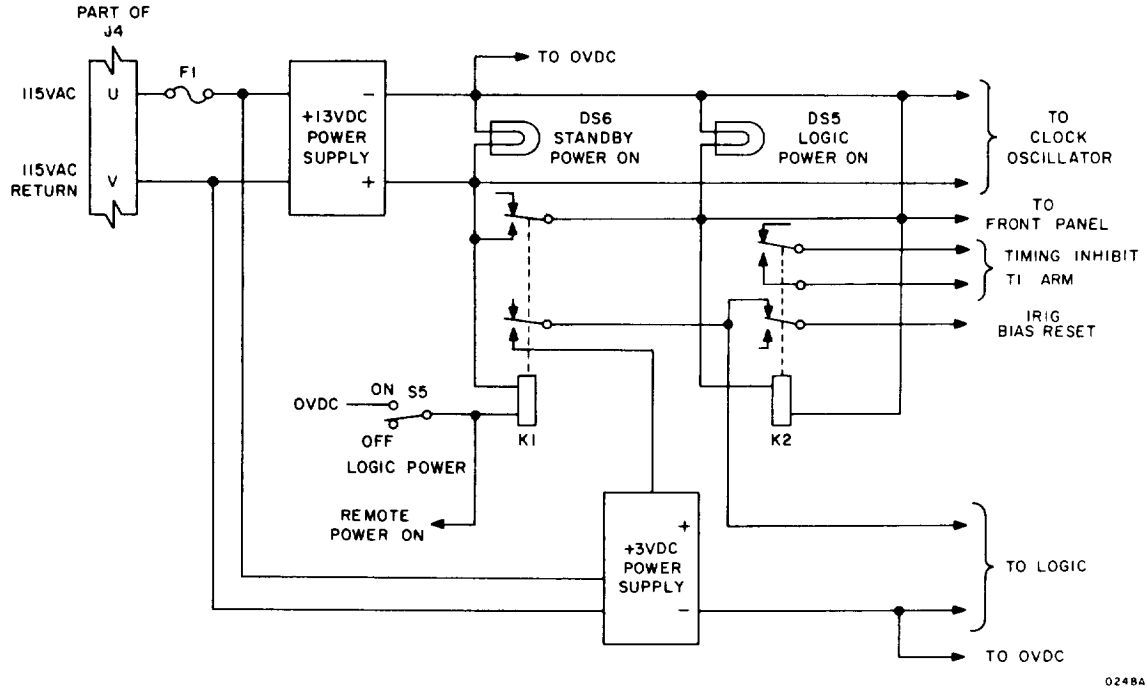

Figure 4-19. Power and Control Circuit for PN 1014061-011, Simplified Schematic Diagram

of 115 vac. Plus 13 vdc is handled as in the -1 configuration. The +3 vdc circuit differs in that the output is controlled by relay K1. Other differences are the addition of a remote power on level to the Optics-Inertial Analyzer and on extra set of relay contacts to enable an external sync to be supplied to the PSA power supply circuits in the event of a simulator power supply failure.

Chapter 5

SYSTEM TIE-IN

5-1 INTRODUCTION

This chapter contains information pertinent to interface between the AGC Simulator and external equipment.

5-2 SIMULATOR INTERFACE

Table 5-I contains a list identifying the signals at each pin of J1 through J4 at the rear of the simulator. Reference to Chapter 4, Theory of Operation, will also prove helpful to the operator.

Table 5-I. AGC Simulator Pin Identification

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks (1)
J1-A					
J1-B	+X OPT CDU SET RET				
J1-C	+X OPT CDU SET	F4D · F5 · SBII	3200 pps	Output	
J1-D	800 PPS A	F7A · SBI	800 pps	Output	
J1-E	800 PPS A RET				
J1-F	12.8 KPPS A	F3A · SBI	12.8 kpps	Output	
J1-G	12.8 KPPS A RET				
J1-H	PIPA CLK RET				
J1-J	PIPA CLK	F4D · F5 · SBII	3200 pps	Output	
J1-K	25.6 KPPS A RET				
J1-L	25.6 KPPS A	F2A · SBI	25.6 kpps	Output	
J1-M	PIPA INTERROGATE	F4D · F5 · SBI	3200 pps	Output	
J1-N	PIPA INTERROGATE RET				
J1-P	-OG CDU ENC HI IN			Input	(2)
J1-R	-OG CDU ENC LO IN			Input	
J1-S	+IG CDU ENC HI IN			Input	
J1-T	+IG CDU ENC LO IN			Input	
J1 U	800 PPS B	F7B · SBI	800 pps	Output	
J1-V	800 PPS B RET				
J1 W	+Y IRIG SET RET				
J1-X	+Y IRIG SET	F4D · F5 · SBII	3200 pps	Output	
J1-Y	25.6 KPPS B RET				
J1-Z	25.6 KPPS B	F2B · SBI	25.6 kpps	Output	
J1-a	3200 PPS A RET				
J1-b	3200 PPS A	F5A · SBI	3200 pps	Output	
J1-c	102.4 KPPS RET				
J1-d	102.4 KPPS (3)	SBII	102.4 kpps	Output	
J1-e	0 VDC				

(1) All outputs are transformer-coupled and have the following characteristics unless otherwise stated:

Amplitude, 5 v p-p
Rise time, 0.2 μsec
Pulse width, 3 ± 0.5 μsec
Droop, 0.5 volt
Test load, 200 ohms.

(2) Refer to NASA document ND 1002193.

(3) Amplitude, 6 v p-p.

Table 5-I. AGC Simulator Pin Identification (cont)

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks
J1-f	-OG CDU ENC HI IN				
J1-g	-OG CDU ENC LO IN			Input	(2)
J1-h	3200 PPS B RET				
J1-i	3200 PPS B	F5B · SBI	3200 pps	Output	
J1-j	-X OPT CDU SET	F4D · SBII · F5	3200 pps	Output	
J1-k	-X OPT CDU SET RET				
J1-m	-Y OPT CDU SET RET				
J1-n	-Y OPT CDU SET	F4D · F5 · SBII	3200 pps	Output	
J1-p	-Y OPT CDU SET	F4D · F5 · SBII	3200 pps	Output	
J1-q	-Y OPT CDU SET RET				
J1-r	PIPA - ΔVy LO IN			Input	(2)
J1-s	PIPA - ΔVx HI IN			Input	(2)
J1-t	Shield ground ACSP				Not internally connected
J1-u	PIPA - ΔVx LO IN			Input	(2)
J1-v	T.I. ARM				Timing inhibit contact closure
J1-w	T.I. N.C.				
J1-x	PIPA - ΔVy HI IN			Input	(2)
J1-y	Test point 4				Test signals for Raytheon use only
J1-z	Test point 3				
J1-AA	Test point 1				
J1-BB	Test point 2				
J1-CC	-Y OPT ENC HI IN			Input	(2)
J1-DD	-X OPT ENC HI IN			Input	
J1-EE	-X OPT ENC LO IN			Input	
J1-FF	-Y OPT ENC HI IN			Input	
J1-GG	-Y OPT ENC LO IN			Input	
J1-HH	-Y OPT ENC LO IN			Input	
J2-A					
J2-B	-OG CDU SET RET				
J2-C	-OG CDU SET	F4D · F5 · SBII	3200 pps	Output	
J2-D	-MG CDU SET RET				
J2-E	-MG CDU SET	F4D · F5 · SBII	3200 pps	Output	
J2-F	-X IRIG SET	F4D · F5 · SBII	3200 pps	Output	
J2-G	-X IRIG SET RET				
J2-H	-MG CDU SET RET				

(2) Refer to NASA document ND 1002193.

Table 5-I. AGC Simulator Pin Identification (cont)

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks
J2-J	-MG CDU SET	F4D · F5 · SBII	3200 pps	Output	
J2-K	-X IRIG SET	F4D · F5 · SBII	3200 pps	Output	
J2-L	-X IRIG SET RET				
J2-M	-OG CDU SET RET				
J2-N	-OG CDU SET	F4D · F5 · SBII	3200 pps	Output	
J2-P	-IG CDU SET RET				
J2-R	-IG CDU SET	F4D · F5 · SBII	3200 pps	Output	
J2-S	+IG CDU SET	F4D · F5 · SBII	3200 pps	Output	
J2-T	+IG CDU SET RET				
J2-U	+MG CDU ENC HI IN			Input	(2)
J2-V	+MG CDU ENC LO IN			Input	
J2-W	OPT RST RET				
J2-X	OPT RST	F4D · F5 · SBI	3200 pps	Output	
J2-Y	IRIG RST	F4D · F5 · SB0	3200 pps	Output	
J2-Z	IRIG RST RET				
J2-a	+X OPT ENC HI IN			Input	(2)
J2-b	+X OPT ENC LO IN			Input	
J2-c	CDU RST	F4D · F5 · SBI	3200 pps	Output	
J2-d	CDU RST RET				
J2-e	0 VDC				
J2-f	-MG CDU ENC HI IN			Input	(2)
J2-g	-MG CDU ENC LO IN			Input	
J2-h	-IG CDU ENC HI IN			Input	
J2-i	-IG CDU ENC LO IN			Input	
J2-j	-Z IRIG SET RET				
J2-k	-Z IRIG SET	F4D · F5 · SBII	3200 pps	Output	
J2-m	-Y IRIG SET RET				
J2-n	-Y IRIG SET	F4D · F5 · SBII	3200 pps	Output	
J2-p	-Z IRIG SET	F4D · F5 · SBII	3200 pps	Output	
J2-q	-Z IRIG SET RET				
J2-r					
J2-s					
J2-t	Shield ground ACSP				Not used internally
J2-u					
J2-v					

(2) Refer to NASA document ND 1002193.

Table 5-I. AGC Simulator Pin Identification (cont)

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks
J2-w					
J2-x					
J2-y	PIPA - ΔVy HI IN			Input	
J2-z	PIPA - ΔVy LO IN			Input	
J2-AA	PIPA + ΔVz HI IN			Input	
J2-BB	PIPA + ΔVz LO IN			Input	(2)
J2-CC	PIPA + ΔVz HI IN			Input	
J2-DD	PIPA - ΔVz LO IN			Input	
J2-EE	PIPA - ΔVx HI IN			Input	
J2-FF	PIPA - ΔVx LO IN			Input	
J2-GG					
J2-HH					
J3-A					
J3-B	+Y OPT ENC HI OUT			Output	
J3-C	+Y OPT ENC LO OUT			Output	
J3-D	-Y OPT ENC HI OUT			Output	
J3-E	-Y OPT ENC LO OUT			Output	
J3-F	PIPA + ΔVx HI OUT			Output	
J3-G	PIPA + ΔVx LO OUT			Output	
J3-H	PIPA - ΔVx HI OUT			Output	(2)
J3-J	PIPA - ΔVx LO OUT			Output	
J3-K	PIPA + ΔVy HI OUT			Output	
J3-L	PIPA + ΔVy LO OUT			Output	
J3-M	PIPA - ΔVy HI OUT			Output	
J3-N	PIPA - ΔVy LO OUT			Output	
J3-P	PIPA + ΔVz HI OUT			Output	
J3-R	PIPA + ΔVz LO OUT			Output	
J3-S	CLOCK SYNC SET RET				
J3-T	CLOCK SYNC SET (4)	C2	512 kc	Output	Square wave
J3-U	+IG CDU ENC HI OUT			Output	
J3-V	+IG CDU ENC LO OUT			Output	
J3-W	-IG CDU ENC HI OUT			Output	(2)
J3-X	-IG CDU ENC LO OUT			Output	
J3-Y	+MG CDU ENC HI OUT			Output	

(2) Refer to NASA document ND 1002193.

(4) Amplitude, 7 v p-p.

Table 5-I. AGC Simulator Pin Identification (cont)

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks
J3-Z	+MG CDU ENC LO OUT			Output	
J3-a	-MG CDU ENC HI OUT			Output	
J3-b	-MG CDU ENC LO OUT			Output	(2)
J3-c	+X OPT ENC HI OUT			Output	
J3-d	+X OPT ENC LO OUT			Output	
J3-e	0 VDC				
J3-f	-X OPT ENC HI OUT			Output	(2)
J3-g	-X OPT ENC LO OUT			Output	
J3-h	EXT T.B. #3	F7B · SBI	800 pps	Output	
J3-i	EXT T.B. #3 RET				
J3-j	EXT T.B. #2	F6B · SBI	1600 pps	Output	
J3-k	EXT T.B. #2 RET				
J3-m	+OG CDU ENC HI OUT			Output	
J3-n	+OG CDU ENC LO OUT			Output	
J3-p					
J3-q					
J3-r					
J3-s					
J3-t					
J3-u					
J3-v					
J3-w					
J3-x					
J3-y	External inhibit			Input	Remote control
J3-z					
J3-AA					
J3-BB					
J3-CC	+3 vdc logic		dc	Output	Monitoring
J3-DD					
J3-EE					
J3-FF					
J3-GG					
J3-HH					
J4-A	Chassis ground				
J4-B					
J4-C					

(2) Refer to NASA document ND 1002193.

Table 5-I. AGC Simulator Pin Identification (cont)

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks
J4-D					
J4-E					
J4-F	-OG CDU ENC HI OUT			Output	⟩ (2)
J4-G	-OG CDU ENC LO OUT			Output	
J4-H					
J4-J					
J4-K					
J4-L					
J4-M					
J4-N					
J4-P					
J4-R					
J4-S					
J4-T					
J4-U	115 vac		60 cps	Input	AC power, single phase
J4-V	115 vac return				
J4-W					
J4-X					
J4-Y					
J4-Z					
J4-a	EXT TB #1 RET				
J4-b	EXT TB #1	F4D · F5 · SBI	3200 pps	Output	
J4-c					
J4-d					
J4-e	0 vdc				
J4-f					
J4-g					
J4-h	REMOTE PROGRAMMED SIGNAL	F4D · F5 · SBII	3200 pps	Output	
J4-i	REMOTE PROGRAMMED SIGNAL RET				
J4-j	PIPA - ΔVz HI OUT			Output	⟩ (2)
J4-k	PIPA - ΔVz LO OUT				
J4-m	T.I. ARM				Timing inhibit contact closure
J4-n	T.I. N.C.				
J4-p					
J4-q					
J4-r					

(2) Refer to NASA document ND 1002193.

Table 5-I. AGC Simulator Pin Identification (cont)

Connector and Pin Number	Signal	Boolean Equation	Frequency	Flow	Remarks
J4-s J4-t J4-u J4-v J4-w J4-x J4-y J4-z J4-AA J4-BB J4-CC J4-DD J4-EE J4-FF J4-GG J4-HH	+13V STBY		dc	Output	Remote control

Chapter 6

CHECKOUT AND ANALYSIS

6-1 INTRODUCTION

This chapter contains information pertinent to checkout and analysis of the AGC Simulator. Included are the calibration procedures required to maintain the simulator at a level of accuracy necessary for proper operation. The procedures contain the test methods for determining the accuracy of the clock oscillator and the drive rate outputs.

6-2 MAINTENANCE

Because of the relative simplicity of construction, maintenance of the AGC Simulator consists of making periodic inspections.

6-2.1 PERIODIC INSPECTION. An inspection of the electrical and electromechanical parts of the simulator is required once a month. Conduct a general inspection, paying particular attention to wiring harnesses that are flexed, such as those connected to logic plate assemblies, the interconnection plate, and the front panel.

6-2.2 LEVEL OF MAINTENANCE. The level of maintenance for the simulator consists of replacing defective modules, wiring harnesses, switches, indicators, controls, relays, and power supplies.

6-3 CHECKOUT AND CALIBRATION

The procedure for checkout and calibration of the AGC Simulator is illustrated on figure 6-1 and described in the following paragraphs. Figure 6-2 is provided as an added visual aid for both checkout and calibration.

6-3.1 TEST EQUIPMENT REQUIRED. The items of equipment required for checkout and calibration are listed in table 2-I. The use of operating controls and calibration of commercial test equipment are explained in the applicable commercial handbooks. The commercial equipment should be calibrated in accordance with manufacturer's instructions prior to calibration of the AGC Simulator.

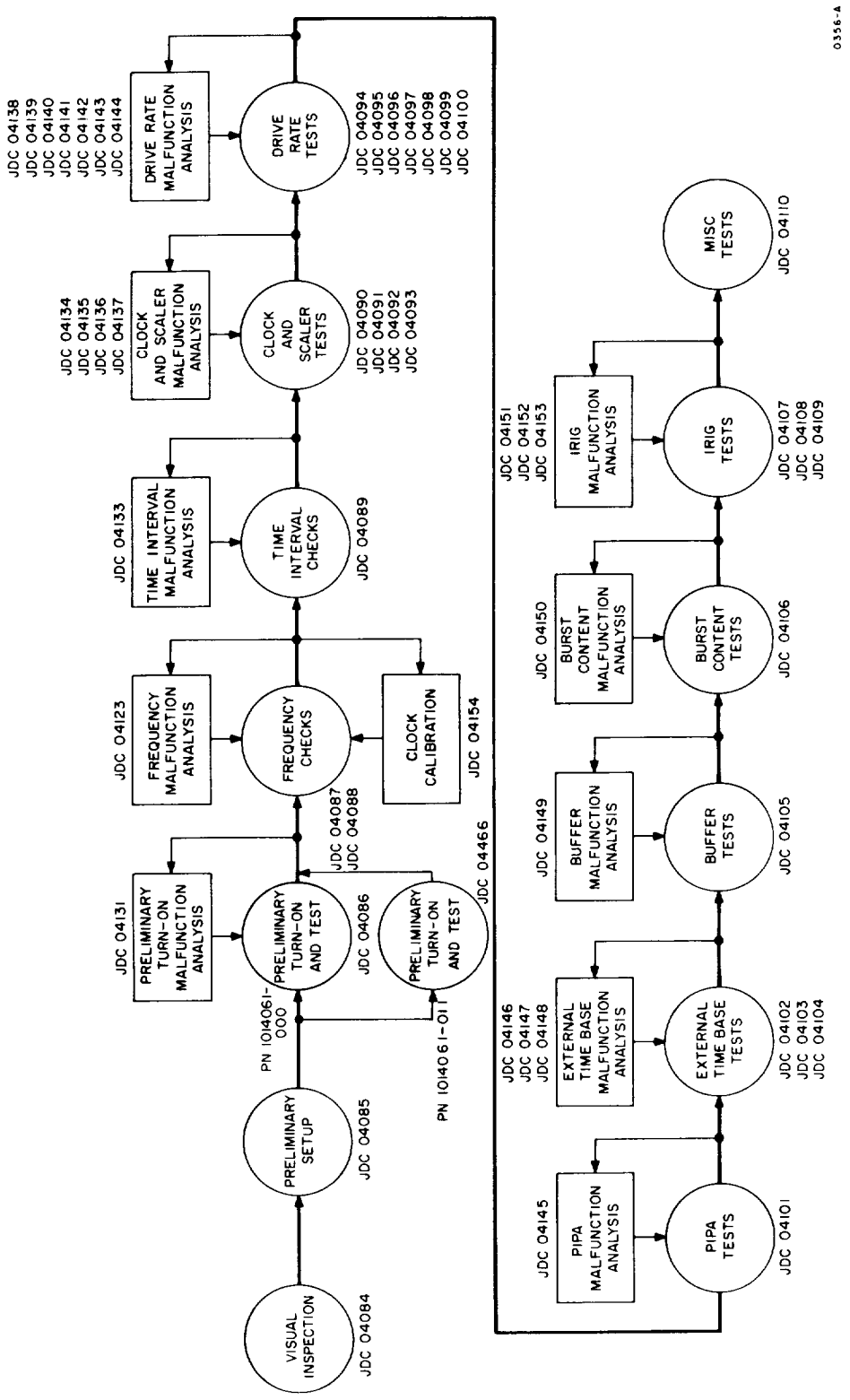

Figure 6-1. AGC Simulator Checkout and Calibration Flowgram

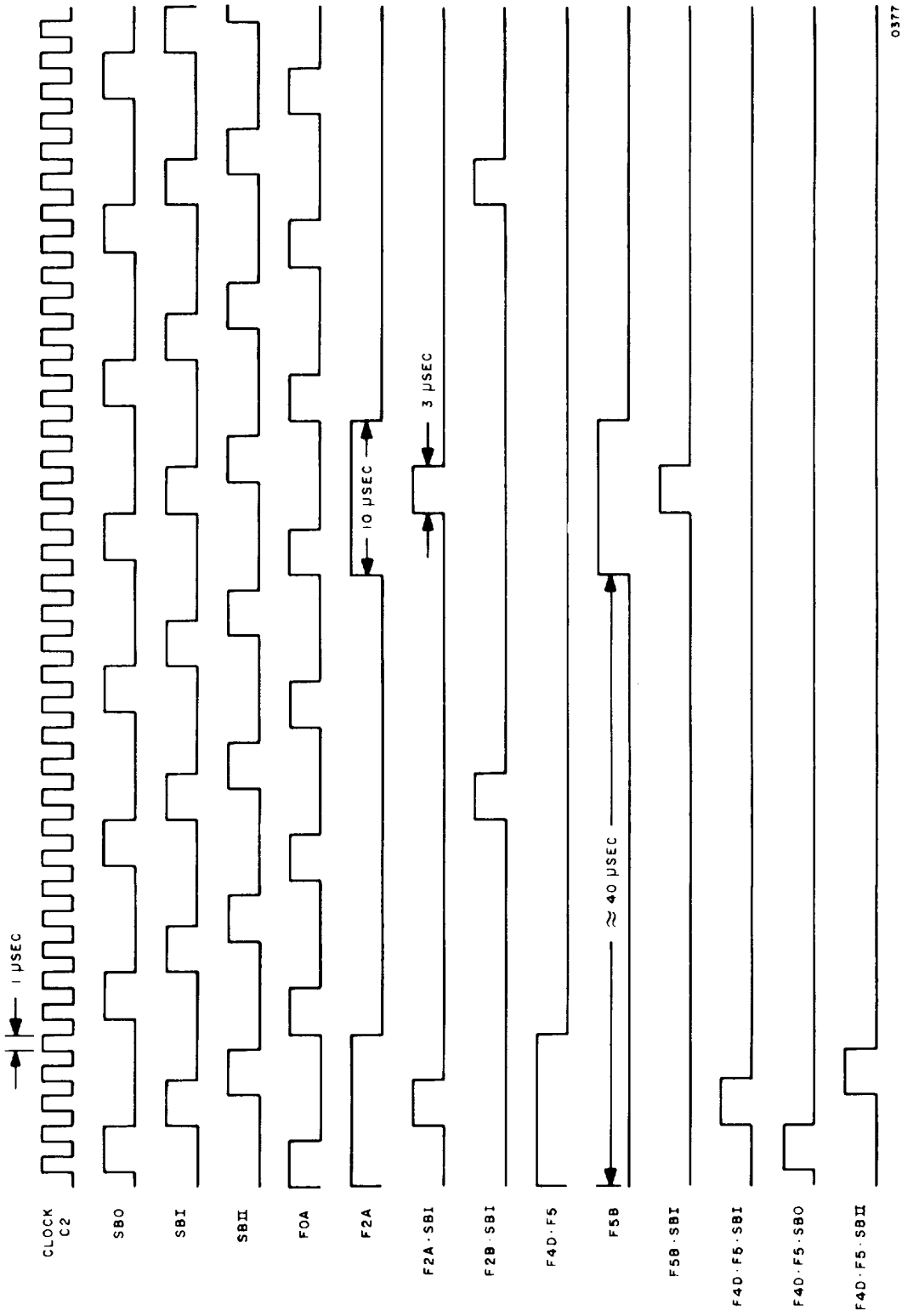

Figure 6-2. Timing Diagram

6-3.2 CALIBRATION SCHEDULE. Calibration of the AGC Simulator is required after each period of 60 working days with the exception of JDC's 04085, 04086, and 04087 which must be performed every 30 days, and after prolonged storage or shipment.

6-3.3 PRELIMINARY CHECKOUT. Perform JDC 04086 for part number 1014061-000 and JDC 04466 for part number 1014061-011 prior to the performance of the checkout and calibration procedure. The JDC can be used also to provide a confidence check if the simulator has not been left idle for an extended period of time.

6-3.4 CHECKOUT AND CALIBRATION PROCEDURE. The procedure for checkout and calibration of the AGC Simulator is contained in JDC's 04084 through 04111, 04466, and 04154. (See figure 6-1.) The definitions and abbreviations used in this procedure are listed in table 6-I.

Table 6-I. Definitions and Abbreviations

Term	Definition
AGC	Apollo Guidance Computer
FTM	Final test method
JDC	Job Description card
NLT	Not less than
NMT	Not more than
Pulse characteristics	See figure 6-3
PW	Pulse width
T_r	Rise time
T_f	Fall time

6-4 MALFUNCTION ISOLATION AND ANALYSIS

Since the operation of the AGC Simulator depends on a delicate relationship between levels, pulses, and trains of pulses, it is important to know some of the techniques that can be used to determine which circuit is at fault when the coincidence of these stimuli is faulty of lacking entirely.

It is not the function of this manual to give all possible malfunctions nor the specific means by which to analyze them. However, a general, yet comprehensive, troubleshooting guide is provided in the Malfunction Analysis JDC's (04131 through 04153), shown in the flowgram, figure 6-1. These

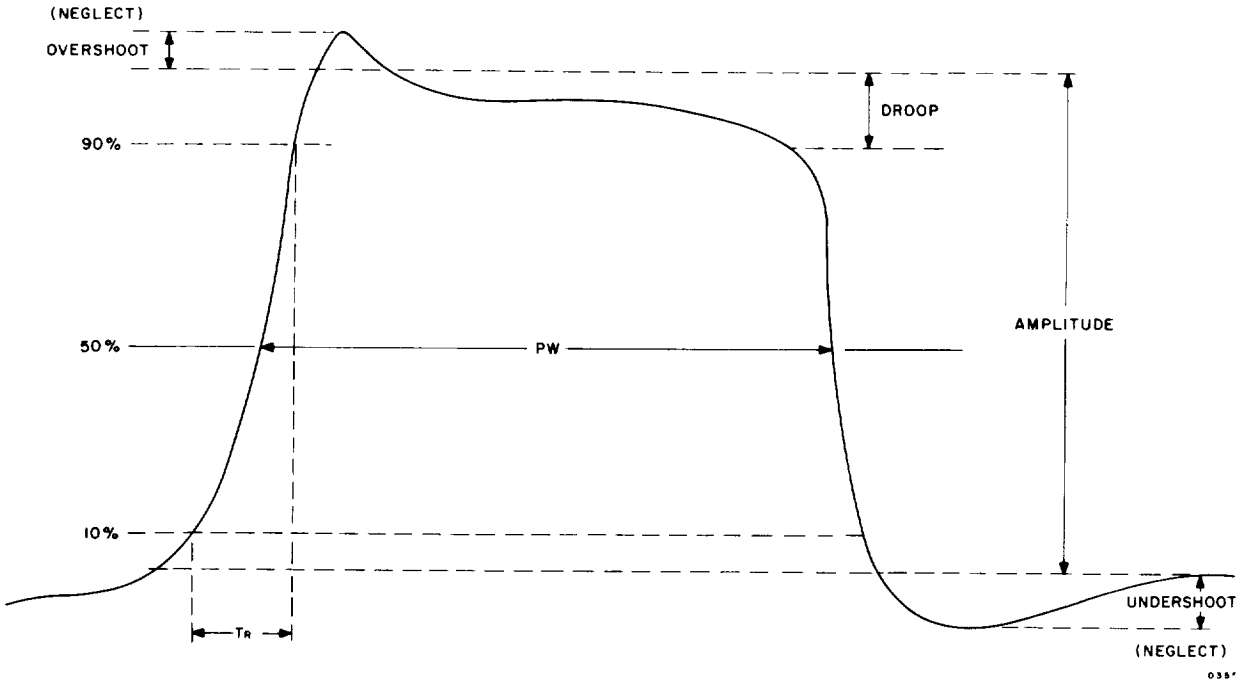

Figure 6-3. Pulse Characteristics

JDC's list the Boolean equations for all major signals and the individual modules from which the signals originate during subsystem tests. Therefore, by validating the equations, i.e., checking inputs and outputs, one can isolate a malfunction to a specific module.

The Malfunction Analysis JDC's also list the schematic reference for each signal. The area in which a particular signal can be found on drawing 1014063 is identified by the sheet number and a location designation consisting of a letter and a number. The letter denotes a vertical page co-ordinate; the number, a horizontal page co-ordinate. The junction of the two is the area of interest.

Drawings and JDC's related to the AGC Simulator are listed in Appendices A and B.

Chapter 7

REPAIR AND REPLACEMENT

7-1 REPAIR

AGC Simulator repair is performed with tools which are available at the site where the simulator is located. Simulator repair requires no special procedures and is accomplished by replacing the defective component.

7-2 REPLACEMENT

Replacement of defective components or wiring harnesses should be performed according to standard procedures. When switches, wiring harnesses, or other devices that are junction points for two or more wires are replaced, it is suggested that all wires be tagged for identification. Modules are removed with the module extraction tool (figure 1-4). The two notched areas on the module, at the end farthest from the connector, accommodate the hooked ends of the tool.

7-3 TESTING

When replacements are made in the AGC Simulator, all tests described in Chapter 6 need not be performed. Determine the affected area(s) and perform those tests required to restore the simulator to a fully operable condition.

Appendix A

NUMERICAL LISTING OF JDC's REFERENCED WITHIN THIS MANUAL

JDC Number	Title
04084	AGC Simulator Visual Inspection (Field)
04085	Preliminary Setup (Field)
04086	Preliminary Turn-on (Field)
04087	Frequency Check of Clock Sync Signal (Field)
04088	Frequency Check of Continuous Outputs (Field)
04089	Time Interval Checks (Field)
04090	Clock and Scaler Test 1 (Field)
04091	Clock and Scaler Test 2 (Field)
04092	Clock and Scaler Test 3 (Field)
04093	Clock and Scaler Test 4 (Field)
04094	Drive Rate Test 1 (Field)
04095	Drive Rate Test 2 (Field)
04096	Drive Rate Test 3 (Field)
04097	Drive Rate Test 4 (Field)
04098	Drive Rate Test 5 (Field)
04099	Drive Rate Test 6 (Field)
04100	Drive Rate Test 7 (Field)
04101	PIPA Clock and PIPA Set Test (Field)
04102	External Time Base Test 1 (Field)
04103	External Time Base Test 2 (Field)
04104	External Time Base Test 3 (Field)
04105	Buffer Tests (Field)
04106	Burst Content Tests (Field)
04107	IRIG Test 1 (Field)
04108	IRIG Test 2 (Field)
04109	IRIG Test 3 (Field)
04110	Miscellaneous Simulator Tests (Field)
04131	Malfunction Analysis for Preliminary Turn-on
04132	Malfunction Analysis for Frequency Check of Continuous Outputs
04133	Malfunction Analysis for Time Interval Checks

Appendix A

NUMERICAL LISTING OF JDC's REFERENCED WITHIN THIS MANUAL (cont)

JDC Number	Title
04134	Malfunction Analysis for Clock and Scaler Test 1
04135	Malfunction Analysis for Clock and Scaler Test 2
04136	Malfunction Analysis for Clock and Scaler Test 3
04137	Malfunction Analysis for Clock and Scaler Test 4
04138	Malfunction Analysis for Drive Rate Test 1
04139	Malfunction Analysis for Drive Rate Test 2
04140	Malfunction Analysis for Drive Rate Test 3
04141	Malfunction Analysis for Drive Rate Test 4
04142	Malfunction Analysis for Drive Rate Test 5
04143	Malfunction Analysis for Drive Rate Test 6
04144	Malfunction Analysis for Drive Rate Test 7
04145	Malfunction Analysis for PIPA Clock and PIPA Set Test
04146	Malfunction Analysis for External Time Base Test 1
04147	Malfunction Analysis for External Time Base Test 2
04148	Malfunction Analysis for External Time Base Test 3
04149	Malfunction Analysis for Buffer Tests
04150	Malfunction Analysis for Burst Content Tests
04151	Malfunction Analysis for IRIG Test 1
04152	Malfunction Analysis for IRIG Test 2
04153	Malfunction Analysis for IRIG Test 3
04154	512-kc Clock Calibration
*19533	Packaging and Packing AGC Simulator
04466	Preliminary Turn-on (Field)
04234	AGC Simulator Checkout Information

*From ND 1021035

Appendix B

NUMERICAL LISTING OF DRAWINGS REFERENCED WITHIN THIS MANUAL

NASA Drawing Number	Title
1006988	Slide, Chassis
1014078	Tool, Extracting
1014027	Channel, Bottom Right
1014028	Channel, Bottom Left
1014045	Chassis Structure
1014046	Cable Assembly
1014063	Logic Flow Diagram
1014084	Chassis Assembly DC Power Supply
1014090	Logic Plate Assembly
1014098	Schematic, Front Panel
1014099	Logic Plate Assembly
1014106	Front Panel
1014110	Logic Plate Assembly
1014112	Cable Assembly
1014113	Interconnection Plate
1014117	Schematic, Interconnection Plate (Part Number 1014061-000)
1014120	Cable Assembly
1014251	Schematic, Front Panel
1020202	Schematic, Interconnection Plate (Part Number 1014061-011)

CAUTION: The JDC's and data sheets contained in this manual may be used for testing, maintenance, or repair instructions only after verification with SIDL. Only the latest revision of a JDC and data sheet should be used for performing any operation on equipment. Printouts of individual JDC's and the associated data sheets can be obtained from aperture cards on file at all sites.

JDC: 04084 REV: A PAGE 1 OF 1

JOB: VISUAL INSPECTION

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment -- AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

Visual inspection prior to use.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	A11	All	WK	WR

REFERENCES:

IMPORTANT:

INTERVAL: Every month

TOOLS AND MATERIAL:

PROCEDURE: Perform the following inspections and record results.

1. Examine interior and exterior of AGC Simulator, paying particular attention to the condition of cables, connectors, switches, and parts with some degree of freedom such as modules, logic plates, etc.
2. Check connectors for good electromechanical connections.
3. Tighten four Allen-head set screws on front panel for good RFI seal. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04084
REV. A
INITIAL TDRR 11119

JOB: VISUAL INSPECTION

ASSEMBLY UNDER TEST

TITLE AGC Simulator

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ _____ (CAL DATE)

NAME _____ SER. NO. _____ _____ (CAL DATE)

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

	Accept	Reject
1. Simulator	_____	_____

VERIFICATION WITH SIDL
REQUIRED BEFORE USE

DATE 21 July 64

JOB: PRELIMINARY SETUP

JDC: 04085 REV: A PAGE 1 OF 1

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment -- AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

Preparation for use.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT:

INTERVAL: Every 30 days

TOOLS AND MATERIAL: Two female crimp-type connector pins (Bendix or equivalent) and jumpers.

PROCEDURE: Perform the following procedure and record the results.

1. Set all switches to the OFF, NORMAL, CONT or fully CCW positions as applicable. Record.
2. Use two female crimp-type connector pins (Bendix or equivalent) and associated jumper wires and apply 115 vac, single-phase 60 cps to the Simulator via pins J4U (high) and J4V (common) on rear external connector, J4. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04085
REV. A
INITIAL TDRR 11119

JOB: PRELIMINARY SETUP

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME ____ SER. NO. ____ CAL DATE ____

NAME ____ SER. NO. ____ CAL DATE ____

CONDUCTED BY ____ (NAME/AFFILIATION) APPROVED BY ____ (NAME/AFFILIATION)

1. Switches ____
2. AC power ____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04086 REV: A PAGE 1 OF 2

JOB: PRELIMINARY TURN-ON (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment -- AGC Simulator

ASSY: 60A06 1014061-000

DESCRIPTION:

Preliminary front panel and power supply checks for AGC Simulator 1014061-1 only.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

ND 1014251
ND 1014117

IMPORTANT: JDC 04085 must be completed before this procedure is performed. This check for PN 1014061-000 only. Use JDC 04466 for PN1014061-011.

INTERVAL:

Every 30 days.

TOOLS AND MATERIAL: VTVM (John Fluke Model 803B or equivalent); VOM (Simpson Model 269 or equivalent)

PROCEDURE: Perform the following procedure and record the results.

1. Energize 115 vac to simulator and check that STANDBY POWER ON lamp glows. Record.
2. Set LOGIC POWER ON switch on d-c power supply assembly (figure 1-6, ND 1021003) to ON position. LOGIC POWER ON lamp should glow. BIAS REQD lamp should glow. Record.
3. Press IRIG BIAS pushbutton. BIAS REQD LAMP should go out. Record.
4. Set SCALER TEST switch to ON. SCALER TEST OPERATING lamp should blink. Record.
5. Set TIMING INHIBIT switch to INHIBIT position. TIMING INHIBIT lamp should glow. SCALER TEST should go off or glow steadily. Read no continuity (refer to ND 1014117 and ND 1014251).

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

From	To
J1v	J1w
J1v	J4n
J4m	J4n
J4m	J1w

6. Return TIMING INHIBIT switch to NORMAL position. Record.

   TIMING INHIBIT lamp should go out.
   SCALER TEST OPERATING lamp should blink.
   Read continuity (refer to ND 1014117 and ND 1014251):

From	To
J1v	J1w
J1v	J4n
J4m	J4n
J4m	J1w

7. Set SCALER TEST switch to OFF. Record.

8. Using VTVM, measure and record.

   +3.0 ± 0.15 vdc at 3-volt test points on power supply assembly.
   +13.0 ± 0.65 vdc at 13-volt points on power supply assembly.

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04086
REV. A
INITIAL TDRR _____

JOB: PRELIMINARY TURN-ON

ASSEMBLY UNDER TEST

TITLE AGC Simulator

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

		Yes	No
1.	STANDBY POWER lamp on		
2.	LOGIC POWER		
	POWER ON lamp on		
	BIAS REQD lamp on		
3.	BIAS REQD lamp out		
4.	SCALER TEST OPERATING lamp blinks		
5.	TIMING INHIBIT switch to INHIBIT		
	TIMING INHIBIT lamp on		
	SCALER TEST lamp off or glowing steady		
	No continuity J1v to J1w		
	J1v to J4n		
	J4m to J4n		
	J4m to J1w		
6.	TIMING INHIBIT switch to NORMAL		
	TIMING INHIBIT lamp out		
	SCALER TEST OPERATING lamp blinks		
	No continuity J1v to J1w		
	J1v to J4n		
	J4m to J4n		
	J4m to J1w		
7.	SCALER TEST switch OFF		
8.	Voltages		
	3 vdc		3.0 ± 0.15 vdc
	13 vdc		13.0 ± 0.65 vdc

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04087 REV: A PAGE 1 OF 1

JOB: FREQUENCY CHECK OF CLOCK SYNC SIGNAL | INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment -- AGC Simulator | ASSY: 1014061-000 and 1014061-001 60A06

DESCRIPTION:

The frequency of clock sync signal is checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 30 days.

TOOLS AND MATERIAL: Coaxial cable with BNC connectors, Counter (Beckman Model 6146 with Extender Model 602 or equivalent)

PROCEDURE: Perform the following procedure and record the results.

1. Allow 45 minutes of warmup time for oscillator to stabilize. Record.
2. Using coaxial cable with BNC connectors, connect CLOCK SYNC jacks on simulator front panel to counter input. Set counter to read a frequency of 512 kc. Record. Read 512000.0 cps.
3. Disconnect counter from simulator.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04087
REV. A
INITIAL TDRR 11119

JOB: FREQUENCY CHECK OF CLOCK SYNC SIGNAL

ASSEMBLY UNDER TEST

TITLE AGC Simulator

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

1. Warmup complete _____
2. Clock sync _____ 512000.0 cps

VERIFICATION WITH SIDL
REQUIRED BEFORE USE

DATE 21 July 64

JOB: FREQUENCY CHECK OF CONTINUOUS OUTPUTS

JDC: 04088 REV: A PAGE 1 OF 1

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment -- AGC Simulator

ASSY: 1014061-000 and 1014061-011 60A06

DESCRIPTION:

The frequencies of the continuous outputs are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Counter (Beckman model 6146 with extender model 602 or equivalent); coaxial cable with BNC connectors.

PROCEDURE: Perform the following procedure and record the results.

1. Adapt test connectors of coaxial cable as necessary to mate with rear connector pins specified in the following steps.
2. Connect counter to J1d and J1c. Read and record 102.4 kpps.
3. Connect counter to J1L and J1K. Read and record 25.6 kpps.
4. Connect counter to J1Z and J1Y. Read and record 25.6 kpps.
5. Connect counter to J1F and J1G. Read and record 12.8 kpps.
6. Connect counter to J1b and J1a. Read and record 3200 pps.
7. Connect counter to J1i and J1h. Read and record 3200 pps.
8. Connect counter to J1D and J1E. Read and record 800 pps.
9. Connect counter to J1U and J1V. Read and record 800 pps.
10. Connect counter to J1J and J1H (PIPA clock). Read and record 3200 pps.
11. Connect counter to J1M and J1N (PIPA set). Read and record 3200 pps.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04088
REV. A
INITIAL TDRR 11119

JOB: FREQUENCY CHECK OF CONTINUOUS OUTPUTS

ASSEMBLY UNDER TEST

TITLE AGC Simulator

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ _____ (CAL DATE)

NAME _____ SER. NO. _____ _____ (CAL DATE)

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

2.	102.4 KPPS	_____	102.4 kpps
3.	25.6A KPPS	_____	25.6 kpps
4.	25.6B KPPS	_____	25.6 kpps
5.	12.8 KPPS	_____	12.8 kpps
6.	3200A PPS	_____	3200 pps
7.	3200B PPS	_____	3200 pps
8.	800A PPS	_____	800 pps
9.	800B PPS	_____	800 pps
10.	PIPA CLK	_____	3200 pps
11.	PIPA SET	_____	3200 pps

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04089 REV: A PAGE 1 OF 1

JOB: TIME INTERVAL CHECKS

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The time intervals between signals are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Counter (Beckman model 6146 with extender model 602 or equivalent)

PROCEDURE: Perform the following procedure and record the results.

1. Set counter for time interval measurement at 10-nanosecond resolution.
2. Connect START counter input to J1D and J1E.
   Connect STOP counter input to J1U and J1V.
   Adjust counter controls as necessary.
   Read 625 ± 0.2 μsec. Record.
3. Connect START counter input to J1b and J1a.
   Connect STOP counter input to J1i and J1h.
   Read 156.2 ± 0.2 μsec. Record.
4. Connect START counter input to J1L and J1K.
   Connect STOP counter input to J1Z and J1Y.
   Read 19.5 ± 0.2 μsec. Record.
5. Connect START counter input to J1b and J1a.
   Connect STOP counter input to J1M and J1N.
   Read 117.2 ± 0.2 μsec. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04089
REV. A
INITIAL TDRR 11119

JOB: TIME INTERVAL CHECKS (FIELD)

ASSEMBLY UNDER TEST

TITLE AGC Simulator

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

2.	800A to 800B	_____	625 ± 0.2 μsec
3.	3200A to 3200B	_____	156.2 ± 0.2 μsec
4.	25.6A to 25.6B	_____	19.5 ± 0.2 μsec
5.	3200A to PIPA SET	_____	117.2 ± 0.2 μsec

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04090 REV: A PAGE 1 OF 2

JOB: CLOCK AND SCALER TEST 1 (FIELD) | INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator | 60A06 ASSY: 1014061-000 and 1014061-011

DESCRIPTION:
The pulse characteristics and timing characteristics of the following signals are checked: 25.6A, CDU +OG, 102.4 KPPS, and 512 KC.

Rev. Let.	Date	TDRR NO.	PAGES REVISED JDC	PAGES REVISED D.S.	APPROVAL MIT	APPROVAL NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL:
Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 535A, Type M preamplifier, or equiv); Probes (4, Tektronix P6000x10, or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male); jumpers

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

25.6A	J1L and J1K
+OG	J2C and J2B
102.4 KPPS	J1d and J1c
512 KC	J3T and J3S.

2. Ground J1K, J2B, J1c, and J3S.

3. Ground scope to Simulator chassis and monitor:

   J1L on channel A
   J2C on channel B
   J1d on channel C
   J3T on channel D.

4. Sync scope on J2Y, J2Z to ground.

5. Monitor channels A and D for coincident signals. Record.

6. Monitor channel B signal for a delay of 2.0 ± 0.2 μsec from channel A signal (DRIVE SELECT to OG; POLARITY to +). Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Monitor channel C signal for a delay of 2.0 ± 0.2 μsec from channel A signal. Record

8. Check channel D for the following characteristics and record:

Wave symmetry	
Amplitude	7 ± 0.7 vpp
Rise time	NMT 0.2 μsec.

9. Check channel C for the following characteristics and record:

Pulse amplitude	6 ± 0.6 vpp
Pulse width	3 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

10. Check channels A and B for the following characteristics and record:

Pulse amplitude	5 ± 0.5 vpp
Pulse width	3 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

11. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04090
REV. A
INITIAL TDRR 11119

JOB: CLOCK AND SCALER TEST 1 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5.	Coincidence	Yes____	No____
6.	Delay	_____	2.0 ± 0.2 μsec
7.	Delay	_____	2.0 ± 0.2 μsec
8.	512-kc characteristics		
	Square wave symmetry	Yes____	No____
	Amplitude	_____	7.0 ± 0.7 vpp
	Rise time	_____	NMT 0.2 μsec
9.	102.4-kpps characteristics		
	Amplitude	_____	6.0 ± 0.6 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
10.	Channel A characteristics (25.6A)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel B characteristics (+OG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04091 REV: A PAGE 1 OF 2

JOB: CLOCK AND SCALER TEST 2 (FIELD) | INITIAL TDRR 11119 D.S. PGS. 1

Ground Support Equipment - | 60A06

SUBSYSTEM: AGC Simulator | ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: 25.6A, 25.6B, 3200A, and 3200B.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04084, 04085, and 04090 must be completed before this JDC is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A Type M preamplifier or equiv); probes (4, Tektronix P6000x10, or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert jumper from J4A to J4e and place loads across:

25.6A	J1L and J1K
25.6B	J1Z and J1Y
3200A	J1b and J1a
3200B	J1i and J1h.

2. Ground J1K, J1Y, J1a, and J1h.

3. Ground scope to Simulator chassis and monitor:

J1L on channel A	J1b on channel C
J1Z on channel B	J1i on channel D.

4. Sync scope on J2Y, J2Z to ground.

5. Check channels A and B for 180° phase relationship. B follows A. Record.

6. Check channels C and D for 180° phase relationship. C follows D. Record.

7. Check channels C and D for one-eighth rate coincidence with channel A. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

8. Check the following characteristics of channels B, C, and D. Record.

   NOTE: Channel A checked in JDC 04090.

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

9. Reverse all grounds and scope inputs. Check for presence of inverted signals, channels A through D. Record.

10. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04091
REV. A
INITIAL TDRR 11119

JOB: CLOCK AND SCALER TEST 2 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

		Yes	No
5.	Channel B 180° from A	_____	_____
6.	Channel D 180° from C	_____	_____
7.	Coincidence C with A	_____	_____
	D with A	_____	_____
8.	Channel B characteristics (25.6B)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel C characteristics (3200A)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel D characteristics		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
9.	Signal inversion, channels A through D	Yes _____	No _____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: CLOCK AND SCALER TEST 3 (FIELD) | INITIAL TDRR 11119 D.S. PGS. 1

Ground Support Equipment - 60A06

SUBSYSTEM: AGC Simulator | ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of RST IRIG signals are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED JDC	PAGES REVISED D.S.	APPROVAL MIT	APPROVAL NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL:

Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male); counter (Beckman model 602 or equiv)

PROCEDURE: Perform the following procedure and record the results.

1. Insert jumper from J4A to J4e and place loads across:

RST IRIG	J2Y and J2Z
102.4	J1d and J1c.

2. Ground J2Z and J1c.
3. Connect counter START to J2Y and J2Z.
4. Connect counter STOP to J1d and J1c.
5. Set counter for time interval measurement (10-nanosecond resolution) and read 4.9 ± 0.2 μsec. Record.
6. Disconnect counter.
7. Ground scope to simulator chassis and monitor J2Y on channel A and J1d on channel B.
8. Sync scope on channel A signal.
9. Measure channel A characteristics as follows and record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

10. Reverse all grounds and scope inputs. Check for presence of inverted signals on channels A and B. Record.

11. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04092
REV. A
INITIAL TDRR 11119

JOB: CLOCK AND SCALER TEST 3 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5.	Time interval	_____	4.9 ± 0.2 μsec
9.	Channel A characteristics (IRIG RST)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
10.	Signal inversion, channels A and B	Yes_____	No_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: CLOCK AND SCALER TEST 4 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

60A06

ASSY: 1014061-000 and 1014061-011

DESCRIPTION: The pulse characteristics and timing relationships of RST OPT signal are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier, or equiv); probes (4, Tektronix P6000x10, or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert jumper from J4A to J4e and place loads across:

RST OPT	J2X and J2W
+OG	J2C and J2B.

2. Ground J2W and J2B.

3. Ground scope to simulator chassis and monitor J2X on channel A and J2C on channel B.

4. Sync scope on J2Y with J2Z to ground.

5. Observe channel B signal delayed 2.0 ± 0.2 μsec from Channel A signal. (POLARITY switch to +, DRIVE SELECT switch to OG.) Record.

6. Check following characteristics of channel A and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Reverse all grounds and scope inputs. Check for presence of inverted signals on channels A and B. Record.

8. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04093
REV. A
INITIAL TDRR 11119

JOB: CLOCK AND SCALER TEST 4 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. _____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5.	Channel B delayed from A	_____	2.0 ± 0.2 μsec
6.	Channel A characteristics (OPT RST)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.	Signal inversion, channels A and B	Yes _____	No _____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04094 REV: A PAGE 1 OF 2

JOB: DRIVE RATE TEST 1 (FIELD) | INITIAL TDRR 11119 D.S. PGS. 1

Ground Support Equipment - | 60A06

SUBSYSTEM: AGC Simulator | ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics of PDR and the timing relationships between PDR and +OG CDU are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

power supply +13 vdc (Harrison laboratory 855B or equiv)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

   PDR J4h and J4i
   +OG J2C and J2B.

2. Ground J4i and J2B.

3. Ground scope to Simulator chassis and monitor:

   J4h on channel A
   J2C on channel B.

4. Sync scope on J4h.

5. Check channel B for coincidence with channel A. (DRIVE SELECT switch to OG, POLARITY switch to +.) Record.

6. Set POLARITY switch to OFF. Note absence of signals on both channels of scope. Record.

7. Return POLARITY switch to + position and measure following signal characteristics of channel A and record:

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v

8. Apply +13 vdc from external power supply (Harrison Laboratory 855B or equivalent) to pin J3y. Observe presence of signal on channel A and absence of signal on channel B. DRIVE RATE INHIBITED lamp should glow. Record.

9. Set DISABLE DRIVE RATE INHIBIT switch to OVERRIDE position and monitor channel B for signal presence. DISABLE DRIVE RATE INHIBIT lamp should glow. DRIVE RATE INHIBITED lamp should remain glowing. Record.

10. Return DISABLE DRIVE RATE INHIBIT switch to NORMAL position. Remove external +13 vdc. Both lamps should extinguish. Monitor scope for presence of signal on channel B. Record.

11. Reverse all grounds and scope inputs. Check for presence of inverted signals on both channels. Record.

12. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04094
REV. A
INITIAL TDRR 11119

JOB: DRIVE RATE TEST 1 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME ____ SER. NO. ____ CAL DATE ____

NAME ____ SER. NO. ____ CAL DATE ____

CONDUCTED BY ____ (NAME/AFFILIATION) APPROVED BY ____ (NAME/AFFILIATION)

		Yes	No
5.	Coincidence A-B		
6.	Absence of signals		
7.	Channel A characteristics (PDR)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v

		Yes	No
8.	Presence of A		
	Absence of B		
	Lamp ON		
9.	Presence of B		
	Lamp ON		
	Lamp ON		
10.	Presence of B		
	Lamps OFF		
11.	Signal inversion, channels A and B		

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04095 REV: A PAGE 1 OF 2

JOB: DRIVE RATE TEST 2 (FIELD) INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator 60A06

ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: +IG CDU, +MG CDU, and +OG CDU.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

RST CDU	J2c and J2d
+OG	J2C and J2B
+IG	J2S and J2T
+MG	J2E and J2D.

Ground J2d, J2B, J2T, and J2D.

2. Ground scope to Simulator chassis and monitor:

J2c on channel A
J2S on channel B
J2E on channel C
J2C on channel D.

3. Sync scope on J4h with J4i to ground.

4. Set DRIVE SELECT switch to IG and POLARITY switch to + and observe channel B delayed from A by 2.0 ± 0.2 μsec. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

5. Set DRIVE SELECT switch to MG. Observe channel C delayed from A by 2.0 ± 0.2 μsec.

6. Set DRIVE SELECT switch to OG. Observe channel D delayed from A by 2.0 ± 0.2 μsec.

7. Measure the following signal characteristics on each channel by enabling the appropriate signal, IG, MG, and OG, by means of the DRIVE SELECT switch: and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 + 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

8. Reverse all grounds and scope inputs. Observe presence of inverted signals on all channels with corresponding settings of DRIVE SELECT switch. Record.

9. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04095
REV. A
INITIAL TDRR 11119

JOB: DRIVE RATE TEST 2 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. _____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

4.	Channel B delayed from A	_____	2.0 ± 0.2 μsec
5.	Channel C delayed from A	_____	2.0 ± 0.2 μsec
6.	Channel D delayed from A	_____	2.0 ± 0.2 μsec
7.	Channel A characteristics (RST CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel B characteristics (+IG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel C characteristics (+MG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel D characteristics (+OG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
8.	Signal inversion, all channels	Yes _____	No _____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: DRIVE RATE TEST 3 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

60A06

ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: -IG CDU, -MG CDU, and -OG CDU.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A Type M preamplifer or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

RST CDU	J2c and J2d
-IG	J2R and J2P
-MG	J2J and J2H
-OG	J2N and J2M.

2. Ground J2d, P, H, and M.

3. Ground scope to simulator chassis and monitor:

   J2c on channel A
   J2R on channel B
   J2J on channel C
   J2N on channel D.

4. Sync scope on J4h with J4i to ground.

5. Set POLARITY switch to - and DRIVE SELECT switch to IG. Observe channel B delayed from A by 2.0 ± 0.2 μsec. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

6. Set DRIVE SELECT switch to MG. Observe channel C delayed from A by 2.0 ± 0.2 μsec. **Record.**

7. Set DRIVE SELECT switch to OG. Observe channel D delayed from A by 2.0 ± 0.2 μsec. **Record.**

8. Measure signal characteristics on each channel by enabling the appropriate signal, IG, MG, or OG, by means of the DRIVE SELECT switch and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

9. Reverse all grounds and scope inputs. Observe presence of inverted signals on all channels with appropriate settings of the DRIVE SELECT switch. Record.

10. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04096
REV. A
INITIAL TDRR 11119

JOB: DRIVE RATE TEST 3 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5.	Channel B delayed from A	_____	2.0 ± 0.2 μsec
6.	Channel C delayed from A	_____	2.0 ± 0.2 μsec
7.	Channel D delayed from A	_____	2.0 ± 0.2 μsec
8.	Channel B characteristics (-IG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel C characteristics (-MG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 μsec
	Channel D characteristics (-OG CDU)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
9.	Signal inversion, all channels	Yes_____	No_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: DRIVE RATE TEST 4 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

60A06

ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: -X IRIG, +Y IRIG, and +Z IRIG.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv), 8 dummy loads (200 ohm, 4 on female pins, 4 on male); counter (Beckman model 6146 with Extender Model 602 or equiv)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

RST IRIG	J2Y and J2Z
+X IRIG	J2F and J2G
+Y IRIG	J1X and J1W
+Z IRIG	J2k and J2j.

2. Ground J2Z, G, j, and J1W.

3. Ground scope to Simulator chassis and monitor:

   J2Y on channel A
   J2F on channel B
   J1X on channel C
   J2k on channel D.

4. Sync scope on J2Y.

5. Set POLARITY switch to + and DRIVE SELECT switch to X IRIG. Observe channel B delayed from A approximately 5 μsec. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

6. Set DRIVE SELECT switch to Y IRIG. Observe channel C delayed from A approximately 5 μsec. Record.

7. Set DRIVE SELECT switch to Z IRIG. Observe channel D delayed from A approximately 5 μsec. Record.

8. Set IRIG RESET INHIBIT switch to INHIBIT. Monitor scope for absence of signal on channel A. Record.

9. Return IRIG RESET INHIBIT switch to NORMAL.

10. Measure the following signal characteristics, using DRIVE SELECT switch as necessary to enable signals on channels B, C, and D and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

11. Reverse all ground and scope inputs. Observe presence of inverted signals on all channels as selected by DRIVE SELECT switch. Record.

12. Return grounds to original configuration and remove scope probes.

13. Connect START counter input to J2Y and J2Z.

14. Connect counter STOP to J2F and J2G and measure time interval (10-nanosecond resolution) of 4.9 ± 0.2 μsec. (DRIVE SELECT switch in X IRIG position.) Record.

15. Repeat step 14 for +Y IRIG and J1X. Record.

16. Repeat step 14 for +Z IRIG and J2k. Record.

17. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04097
REV. A
INITIAL TDRR 11119

JOB: DRIVE RATE TEST 4 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME ____ SER. NO. ____ CAL DATE ____

NAME ____ SER. NO. ____ CAL DATE ____

CONDUCTED BY ____ (NAME/AFFILIATION) APPROVED BY ____ (NAME/AFFILIATION)

		Yes	No
5.	Channel B delayed from A approx 5 μsec		
6.	Channel C delayed from A approx 5 μsec		
7.	Channel D delayed from A approx 5 μsec		
8.	Absence		
10.	Channel B characteristics (+X IRIG)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v
	Channel C characteristics (+Y IRIG)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v
	Channel D characteristics (+Z IRIG)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v
11.	Signal inversion, all channels	Yes	No
14.	Time interval A to B		4.9 ± 0.2 μsec
15.	Time interval A to C		4.9 ± 0.2 μsec
16.	Time interval A to D		4.9 ± 0.2 μsec

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04098 REV: A PAGE 1 OF 2

JOB: DRIVE RATE TEST 5 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: -X IRIG, -Y IRIG, and -Z IRIG.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv), 8 dummy loads (200 ohm, 4 on female pins, 4 on male); counter (Beckman model 6146 with extender model 602 or equiv)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

RST IRIG	J2Y and J2Z
-X IRIG	J2K and J2L
-Y IRIG	J2n and J2m
-Z IRIG	J2p and J2q.

2. Ground J2Z, L, m, and q.

3. Ground scope to Simulator chassis and monitor:

   J2Y on channel A
   J2K on channel B
   J2n on channel C
   J2p on channel D.

4. Sync scope on J2Y.

5. Set POLARITY switch to - and DRIVE SELECT switch to X IRIG. Observe channel B delayed from A approximately 5 μsec. **Record.**

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

6. Repeat step 5 for Y IRIG and channel C. Record.
7. Repeat step 5 for Z IRIG and channel D. Record.
8. Measure the following signal characteristics, using DRIVE SELECT switch as necessary to enable signals on channel B, C, and D and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

9. Reverse all grounds and scope inputs. Observe presence of inverted signals on all channels as selected by DRIVE SELECT switch. Record.
10. Return grounds to original configuration and remove scope probes.
11. Connect counter START input to J2Y and J2Z.
12. Connect counter STOP to J2K and J2L and measure time interval (10-nanosecond resolution) of 4.9 ± 0.2 μsec. (DRIVE SELECT switch to X IRIG position.) Record.
13. Repeat step 12 for J2n and J2m and Y IRIG. Record.
14. Repeat step 12 for J2p and J2q and Z IRIG. Record.
15. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04098
REV. A
INITIAL TDRR 11119

JOB: DRIVE RATE TEST 5 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. ____ CAL DATE ____

NAME _____ SER. NO. ____ CAL DATE ____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

		Yes	No
5.	Channel B delayed from A approx 5 μsec		
6.	Channel C delayed from A approx 5 μsec		
7.	Channel D delayed from A approx 5 μsec		
8.	Channel B characteristics (-X IRIG)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v
	Channel C characteristics (-Y IRIG)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v
	Channel D characteristics (-Z IRIG)		
	Amplitude		5.0 ± 0.5 vpp
	Width		3.0 ± 0.5 μsec
	Rise time		NMT 0.2 μsec
	Droop		NMT 0.6 v
9.	Signal inversion, all channels	Yes	No
12.	Channel B delayed from A		4.9 ± 0.2 μsec
13.	Channel C delayed from A		4.9 ± 0.2 μsec
14.	Channel D delayed from A		4.9 ± 0.2 μsec

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04099 REV: A PAGE 1 OF 2

JOB: DRIVE RATE TEST 6 (FIELD) — INITIAL TDRR 11119 — D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator — ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: +X OPT and +Y OPT.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

RST OPT	J2X and J2W
+X OPT	J1C and J1B
+Y OPT	J1p and J1q.

2. Ground J2W, J1B, and J1q.

3. Ground scope to simulator chassis and monitor:

   J2X on channel A
   J1C on channel B
   J1p on channel C.

4. Sync scope on J2X.

5. Set POLARITY switch to + and DRIVE SELECT switch to X OPT. Observe channel B delayed from A 2.0 ± 0.2 μsec. Record.

6. Repeat step 5 for Y OPT and channel C. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Measure the following signal characteristics of channels B and C, using DRIVE SELECT switch as necessary to enable the appropriate channel and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

8. Reverse all grounds and scope inputs. Observe presence of inverted signals on all channels as selected by DRIVE SELECT switch. Record.

9. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04099
REV. A
INITIAL TDRR 11119

JOB: DRIVE RATE TEST 6 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. _____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5.	Channel B delayed from A	_____	2.0 ± 0.2 μsec
6.	Channel C delayed from A	_____	2.0 ± 0.2 μsec
7.a	Channel B characteristics (+X OPT)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.b	Channel C characteristics (+Y OPT)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
8.	Signal inversion, all channels	Yes_____	No_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: DRIVE RATE TEST 7 (FIELD) | INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator | ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: -X OPT and -Y OPT.

Rev. Let.	Date	TDRR NO.	PAGES REVISED JDC	PAGES REVISED D.S.	APPROVAL MIT	APPROVAL NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

RST OPT	J2X and J2W
-X OPT	J1j and J1k
-Y OPT	J1n and J1m.

2. Ground J2W, J1k, and J1m.

3. Ground scope to Simulator chassis and monitor:

   J2X on channel A
   J1j on channel B
   J1n on channel C.

4. Sync scope on J2X.

5. Set POLARITY switch to - and DRIVE SELECT switch to X OPT. Observe channel B delayed from A 2.0 ± 0.2 μsec. Record.

6. Repeat step 5 for Y OPT and channel C. Record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Measure the following signal characteristics on channels B and C, using DRIVE SELECT switch as necessary to enable the appropriate channel and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

8. Reverse all grounds and scope inputs. Observe presence of inverted signals on all channels as selected by DRIVE SELECT switch. Record.

9. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04100
REV. - A
INITIAL TDRR 1119

JOB: DRIVE RATE TEST 7

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME ____ SER. NO. ____ CAL DATE ____

NAME ____ SER. NO. ____ CAL DATE ____

CONDUCTED BY ____ (NAME/AFFILIATION) APPROVED BY ____ (NAME/AFFILIATION)

5.	Channel B delayed from A	____	2.0 ± 0.2 μsec
6.	Channel C delayed from A	____	2.0 ± 0.2 μsec
7.	Channel B characteristics (-X OPT)		
	Amplitude	____	5.0 ± 0.5 vpp
	Width	____	3.0 ± 0.5 μsec
	Rise time	____	NMT 0.2 μsec
	Droop	____	NMT 0.6 v
	Channel C characteristics (-Y OPT)		
	Amplitude	____	5.0 ± 0.5 vpp
	Width	____	3.0 ± 0.5 μsec
	Rise time	____	NMT 0.2 μsec
	Droop	____	NMT 0.6 v
8.	Signal inversion, all channels	Yes____	No____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: PIPA CLOCK AND PIPA SET TEST (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

Ground Support Equipment - 60A06

SUBSYSTEM: AGC Simulator

ASSY: 1041061-000 and 1040161-011

DESCRIPTION:

The pulse characteristics and timing relationships of the following signals are checked: PIPA CLK and PIPA SET.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); proves (4, Tektronix P6000x10 or equiv), 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

PIPA CLK	J1J and J1H
PIPA SET	J1M and J1N.

2. Ground J1H and J1N.

3. Ground scope to Simulator chassis and monitor:

   J1M on channel A.
   J1J on channel B.

4. Sync scope on J1J with J1H to ground.

5. Observe channel B delayed from A by 2.0 ± 0.2 μsec. Record.

6. Measure the following signal characteristics on both channels and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Reverse all grounds and scope inputs. Observe presence of inverted signals on both channels. Record.

8. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04101
REV. A
INITIAL TDRR 11119

JOB: PIPA CLOCK AND PIPA SET TEST (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5.	Channel B delayed from A	_____	2.0 ± 0.2 μsec
6.	Channel A characteristics (PIPA CLK)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
	Channel B characteristics (PIPA SET)		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.	Signal inversion, all channels	Yes_____	No_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04102 REV: A PAGE 1 OF 2

JOB: EXTERNAL TIME BASE TEST 1 (FIELD) — INITIAL TDRR 11119 — D.S. PGS. 1

Ground Support Equipment - 60A06

SUBSYSTEM: AGC Simulator — ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of signal EXT TB1 are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male pins)

PROCEDURE: Perform the following procedures and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

EXT TB1	J4b and J4a
PIPA SET	J1M and J1N.

2. Ground J4a and J1N.

3. Ground scope to simulator chassis and monitor:

   J4b on channel A
   J1M on channel B.

4. Sync scope on channel A.

5. Check for coincidence of the two signals. Record.

6. Measure the following signal characteristics on channel A and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Reverse all grounds and scope inputs. Observe presence of inverted signals on both channels. Record.

8. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04102
REV. A
INITIAL TDRR 11119

JOB: EXTERNAL TIME BASE TEST 1 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME ____ SER. NO. ____ CAL DATE ____

NAME ____ SER. NO. ____ CAL DATE ____

CONDUCTED BY ____ (NAME/AFFILIATION) APPROVED BY ____ (NAME/AFFILIATION)

5. Coincidence — Yes ____ No ____
6. Channel A characteristics (EXT TB1)

Amplitude	____	5.0 ± 0.5 vpp
Width	____	3.0 ± 0.5 μsec
Rise time	____	NMT 0.2 μsec
Droop	____	NMT 0.6 v

7. Signal inversion, all channels — Yes ____ No ____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04103 REV: A PAGE 1 OF 2

JOB: EXTERNAL TIME BASE TEST 2 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of signal EXT TB2 are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED JDC	PAGES REVISED D.S.	APPROVAL MIT	APPROVAL NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04035 and 04036 must be completed before this procedure is performed.

INTERVAL:
Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

EXT TB2	J3j and J3k
3200 A	J1b and J1a.

2. Ground J3k and J1a.

3. Ground scope to simulator chassis and monitor:

   J3j on channel A
   J1b on channel B.

4. Sync scope on channel A.

5. Check that channel B signal is coincident with channel A but occuring at twice the rate. Record.

6. Measure the following signal characteristics on channel A and record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

7. Reverse all grounds and scope inputs. Observe presence of inverted signals on both channels. Record.

8. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04103
REV. A
INITIAL TDRR 11119

JOB: EXTERNAL TIME BASE TEST 2 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5. Coincidence and rate Yes____ No____
6. Channel A charactertics (EXT TB2)

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion, both channels Yes_____ No_____

VERIFICATION WITH SIDL
REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04104 REV: A PAGE 1 OF 2

JOB: EXTERNAL TIME BASE TEST 3 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

60A06

ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The pulse characteristics and timing relationships of signals EXT TB3 and 800B are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

EXT TB3	J3h and j3i
800B	J1U and J1V.

2. Ground J3i and J1V.

3. Ground scope to simulator chassis and monitor:

   J3h on channel A
   J1U on channel B.

4. Sync scope on channel A.

5. Check for coincidence of the two signals. Record.

6. Measure the following signal characteristics on both channels and record.

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

7. Reverse all grounds and scope inputs. Observe presence of inverted signals on both channels. Record.

8. Remove loads, grounds, and jumper. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04104
REV. A
INITIAL TDRR 11119

JOB: EXTERNAL TIME BASE TEST 3 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

5. Coincidence Yes_____ No_____
6. Channel A characteristics (EXT TB3)

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

Channel B characteristics (800B)

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion, both channels Yes_____ No_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: BUFFER TESTS (FIELD) | INITIAL TDRR 11119 D.S. PGS. 5

SUBSYSTEM: Ground Support Equipment - AGC Simulator | ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:
System transformer drivers are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED JDC	PAGES REVISED D.S.	APPROVAL MIT	APPROVAL NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL:
Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

NOTE: In this test 16 separate circuits are to be examined. In order to reduce procedural complexity, the testing of one such circuit is defined followed by a list of input/output pins each of which should be tested in the same manner.

1. Insert a jumper from J4A to J4e and place a load across J3U (+IG ENC) to J3V. Ground J3V. NOTE: Make sure POLARITY switch is set to either + or -.
2. Jumper J4h to J1S and J4i to J1T. Ground J4i.
3. Ground scope to simulator chassis and monitor:

   J4h on channel A
   J3U on channel B.

   NOTE: J4h should be monitored on channel A for all 16 tests.
4. Sync scope on J4b with J4a to ground.
5. Observe that channel B signal occurs at the same rate as channel A signal (coincidence not necessary). Record.
6. Measure characteristics of signal on channel B and record.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

7. Reverse ground and scope input connections on J3U and J3V. Observe presence of inverted signal on channel B. Record.

8. Remove load.

9. Repeat the above procedure for each of the following signals. Record for each signal.

Buffer Name	Jumper J4h to	Jumper J4i to	Output	Ground
-IG	J2h	J2i	J3W	J3X
+MG	J2U	J2V	J3Y	J3Z
-MG	J2f	J2g	J3a	J3b
+OG	J1f	J1g	J3m	J3n
-OG	J1P	J1R	J4F	J4G
+ΔVX	J1s	J1u	J3F	J3G
-ΔVX	J2EE	J2FF	J3H	J3J
+ΔVY	J1x	J1r	J3K	J3L
-ΔVY	J2y	J2z	J3M	J3N
+ΔVZ	J2AA	J2BB	J3P	J3R
-ΔVZ	J2CC	J2DD	J4j	J4k
+XOP	J2a	J2b	J3c	J3d
-XOP	J1DD	J1EE	J3f	J3g
+YOP	J1FF	J1GG	J3B	J3C
-YOP	J1CC	J1HH	J3D	J3E

10. Remove loads, jumpers, and grounds. (Leave jumper from J4A to J4e installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 5

JDC
NO. 04105
REV. A
INITIAL TDRR 11119

JOB: BUFFER TESTS (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. _____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

+IG ENC

5.	B rate equals A rate	Yes_____	No_____
6.	Channel B characteristics		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.	Signal inversion	Yes_____	No_____

-IG ENC

5.	B rate equals A rate	Yes_____	No_____
6.	Channel B characteristics		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.	Signal inversion	Yes_____	No_____

+MG ENC

5.	B rate equals A rate	Yes_____	No_____
6.	Channel B characteristics		

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v
7. Signal inversion	Yes_____	No_____

-MG ENC

5. B rate equals A rate	Yes_____	No_____
6. Channel B characteristics		
Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v
7. Signal inversion	Yes_____	No_____

+OG ENC

5. B rate equals A rate	Yes_____	No_____
6. Channel B characteristics		
Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v
7. Signal inversion	Yes_____	No_____

-OG ENC

5. B rate equals A rate	Yes_____	No_____
6. Channel B characteristics		
Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v
7. Signal inversion	Yes_____	No_____

+ΔVX

5. B rate equals A rate	Yes_____	No_____

6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

-ΔVX

5. B rate equals A rate Yes_____ No_____
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

+ΔVY

5. B rate equals A rate Yes_____ No_____
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

-ΔVY

5. B rate equals A rate Yes_____ No_____
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

+ΔVZ

JDC
NO. 04105
REV. A

JOB: BUFFER TESTS (FIELD)

5. B rate equals A rate
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

-ΔVZ

5. B rate equals A rate Yes_____ No_____
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

+X ENC OP

5. B rate equals A rate
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

-X ENC OP

5. B rate equals A rate Yes_____ No_____
6. Channel B characteristics

Amplitude	_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

7. Signal inversion Yes_____ No_____

DATE 21 July 64

JDC
NO. 04105
REV. A

JOB: BUFFER TESTS (FIELD)

+Y ENC OP

5.	B rate equals A rate	Yes_____	No_____
6.	Channel B characteristics		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.	Signal inversion	Yes_____	No_____

-Y ENC OP

5.	B rate equals A rate	Yes_____	No_____
6.	Channel B characteristics		
	Amplitude	_____	5.0 ± 0.5 vpp
	Width	_____	3.0 ± 0.5 μsec
	Rise time	_____	NMT 0.2 μsec
	Droop	_____	NMT 0.6 v
7.	Signal inversion	Yes_____	No_____

DATE 21 July 64

JDC: 04106 REV: A PAGE 1 OF 2

JOB: BURST CONTENT TESTS (FIELD) | INITIAL TDRR 11119 D.S. PGS. 1

Ground Support Equipment - | 60A06

SUBSYSTEM: AGC Simulator | ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The generation of a selected number of drive pulses in the proper mode is checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male); counter (Beckman model 6146 with extender model 602 or equiv)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place a load across J2p and J2q.
2. Ground J2q.
3. Set up counter for totaling count and connect J2p to counter input.
4. Set up the following condition on the front panel of the simulator:

DRIVE SELECT	Z IRIG
POLARITY	- (minus)
PULSES/BURST	1
BURST	SINGLE BURST.

All other switches to OFF or NORMAL.

5. Adjust the counter for a count of 1 by repeatedly pushing SINGLE BURST START.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

6. Rotate PULSES/BURST switch through each of its positions, depressing SINGLE BURST START at each position. Observe counter readout corresponding to the number of pulses per burst selected (1 - 256). Record

7. Remove load, jumper, and ground. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04106
REV. A
INITIAL TDRR 11119

JOB: BURST CONTENT TEST (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. _____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

	Switch Position		
6. PULSES/BURST	1	_____	1
	2	_____	2
	4	_____	4
	8	_____	8
	16	_____	16
	32	_____	32
	64	_____	64
	128	_____	128
	256	_____	256

VERIFICATION WITH SIDL
REQUIRED BEFORE USE

DATE 21 July 64

JOB: IRIG TEST 1 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The generation of a selected number of drive pulses in the proper mode is checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10, or equiv), 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

+OG	J2C and J2B
+X IRIG	J2F and J2G
+Y IRIG	J1X and J1W
+X OPT	J1C and J1B

2. Ground J2B, J2G, J1W, and J1B.

3. Ground scope to Simulator chassis and monitor:

   J2C on channel A
   J2F on channel B
   J1X on channel C
   J1C on channel D.

4. Sync scope on J4h with j4i to ground.

5. Set DRIVE SELECT switch to CDU OG, POLARITY switch to +, PULSES/BURST switch to 4, BURST switch to STEADY BURST, and all other switches to OFF or NORMAL.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

6. Observe four CDU pulses per burst on channel A. Bursts should occur approximately every 240 msec. Record.

7. Select X IRIG. Observe four IRIG pulses per burst on channel B. Bursts should occur approximately every 240 msec. Record.

8. Select Y IRIG. Observe four IRIG pulses per burst on channel C. Bursts should approximately every 240 msec. Record.

9. Select X OPT. Observe four OPT pulses per burst on channel D. Bursts should occur approximately every 240 msec. Record.

10. Remove loads, jumper, and grounds. (Leave jumper installed if further tests are to be performed).

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04107
REV. A
INITIAL TDRR 11119

JOB: IRIG TEST 1 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE ____ (START) ____ (END) ____ (SITE/LOCATION)
SER. NO. ____ DWG. ____ REV. ____	TIME ____ (START) ____ (END) ____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME ____ SER. NO. ____ CAL DATE ____

NAME ____ SER. NO. ____ CAL DATE ____

CONDUCTED BY ____ (NAME/AFFILIATION) APPROVED BY ____ (NAME/AFFILIATION)

6.	Channel A pulses	____	4
	Interval	____	240 msec
7.	Channel B pulses	____	4
	Interval	____	240 msec
8.	Channel C pulses	____	4
	Interval	____	240 msec
9.	Channel D pulses	____	4
	Interval	____	240 msec

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04108 REV: A PAGE 1 OF 2

JOB: IRIG TEST 2 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION:

The generation of a selected number of drive pulses in the proper mode is checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04085 and 04086 must be completed before this procedure is performed.

INTERVAL:
Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4 Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male); one-shot pushbutton switch (Minneapolis Honeywell 201 ED2 or equiv); power supply for one shot.

PROCEDURE: Perform the following procedure and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

   +X IRIG J2F and J2G
   +Y IRIG J1X and J1W
   +Z IRIG J2k and J2j.

2. Ground J2G, J1W and j2j.

3. Ground scope to simulator chassis and monitor.

   J2F on channel A
   J1X on channel B
   J2k on channel C

4. Sync scope on channel A.

5. On front panel of Simulator select -X IRIG, 2 pulses per burst, and SINGLE BURST mode.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

6. Depress SINGLE BURST START. BIAS REQD lamp should glow. Record.
7. Depress IRIG BIAS push button. BIAS REQD lamp should extinguish. Observe two pulses occurring simultaneously on all three channels. Record.
8. Depress SINGLE BURST START. BIAS REQD lamp should glow. Record.
9. Using one-shot pushbutton switch, apply an externally generated +12 vdc, ≥ 1 μsec < 2.5 msec, to pin J3AA (use J3FF for return line). BIAS REQD lamp should extinguish. Observe two pulses occurring simultaneously on all three channels. Record.
10. Remove loads, jumper, and grounds. (Leave jumper installed if further tests are to be performed.)

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04108
REV. A
INITIAL TDRR _____

JOB: IRIG TEST 2 (FIELD)

ASSEMBLY UNDER TEST

TITLE AGC Simulator

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ _____ (CAL DATE)

NAME _____ SER. NO. _____ _____ (CAL DATE)

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

6.	Bias REQD lamp ON	Yes_____	No_____
7.	BIAS REQD lamp OFF	Yes_____	No_____
	Channel A pulses	_____	2
	Channel B pulses	_____	2
	Channel C pulses	_____	2
8.	BIAS REQD lamp ON	Yes_____	No_____
9.	BIAS REQD lamp OFF	Yes_____	No_____
	Channel A pulses	_____	2
	Channel B pulses	_____	2
	Channel C pulses	_____	2

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04109 REV: A PAGE 1 OF 1

JOB: IRIG TEST 3 (FIELD)

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

60A06

ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The generation of a selected number of pulses in the proper mode is checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA

REFERENCES:

IMPORTANT: JDC's 04084, 04085, and 04108 should be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: JDC 04108 Oscilloscope (Tektronix 545A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male); JDC 04108; one shot pushbutton switch (Honeywell 201 ED2 or equiv), power supply for one-shot.

PROCEDURE: Perform the following operations and record the results.

1. Insert a jumper from J4A to J4e and place loads across:

   -X IRIG J2K and J2L
   -Y IRIG J2n and J2m
   -Z IRIG J2p and J2q.

2. Ground J2L, J2m, and J2q.

3. Ground scope to simulator chassis and monitor:

   J2K on channel A
   J2n on channel B
   J2p on channel C.

4. Sync scope on channel A.

5. Repeat steps 5 through 10 of JDC 04108.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04109
REV. A
INITIAL TDRR 11119

JOB: IRIG TEST 3 (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

6.	BIAS REQD lamp ON	Yes_____	No_____
7.	BIAS REQD lamp OFF	Yes_____	No_____
	Channel A pulses	_____	2
	Channel B pulses	_____	2
	Channel C pulses	_____	2
8.	BIAS REQD lamp ON	Yes_____	No_____
9.	BIAS REQD lamp OFF	Yes_____	No_____

VERIFICATION WITH SIDL
REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04110 REV: A PAGE 1 OF 1

JOB: MISCELLANEOUS SIMULATOR TESTS(FIELD | INITIAL TDRR 11119 D.S. PGS. 1

Ground Support Equipment - | 60A06

SUBSYSTEM: AGC Simulator | ASSY: 1014061-000 and 1014061-011

DESCRIPTION:

The presence of +3 vdc and the pulse characteristics of signal 800A are checked.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: JDC's 04084, 04085, and 04108 should be completed before this procedure is performed.

INTERVAL: Every 60 days.

TOOLS AND MATERIAL: Oscilloscope (Tektronix 535A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE: Perform the following operations and record the results.

1. Insert a jumper from J4A to J4e.
2. Check for presence of +13 vdc on pin J4y and +3 vdc on J3CC, using scope. Record.
3. Place a load across J1D and J1E.
4. Ground J1E.
5. Ground scope to simulator chassis and monitor J1D on channel A.
6. Sync scope on channel A.
7. Measure the following signal characteristics and record:

Pulse amplitude	5.0 ± 0.5 vpp
Pulse width	3.0 ± 0.5 μsec
Pulse rise time	NMT 0.2 μsec
Pulse droop	NMT 0.6 v.

8. Reverse ground and scope input. Observe presence of inverted signal. Record.
9. Remove load, ground, and jumper.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04110
REV. A
INITIAL TDRR 11119

JOB: MISCELLANEOUS SIMULATOR TESTS (FIELD)

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. _____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

2. Presence check only

+13 VDC	Yes_____	No_____
+3 VDC	Yes_____	No_____

7. Channel A characteristics (800A)

Amplitude	Yes_____	5.0 ± 0.5 vpp
Width	_____	3.0 ± 0.5 μsec
Rise time	_____	NMT 0.2 μsec
Droop	_____	NMT 0.6 v

8. Signal inversion Yes_____ No_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JOB: MALFUNCTION ANALYSIS FOR PRELIMINARY TURN-ON

JDC: 04131 REV: A PAGE 1 OF 2

INITIAL TDRR 11119 D.S. PGS. -

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION: A procedure to isolate malfunctions to the module level through the utilization of Boolean equations is provided.

Rev. Let.	Date	TDRR NO.	PAGES REVISED JDC	PAGES REVISED D.S.	APPROVAL MIT	APPROVAL NASA
A	8-9-65	17371	All	All	WK	WR

REFERENCES:

IMPORTANT: Only for JDC 04086

INTERVAL:

TOOLS AND MATERIAL: VTVM (John Fluke model 803B or equivalent)

PROCEDURE:

1. Isolate the pertinent malfunction to the module, using the table below as a guide in isolation analysis.
2. Replace the defective module.

Equation	Signal Origin: Signal	Signal Origin: Module	NASA Drawing 1014063: Sheet	NASA Drawing 1014063: Location
1 Bias Reqd (lamp on) = IRIG Bias Reset	Bias Reqd Sig IRIG Bias Reset	3A21MK 3A8AC	5 5	A3 A4
1a IRIG Bias Reset = +3V	+3V	Relay K2 (NASA DWG 1014098)	-	-

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
2				
IRIG Bias Has Operated (lamp out)	IRIG Bias Has Operated	3A20KH	5	A3
= Test Signal No. 4 + $\overline{\text{DRIVE RATE}}$ + SBII	Test Signal No. 4	2A20KH	3	D5
	$\overline{\text{DRIVE RATE}}$	1B23AC	2	C2
	SBII	1B20AC,	1	B3
		1B21AC	1	B3
2a				
DRIVE RATE = $\overline{\text{F5}} + \overline{\text{F4D}}$	$\overline{\text{F5}}$	1B12KH	2	C3
	$\overline{\text{F4D}}$	1A19AC	2	C5
2b				
SBII = $\overline{\text{F01}}$ + F04 + T1	$\overline{\text{F01}}$	1B25KH	1	C4
	F04	1A24KH	1	C3
	T1	3A19FD	5	C2
3				
Scaler Monitor (lamp on) = F13A · S13 on	Scaler Monitor	1A4MK	2	2A
	F13A	1B18KH	2	3A
	S13 on		2	2A

DATE 21 July 64

JOB: MALFUNCTION ANALYSIS FOR FREQUENCY CHECK OF CONTINUOUS OUTPUTS

JDC: 04132 REV: A PAGE 1 OF 4

INITIAL TDRR 11119 D.S. PGS. -

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION: A procedure to isolate malfunctions to the module level through the utilization of Boolean equations is provided.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES: JDC 04088

IMPORTANT:

INTERVAL:

TOOLS AND MATERIAL: Counter (Beckman model 6146 with extender model 602 or equivalent)

PROCEDURE:

1. Isolate the pertinent malfunction to the module, using the table below as a guide in isolation analysis.
2. Replace the defective module.

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
1 102.4 KC (SBII) = $\overline{F01}$ + F04 + TI	102.4 KC	1B20AC	1	B3
	$\overline{F01}$	1B25KH	1	C4
	F04	1A24KH	1	C3
	TI	Switch S 3	5	D1

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
2 25.6 KC(A) = $\overline{\text{F2A}}$ + $\overline{\text{SBI}}$	25.6 KC(A) $\overline{\text{F2A}}$ $\overline{\text{SBI}}$	1A8AC 1B11AC 1B8AC	1 2 1	C3 D3 C3
2a SBI = F02 + F04 + TI	F02 F04 TI	1A25KH 1A24KH Switch S-3	1 1 5	C4 C3 D1
3 25.6 KC(B) = $\overline{\text{F2B}}$ + $\overline{\text{SBI}}$	25.6 KC(B) $\overline{\text{F2B}}$ $\overline{\text{SBI}}$	1A8AC 1A9AC 1B8AC	1 2 1	B3 D3 C3
3a SBI = F02 + F04 + TI	See 2a above			
4 12.8 KC(A) = $\overline{\text{F3A}}$ + $\overline{\text{SBI}}$	12.8 KC(A) $\overline{\text{F3A}}$ $\overline{\text{SBI}}$	1A8AC 1B11AC 1B8AC	1 2 1	B3 D2 C3
4a SBI = F02 + F04 + TI	See 2a above			
5 3200 PPS(A) = $\overline{\text{F5A}}$ + $\overline{\text{SBI}}$	3200 PPS(A) $\overline{\text{F5A}}$ $\overline{\text{SBI}}$	1A7AC 1B13A 1B8AC	1 2 1	B3 C3 B3
5a SBI = F02 + F04 + TI	See 2a above			

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
6 3200 PPS(B) = $\overline{F5B}$ + $\overline{SBI}$	3200 PPS(B) $\overline{F5B}$ $\overline{SBI}$	1A7AC 1B13AC 1B8AC	1 2 1	B3 C3 B3
6a SBI = F02 + F04 + TI	See 2a above			
7 800 PPS(A) = $\overline{F7A}$ + $\overline{SBI}$	800 PPS(A) $\overline{F7A}$ $\overline{SBI}$	1A7AC 1B21AC, 1A13AC 1B8AC	1 2 1	A3 C1 B3
7a SBI = F02 + F04 + TI	See 2a above			
8 800 PPS(B) = $\overline{F7B}$ + $\overline{SBI}$	800 PPS(B) $\overline{F7B}$ $\overline{SBI}$	1A7AC 1A13AC 1B8AC	1 2 1	A3 C1 B3
8a SBI = F02 + F04 + TI	See 2a above			
9 PIPA Clock = $\overline{\text{DRIVE RATE}}$ + $\overline{SBII}$	PIPA Clock $\overline{\text{DRIVE RATE}}$ $\overline{SBII}$	3B19AC 1B23AC 1B20AC	5 2 1	D3 C2 B3
9a DRIVE RATE = $\overline{F5}$ + $\overline{F4D}$	$\overline{F5}$ $\overline{F4D}$	1B12KH 1A9AC	2 2	C3 C5
9b SBII = $\overline{F01}$ + F04 + TI	See 1 above			

DATE 21 July 64

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
10 $\overline{\text{PIPA INT}} = \overline{\text{DRIVE}}$ $\overline{\text{RATE}} + \overline{\text{SBI}}$	$\overline{\text{PIPA INT}}$ $\overline{\text{DRIVE RATE}}$ $\overline{\text{SBI}}$	3B17AC 1B23AC 1B8AC	5 2 1	D3 C2 B3
10a $\text{DRIVE RATE} = \overline{\text{F5}} + \overline{\text{F4D}}$	See 9a above			
10b SBI = F02 + F04 +TI	See 2a above			

JOB:	MALFUNCTION ANALYSIS FOR CLOCK AND SCALER TEST 1	JDC: 04134 REV: A PAGE 1 OF 3 INITIAL TDRR 11119 D.S. PGS.
SUBSYSTEM:	Ground Support Equipment AGC Simulator	60A06 ASSY: 1014061-000 and 1014061-011

DESCRIPTION: A procedure to isolate malfunctions to the module level through the utilization of Boolean equations is provided.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES: JDC 04090

IMPORTANT:

INTERVAL:

TOOLS AND MATERIAL: Oscilloscope (Tektronix 535A, Type M preamplifier, or equiv); probes (4, Tektronix P60000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male

PROCEDURE:

1. Isolate the pertinent malfunction to the module, using the table below as a guide in isolation analysis.
2. Replace the defective module.

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
1 $25.6\ KC(A) = \overline{F2A} + \overline{SBI}$	25.6 KC(A)	1A8AC	1	C3
	$\overline{F2A}$	1B11AC	2	D3
	$\overline{SBI}$	1B8AC	1	C3
1a SBI = F02 + F04 + TI	F02	1A25KH	1	C4
	F04	1A24KH	1	C3
	TI	Switch S-3	5	D1

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
2				
+OG CDU SET = OG CDU [+DRIVE (DDR 1 + $\overline{\text{EXT INH}}$)] SBR No. 1	+OG CDU SET	2A13AC	4	D3
	OG CDU	Switch S-11	4	C5
	[+DRIVE ($\overline{\text{DDR 1}}$ + $\overline{\text{EXT INH}}$)]	2B17AC	3	B3
	+DRIVE	Switch S-10	3	B5
	DDR 1	Switch S-4	3	C5
	SBR No. 1	2A14AC	3	A4
2a				
SBR No. 1 = $\overline{\text{DRIVE RATE}}$ + $\overline{\text{SBII}}$ + Burst Gate	$\overline{\text{DRIVE RATE}}$	1B23AC	2	C2
	$\overline{\text{SBII}}$	1B20AC	1	B3
	Burst Gate	3A11AC	5	C2
2a.1				
DRIVE RATE = $\overline{\text{F5}}$ + $\overline{\text{F4D}}$	$\overline{\text{F5}}$	1B12KH	2	C3
	$\overline{\text{F4D}}$	1A9AC	2	C5
2a.2				
SBII = F01 + F04 + TI	$\overline{\text{F01}}$	1B25KH	1	C4
	F04	1A24KH	1	C3
	TI	Switch S-3	5	D1
2a.3				
Burst Gate = $\overline{\text{BURST}}$ + END BURST	$\overline{\text{BURST}}$	3A10AC	5	D2
	END BURST	3A11AC	5	C2
2a.3.1				
$\overline{\text{BURST}}$ = Single Burst + Steady Burst	Single Burst	Switch S-8	5	D5
	Steady Burst	Switch S-8	5	D5

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
3				
102.4 KPPS = $\overline{F01}$ + F04 + TI	102.4 KPPS	1B20AC	1	B3
	$\overline{F01}$	1B25KH	1	C4
	F04	1A24KH	1	C3
	TI	Switch S-3	5	D1
4				
512 KC = C2 + TI	512 KC	3A11AC	5	C3
	C2	1B27KH	1	D2
	TI	Switch S-3	5	D1

JOB: MALFUNCTION ANALYSIS FOR BUFFER TESTS	JDC: 04149 REV: A PAGE 1 OF 3 INITIAL TDRR 11119 D.S. PGS. –
SUBSYSTEM: Ground Support Equipment - AGC Simulator	ASSY: 1014061-000 and 1014061-011

DESCRIPTION: A procedure to isolate malfunctions to the module level through tne utilization of Boolean equations is provided.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	A11	-	WK	WR

REFERENCES: JDC 04105

IMPORTANT:

INTERVAL:

TOOLS AND MATERIAL: Oscilloscope (Tektronix 535A, Type M preamplifier or equiv); probes (4, Tektronix P6000x10 or equiv); 8 dummy loads (200 ohm, 4 on female pins, 4 on male)

PROCEDURE:

1. Isolate the pertinent malfunction to the module, using the table below as a guide in isolation analysis.

2. Replace the defective module.

3. Use Table A as a guide in isolating the buffer modules.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE _____

Table A

Buffer Name	Modules	NASA Drawing	
		Sheet	Location
+IG CDU ENC	1B6DA and 1B4CR	1	B4
-IG CDU ENC	1B6DA and 1B4CR	1	B4
+MG CDU ENC	1A26DA and 1A22CR	1	B4
-MG CDU ENC	1A26DA and 1A22CR	1	B4
+OG CDU ENC	1B5DA and 1B4CR	1	B4
-OG CDU ENC	1B5DA and 1B4CR	1	B4
+ΔVX PIPA	2B27DA and 2A27CR	3	D2
-ΔVX PIPA	2B27DA and 2A27CR	3	D2
+ΔVY PIPA	3B21DA and 3B20CR	6	C4
-ΔVY PIPA	3B21DA and 3B20CR	6	C4
+ΔVZ PIPA	3B22DA and 3B20CR	6	C4
-ΔVZ PIPA	3B22DA and 3B20CR	6	C4
+X OPT ENC	1B22DA and 1A22CR	1	A4
-X OPT ENC	1B22DA and 1A22CR	1	A4
+Y OPT ENC	2A26DA and 2A27CR	3	D2
-Y OPT ENC	2A26DA and 2A27CR	3	D2

DATE _____

Equation	Signal Origin		NASA Drawing 1014063	
	Signal	Module	Sheet	Location
1 PDR (J4-h and J4-i) = SBR No. 1 (±DRIVE)	PDR SBR No. 1 ± DRIVE	2A18AC 2A14AC Switch S10	3 3 3	B3 A4 B5
1a Single Burst Reset No. 1 = $\overline{\text{DRIVE RATE}}$ + Burst Gate + $\overline{\text{SBII}}$	$\overline{\text{DRIVE RATE}}$ Burst Gate $\overline{\text{SBII}}$	1B23AC 3A11AC 1B20AC	2 5 1	C2 C2 B3
1a.1 DRIVE RATE = $\overline{\text{F5}}$ + $\overline{\text{F4D}}$	$\overline{\text{F5}}$ $\overline{\text{F4D}}$	1B12KH 1A9AC	2 2	C3 C5
1a.2 SBII = $\overline{\text{F01}}$ + F04 + T1	$\overline{\text{F01}}$ F04 T1	1B25KH 1A24KH Switch S-3	1 1 5	C4 C3 D1
1a.3 Burst Gate = $\overline{\text{BURST}}$ + END BURST	$\overline{\text{BURST}}$ END BURST	3A10AC 3A12KH	5 5	D2 C2
1a.3.1 $\overline{\text{BURST}}$ = Single Burst + Steady Burst	Single Burst Steady Burst	Switch S-8 Switch S-8	5 5	D5 D5

DATE _____

JDC: 04154 REV: A PAGE 1 OF 1

JOB: 512-KC CLOCK CALIBRATION

INITIAL TDRR 11119 D.S. PGS. 1

SUBSYSTEM: Ground Support Equipment - AGC Simulator

ASSY: 60A06 1014061-000 and 1014061-011

DESCRIPTION: The 512-kc clock in the AGC Simulator is calibrated.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA
A	3-9-65	17371	All	All	WK	WR

REFERENCES: ND 1021002
JDC 04087

IMPORTANT:

INTERVAL:

TOOLS AND MATERIAL: AGC Calibration System; coaxial cable with BNC connectors 04062

PROCEDURE:

1. Perform JDC 04062.
2. Lift up Logic Plate Assembly 1 and remove the screw on the top of the oscillator (1B28BJ).
3. Using the coaxial cable with BNC connectors connect CLOCK SYNC on the simulator front panel to COMPUTER SIGNAL on the Control and Interface Panel of the AGC Calibration System. Record.
4. Turn the tuning adjustment on the oscillator to read 512000.00 ± 0.05 cps on the counter. Record.
5. Replace the screw and disconnect the AGC Calibration System.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 1

JDC
NO. 04154
REV. A
INITIAL TDRR _____

JOB: 512-KC CLOCK CALIBRATION

ASSEMBLY UNDER TEST	TEST HISTORY
TITLE AGC Simulator	DATE _____ (START) _____ (END) _____ (SITE/LOCATION)
SER. NO. _____ DWG. _____ REV. ____	TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

3. CLOCK SYNC connected to COMPUTER SIGNAL _____
4. Oscillator frequency _____ 512000.00 ± 0.05 cps

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 21 July 64

JDC: 04234 REV: - PAGE 1 OF 4

JOB: AGC SIMULATOR CHECKOUT INFORMATION

INITIAL TDRR 19122 D.S. PGS.

Ground Support Equipment - 60A06

SUBSYSTEM: AGC Simulator

ASSY: 1014061-000 and 1014061-011

DESCRIPTION: Contains AGC Simulator checkout flowgram, typical waveform, and timing diagram.

Rev. Let.	Date	TDRR NO.	PAGES REVISED		APPROVAL	
			JDC	D.S.	MIT	NASA

REFERENCES:

IMPORTANT:

INTERVAL:

TOOLS AND MATERIAL:

This JDC contains three figures to aid in AGC Simulator checkout. Figure 1 is the AGC Simulator checkout flowgram. Figure 2 is an illustration of a typical waveform. Figure 3 is a timing diagram.

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE 9 March 65

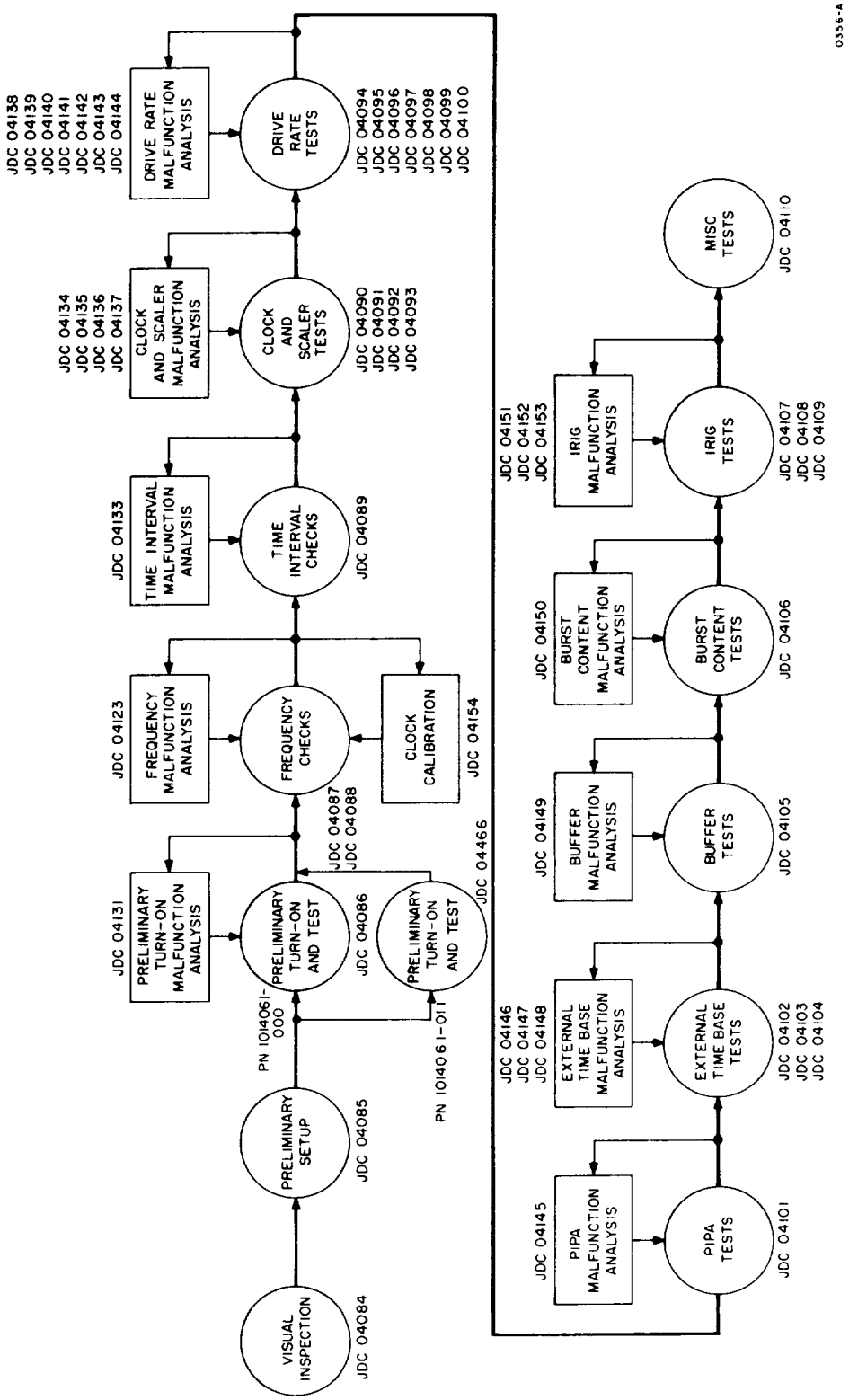

Figure 1. AGC Simulator Checkout Flowgram

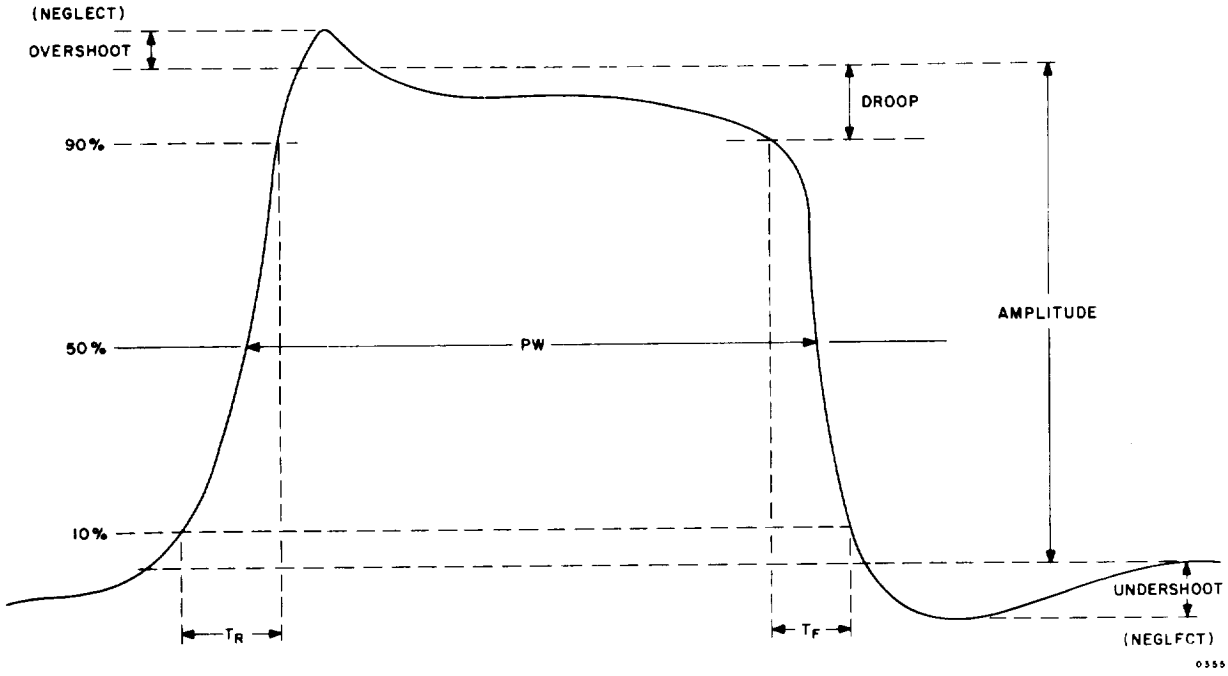

Figure 2. Typical AGC Simulator Waveform

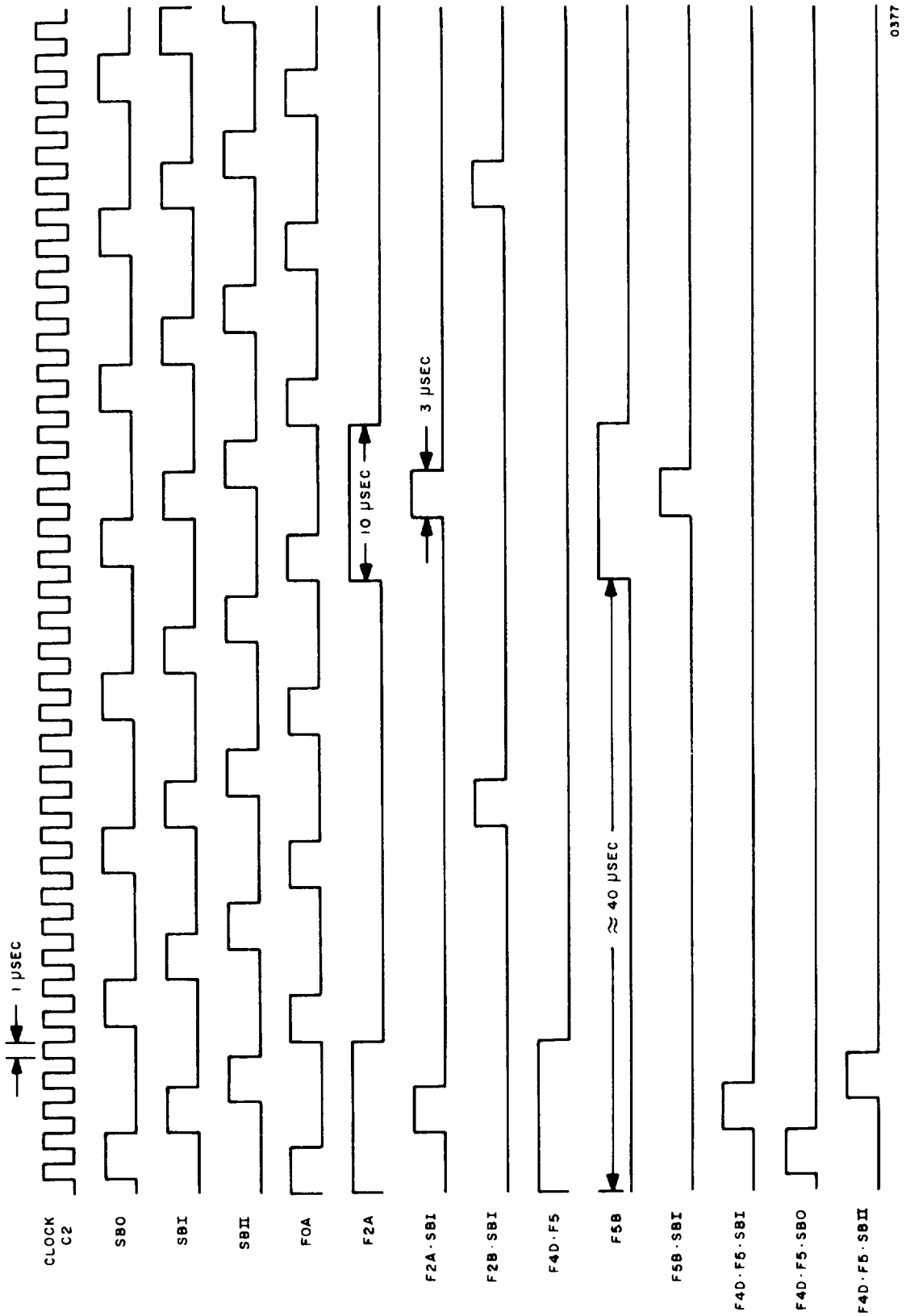

Figure 3. Timing Diagram

DATE 9 March 65

JDC: 04466 REV: - PAGE 1 OF 2

JOB: PRELIMINARY TURN-ON (FIELD)

INITIAL TDRR 16306 D.S. PGS. 2

SUBSYSTEM: Ground Support Equipment

ASSY: AGC Simulator 1014061-011

DESCRIPTION:

Preliminary front panel and power supply checks

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			JDC	D.S.	MIT	NASA

REFERENCES:

ND 1014251
ND 1020202

IMPORTANT: JDC 04085 must be completed before this procedure is performed.

INTERVAL:

TOOLS AND MATERIAL: VTVM (John Fluke Model 803B or equivalent).

PROCEDURE: Perform the following procedure and record the results.

1. Energize 115 vac to Simulator and check that STANDBY POWER ON lamp glows.
2. Set LOGIC POWER ON switch (on d-c power supply assembly) to ON position. LOGIC POWER ON lamp should glow. BIAS REQD lamp should glow.
3. Press IRIG BIAS pushbutton. BIAS REQD LAMP should go out.
4. Set SCALER TEST switch to ON. SCALER TEST OPERATING lamp should blink.
5. Set TIMING INHIBIT switch to INHIBIT position. TIMING INHIBIT lamp should glow. SCALER TEST should go off. Read no continuity (refer to ND 1020202 and ND 1014251):

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE _____

From	To
J1v	J1w
J1v	J4n
J4m	J4n
J4m	J1w

6. Return TIMING INHIBIT switch to NORMAL position.

   TIMING INHIBIT lamp should go out.
   SCALER TEST OPERATING lamp should blink.
   Read continuity (refer to ND 1020202 and ND 1014251):

From	To
J1v	J1w
J1v	J4n
J4m	J4n
J4m	J1w

7. Set LOGIC POWER ON switch (on d-c power supply assembly) to OFF position. LOGIC POWER ON lamp should go off.

8. Connect a jumper wire from J3e to J4BB. LOGIC POWER ON lamp should glow.

9. Set SCALER TEST switch to OFF.

10. Using VTVM, measure

    3.0 ± 0.15 vdc at 3-volt test points on Power Supply Assembly.
    13.0 ± 0.65 vdc at 13-volt points on Power Supply Assembly.

DATE _____

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 1 OF 2

JDC
NO. 04466
REV. -
INITIAL TDRR 16306

JOB: PRELIMINARY TURN-ON (FIELD)

ASSEMBLY UNDER TEST

TITLE AGC Simulator 1014061-011

SER. NO. _____ DWG. _____ REV. ____

TEST HISTORY

DATE _____ (START) _____ (END) _____ (SITE/LOCATION)

TIME _____ (START) _____ (END) _____ (TOTAL ELAPSED)

MAJOR GROUND SUPPORT EQUIPMENT

NAME _____ SER. NO. _____ CAL DATE _____

NAME _____ SER. NO. _____ CAL DATE _____

CONDUCTED BY _____ (NAME/AFFILIATION) APPROVED BY _____ (NAME/AFFILIATION)

	Verify
1. STANDBY POWER lamp on	_____
2. LOGIC POWER	_____
POWER ON lamp on	_____
BIAS REQD lamp on	_____
3. BIAS REQD lamp out	_____
4. SCALER TEST OPERATING lamp blinks	_____
5. TIMING INHIBIT switch to INHIBIT	_____
TIMING INHIBIT lamp on	_____
SCALER TEST lamp off	_____
No continuity J1v to J1w	_____
J1v to J4n	_____
J4m to J4n	_____
J4m to J1w	_____
6. TIMING INHIBIT switch to NORMAL	_____
TIMING INHIBIT lamp out	_____
SCALER TEST OPERATING lamp blinks	_____
Continuity J1v to J1w	_____
J1v to J4n	_____
J4m to J4n	_____
J4m to J1w	_____
7. LOGIC POWER	
POWER ON lamp off	_____

VERIFICATION WITH SIDL REQUIRED BEFORE USE

DATE _____

APOLLO G&N
EQUIPMENT TEST
DATA SHEET 2 OF 2

JDC
NO. 04466
REV. -

JOB: PRELIMINARY TURN-ON (FIELD)

	Verify	
8. LOGIC POWER		
POWER ON lamp on	_____	
9. SCALER TEST switch OFF	_____	
10. Voltages		
3 vdc	_____	3.0 ± 0.15 vdc
13 vdc	_____	13.0 ± 0.65 vdc

DATE _____