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ABSTRACT

An analysis of several computer noise margin testing schemes is presented. A specific machine, the Block II Apollo Guidance Computer (AGC), is used as a concrete example, and its worst-case logic circuit noise margins are analyzed in detail.

It is concluded that static voltage margin testing of the AGC has only limited applicability to establishing a true measure of the actual noise tolerance of the machine. Two alternative test schemes, dynamic voltage margin testing, and a simulated ground plane noise test, show distinct advantages for measuring the amount of logic circuit margin in excess of self-generated noise.

An examination of redundancy in the AGC logic is presented which indicates that useful information might be derived by checking the margins of the computer just prior to flight.

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FROM: J. J. Rocchio

TM-66-1031-3

TECHNICAL MEMORANDUM

1.0 INTRODUCTION

One of the primary design parameters for a digital logic circuit is the so-called "noise margin", generally defined as a measure of the ability of the circuit to tolerate input perturbations without changing state. A noise margin defined in this manner is a function of circuit parameters, as well as of the state of the circuit. To generate an analogous noise susceptibility measure for a digital system (an assembly of interconnected logic circuits) would require, in principle, analysis of every state of the system. As this is a practical impossibility (an assembly of N 2-state circuits could have as many as 2^N distinct states), the worst case circuit noise margin is often used as a measure of the systems noise susceptibility. While it is clear that the noise susceptibility of the system will depend on the noise margins of the logic circuits with which it is constructed, it is also evident that consideration must be given to the level of noise generated within the system which detracts from circuit margins. (State transitions in logic circuits are good sources of noise which can couple between circuits by capacitive and inductive cross-talk.)

In this memorandum several means of testing the noise susceptibility of digital systems will be evaluated with respect to the validity of the resulting measure of the net system noise margin. The discussion to follow was motivated by a specific machine, the Block II Apollo Guidance Computer (AGC), but the principles involved are generally applicable to any digital system.

One of the problems encountered in the design of the AGC involved the d.c. margins of the logic circuits (unique in that a single configuration is used). Study of this problem resulted in the adoption of an additional logic package ("expander gate") to preserve margins for circuits requiring a fan-in greater

than 3 (the capacity of the basic NOR gate). Adoption of the expander gate has, however, not removed all concern over the margins of AGC logic circuits. This is principally a result of:

(a) the fact that a significant number of logic circuits are "overloaded" and consequently have a worst case margin lower than that anticipated from the original design rules;
(b) the fact that the original design margins are degraded at the extremes of the design temperature range and by temperature differentials within the machine; and
(c) the fact that the noise coupling characteristics of the machine are not known in detail, and are expected to vary from machine to machine.

The Procurement Specification (Apollo G&N specification PS 2016005) incorporates a set of FTM's (final test methods) which constitute the AGC Acceptance Test. These tests are designed in part to establish the flight worthiness of production-version computers. The degree to which this set of tests insures confidence in the noise margins of the AGC logic circuitry is considered in this memorandum. It is important to note at the outset, however, that one of the main problems in testing a complex logical system such as the AGC involves insuring that the various subparts are subjected to worst case conditions while operating at reduced margins (and that failures occurring under such conditions are detected). This task is relegated to the computer programs (Newspeak Rope) run during the Acceptance Test. No evaluation of these test programs is attempted here, so it is tacitly assumed that they are meeting this objective.

A discussion of the noise margins of the AGC logic circuits and of several noise margin testing schemes for this machine follows. Appendix A contains detailed noise margin computations. A distinct but related topic is treated in Appendix B, which deals with a type of parallel redundancy present in the AGC logic. Analysis indicates that this redundancy provides a degree of failure tolerance. While this is beneficial to the system, it allows for the possibility of having such failures occur undetected in the pre-flight experience of a given machine. One means of guarding against this possibility and insuring that the full benefit of the redundancy is obtained is to test the margins of the computer just prior to flight.

2.0 NOISE MARGIN ANALYSIS

The noise margin of a logic circuit is a measure of the minimum magnitude of a noise signal which, when superimposed on the information level at the input to the circuit, can cause a false output from the stage. Figure 1 shows a 3-input DCTL NOR gate such as is used in the AGC. The states of this circuit will be denoted as ON when at least one transistor is conducting, and OFF when all transistors are non-conducting. Two noise margins may be defined for a bistable circuit: a margin against false turn-on (V_N-off) and a margin against false turn-off (V_N-on) (see Figure 2). It is general practice to compute such margins on a static or d.c. basis. It should be noted however that the circuits will generally be subject to pulse type noise, such as results from cross-talk coupling. Immunity to such noise is greater than indicated by the static noise margins due to the delay and storage mechanisms of the transistors. In this sense these (static) noise margins are conservative.

2.1 OFF Noise Margin

The worst case "off" noise margin (V_N-off) may be computed for AGC logic gates by taking the difference between the input voltage for which a gate delivers at least some specified output current (V_{OFF}), and the maximum saturation voltage an "on" stage can be expected to have ($\overline{V}_{ZERO}$). Thus:

$$V_N\text{-off} = V_{OFF} - \overline{V}_{ZERO} \quad .$$

The Specification Control Drawing (SCD 1006394) for AGC integrated circuit logic gates guarantees an off margin of at least 200 mv for a normal gate and 100 mv for an expander gate at 25°C. As the off noise margin is primarily a function of the transistor characteristics it does not vary significantly with circuit configuration or with supply voltage. Variation may be expected with temperature and temperature differentials, and the specification indicates off noise margins of 250 mv at 0°C and 100 mv at 70°C for normal gates, and 100 mv at 0°C and 80 mv at 70°C for expander gates.

2.2 ON Noise Margin

For the AGC the worst case "on" noise margin (V_N-on) may be computed as the difference between the "one" signal voltage at a gate input assuming the most unfavorable circuit

configuration and combination of parameters ($\underline{V}_{ONE}$), and the minimum turn-on voltage (V_{ON}) guaranteed by the gate specification. Thus:

$$V_N\text{-on} = \underline{V}_{ONE} - V_{ON} \quad .$$

V_N-on varies markedly as a function of fan-out and supply voltage* (see Figure 3). The initial NOR gate SCD for the Block II AGC was intended to guarantee a minimum on noise margin of 100 mv at 25°C for a fan-out of 5. Recently the SCD was revised to govern performance at the temperature extremes of 0° and 70°C. The revised specification (see Appendix A) is intended to ensure a minimum margin of 80 mv over this temperature range for a circuit with fan-out of 5.

Due to the existence of logic circuit overloads in the AGC design, the actual worst case on noise margin is lower than is predicted from the SCD. Thus, for example, a gate with a fan-out of 6 (20% overload) exhibits a worst case on noise margin of 68 mv at rated supply voltage, or 32 mv below the original design goal. Using the information in the revised SCD, calculations indicate that the worst case on noise margins are 43 mv at 0°C, and 46 mv at 70°C (see Figure 4).

2.3 System Noise Margin

The overall noise tolerance of a digital computer is a measure of the machine's internal noise margins, and of the ability of the design to limit the influence of external sources of noise. While a measure of the system's noise susceptibility in its operational environment is an important evaluation criterion, the attention here is directed towards the more specific subject of net margins of the computer's logic subsystem. Given that a machine design has demonstrated acceptable overall noise tolerance for its application, there can still be valid inquiry into the noise margins of the logic circuits. In space-born applications, for example, one may fly only a subset of a series of flight-qualified machines. A noise margin measure could provide a useful indication of which machine should be assigned for flight. In addition, such a measure could provide

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*Noise margin calculations are contained in Appendix A.

ability to track the performance of a machine throughout its pre- and post-flight experience, and provide assurance against gradual loss of noise tolerance (see Appendix B).

While the circuit noise margins are often used as a figure of merit for logic system designs, a more valid measure results when internal noise is accounted for. A new parameter, denoted as the signal margin (V_m), can be defined as the difference between the actual input to a circuit, signal plus noise, and the threshold of the circuit. Thus for a given gate:

$$V_m\text{-on} = \underline{V}_{ONE} - \bar{V}_D\text{-on} - V_{ON}$$

$$= V_N\text{-on} - \bar{V}_D\text{-on} \quad ,$$

and

$$V_m\text{-off} = V_{OFF} - \bar{V}_D\text{-off} - \bar{V}_{ZERO}$$

$$= V_N\text{-off} - \bar{V}_D\text{-off} \quad ,$$

where $\bar{V}_D$-on is the maximum (over all possible states of the machine) noise voltage at the gate input when the gate is in the ON state and $\bar{V}_D$-off is the corresponding maximum noise voltage in the OFF state. (Note that the noise voltages in the above equations must be equivalent d.c. voltages since the circuit margins have been defined on a static basis.)

In general, noise coupling in a computer's logic circuits is a complex geometrical function of the signal paths, and depends on voltage and current levels as well as on the timing relations between logic signal transitions. If one could predict the worst case noise conditions, an analytic measure of the worst case signal margin could be generated from the above equations. In practice, due to the state dependence of the internal noise, it is possible at best to make a gross estimate of worst case noise levels. The typical design philosophy specifies minimum circuit noise margins (V_N-on, V_N-off) conservatively, and then attempts to constrain cross-talk to be as low as possible.

The difficulty of analytically determining worst case signal margins implies that an operational test procedure, capable of providing a measure of this margin, can be a useful evaluation tool. It is important to note in this context, that the complexity of the noise generation and coupling processes within the logic makes it difficult to stress a machine to worst case conditions. Thus the value of a test procedure will be heavily dependent on having a well designed test program which exercises the machine through those states in which cross-talk noise is likely to be severe. Since an exhaustive test of all states of the machine is prohibitive, the design of such programs is worthy of independent study.

3.0 STATIC VOLTAGE MARGIN TESTING

Since the on noise margin of AGC logic gates is a function of the collector supply voltage (V_{CC}), one means of verifying that a machine has at least some specified minimum on noise margin Δ is to reduce V_{CC} so as to cause a reduction of at least Δ in V_N-on of all circuits. If the logic can operate at this reduced V_{CC}, the on noise margin at rated supply is at least Δ. The AGC Acceptance Test requires that the machine operate at V_{CC} = 3.4, 4, and 4.5 volts at ambient temperature and at the temperature extremes. While such a test is clearly useful in that it stresses the machine at limits greater than allowed by the power supply specification (4 $\pm$ .2 volts), a reduction of 600 mv in V_{CC} causes a reduction of only about 25 mv* in the on noise margin of the worst case circuit (fan-out of 6). Since this reduction is less than the worst case margin (43 mv) it does not provide additional information about this parameter.

The fact that the machine can operate at V_{CC} = 3.4 volts does indicate however that the noise margin at this voltage is greater than the internal noise i.e., that the signal margin is positive. Cross-talk noise, however, is not independent of the supply voltage. In fact, under idealized conditions, it can be shown from transmission line analysis that the magnitude of the cross-talk signal due to a voltage pulse of magnitude ΔE and rise time τ_R is proportional to $\Delta E/\tau_R$. Since the magnitude of the logic signal swing (ΔE) varies directly with V_{CC}, and the rise time of a "0" to "1" signal transition varies (in part) inversely with V_{CC}, the level of cross-talk noise can be expected to have a term proportional to V_{CC}^2 over the range where these assumptions hold.

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*Calculations are in Appendix A.

This variation of self-generated noise with supply voltage implies that a static voltage margin test is not a useful measure of the signal margin (signal excess above internal noise) unless it can be demonstrated that the noise coupling is sufficiently low such that the absolute magnitude of cross-talk noise does not change significantly with changes in V_{CC}.

Figure 5 illustrates how a static voltage margin test may give a false indication of the amount of signal margin when the level of cross-talk noise can vary significantly with V_{CC} (note that the cross-talk noise level is shown as varying linearly with V_{CC} for simplicity). The figure assumes that two machines are tested to failure by lowering the supply voltage. Note that machine A fails at a higher V_{CC} than machine B, and that this could be taken as implying that B had better noise tolerance. However with the assumed noise level curves, machine A in fact has greater signal margin at the rated V_{CC}, and therefore more actual noise tolerance (under operational conditions) than machine B.

4.0 DYNAMIC VOLTAGE MARGIN TESTING

The deficiencies of static voltage margin testing can be overcome to a large degree by a dynamic margin test in which the collector supply voltage, V_{CC}, is pulse modulated so as to generate in effect, a noise signal at the input to all turned-on gates. The magnitude of the noise at the input to a gate caused by V_{CC} modulation may be computed directly from the relation giving the rate of change of V_N-on with respect to V_{CC} as developed in Appendix A. It should be noted that the worst case circuit (FO = 6) is the limiting one since for a given change in V_{CC} it has the highest ratio of induced noise to signal margin. (It is implied here that a means is available for circumventing the filtering of the computer power supply, and any high frequency attenuation of the V_{CC} bus system if necessary.) In addition to introducing a direct signal change at the input to all ON gates, the V_{CC} modulation is capable of exciting (since it introduces a synchronous signal change throughout the logic) many of the noise coupling paths within the machine. An additional advantage of this scheme lies in the fact that it subjects the logic to noise via a path (the V_{CC} bus system) which is a potential operational noise source. Under these circumstances the magnitude of the

pulse disturbance to V_{CC} which can be tolerated by the computer (while operating appropriate test programs) is a truer indication of the minimum signal margin of the machine than is provided by the static voltage margin test. This conclusion is supported by experimental data collected at Berkeley Scientific Laboratories by W. Wattenburg* who suggested the dynamic margin test scheme.

The disadvantages of dynamic voltage margin testing for the AGC lie in the necessity of circumventing the power supply filtering and in the potential difficulty of implementing the desired V_{CC} modulation at the AGC current levels.

5.0 SIMULATED GROUND PLANE NOISE TESTING

Another means of verifying that the AGC has satisfactory margins involves the simulation of ground plane noise by biasing the ground of a given computer module with respect to the ground of the rest of the computer. This scheme has been suggested by MIT/IL and some initial experimental testing has been done there.

The effect of a ground bias on a module of the AGC may be analyzed by considering the circuit shown in Figure 6. For intramodule gate connections (i.e., for gates which either only drive or are driven by other gates within a module) the addition of a ground bias potential of $\pm$ Eg is equivalent to changing the collector supply voltage (V_{CC}) by $\mp$ Eg. However, the ground bias voltage has a different effect on inter-module gate connection. With respect to the off noise margin, the ground bias appears as a direct equivalent noise potential on inter-module signals according to the following table:

Ground Bias Potential	State of Biased Gate	Effect on Off Noise Margin
$\pm$ Eg	OFF	Off margin of module gate (driven by module input) changes by $\pm$ Eg
$\pm$ Eg	ON	Off margin of external gate (driven by module output) changes by $\mp$ Eg

*Consultant to Bellcomm, Inc.

The effect of the ground bias voltage on the on noise margin of gates which are driven by or drive extra-module gates is more complicated. Consider a gate which drives n parallel gates (a circuit with a fan-out of n). Assume that k of the driven gates are located within a biased module and n-k are external to it. In this case, it is immaterial whether the driving gate is internal or external to the biased module, as the effect of the bias voltage is to make the internal gates current hogging or current starved with respect to the non-biased gates. The magnitude of the change in the on noise margin can be calculated (assuming nominal gates) by the relations:

$$\Delta V_N\text{-on} = \pm \frac{kR_C}{nR_C + R_B} \quad x \quad |E_g|$$

for non-biased gates; and

$$\Delta V_N\text{-on} = \mp \frac{(n-k)R_C + R_B}{nR_C + R_B} \; x \; |E_g|$$

for biased gates, where the sign varies according to the sign of the applied bias. Hence the on noise margin is not affected by the full magnitude of the ground bias as is the off noise margin. In the worst case, (allowing a fan-out (n) of 6), however, changes of about .8 E_g and .85 Eg can be realized in on noise margins of non-biased and biased gates respectively.

The above analysis indicates that the simulated ground plane noise test (in which each logic module is biased in turn) has several distinct advantages over a static voltage margin test. Primarily, it allows a direct measure of the signal margin of those gates which generate or receive inter-module signals. This results because the bias potential subtracts almost directly from the signal levels of the affected gates (as opposed to voltage margin testing, where there is significant attenuation of the noise introduced through the collector supply voltage) but causes only a small change in the voltage levels of intra-module signals and no change in extra-module signals. Therefore, cross-talk noise levels due to nonaffected circuits (which will be in the majority) will be essentially unchanged and the amount of bias which can be tolerated is indicative of the worst case signal margin of the affected gates. In addition, the ground bias

stresses both on and off margins, whereas both static and dynamic variation of V_{CC} principally affect only the on noise margin. The disadvantages of the ground bias test lie in the fact that the biased module must be removed from its operational position using an extender for example, and in the fact that intra-module signals are not stressed to any appreciable extent. The latter is not a very severe drawback since in all probability the inter-module signals will have the most severe cross-talk noise.

The ground bias noise test can be operated in a static or dynamic fashion. A.C. modulation of the bias potential would simulate to a degree the effect of ground plane inductance, as well as provide additional noise stressing via cross-talk coupling paths.

6.0 SUMMARY

Three test schemes have been considered with respect to their ability to provide a measure of the net noise margin of the logic subsystem of a digital computer. The conventional scheme, static voltage margin testing has been shown to be deficient compared with either dynamic voltage margin testing or simulated ground plane noise testing. Each of these two latter test procedures may be potentially valuable in testing a machine, particularly as they simulate to a degree different kinds of noise susceptibility. Thus one introduces noise via the collector voltage supply system and the other via the ground plane of the machine. In addition these schemes differ with respect to ease and time required for testing. The dynamic voltage margin test is applied to the entire system and only requires bypassing of the power supply, whereas the simulated ground plane noise test is applied on a module by module basis and requires removal of a module from its operational position. Experimental data are required to establish whether these two test procedures are essentially equivalent or are capable of indicating different modes of noise susceptibility in the logic subsystem.

J. J. Rocchio

1031-JJR-jdc J. J. Rocchio

Attachments
Appendix A and B

APPENDIX A

NOISE MARGIN COMPUTATIONS

The SCD for AGC NOR Gates is being revised to specify performance at 0°C and 70°C. According to information received from MSC the following table of parameters should characterize the gates over the temperature range

Parameter	Units	0°C	25°C	70°C
V_{IN}	mv	925	870	770
V_{ON}	mv	845	770	690
V_{OUT} (GATE)	mv	300	300	300
V_{OUT} (EXPANDER)	mv	450	400	330
V_{OFF}	mv	550	500	410
I_{IN}	μa	155	152	145
I_A	μa	775	760	720

The worst case on noise margin (V_N-on) can be computed according to the equation:

$$V_N\text{-on} = \frac{\frac{V_{CC} - \bar{V}_{BE}}{\bar{R}_C} - \frac{(FO-1)\,(\bar{V}_{BE} - \underline{V}_{BE})}{R_{BH}}}{1/R_{BS} + (FO-1)/R_{BH} + 1/R_C} + \bar{V}_{BE} - V_{ON} \qquad (A1)$$

Appendix A (continued)

where FO is the fan-out, V_{ON} the gate threshold, R_{BH} and $\underline{V}_{BE}$ characterize a current hogging gate and R_{BS} and $\overline{V}_{BE}$ characterize a current starved gate (see Figure 7). It can be demonstrated that the worst case occurs when the starved gate is an expander gate. To calculate $\overline{V}_{BE}$ for an expander, the minimum h_{FE} (d.c. current gain) for the gate must be known. At 25°C the minimum h_{FE} allowed by the SCD is 30.

Case 1 - 25°C

Hogging Gate	Starved Gate (Expander)
V_{IN} = 870 mv	V_{ON} = 770 mv
R_{BH} = 1200 ohms	R_{BS} = 1200 ohms
I_{IN} = 152 μa	I_{IN} = 3.6/(2700 x 30) = 44.5 μa
$\underline{V}_{BE}$ = 870 - (1.2 x 152)	$\overline{V}_{BE}$ = 770 - (1.2 x 44.5)
= 688 mv	= 717 mv.

$\overline{R}_C$ = 4150 ohms (From the SCD).

With these parameters equation (A1) gives V_N-on = 148 mv for a fan-out (FO) of 4, and 105 mv for a fan-out of 5.

For a fan-out of 6 the worst case occurs when the hogging gates have the lowest possible V_{BE}. Assuming this to be .620 volts (a representative value for this kind of device) the hogging gate is specified by:

Hogging Gate

V_{IN} = 870 mv

Appendix A (continued)

I_{IN} = 152 μa

$\underline{V}_{BE}$ = 620 mv

R_{BH} = (870-620)/.152 = 1645 ohms

These parameters with those of the starved gate above entered into eq. (A1) yield V_N-on = 68 mv for a fan-out of 6.

Case 2 - 0°C

Based on manufacturer's data for devices of this class, it will be assumed that h_{FE} can decrease to 22.5 at 0°C and to 20 at 70°C (h_{FE} is measured per the SCD at a higher voltage than is used operationally). In addition the temperature coefficient for the diffused resistors of the gate will be assumed to vary from .965 to .98 at 0°C, and 1.055 to 1.075 at 70°C, referred to the 25°C values. Using these assumptions, the following values may be calculated for hogging and starved gates.

Hogging Gate	Starved Gate (Expander)
V_{IN} = 925 mv	V_{ON} = 845 mv
R_{BH} = 1200x.98 = 1175 ohms	R_{BS} = 1200x.965 = 1160 ohms
I_{IN} = 155 μa	I_{IN} = 3.55/(2700x.965x22.5) = 62 μa
$\underline{V}_{BE}$ = 925 - (1.175 x 155) = 743 mv	$\overline{V}_{BE}$ = 845 - (1.160 x 62) = 773 mv

$\overline{R}_C$ = 4150 x .98 = 4100 ohms.

With these parameters eq. (A1) yields V_N-on = 122 mv for a fan-out of 4, 82 mv for a fan-out of 5. For a fan-out of 6 the hogging gate is specified by:

Appendix A (continued)

Hogging Gate

V_{IN} = 925 mv

R_{BH} = 1645 x .98 = 1610 ohms

I_{IN} = 155 μa

$\underline{V}_{BE}$ = 925 - (1.610 x 155) = 675 mv

These parameters with those of the starved gate above entered into eq. (A1) yield V_N-on = 43 for a fan-out of 6.

Case 3 - 70°C

Hogging Gate

V_{IN} = 770 mv

R_{BH} = 1200 x 1.055 = 1265 ohms

I_{IN} = 145 μa

$\underline{V}_{BE}$ = 770 - (1.265 x 145)
= 587 mv

Starved Gate (Expander)

V_{ON} = 690 mv

R_{BH} = 1200 x 1.055 = 1265 ohms

I_{IN} = 3.67/(2700 x 1.055 x 20) = 64 μa

$\overline{V}_{BE}$ = 690 - (1.265 x 64)
= 609 mv

$\overline{R}_C$ = 4150 x 1.075 = 4480 ohms.

With these parameters, eq. (A1) yields: V_N-on = 127 mv for a fan-out of 4, 84 mv for a fan-out of 5. For a fan-out of 6 the hogging gate is specified by:

Hogging Gate

V_{IN} = 770 mv

R_{BH} = 1644 x 1.075 = 1770 ohms

Appendix A (continued)

$$I_{IN} = 145 \ \mu a$$

$$\underline{V}_{BE} = 770 - (1.77 \times 145) = 514 \text{ mv}$$

These parameters with those of the starved gate above entered into eq. (A1) yield V_N-on = 46 mv for a fan-out of 6.

Case 4 - Interface Circuits

A worst case noise margin for interface circuits assumes an expander gate with a load of 3 kohms to +10 volts. Two inputs of the expander are driven in parallel with 3 hogging gates (see Figure 8).

The noise margin equation is modified for this configuration to:

$$V_N\text{-on} = \frac{\dfrac{V_{CC} - \overline{V}_{BE}}{\overline{R}_C} - \dfrac{(FO-2)\ (\overline{V}_{BE} - \underline{V}_{BE})}{R_{BH}}}{2/R_{BS} + \dfrac{(FO-2)}{R_{BH}} + 1/\overline{R}_C} + \overline{V}_{BE} - V_{ON} \qquad (A2)$$

Due to the different load on the expander a new value for V_{ON} must be computed. As the collector current for the interface load is 1.6 ma per transistor, the required base current can be computed by scaling from the normal collector current. Thus at 25°C

$$I_B = 44.5 \times 1.6/1.33 = 53.5 \ \mu a$$

and

$$V_{ON} = 717 + 30\ (1.6\text{-}1.33) + (1.2 \times 53.5) = 789 \text{ mv}$$

(where 30 ohms has been allowed for the emitter resistance, R_E).

Appendix A (continued)

Using the parameters of Case 1 with the new V_{ON} computed above, equation (A2) yields V_N-on = 91 mv for a fan-out of 5.

At 0°C

$$I_B = 62 \times 1.6/1.39 = 71 \ \mu a$$

$$V_{ON} = 773 + 30\ (1.6-1.39)+(1.165 \times 71) = 862 \text{ mv.}$$

Using the parameters of Case 2 with the new V_{ON} computed above, equation (A2) yields V_N-on = 68 mv for a fan-out of 5.

At 70°C

$$I_B = 1.6/1.28 \times 64 = 80 \ \mu a$$

$$V_{ON} = .609+30\ (1.6-1.28)+(1.265 \times 80) = 720 \text{ mv.}$$

These results are summarized in tabular form below:

Fan-out	D. C. ON NOISE MARGIN		
	0°C	25°C	70°C
4	122 mv	148 mv	127 mv
5	82 mv	105 mv	84 mv
5 (interface)	68 mv	91 mv	60 mv
6	43 mv	68 mv	46 mv

Appendix A (continued)

The noise margins computed above are degraded by leakage current through the off transistors. The amount of leakage varies with the fan-in of the circuit, and its affect on V_N-on is also dependent on the circuit configuration. Quantitatively, the leakage current of 15 μa max. at 25°C guaranteed by the SCD produces a reduction of about 1.5 to 1 mv per fan-in collector for the circuits treated above.

The on noise margin is also degraded by temperature differentials between logic elements in the machine. The principal effect responsible for this is the temperature dependence of the base to emitter threshold voltage V_{BE}. Assuming a variation of -2mv/°C for V_{BE}, and the most unfavorable situation, equation (A1) may be differentiated with respect to $\underline{V}_{BE}$ to yield:

$$\frac{\partial V_N\text{-on}}{\partial T} = \frac{(FO-1)/R_{BH}}{1/R_{BS} + (FO-1)/R_{BH} + 1/\overline{R}_C} \times \frac{\partial \underline{V}_{BE}}{\partial T}$$

For a 10°C temperature differential this equation predicts a loss of 12 to 15 mv from the previously computed margins.

The effect of supply voltage variations on the noise margin V_N-on may be computed by differentiating eq. (A1) with respect to V_{CC}. Thus,

$$\frac{\partial V_N\text{-on}}{\partial V_{CC}} = \frac{1/\overline{R}_C}{1/R_{BS} + (FO-1)/R_{BH} + 1/R_C} - \frac{\partial V_{ON}}{\partial V_{CC}}$$

Since,

$$V_{ON} = \left[\frac{V_{CC} - V_{SAT}}{\underline{R}_C \underline{\beta}}\right] R_{BS} + \overline{V}_{BE} \quad ,$$

Appendix A (continued)

$$\frac{\partial V_{ON}}{\partial V_{CC}} = \frac{R_{BS}}{\underline{R}_C \underline{\beta}}$$

Therefore,

$$\frac{\partial V_N\text{-on}}{\partial V_{CC}} = \frac{1/\overline{R}_C}{1/R_{BS} + (FO-1)/R_{BH} + 1/\overline{R}_C} - \frac{R_{BS}}{\underline{R}_C \underline{\beta}}$$

For the interface circuits V_{ON} will not change if the +4 and +14 volt supplies vary independently. Thus differentiating eq (A2) with this assumption gives

$$\frac{\partial V_N\text{-on}}{\partial V_{CC}} = \frac{1/R_C}{2/R_{BS} + (FO-2)/R_{BH} + 1/\overline{R}_C} \quad \text{(interface)}$$

The rates of change in on noise margin in mv/volt for the cases of interest are listed below:

Fan-out	$\Delta V_N\text{-on}/\Delta V_{CC}$ in mv/volt		
	T=0°C	T=25°C	T=70°C
4	46	53	44
5	34	40	33
5(interface)	54	55	53
6	38	44	36

Appendix A (continued)

This variation in noise margin with supply voltage only holds over the linear range of the input characteristic, and is no longer valid when operating in the knee of the base-emitter diode, i.e., when the margin approaches zero.

APPENDIX B

PARALLEL REDUNDANCY IN AGC LOGIC CIRCUITS

Summary

Logic and register functions in the AGC are realized using a dual 3-input integrated circuit NOR gate and an expander gate. The expander gate is used for circuits requiring a fan-in greater than 3. To implement high fan-out circuits the NOR gates are paralleled. (In a more conventional design a higher power gate, or an emitter follower might be used.)

The analysis in this appendix reveals that these parallel gate configurations are to a certain extent failure tolerant. While this is unquestionably a desirable characteristic, it allows for the possibility of having such failures occur undetected in the pre-flight experience of a given machine. Were this to occur, a computer would be flown with less failure tolerance for its mission than is inherent in the design.

The analysis below indicates that the effect of certain failures is to degrade the noise margins of these parallel gate circuits. This suggests that one means of testing for failures of the type under consideration is to ascertain that no significant change in the computer noise margin occurs during its pre-flight history.

Case 1

Assume a configuration in which a single gate drives from 2 to 5 parallel gates. Consider that a transistor of one of the parallel gates fails with a base-to-emitter short, collector-to-emitter open. Assuming all gates are nominal, the base driving voltage can be computed before and after failure according to the equations:

$$E_D = \frac{V_{CC}\, R_B + k\, V_{BE}\, R_C}{R_B + k\, R_C}$$

with no failures, where $k(2 \leq k \leq 5)$ is the number of parallel gates; and

Appendix B (continued)

$$E'_D = \frac{V_{CC} R_B + (k-1) V_{BE} R_C}{R_B + k R_C}$$

with one failure of the type being considered. Assuming V_{CC} = 4.0 volts, V_{BE} = .7 volts, R_B = 1500 ohms, and R_C = 3400 ohms yields the following table:

k	E_D	E'_D	Loss of On Margin
2	1.30v	1.01v	290 mv
3	1.12v	.92v	200 mv
4	1.03v	.87v	160 mv
5	.97v	.84v	130 mv

Note that the loss of margin shown in the above table is conservative since it ignores the fact that the collector current of the remaining transistors will increase as a result of the failure; this however is a second order effect. These results suggest that a failure of the type indicated could result in a significant loss of margin without causing a hard failure of the gate.

Case 2

Assume a fully loaded parallel gate configuration, i.e., one in which k gates in parallel drive 5k gates (in the AGC some parallel gate circuits are in fact overloaded). Consider a failure such that the drive current capacity of one of the parallel gates is lost as would occur for a collector resistor open or for an output lead open. Assuming no significant change occurs on the input side of the parallel gate combination the effect to be examined is the loss of drive capacity. A nominal analysis indicates that with no failures the output voltage of the parallel gate is:

Appendix B (continued)

$$E_D = \frac{V_{CC} R_B + n/k \, V_{BE} R_C}{R_B + n/k \, R_C}$$

where k is the number of driving gates and n is the number of driven gates. A fully loaded condition corresponds to n/k = 5, in which case

$$E_D = \frac{4.0 \times 1500 + 5 \times .7 \times 3400}{1500 + 5 \times 3400} = .97 \text{ volts}$$

using nominal parameters.

A single failure of the type considered here produces a loss of drive margin as shown in the following table:

No. of Parallel Gates	n/k After Single Failure	Output Voltage After Failure	Margin Loss
2	10	.84v	130 mv
3	15/2	.88v	90 mv
4	20/3	.90v	70 mv
5	25/4	.92v	50 mv

Again it may be noted that in each case the output voltage after failure is sufficient to turn on the driven gates, but with a significient loss of margin.

Case 3

The third failure to be analyzed is the effect of a base-to-emitter open, collector-to-emitter open, in which the collector resistor of the failed gate is still connected to the remaining functioning gates. In this instance there will be a simultaneous increase in both the collector current and base drive of the operational transistors. With no failures the base current to each of k parallel gates driven from a single gate is

Appendix B (continued)

$$I_B = \frac{V_{CC} - V_{BE}}{k\,R_C + R_B} \quad ,$$

whereas after one open failure

$$I_B' = \frac{V_{CC} - V_{BE}}{(k-1)\,R_C + R_B} \quad ,$$

hence

$$\frac{I_B'}{I_B} = \frac{k\,R_C + R_B}{(k-1)R_C + R_B} \quad .$$

Assuming equal collector resistors, the collector current per remaining gate increases by the ratio k/k-1. The following table shows percentage base and collector current increases assuming nominal gates.

No. of Parallel Gates	% Increase in Base Current	% Increase in Collector Current
2	69	100
3	41	50
4	29	33
5	23	25

In this case the principal effect will be an increase in the saturation drop of the operational gates due to increased collector current and a reduction in the drive ratio I_C/I_B. The latter will also tend to increase the rise time of the gate (i.e., decrease the switching speed of an off to on state change). The amount of loss of off margin in this case is difficult to compute due to the lack of data on the saturation characteristic of the AGC NOR gates.

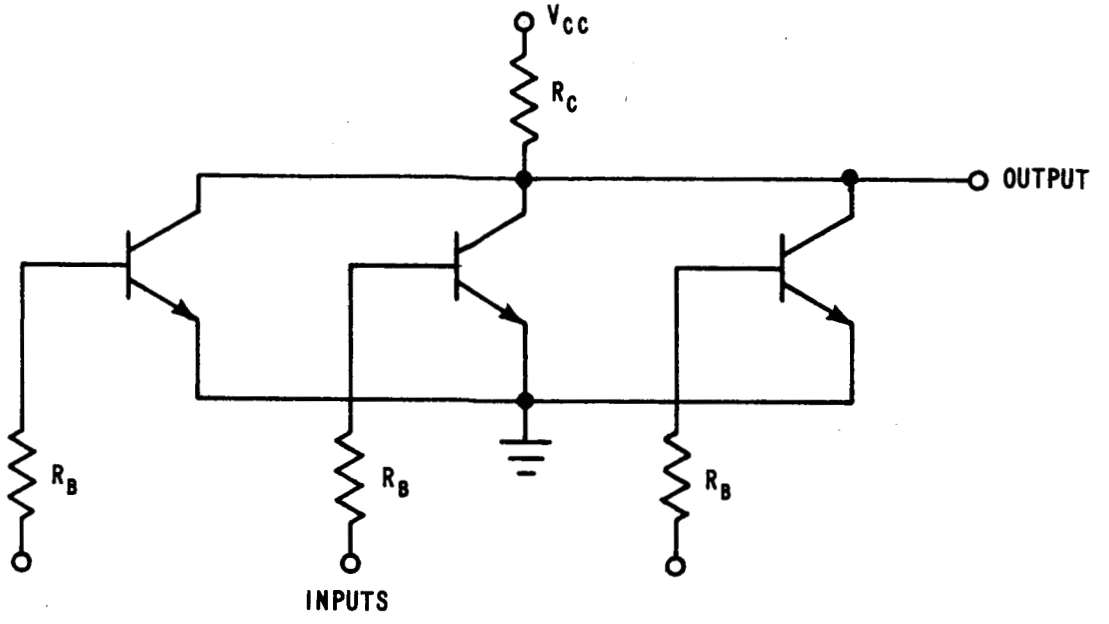
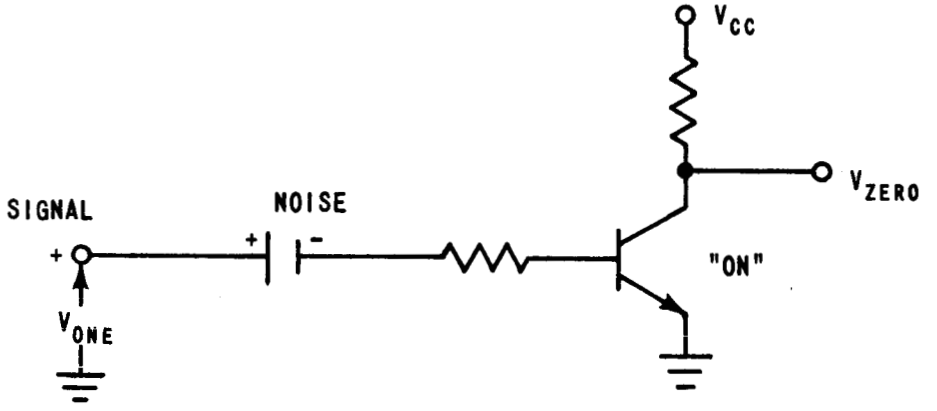
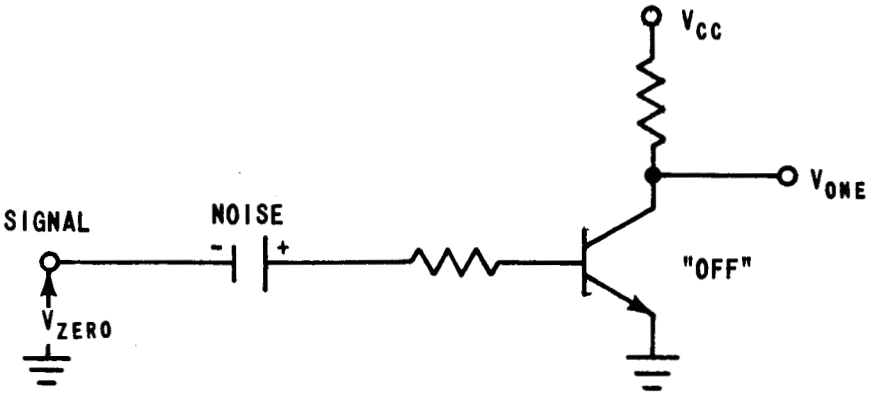


FIGURE 1 - HALF OF A DUAL 3-IMPUT NOR GATE



MINIMUM NOISE VOLTAGE TO CHANGE STATE = V_N - on



MINIMUM NOISE VOLTAGE TO CHANGE STATE = V_N - off

FIGURE 2 - LOGIC CIRCUIT NOISE MARGINS

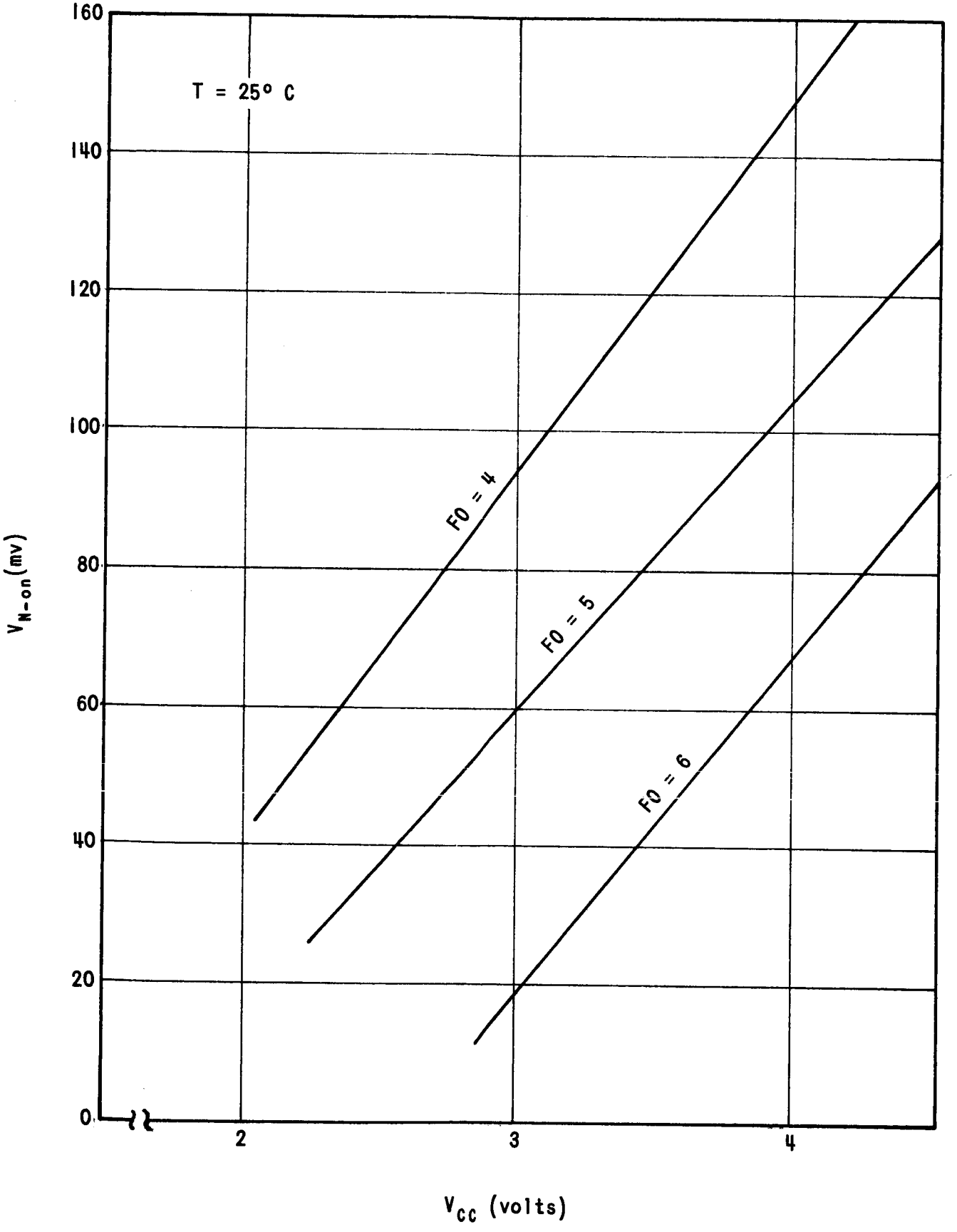


FIGURE 3 - WORST CASE ON NOISE MARGIN AS A FUNCTION OF FAN-OUT AND SUPPLY VOLTAGE

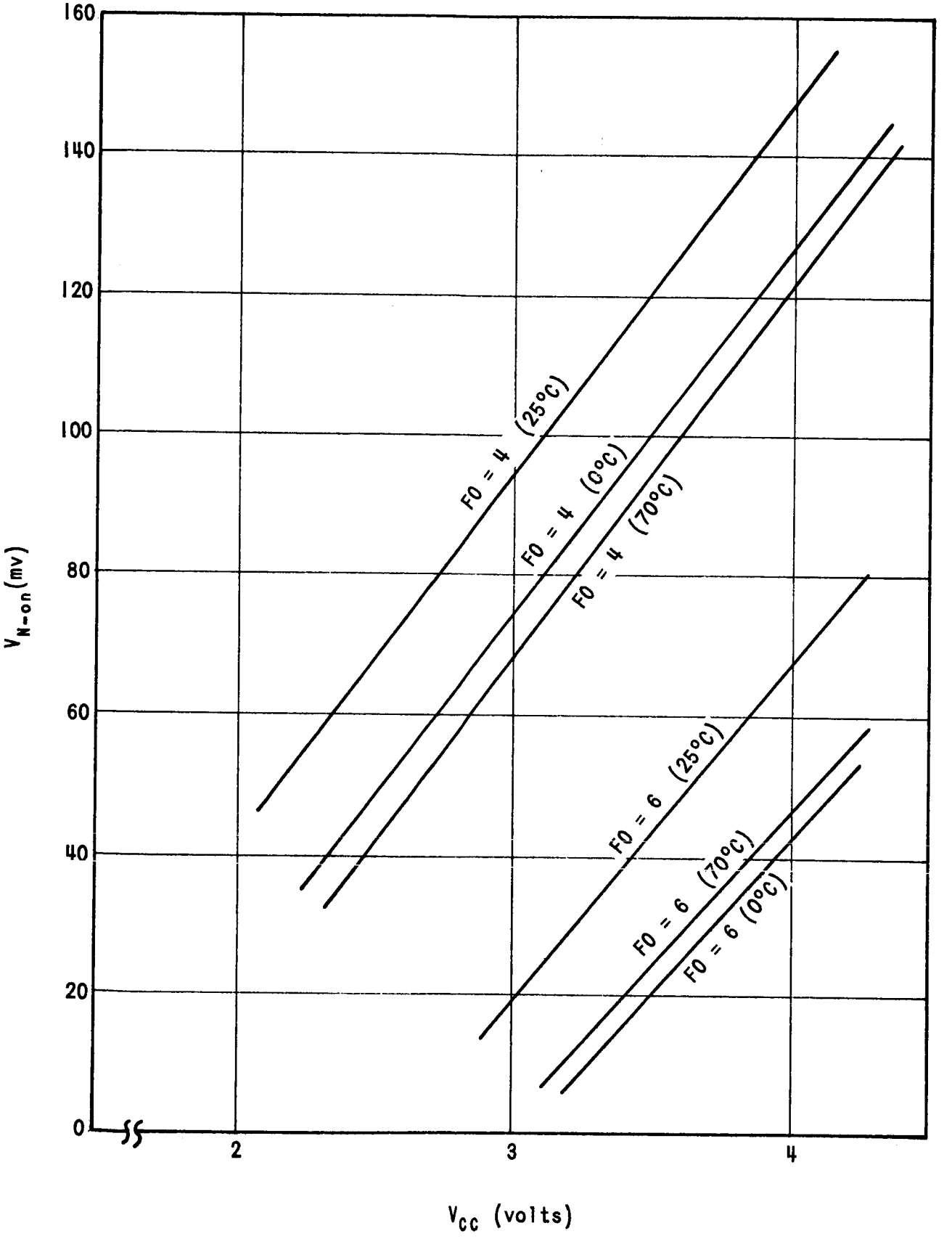


FIGURE 4 - CHANGE IN WORST CASE ON NOISE MARGIN WITH TEMPERATURE

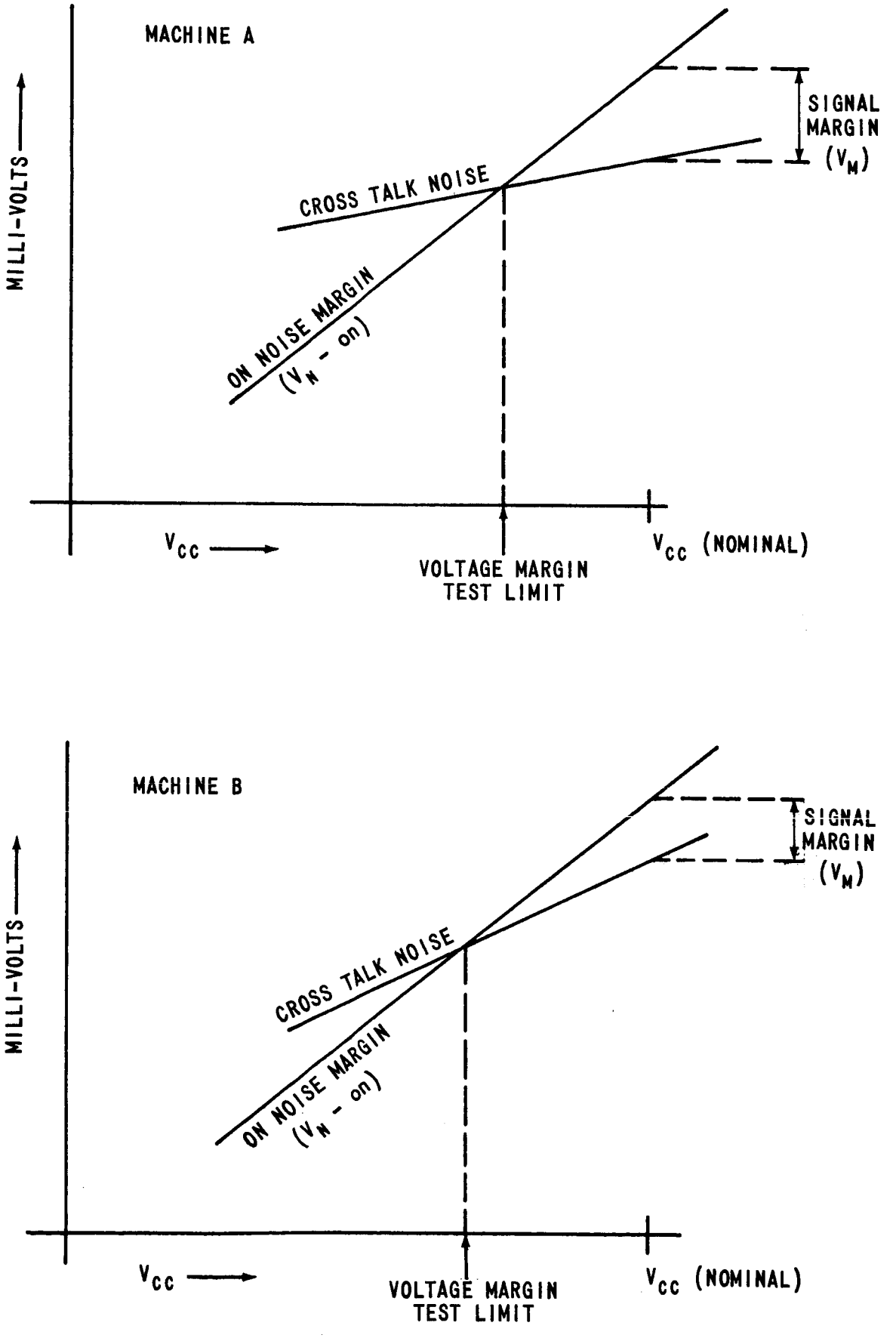


FIGURE 5 - NOISE AND ON MARGIN AS A FUNCTION OF SUPPLY VOLTAGE

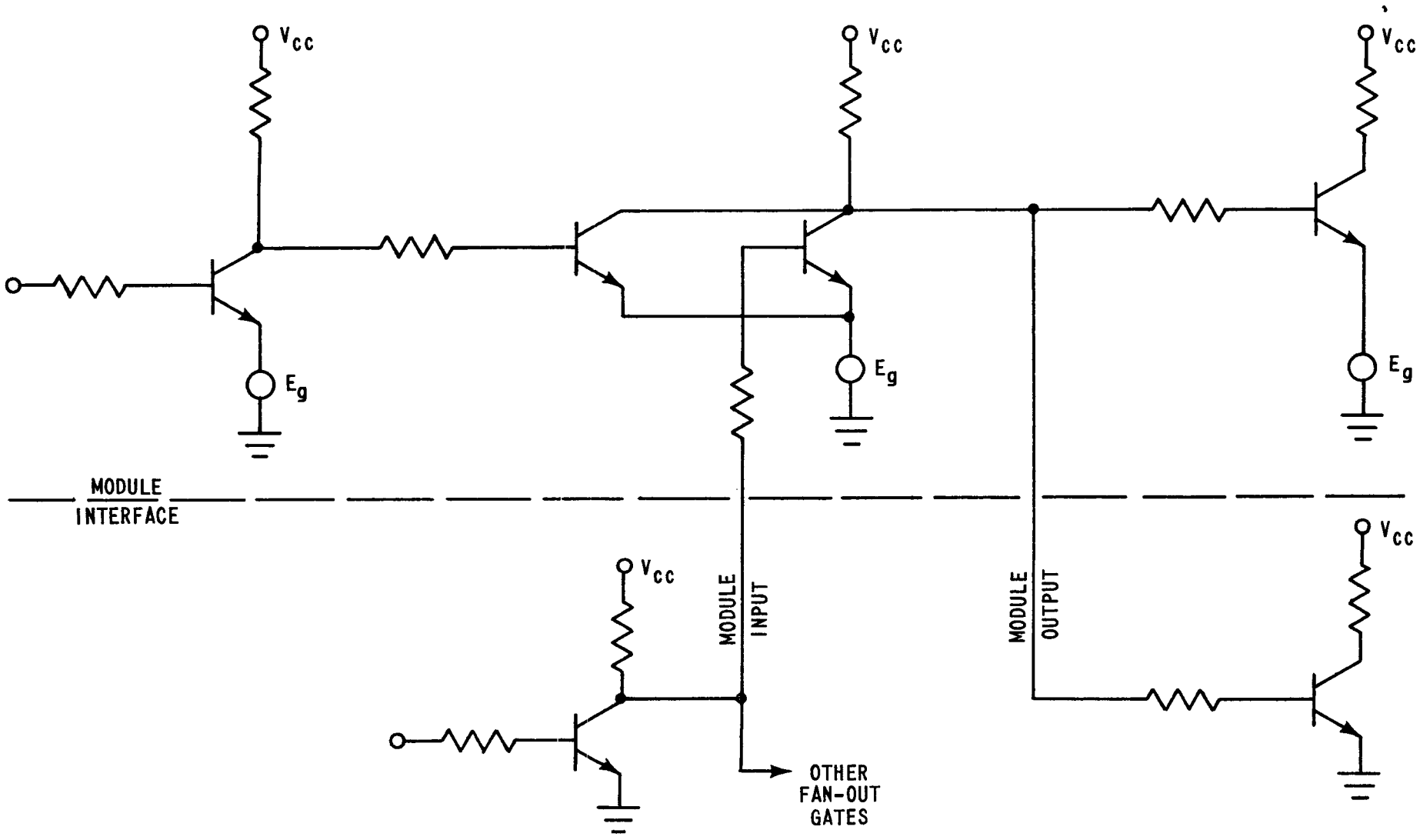


FIGURE 6 - CIRCUIT CONFIGURATION FOR GROUND BIAS MARGIN TEST

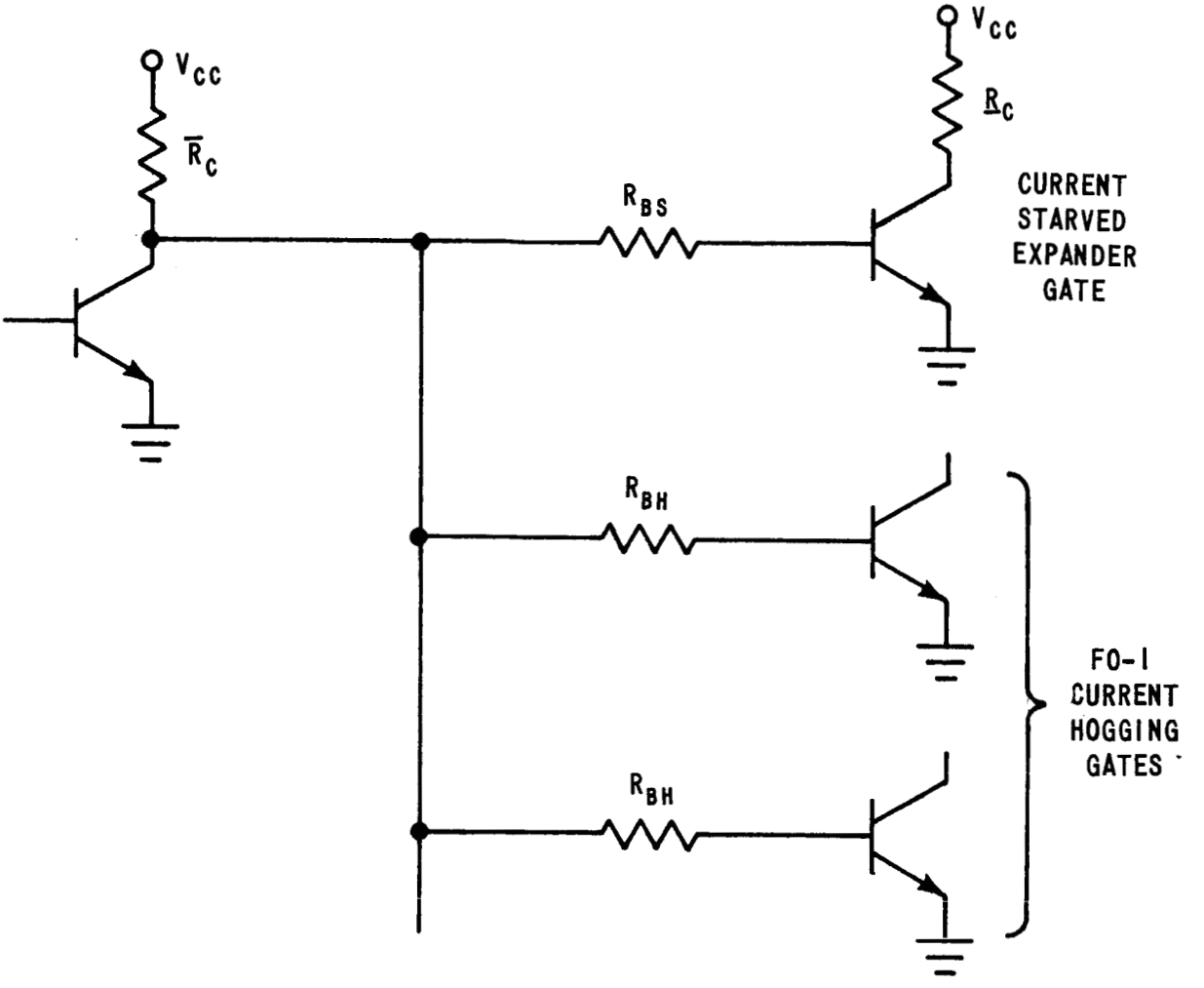


FIGURE 7 - CIRCUIT CONFIGURATION FOR WORST CASE ON NOISE MARGIN

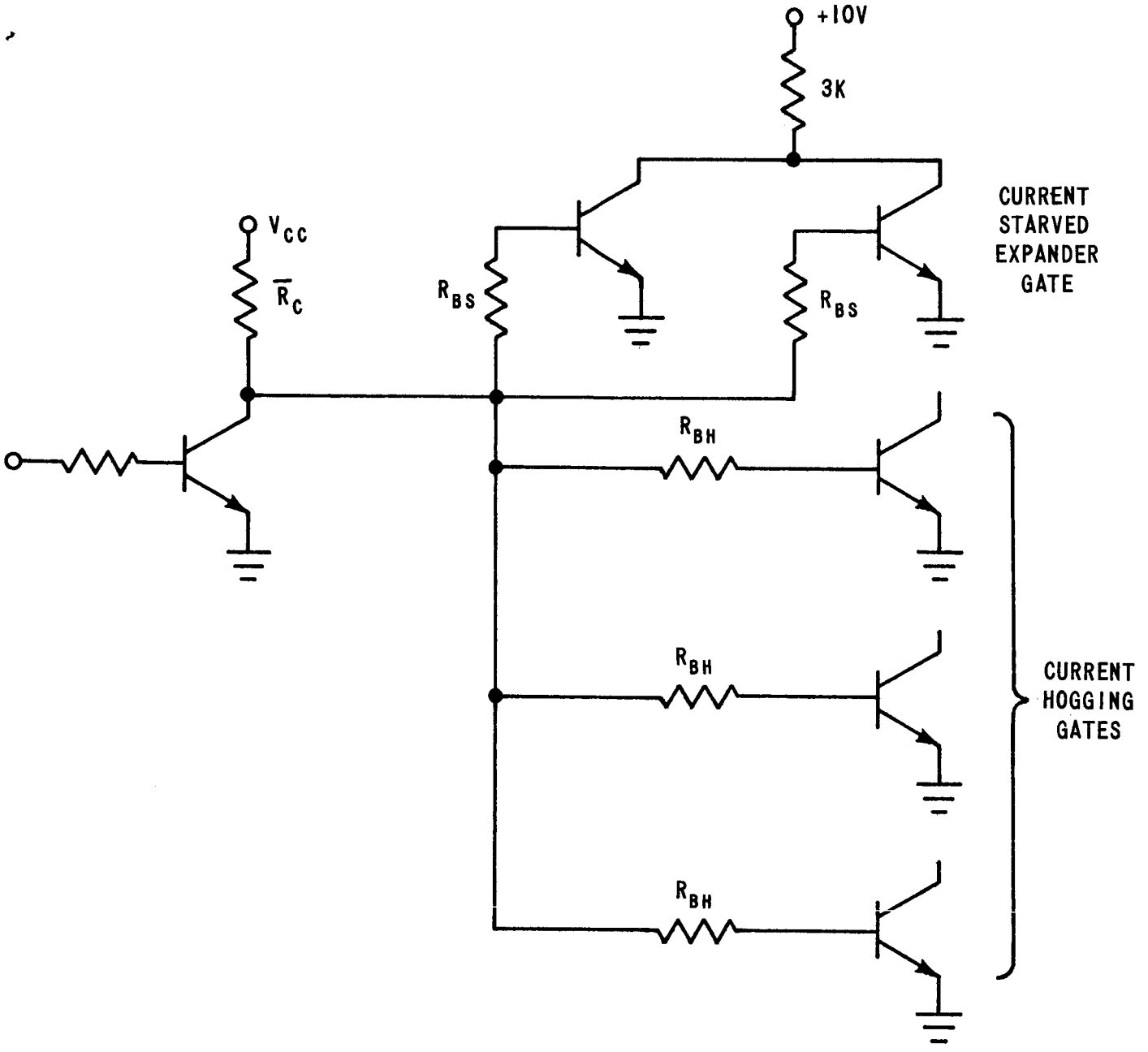


FIGURE 8 - WORST CASE INTERFACE CIRCUIT