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PROJECT APOLLO

LUNAR EXCURSION MODULE

PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM MANUAL

VOLUME II

AC ELECTRONICS
DIVISION OF GENERAL MOTORS
MILWAUKEE, WISCONSIN

ND-1021042
REV LETTER ON VOL I

APOLLO

LUNAR EXCURSION MODULE

PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM MANUAL

VOLUME II OF II

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER

BY

AC ELECTRONICS
DIVISION OF GENERAL MOTORS
MILWAUKEE, WISCONSIN 53201

NASA CONTRACT NAS 9-497

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TYPE II
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			thru I-viiiB, I-ix thru I-xB,		
			I-xii, I-xviii, I-xxxI/I-xxxJ,		
			3-2A thru 3-2C, 3-11 thru		
			3-12E, 4-437, 4-481/4-482,		
			4-539, 6-1, 6-2, 6-4, 7-13,		
			7-16, 7-16A/7-16B, 7-21/7-22,		
			8-14		
AD	11-4-68	36977	Title/I-ii, I-ivK/I-ivL, I-vii	EA	
			thru I-viii, I-xB, I-xxxI thru		
			I-xxxJ, 3-2A, 3-2L thru 3-2Q,		
			7-19/7-20, 7-21/7-22, 8-2,		
			8-6E, 8-7, 8-14 thru 8-15/8-16		
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			I-viii, I-xxxJ, 3-2A, 3-2V,		
			3-2W		
AF	1-20-69	37232	Title/I-ii, I-ivK/I-ivL, I-vii,	EA	
			I-xB, 7-16, 7-16A/7-16B,		
			8-8, 8-8A/8-8B		
AG	8-11-69	37755	Title/I-ii, 1-ivK/I-ivL, I-vii,	EA	
			1-viii, 1-xxxA, I-xxxG, I-xxxH,		
			I-xxxJ, 3-2A thru 3-2P,		
			3-2R thru 3-2U, 3-2W, 3-2X,		
			3-2Z		

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			3-2A, 3-2L, 3-2L-1/3-2L-2,		
			3-2M, 3-22M, 3-22N		
AJ	8-5-71	38455	Title/I-ii, I-ivL, I-vii, I-viii,	EA	
			I-xxxJ, 3-2A, 3-2F, 3-2G,		
			3-2H, 3-2I		
AK	7-6-72	38664	Title/I-ii, I-ivL, I-vii, I-viii,	JS	
			I-xxxJ, 3-2A, 3-2V, 3-2W		

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I-iii thru I-iv	B	I-xxxG thru I-xxxH	AG
I-ivA thru I-ivB	F	I-xxxI	Z
I-ivC thru I-ivD Added	F	1-xxxJ	AK
I-ivE	J	I-xxxi	G
I-ivF	L	I-xxxii	Y
I-ivG	S	I-xxxiii thru I-xxxiv	R
I-ivH	U	I-xxxivA	Y
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I-xxii thru I-xxiii	F	2-29 thru 2-31	Original
I-xxiv	U	2-32 Blank	Original
I-xxivA	Z	2-33	A
I-xxivB Blank	F	2-34	Original
I-xxv	AH	2-35	T
I-xxvi	W	2-36	B
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3-1 thru 3-2	H
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3-2B thru 3-2E	AG
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3-2AB Blank	K
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3-5	H
3-6	C
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3-6B Blank	C
3-7 thru 3-8	Original
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3-12F	V
3-13	Original
3-14	B
3-15	C
3-16	Original
3-17	F
3-18 thru 3-19	B
3-20	AA
3-21 thru 3-22B	AB
3-22C thru 3-22L Added	AB
3-22M thru 3-22N	AH
3-23	Original
3-24	AA
3-24A thru 3-24D Added	L
3-25	W
3-26	V
3-26A Added	V
3-26B Blank	V
3-27	AA
3-28	F
3-29	AA
3-30	B
4-1 thru 4-14	Original
4-15	W
4-16 thru 4-18	Original
4-19	T
4-20 thru 4-21	B
4-22	Original
4-23	T
4-24 thru 4-25	Original
4-26	A
4-27 thru 4-28	Original
4-29 thru 4-30	A
4-31	Original
4-32 thru 4-34	A
4-34A Added	A
4-34B Blank	A
4-34C	T
4-34D Blank	A
4-34E Added	A
4-34F Blank	A
4-34G thru 4-34I Added	A
4-34J Blank	A
4-34K Added	A
4-34L Blank	A
4-34M thru 4-34O Added	A
4-34P Blank	A
4-34Q thru 4-34S Added	A
4-34T Blank	A
4-34U Added	A
4-34V Blank	A

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
564	Implementation of Flat Pack Specifications ND 1002359A and ND 1002358B			U
631	Replace RTV-102 with RTV-109	0102679 0102689 0102690	8102752 8102755 8102754 8102766	U
653	Modification of IMU Wiring to Reduce IRIG Pre-Amp Oscillation		8102763	U
641	Non-metallic Materials Modification for DSKY	0104126	8104241	W
655	New LGC Mounting Bolts and Spacers			W
673	Redesign of DSKY Push-button Cap Housing Assembly Leaf Spring	0104126	8104241	W
678	IRIG End Cap Change	0102697	8102767 8102768	W
633	AOT Pressure Seal Protection and Other Flammability Fixes	0106049 0106048	8106069 8106073	Y
604	Incorporation of E-memory Vibration Pads			Z
688	Modification of IMU to Reduce Sporadic Oscillation of IRIG Preamps		8102773 8102774	Z
657	Conical Sunshade and Radar Shield Assembly for AOT	0106050	8106076	AC
697	AOT Harness Protective Shield	0106054	8106085	AC

LIST OF ENGINEERING CHANGE PROPOSALS (cont)

ECP No.	Functional Description	Retrofit Instruction Bulletin (RIB) No.	Kit No.	Incorporated In Manual Revision
719	Computer Alarm Module Modification, V-Fail Detection	0104132	8104248	AD
735	DSKY 1L and EL Safety Glass Fix	0104135	8104251	AD
743	New Configuration of Installation Kit			AD
757	Design Changes to Correct LEM PSA Reverse Power Problem			AE
768	DSKY EL thermal/ Vacuum Screen modification	0104138	8103954	AG
739	Addition of 4 lights on DSKY indicator panel	0104136	8103952	AG
780	Taping of AOT cable			AG
781	ECDU mounting bolt change in length	0102703	8102789	AG
815	Replace AGC Connector Assembly with a restart monitor	0102705	8102793	AH
1017 & 1032	Replace blower motor in IMU to increase reliability	-	8102796	AJ
1030	Replace ECDU modules containing 1010274 transformers to increase reliability	-	-	AJ
1040	Modification of 800 Hz 5% amplifier in PSA to eliminate amplifier oscillation during system turn-on.	-	-	AK

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ILLUSTRATIONS (cont)

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TABLES

TABLES (cont)

TABLES (cont)

3-1A LEM COMPATIBILITY

Compatibility tables 3-I through 3-IN list the LEM PGNCS components, part numbers, and dash numbers. These tables identify Apollo airborne component configurations and their compatibility to PGNCS applications, and trace Apollo airborne component configuration changes by ECP. The data is organized to assist field site personnel in determining equipment compatibility and to aid in making valid replacement decisions. Table 3-A1 lists the compatibility tables in alphabetical order according to component or assembly. An ECP matrix has also been provided in the table. The matrix is useful for determining which components or assemblies are affected by an ECP.

Table 3-A1. Compatibility and ECP Matrix

Component or Assembly	Table
AOT	3-I
CCRD	3-IA
CDU	3-IB
IMU and PTA	3-IC
Interconnect harness group	3-ID
LGC group	3-IE
LGC	
DSKY	3-IF
LGC group installation kit	3-IG
LGC test modules	3-IH
jumper modules	
rope modules	3-IJ
Nav base	3-IK
PSA	3-IL
Signal conditioner assembly (SCA)	3-IM
Signal conditioner assembly installation kit	3-IN

ECP Number

The symbol ① in the compatibility tables depicts an "OR" gate. Follow one path or the other (not both) for entry or exit from gate.

Table 3-I. AOT Compatibility (Sheet 1 of 2)

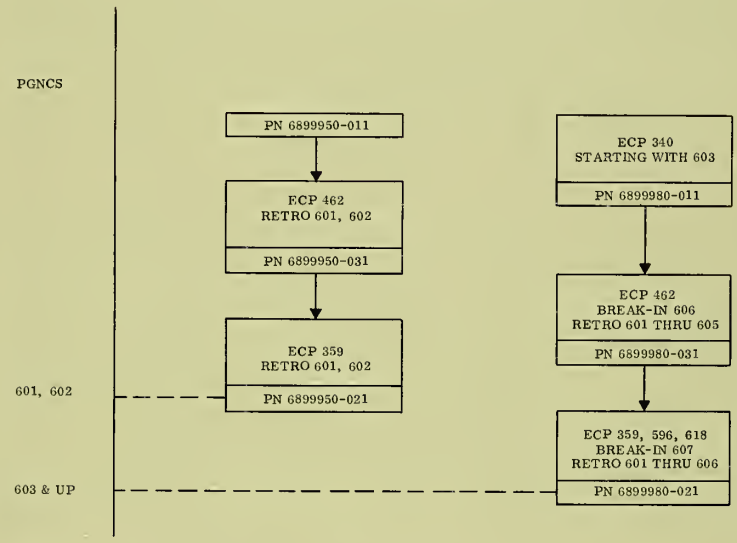
COMPONENT PART NUMBER	DASH NUMBERS FOR PA6015000	SYSTEM SERIAL NUMBERS																	
		011 / 601	021 / 602	031 / 603	041 / 604	051 / 605	061 / 606	071 / 607	081 / 608	091 / 609	101 / 610	111 / 611	121 / 612	131 / 613	141 / 614	151 / 615	161 / 616	171 / 617	181 / 618
6011000	000	X	T			NO													
	012	T	X	T		NO													
	031	C	T	C	T	NO													
	032	C	T	C	X	NO													
	041	C	T	C		NO													
	042	C	T	C		NO													
	071	NO				T													
	072	NO				T													
	073	NO				T													
	074	NO				X	T												
	081	NO				C	T		X	T									
	091	NO				C	T		C	T									
	111	NO				C	X		C	X									
		AOT High Density Filter Assembly Compatibility																	
6011856	000					X													

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used. (AOT-CCRD mounting compatibility is required. Reference ECP 422.)

ECP	DESCRIPTION
173	Reticle mount and objective lens assembly
197	Vacuum testing of AOT BREAK-IN 603
296	Connecting relay assembly BREAK-IN 602
301	Thermal instrumentation BREAK-IN 602 ONLY
318	Corrosion protection of exposed heryllium BREAK-IN 602
320	Blacken lens edges BREAK-IN 603
321	Incorporate eyepiece heaters BREAK-IN 603
353	Change pressure seal material BREAK-IN 603
360	Incorporate eyepiece locking lever BREAK-IN 603
410	Reposition eyepiece locking lever BREAK-IN 606 RETRO 605
421	Modify lens housing BREAK-IN 605 RETRO 604
422	CCRD mounting change BREAK-IN 606 RETRO 605
454	Improved pinning methods BREAK-IN 604
473	Incorporate shield to eliminate light scatter BREAK-IN 609 RETRO 605 through 608

ECP	DESCRIPTION
512	AOT high density filter assembly (sun filter) BREAK-IN 605
539	AOT reticle lamp change BREAK-IN 612 RETRO 604 through 611
540	AOT reticle knob change BREAK-IN 612 RETRO 604 through 611
542	AOT eyeguard plug BREAK-IN 612 RETRO 604 through 611
543	AOT counter moisture proofing and illumination BREAK-IN 612 RETRO 604 through 611
582	LTA-8 modifications AFFECTS 602 ONLY
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
633	AOT pressure seal protection and other flammability fixes BREAK-IN 612 RETRO 605 through 611
657	Conical sunshade and radar shield assembly for AOT BREAK-IN 618 RETRO 605 through 607, 609 through 617
697	AOT harness protective shield BREAK-IN 619 RETRO 605 through 607, 609 through 618
780	Taping of AOT cable assembly RETRO 605 through 618

Table 3-IK. Nav Base Compatibility (Sheet 2 of 2)



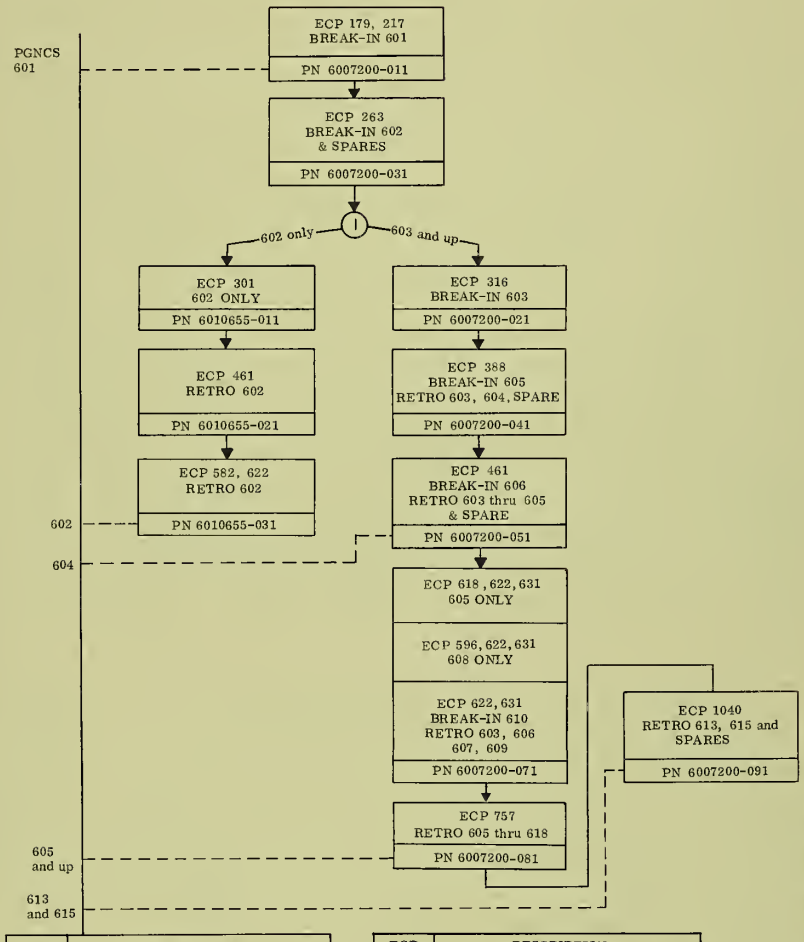
ECP	DESCRIPTION
340	Nav base redesign STARTING WITH 603
359	Replacement of IMU mounting bolts BREAK-IN 607 RETRO 601 thru 606
462	Addition of ground strap to LM nav base BREAK-IN 606 RETRO 601 thru 605
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY

Table 3-IL. PSA Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000 / SYSTEM SERIAL NUMBERS 011/601	021/602	031/603	041/604	051/605	061/606	071/607	081/608	091/609	101/610	111/611	121/612	131/613	141/614	151/615	161/616	171/617	181/618
6007200	011	X	T		T →														
	021	C	T		T →														
	031	C	T		T →														
	041	C	T		T →														
	051	C	T		X	T →													
	071	C	T		C	T →													
	081	C	T		C	X →													
	091	C	T		C →									X	C	X	C →		
6010655	011	T →			T →														
	021	T →			T →														
	031	T	X		T →														

X Required per print
C Compatible: as good as or better than print requirement. See ECP flow chart.
T Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO CANNOT be used.

Table 3-IL. PSA Compatibility (Sheet 2 of 2)



ECP	DESCRIPTION
179	G and N filter change BREAK-IN 601
217	Delete signal conditioner power supply assembly BREAK-IN 601
263	New helicoil and screw BREAK-IN 602 and spare
301	Thermal instrumentation BREAK-IN 602
316	Potting voids in header BREAK-IN 603
388	Corrosion and outgassing protection BREAK-IN 605 RETROFIT 603, 604, spare 1
461	Change gimbal servo amplifier BREAK-IN 606 RETROFIT 602 thru 605
582	LTA-8 modifications AFFECTS 602 ONLY

ECP	DESCRIPTION
596	LM-2 modifications AFFECTS 608 ONLY
618	LM-3 modifications AFFECTS 605 ONLY
622	Non-metallic materials flammability modification for PSA BREAK-IN 610 RETROFIT 602, 603, 605 thru 609
631	Replace RTV-102 with RTV-109. ECP 631 should be incorporated in PN 6007200-071 and above. ECP 631 does not affect part number change. It may be included in other part number assemblies.
757	Design changes to correct LEM PSA reverse power problem RETROFIT 605 thru 618
1040	Modification of 800 hz 5% amplifier in power and servo assembly to eliminate amplifier oscillation during system turn-on. RETROFIT 613, 615 and spares

Table 3-IM. Signal Conditioner Assembly Compatibility (Sheet 1 of 2)

COMPONENT PART NUMBER		DASH NUMBERS FOR PN6015000									SYSTEM SERIAL NUMBERS								
		011 601	021 602	031 603	041 604	051 605	061 606	071 607	081 608	091 609	101 610	111 611	121 612	131 613	141 614	151 615	161 616	171 617	181 618
6007010	011	X	T	X*	X	T	NO →		T	NO →									
	021	C	X →		C	X	NO →		X	NO →									
6007013	011	NO →				→	T →		NO	T →									
	021	NO →				→	X →		NO	X →									

X	Required per print
C	Compatible: as good or better than print requirement. See ECP flow chart.
T	Not as good as print requirement, but can be used for testing. See ECP flow chart.
NO	CANNOT be used.
*	See note on sheet 2 of 2.

Control pulse TMZ detects a minus zero quantity placed onto write lines WL16 through WL01. Control pulse TMZ is first gated by signal PHS3 to clear the branch 2 flip-flop and then by signal PHS4 to set the flip-flop if minus zero exists.

Control pulse TSGN2 tests write line WL16 for positive and negative values. If signal WL16 is present, a negative quantity has been placed onto the write lines. Control pulse TSGN2 is first gated by signal PHS3 to clear the branch 2 flip-flop and then by signal PHS4 to set the flop-flop if signal WL16 is present.

Signal BR2 is produced when the branch 2 flip-flop is set. Signal MBR2 is sent to the peripheral equipment to indicate the state of the branch 2 flip-flop.

The outputs of the branch flip-flops are used by the crosspoint generator circuits to produce control pulses. In addition, the branch decoder circuit detects states 01, 01 or 10, 10, and 00, and produces signals BR1B2, BRD1F, BR12B, and BR1B2B, respectively.

The special instruction flip-flop is used to control RELINT, INHINT, and EXTEND instructions. These special instructions are address-dependent and identified by order codes 00.0003, 00.0004, and 00.0006, respectively. These order codes are never entered into register SQ. Instead, they are entered into register G and recognized when certain subinstructions are being executed. The subinstructions which recognize the special instruction order codes produce signal TSUD0. They are STD2, TC0, TCF0, RSM3, MP3, BZF0, and BZMF0. Each of these subinstructions fetch the next instruction to be executed. When doing so, signal TSUD0 and time pulse T7PHS4 are ANDed. The resulting crosspoint pulse tests the decoded output of register G for octal 3, 4, or 6 and produces signal RELPLS, INHPLS, or EXTPLS if the respective octal quantity is contained in register G. Flip-flop A is set by signal RELPLS, INHPLS, or EXTPLS at time pulse T7PHS4 and is reset by time pulse T12. At time pulse T08 of these fetching subinstructions, control pulse RAD is produced by signals TSUD0 and T08 and converted into signal RADRZ if flip-flop A is set, or into signal RADRG if the flip-flop is not set. Signal RADRZ is then converted into control pulses RZ and ST2 which cause subinstruction STD2 to be executed. Signal RADRG, produced when anything other than a special instruction is being fetched for execution, is then converted into control pulse RG which, in conjunction with control pulse WB, transfers the basic instruction word to the central processor register B. Signal EXTPLS which set flip-flop A and produces control pulses RZ and ST2 also sets the FUTEXT flip-flop in the register SQ circuit. Similiarly, signal INHPLS sets the INHINT flip-flop in the register SQ control and signal RELPLS resets the INHINT flip-flop.

4-5.5 CENTRAL PROCESSOR. The central processor performs all arithmetic operations required of the computer, initiates the selection of and buffers all information coming from and going to memory, checks for correct parity on all words coming from memory, and generates parity for all words written into memory.

4-5.5.1 Central Processor Functional Description. The central processor consists of eight 16 bit flip-flop registers with service gates, a 12 bit memory address register and decoder, the write amplifiers, and parity logic. The flip-flop registers to be discussed are special and central registers (A, Q, Z, and L) which are addressable, register B, the memory buffer register G, and registers X and Y which comprise the arithmetic unit or adder. In addition, there are three addressable bank registers that aid in identifying memory addresses. These registers consist of a 3-bit erasable bank (EB) register, a 5-bit fixed bank (FB) register, and a 3-bit fixed bank extendible (FEXTB) register.

Data words and basic instruction words consist of 16 bits when stored in fixed or erasable memory. The word format is illustrated in figure 4-137. The formats presented in this illustration indicate the word as it actually appears in the hardware. The concept employed by programmers when indicating a data word or basic instruction word differs from that shown in figure 4-137.

An instruction word in memory (a) contains the operation code (OC) in bit positions 16, 14, and 13, parity (P) in bit position 15, and the data address (A) in bit positions 1 through 12. When the word is read out of memory, the parity bit is applied directly to

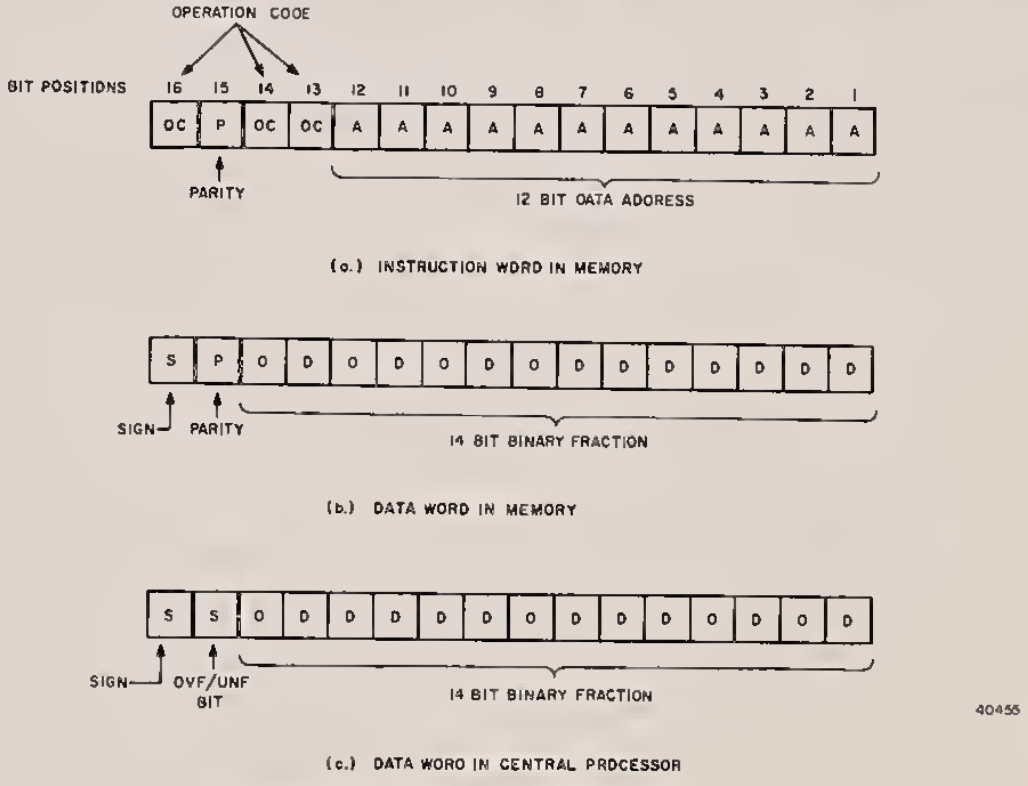


Figure 4-137. Word Formats

the parity logic. There is no other manipulation of the parity bit within the central processor. The word contains the same quantity in bit positions 15 and 16 when residing in the central processor. The operation code is applied to the sequence generator, and the 12 bit address to the memory address register. Program listings indicate the order of an instruction word using six octal bits as follows:

0 6501 0

The first bit (0) represents the operation code and includes bit positions 16, 14, and 13. The next four bits (6501) represent the relevant address of the instruction word in positions 12 through 1. The bit at the extreme right is the parity bit (position 15).

A data word in memory (b) contains the sign in bit position 16, parity in bit position 15, and the value bits in positions 14 through 1. When transferred to the central processor, the parity bit is again applied to the parity logic. A data word in the central processor (c), contains the sign entered into bit positions 15 and 16. Position 15 then becomes an indication of overflow or underflow. Program listings indicate the order of a data word using six octal bits as follows:

50106 0

The first octal bit (5, which is 101 in binary) includes bit positions 16, 14, and 13. In this case, the sign is minus indicating a negative number, and positions 14 and 13 are the two high order bits of the 14 bit binary fraction. The remaining 12 bits are represented by octal bits 0106. The parity bit is at the extreme right.

Each flip-flop register consists of 16 bit positions, which is consistent with the word format discussed previously. The register service gates control the write-in and read-out operations of each register. (See figure 4-138.) The bit positions are cleared coincident with write-in. Normally, data from the write lines is applied to the service gates, and is written into a particular register under control of a write control pulse from the sequence generator. For example, data from the write lines applied to register A service is written into register A coincident with write control pulse WA. Information in the register is read out by read control pulse RA. Data is exchanged between registers in this manner by reading out one register and writing into another simultaneously. Some of the flip-flop registers have additional conditions under which information is written in. Under program control, an associated address can be generated to write into and read out of each of these registers. Registers A, Q, Z, and L are addressable and are referred to as special and central registers.

Registers A (accumulator), L (low order product), Q, and X and Y (arithmetic unit or adder) are primarily involved in arithmetic operations. The adder processes two quantities; the quantity entered into Y and one of three quantities (+1, -1, +2) entered into X dependent on the instruction being executed. Registers Z and B are essentially storage elements in that they store the operation or step to be performed next in the program.

Register G is normally controlled by the service gates and control pulses WG and RG. However, under program control and coincident with an associated address, a word entered into register G is manipulated by the editing control section. Register G buffers all information read out of memory into the central processor, and buffers all information written into memory from the central processor. A word transferred from memory (SA01-SA16) as a result of selection through the memory address register is deposited directly into the bit positions of register G. The word is read out to the write lines under eontrol of read pulse RG. A word being written into erasable memory (GEM01-GEM16) is buffered through G from the write lines by control pulse WG. Editing control allows a word entered into register G to be cycled or shifted (as a function of address) to accomplish specific program manipulations.

The parity bit (SAP) is entered into the parity logic on a read-out from memory, and is used to indicate correct parity. A parity alarm oocurs in case of incorrect parity. There is no manipulation of the parity bit within the central processor. The parity logic also generates a parity bit (GEM15) when a word is written into erasable memory. Odd parity is used in the computer; therefore, the total number of ONE's in the word including parity is odd.

The memory address register (S) aecepts the 12 bit address contained in an address word. The outputs of this register are decoded by the decoding logic, and selection signals are generated to select the location in memory specified by the address. The content of S does not always uniquely determine the address of the memory word. The locations in memory, particularly fixed memory, beyond the capacity of register S are seleeted by the content of S in conjunction with the erasable, fixed and/or fixed extendible bank registers.

Data is transferred between registers of the central processor or from the central processor to other portions of the system through the write amplifiers. There are 16 write amplifiers, each of which is associated with one bit position in each of the registers. Data is applied to the write amplifiers as a result of readout from a flip-flop register or from other functional areas. The data is merely ORed and becomes available on the write lines as outputs WL01-WL16. Inputs to the write amplifiers from other functional areas include the content of the erasable and fixed bank registers, inputs representing the addresses of the input counters in priority control, program interrupt addresses, control pulses from the sequence generator which are used during specific instructions, information from the input/output channels including the real time word, the start address, and the word from the CTS during test.

Word formats and data flow to and from the three bank registers are illustrated in figures 4-138A and 4-138B. All three registers are addressable. The erasable bank register supplements the content of S to control the address decoder and to select erasable memory addresses. The fixed bank register and the fixed bank extendible register control the fixed address generator, and select fixed memory addresses in conjunction with the address decoder output. As illustrated in figures 4-138, 4-138A, and 4-138B, the bank registers are serviced similar to the other central processor registers with one major difference. The erasable and fixed bank registers receive inputs directly from the adder service as well as from the write amplifiers.

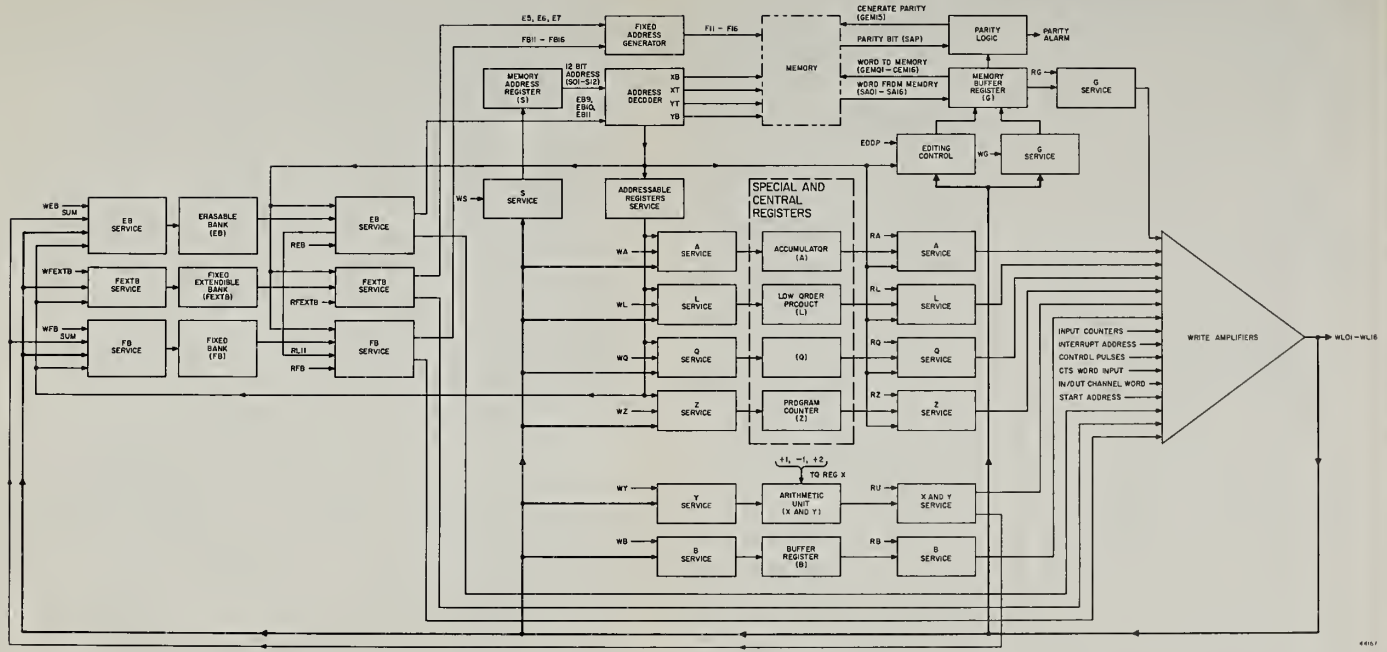


Figure 4-138. Central Processor, Functional Diagram

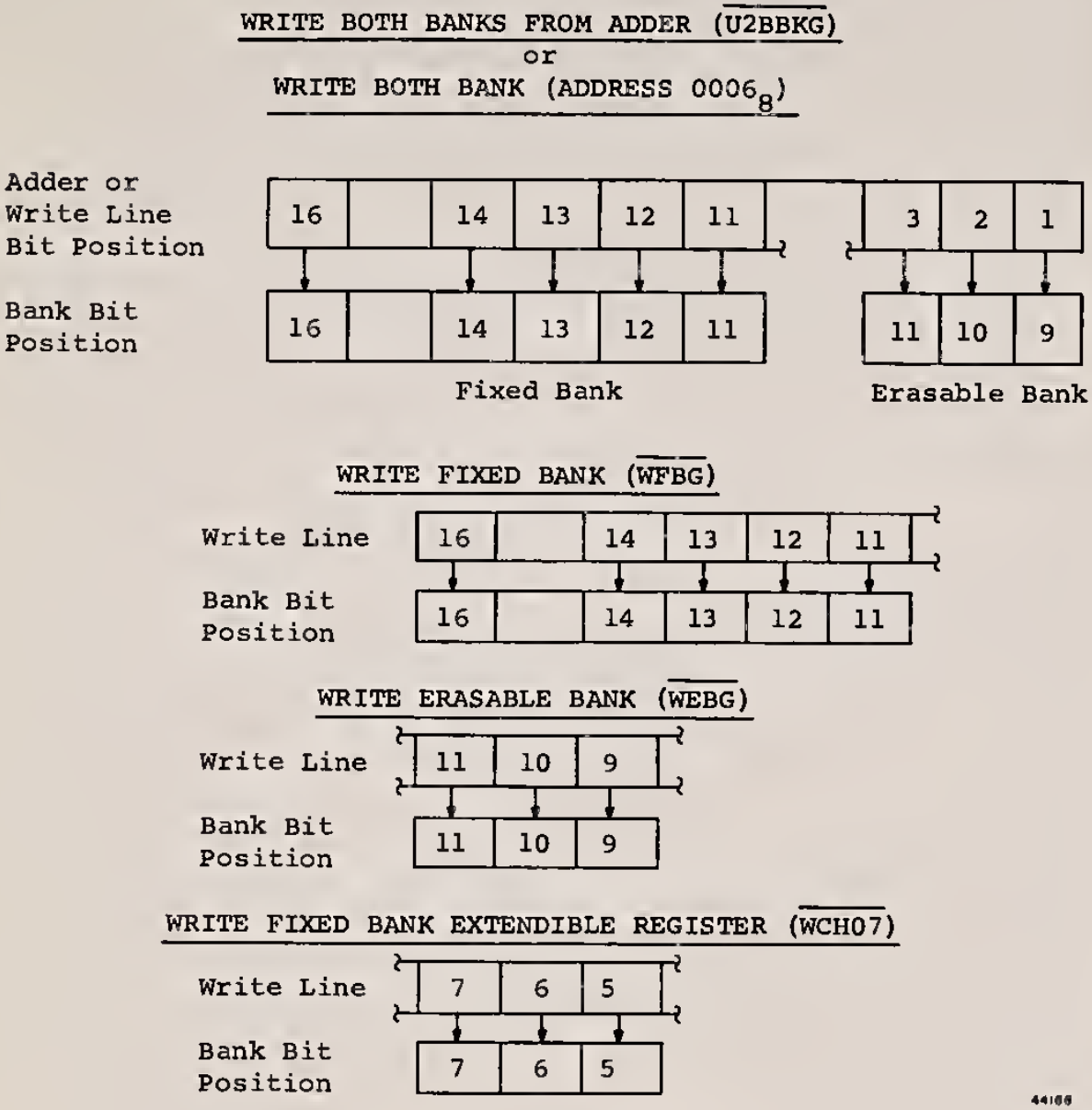


Figure 4-138A. Data Flow to Erasable, Fixed, and Fixed Extendible Registers

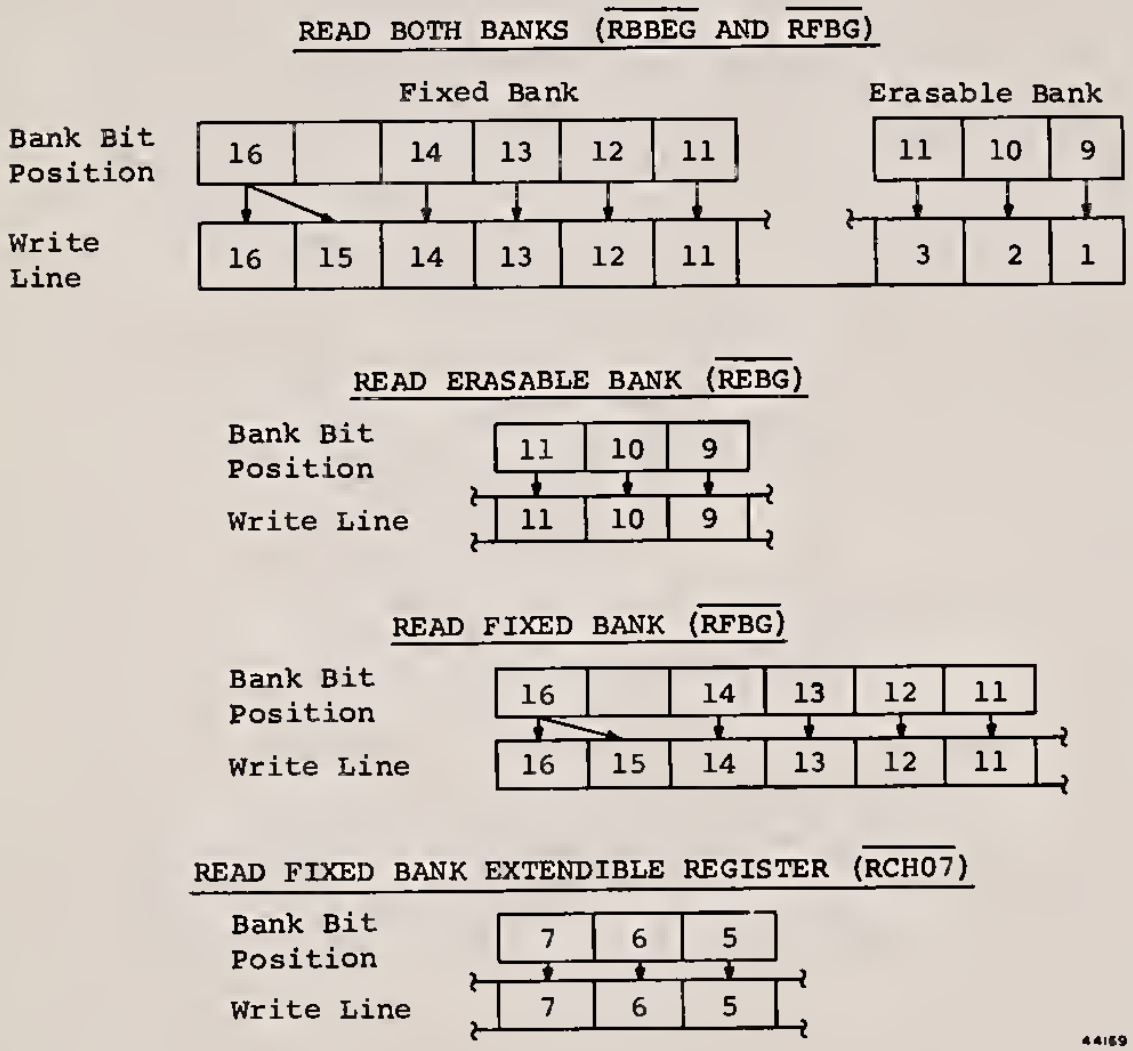


Figure 4-138B. Data Flow from Erasable, Fixed, and Fixed Extendible Registers

4-5.5.2 Flip-Flop Register Operation Detailed Description. A single bit position of flip-flop registers Q and Z is illustrated in figure 4-139. The description in the following paragraphs details operation of these bit positions, which are identical to all flip-flops in both registers. The concepts presented in this discussion are basic to all flip-flop registers in the central processor. Functional differences between the registers are described under the specific register headings.

Each of the flip-flop registers has a capacity of 16 bits. Four bit positions of each register are contained in each of four identical bit modules (A8-A11). For

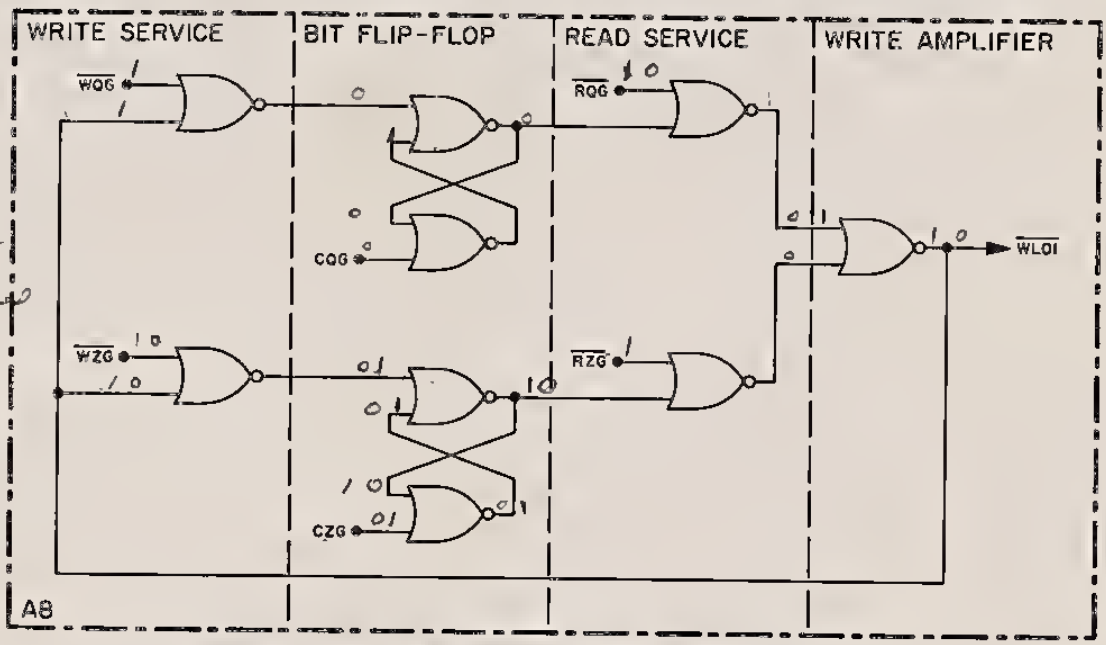


Figure 4-139. Flip-Flop Register, Single Bit Positions

example, module A8 contains bits 1 through 4 of all registers, module A9, bits 5 through 8, etc. Each bit position of the registers consists of a bit flip-flop and the write service and read service gates. The bit output is applied to an associated write amplifier. The entire register is cleared by a clear or reset pulse (CQG or CZG) applied directly to the reset input of each bit position. Information is written into the register from the write lines ($\overline{WL01}$) when the write signal ($\overline{WQG}$ or $\overline{WZG}$) enables the write service gate. The flip-flop is cleared and immediately written into. The read signal enables the read gate and causes the information stored in the flip-flop to be placed on the write lines. The write line outputs are labeled $\overline{WL01}$ through $\overline{WL16}$ corresponding to the bit positions of the registers. By enabling the read gates of register Z, and the write gates of register Q simultaneously, information is transferred between the two registers. This can be accomplished between any two registers in the central processor.

4-5.5.2A Bank Registers Operation Detailed Description. Each bit position of the bank registers operates in a manner similar to eacb bit position of the flip-flop registers. The bank registers service section generates write, clear, and read signals, which function as the related signals for the flip-flop registers.

The erasable and fixed bank register flip-flops are contained in module A15, and the fixed bank extendible register flip-flops are contained in module A23. The erasable bank register contains 3 bits and can be written into directly from the write amplifiers, or can receive inputs directly from the adder. If gated from the adder, the erasable bank register bit inputs are $\overline{\text{SUMA01}}$ tbrough $\overline{\text{SUMA03}}$ and complements $\overline{\text{SUMB01}}$ tbrough $\overline{\text{SUMB03}}$. The fixed bank register has 5 bits and receives corresponding SUM signals from tbe adder. The 3-bit fixed bank extendible register does not receive inputs from the adder. It is controlled like the input registers discussed in the input/output section.

4-5.5.3 Register Service Gates. Information is transferred into and out of the flip-flop registers under control of write, clear, and read signals generated by associated write and read service gates for each register. Inputs to the service gates consist of write and read control pulses from the crosspoint matrix of the sequence generator and timing signals $\overline{\text{WT}}$, $\overline{\text{CT}}$, and $\overline{\text{RT}}$ (write time, clear time, and read time respectively) from the timer.

The write signals for each register are derived by gating a write control pulse and timing signal $\overline{\text{WT}}$. The clear pulse is derived as a function of the write signal and timing signal $\overline{\text{CT}}$. The read signal for eacb register is derived by gating a read control pulse and timing signal $\overline{\text{RT}}$. The write, clear, and read signals for register Z are illustrated in figure 4-140 and discussed in the following paragraphs.

Write control pulse $\overline{WZ}$ from the sequence generator is a 0.75 microsecond pulse and is illustrated as occurring at time 5 (T05) of a particular instruction. This control pulse coincident with timing signal $\overline{WT}$ results in 0.50 microsecond write signal $\overline{WQG}$ from the write service gates. The clear or reset pulse, CQG, is generated by gating the write signal $\overline{WQG}$ and timing $\overline{CT}$. This is a 0.25 microsecond positive transition and occurs during the first half of the enabling portion of the write signal as shown in figure 4-140. Thus, the flip-flop is cleared and the register immediately written into. The clear pulse occurs only when a write signal is generated; therefore, information written into the register is retained until the next write signal occurs.

The read control pulse $\overline{RZ}$, similar to the write control pulse, is 0.75 sec wide, and is shown in figure 4-140 as occurring at time 8 (T08). This signal from the sequence generator is gated with timing signal $\overline{RT}$ to produce read signal $\overline{RZG}$ from the read service gates. The read signal enables the read gates and causes information in the registers to be placed on the write lines. The read signal does not destroy the content of the register. Information is retained in each flip-flop and can actually be read out several times until the next write signal occurs. A detailed discussion of the write and read service for each register is included with the discussion on the flip-flop registers.

4-5.5.3.1 Addressable Registers Service. The four special and central registers (A, L, Q and Z) and the bank registers are addressable registers in that write, clear, and read signals can be generated as a function of an associated address supplied by the program. This is in addition to the write and read signals generated normally. These addresses are 0000 for register A, 0001 for register L, 0002 for register Q, 0005 for register Z, 0003 for the erasable bank register, 0004 for the fixed bank register, and 0007 for the fixed extendible bank register. Address 0006 enables both erasable and fixed bank registers simultaneously.

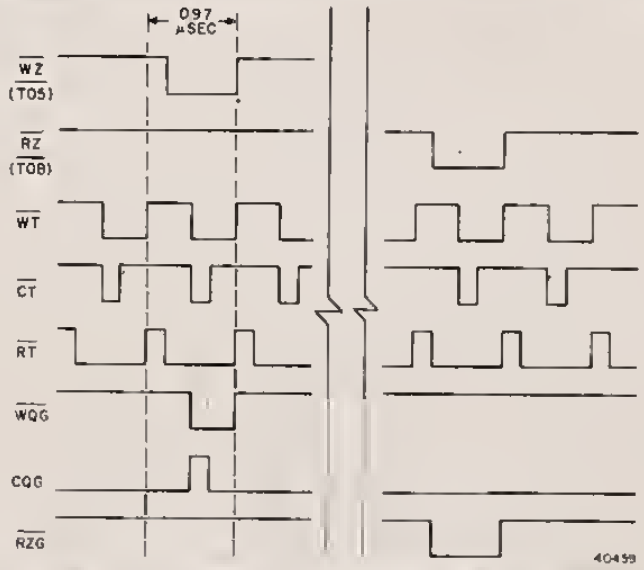


Figure 4-140. Write, Clear, and Read Timing

Write and read control signals are generated for the addressable registers by the logic illustrated in figure 4-141. Inputs $\overline{WSC}$ and $\overline{RSC}$, control pulses generated in the sequence generator, gate with timing signals $\overline{WT}$ and $\overline{RT}$ respectively to produce write signal $\overline{WSCG}$ and read signal $\overline{RSCG}$. These signals are applied to the service gates of each of the four registers along with the address supplied by the program. The register to be written into and readout of is determined by the address. Signal $\overline{SCAD}$ enables the gates if any one of octal addresses 0000 through 0007 is present. There is no access to memory at this time since signal SCAD is a logic ONE and inhibits erasable memory cycle timing. For all addresses above octal 0007, at least one of the inputs to gates 39345 and 39346 is a ONE and inhibits the addressable register service.

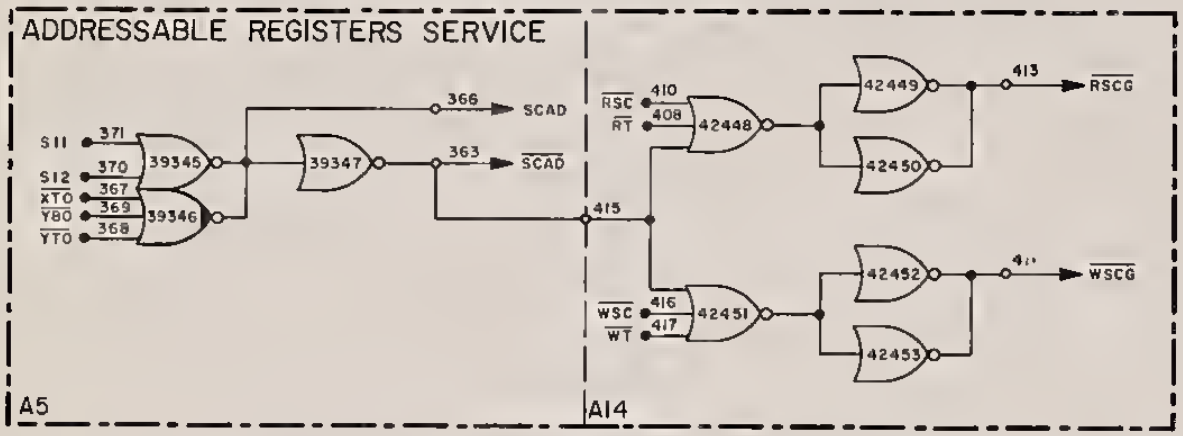


Figure 4-141. Addressable Registers Service

4-5.5.4 Register A. Register A (see figure 4-142), or accumulator, normally retains information between the execution of individual instructions. This is accomplished by write signal $\overline{WAG}$ from the write services (figure 4-143) which gates information on the write lines ($\overline{WL01}$ - $\overline{WL16}$) into register A. The write signal is generated as a function of control pulse $\overline{WA}$ from the sequence generator and timing signal $\overline{WT}$, or by octal address 00000 (indicated by $\overline{XB0}$) supplied by program and control pulse $\overline{WSCG}$. Either write condition causes the clear pulse CAG to be generated and clear the register prior to write-in. Write signal $\overline{WALSG}$ is generated to write into register A as a function of control pulse $\overline{ZAP}$. This latter control pulse is produced during multiply subinstructions MP1 and MP3 during which time the accumulator is used in conjunction with register L to form a double precision quantity accumulator. Write signal $\overline{WALSG}$ causes the write line inputs to be deposited into register A as indicated in table 4-LXXVI (the bit content of register L is also shown).

This manipulation of data accomplishes the required shifting during a multiply instruction.

4-5.5.5 Register L. Register L (see figure 4-142) functions during instruction MP (multiply) and DV (divide) and during the addition of double precision quantities. During instruction MP, register L holds the low order product; during instruction DV, the remainder.

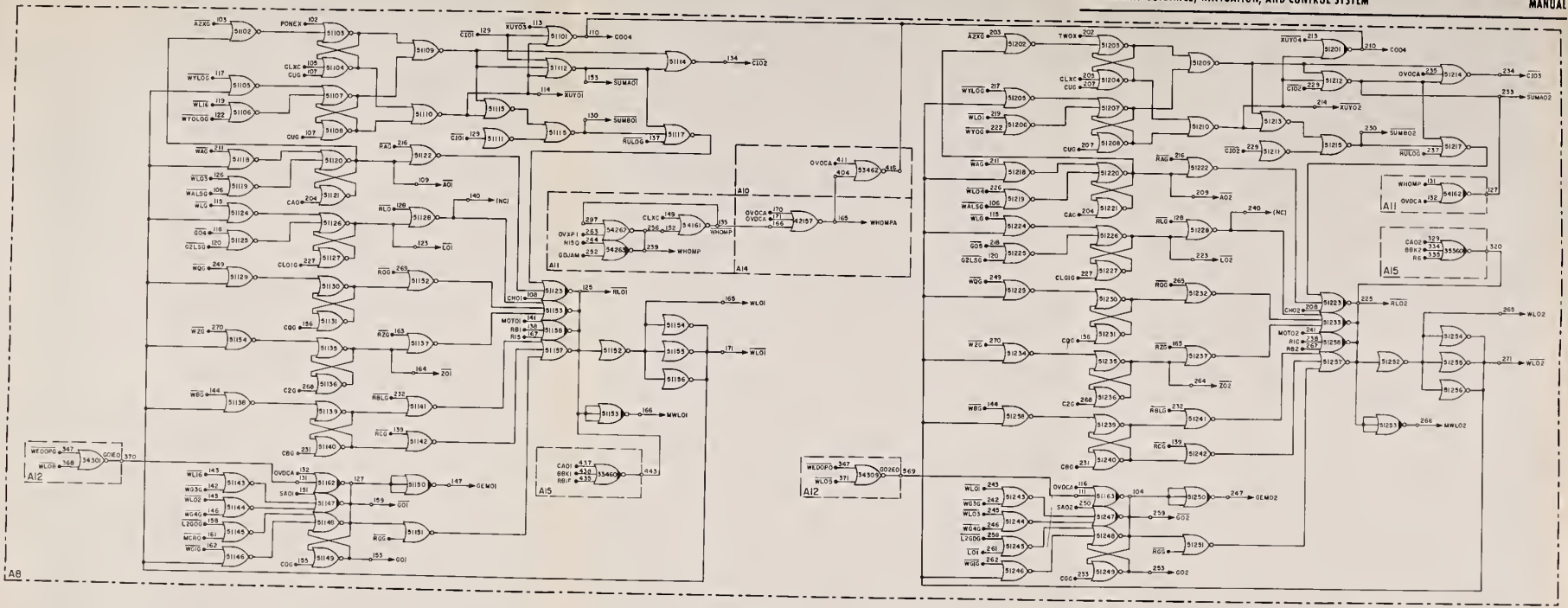


Figure 4-142. Flip-Flop Registers, (Sheet 1 of 8)

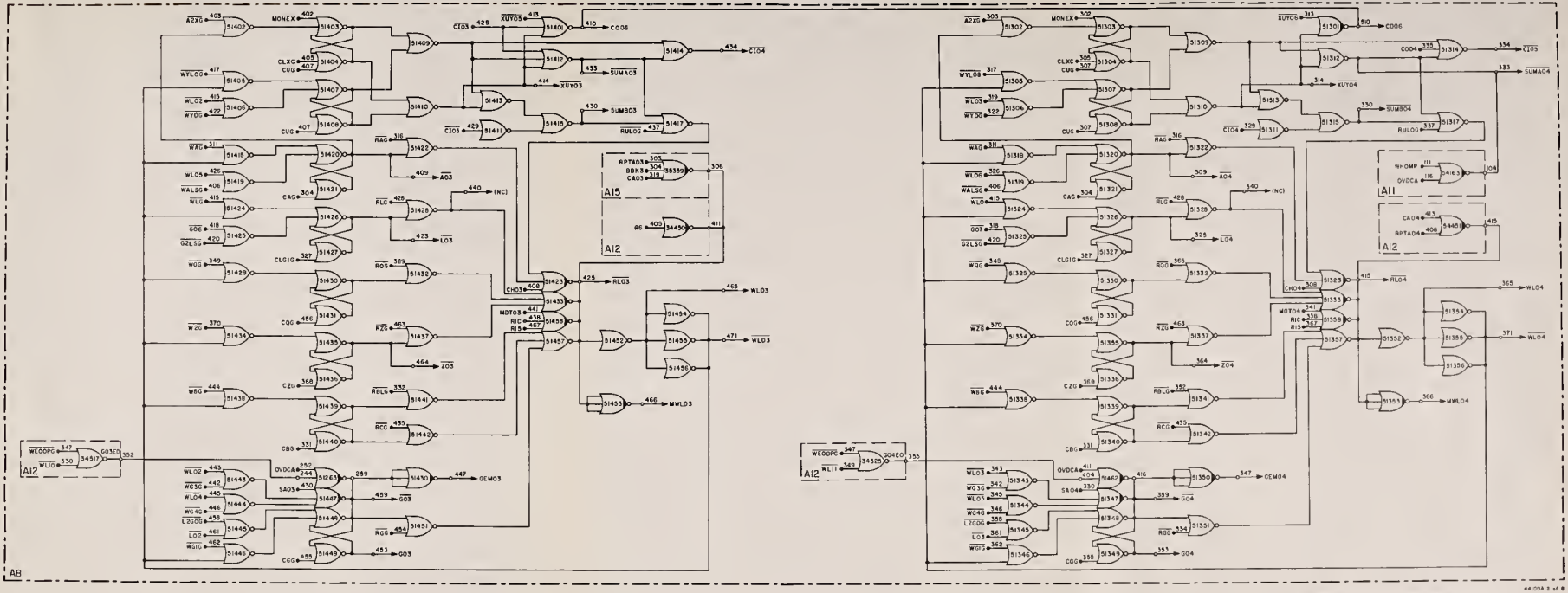


Figure 4-142. Flip-Flop Registers
(Sheet 2 of 8)

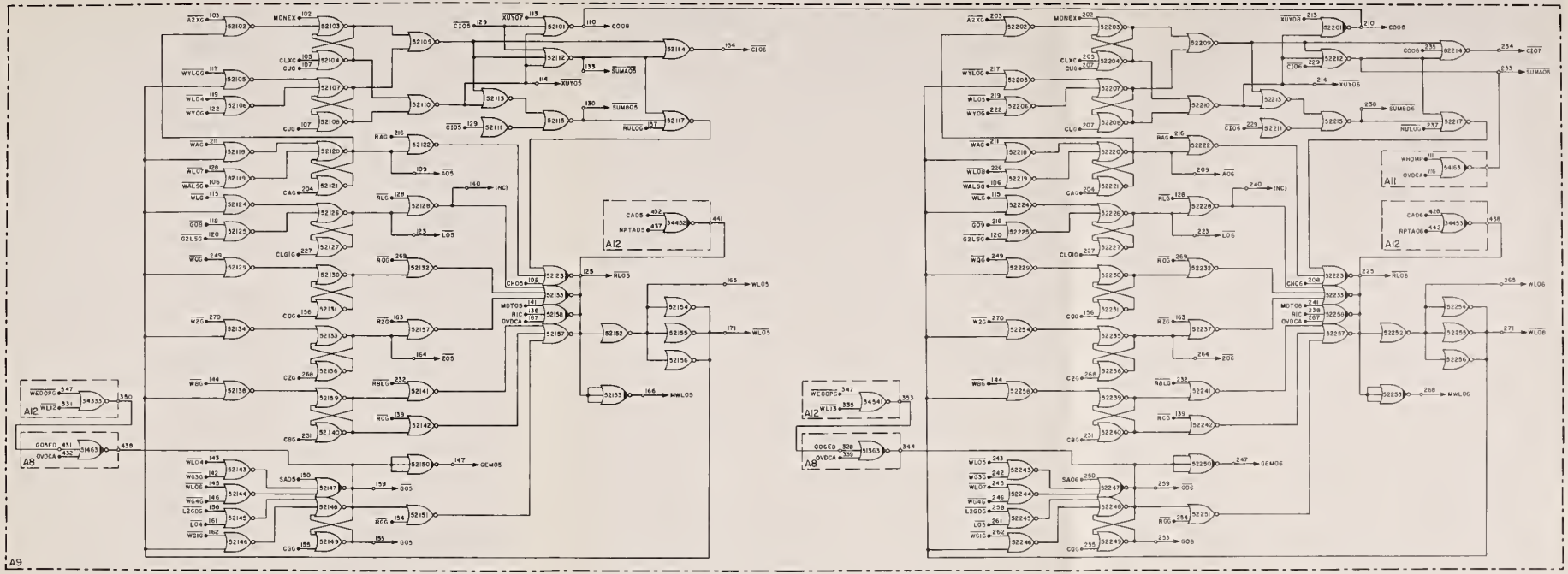


Figure 4-142. Flip-Flop Registers, (Sheet 3 of 8)

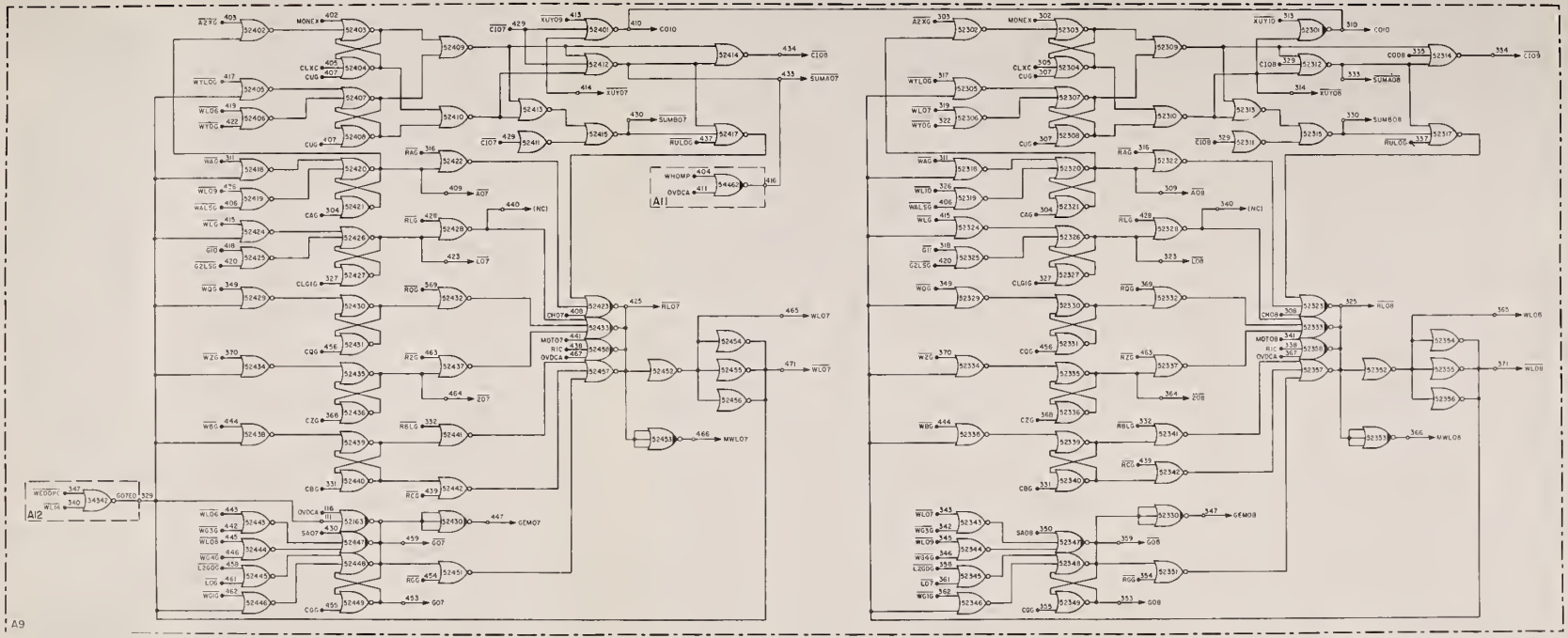


Figure 4-142. Flip-Flop Registers, (Sheet 4 of 8)

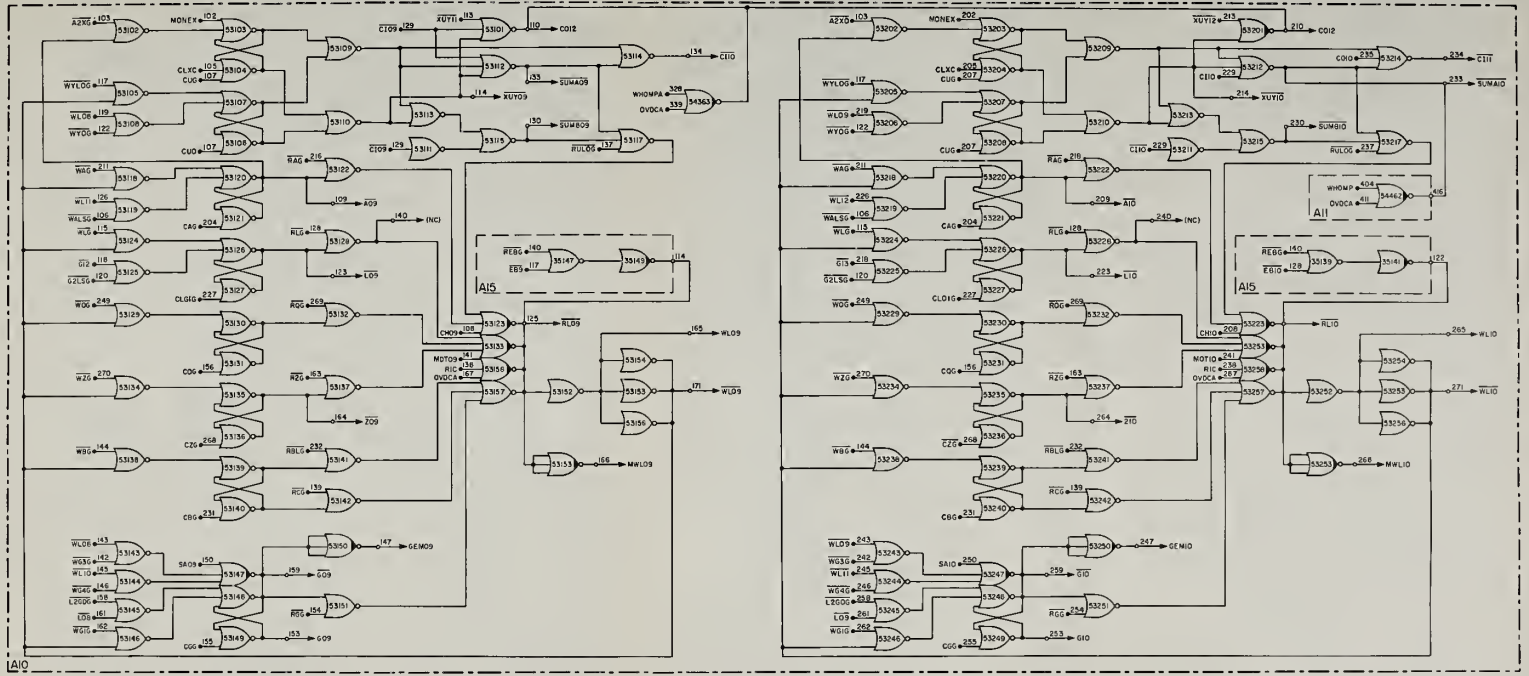


Figure 4-142. Flip-Flop Registers, (Sheet 5 of 8)

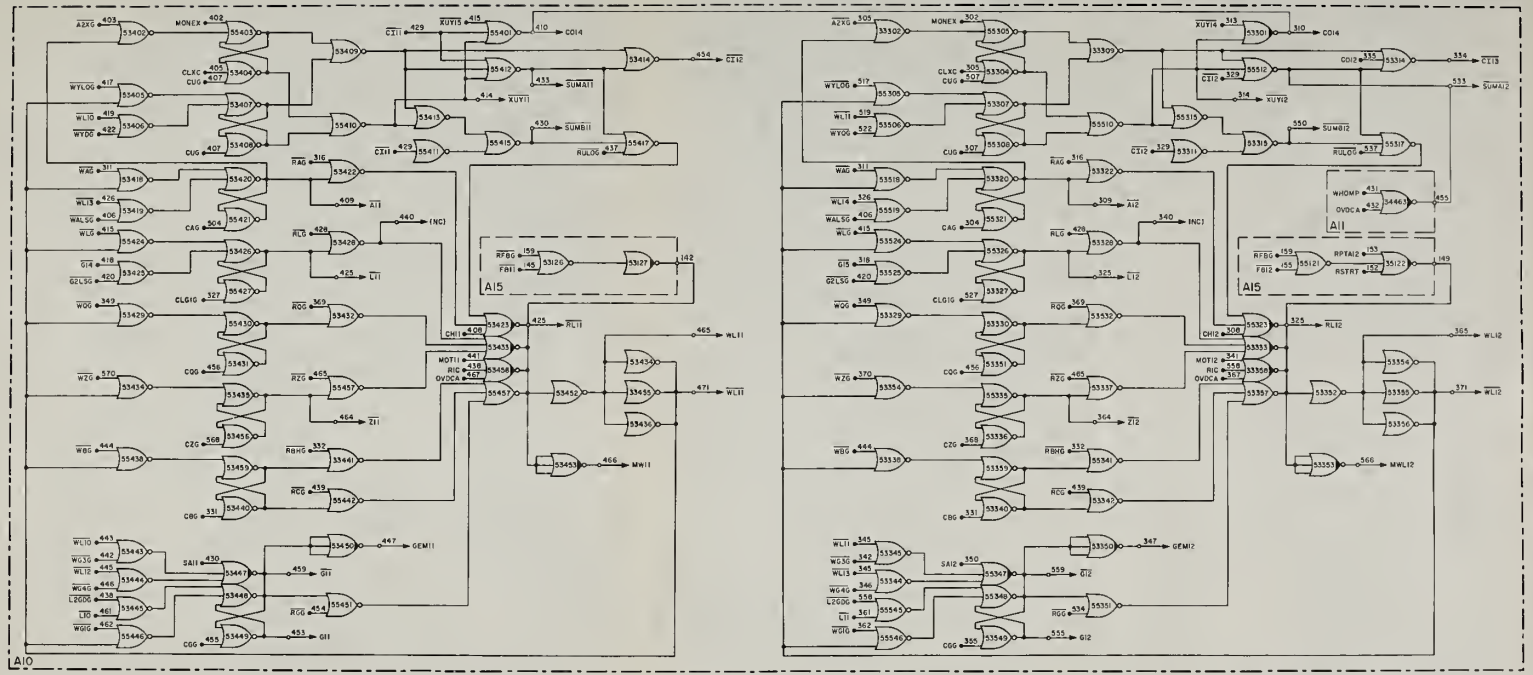


Figure 4-142. Flip-Flop Registers, (Sheet 6 of 8)

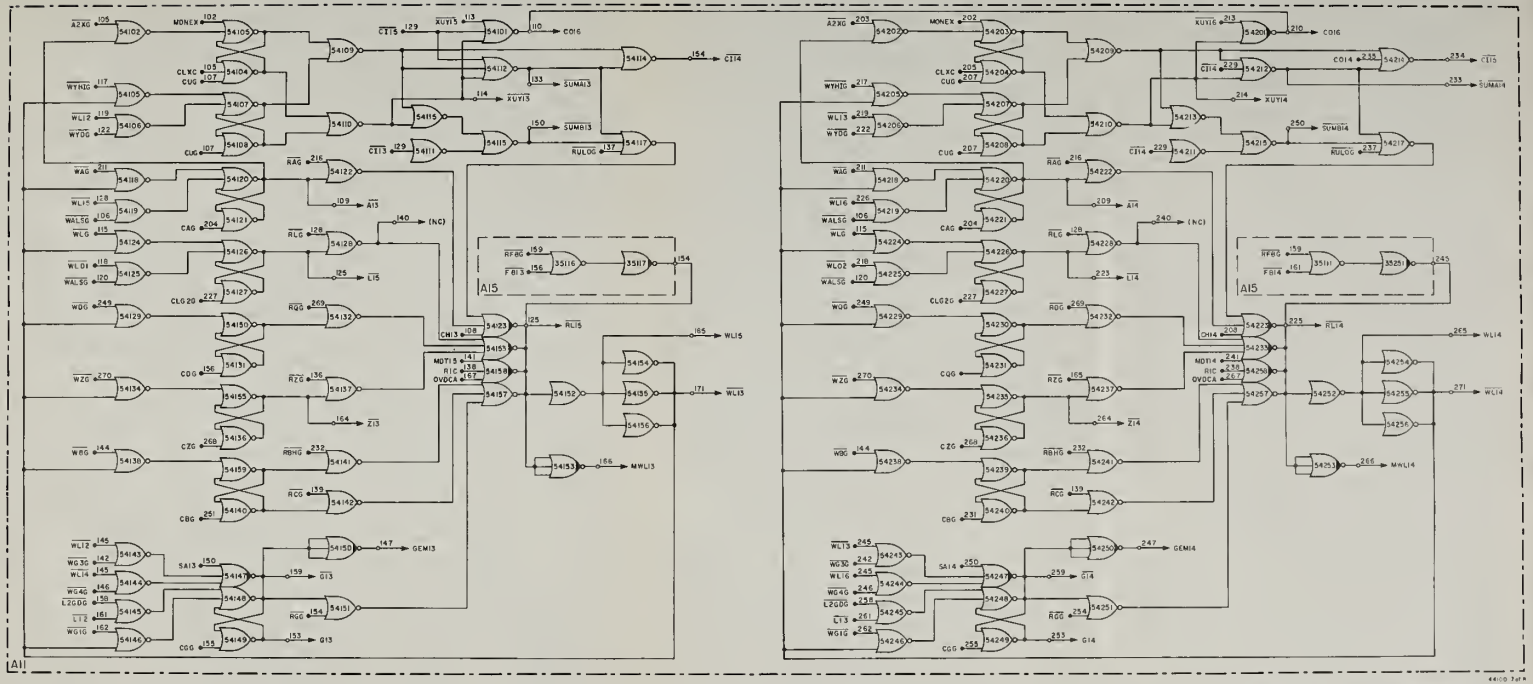


Figure 4-142. Flip-Flop Registers, (Sheet 7 of 8)

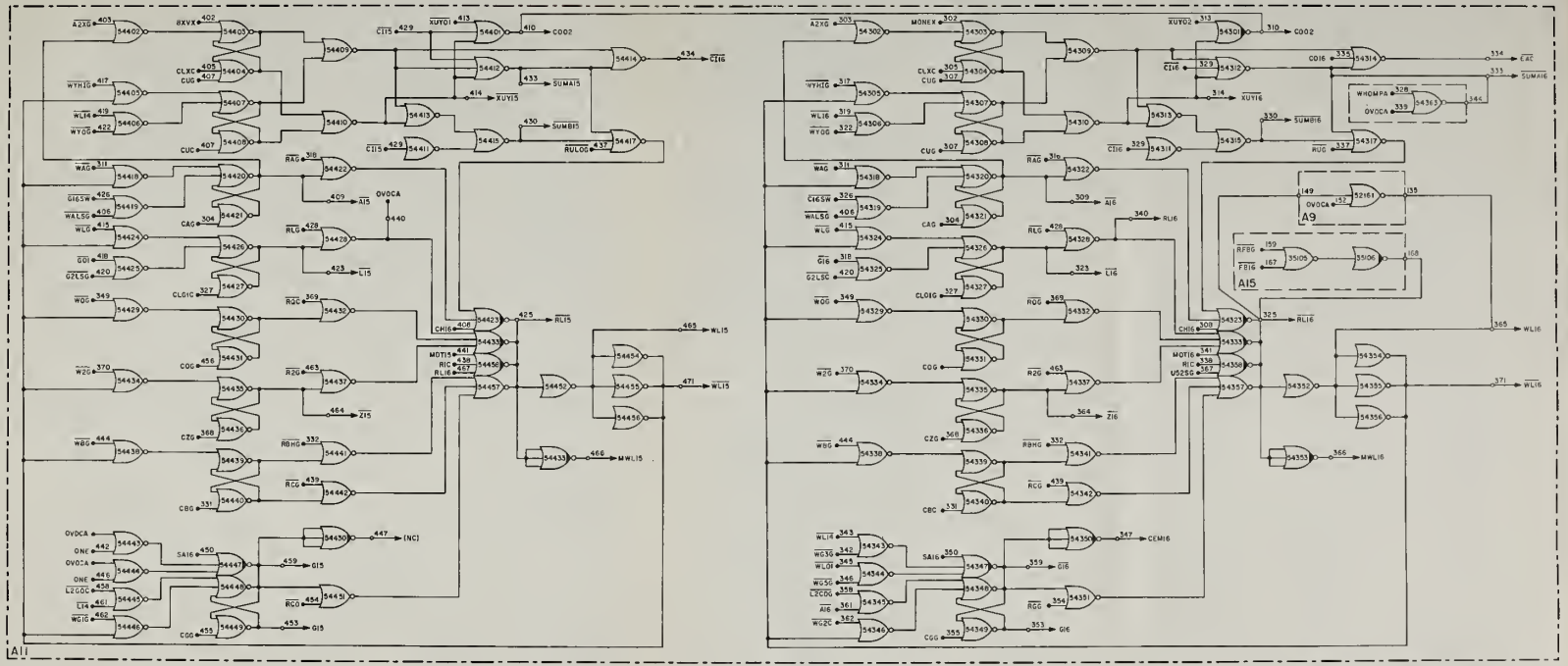


Figure 4-142. Flip-Flop Registers,
(Sheet 8 of 8)

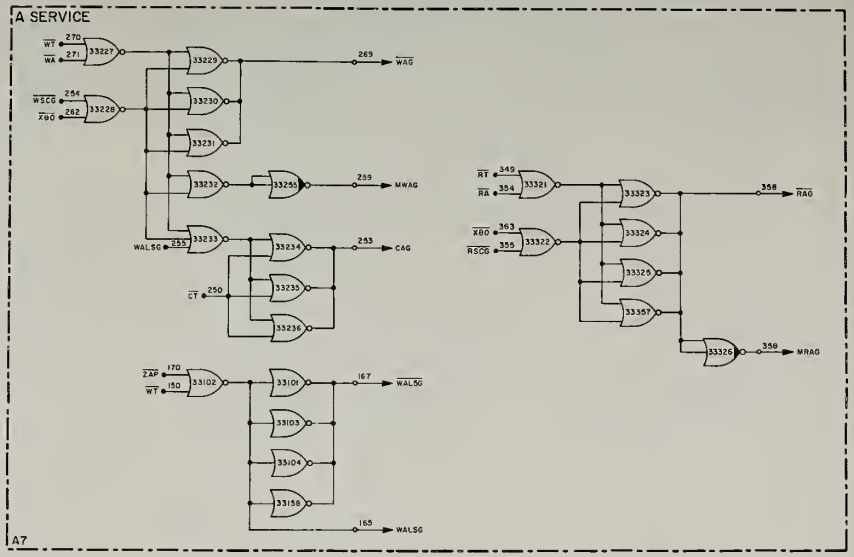


Figure 4-143. Register A Service

Table 4-LXXVI. Register A and L Write Line Inputs

A BIT															
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
G16	G16	WL16	WL15	WL14	WL13	WL12	WL11	WL10	WL09	WL08	WL07	WL06	WL05	WL04	WL03

L BIT															
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
G16	G01	WL02	WL01	G15	G14	G13	G12	G11	G10	G09	G08	G07	G06	G05	G04

The L service gates (figure 4-144) generate the necessary write, clear and read signals. Write signal $\overline{WLG}$ is generated as a function of three inputs:

(1) Control pulse $\overline{WL}$ from the sequence generator.

(2) Special and central address 0001.

(3) Channel address 01.

Write control pulse $\overline{WL}$ is generated during most of the instructions for which register L is used. These include instructions DV, DAS (add double precision), and subinstruction MP0. Register L, similar to register A, is addressable. Under program control, octal address 0001 (indicated by $\overline{XB1}$ to the service gates) coincident with the addressable registers write control signal $\overline{WSCG}$ causes write signal $\overline{WLG}$ to be generated. Register L is also accessible with IN/OUT channel address 01. A channel instruction generates write control pulse $\overline{WCHG}$. This control pulse coincident with channel address 01 generates write signal $\overline{WLG}$.

A fourth condition for writing into register L is provided by write signal $\overline{G2LSG}$. This signal is generated during subinstructions MP1 and MP3 and occurs coincident with write signal $\overline{WALSG}$ for register A (both are generated as a function of control pulse $\overline{ZAP}$). The bit content of L as a result of write signal $\overline{G2LSG}$ is listed in table 4-LXXVI. Signal $\overline{G2LSG}$ allows writing into bit positions 1 through 12 and 15 and 16; signal $\overline{WALSG}$ allows writing into bit positions 13 and 14.

The clear signal for register L is generated as a function of the write-in conditions described above and control pulse $\overline{CT}$.

4-5.5.6 Register Q. Register Q (see figure 4-142) is used during instructions TC (transfer control) and QXCH (exchange). During a TC instruction, the return address is stored in Q in the event that a transfer to the original sequence of instructions takes place. During QXCH instruction, the quantity in Q is exchanged with a quantity in E memory.

The manipulation of data in register Q is determined by the write and read signals generated by the Q service gates (figure 4-145). These signals are produced in a manner similar to that described for the other registers. Control pulse $\overline{WQ}$ from the sequence generator is produced during instructions TC and QXCH, and causes write signal $\overline{WQG}$ to be generated. The write signal is also generated as a function of memory address 0002 (indicated by $\overline{XB2}$ to the service gates) coincident with the addressable registers write control signal $\overline{WSCG}$. The Q register is also accessible with IN/OUT channel address 02. The channel instruction write signal $\overline{WCHG}$ coincident with channel address 02 ($\overline{XTO} \cdot \overline{XB2}$) causes write signal $\overline{WQG}$. Any one of the three write-in conditions described above causes the register clear pulse CQG to be generated. The read signal $\overline{RQG}$ is generated to read out the Q register as described for registers A and L.

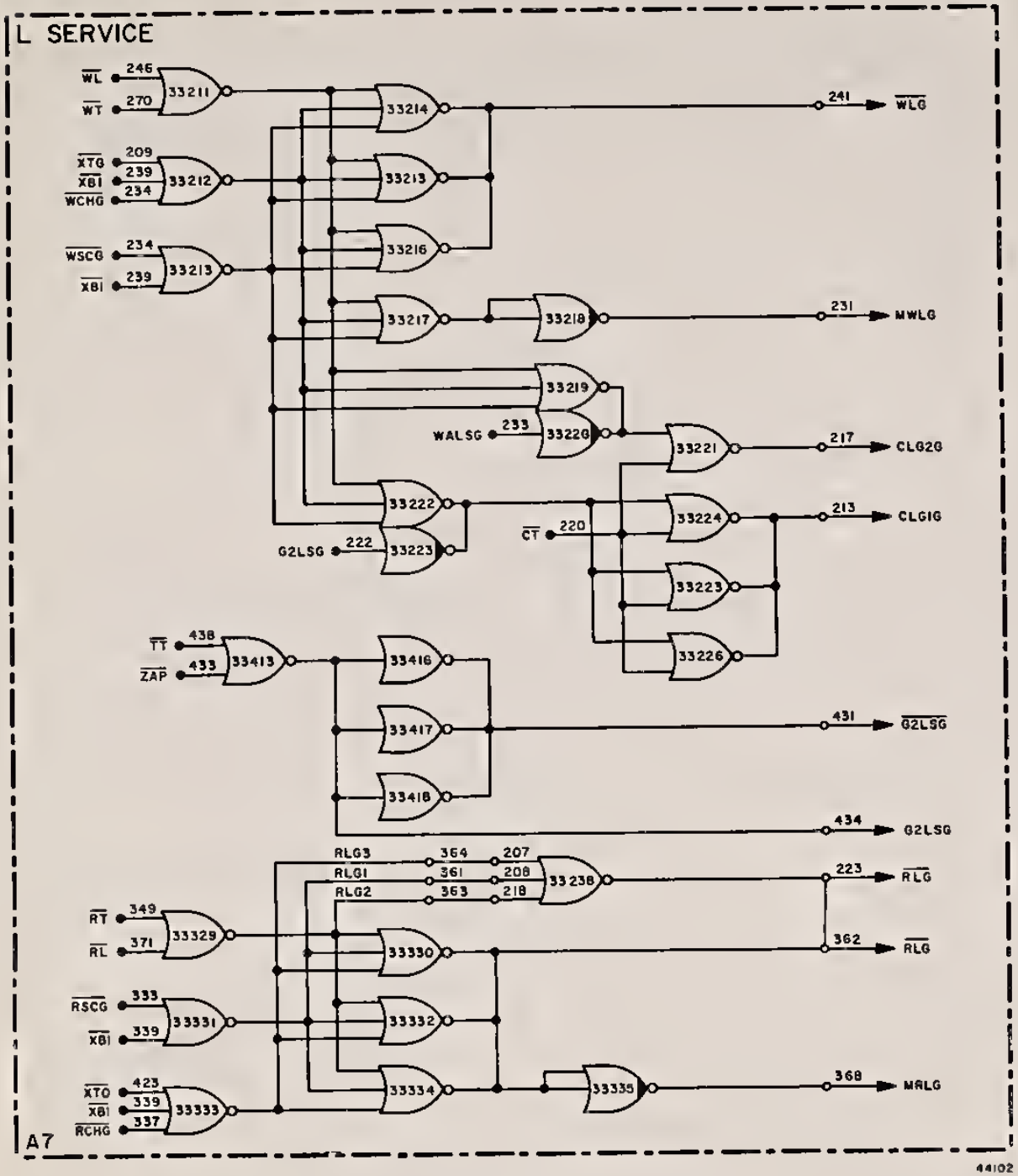


Figure 4-144. Register L Service

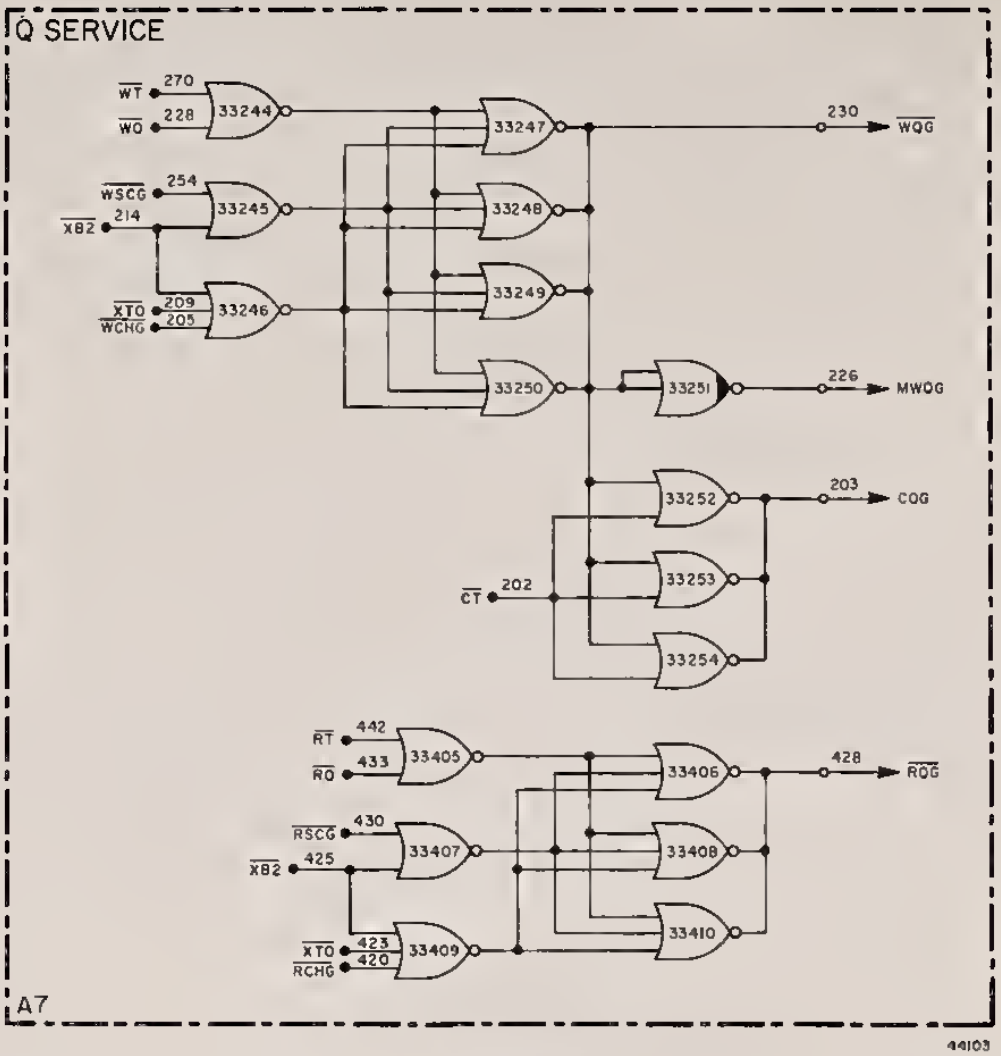


Figure 4-145. Register Q Service

4-5.5.7 Register Z. Register Z (see figure 4-142), also referred to as the program counter, stores the address of the instruction to be executed next. During the execution of an instruction, the content of register Z is incremented by one in the adder. The result (next address) is again stored in register Z. The write, clear, and read service (figure 4-146) generates the signals necessary to write into and read out of register Z. These are generated similar to those for registers A, Q, and L, with the exception that memory address 0005 ($\overline{XB5}$ to the service section) is used to write in and read out coincident with the addressable registers write and read control signals.

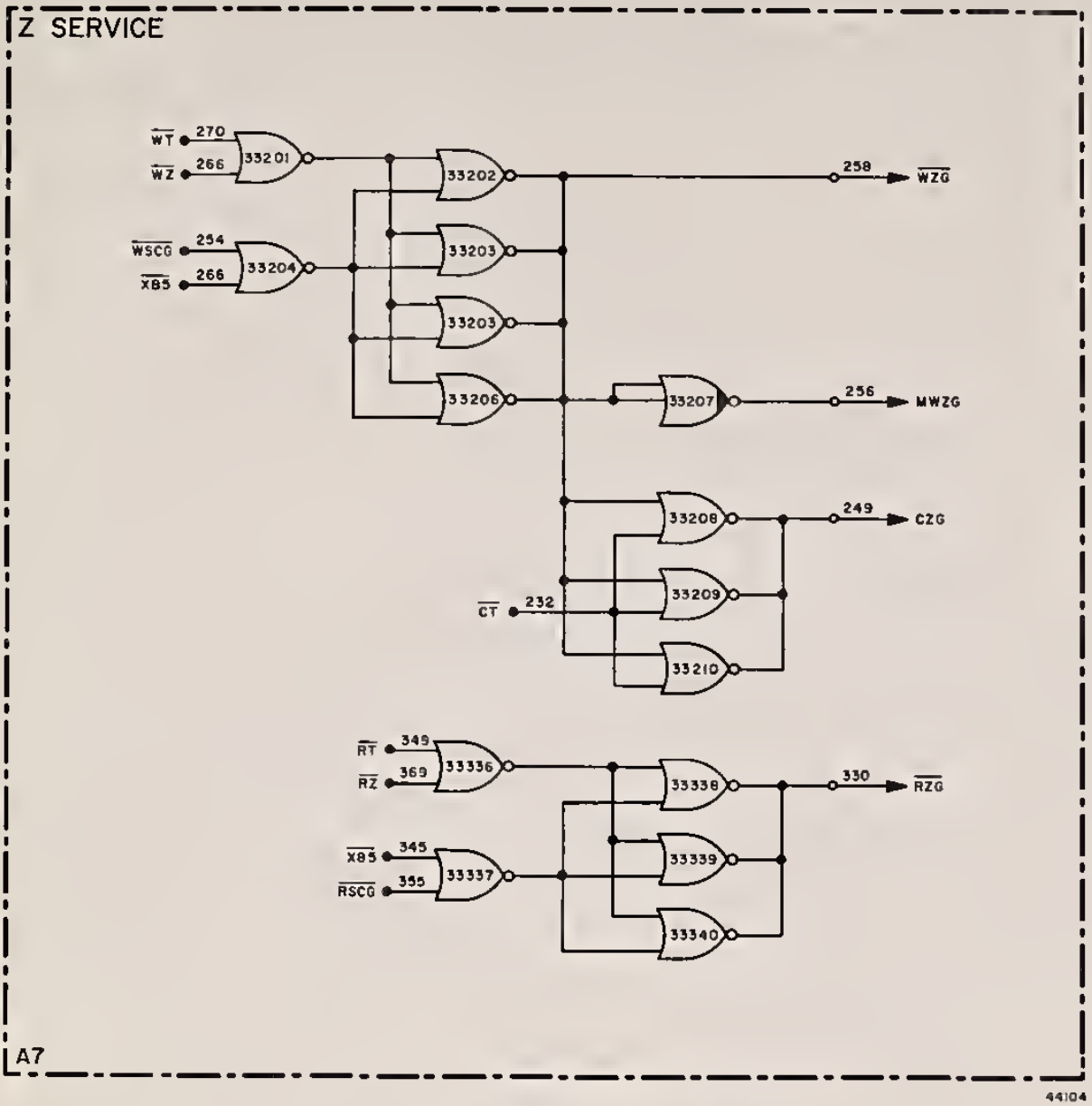


Figure 4-146. Register Z Service

Register Z write-in conditions for bit positions 15 and 16 also include the configuration illustrated in figure 4-147. During instruction DV1 (divide), a test for sign takes place (indicated by $\overline{BR1}$ to gate 39401). If the sign is negative, a ONE is inserted into bit position 16 of register Z at time 5 ($\overline{T05}$); at time 9, after a second test for sign, a ONE is inserted into bit position 15 of register Z if the sign is negative.

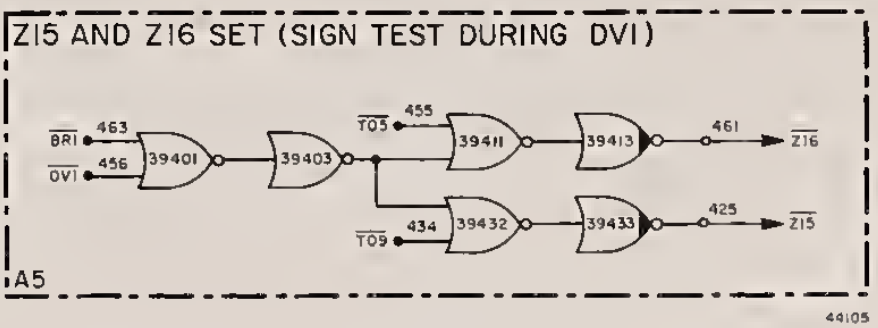


Figure 4-147. Z15 and Z16 Set (Sign Test During DV1)

4-5.5.8 Register B. Register B (see figure 4-142) is primarily a storage element. This register stores the order code and relevant address of the instruction to be executed next. This is not in conflict with register Z whicb stores the next address in the program.

The write, clear, and read signals for register B are generated by the service section (figure 4-148), in the same manner as described previously. This register is not addressable through program control. Readout of register B is accomplished normally by read control pulse $\overline{RB}$ from the sequence generator. This pulse causes read signals $\overline{RBHG}$ and $\overline{RBLG}$ to be generated. Signal $\overline{RBLG}$ reads out bit positions 1 through 10; signal $\overline{RBHG}$ reads out bit positions 11 through 16. Bit positions 1 through 10 only can be read out and placed on the write lines by $\overline{RBLG}$ which is generated as a function of signal RL10BB. This latter signal is generated during certain instructions to place the 10 low order bits of B on the write lines. Read signal $\overline{RCG}$ gates the complement of register B onto the write lines when required during certain instructions.

4-5.5.9 Register G. Register G (see figure 4-142) buffers all information coming from and going to erasable and fixed memory. This register also functions during certain instructions to shift or cycle information as required.

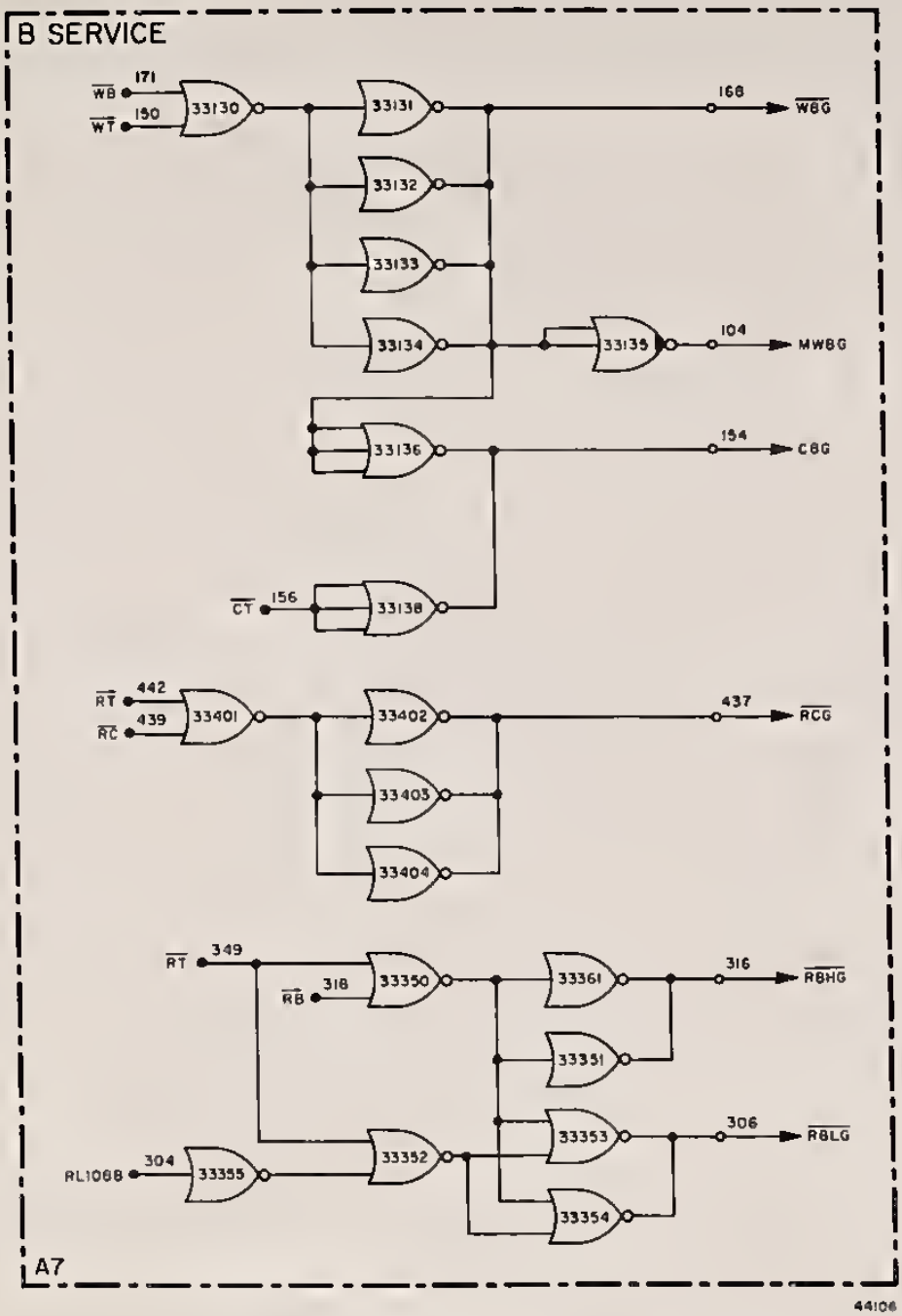


Figure 4-148. Register B Service

Data from fixed or erasable memory is written into register G from sense amplifier outputs SA01 through SA14 and SA16, which are wired directly into the corresponding bit positions of register G. Sense amplifier output SA16 which is the sign bit, is wired into both bit positions 15 and 16 of G. This results in the same bit value in these two bit positions when a quantity is entered into the central processor from memory as described previously under word formats.

There is no manipulation of the parity bit within the central processor. Consequently, register G never sees this bit during readout or write-in to memory. The parity logic controls all manipulations of the parity bit.

Write service for register G (figure 4-149), consists of six write signals, $\overline{WG1G}$ through $\overline{WG5G}$ and $\overline{WEDOPG}$. For all addresses except octal 0020 through 0023, write signals $\overline{WG1G}$ and $\overline{WG2G}$ are generated and information is gated from the write lines into register G. Write signal $\overline{WG1G}$ gates bit positions 1 through 15; write signal $\overline{WG2G}$ gates bit position 16. These two signals are produced by write control pulse $\overline{WG}$ from the sequence generator (which appears as $\overline{WGA}$ in G service) coincident with timing pulse $\overline{WT}$ into gate 33140 of figure 4-148. This results in WGNORM which causes write signals $\overline{WG1G}$ and $\overline{WG2G}$. Signal GINH from the editing control logic inhibits write signal $\overline{WG1G}$ during shift and cycle operations. Bit position 15 is not used during any shifting and cycling operations.

Octal addresses 0020 through 0023 are produced under program control to perform shift and cycle operations. The decoded signals representing these addresses are applied to the editing control logic (figure 4-150) which generates the signals necessary to manipulate data into register G. Signal OCTAD2 is inverted by gate 34343 and enables the input gates of editing control for octal addresses 0020 through 0027. The cycle and shift control signals are generated at time 2 ($\overline{T02}$) coincident with the particular address.

Address 0020 causes a word to be cycled right when entered into register G. The decoded signals representing this address ($\overline{OCTAD2} \cdot \overline{XB0}$) set the cycle right control flip-flop in editing control at time 2. The flip-flop output ($\overline{CYR}$) enables the write gates in the service section, and, coincident with write control pulse $\overline{WGA}$, causes write signals $\overline{WG4G}$ and $\overline{WG5G}$ to be produced. Data is cycled right as shown in figure 4-151. The programmer would consider this transformation as follows:

CYR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0020	01	15	14	13	12	11	10	09	08	07	06	05	04	03	02	G Register

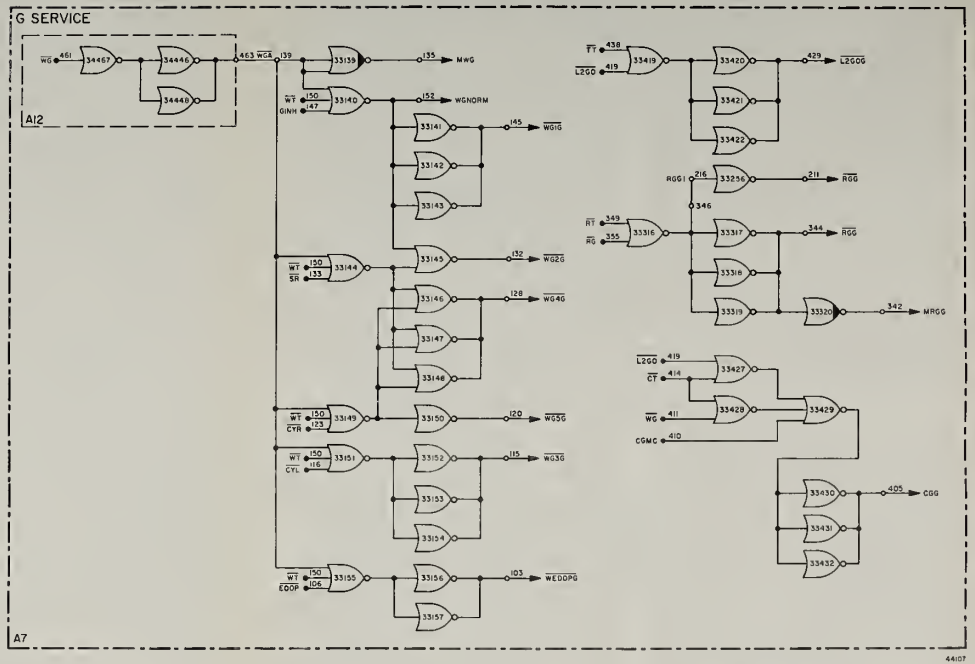


Figure 4-149. Register G Service

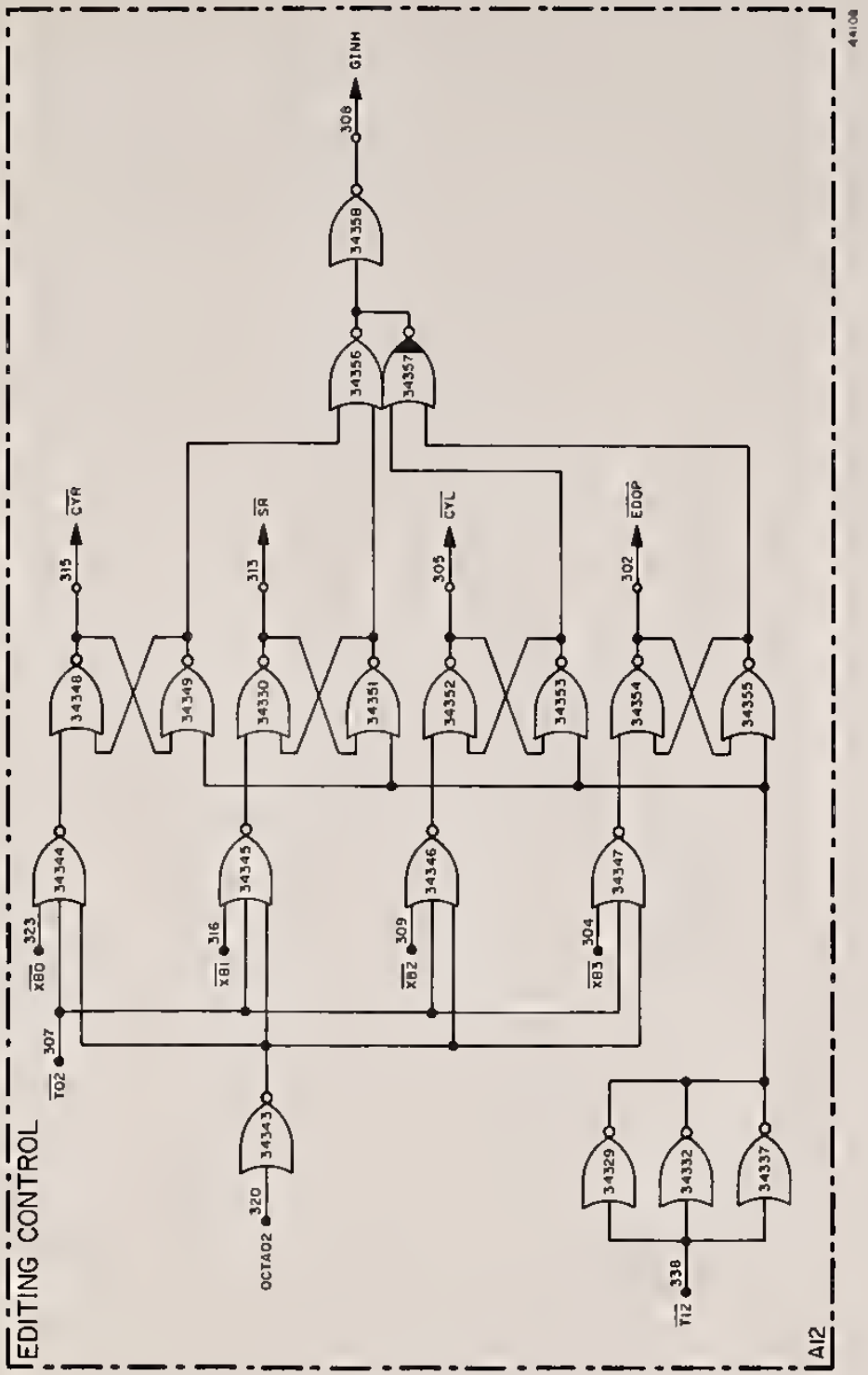


Figure 4-150. Editing Control

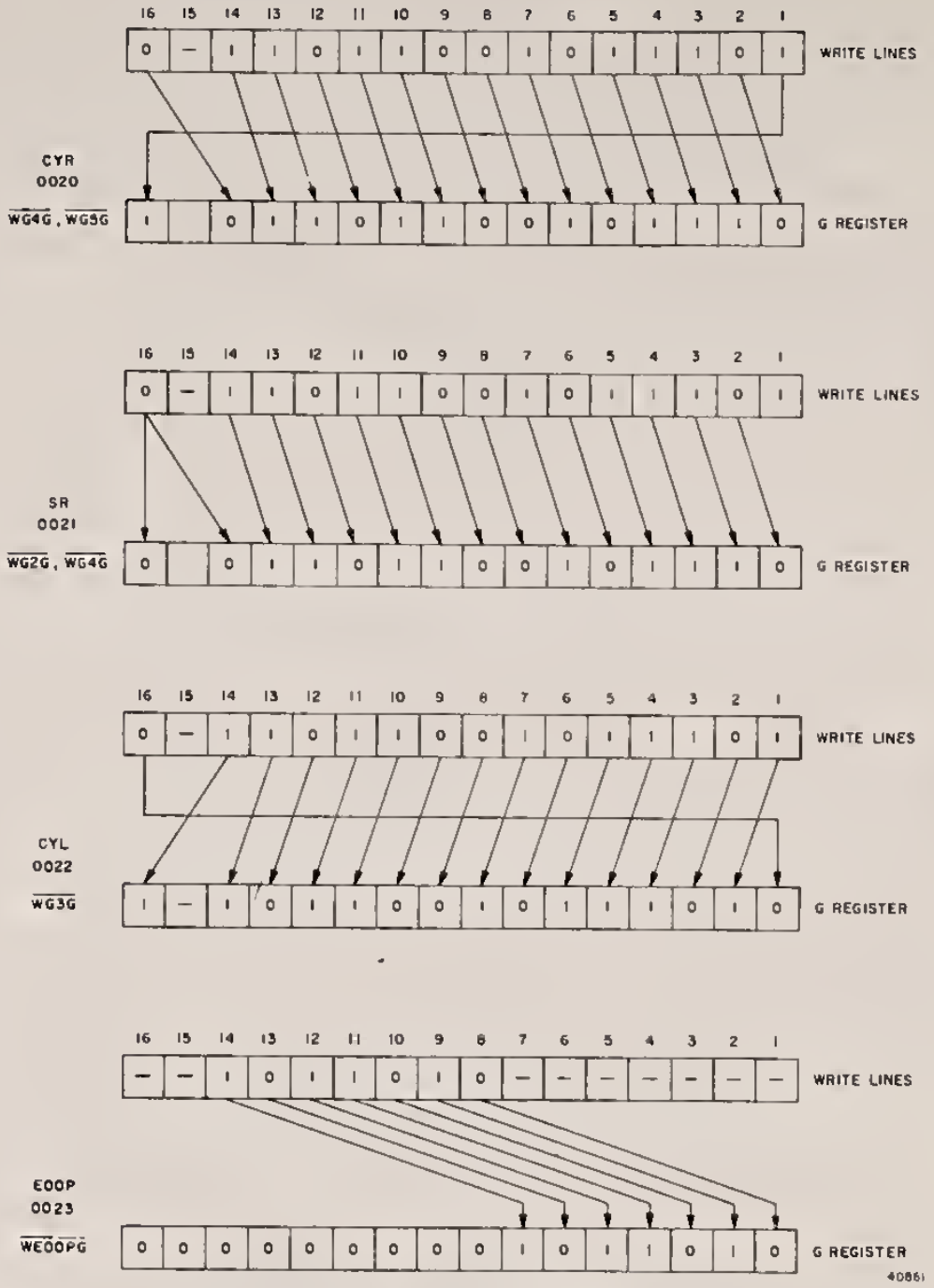


Figure 4-151. Editing Transformations

Address 0021 ($\overline{\text{OCTAD2}} \cdot \overline{\text{XB1}}$) sets the shift right control flip-flop. The flip-flop output ($\overline{\text{SR}}$) enables the write control pulse $\overline{\text{WGA}}$, and causes write signals $\overline{\text{WG2G}}$ and $\overline{\text{WG4G}}$ to be produced. Bit 16 from the write lines is entered into bit positions 16 and 14 of register G, and all other bits are shifted one position to the right. No action occurs with bit 1 from the write lines - this bit is effectively shifted off the end. The programmer would consider this transformation as follows:

SR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0021	15	15	14	13	12	11	10	09	08	07	06	05	04	03	02	G Register

Address 0022 ($\overline{\text{OCTAD2}} \cdot \overline{\text{XB2}}$) sets the cycle left control flip-flop. The flip-flop output ($\overline{\text{CYL}}$) enables the write gates, and, coincident with write control pulse $\overline{\text{WGA}}$, causes write signal $\overline{\text{WG3G}}$ to be produced for a cycle left operation. As sbown in figure 4-151, bit 16 from the write lines is written into bit position 1 of G, bit 2 is written into bit position 3, etc. The programmer would consider this transformation as follows:

CYL	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0022	14	13	12	11	10	09	08	07	06	05	04	03	02	01	15	G Register

The last editing transformation involves bits 8 through 14 from the write lines. Address 0023 sets the edit operation flip-flop ($\overline{\text{EDOP}}$) in the editing control logic. The flip-flop output enables the associated write gates in the service section, and causes write signal $\overline{\text{WEDOPG}}$ to be produced. This signal writes bits 8 through 14 from the write lines into bit positions 1 through 7 of register G as illustrated in figure 4-151. The programmer would consider this transformation as follows:

EDOP	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0023	--	--	--	--	--	--	--	--	14	13	12	11	10	09	08	G Register

During divide and multiply instructions, the G register is used in the manipulation of data in the central processor. Write-in is accomplished by write signal $\overline{\text{L2GDG}}$ which is generated only during these instructions. The signal is generated as a function of

write control pulse $\overline{\text{L2GD}}$ from the sequence generator, and timing pulse $\overline{\text{TT}}$ from the timer. Signal $\overline{\text{TT}}$ is identical to the write time signal $\overline{\text{WT}}$. The content of register G after write-in by $\overline{\text{L2GDG}}$ is as follows:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
MCRO	L01	L02	L03	L04	L05	L06	L07	L08	L09	L10	L11	L12	L13	L14	L16

Bit position 16 contains bit 16 from the accumulator, positions 15 through 2 contain L bits 14 through 1 respectively, and the data in bit position 1 is a function of control pulse $\overline{\text{MCRO}}$. This latter control pulse is generated in the sequence generator as a function of the content of register L during a multiply instruction and enters a ONE into bit position 1 of the G register. The clear signal for register G (CGG) is generated as a function of write signals $\overline{\text{WG}}$ and $\overline{\text{L2GD}}$ coincident with timing pulse $\overline{\text{CT}}$. Register G is also cleared by signal CGMC. This signal is generated as a function of the strobe signals for erasable and fixed memory. When the sense amplifiers are strobed (STBE or STBF), signal CGMC is generated and clears register G.

The read signal ($\overline{\text{RGG}}$) is generated as a function of read control pulse $\overline{\text{RG}}$ and timing signal $\overline{\text{RT}}$.

4-5.5.10 Arithmetic Unit (Registers X and Y). The arithmetic unit (see figure 4-142) is a 16 bit parallel adder with end-around carry and is the basic arithmetic unit of the computer. The adder processes two numbers at a time; one number is contained in register Y, and a quantity is entered into X by control pulse action dependent on the instruction being executed. The output gating complex senses for the carry and provides outputs from each bit position to the write lines.

Registers X and Y are functionally similar to the other flip-flop registers. However, the write service is more complex for register Y than for the other flip-flop registers. Register X has only one write signal ($\overline{\text{A2XG}}$), and this is constrained to register X being used in conjunction with register A during certain instructions.

Register Y is written into from the write lines; register X is not. The quantity entered into X is by control pulse action or by write signal $\overline{\text{A2XG}}$ as indicated above. The clear pulse (CUG) is generated as a function of the Y register write signals and clears both X and Y simultaneously.

The service gates for registers X and Y are illustrated in figure 4-152. Data from the write lines is written into the corresponding bit positions of register Y by write signals $\overline{WYLOG}$ and $\overline{WYHIG}$. Both of these signals are generated as a function of write control pulse $\overline{WY}$ and timing pulse $\overline{WT}$. Write signal $\overline{WYLOG}$ writes into bit positions 1 through 12; write signal $\overline{WYHIG}$ writes into bit positions 13 through 16. Signal $\overline{WYLOG}$ is also generated as a function of control pulse $\overline{WY12}$ from the sequence generator. This control pulse occurs during the execution of specific instructions to write into positions 1 through 12 of register Y. (Refer to the sequence generator which indicates the conditions for generating $\overline{WY12}$). In this case, positions 13 through 16 would not be written into and as a result of the clear pulse action would contain ZERO's.

Write signals $\overline{WYDG}$ and $\overline{WYDLOG}$ are generated during the multiply and divide instructions, and counter instructions SHINC and SHANC. There is some additional manipulation with bit position 1 of Y as a result of $\overline{WYDLOG}$. Write control pulse $\overline{WYD}$ is generated in the sequence generator and coincident with timing pulse $\overline{WT}$ generates write signals $\overline{WYDG}$ and $\overline{WYDLOG}$. The bit content of Y as a result of this write-in condition is as follows:

BIT	16	15	14	13	12	11	10	9
	$\overline{WL16}$	$\overline{WL14}$	$\overline{WL13}$	$\overline{WL12}$	$\overline{WL11}$	$\overline{WL10}$	$\overline{WL09}$	$\overline{WL08}$
BIT	8	7	6	5	4	3	2	1
	$\overline{WL07}$	$\overline{WL06}$	$\overline{WL05}$	$\overline{WL04}$	$\overline{WL03}$	$\overline{WL02}$	$\overline{WL01}$	$\overline{WL16}$

Bit 16 from the write lines is entered into positions 16 and 1 of Y; positions 15 through 2 contain write line inputs 14 through 1, respectively. Write-in to bit position 1 by $\overline{WYD}$ is inhibited by several functions. Interflow from the register A bit 1 is inhibited during a multiply instruction if bit 15 of register L contains a ONE. This condition is sensed by gate 33125 in the service section. Also, during multiply, end-around carry is inhibited. This condition is satisfied by signal NEAC (no end-around carry) to gate 33124. Lastly, during counter instruction SHINC (shift), write-in to bit position 1 is inhibited by counter command SHINC.

The write signal $\overline{A2XG}$ is generated to write into register X mostly during extra-code instructions (the one exception is basic instruction AD-add). This signal copies the content of register A into the corresponding bit positions of register X. This is illustrated in figure 4-142. The flip-flop outputs of A are wired directly to the only write gate inputs to register X, and are gated by signal $\overline{A2XG}$.

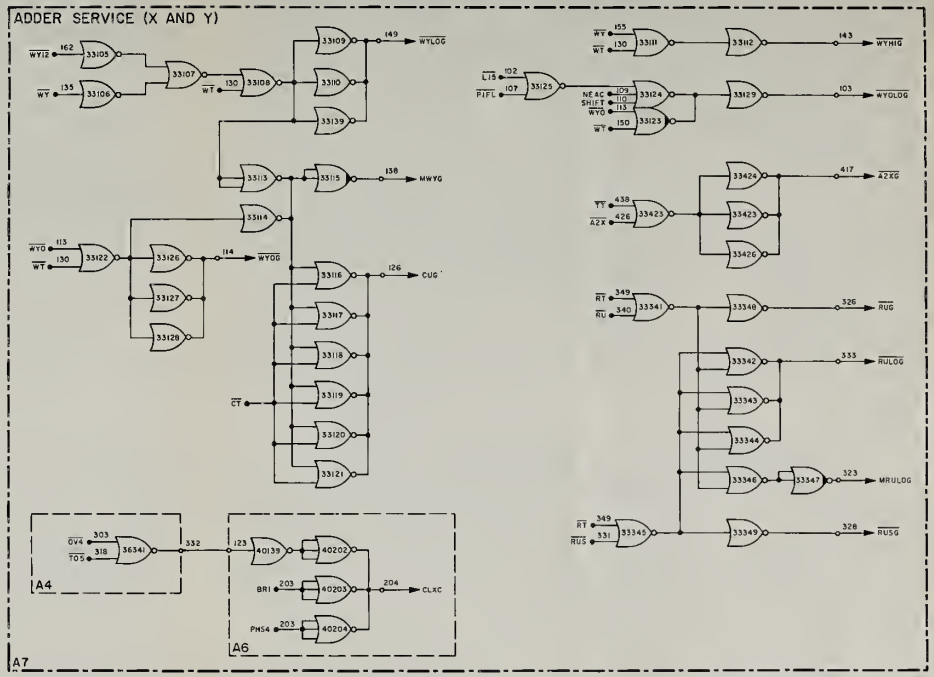


Figure 4-152. Adder Service (Registers X and Y)

Since the arithmetic unit processes two numbers, one number is obviously entered into Y from the write lines. Another quantity, dependent on the instruction being executed, is entered into register X. This is accomplished by control pulses PONEX, MONEX, TWOX, and BXVX. These control pulses enter the quantities +1, -1, +2 and 40000 (octal) respectively. The quantity +0 is effectively entered into X by clear signal CLXC. This signal occurs during a divide instruction as a result of a branching condition and subsequently clears register X.

Two read signals are generated to read out the adder. Signal $\overline{\text{RULOG}}$ reads out positions 1 through 15; signal $\overline{\text{RUG}}$ reads out position 16 only. The two signals are generated simultaneously as a function of read control pulse $\overline{\text{RU}}$ coincident with timing signal $\overline{\text{RT}}$. Only bit positions 1 through 15 are read out by read signal $\overline{\text{RULOG}}$ which is generated as a function of control pulse $\overline{\text{RUS}}$. This control pulse is generated during extracode instruction MSU (modular subtract) and counter instructions PCDU, MCDU and SHIFT. Output signals $\overline{\text{SUMA01}}$ through $\overline{\text{SUMA16}}$ and $\overline{\text{SUMB01}}$ through $\overline{\text{SUMB16}}$ do not require a read signal. They are direct inputs to the erasable and fixed bank registers.

The carry gate output from each bit position ($\overline{\text{CI02}}$-$\overline{\text{CI15}}$) is applied to the next high order bit position ($\overline{\text{CI02}}$ from bit position 1 to bit position 2, etc). The end-around carry from bit position 16 ($\overline{\text{EAC}}$) is applied to bit position 1 through the carry logic (figure 4-153). End-around carry is inhibited during a multiply instruction. At time 10

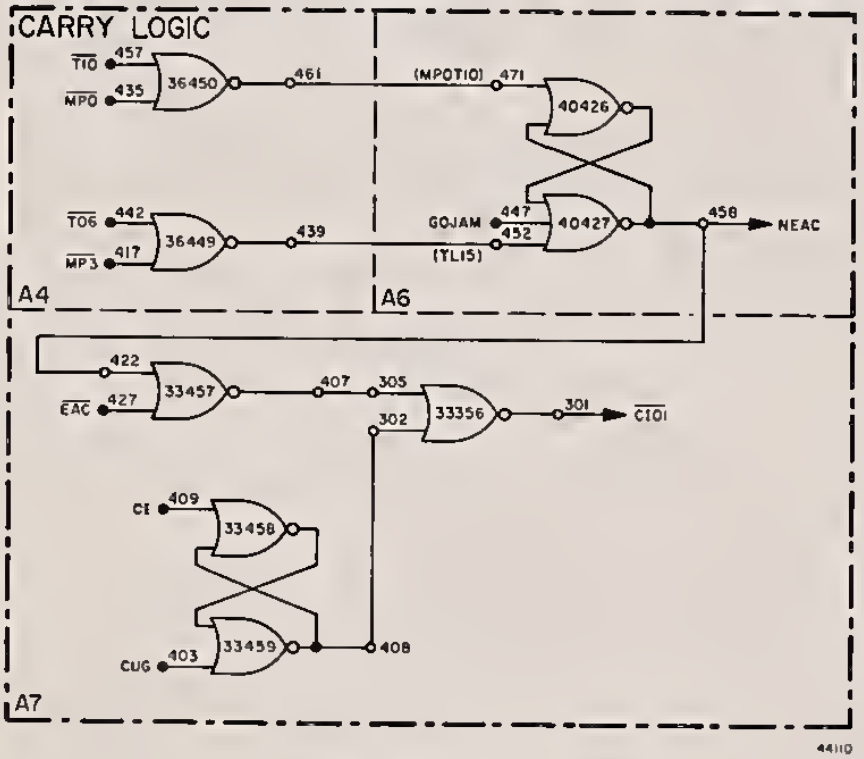


Figure 4-153. Carry Logic

of subinstruction MP0, FF40426-40427 is set and signal NEAC (no end-around carry) inhibits the carry-in gate. The gate is again enabled at time 6 of subinstruction MP3 which occurs at the end of the multiply instruction. A logic ONE is forced into bit position 1 during certain instructions by the carry-in flip-flop (FF33458-33459). Control pulse C1 from the sequence generator sets this flip-flop, the output of which is applied as an enabling level to the carry-in gate of bit position 1. Clear signal CUG resets the flip-flop.

The carry-propagate and carry-skip chains (figure 4-153A) control the carry gate outputs $\overline{C102}$ through $\overline{C116}$ and the end-around-carry signal, EAC. The carry-propagate chain comprises 16 series sections; each section controls the carry-in function to the next bit position in line. Bit position 16 controls $\overline{EAC}$ and, consequently, the carry-in function to bit position 1. Without the carry-skip chain, a carry could be propagated in series through all bit sections with a corresponding excessive propagation delay. The carry-skip chain prevents this excessive delay by sampling sets of four bit-sections and the carry-in to the first bit of each set. If a carry would be passed through all four bits of a monitored set by the carry-propagate chain, then the carry-skip circuit passes the carry-in to the fifth bit-section in line. The seven carry-skip-chain circuits monitor bits 1 through 4, 3 through 6, 5 through 8, 7 through 10, 9 through 12, 11 through 14, and 13 through 16. The worst case-propagation time through the skip chain requires 3 skip detections and 4 carry propagations.

Generation of carry-in signal $\overline{C102}$ produced by gate 51114 is typical of all carry-in signals except $\overline{C101}$. Gate 51114 produces $\overline{C102}$ (representing a carry-in to bit position 2) when a ONE is contained in bit position 1 of registers X and Y (gate 51109) is enabled) or when gate 51112 is enabled. Gate 51112 senses three conditions to perform an exclusive OR function; either or both bit positions are cleared (either the X bit or the Y bit is a ZERO), $\overline{C101}$ is present (there is a carry-in), and $\overline{XUY01}$ is present (one or both bit positions are filled). Signal $\overline{C102}$, applied to the next propagate section in the chain, controls generation of $\overline{C103}$.

Generation of carry-skip signal C004 (1, 2, 3, and 4 skip-gates 53462, 51101, and 51201) is typical of the seven skip signals. Signals WHOMP and WHOMPA may or may not inhibit the skip signals (in this case through gate 53462). Signals WHOMP and WHOMPA are assumed not present. Gates 51101 and 51201 produce C004 when signals $\overline{XUY01}$ through $\overline{XUY04}$ and $\overline{C101}$ are present. The $\overline{XUY}$ signals indicate that a corresponding bit position contains a ONE. Therefore, to produce C004 there must be bits present in positions 1 through 4 (X or Y) and a carry-in for bit position 1. With these conditions, C004 generates the carry-in signal $\overline{C105}$ directly for bit position 5 through gate 51314. Signal $\overline{C105}$ conditions gate 52101 which controls the next skip signal in line, C008. The skip chain produces signals C004, $\overline{C105}$, C008, $\overline{C109}$, C012, $\overline{C113}$, and finally C016 in sequence if a carry is propagated through the adder. This carry path generates EAC before either the propagate chain or the other skip circuits. All the skip circuits and the entire propagate chain will be enabled when a carry is propagated through the entire adder.

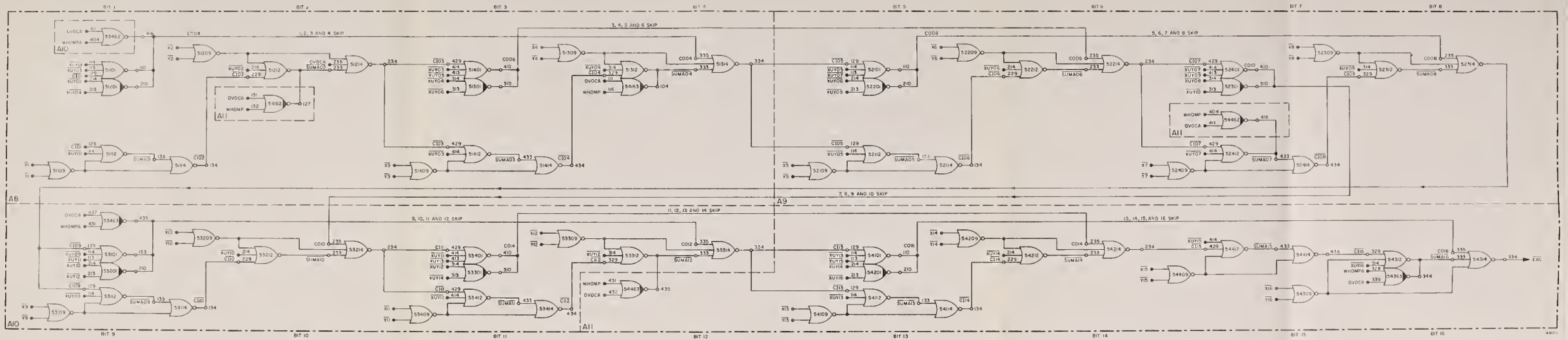


Figure 4-153A. Adder Carry-Propagate and Carry-Skip Chains

The carry-propagate and carry-skip chains speed-up computations in the adder. Also, removal of the carry must be accomplished in as short a time as possible; signals WHOMP and WHOMPA accomplish this latter condition. During the divide instruction, signal CLXC clears the X register. The desired sum readout during the next microsecond is the content of tbe Y register without any X register content or any carry detected. Signal $\overline{\text{EAC}}$, indicating a carry into bit position 1, remains when eitber the carry-propagate or carry-skip chain remains enabled at bit position 16. Due to propagation delay through the chains, EAC would not be removed by the chains in time. Signal CLXC initiates signals WHOMP and WHOMPA. They inhibit enough carry-propagate and skip gates in the chains to remove all carry signals, including $\overline{\text{EAC}}$, in time for the proper sum to be readout. Divide instruction control pulse DVXP1 or control pulse NISQ removes WHOMP and WHOMPA before another carry operation is required.

An example of the inhibiting operation is as follows: Gate 54314 requires enabling logic ZERO levels on all three legs to remove $\overline{\text{EAC}}$. The output of gate 54309 applied to gate 54314 is a logic ZERO level because X16 inhibits gate 54309 (CLXC cleared the X register). Signal WHOMP inhibits gate 54363 which enables a second leg of gate 54314. Gate 53314 (signal $\overline{\text{C113}}$) is enabled and inhibits gates 54101 and 54201 which supply enabling voltage to the remaining leg of 54314. Signal WHOMP controls two enabling inputs of gate 53314; gate 53309, inhibited by signal $\overline{\text{X12}}$, enables the remaining output.

The quantities entered into the arithmetic unit during normal computations contain the sign in both positions 15 and 16. If overflow or underflow occurs, bit position 15 will contain a value bit which is opposite to the correct sign bit. A ONE in bit position 15 indicates overflow when both operands are positive; a ZERO in bit position 15 indicates underflow when both operands are negative. The correct sign of the sum is always contained in bit position 16.

4-5.5.10A Erasable and Fixed Bank Registers Service. Service for tbe two bank registers is illustrated in figure 4-153B. Read, write, and clear signals are generated to accomplish the data flow as illustrated in figures 4-138A and 4-138B. Either bank register or both registers can be addressed simultaneously. The individual signals such as $\overline{\text{REBG}}$, $\overline{\text{WEBG}}$, and CEBG for the erasable bank register, and $\overline{\text{RFBG}}$, $\overline{\text{WFBG}}$, and CFBG for the fixed bank register, are generated similar to the signals produced for the flip-flop registers. In addition, signal U2BBK (register U to botb banks) and signal RBBK (read both banks) operate the service to clear both banks, to write information directly from the adder, and to read that content into the memory address circuits. Address signals $\overline{\text{XB3}}$ (address 0003) and $\overline{\text{XB4}}$ (address 0004) initiate service signals for the erasable bank register (0003) or the fixed bank register (0004), respectively. Signal $\overline{\text{WSCG}}$ and address 0006 (signal $\overline{\text{XB6}}$) enable gate 33312 which causes clear and write signals to be produced for both banks simultaneously. Signals $\overline{\text{RSCG}}$ and $\overline{\text{XB6}}$ at gate 33413 produce simultaneous read signals.

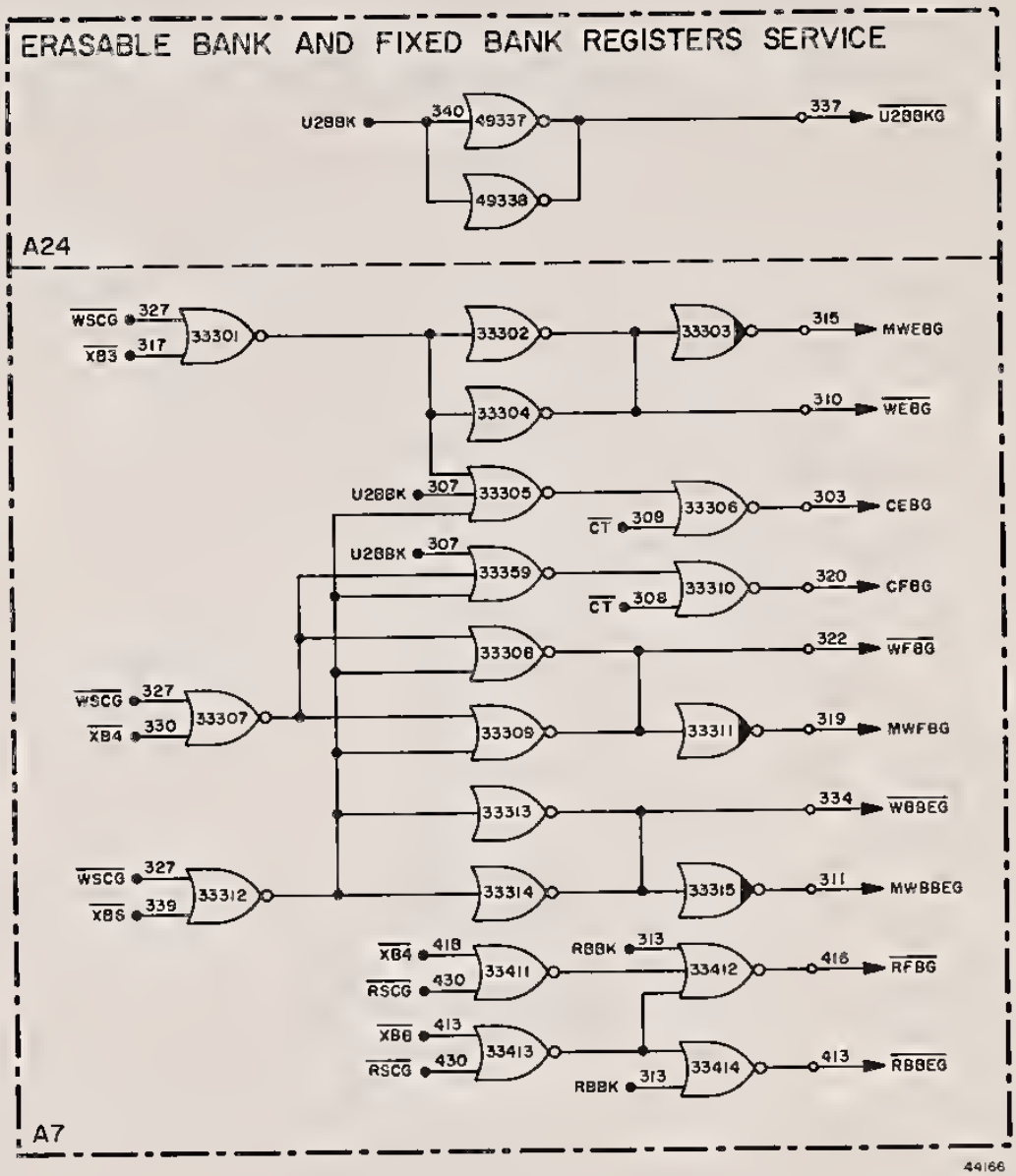


Figure 4-153B. Erasable and Fixed Bank Registers Services

4-5.5.10B Erasable Bank Register. The erasable bank register (figure 4-153C) receives bit inputs from the adder (SUM A - direct or SUM B - complement); write lines 1, 2, and 3 if both banks are being written into; or write lines 9, 10, and 11 if the erasable bank register alone is being written into. The content of this register is detected as outputs EB9, EB10, and EB11 and their complements. Two read signals are used to transfer the register content to the write amplifiers, $\overline{\text{REBG}}$ and $\overline{\text{RBBEG}}$. Signal $\overline{\text{REBG}}$ transfers the content to write amplifiers 9, 10, and 11. Bit 11 is placed on the write lines through gate 35127 in the fixed bank register. Since bit 11 is time shared by both the erasable and fixed bank register, this read sequence is used when only the erasable bank register is read. When both are read, signals BBK1, BBK2, and BBK3 are coupled to write amplifiers 1, 2, and 3. Output signals EB9 through EB11 and complements are applied to the address decoder to be used with the S register content.

4-5.5.10C Fixed Bank Register. The fixed bank register (figure 4-153C) receives bit inputs from the adder (SUM A - direct or SUM B - complement) and from write lines 11, 12, 13, 14, and 16. The output of this register is detected as outputs FB11, FB12, FB13, FB14, and FB16 and their complements. Only one read signal, RFBG, is used to readout the content of this register. It is produced when either the fixed bank register or both the fixed bank register and the erasable bank register are being read out. Signals RL11, RL12, RL13, RL14, and RL16 are applied to respective write amplifiers, and signal BK16 enters write amplifier 15. The fixed bank register outputs are applied to the fixed address generator where, in conjunction with the fixed bank extendible register and the address decoder outputs, a fixed memory location is selected.

4-5.5.10D Fixed Bank Extendible Register. The fixed bank extendible register (figure 4-153C) is serviced (write-in or readout) as an input channel (0007) using bits 5, 6, and 7. Its outputs (E5, E6, and $\overline{\text{E7}}$) are coupled to the fixed address generator to be used in conjunction with the fixed bank register outputs and register S outputs $\overline{\text{S11}}$ and $\overline{\text{S12}}$. The fixed address generator outputs in conjunction with the address decoder outputs specify a fixed memory address.

4-5.5.11 Write Amplifiers. The write amplifiers consist of an extended NOR input configuration, the output of which is applied through an output driver. One write amplifier configuration is associated with each bit position of the flip-flop registers as shown in figure 4-142. Outputs WL01 through WL16 and their complements are available and are designated as the write lines. The write amplifiers function logically as an OR gate. If any one input is a logic ONE, output WL-- is a logic ONE, and the complement output $\overline{\text{WL--}}$ is a logic ZERO. The latter output is used extensively as an enabling level to transfer information from one register to another, and for other gating functions throughout the computer.

The majority of inputs to the write amplifiers are from the flip-flop registers. The output from each bit position of the registers is wired directly to an associated write amplifier input. The 16 bit output of any one register involves the 16 write amplifiers contained in logic modules A8 through A11.

The inputs to the write amplifiers, excluding the flip-flop register inputs, are indicated in table 4-LXXVII and are described in the following paragraphs.

Inputs CAD1 through CAD6, from the counter address generator in priority control, determine the address of the counter in erasable memory which is to be updated. Since these inputs are applied to the six low-order bit positions, counters at locations up to 0077 could be addressed. However, the arrangement of counters in erasable memory at present involves addresses 0024 through 0060. A specific counter address is determined by the correct combination of inputs CAD1 through CAD6. This is illustrated as follows for the address of the time 6 (T6) counter - address 0031. For this address, inputs CAD5, CAD4, and CAD1 are logic ONE's; the remaining inputs are logic ZERO's. Inputs to write amplifiers 7 through 15 are not enabled; therefore, the full address is 00031 (octal).

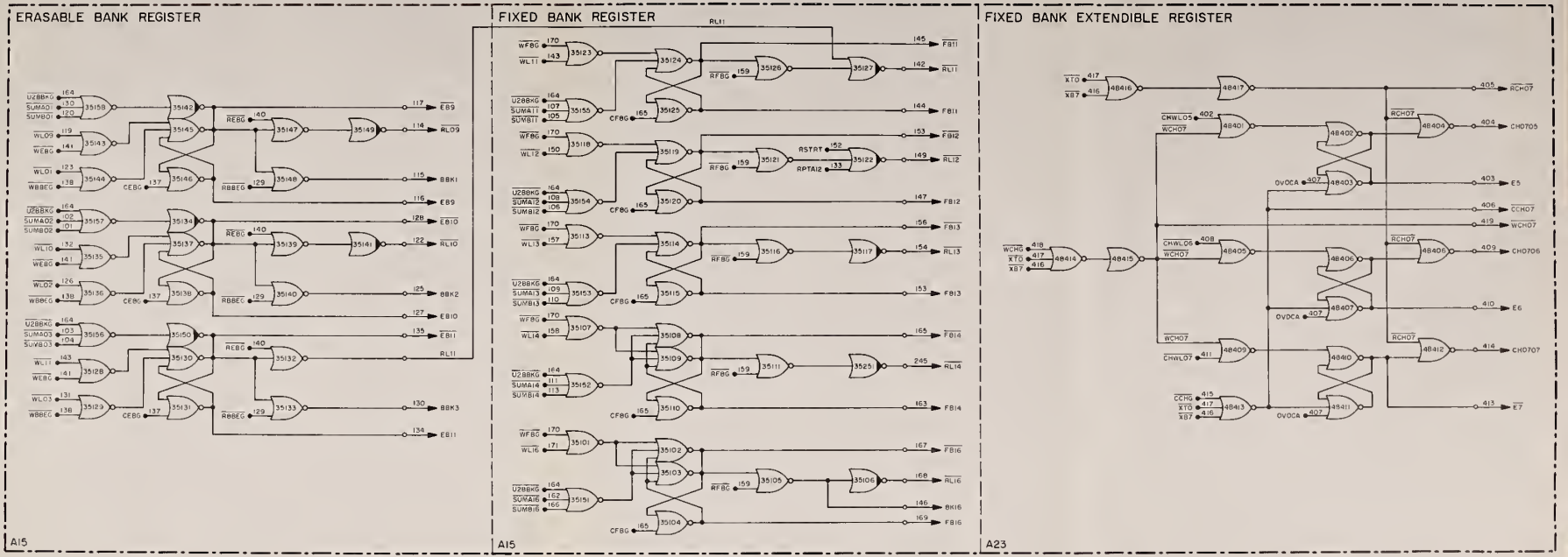


Figure 4-153C. Erasable Bank, Fixed Bank, and Fixed Bank Extendible Registers

Table 4-LXXVII. Write Amplifiers External Inputs

WL16	WL15	WL14	WL13	WL12	WL11	WL10	WL09	WL08	WL07	WL06	WL05	WL04	WL03	WL02	WL01
----	----	----	----	----	----	----	----	----	----	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1
----	----	----	----	RPTAD12	----	----	----	----	----	RPTAD6	RPTAD5	RPTAD4	RPTAD3	----	----
----	----	----	----	----	----	----	----	----	----	----	----	----	BBK3	BBK2	BBK1
----	----	----	----	----	----	EB10	EB09	----	----	----	----	----	----	----	----
FB16	----	FB14	FB13	FB12	FB11	----	----	----	----	----	----	----	----	----	----
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	RB1F
----	----	----	----	----	----	----	----	----	----	----	----	----	R6	R6	----
----	----	----	----	----	----	----	----	----	----	----	----	R15	R15	----	R15
R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	----
----	----	----	----	----	----	----	----	----	----	----	----	----	----	RB2	RB1
----	----	----	----	RSTRT	----	----	----	----	----	----	----	----	----	----	----
----	RL16	----	----	----	----	----	----	----	----	----	----	----	----	----	----
CH16	CH16	CH14	CH13	CH12	CH11	CH10	CH09	CH08	CH07	CH06	CH05	CH04	CH03	CH02	CH01
MDT16	MDT15	MDT14	MDT13	MDT12	MDT11	MDT10	MDT09	MDT08	MDT07	MDT06	MDT05	MDT04	MDT03	MDT02	MDT01

WRITE LINE	15 14 13	12 11 10	9 8 7	6 5 4	3 2 1
	0 0 0	0 0 0	0 0 0	0 1 1	0 0 1
	0	0	0	3	1

Inputs RPTAD3, 4, 5, 6, and RPTAD12 are placed on the write lines from the interrupt address generator in priority control. These inputs are used to determine one of addresses 4004, 4010, 4014, 4020, 4024, 4030, 4034, 4040, 4044, 4050, which are respectively the locations in fixed memory for the first instruction of the T6RUPT, T5RUPT, T3RUPT, T4RUPT, KYRPT1, KYRPT2, UPRUPT, DLKPPT, RADRPT, and HNDPPT transfer routines. These locations are addressed as indicated below when interrupt priority control receives interrupt requests.

RPTAD12	RPTAD6	RPTAD5	RPTAD4	RPTAD3	ADDRESS	ROUTINE
1	0	0	0	1	4004	T6RUPT
1	0	0	1	0	4010	T5RUPT
1	0	0	1	1	4014	T3RUPT
1	0	1	0	0	4020	T4RUPT
1	0	1	0	1	4024	KYRPT1
1	0	1	1	0	4030	KYRPT2
1	0	1	1	1	4034	UPRUPT
1	1	0	0	0	4040	DLKRPT
1	1	0	0	1	4044	RADRPT
1	1	0	1	0	4050	HNDRPT

Inputs BBK1 through BBK3 appear on the write lines in conjunction with the contents of the erasable bank (EB) and the fixed bank (FB) registers, when both of these registers are read out simultaneously. The content of either of these registers can also be individually placed on the write lines and appear as EB9, EB10 or FB11 through FB16 respectively.

Control pulse R6 is generated as a function of peripheral instruction FETCH, and causes address 00006 to be generated to address EB and FB registers.

Octal address 00015 is placed on the write lines by control pulse R15 which is generated during instructions RUPT and RSM. During an interrupt program (RUPT), the address of the instruction to be executed next and which is stored in register Z, is transferred to location 00015 in erasable memory. When the interrupt program is completed, the resume instruction (RSM) generates control pulse R15 whicb in turn produces address 0015. The information entered into this location in memory during RUPT is returned to the central processor.

The quantity minus one is placed on the write lines by control pulse R1C, which is applied to write amplifiers 2 through 16. There is no connection to write amplifier 1. This action results in the quantity 1 111 111 111 111 110 (177776_8) when R1C is generated.

Control pulse RB1 is generated during certain subinstructions and causes the quantity plus one (000001_8) to be placed on the write lines. Similarly, the quantity plus two (000002_8) is placed on the write lines by control pulse RB2.

Control pulse RSTRT produces the start address when instruction GO is generated by signal GOJAM. The start address is in fixed memory at location 04000, which is determined by RSTRT as a ONE in bit 12.

Data from the IN/OUT channels is routed through the write amplifiers as inputs CH01 - CH14 and CH16.

A 16 bit word can be loaded into the computer from the CTS during tests through Inputs MDT01 through MDT16.

4-5.5.12 Register S. Register S, the memory address register, accepts the 12 bit relevant address contained in an address word. The address is written into register S (figure 4-154) from the write lines subject to write pulse $\overline{WSG}$ which is generated when control pulse $\overline{WS}$ and timing signal $\overline{WT}$ are coincident. No read signal is generated to read the address out of register S. The outputs (S01 through S12) and their complements are available directly from the output gates. Ten bit positions are used to select the first 1024 storage locations in erasable memory. All 12 bit positions are used in conjunction with three bit positions of register EBANK to select the remaining 1024 storage locations in erasable memory. In addition, all 12 bit positions of register S, 5 bit positions of register FBANK, and 3 bit positions of register FEXT enable access to all storage locations in fixed memory.

4-5.5.13 Address Decoder. A storage location in erasable memory is selected by means of an X-Y coordinate system. There are 64 X coordinates and 32 Y coordinates. The X coordinates are controlled by selection signals XB0 through XB7 and XT0 through XT7. The Y coordinates are controlled by selection signals YB0 through YB3 and YT0 through

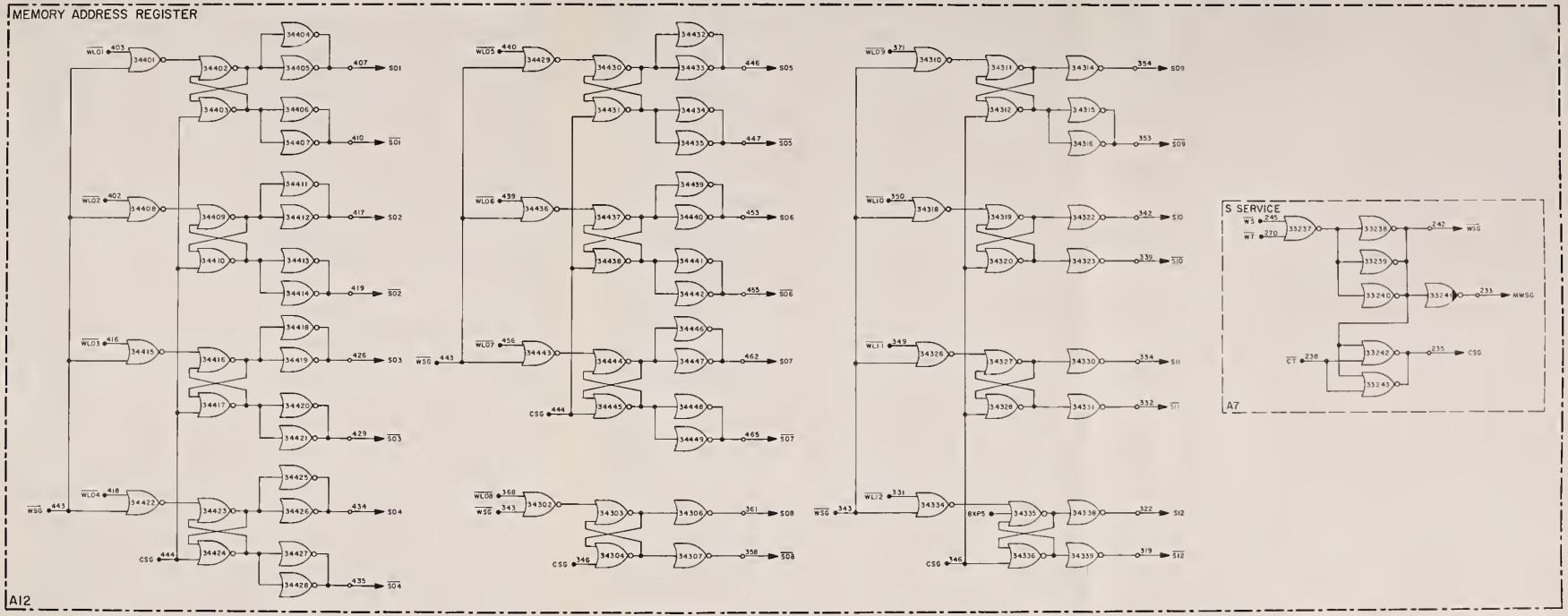


Figure 4-154. Memory Address Register (S)

YT3. Signals XB, XT, YB and YT are generated by the address decoder (figure 4-155) as a function of bits 1 through 12 from register S (S01 - S12). Bits 1 through 3 produce signals SB0 through SB7; bits 4 through 6 produce signals XT0 through XT7; bits 7 and 8 produce signals YB0 through YB3; and bits 9 and 10 in conjunction with bits EB9 through EB11 produce signals YT0 through YT7. (See table 4-LXXVIII.)

Combinations of selection signals XB, XT, YB and YT allow access to all locations in erasable memory. Signal XB, XT and YB in conjunction with signals YT0 through YT2 allow access to the first 1024 locations of erasable memory (unswitched erasable memory). Signals XB, XT, and YB in conjunction with signals YT3 through YT7 allow access to the remaining 1024 locations of erasable memory (switched erasable memory). Locations in unswitched erasable memory can also be addressed as locations of switched erasable memory if the proper bank number is entered into register EBANK. This is due to an overlap in the addressing scheme. However, addresses 0000 through 0377 (Bank 0) are normally addressed only by register S.

4-5.5.13A Fixed Address Generator. The fixed address generator (figure 4-155A) produces outputs F11 through F16 and complements which are applied to fixed memory. These signals, in conjunction with the address decoder outputs, specify fixed memory addresses as discussed in the memory section. The outputs are produced as a function of bits 11 and 12 from the S register; E5, E6, and $\overline{E7}$ from the fixed bank extendible register; and signals from the fixed bank register.

4-5.5.14 Counter Address Signals. Counter address signals (figure 4-156) are generated whenever counters in erasable memory must be updated. These signals are generated as a function of bits 11 and 12 of register S; address selection signals $\overline{YT0}$, $\overline{YB0}$, and $\overline{XT2}$ through $\overline{XT6}$; and EB9, EB10, and EB11 from the erasable bank register. The address specified by these inputs must be less than 0100_8 or the generation of the counter address signals is inhibited by signal $\overline{NDR100}$.

Each counter address signal specifies certain locations in erasable memory as follows:

(1) OCTAD2 - Locations 0020 through 0027.

(2) OCTAD3 - Locations 0030 through 0037.

(3) OCTAD4 - Locations 0040 through 0047.

(4) OCTAD5 - Locations 0050 through 0057.

(5) OCTAD6 - Locations 0060 through 0067.

These output signals are supplied to priority control to prepare the priority cells to accept new incremental information.

4-5.5.15 Parity Logic. The parity logic (figure 5-157) insures that all words transferred from memory to the central processor are read out correctly and generates a parity bit for all words written into erasable memory. Parity check in the computer is that of odd parity; that is, the total number of ONE's in the word including the parity bit is odd.

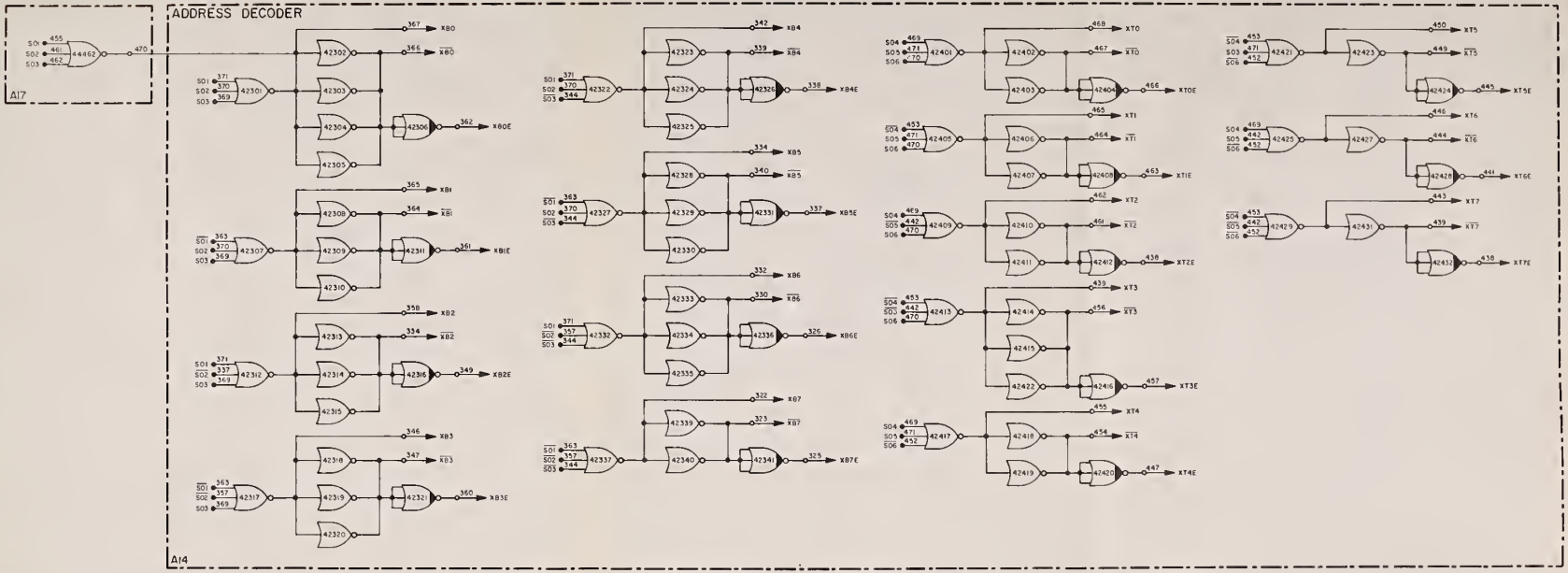


Figure 4-155. Address Decoder (Sheet 1 of 2)

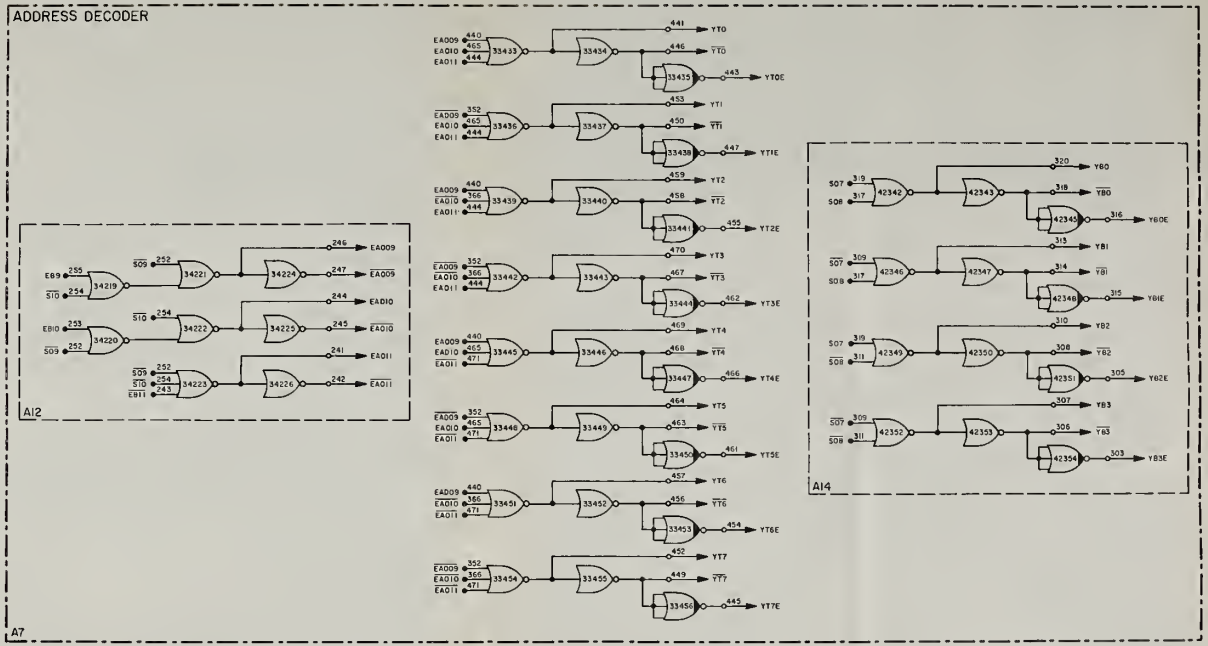


Figure 4-155. Address Decoder (Sheet 2 of 2)

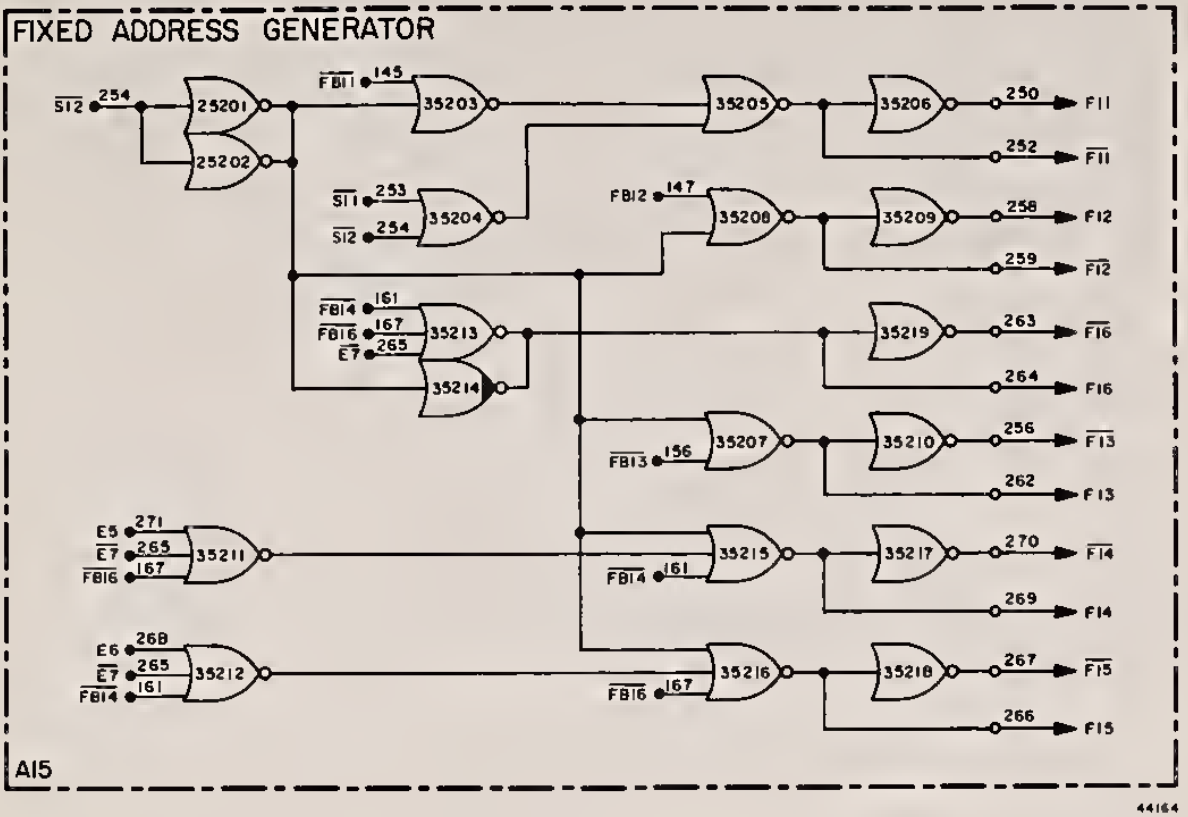


Figure 4-155A. Fixed Address Generator

Table 4-LXXVIII. Erasable Memory Address Selection

Unswitched Erasable Memory									Switched Erasable Memory									
Address	Register S Bits							Address Selection Signals	Bank	Address	E Bank Bits	Register S Bits						Address Selection Signals
	12 11 10	9 8 7	6 5 4	3 2 1							11 10 9	12 11 10	9 8 7	6 5 4	3 2 1			
0 0 0 0	0 0 0	0 0 0	0 0 0	0 0 0			XB0			1 4 0 0	0 0 0	0 0 1	1 0 0	0 0 0	0 0 0	YT0	YB0	XT0 XB0
				0 0 1														
				0 1 0														
				0 1 1	YT0	YB0	XT0		0									
				1 0 0														
				1 0 1														
				1 1 0														
0 0 0 7	0 0 0	0 0 0	0 0 0	1 1 1			XB7			1 7 7 7	0 0 0	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
0 0 1 0	0 0 0	0 0 0	0 0 1	0 0 0			XT1	XB0		1 4 0 0	0 0 1	0 0 1	1 0 0	0 0 0	0 0 0	YT1	YB0	XT0 XB0
					YT0	YB0			1									
0 0 7 7	0 0 0	0 0 0	1 1 1	1 1 1			XT7	XB7		1 7 7 7	0 0 1	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
0 1 0 0	0 0 0	0 0 1	0 0 0	0 0 0		YB1	XT0	XB0		1 4 0 0	0 1 0	0 0 1	1 0 0	0 0 0	0 0 0	YT2	YB0	XT0 XB0
					YT0				2									
0 3 7 7	0 0 0	0 1 1	1 1 1	1 1 1		YB3	XT7	XB7		1 7 7 7	0 1 0	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
0 4 0 0	0 0 0	1 0 0	0 0 0	0 0 0		YB0	XT0	XB0		1 4 0 0	0 1 1	0 0 1	1 0 0	0 0 0	0 0 0	YT3	YB0	XT0 XB0
					YT1				3									
0 7 7 7	0 0 0	1 1 1	1 1 1	1 1 1		YB3	XT7	XB7		1 7 7 7	0 1 1	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
1 0 0 0	0 0 1	0 0 0	0 0 0	0 0 0		YB0	XT0	XB0		1 4 0 0	1 0 0	0 0 1	1 0 0	0 0 0	0 0 0	YT4	YB0	XT0 XB0
					YT2				4									
1 3 7 7	0 0 1	0 1 1	0 0 0	0 0 0		YB3	XT7	XB7		1 7 7 7	1 0 0	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
										1 4 0 0	1 0 1	0 0 1	1 0 0	0 0 0	0 0 0	YT5	YB0	XT0 XB0
									5									
										1 7 7 7	1 0 1	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
										1 4 0 0	1 1 0	0 0 1	1 0 0	0 0 0	0 0 0	YT6	YB0	XT0 XB0
									6									
										1 7 7 7	1 1 0	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7
										1 4 0 0	1 1 1	0 0 1	1 0 0	0 0 0	0 0 0	YT7	YB0	XT0 XB0
									7									
										1 7 7 7	1 1 1	0 0 1	1 1 1	1 1 1	1 1 1		YB3	XT7 XB7

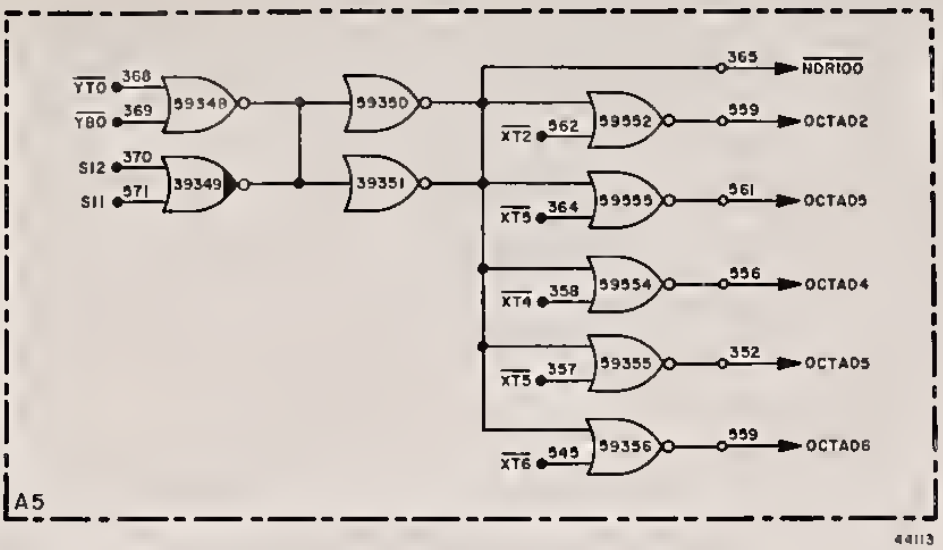


Figure 4-156. Counter Address Signals

A word read out of memory is applied directly to the parity logic from the bit outputs of register G (G01-G14 and G16), excluding bit 15, the parity bit, which is never placed on the write lines. The input gating complex of the parity logic combines the 15 bit input into a 5 bit output. The five bits are indicative of the inputs combined: PA03 indicates bits 1, 2, and 3; PA06, bits 4, 5 and 6; PA09, bits 7, 8, and 9; PA12, bits 10, 11 and 12; and PA15, bits 13, 14, and 16. The five bits are also indicative of the number of ONE's in each three bits and the total number of ONE's in the word. If any bit (PA03, PA06, etc.) is ZERO, an odd number of ONE's was contained in the three bits combined; if any is a ONE, an even number of ONE's was contained in the three bits combined. Likewise, if the 5 bit combination contains an odd number of ONE's, the entire word contained an odd number of ONE's and vice versa.

The five bit outputs and complements are applied to the parity tree (gates 34227, etc.). The inputs (PA03, PA06, etc.) are combined in this gating complex into a single output from gate 34240. This output is inverted by gate 34242.

The parity bit from memory (SAP) is applied to FF34245-34246. If the parity bit is a ONE, the flip-flop is set; if the parity bit is a ZERO, the flip-flop remains reset. The set and reset outputs of the flip-flop gate against the outputs of gates 34240 and 34242, respectively. If parity is correct, no alarm occurs; a parity error generates a parity alarm signal (PAL E).

When a word is to be written into erasable memory, the parity logic generates a parity bit and writes this bit into memory. This is accomplished as follows: A word being written into memory is deposited in register G. Simultaneously, the bit outputs of G are applied to the parity logic. The word is checked for an even or odd number of ONE's, and PAL E occurs in case of incorrect parity. The parity tree output is applied to gate 34243. This output (PC15) is the correct parity bit of the word. The parity bit is applied directly to memory as signal GEM15.

4-5.6 PRIORITY CONTROL. Priority control (figure 4-158) consists of three separate and functionally independent areas: start instruction control, interrupt instruction control, and counter instruction control. The start instruction control restarts the computer following a hardware or program failure. The interrupt instruction control forces the execution of the interrupt instruction RUPT to interrupt the current operation of the computer in favor of a programmed operation of higher priority. The counter instruction control updates counters in erasable memory upon the reception of certain incremental pulses.

4-5.6.1 Start Instruction Control. The start instruction control consists of the logic alarms processor and the start-stop generator. The logic alarms processor detects the presence of any one of several abnormal conditions that may occur within the computer, and generates an alarm signal (ALGA) whenever any of these conditions exist. The abnormal conditions are as follows:

1) RUPT lock

2) TC trap

3) Parity alarm

4) Night watchman fail.

A RUPT lock alarm indication occurs if a program interrupt has been in progress too long, or if an interruption has not occurred during a predetermined period. The latter is indicated by the presence of the interrupt in progress signal (IIP) from the sequence generator. A TC trap alarm indication occurs if too many TC or TCF instructions are executed, or if instruction TCF or increment signal (INKL) is not executed often enough. A parity alarm occurs if a word entered into the central processor from memory has been incorrectly read-out. A night watchman fail indication occurs if the computer fails to address location 0067 within a period varying from 0.64 to 1.92 sec.

The start-stop generator receives signal ALGA and generates the start order code signal (GOJAM) at the next time 12 to restart the computer. The restart condition is indicated on the DSKY by the RESTART lamp being lighted. The start-stop generator simultaneously produces the T12 STOP signal, which inhibits the generation of timing pulses $\overline{T01}$ through $\overline{T12}$ in the timer until signal GOJAM has reset all critical circuits in the computer, and forces the sequence generator to execute instruction GO.

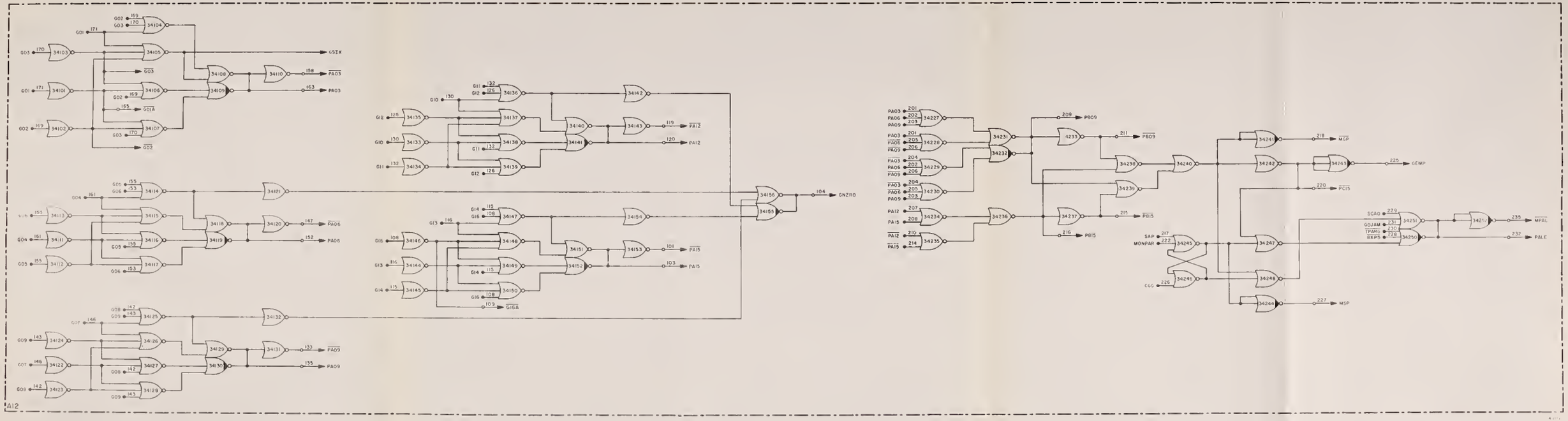


Figure 4-157. Parity Logic

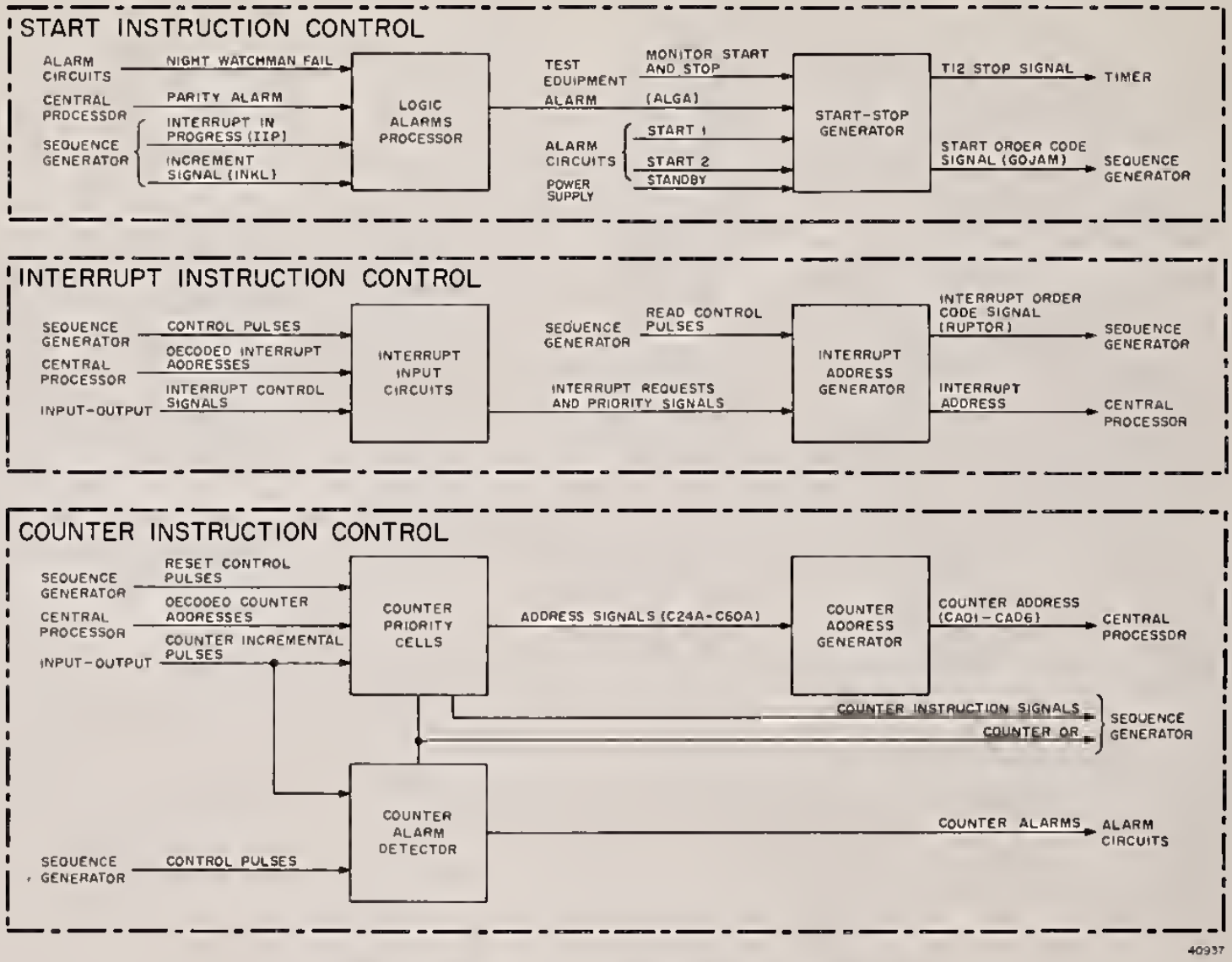


Figure 4-158. Priority Control Functional Diagram

Alarm signal STRT1 (power supply fail), alarm signal STRT2 (oscillator fail), or signal SBY (standby) also cause the computer to be restarted. In addition, the computer can be started or stopped manually from the peripheral equipment by signals monitor start and monitor stop. Signal monitor start coincident with timing pulse $\overline{T12}$ causes the generation of signal GOJAM, and signal monitor stop coincident with $\overline{T12}$ inhibits the generation of timing pulses $\overline{T01}$ through $\overline{T12}$ until the monitor stop signal is removed.

4-5.6.2 Interrupt Instruction Control. The interrupt instruction control, which consists of interrupt input circuits and an interrupt address generator, generates an interrupt address and the interrupt order code signal (RUPTOR) when interrupt control signals (requests) are received from the input-output section. The 12 bit interrupt address causes the addressing of one of ten locations in fixed memory in the LGC and one of nine locations in the CMC, dependent upon the interrupt request received. These locations contain the first instruction of an interrupt (RUPT) transfer subroutine which, when executed, initiates the execution of a particular routine within the program.

The interrupt input circuits receive interrupt control signals from the input-output section and decoded addresses from the central processor. From these inputs, the input circuits generate interrupt requests and priority signals subject to control pulses from the sequence generator. The interrupts are processed on a priority basis so that those interrupts having the highest priority (lowest priority number) are processed first. The priority signals specify the priority of the interrupt being processed. The interrupts and their respective priorities are indicated in table 4-LXXIX.

Table 4-LXXIX. LGC/CMC Interrupts

Priority	Interrupt Subroutine		Address
	LGC	CMC	
1	T6 RUPT	T6 RUPT	4004
2	T5 RUPT	T5 RUPT	4010
3	T3 RUPT	T3 RUPT	4014
4	T4 RUPT	T4 RUPT	4020
5	KYRPT1	KYRPT1	4024
6	KYRPT2, MKRPT	KYRPT2, MKRPT	4030
7	UPRUPT	UPRUPT	4034
8	DLKRPT	DLKRPT	4040
9	RADRPT	---	4044
10	HNDRPT	HNDRPT	4050

A T6RUPT enables information to be sent to the reaction control system; a T5RUPT enables information to be sent to the thrust vector control system; a T3RUPT enables the computer to perform internal tasks that must be performed at a specific time; and a T4RUPT enables information to be sent to the DSKY, ISS, and OSS. In the LGC, keycode interrupt KYRPT1 occurs when any key is depressed on the DSKY. Keycode interrupt KYRPT2 occurs when mark signals are received from the CCRD. An UPRUPT is generated when the flag bit appears in bit position 16 of the uplink word, indicating serial-to-parallel conversion is complete. A DLKRPT is generated when the downlink end pulse is received, indicating the end of a downlink transmission. This interrupt allows the appropriate output channel to be loaded in preparation for the next downlink transmission. A RADRPT occurs when inputs are received from the rendezvous radar. A HNDRPT occurs whenever a command is received from the hand controllers in the spacecraft.

The CMC has two associated DSKY's. Interrupts KYRPT1 and KYRPT2 occur as a result of inputs from the main and navigation keyboards respectively. The mark signals cause MKRPT directly in the CMC. The remaining interrupts are identical to those of the LGC except that there is no radar interrupt subroutine (RADRPT).

The interrupt address generator receives interrupt requests and priority signals and generates the address of the first location of the appropriate interrupt transfer subroutine. The addresses and the associated interrupt transfer subroutines are also indicated in table 4-LXXIX.

The interrupt address generator produces a signal $\overline{\text{RUPTOR}}$ which is applied to the sequence generator to cause the generation of instruction RUPT. Thus, when an interrupt condition occurs, the priority of the request is generated which inhibits the generation of lower priority interrupts, the address of the interrupt transfer subroutine is formed, and the sequence generator is conditioned to interrupt the normal program operation to allow the interrupt to be processed. The interrupt address is then supplied to the interrupt input circuits to reset them in preparation for the next interrupt.

4-5.6.3 Counter Instruction Control. The counter instruction control receives incremental pulses from the input-output section to update the various counters in erasable memory (locations 0024 through 0060). Counter instruction control consists of counter priority cells, a counter alarm detector, and a counter address generator. There are 29 priority cells in the counter instruction control, one cell per counter. When an incremental pulse is received, the appropriate priority cell generates an address signal and a counter instruction signal. The address signal enables the counter address generator to form the address of the counter to be updated; the counter instruction signal forces the sequence generator to generate counter instructions (PINC, MINC, SHINC, SHANC, PCDU, MCDU, and DINC).

The counters in memory are updated according to a priority scheme in which the counter having the lowest address has the highest priority and the counter having the

highest address has the lowest priority. When a particular counter is being updated, all other counters of lower priority are inhibited from being updated by the priority cells. In addition, the priority cells generate a counter OR (CTROR) signal which is supplied to the sequence generator and the counter alarm detector. This signal is used in the sequence generator to produce increment signal INKL, which must be generated prior to a counter instruction.

The counter address generator receives address signals from the priority cells and generates the address of the counter to be updated. This address is contained in six bits (CAD1 through CAD6) which are the six least significant bits; however, these six bits produce a 12 bit address in the central processor since the six most significant bits contain ZERO's when placed on the write lines. When the counter address is supplied to memory by the central processor, it is also supplied to the counter priority cells. This address in conjunction with reset control pulses from the sequence generator resets the priority cell that generated the address signal in preparation for the next incremental pulse.

Counter incremental pulses are also supplied to the counter alarm detector to insure the detection of abnormal counter activity. A counter alarm is generated if a counter is not updated following the generation of an increment request (INKL) by the sequence generator or if a counter increment lasts too long (over 0.625 msec). The counter alarm is forwarded to the alarm circuits to initiate a failure display.

4-5.6.4 Start Instruction Control Detailed Description. The start instruction control consisting of the logic alarms processor and the start-stop generator is illustrated in figure 4-159. Signal GOJAM is the resultant output of the start instruction control logic. This is, in effect, a master clear signal, which is applied to all functional areas of the computer except the power supplies, and conditions these functional areas for a restart condition. Signal GOJAM is generated by the start-stop generator for certain logic alarms, voltage failures from the power supply, standby operation initiation, or inputs from the peripheral equipment.

A RUPT alarm occurs if no interrupts occur within 160 milliseconds of each other, or if an interrupt is in progress for too long a time. This latter condition is referred to as RUPT lock. The RUPT alarm circuit consists of the two flip-flops: FF41107-41108 and FF41109-41110.

Consider that an interrupt has taken place and terminated. The condition being sensed is that another interrupt should occur within the specified period of 160 milliseconds. Refer to number 1 encircled on the timing diagram of figure 4-160. Signal F14B resets both flip-flops. However, as the interrupt terminates, signal $\overline{11P}$ becomes a logic ONE and sets FF41109-41110. The set output of this flip-flop inhibits gate 41113. The failure of another interrupt to occur is sensed by gate 41112. ff another interrupt occurs, FF41107-41108 is set by signal 11P. The set output inhibits gate 41112 and no alarm occurs. However, if another interrupt does not occur, the flip-flop remains reset. Signal $\overline{F14H}$ strobes gate 41112 generating signal ALGA (refer to number 2 encircled on figure 4-160).

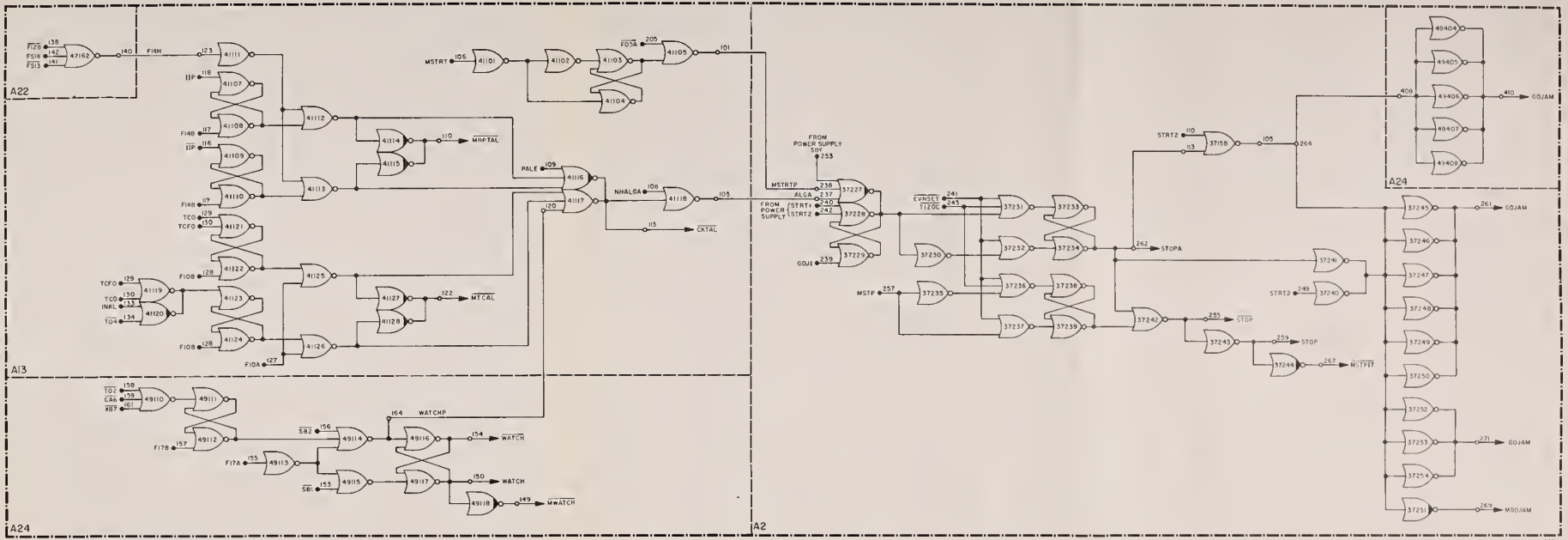


Figure 4-159. Start Instruction Control Detailed Logic

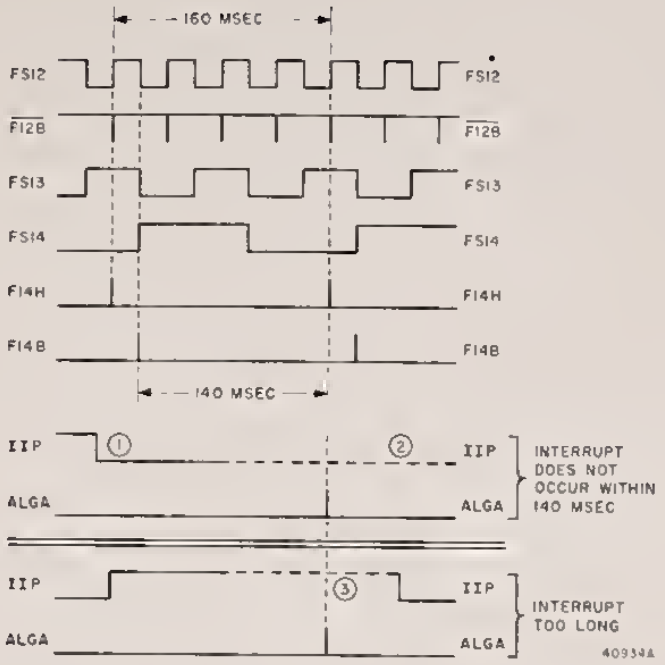


Figure 4-160. RUPT Alarm Logic Timing Diagram

A RUPT lock condition is sensed by gate 41113. When an interrupt occurs, FF41107-41108 is set by signal IIP thus inhibiting gate 41112. If the interrupt condition remains through the interval of two succeeding strobe pulses (F14H), FF41109-41110 will not be reset by F14B since signal $\overline{\text{IIP}}$ remains at a logic ZERO level. Signal $\overline{\text{F14H}}$ strobes gate 41113 generating signal ALGA (refer to number 3 encircled on figure 4-160). A RUPT alarm condition, either the failure of interrupts to occur within the specified period or a RUPT lock, is available to the peripheral equipment as signal $\overline{\text{MRPTAL}}$. There is no differentiation within the CSS between these two conditions. Actually there is no differentiation between any of the logic alarms described here. The only indication within the CSS of a logic alarm or power supply failure is the illumination of the RESTART lamp on the DSKY.

The transfer control alarm logic (FF41121-41122 and FF41123-41124) generates an alarm condition if transfer control (TC) or transfer control to fixed memory (TCF) instructions do not occur within approximately 15 milliseconds of each other, or if too many consecutive TC or TCF instructions are executed. The latter condition is referred to as TC trap. A condition of excessive counter incrementing is also indicated by this alarm logic.

Timing signals F10A and F10B establish the required interval for sensing a TC alarm condition. The period between these two pulses is 5 milliseconds as shown in figure 4-161. Signal F10B resets both flip-flops in the alarm logic, and signal F10A strobes the output gates. Consequently, approximately 5 to 15 milliseconds can elapse before a TC alarm is generated. This maximum period is illustrated in figure 4-161. A TC instruction is shown occurring first after reset pulse F10B. Signal F10B resets both flip-flops of the TC alarm logic. It would appear that FF41123-41124 would remain reset thus enabling gate 41126. However, in the first MCT following reset signal F10B, the flip-flop is set at time 4 ($\overline{T04}$) thus inhibiting gate 41126. Therefore, gate 41125 senses successive TC instructions within the specified period. Referring to figure 4-161 again, a TC instruction is executed and the signal TC0 or TCF0 sets FF41121-41122. Approximately 5 milliseconds elapses before F10A occurs to strobe the output gate. No alarm occurs since the set state of the flip-flop inhibits gate 41125 (number 1 encircled on figure 4-161). Signal F10B again resets both flip-flops. FF41123-41124 is set at time 4. If no TC or TCF0 instruction is executed before the next F10A strobe, signal ALGA is generated coincident with F10A as shown by number 2 encircled on figure 4-161.

If the computer is executing TC instructions continually (TC trap) or if counter incrementing is excessive, the indication to the alarm logic is effectively a level since the computer is caught in a continuous loop. The period in which this condition would be sensed varies from a minimum of approximately 5 milliseconds to a maximum of approximately 15 milliseconds. Figure 4-161 depicts the maximum period (number 3 encircled). FF41123-41124 can conceivably set immediately after F10B occurs. Therefore, when the first F10A strobe occurs after the computer is in a TC trap, no alarm indication is generated. An alarm indication is generated when the second F10A strobe occurs. A TC alarm condition is available to the peripheral equipment as $\overline{MTCAL}$.

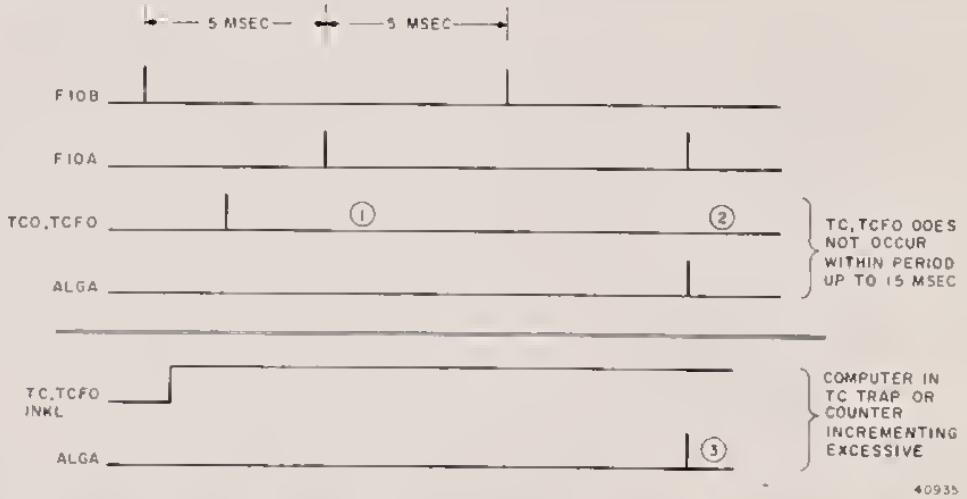


Figure 4-161. Transfer Control Alarm Logic Timing Diagram

The WATCH logic alarm generates signal ALGA if the computer fails to address location 00067 within a period varying from approximately 0.65 sec. to approximately 1.9 sec. The period is established by signals F17A and F17B as shown on the timing diagram of figure 4-162. Signal F17B resets FF49111-49112. If location 0067 is addressed before F17A occurs, the flip-flop is set thus inhibiting gate 49114. If this location is not addressed within this interval, the flip-flop remains reset and gate 49114 is enabled and strobed by F17A. Thls action generates signal WATCHP, which produces ALGA and causes the watch flip-flop (FF49116-49117) to set. The minimum and maximum intervals are illustrated in figure 4-162.

The output of gate 49110 is indicative of location 0067 being addressed at time 2 of a particular memory cycle. At the time shown, the location is addressed approximately 0.65 millisecond prior to F17A. The location must be addressed again prior to the next F17A strobe. As indicated, this address is a maximum of approximately 1.9 seconds from the previous time at which location 0067 was addressed.

A parity alarm (PALE) indicates that a word read out of fixed or erasable memory contains an even number of ONE's. This logic alarm indication is applied directly to the output gates of the logic alarms processor to generate signal ALGA, and subsequently signal GOJAM. Signal ALGA can be inhibited by input NHALGA which is applied to gate 41118 from the peripheral equipment. This inhibit prevents any of the logic alarms described above from generating signal GOJAM.

The start-stop generator generates signal GOJAM to restart the computer in response to the logic alarms go signal ALGA; signals STRT1, STRT2, and SBY from the power supplies, and inputs from the peripheral equipment. Signal STRT1 indicates failure of the +4 and +14 volt power supplies; signal STRT2 indicates failure of the oscillator (both are described in paragraph 4-5.9 - Power Supplies). Signal SBY occurs when the standby mode of operation is initiated. Signal MSTRT from the peripheral equipment sets FF41103-41104. The flip-flop output is gated by timing signal $\overline{F05A}$

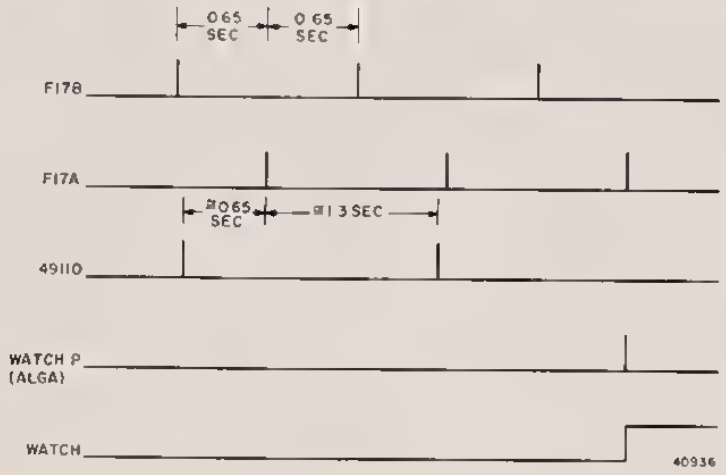


Figure 4-162. Watch Alarm Timing

to produce MSTRTP to the input flip-flop (FF37228-37229) of the start-stop generator. Flip-flop 41103-41104 is reset when MSTRT reverts to logic ZERO.

Any one of the signals described, ALGA, STRT1, STRT2, SBY, or MSTRTP, sets the start-stop generator input flip-flop. At the following time 12 or at the end of a memory cycle, a secondary level flip-flop (FF37233-37234) is set. The STOPA output of this latter flip-flop generates signal STOPA, STOP and its complement, and causes signal GOJAM. Signal STOP inhibits outputs from the time pulse generator in the timer, and $\overline{\text{STOP}}$ the memory cycle timing. Signal GOJAM is applied to all functional areas of the computer except the power supplies and essentially initializes the computer for a restart condition. In the sequence generator, GOJAM causes subinstruction GOJI to be generated. This signal resets the input flip-flop which subsequently resets the secondary level flip-flop (coincident with $\overline{\text{EVNSET}}$) thus removing the STOP signal, which allows the time pulse generator to run. Signal STRT2, the oscillator fail signal, generates signal GOJAM immediately without the timing restrictions of $\overline{\text{EVNSET}}$ and $\overline{\text{T12DC}}$ applied to gate 37231.

Signals STOP and GOJAM are also generated by input MSTP from the peripheral equipment. The monitor stop input sets FF37238-37239 at the end of a memory cycle ($\overline{\text{T12DC}}$), and causes signals STOP and GOJAM. The time pulses resume when the monitor stop input is removed. This feature allows individual memory cycle times to be observed on the peripheral equipment.

4-5.6.5 Interrupt Instruction Control Detailed Description. The interrupt instruction control logic (figure 4-163) accepts interrupt requests, generates an associated address, and causes a program interrupt routine to be initiated.

There are ten interrupt conditions in the LGC and nine in the CMC, indicated in table 4-LXXIX. Each interrupt sets an associated flip-flop in the input circuits. The flip-flops are arranged in order of priority of the interrupts in figure 4-163. The outputs labeled R1 through R10 (and complements) also indicate this priority. An input flip-flop is set by an interrupt request; its outputs are applied through the priority control logic to the address generator. The flip-flop is reset by reset pulse $\overline{\text{KRPTA}}$ coincident with the generated address. For example, a T6RUPT occurs when address 0031 is coincident with signal $\overline{\text{ZOUT}}$ in the counter priority cells. The output of gate 35307 sets FF35308-35309 generating signal R1. The output of gate 35307 also generates signal T6RUPT which clears bit position 15 of channel 13. All lower priority interrupts are inhibited until T6RUPT is completed. This is accomplished by signal R1 applied to gate 35320. The inhibit action is effective down through all lower priority control gates and allows FF35234-35235 to set (by timing pulse T10) enabling signal $\overline{\text{RUPTOR}}$. This flip-flop is reset when no further interrupt requests are present. Signal $\overline{\text{RUPTOR}}$ is applied to the sequence generator to initiate the interrupt condition in the computer.

Signal R1 is applied to the address generator, directly to gate 35350 and through gates 35314 and 35319. This action enables the output gates, and, when read signal $\overline{\text{RRPA}}$ occurs, output RPTAD3 becomes a logic ONE. All of the outputs from the

priority control as a function of bit 8. A ONE entered into this bit position of channel 13 allows these incremental inputs to initiate a counter interrupt sequence in priority control and update an associated counter in memory. Bits 10, 11, and 15/16 of channel 13 are control bits for functions internal to the LGC. Bit 10 (Alarms Test) lights the RESTART and STBY lamps on the DSKY. Bit 11 enables the LGC to enter the standby mode. Bit 15/16 enables the T6 interrupt routine. The manual inputs entered into channel 31 (attitude and translational) initiate an interrupt sequence under program control through bits 12 and 13 of channel 13. The manual discrete inputs are applied to the handrupt control logic. The program enters the proper data into positions 12 and/or 13 and HNDRPT is initiated.

The output channels (figure 4-159) are all flip-flop registers with write and read service. Data is written into the output channels from the central processor coincident with an address supplied by the program into the service gates. Output channels 5, 6, 10, 11, and 12 supply output discretes to other systems as indicated in figure 4-159. Channel 14 controls the transmission of incremental drive pulses to the gyros and the CDU. An output is enabled (gyro or CDU) by placing a ONE in the proper bit position of channel 14. This is accomplished by the program. For example, the program enters a ONE into bit position 11 of channel 14. This results in an interrupt request signal which is applied to priority control. Further processing by priority control results in a command request to the sequence generator and an address command to the central processor. This same address (in this case 0054) enables the output drive logic and allows the drive pulses to be gated out. The associated output counter register in memory is loaded by program and a pulse burst is sent to the CDU. Each time the counter is processed the number in the counter register is diminished by one such that the content of the counter approaches zero. When the number has reached zero, the channel bit position is reset and the pulse burst terminates.

The outlink control logic is functionally illustrated in figure 4-161. Outlink consists of the downlink word to the spacecraft telemetry, and the crosslink word to the CMC. The word to be transmitted downlink is loaded into channel 34 from the central processor. DLKRPT is initiated by the downlink rupt circuit. DKSTRT is converted to a clear pulse to clear the downlink counter, and also sets the read flip-flop. The bit sync pulses then step the counter and the outputs are decoded to strobe the bit positions of channel 34, and produce a serial word output. The rate of transmission is monitored, and, if too fast, a bit is entered into bit position 12 of channel 33. Crosslink is the output word from the LGC to the CMC. Bit 1 of channel 14 enables the outlink control logic. An interrupt request signal is sent to priority control to initiate an interrupt sequence. The address of the crosslink counter enables the word from the central processor to be transmitted serially to the CMC.

4-5.8 MEMORY. Memory consists of an erasable memory with a storage capacity of 2048 words and a fixed core rope memory with a storage capacity of 36,864 words. Erasable memory is a random-access, destructive readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a nondestructive storage device. Data stored in fixed memory is unalterable since the data is wired in.

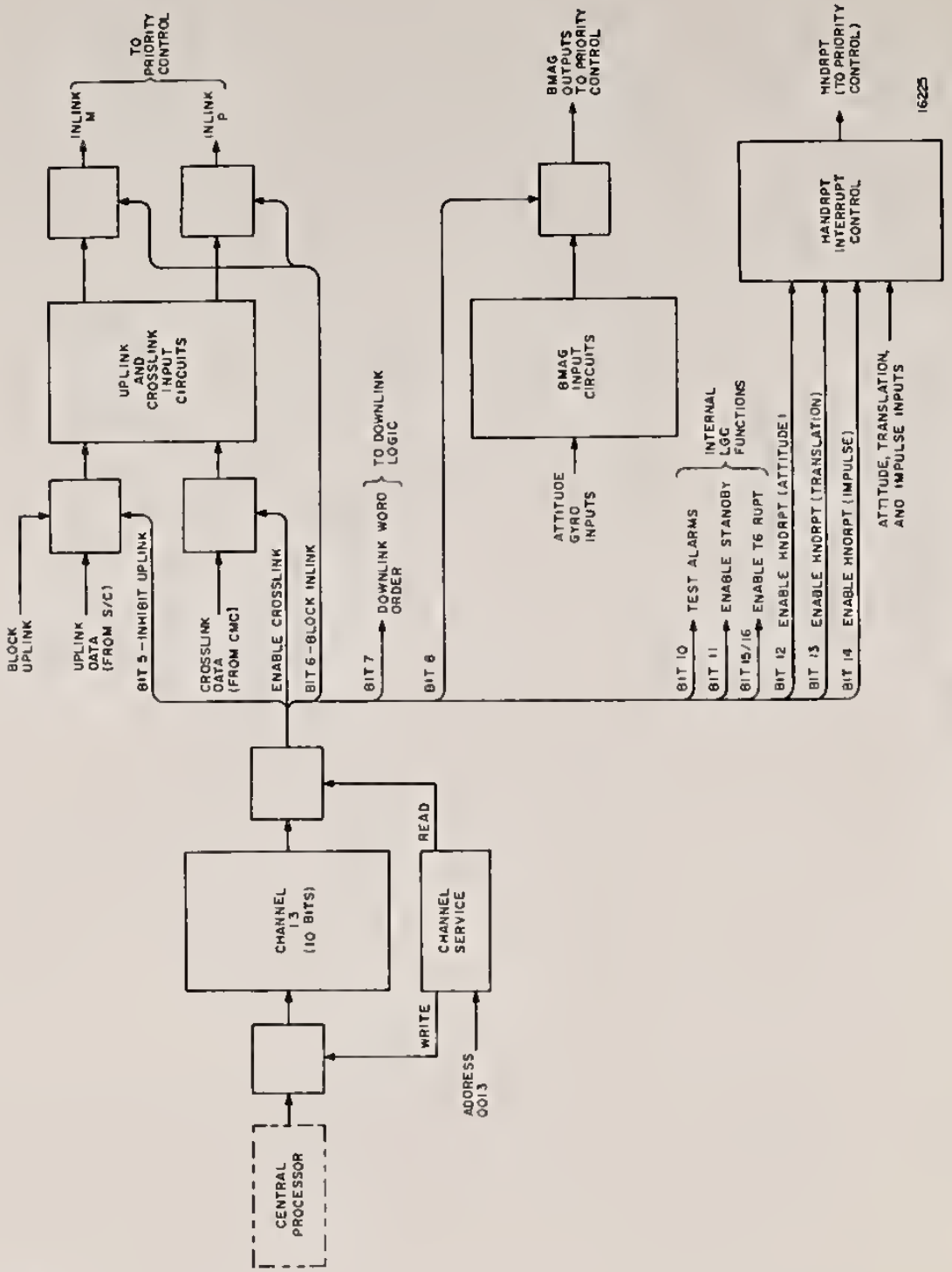


Figure 4-160. Inlink Functional Diagram

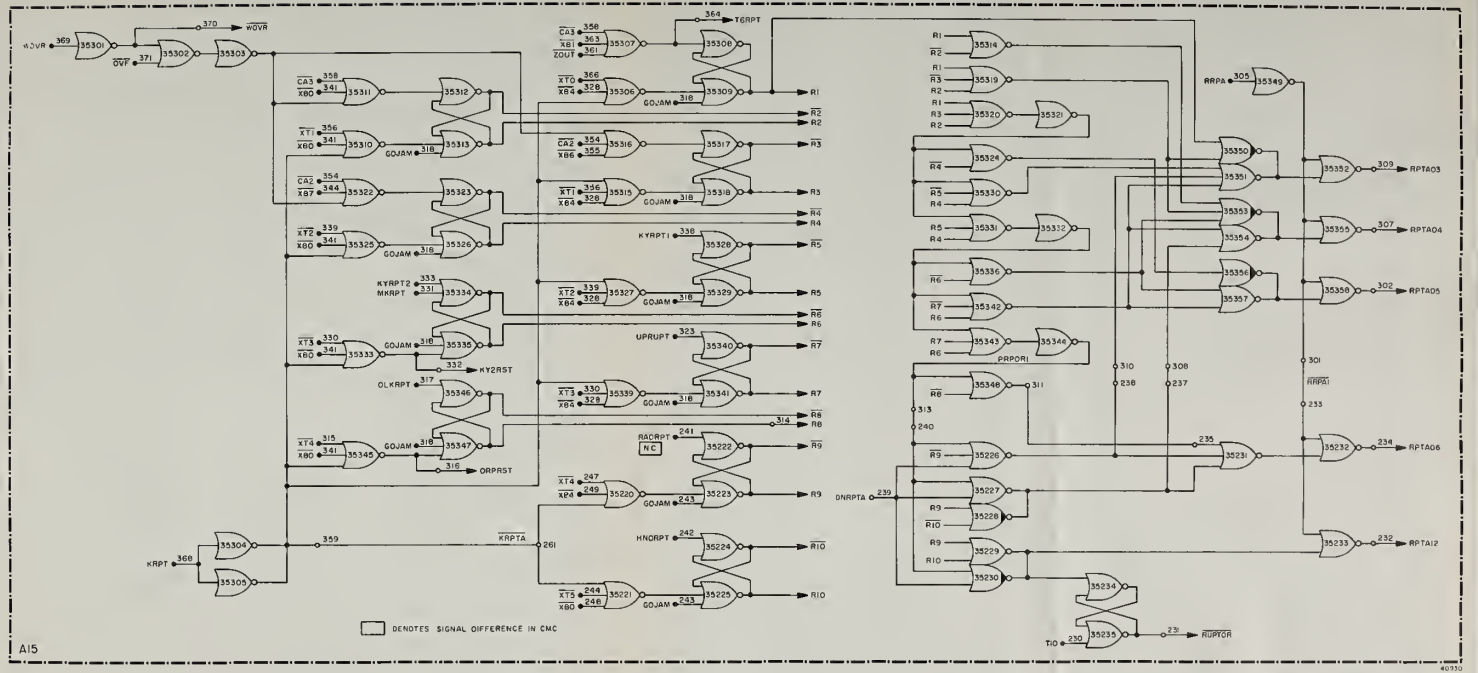


Figure 4-163. Interrupt Instruction Control Detailed Logic

address generator (RPTAD3, RPTAD4, RPTAD5, RPTAD6, and RPTA12) in combination generate address 4004 from the write lines in the central processor. This is the address of the T6RUPT routine.

When $\overline{\text{RUPTOR}}$ initiates the routine to interrupt the program presently being executed, the sequence generator causes suhinstruction RUPT0 and RUPT1 to be executed. During subinstruction RUPT0, information on the program is temporarily stored in memory and the computer is readied to execute RUPT1. At time 3 of subinstruction RUPT1, the interrupt address is placed on the write lines by read signal $\overline{\text{RRPA}}$. The computer then executes the interrupt routine. At time 9 of subinstruction RUPT1, reset signal $\overline{\text{KRPTA}}$ resets the T6RUPT input flip-flop coincident with partial address 04 ($\overline{\text{XT0}}$ $\overline{\text{XB4}}$). Any lower priority interrupt request is then processed after the completion of T6RUPT.

The remaining interrupts are processed in a manner identical to that of T6RUPT except that the portion of the address used to reset the input flip-flop is the address associated with the particular interrupt involved. The address portion used can be determined from table 4-LXXIX (10 - T5RUPT, 14 - T3RUPT etc.). Interrupts KYRPT2 and MKRPT share the same input flip-flop (FF35334-35335) and consequently the same priority. Table 4-LXXX indicates the function of all interrupt routines in both the LGC and CMC.

Tahle 4-LXXX. LGC/CMC Interrupt Functions

Interrupt	Priority	Function
T6RUPT	R1	Causes execution of program section Reaction Control.
T5RUPT	R2	Causes execution of program section Trans Vector Control when T5 counter overflows.
T3RUPT	R3	Causes execution of routine T3RUPT of program section Waltlister - Task Control when T3 counter overflows.
T4RUPT	R4	Causes execution of routine T4RUPT of program section T4RUPT - Output Control when T4 counter overflows. Enahles information to he sent to DSKY, ISS, and OSS.
KYRPT1	R5	Causes execution of program section Keyboard and Display when data from DSKY is punched-in (main DSKY in CMC).

(Sheet 1 of 2)

Table 4-LXXX. LGC/CMC Interrupt Functions

Interrupt	Priority	Function
KYRPT2	R6	Causes execution of associated program section when inputs occur from MARK button in LGC. (Program section Keyboard and Display is executed in CMC as a result of navigation keyboard inputs.)
MKRPT	R6	Causes execution of associated program section to process rate of descent inputs in LGC. (Program section MARK is executed in CMC to process optics data.)
UPRUPT	R7	Causes execution of program section UPRUPT to process uplink data when flag bit of uplink word is received.
DLKRPT	R8	Causes execution of program section DOWNRUPT to load downlink channel 34 with new word.
RADARPT (LGC only)	R9	Causes execution of program section Radar to process data from rendezvous radar when flag bit is received.
HNDRPT	R10	Causes execution of program section Hand Control when attitude, translation, or impulse hand control inputs occur.

(Sheet 2 of 2)

4-5.6.6 Counter Instruction Control Detailed Description. Counter instruction control consists of 29 priority cells, each of which has an associated counter register in erasable memory. Table 4-LXXXI lists the priority cells and associated counters, the location in erasable memory, the type of cell (input or output), and the instruction(s) initiated by each cell as a result of input data. The listing in table 4-LXXXI also indicates the priority in which the counter registers are processed. The counter with the lowest address (0024) has the highest priority, and the counter with the highest address (0060) the lowest priority. Twenty of the priority cells accept either incremental or serial data inputs and are termed input cells. Of the remaining nine cells, eight are used in conjunction with output pulse trains to the gyros, CDU's, and the spacecraft. The ninth is used to form the serial outlink word. These cells are termed

Table 4-LXXXI. LGC/CMC Counter Cell/Register Assignments

Octal Address	Cell Register Name	Type	Instruction Initiated	
0024	T2(TIME2)	Input	PINC	+ Increment Add One
0025	T1(TIME1)	Input	PINC	
0026	T3(TIME3)	Input	PINC	
0027	T4(TIME4)	Input	PINC	
0030	T5(TIME5)	Input	PINC	
0031	T6(TIME6)	Input	DINC	Diminish by One
0032	CDUX	Input	PCDU, MCDU	+ or - CDU Add One, Subtract One (TWO's Complement)
0033	CDUY	Input	PCDU, MCDU	
0034	CDUZ	Input	PCDU, MCDU	
0035	TRN	Input	PCDU, MCDU	
0036	SHFT	Input	PCDU, MCDU	
0037	PIPAX	Input	PINC, MINC	+ or - Increment Add One, Subtract One (ONE's Complement)
0040	PIPAY	Input	PINC, MINC	
0041	PIPAZ	Input	PINC, MINC	
0042	BMAG X (RHC)	Input	PINC, MINC	
0043	BMAG Y (RHC)	Input	PINC, MINC	
0044	BMAG Z (RHC)	Input	PINC, MINC	
0045	INLINK	Input	SHINC, SHANC	Shift (ZERO in) OR Shift & Add One (ONE in)
0046	RNRAD (LGC Only)	Input	SHINC, SHANC	
0047	GYROD	Output	DINC	Diminish by One
0050	CDUXD	Output	DINC	
0051	CDUYD	Output	DINC	
0052	CDUZD	Output	DINC	
0053	TRUND	Output	DINC	
0054	SHAFTD	Output	DINC	
0055	THRSTD	Output	DINC	
0056	EMSD	Output	DINC	
0057	OTLNK	Output	SHINC	Shift (Serial Output)
0060	ALT (LGC Only)	Output	SHINC	

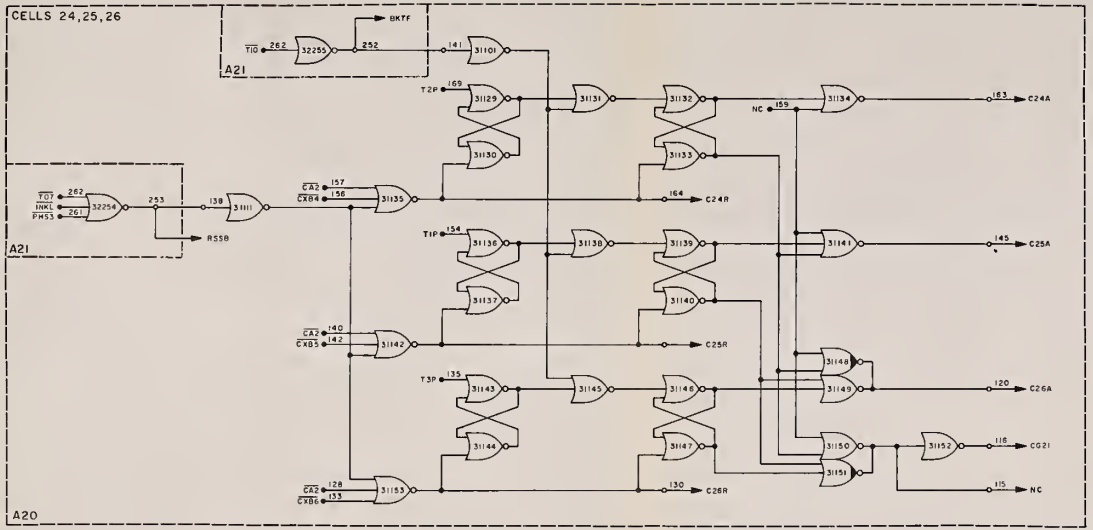
output cells. The priority cells are further differentiated by the type of instruction or command generated to update the counter. The time counter registers, T1 through T5, are incremented only. Consequently, the cells associated with these counter registers initiate a PINC (plus increment) instruction only. Time counter register T6 is preset by program. The cell associated with this register initiates instruction DINC (decrement) to diminish the contents of the counter toward zero. The counter cells for the CDU's of the ISS and OSS initiate instructions PCDU or MCDU dependent on the input. In a similar manner, the counter cells for the PIPA's and BMAG's initiate either a plus increment (PINC) or minus increment (MINC) instruction. The inlink and radar words are serial inputs. Consequently, shift instructions SHINC or SHANC are initiated by the associated counter cell depending on whether a ZERO or ONE bit is received.

All of the output cells, with the exception of outlink control (OTLNK) and altitude meter control (ALT), initiate instruction DINC. The associated counter registers are preset by program, and the contents diminished toward zero when the cells receive input requests. The outlink and altitude meter control output cells initiate instruction SHINC only. These are serial outputs and instruction SHINC causes the word to be shifted out serially.

The input counter priority cells (figure 4-164) store incoming requests for updating the counter registers until the requests can be processed. The requests are stored in an input flip-flop. At time 10 of a particular memory cycle, a transfer pulse occurs (BKTF), the request is transferred to a secondary flip-flop which generates an address request signal, and an inhibit signal is applied to all lower priority counter cells. For example, input pulse T2P sets FF31129-31130 of cell 24. At time 10, transfer signal BKTF occurs and causes FF31132-31133 to set. The set output is applied to the output gates of cells 25 and 26 and inhibits the outputs from these cells. The set output of FF31132-31133 is also applied through gate 31150 to generate inhibit signal CG21, which is applied to the output gates of cells 27, 30, and 31. Inhibit signal CG22 is generated from gate 31252 by signal CG21 and inhibits outputs from cells 32 and 33. The inhibit action continues down through all lower priority cells (CG11, CG12 etc.) to the altitude cell (0060). At this point, the inhibit signal generates CTROR, which is applied to the sequence generator indicating a counter increment request.

The reset output of FF31332-31333 is used to generate address and command request signal C24A. This is applied simultaneously to the counter address generator to produce address 0024 and to the counter instruction logic in sequence generator to initiate instruction PINC. Instruction PINC increments by one the content of the T2 counter register in erasable memory.

Both the input flip-flop (FF31129-31130) and the secondary flip-flop (FF31132-31133) are reset by the generated address (inputs $\overline{CA2}$ and $\overline{CXB4}$ to gate 31135) coincident with reset signal $\overline{RSSB}$. The latter signal is generated at time 7 as a function of counter increment request signal $\overline{INKL}$ from the sequence generator.



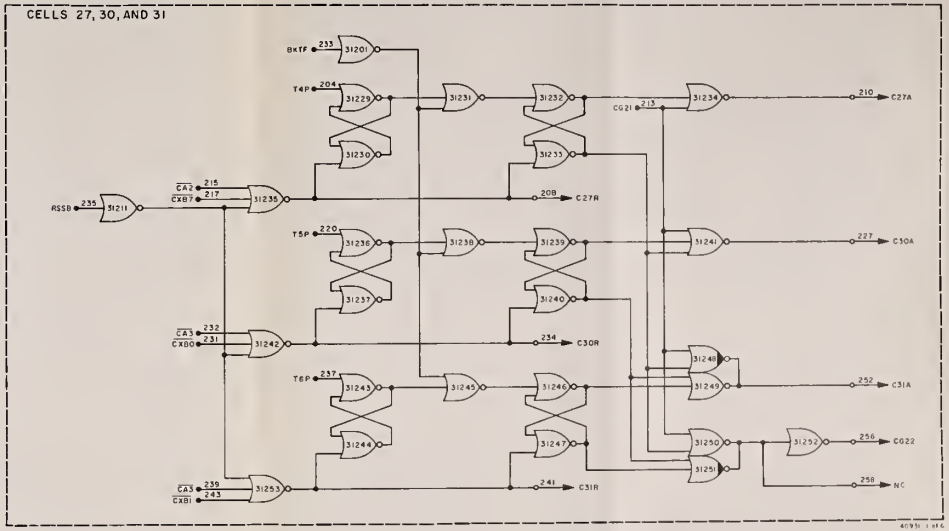
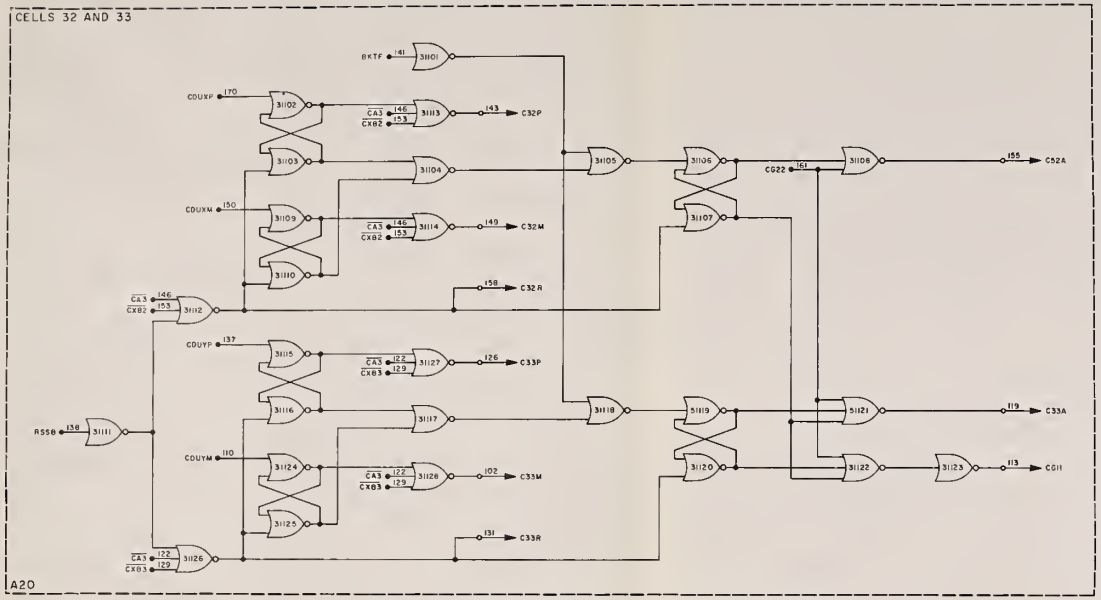


Figure 4-164. Counter Priority Cells
(Sheet 1 of 6)



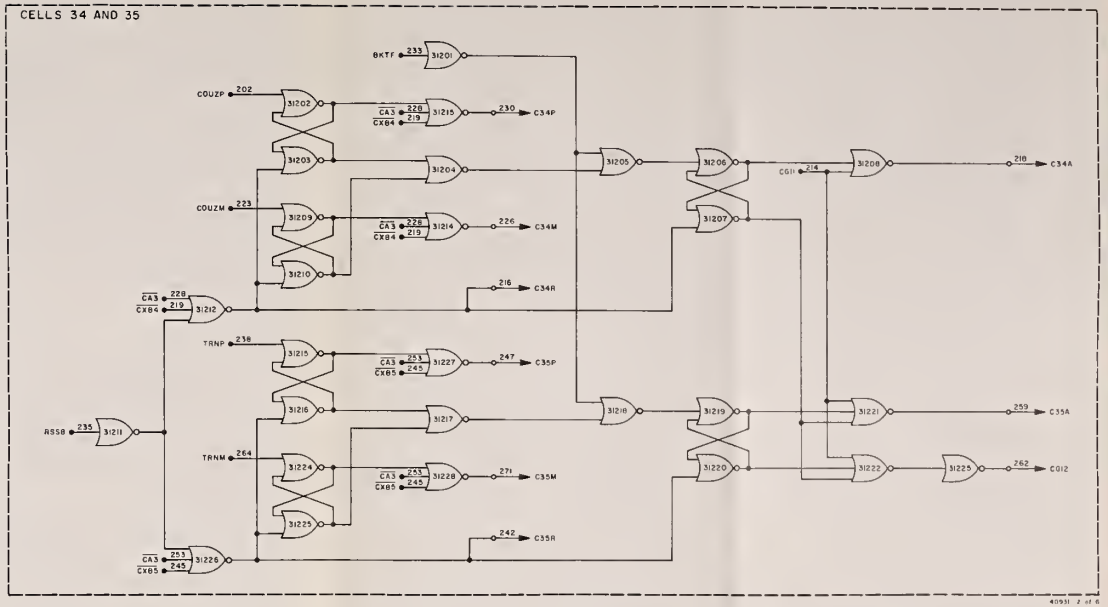
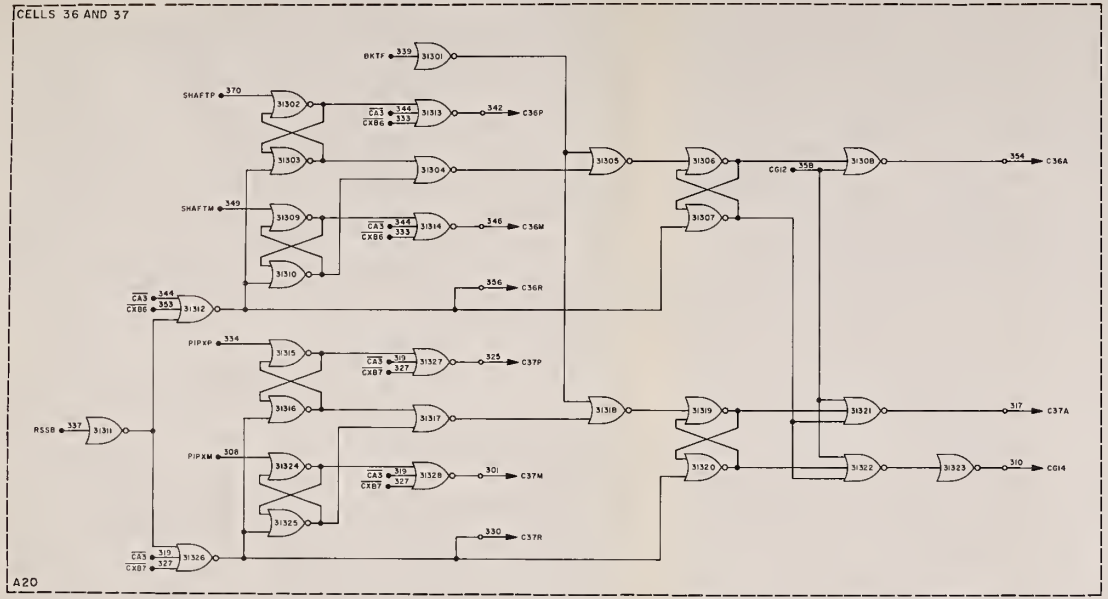


Figure 4-164. Counter Priority Cells (Sheet 2 of 6)



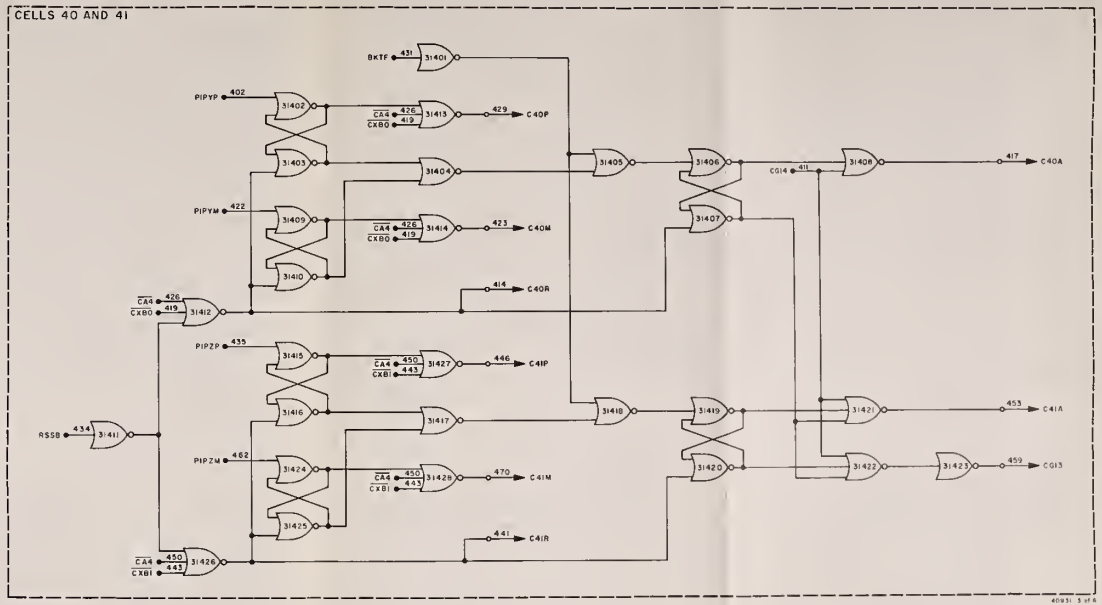
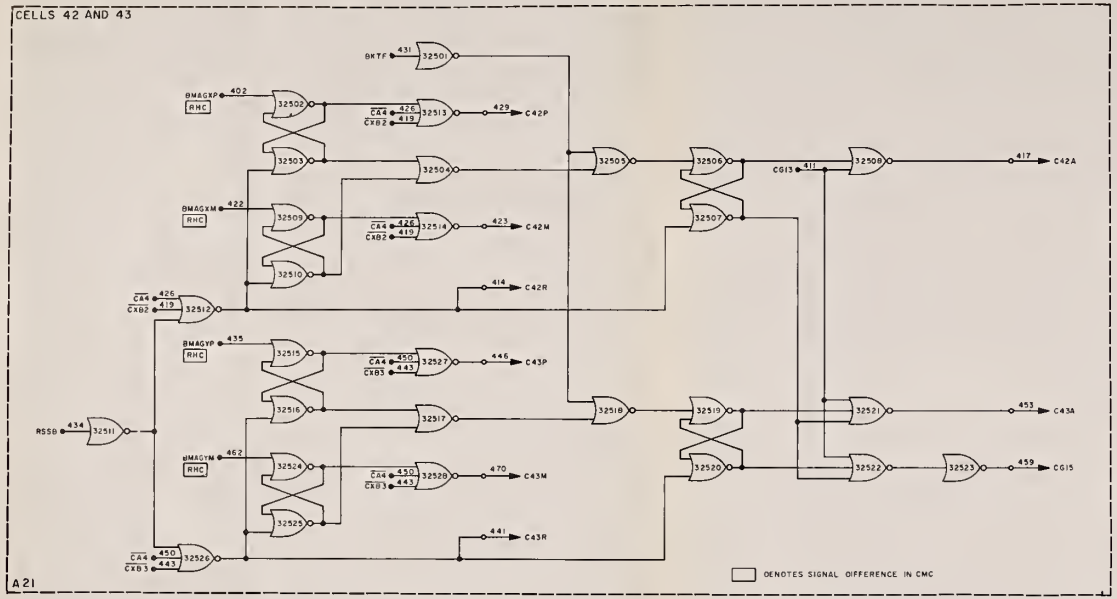


Figure 4-164. Counter Priority Cells (Sheet 3 of 6)



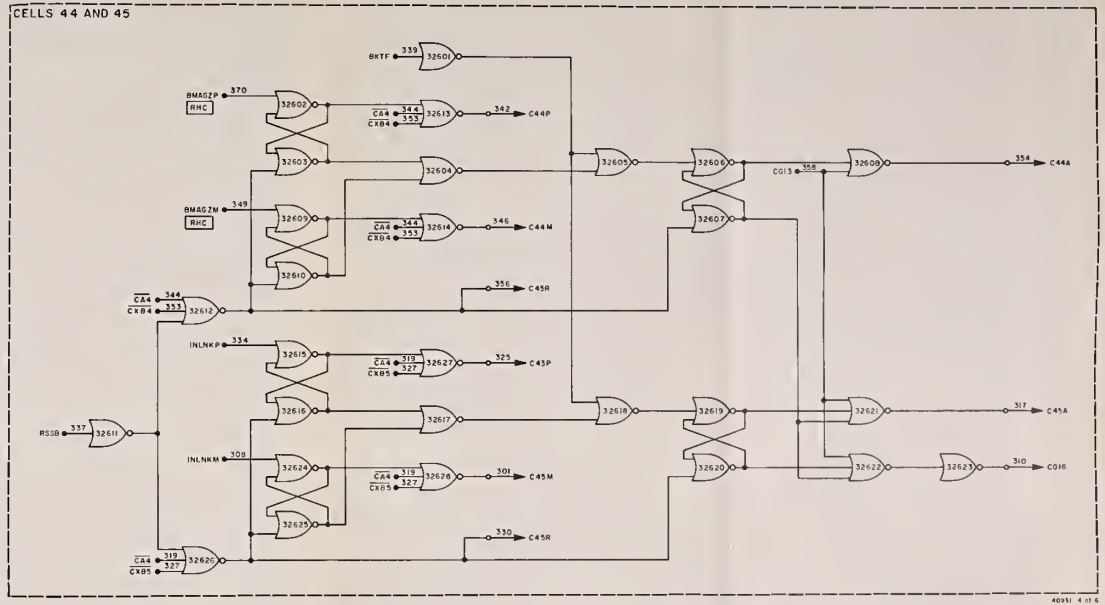
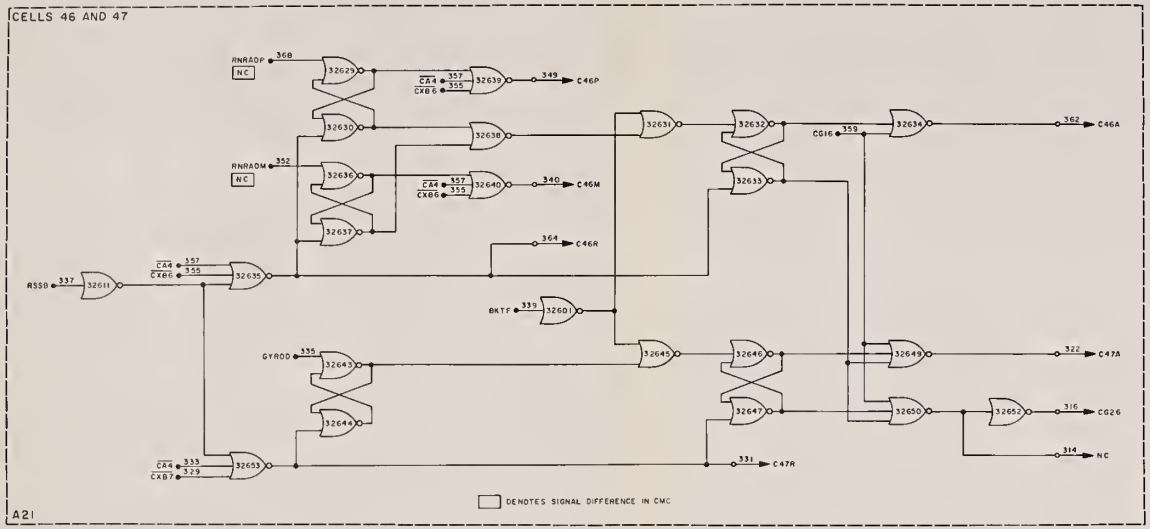


Figure 4-164. Counter Priority Cells
(Sheet 4 of 6)



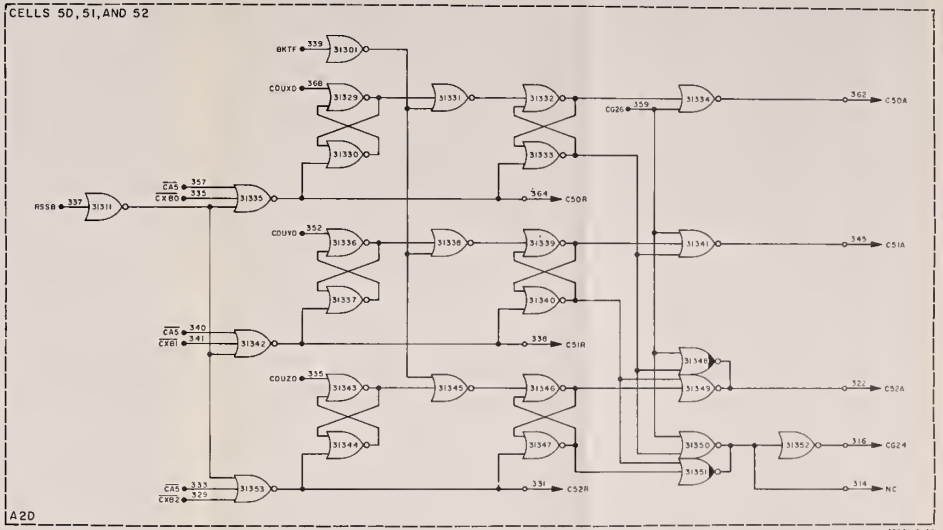
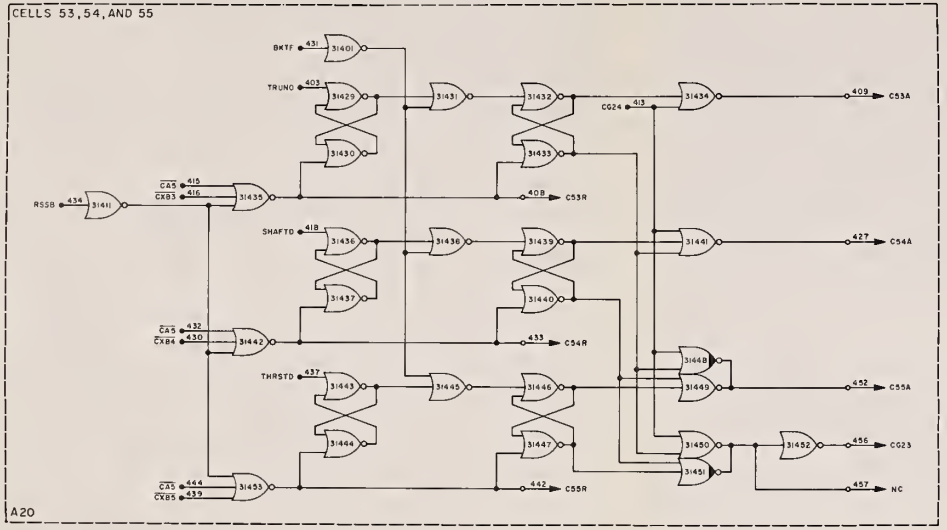


Figure 4-164. Counter Priority Cells (Sheet 5 of 6)



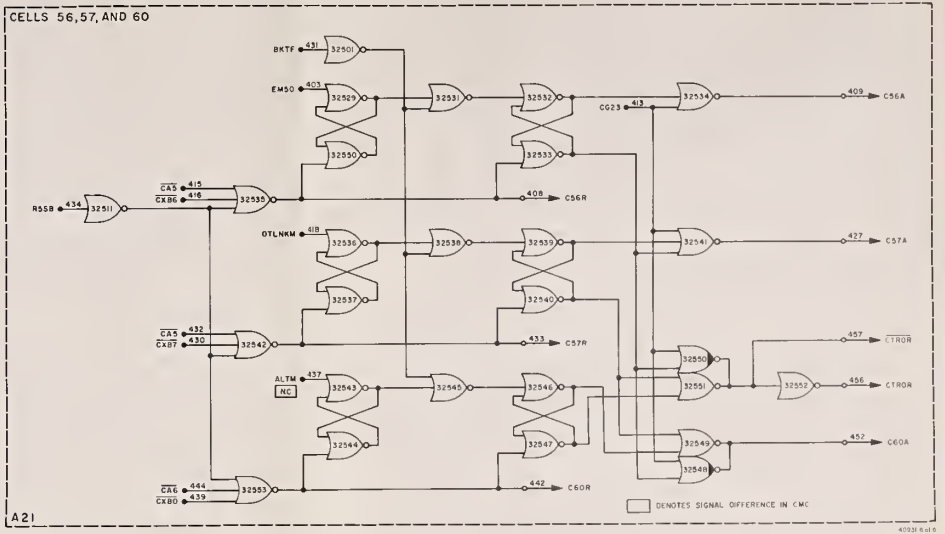


Figure 4-164. Counter Priority Cells (Sheet 6 of 6)

Cells 25, 26, 27 and 30, 31 are identical in operation to cell 24. One difference exists in cell 31; instruction DINC is executed instead of instruction PINC. This counter register is preloaded by program. The content of the counter is diminished by one each time request signal T6P occurs.

Cells 32 through 36 (PCDU and MCDU) and 37, 40 through 44 (PINC and MINC) contain two input flip-flops to accommodate incremental pulses representing a positive or negative input. The processing of these inputs in priority control is different in that two separate signals are generated to produce the counter instructions. The instructions initiated update the counter registers in TWO's complement notation in the case of the CDU inputs, or in ONE's complement in the case of the PIPA and BMAG inputs. The correct notation is accomplished in the central processor as a result of the instructions initiated by the inputs to these cells.

As an example of the operation of these cells, consider cell 35 (TRN). An incremental input TRNP or TRNM sets a respective input flip-flop (FF31215-31216 or FF31224-31225). The set outputs of both flip-flops are OR'ed and gated with transfer signal $\overline{\text{BKTF}}$ to set the secondary flip-flop (FF31219-31220). This set output of this flip-flop generates priority signal CG12 to inhibit all lower priority cells. The reset output generates address request signal C35A, which is applied to the counter address generator only. One of two counter instructions is initiated by the cell. The address request signal does not initiate the instruction, as cell 24 request signal does. With a positive incremental input, signal C35P from the input flip-flop initiates instruction PCDU; with a negative incremental input, signal C35M initiates instruction MCDU. These two instructions are analogous to instructions PINC and MINC for the PIPA and BMAG (RHC) inputs except that TWO's complement notation is employed in the central processor as described. The timing relationship between the transfer and reset signals is identical to that described for cells 24 through 31.

Input cells 45 and 46, the inlink and rendezvous radar counters respectively, receive serial input data. The rendezvous radar cell and counter register is active in the LGC only. The serial inputs are converted to a parallel word by instruction SHINC for a ZERO in, and SHANC for a ONE in. The cells operate as cell 35, described above, operates. There are two input flip-flops in each cell for receiving one of two possible inputs. The input flip-flop outputs initiate instruction SHINC or SHANC, and a secondary flip-flop is used to generate the address. In the central processor, instruction SHINC shifts a ZERO into the parallel word being formed; instruction SHANC shifts and adds a ONE to the word being formed. When the complete word is formed, the flag bit initiates a program interrupt routine (UPRUPT or RADRPT).

Output cells 47, 50 through 57, and 60 operate in conjunction with output counter registers in erasable memory. Cells 47, and 50 through 56 are used in conjunction with functional areas of the input/output section providing drive pulses to the gyros, CDU's and the spacecraft (see table 4-LXXXI). These cells are identical in operation to cell 24 described above except that instruction DINC is initiated. The counter registers are preloaded by program. Each time an incremental request occurs (such

as GYROD, CDUXD etc.) instruction DINC diminishes the counter content toward zero. Drive pulses are transmitted to the associated unit until the counter reaches zero, at which time the drive pulses cease.

The outlink and altitude meter control cells (57 and 60) initiate instruction SHINC to shift the associated word contained in the counter register in memory out in serial fashion. For example, the outlink logic supplies incremental input OTLNKM. This input is generated as a function of a ONE entered into channel 14, bit 1 (outlink activity). The cell generates request signal C57A, which places address 0057 onto the write lines from the address generator, and initiates instruction SHINC in the sequence generator. Instruction SHINC causes one bit of the word to be shifted out through the outlink logic in the input-output section. The manipulation is accomplished in the central processor. The word from the outlink counter register in memory is deposited into register Y in the central processor. Instruction SHINC essentially shifts the word left so that one bit is shifted into the overflow bit position on each shift request. Overflow is sensed for by the branch control logic in the sequence generator, and the appropriate bit is shifted out through the outlink logic. The shift manipulation for the altitude meter control word is identical to that for the outlink word.

4-5.6.6.1 Counter Address Generator. The counter address generator, figure 4-165, supplies the appropriate address for the counter priority cells to the write lines in the central processor. The address is represented by a combination of outputs CAD6 through CAD1 (low order to high order). These outputs connect the six low order write lines (6 through 1, see table 4-LXXX) to generate the proper counter addresses.

To generate an address, the generator outputs are logic ONE's in response to an address request signal. For example, address request signal C42A from the BMAGX cell generates address 0042 as follows:

CAD6	CAD5	CAD4	CAD3	CAD2	CAD1
C42A	-	-	-	C42A	-
1	0	0	0	1	0
	4			2	

As indicated, the proper output signals (CAD6 and CAD2) become logic ONE's in response to address request signal C42A. The remaining counter register addresses can be ascertained in this manner.

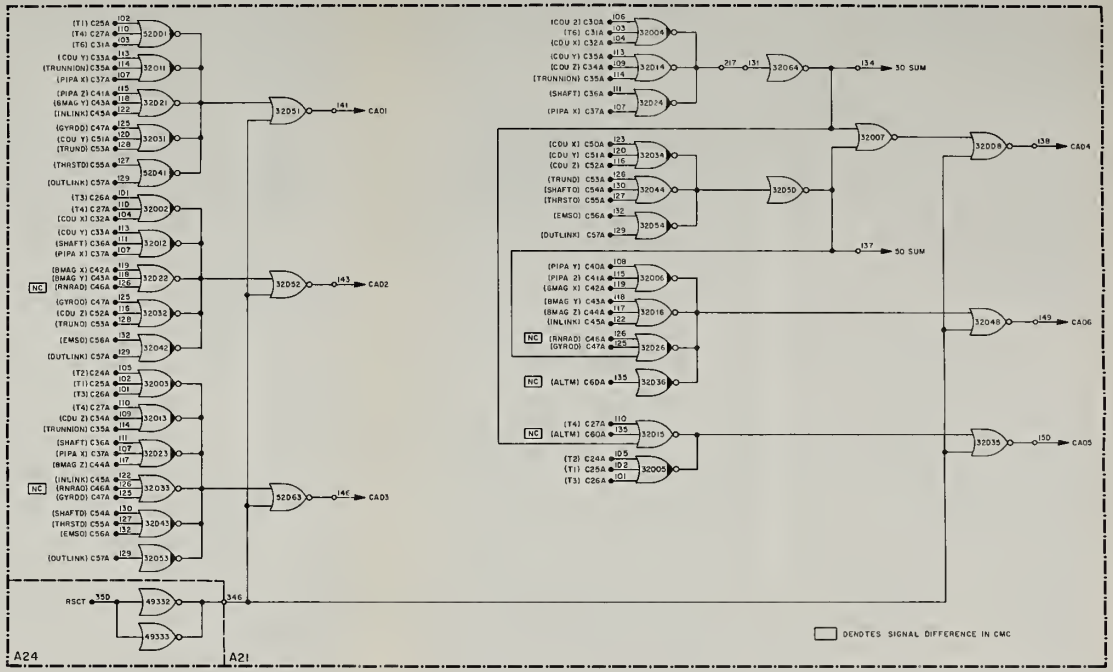


Figure 4-165. Counter Address Generator

The counter address is placed on the write lines by read signal $\overline{\text{RSCT}}$ at time 1 of the memory cycle time immediately following that cycle in which the request to increment is processed by the sequence generator. This is accomplished as follows.

An input to the input flip-flop of the counter priority cells is transferred to the secondary flip-flop at time 7 by transfer signal $\overline{\text{BKTF}}$. Simultaneously, signal CTROR is generated, and is used to produce increment signal INKL in the sequence generator. At time 12, following the completion of an instruction (counter increments are not executed between subinstructions), the sequence generator allows the counter increment to occur. At time 1 in the next memory cycle, read signal $\overline{\text{RSCT}}$ is generated as a function of increment signal INKL, and places the appropriate counter address on the write lines.

The outputs from gates 32064 (30 SUM) and 32050 (50 SUM) are essentially OR signals for any of counter cells 0030-0037 and 0050-0057, respectively. The OR signals generate the three high order bits of the address for the counters at these locations.

4-5.6.6.2 Counter Alarm Detector. The counter alarm detector, figure 4-166, supplies an alarm signal to the failure detection circuits in the power supply if counter increments occur too frequently (continuous counter incrementing) or if a counter increment fails to occur following an increment request.

Excessive counter incrementing is sensed by FF41149-41150. This flip-flop is reset by timing pulse F07A. The set output conditions one leg of gate 41151. This gate is strobed by timing pulse $\overline{\text{F07B}}$. If FF41149-41150 sets prior to $\overline{\text{F07B}}$, no alarm indication is generated. The set conditions are the $\overline{\text{T03}}$ timing pulse coincident with no counter increment activity, indicated by signals INKL and CTROR remaining at a logic ZERO level. If a counter increment request occurs within the test period, one or both of signals INKL or CTROR are a logic ONE. The flip-flop does not set and an alarm indication occurs.

Any request to increment is OR'ed through extended NOR gate 41134 and sets FF41138-41139. This conditions one leg of gate 41140. This flip-flop is reset (thus inhibiting gate 41140) by counter increment signal INKL. Therefore, if a counter increment request occurs (T1P, T2P etc.), and is not processed, signal INKL is not generated. Flip-flop 41141-41142 is set at time 9 and causes an alarm indication.

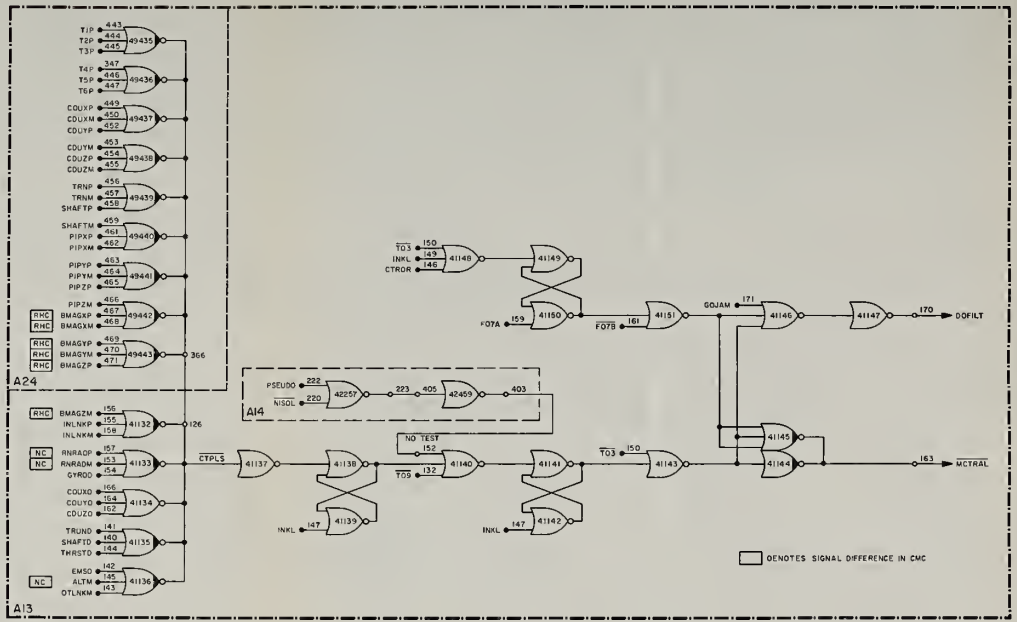


Figure 4-166. Counter Alarm Detector

4-5.7 INPUT-OUTPUT. The input-output section consists basically of the interface circuits and the input and output channels which transfer information between the computer and the other spacecraft subsystems. The interface differences in input/output between the LGC and the CMC are described in the following paragraphs.

4-5.7.1 Input-Output Functional Description. The interface circuits accept all inputs to and route all outputs from the computer. These circuits provide the necessary voltage levels or electrical isolation of the input and output signals. Incremental inputs as well as serial pulse inputs are applied to input transformer circuits. All discrete inputs such as the keycode from the DSKY are applied to resistive-capacitive networks. Serial pulse outputs and incremental output drive pulses such as those to the gyros and CDU's are applied to output transformer circuits. Timing and synchronization pulse trains to other spacecraft systems are also applied to output transformer circuits. Discrete outputs are applied to output transistor driver circuits. Power outputs (+28 COM, +4, and +14 volts) are supplied to isolation resistors located in the interface circuits. Most of the input signals to the computer are applied to the input channels; most of the output signals come from the output channel network. The remaining inputs and outputs are applied to or come from other functional areas within the computer.

There are six input channels and eight output channels which interface with other spacecraft systems and the DSKY. These channels are illustrated in figure 4-167 for the LGC, and figure 4-168 for the CMC. A ninth output channel (7) functions internally in the computer to access fixed memory. The channels are accessed by an address which is the same as the channel number (channel 30 - address 0030). Input channels 15 and 16 are flip-flop registers similar to the flip-flop registers of the central processor. Channels 30 through 33 each consist of an input gating complex to which discrete inputs are applied. The channels are interrogated under program control by a set of channel instructions. An address, supplied by program, is applied to the service gates of an associated channel and the data in that channel is read-out to the central processor. The numbers used to address both the input and output channels coincide with some of the numbers used as memory addresses. However, the addresses used for the input and output channels are supplied by the IN/OUT instruction group and are always channel addresses. The addresses in other instructions are always memory addresses. This coincidence of addresses can be used to access two registers in the central processor. Register L is accessible both at memory address 0001 and channel address 01; register Q is accessible at memory address 0002 and channel address 02. There is no write process involved with the input channels as is the case with the flip-flop registers of the central processor, however. Inputs are entered directly into the bit positions of the channels. The number of bits in parentheses in each channel block in figure 4-167 indicates the number of active bit positions. All channels have a capacity of 15 bits.

Only discrete inputs enter the input channels of both computers. These inputs are classified as interrupting and non-interrupting. The keyboard and mark inputs entered into channels 15 and 16 are the only two interrupting discrete type inputs.

For example, a keycode from the DSKY entered into channel 15 interrupts the program being executed and forces the computer to interrogate that particular channel. This is accomplished by an interrupt signal (KEYRUPT 1, KEYRUPT 2, or MKRPT) which is generated as the inputs are entered into channel 15 or 16. The inputs entered into the remaining channels from the various other spacecraft systems are non-interrupting. The channels are interrogated by program, as described previously, and the information is read-out to the central processor.

Incremental inputs representing velocity are applied directly from the interface circuits to the PIPA precount logic section. From this logic section, incremental pulses are applied to priority control to initiate a counter interrupt routine and update an associated counter in memory. In a similar manner, the incremental inputs representing the gimbal position of the ISS and OSS CDU's are applied directly to priority control and also initiate a counter interrupt routine.

In the LGC, channel 13 (figure 4-169) controls the serial inlink input to the computer, the downlink transmission, the RHC inputs (rotation hand controller), the rendezvous and landing radar inputs, and internal functions of the LGC.

In the CMC, channel 13 controls the serial inlink inputs, the downlink transmission, the BMAG inputs (body mounted attitude gyros) and internal functions of the CMC.

Information is entered into the respective bit positions of channel 13 from the central processor. Bits 1 through 4 in the LGC control outputs to the radar. These bit positions are not used in the CMC. Inlink consists of the uplink word from the spacecraft telemetry and the crosslink word from the other computer (LGC to CMC and CMC to LGC).

Normally, the uplink data is entered into the input circuits and subsequently to priority control to initiate a counter interrupt. A ONE entered into bit position 5 of channel 13 from the central processor inhibits uplink and enables the crosslink input between computers. Uplink information can also be inhibited by the BLOCK UPLINK signal from the PGNCS. Bit 6 of channel 13 inhibits any inlink (uplink or crosslink) information from entering the computer. Bit 7 controls the word order gate in the downlink logic, which is discussed under the output channel logic. The RHC inputs to the LGC and the BMAG inputs to the CMC are applied to priority control as a function of bit 8. A ONE entered into this bit position of channel 13 allows these incremental inputs to initiate a counter interrupt sequence in priority control and to update an associated counter in memory. Bits 10, 11, and 15/16 of channel 13 are control bits for internal functions of both computers. Bit 10 (alarms test) lights the RESTART and STBY lamps on the DSKY. Bit 11 enables the computer to enter the standby mode. Bit 15/16 enables the T6 interrupt routine. The manual inputs entered into channels 31 (attitude and translational) and 32 (impulse) initiate an interrupt sequence under program control through bits 12, 13, and 14 of channel 13. The manual discrete inputs are applied to the handrupt control logic. The program enters the proper data into positions 12, 13, and/or 14 and an interrupt sequence (HNDRPT) is initiated.

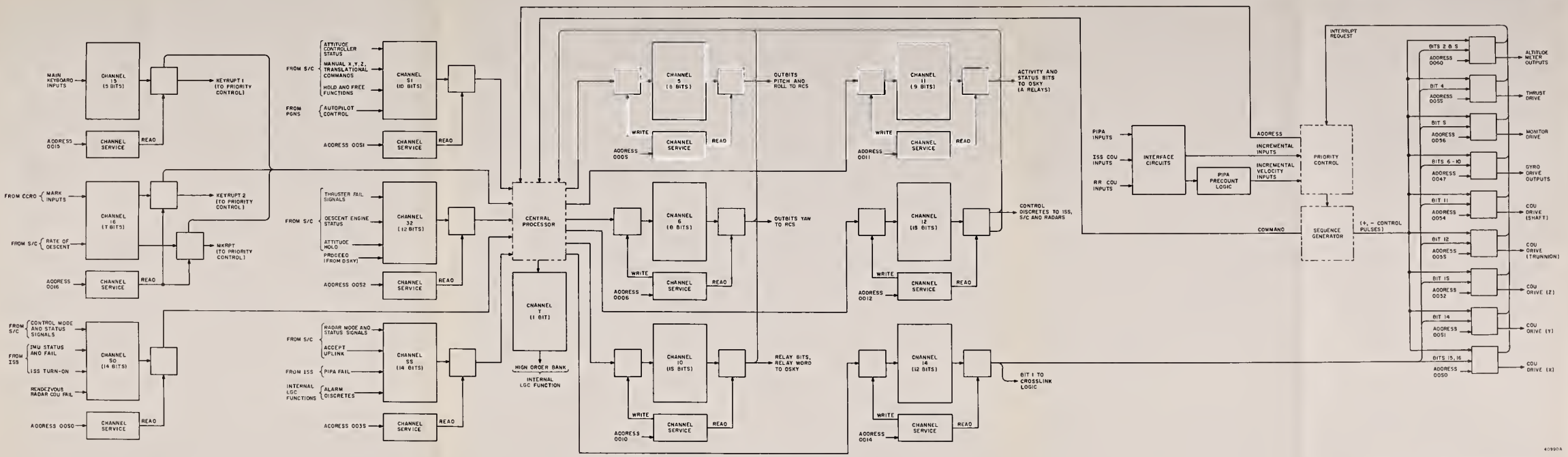


Figure 4-167. Input-Output Channels Functional Diagram-LGC

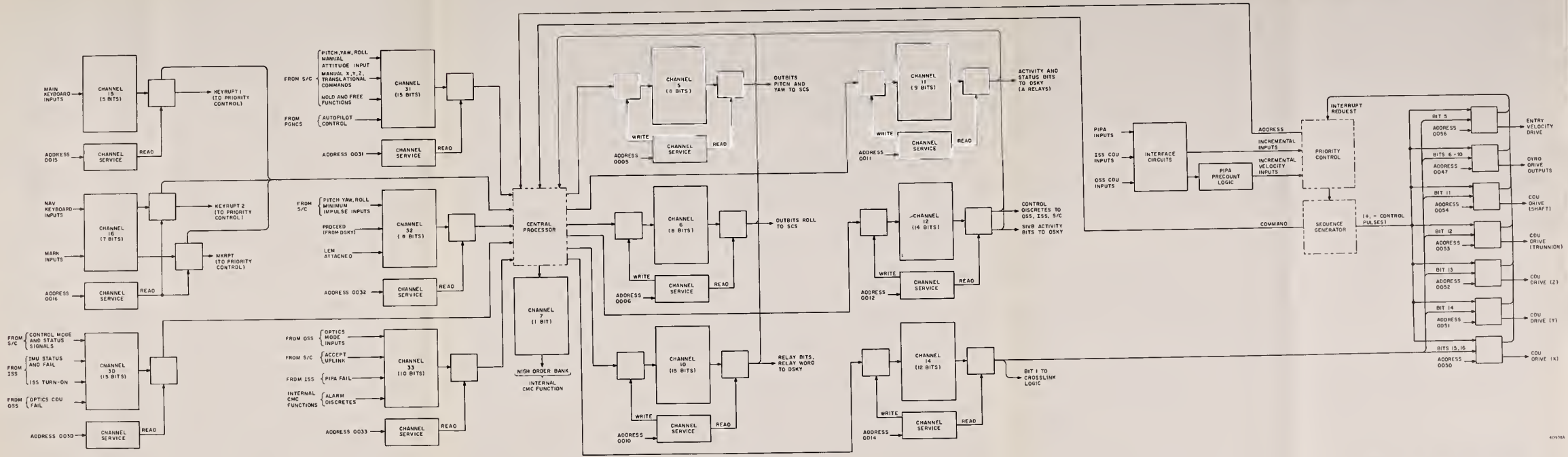


Figure 4-168. Input-Output Channels Functional Diagram - CMC

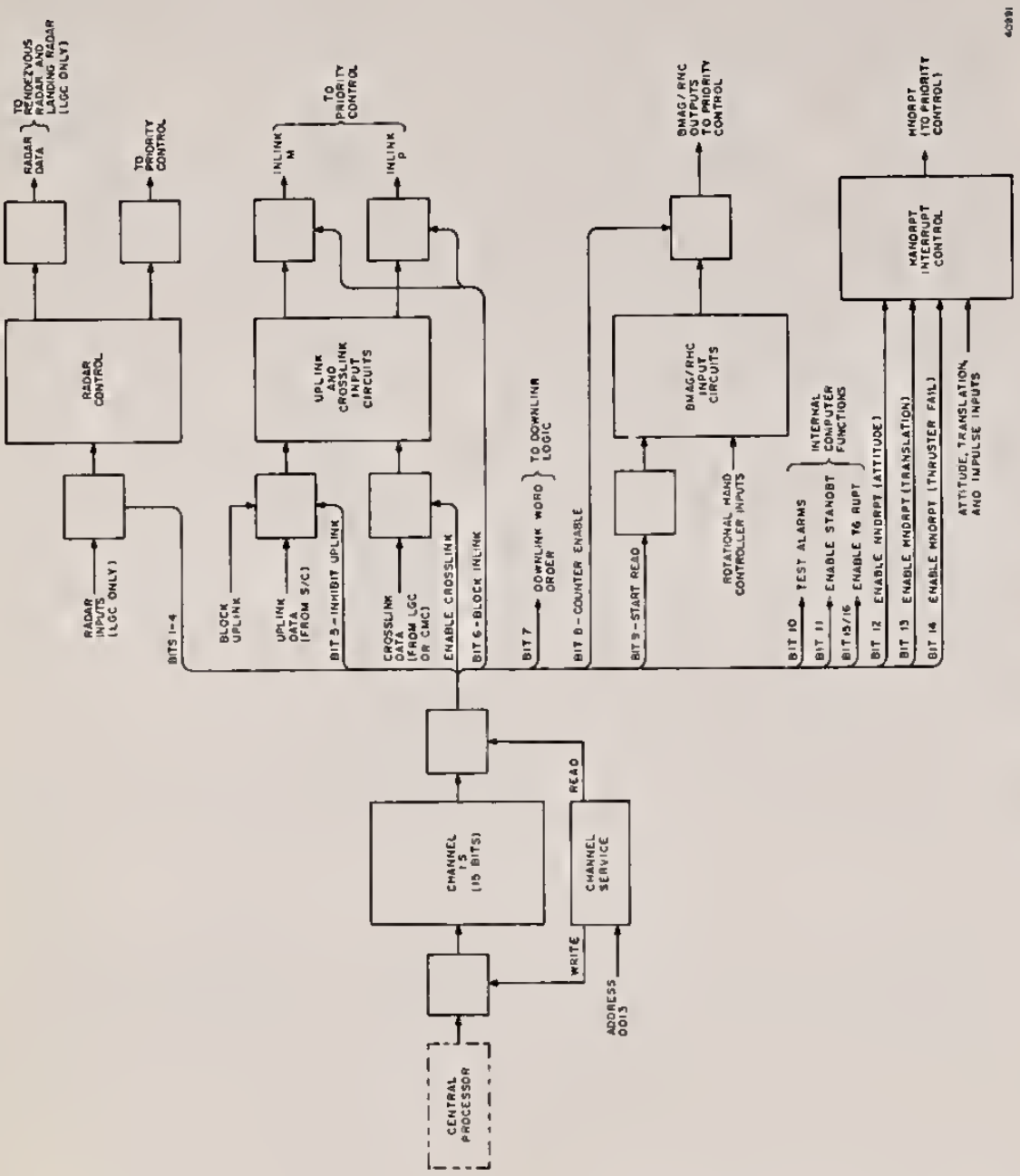


Figure 4-169. Inlink Functional Diagram

The output channels (figure 4-168) are all flip-flop registers with write and read service. Data is written into the output channels from the central processor coincident with an address supplied by program into the service gates. Output channels 5, 6, 10, 11, and 12 supply output discretes to other systems as indicated on figure 4-168.

Channel 14 controls the transmission of incremental drive pulses to the gyros, and CDU's in both the LGC/CMC, and, in addition, controls the altitude meter and thruster outputs in the LGC. An output is enabled by placing a ONE in the proper bit position of channel 14. This is accomplished by program. For example, the program enters a ONE into bit position 11 of channel 14. This results in an interrupt request signal which is applied to priority control. Further processing by priority control results in a command request to the sequence generator and an address command to the central processor. This same address (in this case 0054) enables the output drive logic and allows the drive pulses to be gated out. The associated output counter register in memory is loaded by program and a pulse burst to the CDU (shaft) occurs. Each time the counter is processed the number in the counter register is diminished by one so the content of the counter approaches zero. When the number has reached zero, the channel bit position is reset and the pulse burst terminates.

The outlink control logic is functionally illustrated in figure 4-170. Outlink consists of the downlink word to the spacecraft telemetry from the LGC/CMC, and the crosslink word between the LGC/CMC. The word to be transmitted downlink is loaded into channels 34 and 35 from the central processor. An interrupt sequence (DLKRPT) is initiated by the downlink rupt circuit. The downlink start signal (DKSTRT) is converted to a clear pulse to clear the downlink counter and also sets the read flip-flop. The bit sync pulses then step the counter. The outputs of the counter are decoded to strobe the bit positions of channels 34 and 35 and to produce a serial word output. The rate of transmission is monitored, and, if too fast, a bit is entered into bit position 12 of channel 33. Crosslink is the output word from the LGC to the CMC or vice-versa. Bit 1 of channel 14 enables the outlink control logic. An interrupt request signal is sent to priority control to initiate an interrupt sequence. The address of the crosslink counter enables the word entered from the central processor to be transmitted serially to the CMC or vice-versa.

4-5.7.2 Input-Output Service. Information is transferred into and out of the various input-output channels under the control of write, clear, and read signals generated by associated service gates (figure 4-171). Inputs to the service gates consist of write and read control pulses ($\overline{WCH}$ and $\overline{RCH}$) from the sequence generator and timing signals ($\overline{WT}$, $\overline{CT}$, and $\overline{RT}$) from the timer. The outputs of the write and clear service gates ($\overline{WCHG}$ and $\overline{CCHG}$) are supplied to the output channels to generate individual output channel write and clear signals. The output of the read service gate ($\overline{RCHG}$) causes information from the various input-output channels to be placed on the write lines at read time.

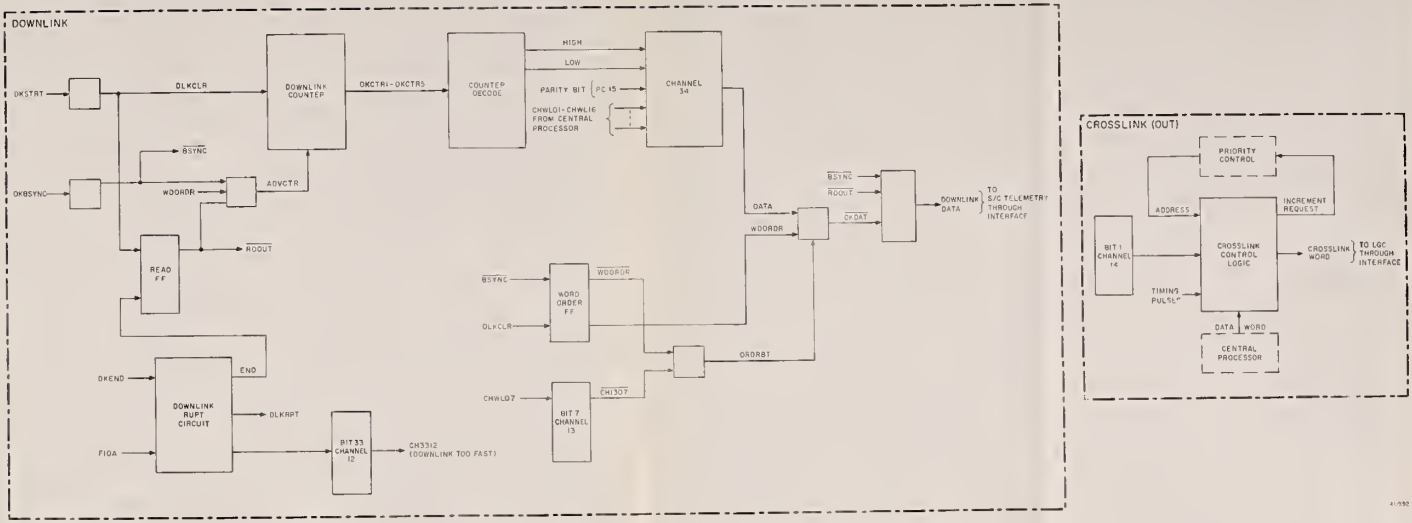


Figure 4-170. Outlink Functional Diagram

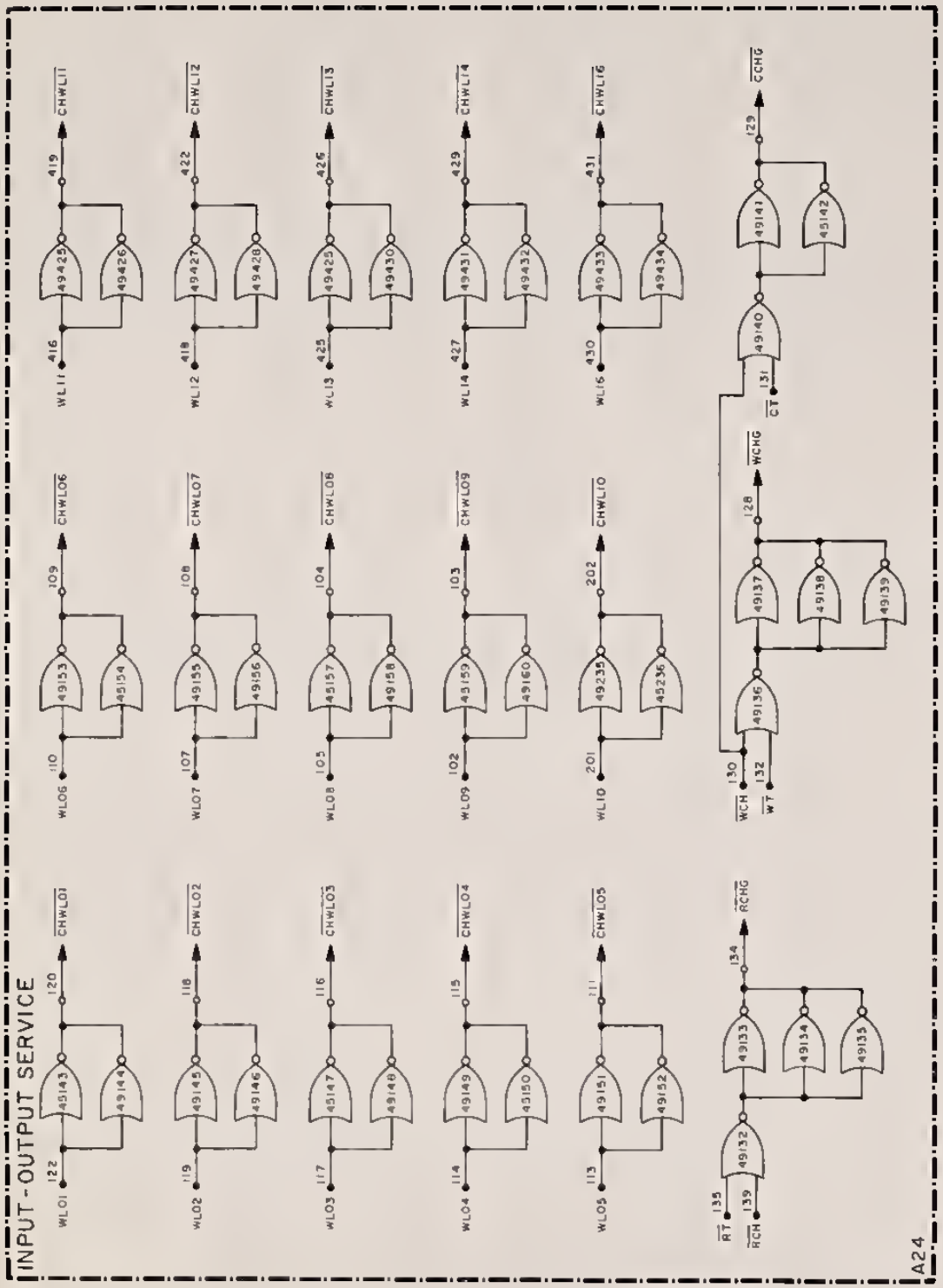


Figure 4-171. Input-Output Service

Data is supplied to the output channels from the write lines in the form of signals CHWL01-CHWL14 and CHWL16. The data is entered into a particular channel when that channel is addressed. All input-output data is ORed and is placed on the write lines and made available to the central processor as signals CH01-CH16 (figure 4-172.)

4-5.7.3 Input Channels 15 and 16. Input channels 15 and 16 (figure 4-173) receive discrete signals from the DSKY, Optical Subsystem (OSS), and spacecraft. Reception of these signals results in the generation of interrupt signals which are supplied to the priority control to interrupt the current computer operation and allow the inputs to be accepted and processed. Channel 15 in the LGC receives the five-bit keycode from the DSKY (MKEY1-MKEY5) whenever any key on the DSKY, except the STANDBY key, is depressed. In a similar manner, channel 16 receives discrete inputs from tbe OSS whenever any of the MARK pushbuttons are depressed or from the spacecraft whenever a manual command is generated to increase or decrease the LEM rate of descent. Since the logic associated with channels 15 and 16 is similar, only channel 15 and the differences between channels 15 and 16 are described in detail. Channel 15 in the CMC receives the five-bit keycode from the main DSKY. Channel 16 receives the five-bit keycode from the navigation DSKY and inputs from the OSS whenever any of the MARK buttons are depressed.

Initially, the channel 15 input flip-flops are reset and FF 45135-45136 is set. When a keycode is received, the MKEY1-MKEY5 signals that are logic ONE's set an associated input flip-flop. The flip-flop outputs are ORed through gates 45125 and 45126, and are used to set FF 45129-45130 subject to timing signal $\overline{\text{F09A}}$. Interrupt signal KYRPT1 is generated during T5 or T11 time subject to signal $\overline{\text{F09B}}$ as a result of setting the flip-flop. Signal KYRPT1 resets FF 45135-45136 to prevent the processing of additional keycodes until the current keycode has been processed. Signal KYRPT1 is also supplied to the priority control to interrupt computer operation and to cause the execution of interrupt routine KEYRUPT1. Routine KEYRUPT1 interrogates channel 15 by generating memory selection signals $\overline{\text{XT1}}$ and $\overline{\text{XB5}}$ (address 0015). This action causes the generation of read signal $\overline{\text{RCH15}}$ which places the keycode on the write lines, thus supplying the keyed in data to the central processor.

When the pressed DSKY key is released, signal MAINRS resets the input flip-flop and sets FF 45135-45136. Thus channel 15 is cleared and made ready to accept tbe next keycode input.

Channel 16 has a capacity of seven bits. However, only five are used in the LGC. The three discrete inputs MARK X, MARK Y, and REJ MRK cause routine KYRPT2 to be executed. The remaining two discrete inputs, PDESCT and MDESCT, cause routine MKRPT to be executed. This arrangement in channel 16 in the LGC differs from the CMC since there is only one DSKY in the LEM. Routine KYRPT2 is executed in the CMC as a function of the navigation DSKY keyboard inputs. Routine MKRPT is executed as a function of the Mark inputs MARK and MARKREJ. When the priority control receives either of these interrupt signals (KYRPT or MKRPT), computer operation is interrupted and interrupt routine KEYRUPT2 is executed which interrogates channel 16 and enables the data in the channel to be forwarded to the central processor.

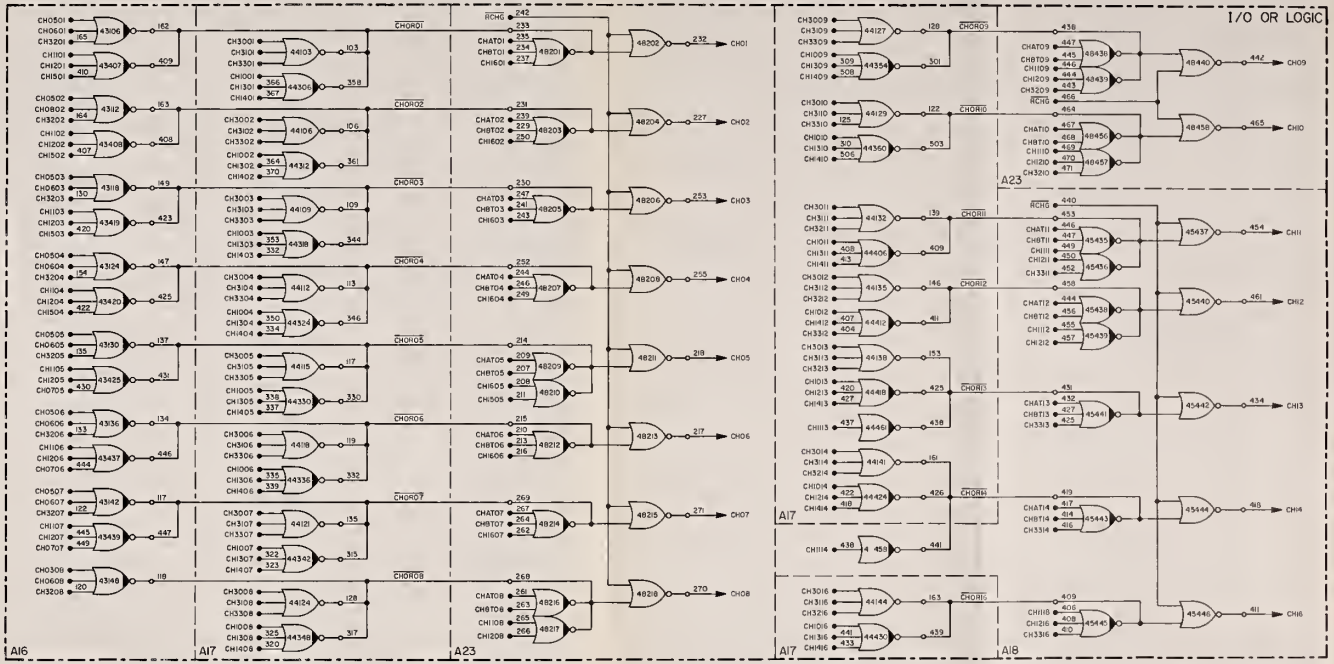


Figure 4-172. Input-Output OR Configuration

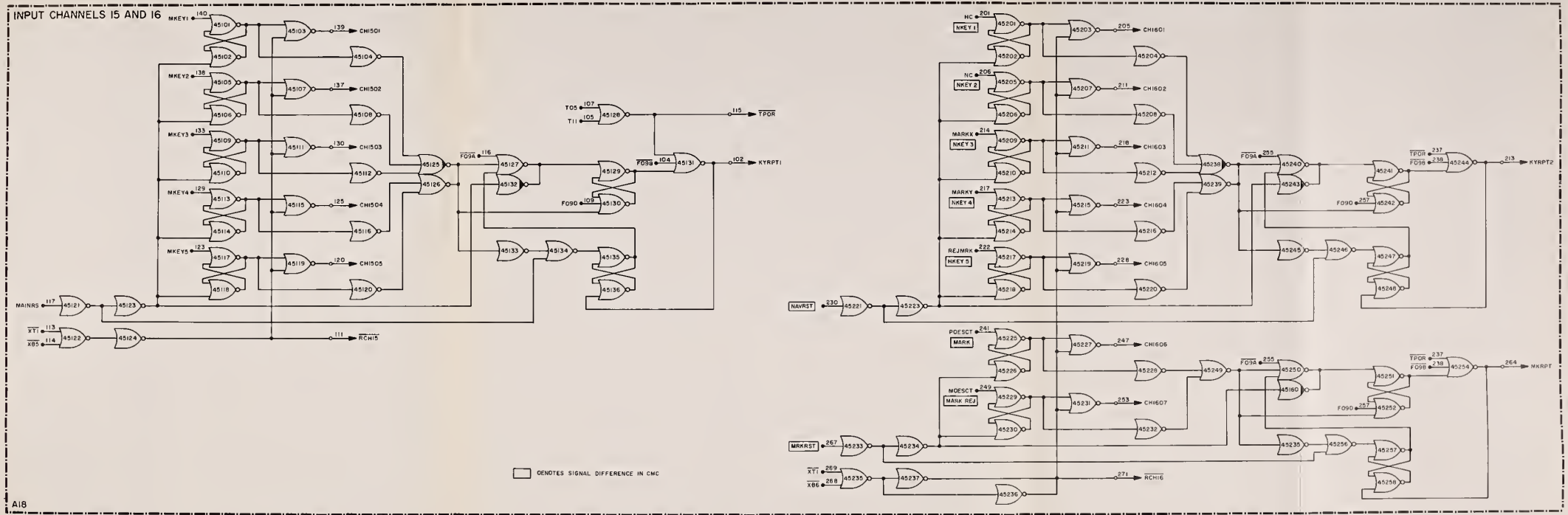


Figure 4-173. Input Channels 15 and 16

In the LGC, channel 16 is conditioned to accept new data when the input discretes are removed and signal MRKRST is received from the OSS or signal DESRST is received from the spacecraft. Channel 16 in the CMC is conditioned to accept new data when signal NAVRST from the navigation DSKY or MRKRST from the OSS is received.

4-5.7.4 Input Channels 30 through 33. Channels 30 through 33 (figure 4-174) consist of a series of gates which receive discrete inputs from the spacecraft and various subsystems of the PGNCS. Data is supplied directly to the gates and is placed on the write lines subject to read signals $\overline{\text{RCH30}}$, $\overline{\text{RCH31}}$, $\overline{\text{RCH32}}$, and $\overline{\text{RCH33}}$ whenever the individual channels are addressed. Each channel has a 15-bit capability; however, not all bit positions are used. Tables 4-LXXXII through 4-LXXXV list the various bit positions, the signal received by each and the description of the signals in the LGC. Tables 4-LXXXVI through 4-LXXXIX list the same information for the CMC.

4-5.7.5 PIPA Precount Logic. The PIPA precount logic (figure 4-175) consists of three forward-backward counters and a failure detection circuit.

When the PIPA's are experiencing no acceleration, each acceleration loop in the ISS continuously generates a series of three positive pulses followed by three negative pulses. The PIPA precount logic counters receive these pulses from the X, Y, and Z acceleration loops as signals PIPAX+ or PIPAX-, PIPAY+ or PIPAY-, and PIPAZ+ or PIPAZ-. The pulses are forwarded to the counters subject to timing signal PIPSAM, a 1 μsec pulse at 30 pps. Each counter counts forward three and then backward three without generating an output. Only when a counter receives more than three positive or negative pulses in a sequence does it generate an output. The output is dependent on the input. A plus output pulse (PIPXP, PIPYP, or PIPZP) is generated if the plus input pulses exceed three; a minus output pulse (PIPXM, PIPYM, or PIPZM) is generated if the minus input pulses exceed three. Using the counter for the Z axis PIPA as an example, table 4-XC illustrates the operation of the forward-backward counters. The left side of the table indicates the initial state of signals B and D and the input signal applied to the counter. The right side of the table indicates the state of signals B and D as a result of the input signal and it also indicates the presence or absence of an output signal.

The PIPA failure detection circuit generates signal PIPAFL if PIPA pulses are not received often enough, or if the time between the reception of a plus or minus PIPA pulse from one PIPA is too long, or if a plus and a minus PIPA pulse is received simultaneously from the same PIPA. Timing signal F5ASB2 causes the generation of signals MISSX, MISSY, and MISSZ every 312.5 μsec. If no inputs are received from the PIPA's prior to the reception of timing signal F5ASB0, FF 48107-48108 is set and signal PIPAFL is generated. Similarly, timing signal F18AX causes the generation of signals NO-P and NO-M every 2.6 seconds. If both a plus and a minus input is not received from each PIPA prior to the reception of timing signal F18B, signal PIPAFL is generated. The remaining failure condition occurs if plus and minus PIPA inputs are received simultaneously. When this condition exists, signal BOTHX, BOTHY, or BOTHZ is generated which causes signal PIPAFL to be generated.

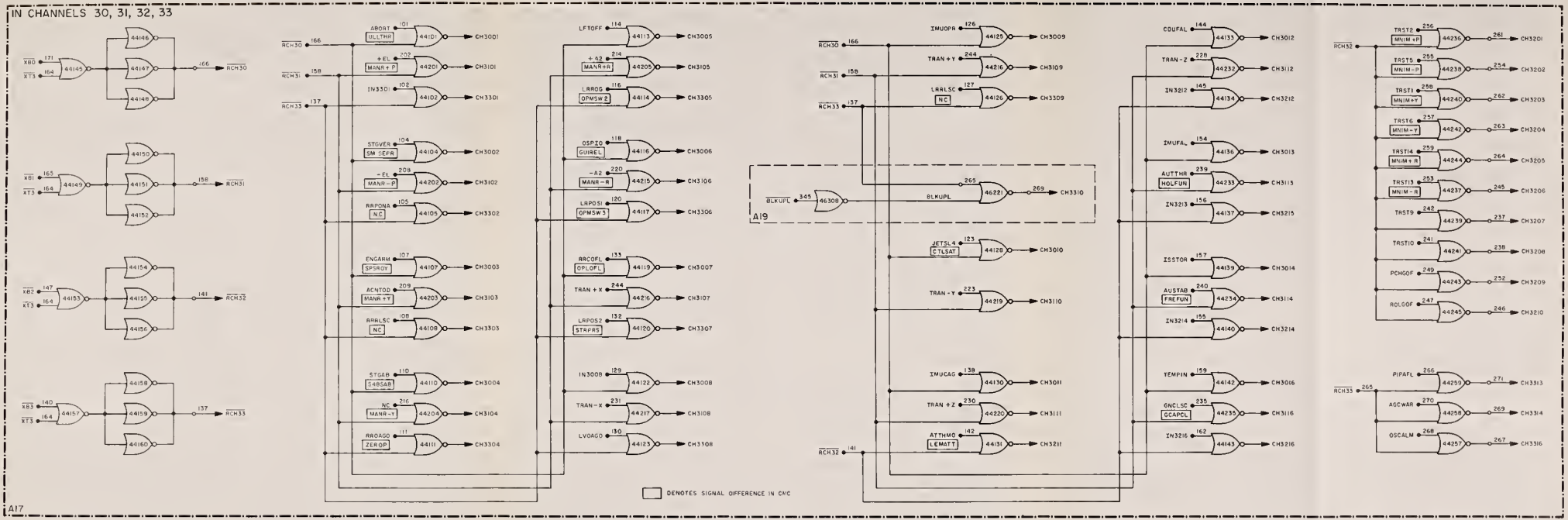


Figure 4-174. Input Channels 30, 31, 32, and 33

Tahle 4-LXXXII. Input Channel 30 - LGC

Bit	Signal	Description
1	ABORT	Indicates an ahort using the descent engine bas been manually initiated. The signal is generated by pressing tbe ABORT pushbutton on the PGNCS display and control panel.
2	STGVER (stage verify)	Indicates staging has successfully been completed. The signal is originated within the spacecraft hy explosive devices which accomplish separation.
3	ENGARM (engine armed)	Indicates that either tbe ascent or descent engine has heen armed. Tbe signal is initiated in tbe spacecraft at the PGNCS display and control panel.
4	STGAB (abort stage)	Indicates an ahort using the ascent engine has been manually initiated. Tbe signal is generated hy pressing the ABORT STAGE pushbutton on the PGNCS display and control panel.
5	LFTOFF (lift off)	Spare
6	DSPID (display inertial data)	Requests the LGC to supply forward and lateral velocity for display on the PGNCS Display and Control Panel.

(Sbeet 1 of 2)

Table 4-LXXXII. Input Channel 30 - LGC

Bit	Signal	Description
7	RRCDFL (rendezvous radar CDU fail)	Indicates a failure in one of the radar CDU's.
8	IN3008	Spare
9	IMUOPR (IMU operate)	Indicates the IMU is turned on and operating normally.
10	JETSL4 (four jet select)	Requests the LGC to use four reaction control jets while maneuvering the LEM.
11	IMUCAG (IMU cage)	Indicates that the IMU is in the cage mode.
12	CDUFAL (IMU CDU fail)	Indicates a failure in one of the inertial CDU's.
13	IMUFAL (IMU fail)	Indicates a failure in the IMU stabilization loops.
14	ISSTOR (ISS turn on request)	Indicates the ISS bas been energized or has been commanded to be energized.
15/16	TEMPIN (temperature in limits)	A logic ONE indicates the stable member temperature bas not exceeded its design limits. A logic ZERO indicates the limits have been exceeded.

(Sheet 2 of 2)

Table 4-LXXXIII. Input Channel 31 - LGC

Bit	Signal	Description
1	+EL	Spare
2	-EL	Spare
3	ACNTOD (attitude controller out of detent)	Indicates the attitude controller is not in the neutral position and requests the LGC to issue attitude change commands to the reaction control system (RCS).
4		Spare
5	+AZ	Spare
6	-AZ	Spare
7 thru 12	TRAN+X TRAN-X TRAN+Y TRAN-Y TRAN+Z TRAN-Z (X, Y, X translation commands)	Indicates translation controller commands about the X, Y, and Z axes which request the LGC to issue translation change commands to the RCS in accordance with the controller motion (bits 7 through 12).
13	AUTTHR (auto throttle)	Indicates the descent engine is in the automatic throttling mode under LGC control.

(Sheet 1 of 2)

Table 4-LXXXIII. Input Channel 31 - LGC

Bit	Signal	Description
14	AUSTAB (auto stabilization)	Indicates the automatic stabilization mode has been selected.
15/ 16	GNCLSC (G/N control of S/C)	Indicates the PGNCS mode has been selected to control the spacecraft.

(Sheet 2 of 2)

Table 4-LXXXIV. Input Channel 32 - LGC

Bit	Signal	Description
1	TRST2 (thruster 2 & 4 fail)	Indicates thruster pair failure which causes LGC to cease commanding these jets and to compensate for their loss (bits 1 through 8).
2	TRST5 (thruster 5 & 8 fail)	
3	TRST1 (thruster 1 & 3 fail)	
4	TRST6 (thruster 6 & 7 fail)	
5	TRST14 (thruster 14 & 16 fail)	
6	TRST13 (thruster 13 & 15 fail)	
7	TRST9 (thruster 9 & 12 fail)	
8	TRST10 (thruster 10 & I1 fail)	
9	PCHGOF (pitch gimbal off)	Indicates the descent engine pitch gimbal is off null.
10	ROLGOF (roll gimbal off)	Indicates the descent engine roll gimbal is off null.
11	ATTHMD (attitude hold mode)	Indicates the attitude hold mode has been selected.

(Sheet I of 2)

Table 4-LXXXIV. Input Channel 32 - LGC

Bit	Signal	Description
12	IN3212	Spare
13	IN3213	Spare
14	IN3214	Proceed - using PRO pushbutton on DSKY, astronaut can allow program to proceed without data in lieu of entering VERB 33.
15/16	IN3216	Spare

(Sheet 2 of 2)

Table 4-LXXXV. Input Channel 33 - LGC

Bit	Signal	Description
1	IN3301	Spare
2	RRPONA (RR power on/auto)	Indicates the rendezvous radar (RR) power is on and the radar is operating in the automatic mode.
3	RRRLSC (RR range low scale)	Indicates the rendezvous radar scale factor is on low scale. The signal is generated automatically hy the radar at a range of approximately 50 nautical miles.
4 5	RRDAGD (RR data good) LRRDG (LR range data good)	Indicates the RR and LR range trackers have locked on (bits 4 and 5).
6 7	LRPOS1 LRPOS2 (LR position 1 and 2)	Indicates the position of tbe landing radar antenna (bits 6 and 7).
8	LVDAG (landing velocity data good)	Indicates the LR velocity trackers have locked on.
9	LRRLSC (LR range low scale)	Indicates the landing radar scale factor is on low scale. The signal is generated automatically by the radar at a range of approximately 2,500 feet.

(Sheet 1 of 2)

Table 4-LXXXV. Input Channel 33 - LGC

Bit	Signal	Description
10	BLKUPL (block uplink)	Indicates the reception of uplink data has been inhihited.
11	Logic ONE	Indicates the uplink telemetry rate is too fast. This bit position is used in conjunction with the uplink and crosslink input circuits in output channel 13.
12	Logic ONE	Indicates the downlink telemetry rate is too fast. This hit position is used in conjunction with the downlink converter.
13	PIPAFL (PIPA fail)	Indicates a PIPA failure. The failure is detected hy the PIPA precount logic.
14	AGCWAR (AGC warning)	Indicates one of the following internal computer conditions: 1. computer restart 2. counter failure 3. voltage failure 4. alarm test 5. scaler alarm
15/ 16	OSCALM (oscillator alarm)	Indicates the oscillator in the timer has failed.

(Sheet 2 of 2)

Table 4-LXXXVI. Input Channel 30 - CMC

Bit	Signal	Description
1	ULL THR (ullage thrust)	(Indicates the SIVB is performing a ullage maneuver or that the SIVB tanks are being vented.
2	SMSEPR (service module separation)	Indicates the service module has separated from the command module.
3	SPSRDY (service propulsion system ready)	Indicates the SPS engine start checklist has been completed and the SPS is ready for thrusting. The signal is initiated in the spacecraft at the PGNCS display and control panel.
4	S4BSAB (SIVB separation)	Indicates the SIVB has separated from the service module.
5	LFTOFF (lift off)	Spare
6	GUIREL (guidance reference release)	Indicates that gyro-compassing can he discontinued and the stable member can he inertially referenced.
7	OPCDFL (optics CDU fail)	Indicates a failure has occurred in one of the optics CDU's.
8	IN 3008	Spare
9	IMUOPR (IMU operate)	Indicates the IMU is turned on and operating normally.

(Sheet 1 of 2)

Table 4-LXXXVI. Input Channel 30 - CMC

Bit	Signal	Description
10	CTLSAT (Saturn control)	Indicates a request for the CMC to control the Saturn instrumentation unit. The signal is generated by a switch setting on the PGNCS display and control panel.
11	IMUCAG (IMU cage)	Indicates that the IMU is in the cage mode.
12	CDUFAL (IMU CDU fail)	Indicates a failure has occurred in one of the inertial CDU's.
13	IMUFAL (IMU fail)	Indicates a failure bas occurred in the IMU stabilization loops.
14	ISSTOR (ISS turn on request)	Indicates tbe ISS bas been energized or has heen commanded to he energized.
15/ 16	TEMPIN (temperature in limits)	A logic one indicates the stable memher temperature has not exceeded its design limits. A logic zero indicates the limits have been exceeded.

(Sbeet 2 of 2)

Table 4-LXXXVII. Input Channel 31 - CMC

Bit	Signal	Description
1 thru 6	MANR+P MANR-P MANR+Y MANR-Y MANR+R MANR-R (manual pitch, yaw, and roll rotational commands)	Indicates rotational controller commands for pitch, yaw, and roll which request the CMC to issue rotational change commands to the RCS in accordance with the controller motion.
7 thru 12	TRAN+X TRAN-X TRAN+Y TRAN-Y TRAN+Z TRAN-Z (X, Y, Z translation commands)	Indicates translation controller commands about the X, Y, and Z axes which request the CMC to issue translation change commands to the RCS in accordance with the controller motion.
13	HOLFUN (hold function)	Indicates the CMC is set in an attitude hold mode in which the computer maintains the attitude selected by the rotational hand controller.
14	FREFUN (free function)	Indicates the CMC has no control over the attitude of the spacecraft.
15/ 16	GCAPCL (guidance control, auto pilot control)	Indicates the PGNCS mode has been selected.

Table 4-LXXXVIII. Input Channel 32 - CMC

Bit	Signal	Description
1 thru 6	MNIM+P MNIM-P MNIM+Y MNIM-Y MNIM+R MNIM-R (minimum impulse pitch, yaw and roll)	Indicates minimum impulse commands for pitch, yaw, and roll which request the CMC to issue commands to position the spacecraft during navigation or IMU alignment sighting with the OSS.
7	TRST9	Spare
8	TRST10	Spare
9	PCHGOF (pitch gimbal off)	Spare
10	ROLGOF (roll gimbal off)	Spare
11	LEMATT (LEM attached)	Indicates the LEM is attached to the CM.
12	IN3212	Spare
13	IN3213	Spare
14	IN3214	Proceed - using PRO pushbutton on DSKY, astronaut can allow program to proceed without data in lieu of entering VERB 33.
15/16	IN3216	Spare

Table 4-LXXXVIX. Input Channel 33 - CMC

Bit	Signal	Description
1	IN 3001	Spare
2	RRPONA (RR power on/auto)	Spare
3	RRRLSC (RR range low scale)	Spare
4	ZEROP (zero optics)	Indicates a request for the zero optics has been made in which the CMC zeroes the optics angle counters.
5	OPMSW2 (optics mode switch 2)	Indicates the optics mode switch is in position 2.
6	OPMSW3 (optics mode switch 3)	Indicates the optics mode switch is in position 3.
7	STRPRS (star present)	Indicates the presence of a star in the tracker field of view.
8	LVDAG (landing velocity data good)	Spare
9	LRRLSC (LR range low scale)	Spare
10	$\overline{\text{BLKUPL}}$ (block uplink)	Indicates the reception of uplink data has been inhibited.

(Sheet 1 of 2)

Table 4-LXXXVIX. Input Channel 33 - CMC

Bit	Signal	Description
11		Indicates the uplink telemetry rate is too fast. This hit position is used in conjunction with the uplink and crosslink input circuits in output channel 13.
12		Indicates the downlink telemetry rate is too fast. This bit position is used in conjunction with the downlink converter.
13	PIPAFL (PIPA fail)	Indicates a PIPA failure has been detected by the PIPA precount logic. This detection is an internal CMC function.
14	AGCWAR (AGC warning)	Indicates one of the following internal computer conditions: 1. computer restart 2. counter failure 3. voltage failure 4. alarm test 5. scaler alarm
15/16	OSCALM (oscillator alarm)	Indicates the oscillator in the timer has failed. This is an internal CMC function.

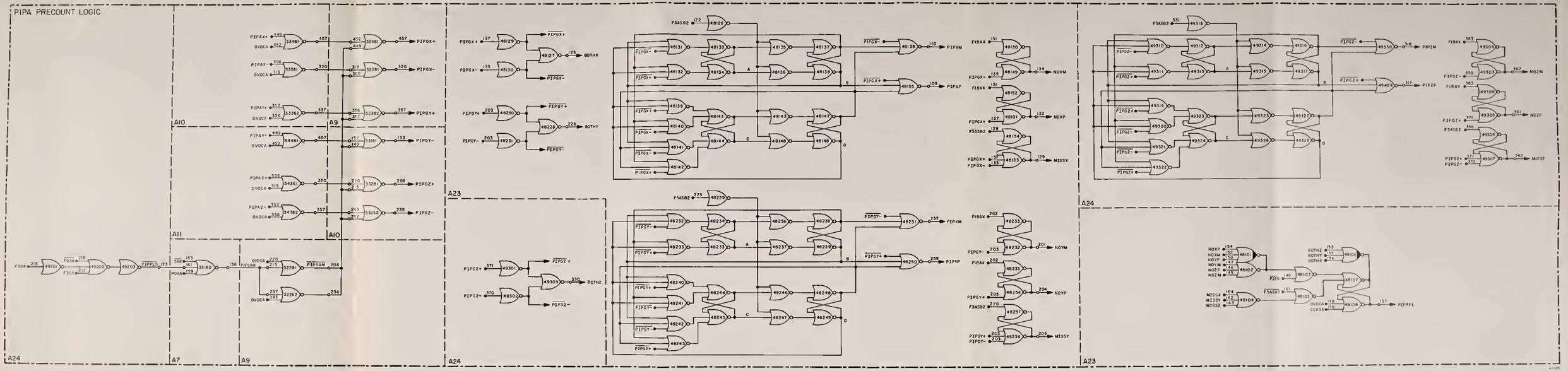


Figure 4-175. PIPA Precount Logic

Table 4-XC. Truth Table for Z Axis PIPA Counter

Signal B	Signal D	Input Signal	Signal B	Signal D	Output Signal
1	1	PIPGZ+	1	0	—
1	0	PIPGZ+	0	0	—
0	0	PIPGZ+	0	1	—
0	1	PIPGZ+	0	1	PIPZP
0	1	PIPGZ-	0	0	—
0	0	PIPGZ-	1	0	—
1	0	PIPGZ-	1	1	—
1	1	PIPGZ-	1	1	PIPZM

4-5.7.6 Output Channels 05 and 06. Channels 05 and 06 in the LGC (figure 4-176) control the reaction control system (RCS) to provide maneuvering commands for the spacecraft. Maneuver requests are received by the LGC through input channel 31 and are converted to maneuver commands by program action. The commands are written into channels 05 and 06 and forwarded to the RCS when the channels are addressed. Data is processed in these channels and all other output channels similarly to that of a register in the central processor, namely, clear, write, and read. In the event of a GOJAM condition, all data in channels 05 and 06 is cleared in preparation for a computer restart. Table 4-XCI contains a list of the RCS control signals supplied by channel 05 in the LGC.

Channels 05 and 06 in the CMC control the RCS in the command module (see figure 4-176). The RCS can be operated in either the SM mode or the CM mode depending upon the switch setting on the display and control panel. With the SM mode selected, all 16 bits contained in the two channels (eight bits per channel) are used to control 16 thrusters in the SM. With th CM mode selected, only 12 bits are used to control the 12 thrusters on the CM. Bits 5 through 8 of channel 06 are not used in the CM mode. The signals generated by channels 05 and 06 for the two modes are listed in table 4-XCI.

4-5.7.7 Output Channels 10 and 11. The output signals from Channels 10 and 11 (figures 4-177 and 4-178) activate relays in the DSKY which causes various numerical displays and status and caution indications. All 15 bit positions of channel 10 are used simultaneously to control a relay matrix in the DSKY. Bit positions 12 through 15/16 generate signals RYWD12 through RYWD14 and RYWD16 which select the proper row in the matrix to be activated. Bit positions 1 through 11 generate signals RLYB01 through RYLB11 which activate relays in the selected row. Thus, any relay in the matrix can be activated subject to the contents of channel 10.

Seven bits from channel 11 (bits 1 through 7) are used to provide specific indications to the DSKY. The data in these bit positions is identical for both the LGC and the

Table 4-XCI. RCS Control Signals - LGC and CMC

Channel	Bit Position	Output Signal LGC	Output Signal - CMC	
			SM Mode	CM Mode
05	1	-X/-P/+R	RC+X+P	+PCH/-X/+YAW
	2	+X/+P/-R	RC-X-P	-PCH/+Z
	3	-X/+R/+P	RC-X+P	+PCH/-X/-YAW
	4	+X/-R/-P	RC+X-P	-PCH/-Z
	5	-X/+P/-R	RC+X+Y	+YAW/-X/+PCH
	6	+X/-P/+R	RC-X-Y	-YAW/-X/-PCH
	7	-X/-R/-P	RC-X+Y	+YAW/-X/-PCH
	8	+X/+R/+P	RC+X-Y	-YAW/-X/+PCH
06	1	+Z/+YAW	RC+Z+R	+RLL/(+Y, +Z)
	2	-Z/-YAW	RC-Z-R	-RLL/(-Y, -Z)
	3	-Z/+YAW	RC-Z+R	+RLL/(+Y, -Z)
	4	+Z/-YAW	RC+Z-R	-RLL/(-Y, +Z)
	5	+Y/+YAW	RC+Y+R	Not used
	6	-Y/-YAW	RC-Y-R	Not used
	7	-Y/+YAW	RC-Y+R	Not used
	8	+Y/-YAW	RC+Y-R	Not used

CMC. Each bit position generates a signal which activates a relay in the DSKY and causes an indicator to light. In addition, bit positions 5, 6, and 7 receive signal FLASH from the timer which interrupts the generation of the relay activating signals they produce, thus causing the indicators they control to flash. Table 4-XCII lists all of the bit positions for channel 11, the signals generated, and the function of each signal for both the LGC and CMC. Signal OUTCOM which is generated by bit position 9 is used for test purposes. Signal W1110, which is generated by bit position 10, is used to inhibit the generation of signal RESTRT, thereby turning on indicator RESTART on the DSKY and turning off several caution indicators in the spacecraft. Note that bits 13 and 14 are used in the LGC only.

4-5.7.8 Output Channel 12. Channel 12 (figure 4-179) provides signals which control various spacecraft and PGNCS systems. The channel consists of 15 bit positions. Table 4-XCIII for the LGC and 4-XCIV for the CMC list the bit positions, the signals generated, and the function of each signal.

4-5.7.9 Output Channel 13. Channel 13 produces signals which are used to perform various internal functions and which are common in both the LGC and the CMC. Additional logic circuits in the LGC control the rendezvous and landing radars and are not contained in the CMC. Common logic functions are described in the same paragraph in the sections to follow. Specific logic circuits peculiar only to the LGC are described separately.

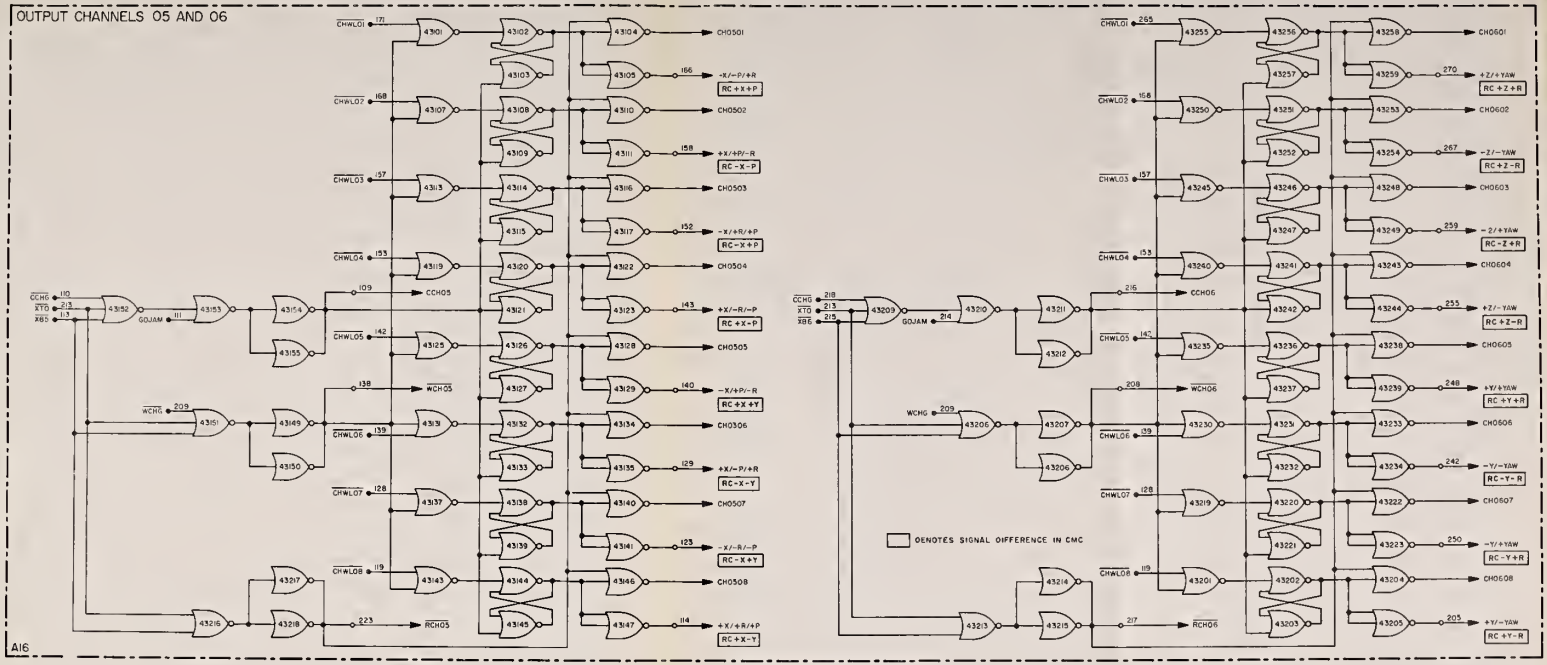


Figure 4-176. Output Channels 05 and 06

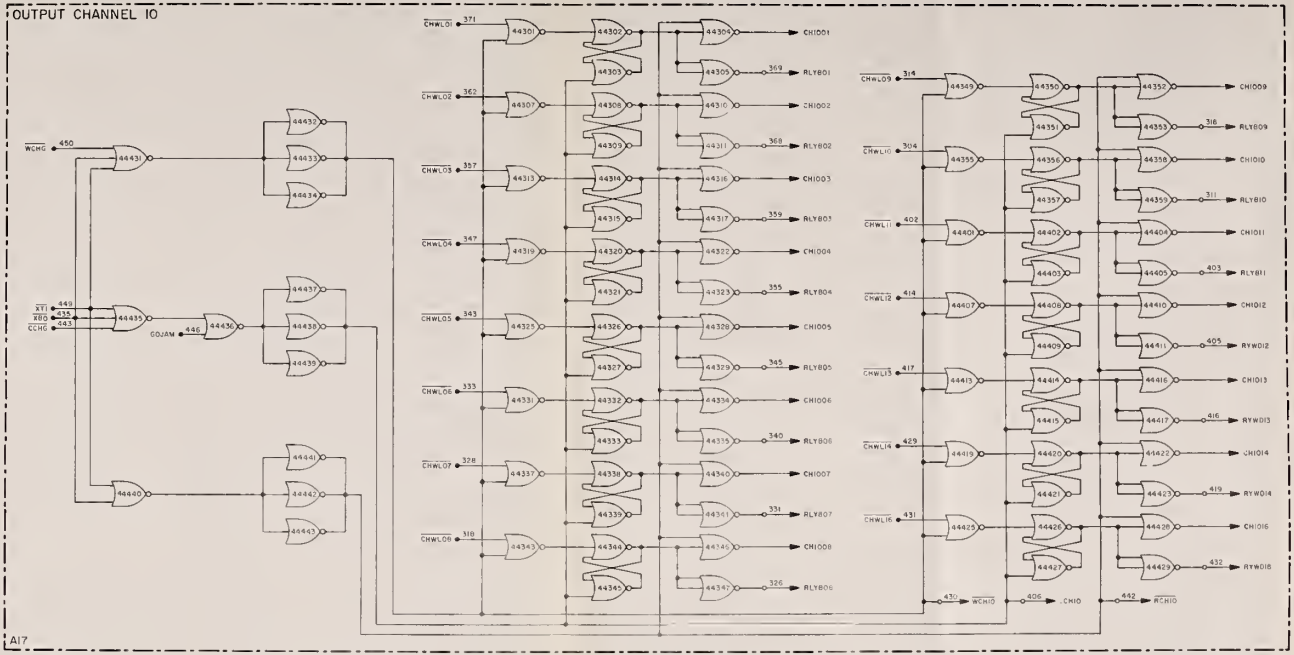


Figure 4-177. Output Channel 10

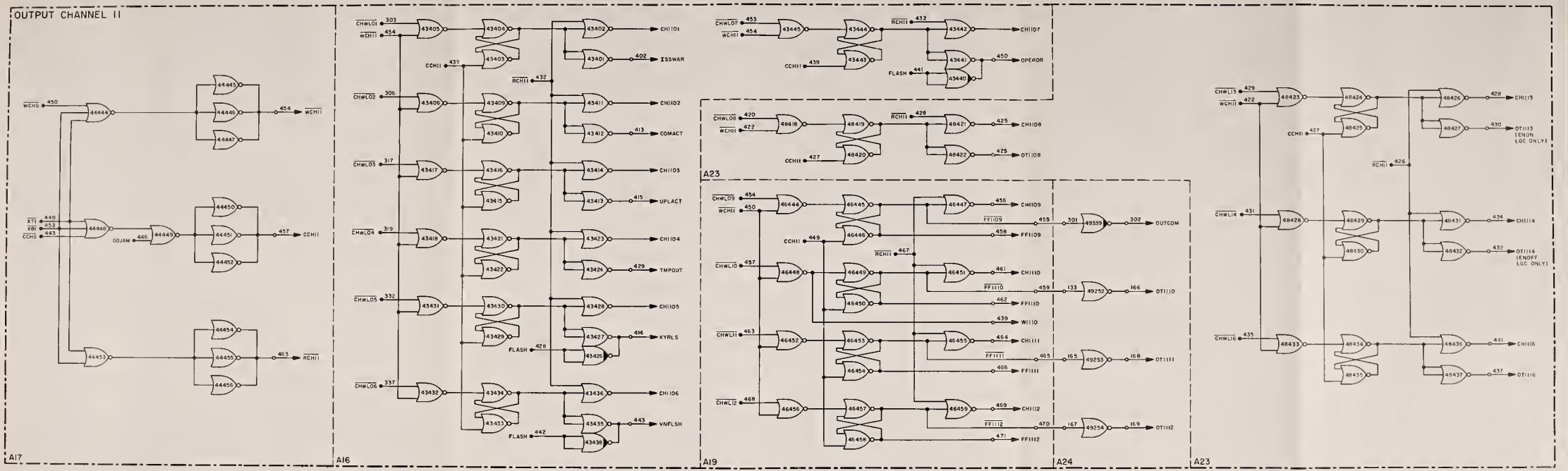


Figure 4-178. Output Channel 11

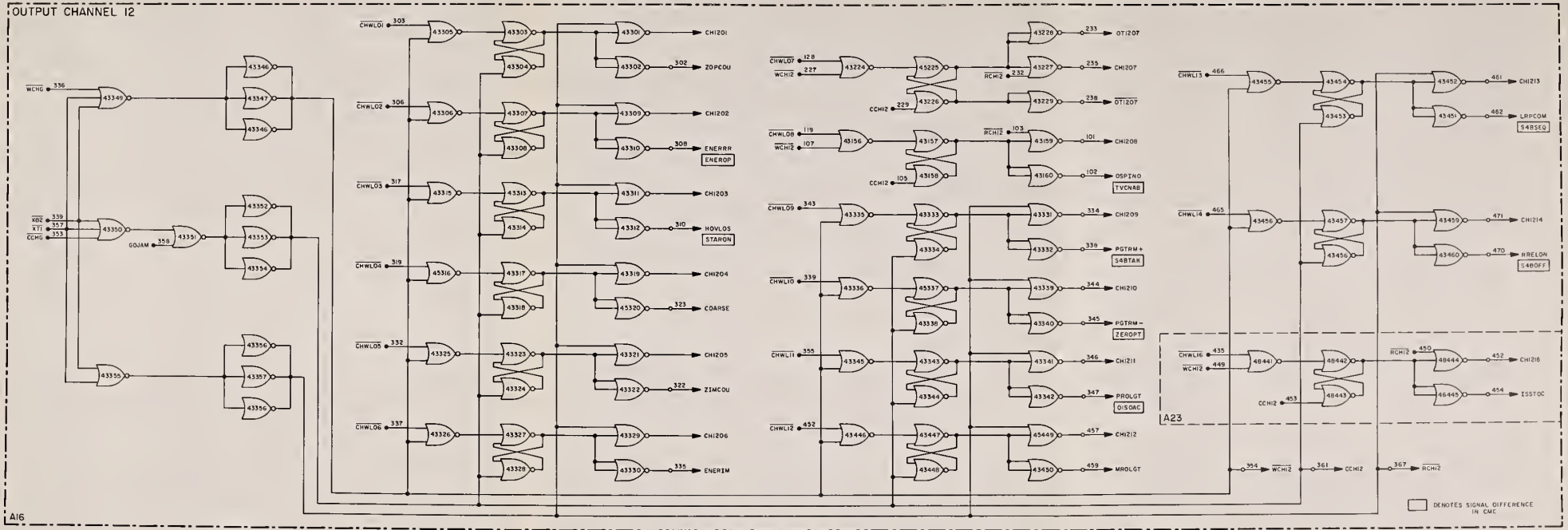


Figure 4-179. Output Channel 12

Table 4-XCII. Channel 11 Output Signals

Bit Position	Output Signal	Function
1	ISSWAR (ISS warning)	Indicates an abnormal condition exists in the ISS.
2	COMACT (computer activity)	Indicates the computer is not in the standby mode and is processing some routine other than the dummy job.
3	UPLACT (uplink activity)	Indicates the computer is receiving uplink information.
4	TMPOUT (temperature out)	Indicates the stable member temperature bas exceeded its design limits.
5	KYRLS (key release)	Indicates routine pinball, tbe keyboard and display routine, has attempted to use the DSKY to display information but found it busy.
6	VNFLSH (verb/noun flash)	Causes the verb and noun indicators to flash which indicates additional information must be keyed in before the computer can perform the requested operation.
7	OPEROR (operator error)	Indicates the operator performed some illegal operation using the keyboard.
8	-	Spare
9	OUTCOM	Test
10	OT1110	Spare
11	-	Spare
12	-	Spare
13 (LGC only)	OT1113 (engine on)	Indicates the ascent or descent engine is on.
14 (LGC only)	OT1114 (engine off)	Indicates the ascent or descent engine is off.

Table 4-XCIII. Channel 12 Output Signals - LGC

Bit Position	Output Signal	Function
1	ZOPCDU (zero optics CDU)	Clears the optics CDU shaft and trunnion read counters and inhibits the transmission of error angle pulses to the LGC.
2	ENERRR (energize rendezvous radar)	Requests that the rendezvous radar be energized.
3	HOVLOS (horizontal velocity low scale)	Spare
4	COARSE (coarse align enable)	Indicates a request for the coarse align mode.
5	ZIMCDU (zero IMU CDU's)	Clears the IMU read counters and inhibits the transmission of gimbal angle error pulses to the LGC.
6	ENERIM (enable IMU error counter)	Enables the IMU error counters and allows them to accept LGC drive pulses.
7	OT1207	Spare
8	DSPIND (display inserted data)	Requests the display-inertial-data mode for display of inertially-derived forward and lateral velocity on PGNCS Display and Control Panel.
9	PGTRM+ (plus pitch gimbal trim)	Commands plus and minus pitch and roll gimbal trim with bit positions 10, 11, and 12.
10	PGTRM- (minus pitch gimbal trim)	Same as bit position 9.

(Sheet 1 of 2)

Table 4-XCIII. Channel 12 Output Signals - LGC

Bit Position	Output Signal	Function
11	PROLGT (plus roll gimbal trim)	Same as bit position 9.
12	MROLGT (minus roll gimbal trim)	Same as bit position 9.
13	LRPCOM (landing radar position command)	Commands the positioning of the landing radar to one of two possible positions.
14	RRELON (rendezvous radar enable lock-on)	Commands a radar lock-on if tbe automatic lock-on is not achieved.
15/ 16	ISSTDC (ISS turn on delay completed)	Indicates tbe gyro wheels bave had time to run up to speed.

(Sheet 2 of 2)

Table 4-XCIV. Channel 12 Output Signals - CMC

Bit Position	Output Signal	Function
1	ZOPCDU (zero optics CDU)	Clears the optics CDU sbaft and trunnion read counters and inhibits tbe transmission of error angle pulses to tbe CMC.
2	ENEROP (enable optics error counter)	Enables the optics CDU sbaft and trunnion error counters to accept CMC drive pulses.
3	STARON (star tracker on)	Indicates a request for tbe optics star tracker mode.

(Sheet 1 of 2)

Table 4-XCIV. Channel 12 Output Signals - CMC

Bit Position	Output Signal	Function
4	COARSE (coarse align enable)	Indicates a request for the coarse align mode.
5	ZIMCDU (zero IMU CDU's)	Clears the IMU read counters and inhibits the transmission of gimbal angle error pulses to the CMC.
6	ENERIM (enable IMU error counter)	Enables the IMU error counters to accept CMC drive pulses.
7	OT1207	Spare
8	TVCNAB (thrust vector control enable)	Indicates a request for the thrust vector control mode in which the CMC controls the SPS.
9	S4BTAK (SIVB takeover)	Indicates the CMC has been selected to control the SIVB guidance.
10	ZEROPT (zero optics)	Indicates a request for the zero optics mode.
11	DISDAC (disengage optics DAC)	Prevents the optics DAC's from processing error signals.
12	-	Spare
13	S4BSEQ (SIVB start sequence)	Enables the SIVB start injection sequence.
14	S4BOFF (SIV engine cutoff)	Cuts off the SIVB engines.
15/ 16	ISSTDC (ISS turn on delay completed)	Indicates the gyro wheels have had time to run up to speed.

(Sheet 2 of 2)

4-5.7.9.1 Channel 13 Service. Read and write service for all bit positions of channel 13 in both the LGC and CMC is illustrated in figure 4-180. The write and read signals are generated as a function of a write or read control pulse, respectively, and address 0013 ($\overline{XT1}$,$\overline{XB3}$). The channel is cleared coincident with write-in (CCH13) or whenever signal GOJAM occurs.

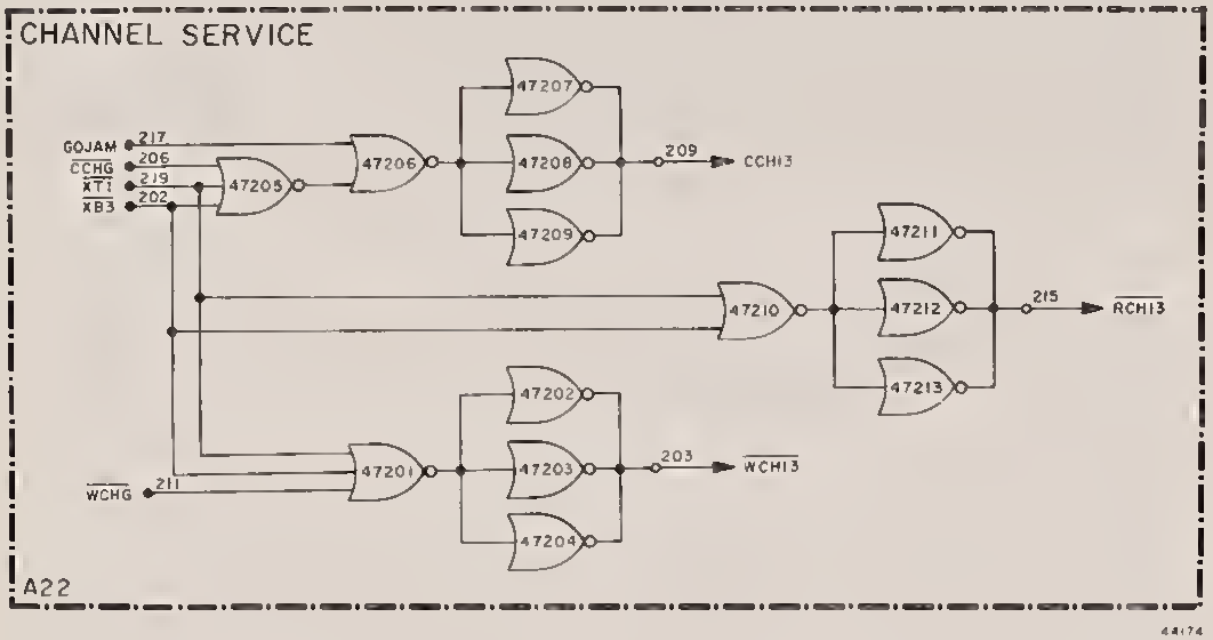


Figure 4-180. Channel 13 Service

4-5.7.9.2 Radar Control. The radar control logic is active in the LGC only. (See figure 4-181.) Bit positions 1 through 4 of channel 13 control the processing of radar data for both the rendezvous radar (RR) and landing radar (LR). Bit position 4 must contain a ONE for radar data to be processed. Bit positions 1 through 3 of channel 13 determine the type of data to be processed. The resultant output signals to the radars are indicated in table 4-XCV.

Table 4-XCV. Radar Data Processing

Bit Positions			Radar Data Processed	Signal Generated
3	2	1		
0	0	0		
0	0	1	RR range	(RRRANG)
0	1	0	RR range rate	(RRRARA)
0	1	1		
1	0	0	LR range	(LRRANG)
1	0	1	LR X velocity	(LRXVEL)
1	1	0	LR Y velocity	(LRYVEL)
1	1	1	LR Z velocity	(LRZVEL)

Inputs from the radars to the LGC occur in the form of pulses (RRIN1, RRIN0 and LRIN1, LRIN0) subject to sync pulses RRSYNC or LRSYNC. The input radar data is applied to priority control as signals RNRADP and RNRADM. When 15 pulses have been received from the radar, the radar control generates signal RADRPT to terminate the generation of sync pulses and cause the priority control to request the execution of interrupt RUPT9. This interrupt enables the execution of the radar leadin routines which digest the radar inputs.

When a ONE is entered into bit position 4 together with the necessary selection data in bit positions 1 through 3, FF 45402-45403 is set the next time signal F10A is generated. This action results in the generation of the 3 μ sec, 100 pps signal ADVCNT which steps the counter consisting of gates 45405 through 45434. Signal ADVCNT also sets FF 45320-45321 which enables the generation of the radar data request signals specified by the contents of bit positions 1 through 3. The 3200 pps radar request signal is supplied to the appropriate radar subject to timing signal F5BSB2. At the occurrance of the ninth ADVCNT pulse, the counter generates signal CNTOF9 thereby inhibiting the generation of the radar data request signals and enabling the reception of the requested radar data.

The first GTSET signal to occur following the generation of signal CNTOF9 causes FF 45337-45338 to be set. (Signal GTSET occurs approximately every 5 msec.) This action enables gate 45339 and causes the generation of either RRSYNC or LRSYNC

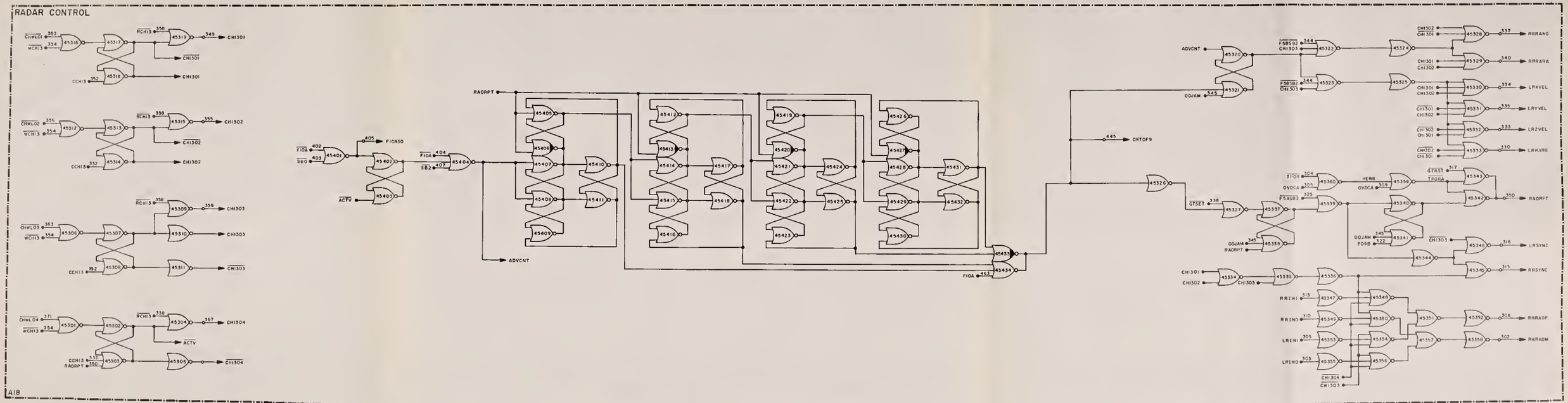


Figure 4-181, Radar Control Logic

pulses at a 3200 pps rate. The sync pulse generated is dependent upon the content of bit position 3. (The timer generates 3200 pps reset pulses RRRST and LRRST which occur halfway between the sync pulses.) The radar, under control of both a radar request signal and a sync pulse, returns the requested data in serial form as pulses RRIN1 and RRIN0 or LRIN1 and LRIN0. The incoming pulses are gated according to the contents of bit positions 1 through 4 and cause the generation of pulses RNRADP or RNRADM. A RRIN1 or a LRIN1 pulse gated causes a RNRADP to be generated; a RRIN0 or a LRIN0 pulse causes a RNRADM to be generated. Each RNRADP or RNRADM pulse is forwarded to the priority control to request the execution of instruction SHINC or SHANC, respectively.

When gate 45339 was enabled to cause the generation of sync pulses, FF 45340-45341 was also set. This allows for the generation of signal RADRPT upon the occurrance of signal GTRST. Since signal GTRST is generated approximately 5.0 msec after signal GTSET, 15 sync pulses are generated during the interval and 15 input signals are received from the radars. When signal GTRST occurs, signal RADRPT is generated which:

a. Resets RR 45337-45338 to inhibit itself and the generation of sync pulses.

b. Resets bit position 4, thus resetting FF 45402-45403 and inhibiting signal ADVCNT.

c. Resets the radar counter in preparation for the next ADVCNT signal.

d. Requests the execution of RUPT9 to enable the processing of the radar data.

Thus radar data is requested, received, and processed within the LGC.

4-5.7.9.3 Uplink and Crosslink Input Logic. The uplink and crosslink input logic (figure 4-182) is identical for the LGC and CMC. Bit positions 5 and 6 control the processing of serial data from both uplink and crosslink. Bit position 6 must contain a logic ZERO for either type of data to be processed. The contents of bit position 5 determine which type of data is processed, a logic ZERO for uplink or a logic ONE for crosslink. Output signals INLNKP and INLNKM increment or decrement the inlink counter subject to timing signal F04A and input signals UPL0, UPL1, XLNK0, and XLNK1. Each INLNK pulse is supplied to the priority control to request the execution of instruction SHINC or SHANC.

When bit positions 5 and 6 contain ZERO's and signal BLKUPL (block uplink) is not present, signal INLNKM is generated whenever signal UPL0 is received from uplink and signal INLNKP is generated whenever signal UPL1 is received. When bit position 5 contains a ONE and bit position 6 contains a ZERO, FF 46224-46225 is set which inhibits the processing of uplink data and enables the processing of crosslink data. In this case output signal INLNKM is generated subject to signal XLNK0 from crosslink and signal INLNKP is generated subject to signal XLNK1. Timing signal F04A, which is generated every 156 μ sec, sets FF 46216-46217 and enables gates 46203 and 46206

thereby allowing signals INLNKM and INLNKP to be supplied to the priority control. When signal C45R is received from the priority control indicating the inlink cell has been reset, FF 46216-46217 is reset which inhibits the generation of additional INLNK pulses. In addition, gate 46211 is enabled so the reception of an uplink or crosslink pulse before FF 46216-46217 is set again by signal F04A, causes bit position 11 of channel 33 to be set indicating the inlink rate is too fast.

4-5.7.9.4 RHC Input Logic. The RHC input logic (figure 4-183) is contained in the LGC only. Bit positions 8 and 9 of channel 13 control the processing of data from the rotational hand controller. Whenever the hand controller is moved out of the detent position, a ONE is entered into bit position 3 of channel 31 and the controller and meter routine is executed. This routine clears the RHC counters and sets bit positions 8 and 9 of channel 13. A ONE in bit position 9 causes FF 46328-46329 to be set at the occurrance of timing signal F07D. Approximately 234 μsec later the flip-flop is reset by signal F07B. During the interval between F07D and F07B, signal RHCGO is generated which resets bit position 9 and enables an analog-to-digital converter (circuit A) in the interface circuits. The A/D converter generates signals SIGNX, Y, and Z (SIGN__) and signals GATEX, Y, and Z (GATE__) in response to the RHCGO signal. If bit position 8 contains a ONE, signals BMAGXP through BMAGZM are generated subject to the inputs from the A/D converter. The outputs are termed BMAGXP, etc., to maintain consistency with engineering information. If the SIGN__ signal is a logic ONE, the appropriate BMAG__P signal is produced; if the SIGN__ signal is logic ZERO, the appropriate BMAG__M signal is produced. Signals GATEX, GATEY, and GATEZ are variable length dc signals which may gate as many as 32 BMAG signals. The width of the GATE__ signals is proportional to the amplitude of the input to the A/D converter from the rotational hand controller. The BMAG signals are sent to the priority control to request the execution of instructions PINC or MINC which increment or decrement the appropriate BMAG counters.

4-5.7.9.5 BMAG Input Logic. The BMAG input logic (figure 4-184) is contained in the CMC. Bit position 8 of channel 13 controls the processing of data from the body mounted attitude gyros. With a ONE in bit position 8 (supplied by program), the three-axes BMAG data is applied to priority control to initiate a counter instruction (PINC or MINC) and to update the associated BMAG counter in memory.

4-5.7.9.6 Handrupt Interrupt Control. In the LGC, bit positions 12 through 14 of channel 13 enable the processing of various inputs from the spacecraft (figure 4-185). When the LGC receives inputs from hand controllers, thrusters, or gimbals, signal HNDRUPT is supplied to the priority control to interrupt computer operation and initiate the execution of the hand control interrupt routine. Bit positions 12, 13, or 14 must contain a logic ONE in order for the interrupt to be generated. Bit 12 must be set in conjunction with the altitude-controller-out-of-detent input (azimuth or elevation data not yet supplied), bit 13 with the translation inputs, and bit 14 with the thruster fail and gimbal inputs. The three bit positions function similarly; therefore, only bit position 12 is described in detail.

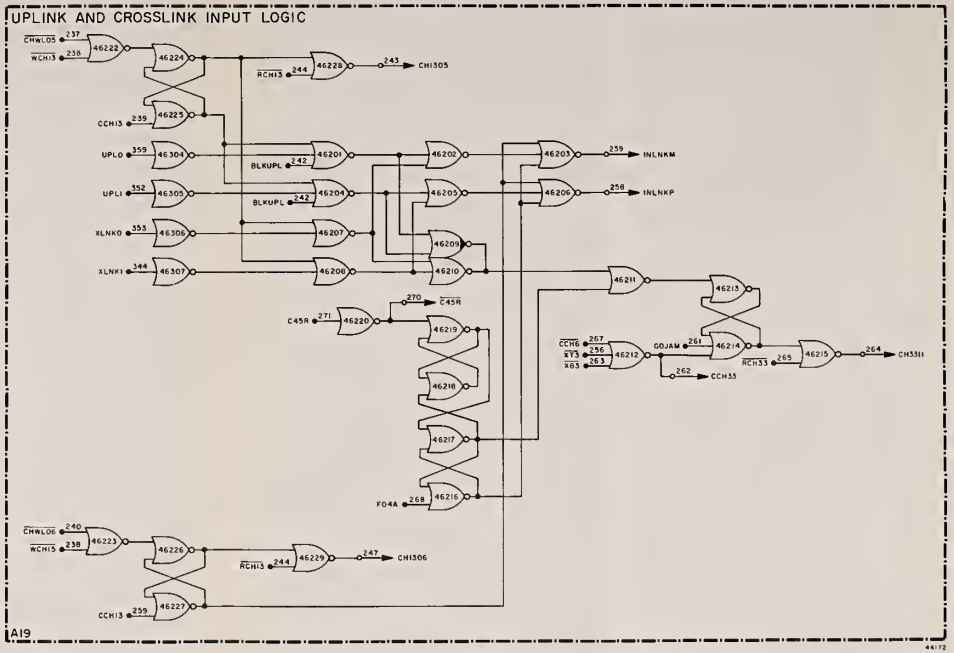


Figure 4-182. Uplink and Crosslink Input Logic

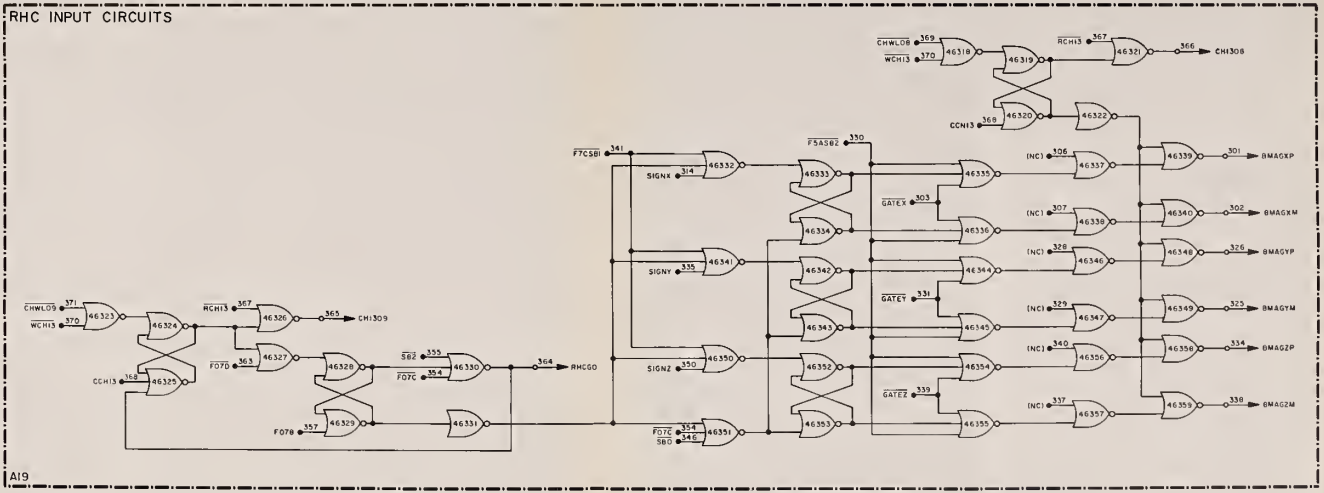


Figure 4-183. RHC Input Logic

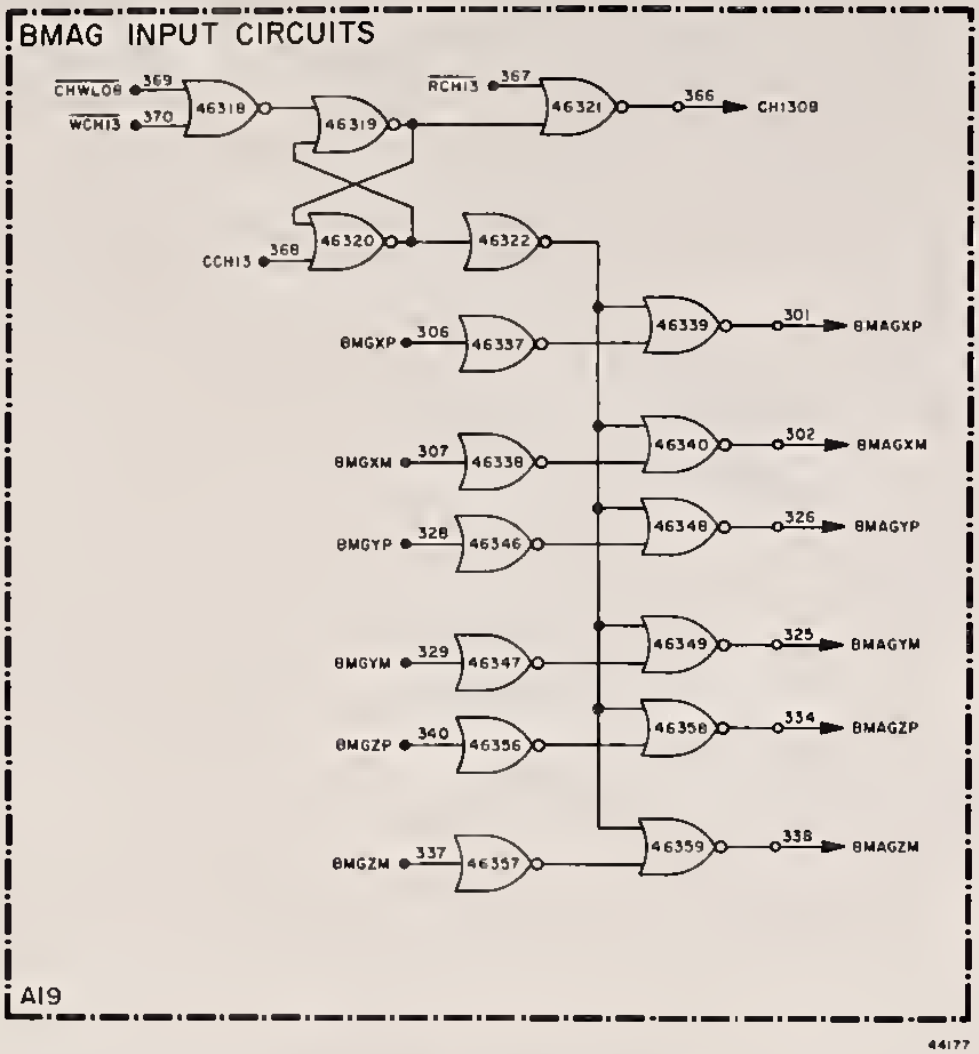


Figure 4-184. BMAG Input Logic

Assuming FF 44213-44212 and 44209-44210 to be initially reset, the occurrence of signal CHWL12 sets FF 44213-44212. This action, coincident with the reception of signal ACNTOD, allows gate 44208 to be enabled by timing signal F05A. When gate 44208 is enabled, FF 44209-44210 is set and gate 44211 is enabled subject to timing signal F05B. This action resets FF 44213-44212 and results in the generation of signal HNDRPT subject to signal TPOR which is generated at T5 or T11 time. The outputs of all three bit positions are ORed by gate 44230 such that any hand controller input produces signal HNDRPT.

In the CMC, bit positions 12 tbrough 14 of channel 13 control the rotation, translation, or minimum impulse hand controller inputs. These differences are as indicated in the boxed signals in figure 4-185. The operation of these logic circuits is similar to that described for the LGC.

4-5.7.9.7 Channel 13 - Bits 10, 11, and 15/16. Bit positions 10, 11, and 15/16 of channel 13 perform separate internal functions common to both the LGC and CMC. A one in bit position 10 causes the generation of signal ALTEST (figure 4-186) whicb inhibits signal RESTRT in the alarm circuit. This allows various caution indicators on the DSKY and the PGNCS panel to be tested. The indicators are inaccessible to program testing. A ONE in bit position 11 enables the standby circuits and a ONE in bit position 15/16 causes tbe generation of a T6RUPT.

4-5.7.10 Output Channel 14. Channel 14 (figure 4-187) controls various areas of the LGC/CMC to transfer data from counters in erasable memory to various PGNCS and spacecraft systems. In the LGC, bit position 1 enables the crosslink control logic which provides a serial data word to the crosslink equipment. Bit positions 2 and 3 are the altitude meter control which provides altitude and altitude-rate data for the altitude meter on the PGNCS display and control panel. Bit positions 4 and 5 are the thrust drive control whicb provides plus and minus drive pulses to the LEM monitoring system and to the propulsion system. Bit positions 6 through 10 constitute the gyro drive control which provides plus and minus drive pulses to the X, Y, and Z gyros. Bit positions 11 througb 15/16 constitute the CDU drive control which provides plus and minus drive pulses to the optics shaft and optics trunnion CDU's and the X, Y, and Z CDU's.

In the CMC, the crosslink logic (bit 1) is identical. Bit positions 2, 3, and 4 are not used. Bit 5 of channel 14 controls the entry monitor system (EMS) outputs. The remaining bit positions control output logic circuits (gyro and CDU) identical to those in the LGC.

4-5.7.10.1 Crosslink Control Logic. The crosslink control logic generates signals OTLNKM, OTLNKO, and OTLNK1 to convert the LGC data word into a 15-bit serial data word to be transmitted by the crosslink equipment. Signal OTLNKM is supplied to the priority control to request the execution of instruction SHINC. Signals OTLNKO and OTLNK1 provide the crosslink data.

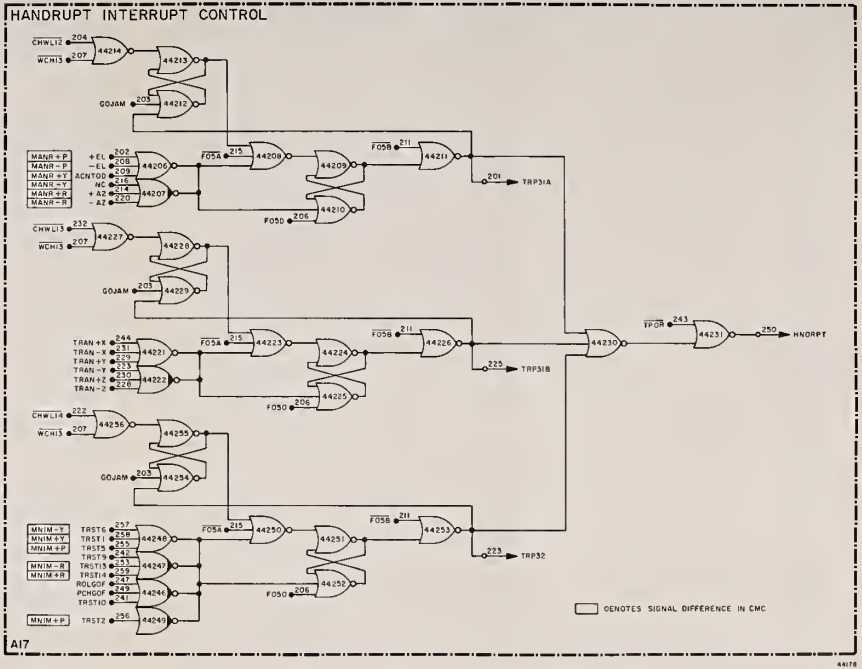


Figure 4-185. Handrupt Interrupt Control Logic

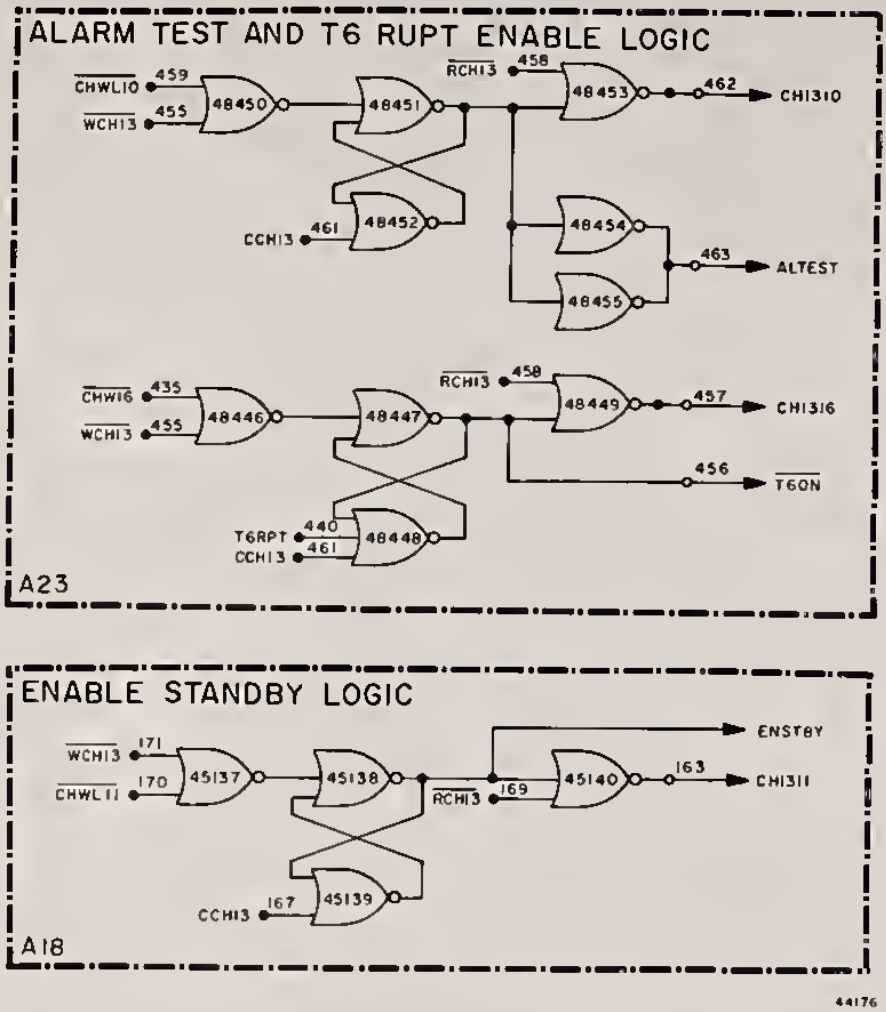


Figure 4-186. Alarm Test, T6RUPT, and Enable Standby Logic

When a ONE is entered into bit position 1, FF 46135-46136 is set. The incidence of signal $\overline{\text{GTSET}}$ sets FF 46138-46139 and prepares gate 46140 for the arrival of signal $\overline{\text{F5ASB2}}$ which occurs approximately 156μ sec later (figure 4-188). Signal $\overline{\text{F5ASB2}}$ sets FF 46141-46142 which resets FF 46135-46136 and causes one OTLNK1 pulse to be generated which is the flag bit for the crosslink word. Approximately 156μ sec later, signal GTONE occurs and resets FF 46138-46139 which inhibits gate 46140. Signal $\overline{\text{F5ASB0}}$, which occurs 156μ sec after signal GTONE, causes signal OTLNKM to be generated and forwarded to the priority control. Since FF 46141-46142 is set, signal OTLNKM is generated every time signal $\overline{\text{F5ASB0}}$ occurs (every 312μ sec). This action continues until signal GTSET occurs again. Since signal GTSET occurs every 5 msec, 15 OTLNKM pulses are generated during the interval to provide for a complete crosslink word.

Each time an OTLNKM pulse is supplied to the priority control, instruction SH1NC is requested and the address of the outlink counter (0057) is formed. Each time SH1NC is executed, the content of counter OUTLNK which was loaded by the program is shifted one place to the left and the bit shifted out is converted to an OTLNKO pulse. The counter address (signals $\overline{\text{CA5}}$ and $\overline{\text{CXB7}}$), together with instruction SH1NC at T06 time (signal $\overline{\text{SH3M3}}$), enables gates 46146 and 46147 so that the state of signal BR1 determines whether pulse OTL1NK1 or OTLINK0 is generated. If the bit shifted out of counter OUTLNK is a ONE, signal BR1 is a ONE and pulse OTLINK1 is generated. If the shifted bit is a ZERO, signal BR1 is also a ZERO and pulse OTLINKO is generated. When a new crosslink word is entered into counter OUTLNK, bit position 1 of channel 14 is set and the operation is repeated.

4-5.7.10.1A Altitude Meter Control. The altitude meter control logic is contained in the LGC only. This logic section converts an LGC data word into a 15-bit serial data word to be used to control the altitude meter on the PGNCS display and control panel. Signal ALTM is supplied to the priority control to request the execution of instruction SH1NC. Signals ALT0, ALT1, and ALTR1 provide the altitude data subject to sync pulse ALTSNC. The contents of bit position 2 determine whether altitude (ALT0, ALT1) or altitude rate (ALTR0, ALTR1) data is processed. Bit position 3 is used like bit position 1 for the crosslink control and the timing shown in figure 4-188 is identical except that signal ALTM is generated by the altitude meter control in place of signal OTLNKM for the crosslink control.

When a ONE is entered into bit position 3, FF 46124-46125 is set with the occurrence of signal GTSET and signal ALTSNC is generated. Approximately 156μ sec later, subject to timing signal F5ASB2, an ALT1 or ALRT1 pulse (the flag bit for the altitude word) is generated. In addition, FF 46127-46128 and 46130-46131 are set and bit position 3 is reset. Signal GTONE is generated approximately 156μ sec later which resets FF 46124-46125 and 46130-46131. This has no effect on signal ALTSNC since FF 46127-46128 is still set, generating signal ALTSNC. Signal ALTM is generated 156μ sec after signal GTONE subject to timing signal F5ASB0. Signal ALTM is then generated every 312 μ sec until inhibited by the next GTSET signal which resets FF 46127-46128 and also inhibits signal ALTSNC. A total of 15 ALTM signals are generated between the occurrence of signals GTONE and GTSET.

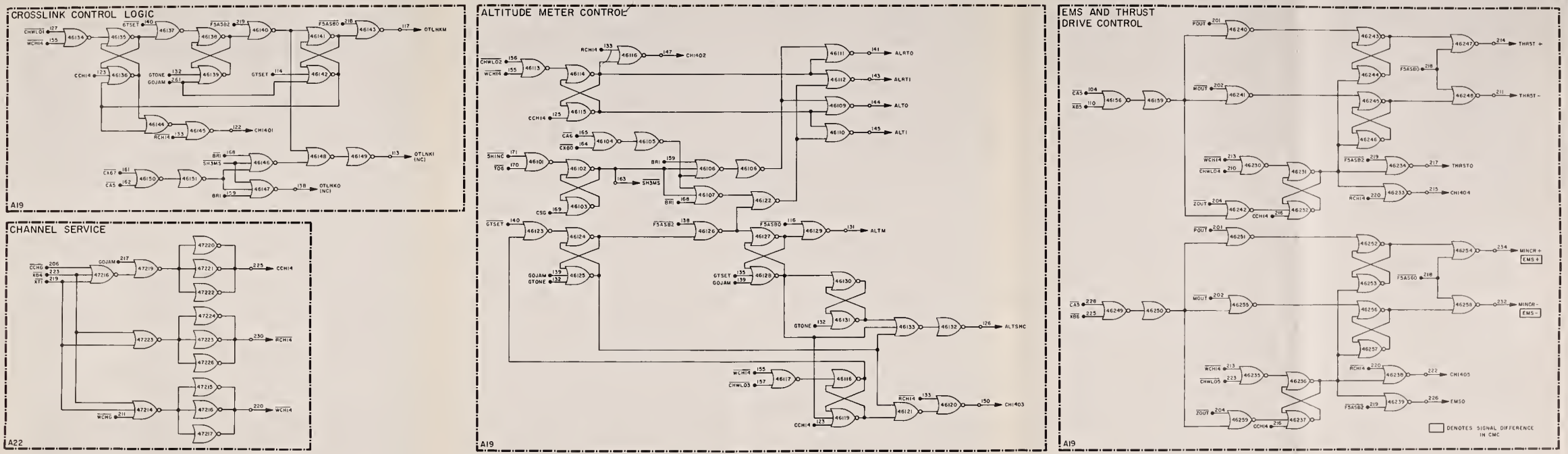


Figure 4-187. Crosslink, Attitude Meter, EMS and Thrust Drive Control Logic

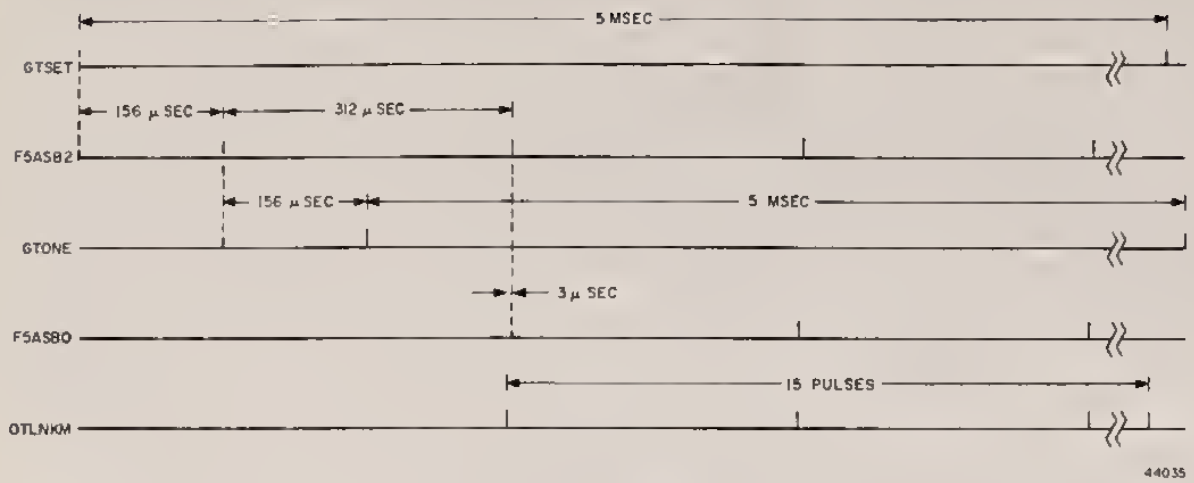


Figure 4-188. Crosslink Timing

Each time signal ALTM is supplied to the priority control, instruction SHINC is requested and the address of the altitude meter counter (0060) is formed. Instruction SHINC shifts the content of the preloaded counter one place to the left and the bit shifted out is converted to an ALT or an ALRT pulse. The counter address (signals CA6 and CXB0) together with instruction SHINC at T06 time enables gate 46106 or 46107 so that the state of signal BR1 determines which pulse (ALT or ALRT) is generated. If the bit shifted out of the counter is a ONE, signal BR1 is a ONE and pulse ALT1 or ALRT1 is generated depending upon the content of bit position 2. If the shifted bit is a ZERO, signal BR1 is ZERO and pulse ALT0 or ALRT0 is generated. When a new altitude meter word is entered into the counter, bit position 3 is set and the operation is repeated.

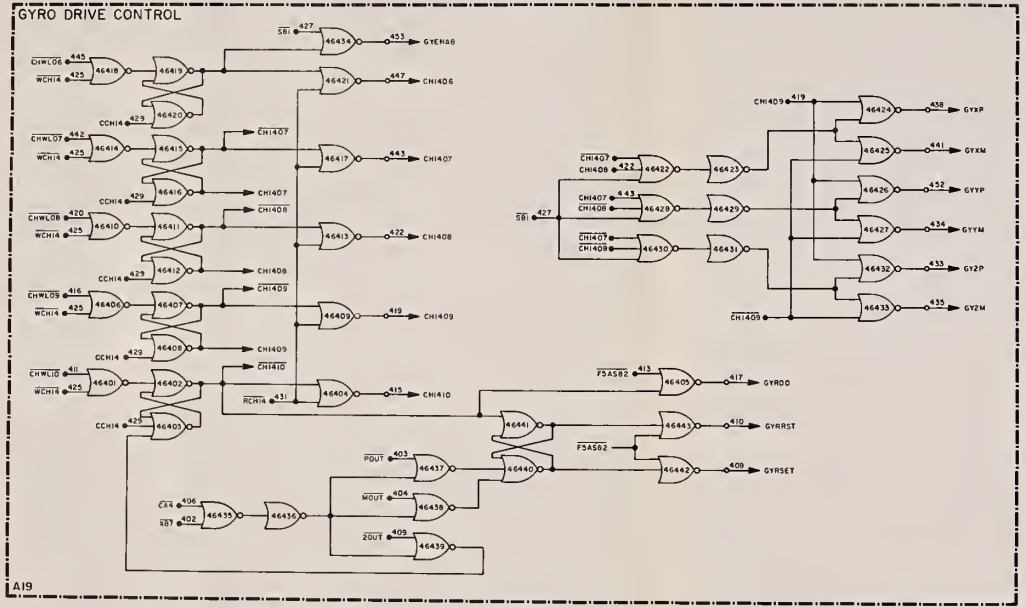
4-5.7.10.2 Thrust Drive Control. The thrust drive control (figure 4-181) is active in the LGC only. Bit positions 4 and 5 of channel 14 cause signals THRSTD, EMSD, THRST+, THRST-, MINCR+, and MINCR- to be generated. Signals THRSTD and EMSD are supplied to the priority control to request the execution of instruction DINC and the remaining signals supply plus and minus drive pulses to the propulsion system and the LEM monitoring system depending upon the content of the associated counters in erasable memory. Since the operation of both bit positions is identical, only the operation of bit position 5 is described.

A ONE entered into bit position 5 of channel 14 enables the generation of signal EMSD every 312μ sec subject to timing signal F5ASB2. Each signal EMSD requests the execution of instruction DINC to decrement the content of the EMS counter. Signal EMSD also causes the forming of address 0056 (signals $\overline{CA5}$ and $\overline{XB6}$). This address and signal POUT or MOUT from the sequence generator produce output pulse MINCR+ or MINCR-, respectively. Each time signal EMSD is generated, this operation is repeated until the EMS counter contains zero. When this occurs, signal ZOUT is generated which resets FF 46236-46237 and inhibits any additional EMSD signals.

In the CMC, bit position 5 only is used to generate outputs EMS+ and EMS- to the entry monitor system. Operation of this logic is similar to that for MINCR+ and MINCR- described above for the LGC.

4-5.7.10.3 Gyro Drive Control. The gyro drive control (figure 4-189) is identical in both the LGC and CMC. Bit positions 6 through 10 of channel 14 generate gyro enable (GYENAB), gyro set (GYRSET), gyro reset (GYRRST), and six drive pulses to torque the gyros. In addition, the gyro drive control sends signal GYROD to the priority control to request the execution of instruction DINC. Bit position 6 controls the generation of GYENAB, bit position 10 controls GYROD, and bit positions 7 through 9 determine the gyro to be torqued and the direction of torquing.

Assuming an initial condition where FF 46402-46403 is reset and FF 46441-46440 is set, GYRRST pulses are sent to the gyros at a 3200 pps rate subject to signal F5ASB2. When the desired quantity is entered into the GYROS counter in erasable memory, a ONE is entered into bit positions 6 and 10 and some combination of ONE's and ZERO's is entered into bit positions 7 through 9. (Refer to table 4-XCVI for the decoding of these bits into drive pulses.) Signals GYENAB and GYROD are generated subject to timing signals SB1 and F5ASB2, respectively. Signal GYENAB enables the gyros for torquing; signal GYROD requests the execution of instruction DINC and causes the forming of address 0047 (signals $\overline{CA4}$ and $\overline{XB7}$). This address, coincident with signal POUT or MOUT from the sequence generator, causes FF 46441-46440 to be reset. Gate 46443 is inhibited and gate 46442 is enabled thus inhibiting GYRRST pulses and initiating GYRSET pulses. When the content of the GYROS counter has been reduced to zero, signal ZOUT is received which resets FF 46402-46403, sets FF 46441-46440, inhibits pulses GYROD and GYRSET, and enables the generation of GYRRST pulses. Thus, the torquing cycle is complete.



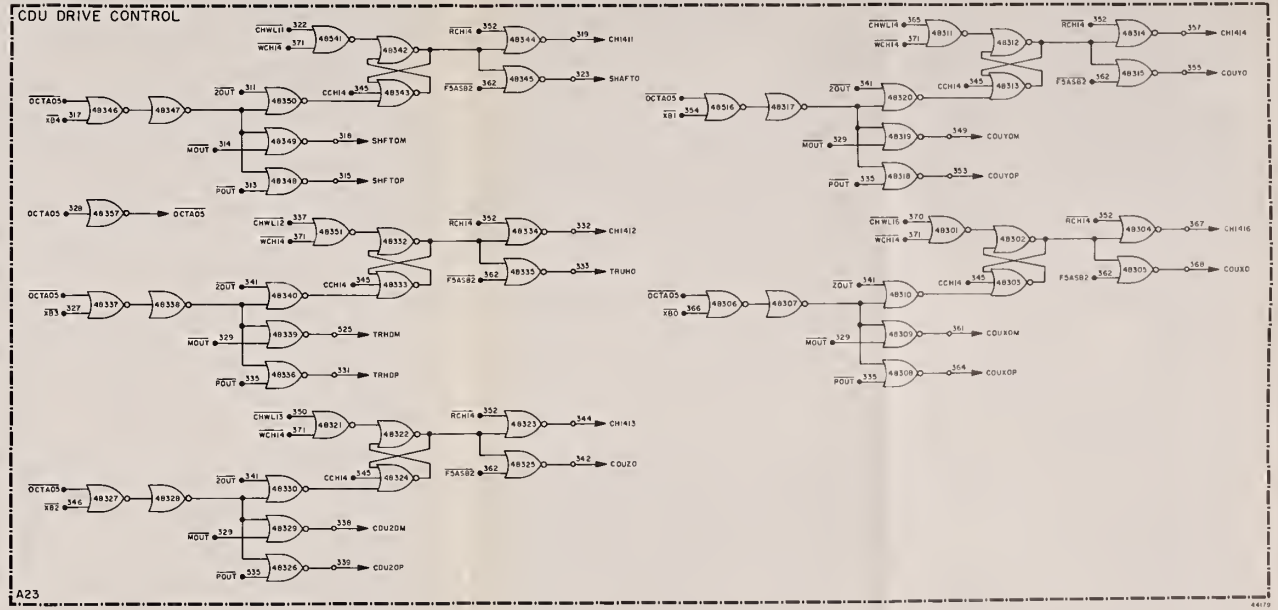


Figure 4-189. Gyro and CDU Drive Control Logic

4-5.7.10.4 CDU Drive Control. The CDU drive control is also identical in both the LGC and CMC. Bit positions 11 through 15/16 of channel 14 generate drive pulses to position the X, Y, Z shaft, and trunnion CDU's. Since the operation of the five bit positions is identical, only bit position 11 is described.

A ONE in bit position 11 causes the generation of signal SHAFTD which requests instruction DINC and causes address 0054 (signals $\overline{CA5}$ and $\overline{XB4}$) to be formed. Signal POUT or MOUT from the sequence generator causes the shaft CDU to be driven positive or negative until the contents of the shaft CDU counter is reduced to zero. When the CDU counter is a zero, signal ZOUT is received from the sequence generator, FF 48342-48343 is reset, and signal SHAFTD is inhibited.

Table 4-XCVI. Gyro Drive Pulses

Bit Positions			Drive Pulse Generated
7	8	9	
0	0	0	No output
1	0	0	No output
0	0	1	GYXP (X gyro plus)
1	0	1	GYXM (X gyro minus)
0	1	0	GYYP (Y gyro plus)
1	1	0	GYYM (Y gyro minus)
0	1	1	GYZP (Z gyro plus)
1	1	1	GYZM (Z gyro minus)

4-5.7.11 Downlink Converter. The downlink converter (figure 4-190) converts parallel data contained in output channels 34 and 35 into serial data for transmission downlink. Three pulses (DKSTRT, DKBSNC, and DKEND), received from the telemetry equipment, control the operation of the downlink converter. Pulse DKSTRT starts the downlink transmission; pulse DKBSNK processes one bit at a time out of channels 34 and 35; pulse DKEND ends the downlink transmission. When the transmission is complete, signal DLKRPT is generated by the downlink interrupt circuit which causes the execution of the downlink routine. This routine loads new data into channels 34 and 35 and sets bit position 7 of channel 13. If signal DKEND is received more than once in a 10 msec interval, bit position 12 of channel 33 (the downlink interrupt circuit) is set to indicate the downlink transmission rate is too fast.

Signal DKSTART causes the generation of signal DLKCLR which resets the five-stage downlink counter and sets FF 47105-47104 in the downlink counter and 47153-47154 in the word order logic. The first flip-flop generates signal $\overline{\text{RDOUT}}$ and the latter generates signals WDORDR and ORDRBIT. These three signals set up gates 47256 and 47261 so that the reception of a sync pulse ($\overline{\text{BSYNC}}$) causes the gates to be enabled thereby transmitting data downlink via signals DKDATA and DKDATB. Each $\overline{\text{BSYNC}}$ pulse is also supplied to gate 47106 in the downlink counter. The first $\overline{\text{BSYNC}}$ pulse has no effect on the counter since signal WDORDR inhibits the gate and prevents the generation of signal ADVCTR; however, the order bit is transmitted downlink to identify the type of data being transmitted. The first $\overline{\text{BSYNC}}$ resets FF 47153-47154 which inhibits signal WDORDR and enables gate 47106. As each successive $\overline{\text{BSYNC}}$ pulse is received, the downlink counter is advanced by one suhject to signal ADVCTR until a count of 16 has heen reached. Then pulse DKEND is received which resets FF 47105-47104 and inhibits the generation of signals DKDATA and DKDATB via signal $\overline{\text{RDOUT}}$. Pulse DKEND also causes the generation of signal DLKRPT as previously described.

The outputs of the downlink counter (signals DKCTR1-DKCTR5) are decoded and are used to control the read gates of channel 34. The decoding is such that the content of bit position 15 is transmitted first followed by the contents of bit positions 14 through 1 and the parity bit. Thus a total 33 bits are transmitted downlink, the order bit (ORDRBT) and 16 data bits.

4-5.7.12 Interface Modules A25-A29. The interface modules provide interfacing between the LGC/CMC and the DSKY, spacecraft, and remainder of the PGNCS. All inputs to and outputs from the LGC/CMC are routed through these modules. Interface modules A25 and A26 are identical as are A27 through A29. Figures 4-191 and 4-192 illustrate the signal flow of all signals.

Seven interface circuits provide the proper voltage levels and impedance matching between the computer and other spacecraft systems. Circuit A is an analog-to-digital converter contained in the LGC only. This circuit converts rotational hand controller position signals to pulses for use in the RHC input circuits. The upper half of the transformer (T1) secondary charges capacitors C3 and C4 through CR1 and the base to

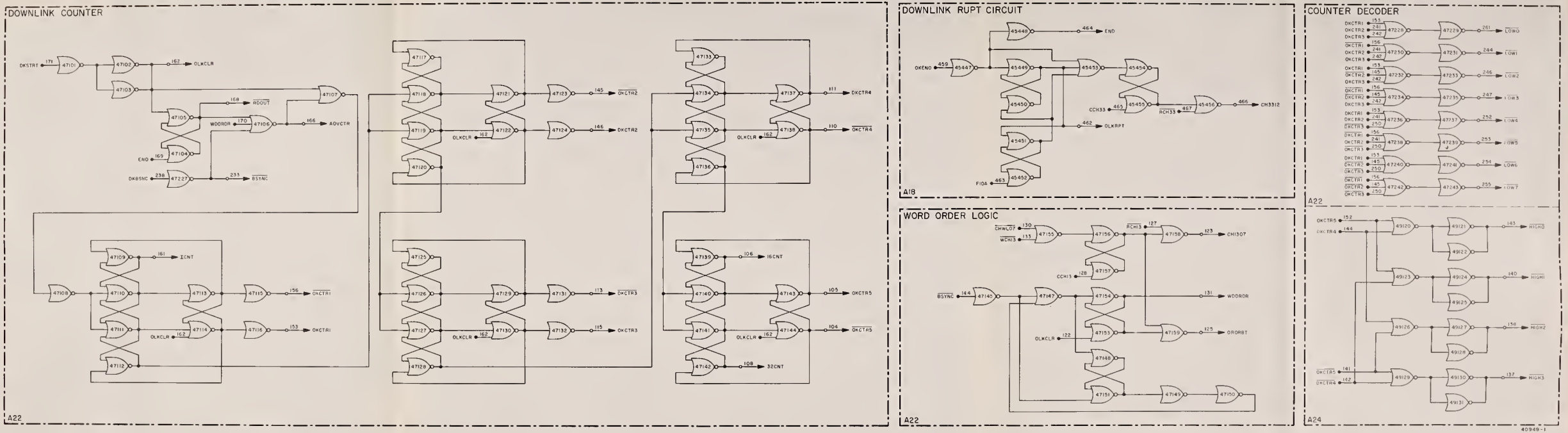


Figure 4-190. Downlink Control Logic (Sheet 1 of 3)

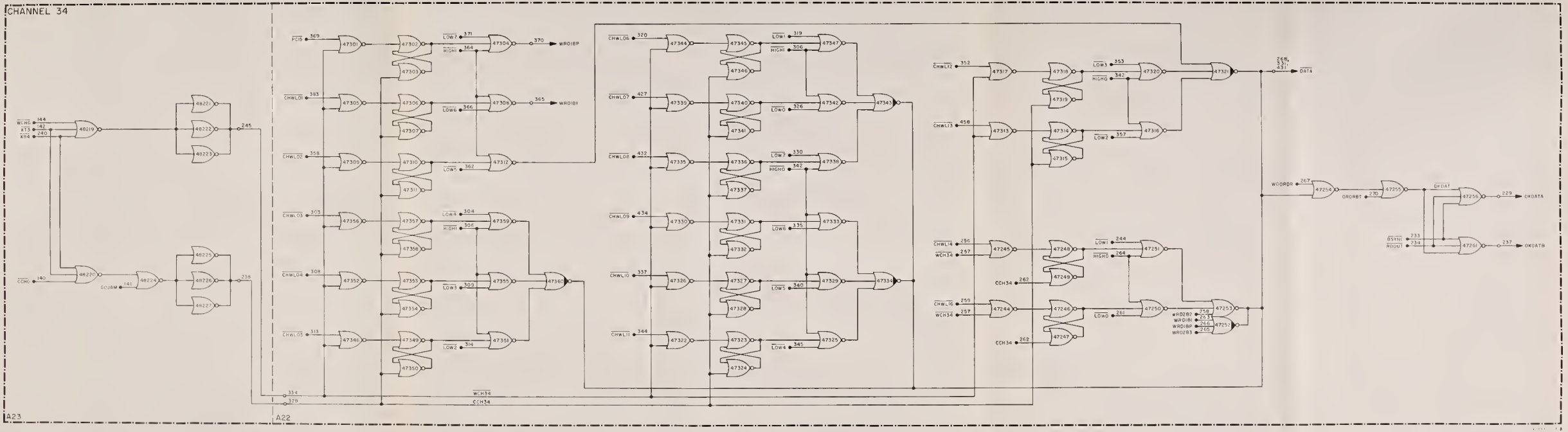


Figure 4-190. Downlink Control Logic
(Sheet 2 of 3)

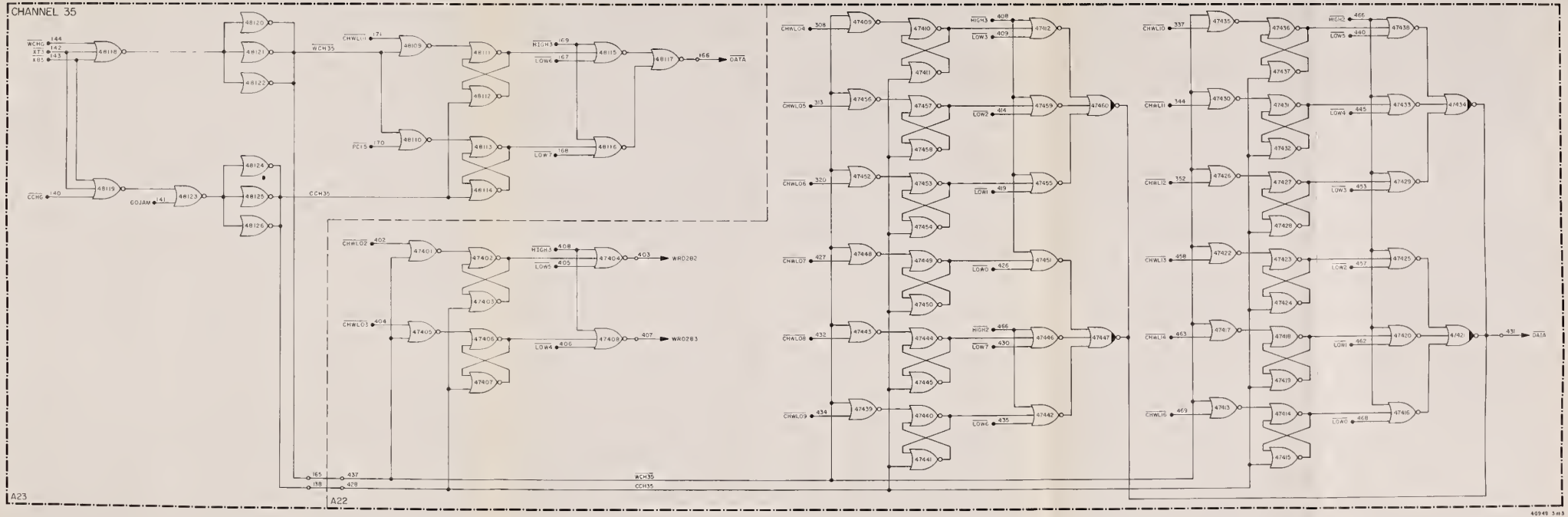
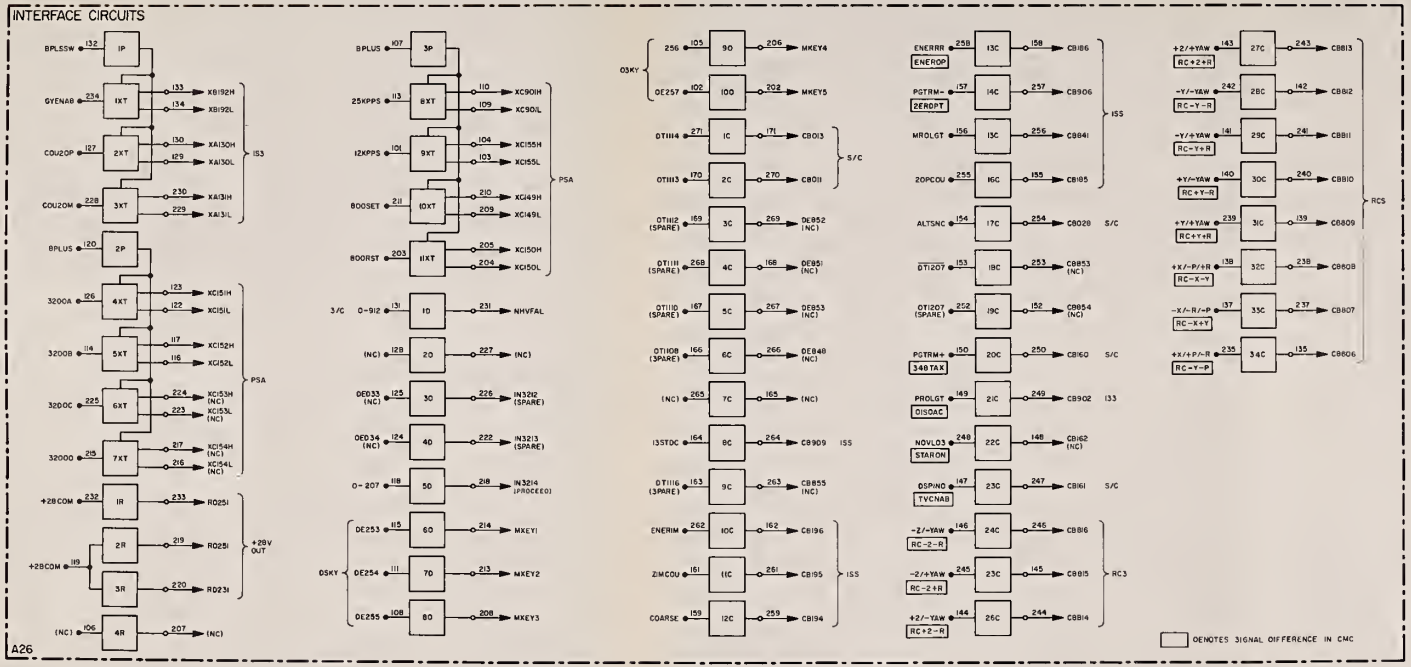


Figure 4-190. Downlink Control Logic (Sheet 3 of 3)



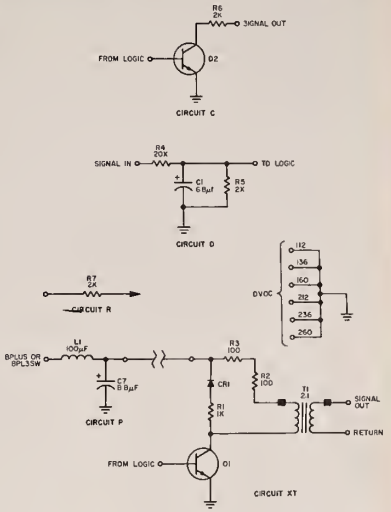


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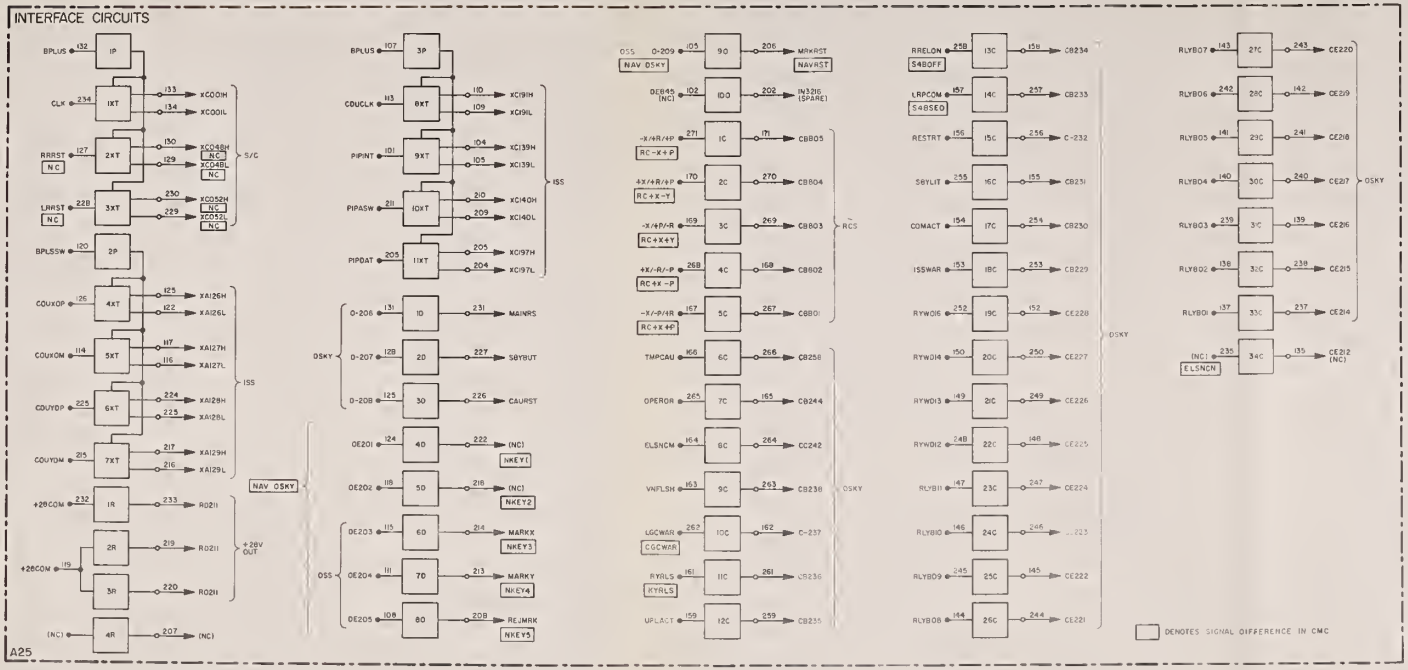
Figure 4-191. Interface Modules A25 and A26 (Sheet 1 of 2)



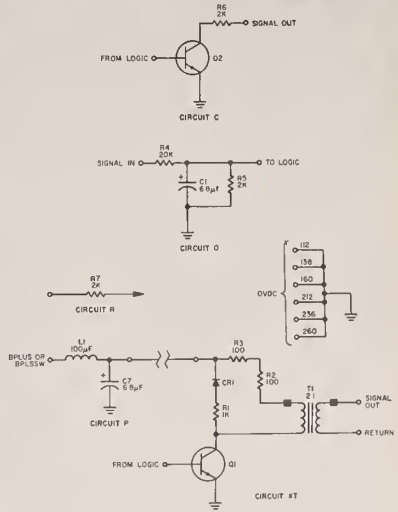
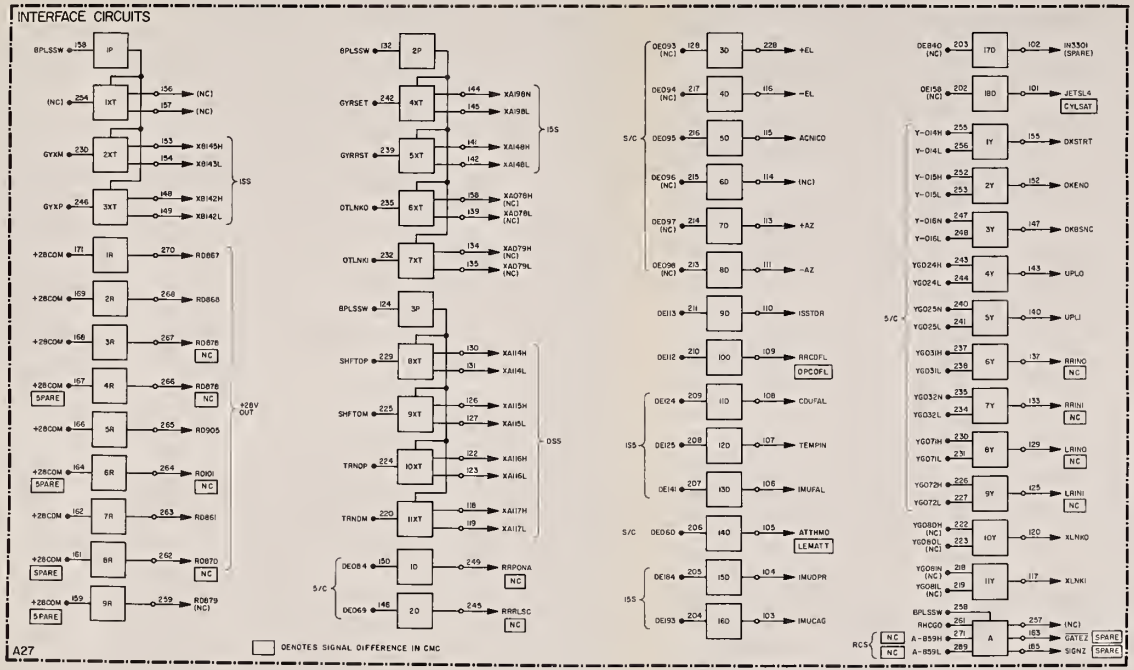


Figure 4-191. Interface Modules A25 and A26 (Sheet 2 of 2)



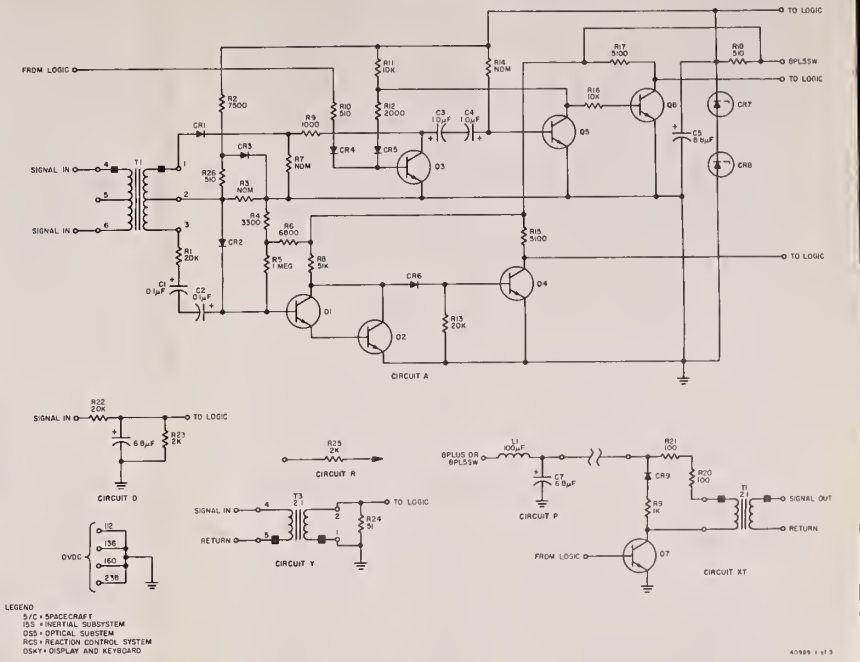
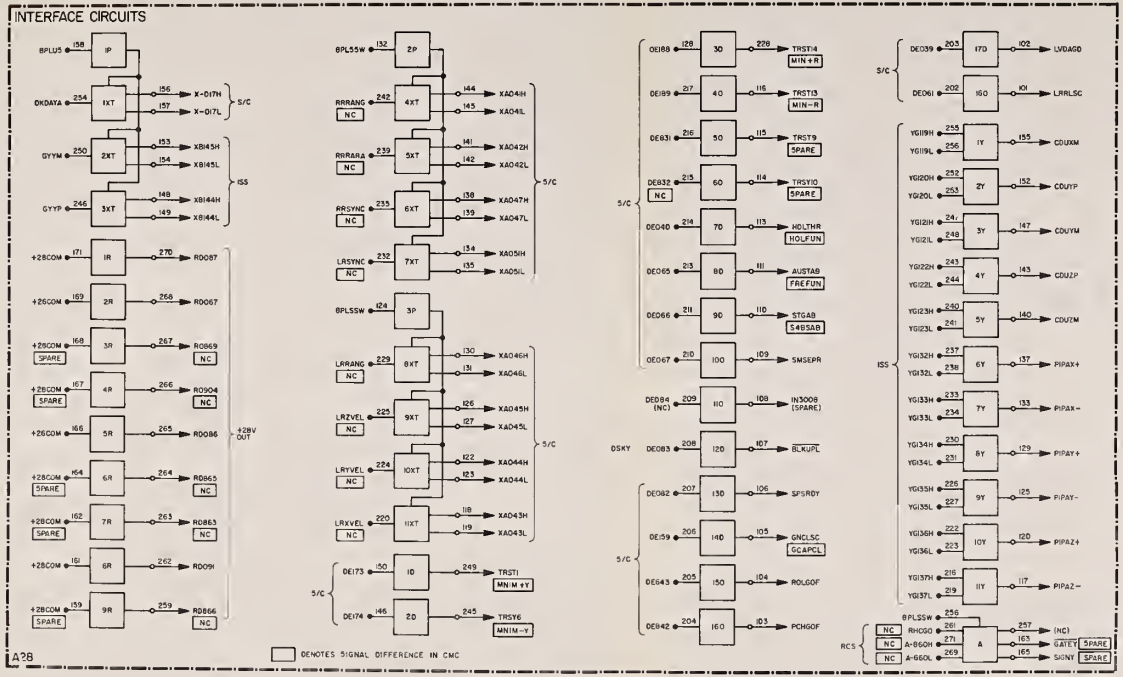


Figure 4-192. Interface Modules A27, A28, and A29 (Sheet 1 of 3)



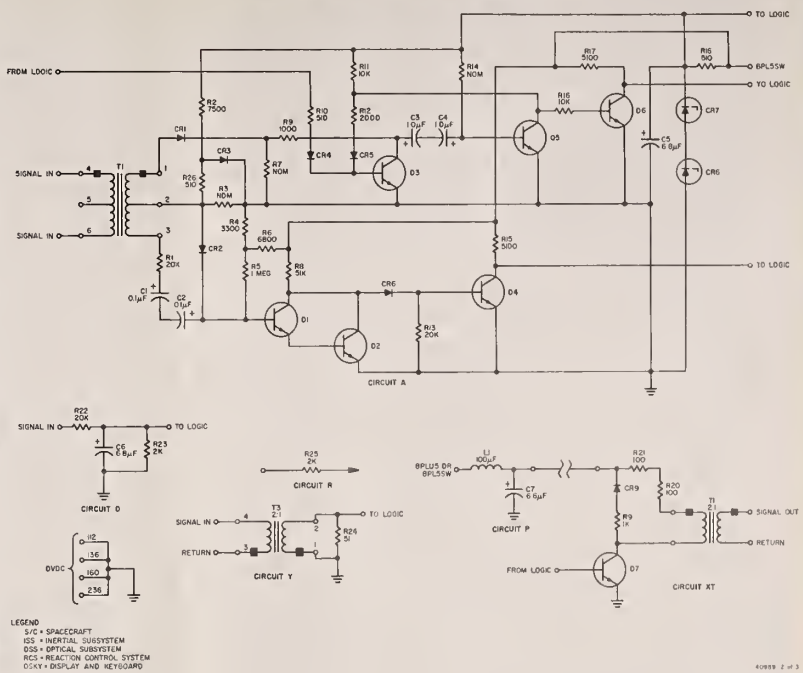
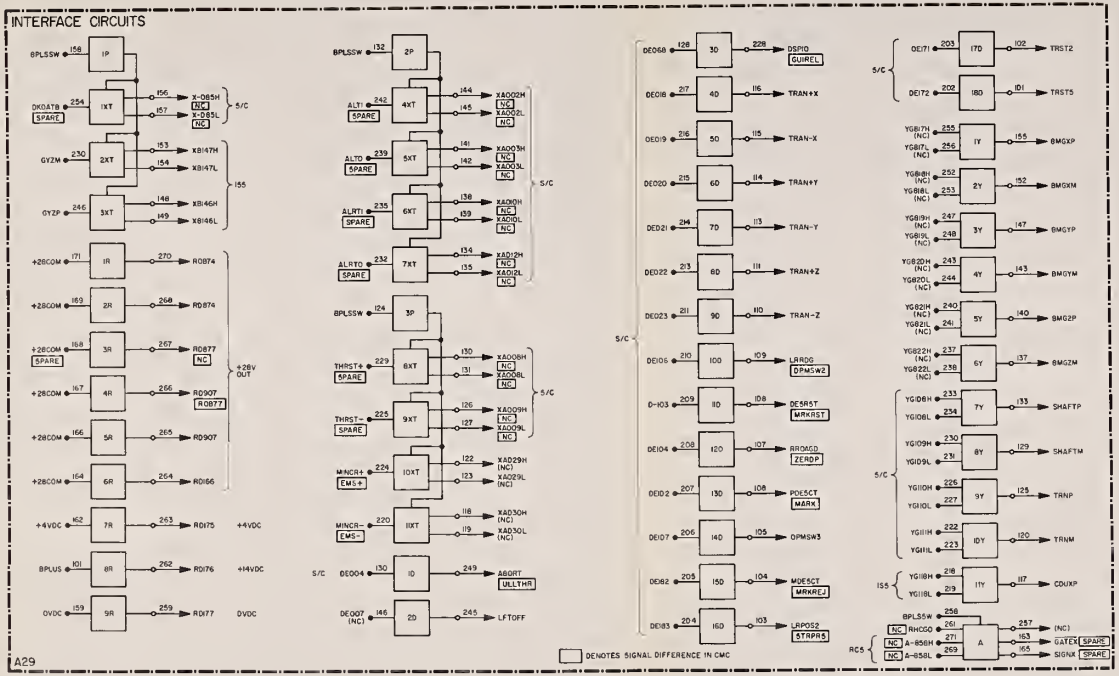


Figure 4-192. Interface Modules A27, A28, and A29 (Sheet 2 of 3)



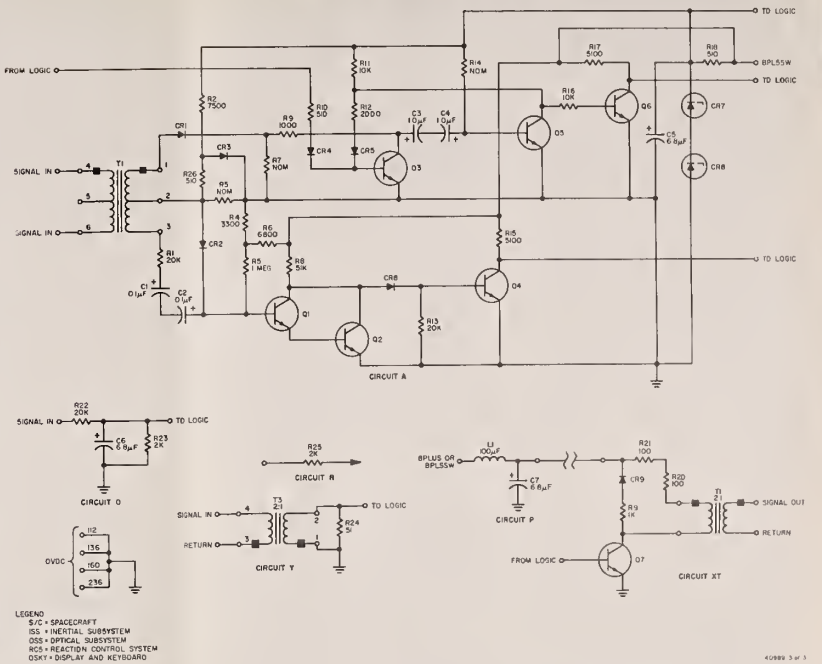


Figure 4-192. Interface Modules A27, A28, and A29 (Sheet 3 of 3)

emitter path of transistor Q5. When pulse RHCGO is applied to the base of Q3, transistor Q5 is cut off for a time proportional to the peak voltage at the input. Therefore the width of the output pulse (GATEX, Y, or Z) at the collector of Q6 is proportional to the amplitude of the input signal. The bottom half of the transformer secondary squares the input signal to detect phase. The output pulse (SIGNX, Y, or Z) at the collector of Q4 reflects the polarity of the input signal from the hand controller. The C circuit is a transistor driver circuit which buffers outputs from the computer to the DSKY and the reaction control system. The D circuit consists of an RC filter, the output of which is applied directly to the computer logic circuits. The P circuit filters the +14 volt input to the XT circuit. The series resistor R circuit is used to provide short circuit protection for outputs from the power supply. The transformer output interface circuit (XT) consists of a pulse transformer driven by an input transistor circuit. It provides the required output impedance to match spacecraft circuits and other subsystems of the PGNCS. The transformer input interface circuit (Y) consists of a pulse transformer and associated components which provide impedance matching and voltage level necessary to operate the logic in the computer.

All signals interfaced with the computer have an alphanumeric code rather than the functional name when routed outside any particular subsystem. This code is used in the interface drawings and designates the interface circuit type and signal type and number (for example, DE040).

The first letter designates the interface circuit type:

A Analog-to-digital converter

C Discrete type output circuit

D Discrete type input circuit

R Resistor in series
S Switch closure
} direct wire no interface circuit required

W Connecting wire

X Transformer coupled output circuit (XT)

Y Transformer coupled input circuit

The second letter designates the type of signal:

A Indicates the signal is under counter control; each output pulse is counted

B Indicates the signal is under program control

C Indicates the signal is continuous

D Indicates the signal is a dc level

E Indicates the signal goes to an IN bit or comes from an OUT bit

G Indicates the signal goes to a counter

The digits indicate interface signals between specific systems:

001 - 100	LGC/spacecraft interface
100 - 200	LGC/PGNCS interface
200 - 300	LGC/DSKY interface
300 - 400	DSKY/PGNCS interface
400 - 500	DSKY/spacecraft interface
600 - 700	LGC/GSE interface
700 - 800	LGC/GSE interface
800 - 900	LGC/spacecraft interface
900 - 1000	LGC/PGNCS interface

4-5.8 MEMORY. Memory consists of an erasable memory with a storage capacity of 2048 words and a fixed core rope memory with a storage capacity of 36,864 words. Erasable memory is a random-access, destructive readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a nondestructive storage device. Data stored in fixed memory is unalterable since the data is wired in.

Both memories contain magnetic-core storage elements. In erasable memory the storage elements form a core array (one module); in fixed memory the storage elements form three core ropes (six modules). Erasable memory has a density of one word per 16 cores; fixed memory has a density of twelve words per core. Each word is located by an address from the central processor.

4-5.8.1 Erasable Memory Functional Description. Erasable memory (figure 4-193) consists of a core array, memory cycle timing circuits, selection circuits, and sense amplifiers. The core array is the medium by which data is stored in erasable memory. The memory cycle timing circuits generate strobe signals which enable the selection circuits and the sense amplifiers. The selection circuits select the addressed storage location under control of the selection signals from the address decoder in the central processor and strobe signals from the memory cycle timing circuits. The sense amplifiers detect the contents of the selected storage location and supply half of the data directly to the central processor and the other half through the fixed memory sense amplifier.

Erasable memory is addressed (table 4-XCVII) by the contents of registers S and EBANK of the central processor. Erasable memory is subdivided into eight banks (0 through 7), each storing 256 words. The first 8 locations of bank 0 are used for addressing the central processor registers. Another 12 addresses are reserved for addressing special locations and 29 for addressing counters. The remaining 207 addresses of bank 0 are used for addressing locations which are accessible for general use.

Banks 0, 1, and 2 are referred to as unswitched E memory because all their locations can be addressed by register S without regard to what might be contained in EBANK. Banks 3 through 7 are referred to as switched E memory because their locations can be addressed only through a combination of the S and EBANK registers. Locations in unswitched E memory can also be addressed as locations in switched E memory if the proper bank address is contained in register EBANK.

Erasable memory is addressed only when bit positions 12 and 11 of register S are logic ZERO's. When bit positions 10 and 9 also contain ZERO's it indicates that a location in bank 0 is addressed, regardless of the contents of register EBANK. When bit 10 or 9, but not both contain a ONE, a location in bank 1 or 2 is addressed regardless of the contents of register EBANK. When bit positions 10 and 9 both contain a ONE, a location is addressed in that bank, the number of which is contained in register EBANK.

4-5.8.1.1 Core Array. The core array of erasable memory has 2048 word storage locations, contained in 16 bit planes and defined by the intersection of 64 X lines and 32 Y lines. Each bit plane contains 2048 cores. An individual bit in each plane is selected by the intersection of an X and Y line threading a core. Thus, one word storage location is selected. Each core is also threaded by a sense line and an inhibit line. The sense line threads all cores in a particular bit plane, such that current is induced into the sense line if the state of any core in the plane is changed. Current through

the inhibit line prevents any core in the bit plane from switching since it opposes the current on tbe X and Y selection lines. Thus, current in a combination X, Y, and inhibit lines determines which cores are selected. Core selection is identical for both the read and write operations.

4-5.8.1.2 Erasable Memory Cycle Timing Circuits. The erasable memory cycle timing circuits consist of timing control and timing flip-flops, which generate strobe signals to sequence the operation of erasable memory. These strobe signals are generated during one memory cycle time (11.97 microseconds), subject to timing signals from the timer as shown in figure 4-194. The timing flip-flops generate the strobe signals subject to signal $\overline{\text{ERAS}}$ from the timing control. Signal $\overline{\text{ERAS}}$ is generated only when bits 11 and 12 of register S in the central processor are both ZERO's, the subinstruction commands from the sequence generator are all ZERO's, and signal SCAD is not present. Bits 11 and 12 are ZERO's when the specified memory address is lower than 2000 (octal). Signal SCAD is a ONE only when the specified address is lower than 0007. The timing control also generates signal T1MR when signal $\overline{\text{STOP}}$ (represents CTS start and stop or alarm condition) is present. Signal T1MR resets several timing flip-flops in erasable memory and inhibits the addressing of the ropes in fixed memory. Input signal MYCLMP inhibits access to memory if the +4 vdc power supply fails or the computer is in the standby mode.

The timing flip-flops generate the various strobe signals which enable the selection circuits and sense amplifiers. As previously discussed, several strobe signals are inhibited by signal T1MR and those remaining by signal GOJAM.

4-5.8.1.3 Selection Circuits. Selection signals (X and Y) from the address decoder in the central processor are applied to the top and bottom select drivers. When these drivers receive the set strobe, the selection signals are supplied to the top and bottom selection switches. The read signals (X and Y) enable the top selection switches and allow current to flow from the bottom selection switch through the core array to the top selection switches. The current flowing through the X and Y lines coincides at the addressed storage location (one core of each plane) in the core array. As a result, current is induced into the sense lines which thread those cores that switched from a ONE to a ZERO. The current on the sixteen sense lines is detected by the sense amplifiers and applied to register G when the sense strobe is generated. The selection switches remain set until the reset signals are received.

The write signals (X and Y) enable the bottom selection switches and allow current to flow from the top selection switches through the core array to the bottom selection switches. Again the current flowing through the X and Y lines coincides at the addressed location in the core array. However, during the write operation the cores in the addressed location are switched to a ONE, provided they are not also receiving current in the inhibit lines. All cores receiving inhibit current remain in a ZERO condition. Inhibit current is governed by the content of register G. There are 16 inhibit drivers, and each is connected to a bit plane. Thus, the content of register G determines which cores in a storage location are switched by the X and Y selection lines during the write operation.

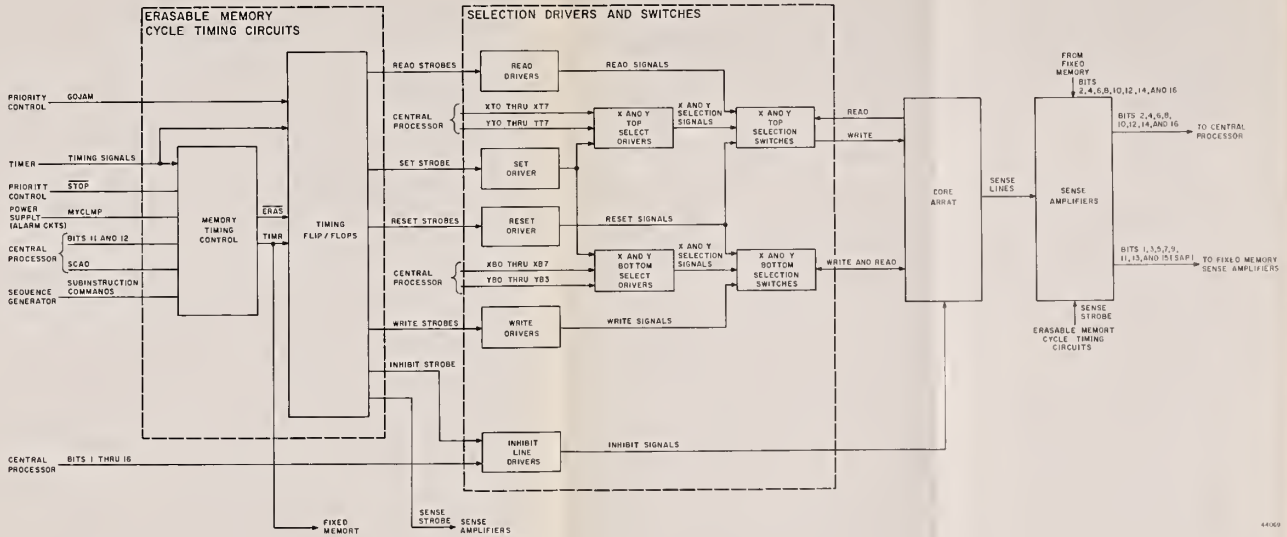


Figure 4-193. Erasable Memory, Functional Diagram

Table 4-XCVII. E Addressing

Register or Location Groups			Octal Address		EBANK	S											
			Pseudo	Real	11 10 9	12	11	10	9	8	7	6	5	4	3	2	1
CP			0000-0007	0000-0007 1400-1407	x x x 0 0 0	0 0	0 0	0 1	0 1	0 0	0 0	0 0	0 0	0 0	y y	y y	y y
Unswitched E Memory	EBANK 0	Special Locations	0010-0023	0010-0023 1410-1423	x x x 0 0 0	0 0	0 0	0 1	0 1	0 0	0 0	0 0	y y	y y	y y	y y	y y
		Counters	0024-0060	0024-0060 1424-1460	x x x 0 0 0	0 0	0 0	0 1	0 1	0 0	0 0	y y	y y	y y	y y	y y	y y
		General Use	0061-0377	0062-0377 1462-1777	x x x 0 0 0	0 0	0 0	0 1	0 1	y y	y y	y y	y y	y y	y y	y y	y y
	E-Bank 1		0400-0777	0400-0777 1400-1777	x x x 0 0 1	0 0	0 0	0 1	1 1	y y	y y	y y	y y	y y	y y	y y	y y
	E-Bank 2		1000-1377	1000-1377 1400-1777	x x x 0 1 0	0 0	0 0	1 1	0 1	y y	y y	y y	y y	y y	y y	y y	y y
Switched E Memory	E-Bank 3		1400-1777	1400-1777	0 1 1	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 4		2000-2377	1400-1777	1 0 0	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 5		2400-2777	1400-1777	1 0 1	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 6		3000-3377	1400-1777	1 1 0	0	0	1	1	y	y	y	y	y	y	y	y
	E-Bank 7		3400-3777	1400-1777	1 1 1	0	0	1	1	y	y	y	y	y	y	y	y

(1) x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

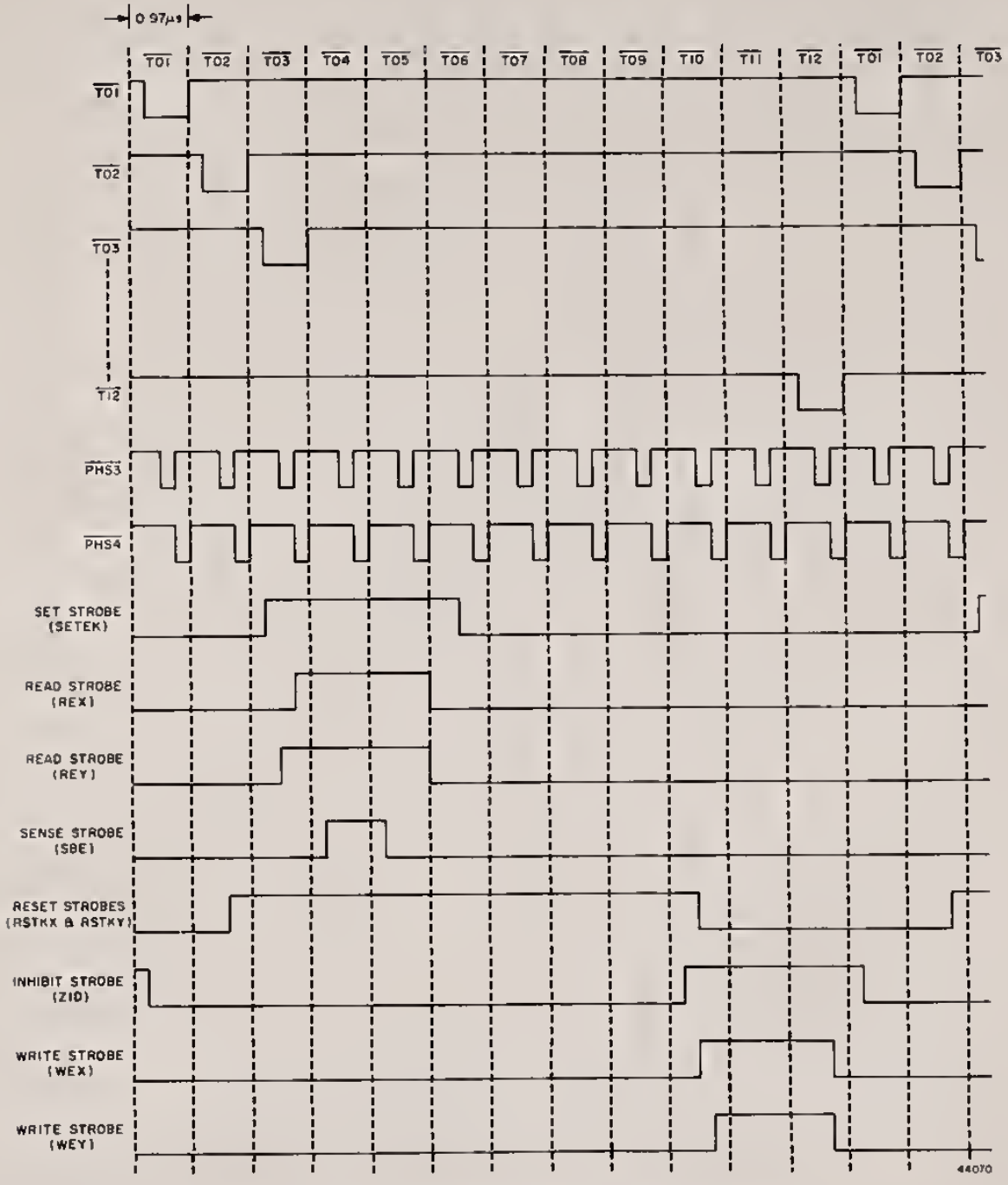


Figure 4-194. Erasable Memory Timing Diagram

Figure 4-195 is a simplified diagram of the selection circuits. Each selection signal effectively closes one top or bottom selection switch. Any one of 64 lines can be selected by closing one top and one bottom selection switch (XT and XB). Similarly any one of 32 lines can be selected by closing one top and one bottom selection switch (YT and YB). Where they intersect in the core array is the addressed location. This occurs in the same position in all sixteen bit planes of erasable memory.

4-5.8.1.4 Sense Amplifiers. There are 16 sense amplifiers in erasable memory. Each amplifier senses the content of a bit location during the read operation. The bi-polar sense signals are converted to single polarity signals and half are applied directly to tbe central processor and the other half are gated through the fixed memory sense amplifiers when the amplifiers are enabled with the sense strobe. In addition, half of the word read out of fixed memory is also gated through the erasable memory amplifiers to the central processor.

4-5.8.2 Fixed Memory Functional Description. Fixed memory (figure 4-196) consists of fixed memory cycle timing circuits, selection circuits and drivers, core ropes and return circuits, and the sense amplifiers. Memory cycle timing generates the timing signals necessary for fixed memory operation. A location in fixed memory is addressed according to the contents of registers S, FBANK, and FEXT in the central processor. The selection circuits convert the contents of registers S, FBANK, and FEXT into the various signals necessary to select the addressed storage location. The tbree core ropes, which are the storage medium for storing data in fixed memory, are designated ropes R, S, and T. A rope consists of two modules and each module contains 512 cores. Tbe sense amplifiers detect the content of the addressed storage location and supply this data through the sense amplifiers in erasable memory to the central processor.

Fixed memory is subdivided into 64 banks for addressing (table 4-XCVIII), each storing 1024 words. However, only 36 banks (00 through 43) are built into the computer, but the other 28 banks (44 through 77) can be added.

Banks 00 through 27 are referred to as FEXT - Channel X because all of tbe locations can be addressed by entering the address in registers S and FBANK without regard to what might be contained in register FEXT. All other banks, 30 through 77, may be addressed only if the correct channel number (0-3, 4, 5, 6, or 7) is contained in register FEXT.

Banks 02 and 03 are also referred to as fixed-fixed memory because the locations can be addressed by entering the proper address in register S without regard to what might be contained in register FBANK. Banks 00, 01 and 04 through 27 are also referred to as variable fixed memory, however, tbe proper bank number must be contained in register FBANK.

Fixed memory is addressed only when bit position 12 or 11, or both, of register S contain a ONE. Whenever bit position 12 contains a ONE, fixed-fixed memory is addressed, regardless of the contents of registers FBANK and FEXT. Whenever bit position 12 contains a ZERO and bit position 11 a ONE, a location is addressed in that bank whicb is defined by the contents of registers FBANK and FEXT.

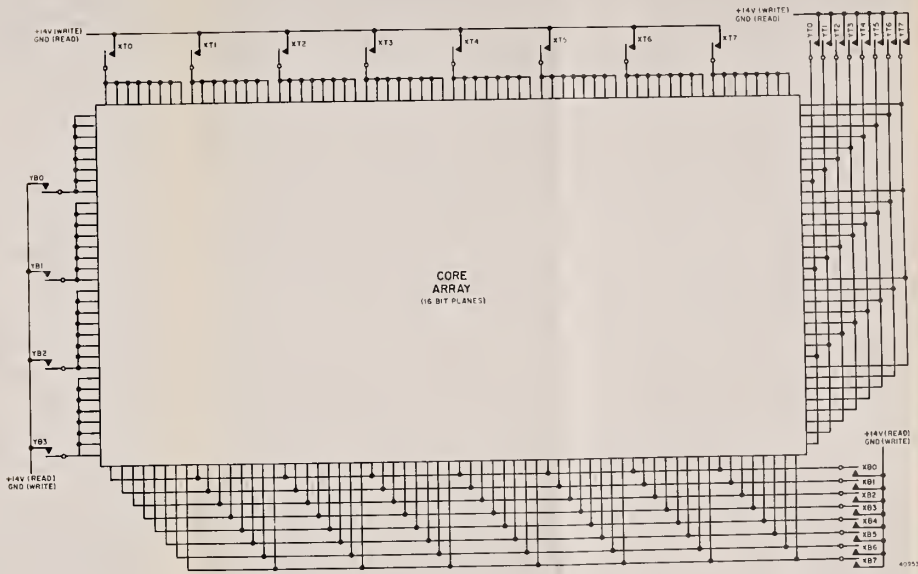


Figure 4-195. X and Y Selection, Simplified Diagram

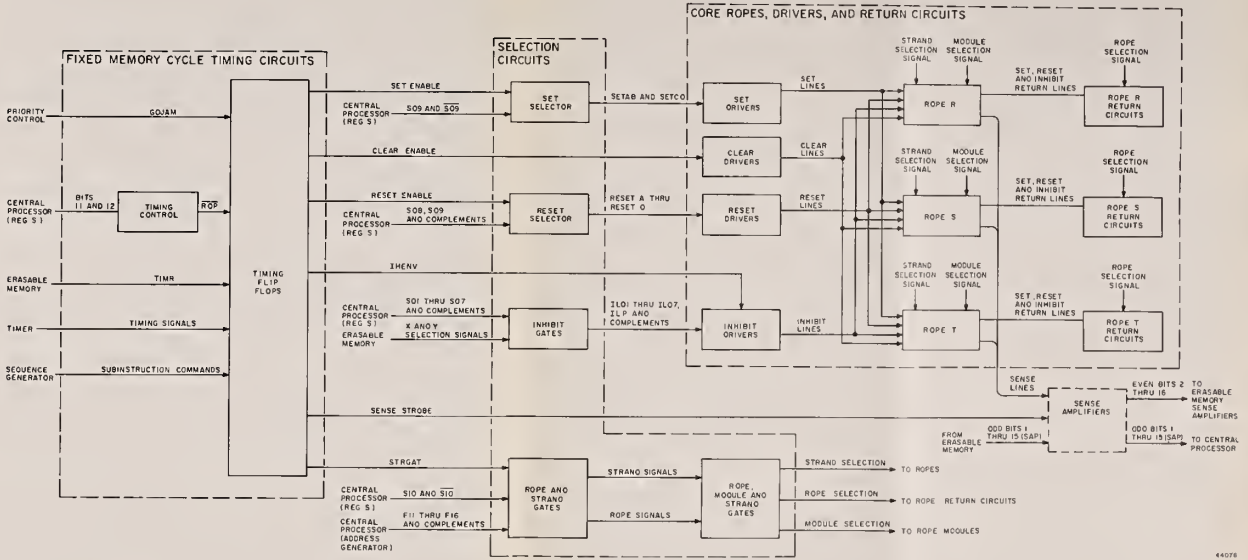


Figure 4-196. Fixed Memory, Functional Diagram

When bit positions 16 and 14 of register FBANK both contain ZERO's, or a ZERO and a ONE, bit position 12 of register S contains a ZERO, and bit position 11 a ONE, it indicates that a bank in FEXT (Channel X) is addressed, in which case the content of register FEXT is irrelevant. When bit positions 16 and 14, of register FBANK, contain ONE's, a bank in FEXT - Channel 0-3, or 4 through 77 is addressed.

4-5.8.2.1 Fixed Memory Cycle Timing Circuits. Fixed memory cycle timing consists of timing control and timing flip-flops. The timing control regulates the generation of timing signals, used for fixed memory operation, by means of signal $\overline{\text{ROP}}$. Signal $\overline{\text{ROP}}$ is generated when either bit 11 or bit 12, or both, are ONE's. Signal $\overline{\text{ROP}}$ occurs for memory addresses above 1777. The timing flip-flops generate the timing signals (figure 4-197) necessary to sequence the operation of fixed memory subject to timing signals from the timer, and subinstruction commands from the sequence generator. The timing signals generated are IHENV (enables the inhibit drivers), SET ENABLE (enables the set circuits), STRGAT (enables the rope and strand circuits), RESET ENABLE (enables the reset circuits), and SBF (enables the sense amplifiers). The generation of the inhibit and set signals is inhibited by signal TIMR from the erasable memory cycle timing circuits. The remaining timing signals are inhibited by signal GOJAM from priority control.

4-5.8.2.2 Selection Circuits and Drivers. The selection circuits generate the rope, strand, module, set, reset, and inhibit signals necessary to select an addressed storage location in fixed memory.

Set selection is accomplished by signals S09 and $\overline{\text{S09}}$ subject to the set enable timing signal. One of two set signals (SETAB or SETCD) is fed through a driver circuit and applied to the core ropes.

Reset selection is accomplished by signals S08, $\overline{\text{S08}}$, S09, and $\overline{\text{S09}}$ subject to the reset enable timing signal. One of four reset signals (RESET A, B, C or D) is fed through a driver circuit and applied to the core ropes.

Inhibit selection is divided into two parts. Signals S01 through S07 and their complements determine which of the 14 inhibit lines is activated, and the remaining two lines are activated by X and Y selection signals from erasable memory. The inhibit lines are applied to the core ropes subject to timing signal IHENV.

The rope and strand selection is accomplished by combining signals S10 and $\overline{\text{S10}}$ with signals F11 through F16 and their complements. Module selection is accomplished by combining the rope and strand selection signals.

A rope is selected by applying one of three rope selection signals to a particular rope return circuit. The sense lines threading or bypassing each core are grouped together into strands. A particular sense strand (1 of 72) is selected and applied to the core ropes. Module selection allows one module of the six in the core ropes to be activated.

Table 4-XCVIII. F Addressing

Register or Location Groups			Octal Address		FEXT	FBANK	S
			Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel X	Fixed F Memory	F-Bank 02	04000-05777	4000-5777 2000-3777	x x x x x x	x x x x x 0 0 0 1 0	1 0 y y y y y y y y y y 0 1 y y y y y y y y y y
		F-Bank 03	06000-07777	6000-7777 2000-3777	x x x x x x	x x x x x 0 0 0 1 1	1 1 y y y y y y y y y y 0 1 y y y y y y y y y y
	Variable F Memory	F-Bank 00	00000-01777	2000-3777	x x x	0 0 0 0 0	0 1 y y y y y y y y y y
		F-Bank 01	02000-03777	2000-3777	x x x	0 0 0 0 1	0 1 y y y y y y y y y y
		F-Bank 04	10000-11777	2000-3777	x x x	0 0 1 0 0	0 1 y y y y y y y y y y
		F-Bank 05	12000-13777	2000-3777	x x x	0 0 1 0 1	0 1 y y y y y y y y y y
		F-Bank 06	14000-15777	2000-3777	x x x	0 0 1 1 0	0 1 y y y y y y y y y y
		F-Bank 07	16000-17777	2000-3777	x x x	0 0 1 1 1	0 1 y y y y y y y y y y
		F-Bank 10	20000-21777	2000-3777	x x x	0 1 0 0 0	0 1 y y y y y y y y y y
		F-Bank 11	22000-23777	2000-3777	x x x	0 1 0 0 1	0 1 y y y y y y y y y y
		F-Bank 12	24000-25777	2000-3777	x x x	0 1 0 0 1	0 1 y y y y y y y y y y
		F-Bank 13	26000-27777	2000-3777	x x x	0 1 0 1 1	0 1 y y y y y y y y y y
		F-Bank 14	30000-31777	2000-3777	x x x	0 1 1 0 0	0 1 y y y y y y y y y y
		F-Bank 15	32000-33777	2000-3777	x x x	0 1 1 0 1	0 1 y y y y y y y y y y
		F-Bank 16	34000-35777	2000-3777	x x x	0 1 1 1 0	0 1 y y y y y y y y y y
		F-Bank 17	36000-37777	2000-3777	x x x	0 1 1 1 1	0 1 y y y y y y y y y y
		F-Bank 20	40000-41777	2000-3777	x x x	1 0 0 0 0	0 1 y y y y y y y y y y

⚠ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

Sheet 1 of 4)

Table 4-XCVIII. F Addressing

Register or Location Groups			Octal Address		FEXT	FBANK	S
			Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel X (cont)	Variable F Memory (cont)	F-Bank 21	42000-43777	2000-3777	x x x	1 0 0 0 1	0 1 y y y y y y y y y y
		F-Bank 22	44000-45777	2000-3777	x x x	1 0 0 1 0	0 1 y y y y y y y y y y
		F-Bank 23	46000-47777	2000-3777	x x x	1 0 0 1 1	0 1 y y y y y y y y y y
		F-Bank 24	50000-51777	2000-3777	x x x	1 0 1 0 0	0 1 y y y y y y y y y y
		F-Bank 25	52000-53777	2000-3777	x x x	1 0 1 0 1	0 1 y y y y y y y y y y
		F-Bank 26	54000-55777	2000-3777	x x x	1 0 1 1 0	0 1 y y y y y y y y y y
		F-Bank 27	56000-57777	2000-3777	x x x	1 0 1 1 1	0 1 y y y y y y y y y y
FEXT Channel 0-3		F-Bank 30	060000-061777	2000-3777	0 x x	1 1 0 0 0	0 1 y y y y y y y y y y
		F-Bank 31	062000-063777	2000-3777	0 x x	1 1 0 0 1	0 1 y y y y y y y y y y
		F-Bank 32	064000-065777	2000-3777	0 x x	1 1 0 1 0	0 1 y y y y y y y y y y
		F-Bank 33	066000-067777	2000-3777	0 x x	1 1 0 1 1	0 1 y y y y y y y y y y
		F-Bank 34	070000-071777	2000-3777	0 x x	1 1 1 0 0	0 1 y y y y y y y y y y
		F-Bank 35	072000-073777	2000-3777	0 x x	1 1 1 0 1	0 1 y y y y y y y y y y
		F-Bank 36	074000-075777	2000-3777	0 x x	1 1 1 1 0	0 1 y y y y y y y y y y
		F-Bank 37	076000-077777	2000-3777	0 x x	1 1 1 1 1	0 1 y y y y y y y y y y

⚠ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

Table 4-XCVIII. F Addressing

Register or Location Groups		Octal Address		FEXT	FBANK	S
		Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel 4	F-Bank 40	100000-101777	2000-3777	1 0 0	1 1 0 0 0	0 1 y y y y y y y y y y y
	F-Bank 41	102000-103777	2000-3777	1 0 0	1 1 0 0 1	0 1 y y y y y y y y y y y
	F-Bank 42	104000-105777	2000-3777	1 0 0	1 1 0 1 0	0 1 y y y y y y y y y y y
	F-Bank 43	106000-107777	2000-3777	1 0 0	1 1 0 1 1	0 1 y y y y y y y y y y y
	F-Bank 44	110000-111777	2000-3777	1 0 0	1 1 1 0 0	0 1 y y y y y y y y y y y
	F-Bank 45	112000-113777	2000-3777	1 0 0	1 1 1 0 1	0 1 y y y y y y y y y y y
	F-Bank 46	114000-115777	2000-3777	1 0 0	1 1 1 1 0	0 1 y y y y y y y y y y y
FEXT-Channel 5	F-Bank 47	116000-117777	2000-3777	1 0 0	1 1 1 1 1	0 1 y y y y y y y y y y y
	F-Bank 50	120000-121777	2000-3777	1 0 1	1 1 0 0 0	0 1 y y y y y y y y y y y
	F-Bank 51	122000-123777	2000-3777	1 0 1	1 1 0 0 1	0 1 y y y y y y y y y y y
	F-Bank 52	124000-125777	2000-3777	1 0 1	1 1 0 1 0	0 1 y y y y y y y y y y y
	F-Bank 53	126000-127777	2000-3777	1 0 1	1 1 0 1 1	0 1 y y y y y y y y y y y
	F-Bank 54	130000-131777	2000-3777	1 0 1	1 1 1 0 0	0 1 y y y y y y y y y y y
	F-Bank 55	132000-133777	2000-3777	1 0 1	1 1 1 0 1	0 1 y y y y y y y y y y y
	F-Bank 56	134000-135777	2000-3777	1 0 1	1 1 1 1 0	0 1 y y y y y y y y y y y
	F-Bank 57	136000-137777	2000-3777	1 0 1	1 1 1 1 1	0 1 y y y y y y y y y y y

⚠ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

Table 4-XCVIII. F Addressing

Register or Location Groups		Octal Address		FEXT	FBANK	S
		Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel 6	F-Bank 60	140000-141777	2000-3777	1 1 0	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 61	142000-143777	2000-3777	1 1 0	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 62	144000-145777	2000-3777	1 1 0	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 63	146000-147777	2000-3777	1 1 0	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 64	150000-151777	2000-3777	1 1 0	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 65	152000-153777	2000-3777	1 1 0	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 66	154000-155777	2000-3777	1 1 0	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 67	156000-157777	2000-3777	1 1 0	1 1 1 1 1	0 1 y y y y y y y y y y
FEXT-Channel 7	F-Bank 70	160000-161777	2000-3777	1 1 1	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 71	162000-163777	2000-3777	1 1 1	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 72	164000-165777	2000-3777	1 1 1	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 73	166000-167777	2000-3777	1 1 1	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 74	170000-171777	2000-3777	1 1 1	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 75	172000-173777	2000-3777	1 1 1	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 76	174000-175777	2000-3777	1 1 1	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 77	176000-177777	2000-3777	1 1 1	1 1 1 1 1	0 1 y y y y y y y y y y

⚠ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

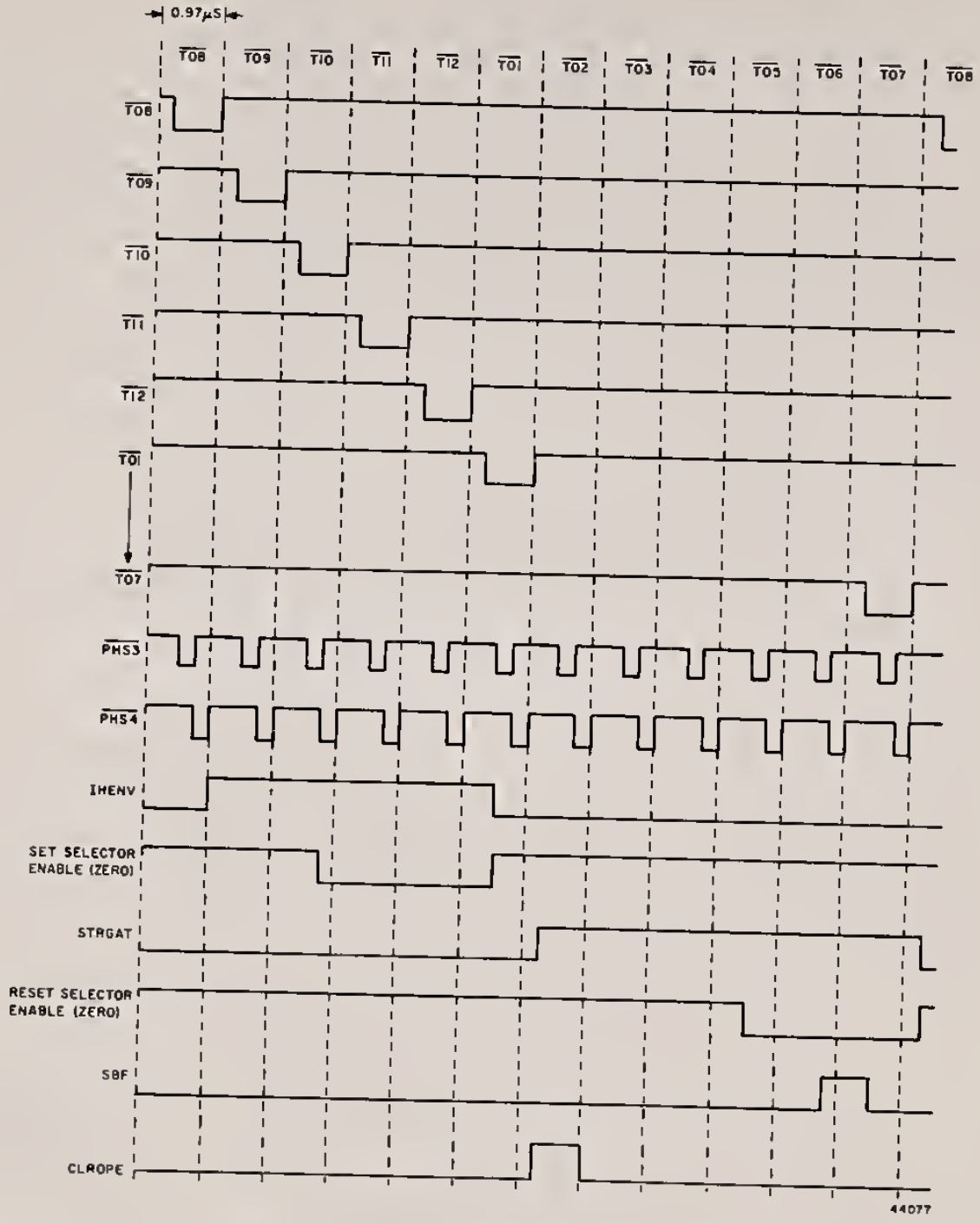


Figure 4-197. Fixed Memory, Timing Diagram

4-5.8.2.3 Core Ropes and Return Circuits. The drive lines (2 set, 4 reset, and 16 inhibit) threading the three ropes are connected in parallel, but return to three separate rope return circuits. Thus, a particular rope is selected by enabling the appropriate rope return circuit. This enabling occurs when one of three rope selection signals is received. At the same time, one of the two modules in a rope will be enabled by a module selection signal.

A strand consists of 16 sense lines (one per bit) and there are 12 strands per module for a total of 72 strands in fixed memory. However, only one strand select signal is present at a time. The 12 strands thread or bypass all cores in a module. Therefore, when a strand select signal is present, one word (one of twelve) of each core in a module is conditioned.

The combination of the inhibit, set, and reset lines are then used to select one core of the 512 cores in a module. During reset time the selected word is detected and amplified by 16 sense amplifiers which are enabled by signal SBF.

4-5.8.2.4 Sense Amplifiers. As in erasable memory, there are 16 sense amplifiers in fixed memory. Each amplifier amplifies the data on the selected sense line and forwards the data through the erasable memory sense amplifiers, when enabled by timing signal STROBE.

4-5.8.3 Erasable Memory Detailed Description. The functional presentation of the core array, timing circuits, selection circuits, and the sense amplifiers in erasable memory is detailed in the following paragraphs.

4-5.8.3.1 Core Array. The core array (figure 4-198) contains 16 bit planes. Each bit plane consists of 2048 cores arranged in 64 columns and 32 rows. An individual bit is selected by the intersection of X selection lines (XT, XB) and Y selection lines (YT, YB) threading a core. The selection lines are threaded through the cores so one core on each bit plane is selected by a given X-Y combination. Each core selected is in the same location in every bit plane, that is, at the intersection of the X and Y selection lines carrying current. The location of the line intersection is determined by addressing through the selection circuits. The 16 selected cores, one per bit plane, constitute a word storage location. The direction in which current flows through the lines determines whether data is being written into or read out of a selected core.

In addition to the X and Y lines, each core in a bit plane (figure 4-199) is threaded by an inhibit line and a sense line. Current through the inhibit line is in opposition to the X and Y selection currents and prevents all unselected cores in the bit plane from being switched since it cancels one-half the selection current. Current is induced into the sense line if the state of any core is changed from a ONE to a ZERO; no current is induced if the core is already in a ZERO state. The sense lines are connected to 16 amplifiers, each amplifying the current in a sense line and providing the power necessary to write ONE's into register G of the central processor. In this manner the contents of an erasable memory location are detected.

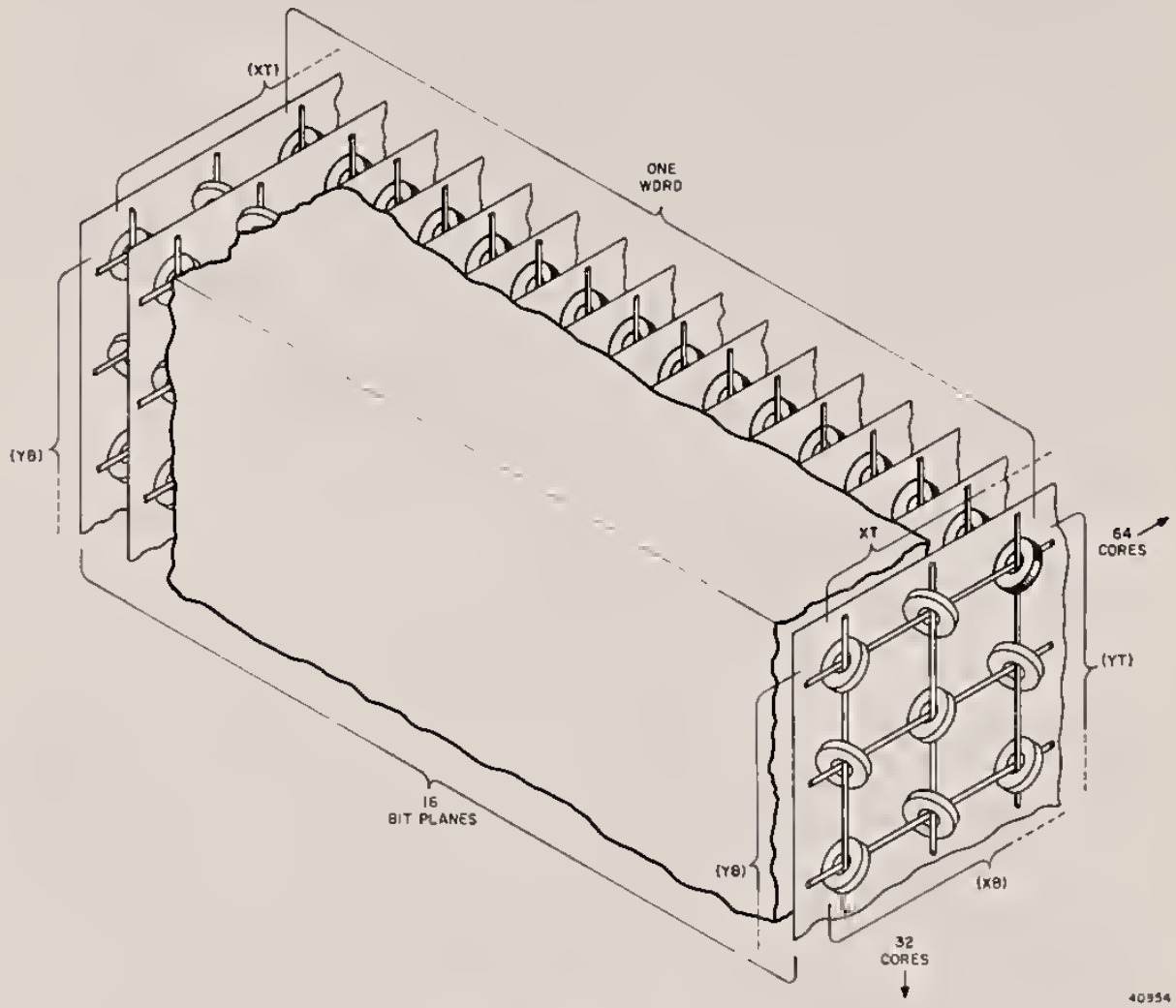


Figure 4-198. Core Array

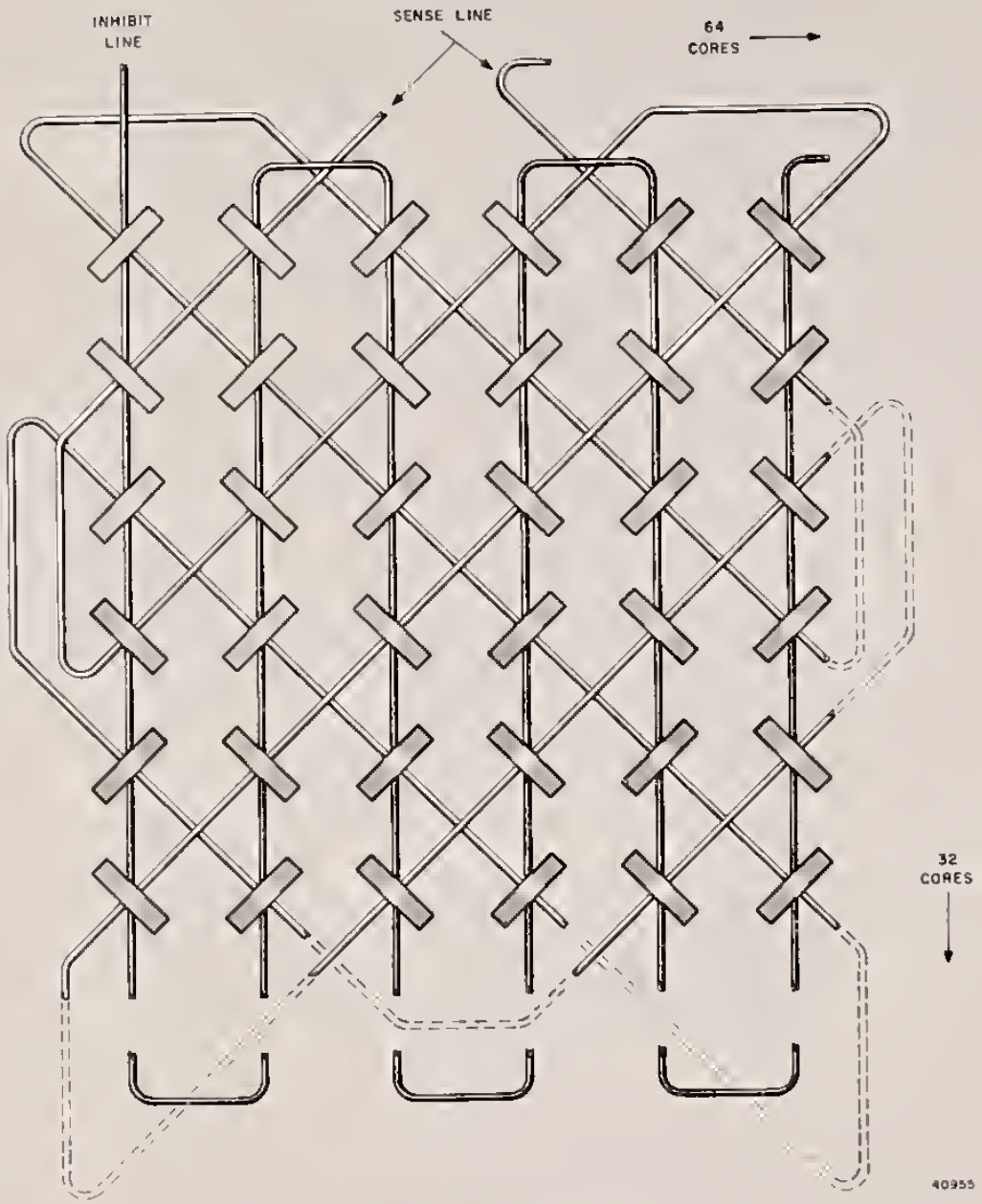


Figure 4-199. Bit Plane

Before a storage location in erasable memory is written into, the location must be cleared. This is accomplished by applying reset signals to the selection switches. All the cores of the addressed location which are in the ONE state will change to the ZERO state; all other cores in the ZERO state remain in that state. When the particular storage location is written into, current is sent through the X and Y selection lines as previously discussed but in the opposite direction. A current also is fed into the inhibit lines of all bit planes in which no ONE is to be written, i.e., where a ZERO should remain in a particular core. At write time several different current conditions exist for the various cores. Whenever a core is intersected by only one selection line (X or Y), the core remains in its existing state. Whenever a core is intersected by one selection line (X or Y) and an inhibit line, the effects of both currents cancel, and the core remains in its existing condition. Whenever a core is intersected by two selection lines (one X line and one Y line) and an inhibit line, the net effect of all three currents is equal to the effect of a single select current (passing through a core of an addressed location which has been cleared), and the core remains in the ZERO state. Only if a core is intersected by two selection lines (one X line and one Y line) but not an inhibit line will a core change from the ZERO to the ONE state. In this manner a 16-bit word is entered into erasable memory.

4-5.8.3.2 Erasable Memory Cycle Timing. Erasable memory cycle timing (figure 4-200) consists of several flip-flop circuits, which produce the timing signals for erasable memory. These timing signals (refer to figure 4-197) are produced in one memory cycle time (T01 through T12). Bits 11 and 12 (S11 and S12) from register S are logical ZERO's when erasable memory is addressed. This condition, coincident with subinstruction command signals TCSAJ3, 1NOUT, CHINC, and GOJ1, produces gating signal $\overline{\text{ERAS}}$. The generation of $\overline{\text{ERAS}}$ allows the flip-flops associated with signals SETEK, SBE, REY and REX to be set at the times indicated.

The set strobe (SETEK) is initiated by timing signal $\overline{\text{T03}}$ and is terminated when signals $\overline{\text{T06}}$ and $\overline{\text{PHS3}}$ are coincident. Signal SETEK conditions the core selection switches to be addressed. The flip-flop formed by gates 42246 and 42247 produces strobe signal SBE which enables the sense amplifiers to supply data to register G. The flip-flop is set by signals $\overline{\text{T04}}$ and SCAD. Signal SCAD is a logical ZERO when a flip-flop register is not being addressed. The SBE flip-flop is reset by timing signal T05. Read strobes REX and REY enable data to be read out of memory. Read strobe REX is generated when signals $\overline{\text{T03}}$ and $\overline{\text{PHS3}}$ are coincident. Read strobe REY is generated when signals $\overline{\text{T03}}$ $\overline{\text{PHS4}}$ are coincident. Both are terminated (REDRST) when T05 and PHS3 are coincident. The flip-flops associated with signals SETEK, SBE, REY, and REX are also reset by signal FOJAM. In addition signal SETEK may be inhibited by signal MYCLMP.

The generation of signal $\overline{\text{FNERAS}}$ from flip-flop gates 42225 and 42226, when signals $\overline{\text{ERAS}}$ and T05 are coincident, allows the flip-flops associated with signals WEX, WEY, RSTKX, RSTKY, and ZID to be set at the times indicated.

The write strobes WEX and WEY enable data to be written into memory. Write strobe WEX is generated when signals $\overline{\text{T10}}$ and $\overline{\text{PHS3}}$ are coincident. Write strobe WEY is generated when signals $\overline{\text{T10}}$ and $\overline{\text{PHS4}}$ are coincident. Both are terminated when signals $\overline{\text{T12}}$ and $\overline{\text{PHS3}}$ are coincident. The reset strobes $\overline{\text{RSTKX}}$ and $\overline{\text{RSTKY}}$ are produced simultaneously when signals $\overline{\text{T10}}$ and $\overline{\text{PHS3}}$ are coincident. These signals enable the reset drivers, thereby clearing the addressed memory location prior to

writing in data. The reset strobe flip-flop, consisting of gates 42218 and 42219, is reset when signals $\overline{PHS4}$ and $\overline{T02}$ are coincident. The inhibit strobe (ZID) gates the inhibit drivers at $\overline{T10}$ time. Signal ZID is terminated at T01 time. In addition, signal ZID may be inhibited by signal MYCLMP. The flip-flops which produce the write, reset, and inhibit strobes are reset by signal TIMR. Signals STRT2, $\overline{STOP}$, and timing signals P01, P04, and $\overline{P05}$ control the generation of TIMR, to ensure the signal is not generated until after the completion of the strobes.

4-5.8.3.3 Selection Circuits. As previously stated, information is written into and read out of a storage location by means of core selection. There are 64 X coordinates and 32 Y coordinates (figure 4-201). Combinations of control signals XT, SB, YT, and YB set the proper selection switches (figure 4-202) and allow 16 cores (one in each plane) to be selected. Figure 4-202 illustrates the selection switches and their associated index circuits. Since X and Y operations function the same, only one set of selection switches (X bottom and X top) and their associated drivers (X bottom, X top, X read, X write, and X reset) is discussed. Signal names and pin numbers for circuits other than those discussed may be found on figure 4-202.

The set strobe driver acts as a power switch for the bottom and top select drivers by supplying +14 volts to the drivers. Signal SETEK forces transistor Q4 to conduct, which causes transistors Q5, Q6, and Q7 to conduct. When Q6 and Q7 conduct, +14 volts are supplied to the collectors of transistors Q13 and Q14, causing both to conduct.

Since the read and write drivers operate in the same manner only the write driver is discussed. Input signal WEX causes transistor Q10 to conduct which in turn causes Q11 and Q12 to conduct. Resistors R17 and R27, and diodes CR10, CR11, CR27, and CR28 stabilize the base current on transistor Q12. The collector current of transistor Q12 is controlled by inductor L3.

The reset driver supplies a path for current through winding D of the selection switches to reset the cores. Signal $\overline{RSTKX}$ holds transistor Q8 off allowing transistor Q9 to conduct. Diodes CR5, CR6, and CR7 maintain a constant voltage on the base of Q9, which provides a constant output current.

Each selection switch contains a ferrite selection core with four windings, two of which are connected to power transistors. Transistor Q3 of the X bottom select switch and transistor Q55 of the X top select switch form a path for read current. Transistors Q4 and Q56 form a path for write current. In order to generate a current on the X selection line, the selection switches and drivers must be energized.

Transistor Q3 in the bottom select driver conducts, through winding A of core T2, only if control signal XB0E is present and signal SETEK is supplied to the set strobe driver. Current flowing through the A winding and Q14 changes the state of T2 so a current is induced in winding B, which causes transistor Q3 of the bottom selection switch to conduct and transistor Q4 to be cut off. In a similar manner another control signal XT0E causes Q18 of the top select driver to conduct and transistor Q13 changes the state of T28. As T28 switches, transistor Q55 is forced to conduct and transistor Q56 is cut off. At the time that transistor Q3 and Q55 are conducting and signal REX

is applied to the X read driver, read current flows from +14 volts (through transistor Q3 in the bottom selection switch, the core array, transistor Q55 in the top selection switch, and transistor Q12 in the read driver) to 0 vdc.

Generation of a write current is similar to generation of a read current. Signal $\overline{\text{RSTKX}}$ enables the reset driver, which allows current to flow through winding D of both selection switches. Current through winding D resets cores T2 and T28, which in turn induces current in both C windings causing transistors Q4 and Q56 to conduct and transistors Q3 and Q55 to cut off. At the same time signal WEX enables the write driver. A current path is provided from +14 volts (through transistor Q56, the core array, transistor Q4, and transistor Q12 in the write driver) to 0 vdc.

The inhibit line drivers prevent the setting of a core in erasable memory when a ZERO is to be written into a bit location. In order to address a storage location, 16 inhibit line drivers are required, one per bit plane. Each driver (figure 4-203) receives a +14 volts signal (40017A) when inhibit strobe ZID occurs from memory cycle timing, and one bit (GEM01 through 16) from register G. During the write operation ZID initiates a power switching action similar to that of the set strobe driver and +14 volts are applied to the collectors of transistors Q1 and Q2. If the input from register G is a logic ONE, Q1 conducts and inhibits Q2 and Q3. This prevents current from flowing through the inhibit line and the addressed core can be switched to the ONE state. When the input is a logic ZERO, Q1 is kept off allowing Q2 and Q3 to conduct. When transistor Q3 conducts, a path is provided for the inhibit current which prevents the switching of the addressed core.

4-5.8.3.4 Sense Amplifiers. Sixteen sense amplifiers are associated with erasable memory. Each sense amplifier (figure 4-204) accepts bipolar signals SAF01 through 16 and SBF01 through 16 from the core array sense lines. For simplification only circuit 40607 will be discussed. When a core is reset, a current is induced in the sense lines and applied to transformer T1 (signals SAF01 and SBF01). The output of T1 is applied to a differential amplifier consisting of transistors Q1 and Q2 (SA1). Base bias voltage VZE is applied to the bases of Q1 and Q2 through resistors R1 and R2. Transistor Q3 is a constant-current source for the differential amplifier and establishes the dc operating point. Voltage VXE establishes the bias for transistor Q3. The output from the differential amplifier is OR'ed at the bases of a threshold detector consisting of Q5 and Q6. The collector of Q2 supplies the base input of Q5, and the collector of Q1 supplies the base input of Q6. This produces a single polarity output, even though the input waveform is bipolar. The threshold for Q5 and Q6 is set by voltage VYE1 which is connected to the emitters of Q5 and Q6. Transistors Q5 and Q6 can not be switched on unless the base drive exceeds a predetermined level established by VYE1. Sense amplifier output 406011A is fed to the fixed memory sense amplifiers by strobing Q4 with signal STROBE from the strobe driver. Signal 406011A, in fixed memory sense amplifier circuits, will be applied to a transistor identical to emitter follower Q1 and out to register G. Signals SAF02 and SBF02 goes through an identical operation in SA2 except the output isytrobed through emitter follower Q1 and applied directly to register G. Thus, for erasable memory sense amplifier operation, register G will receive 8 bits from the sense amplifiers in erasable memory and 8 bits from the fixed memory sense amplifiers.

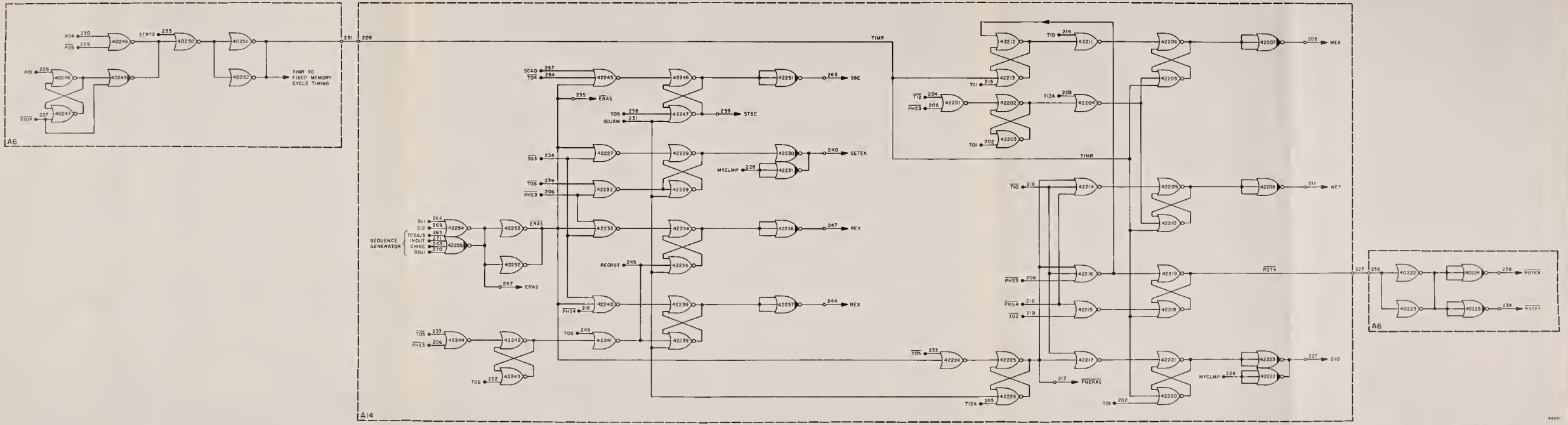


Figure 4-200. Memory Cycle Timing, Erasable

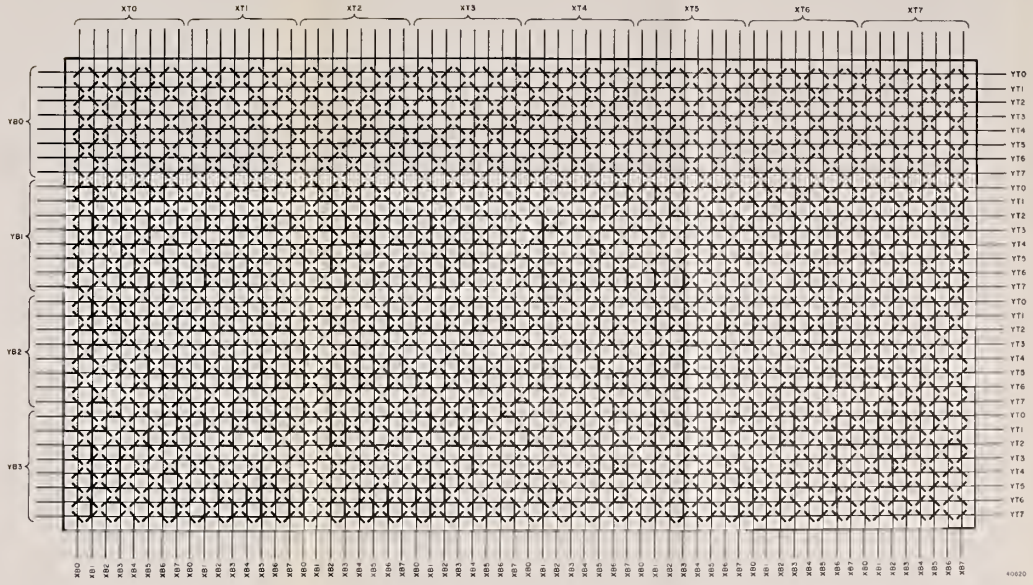


Figure 4-201. X and Y Coordinates

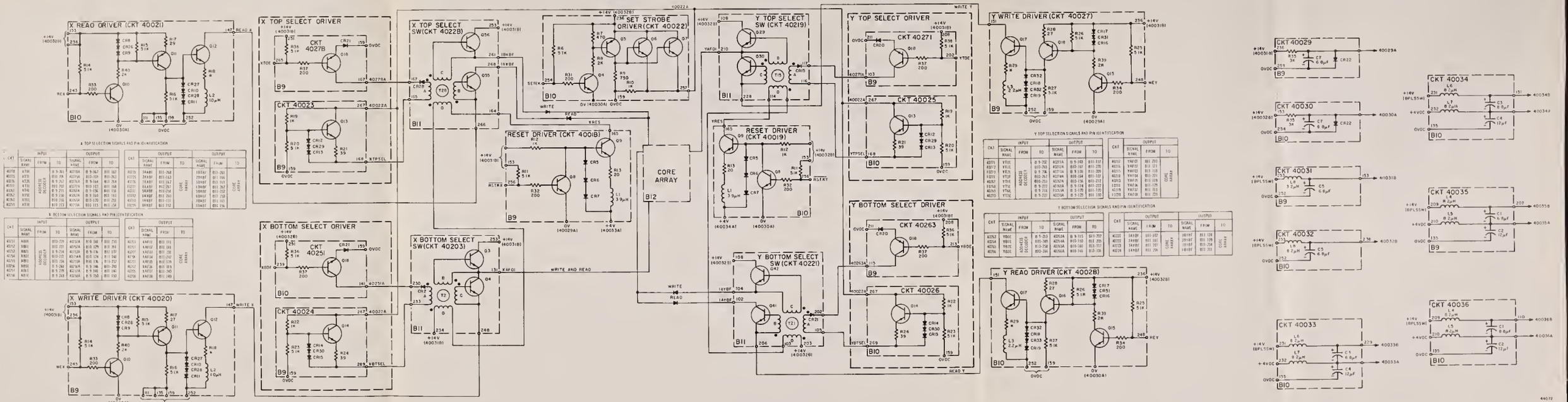


Figure 4-202. Selection Switches and Drivers

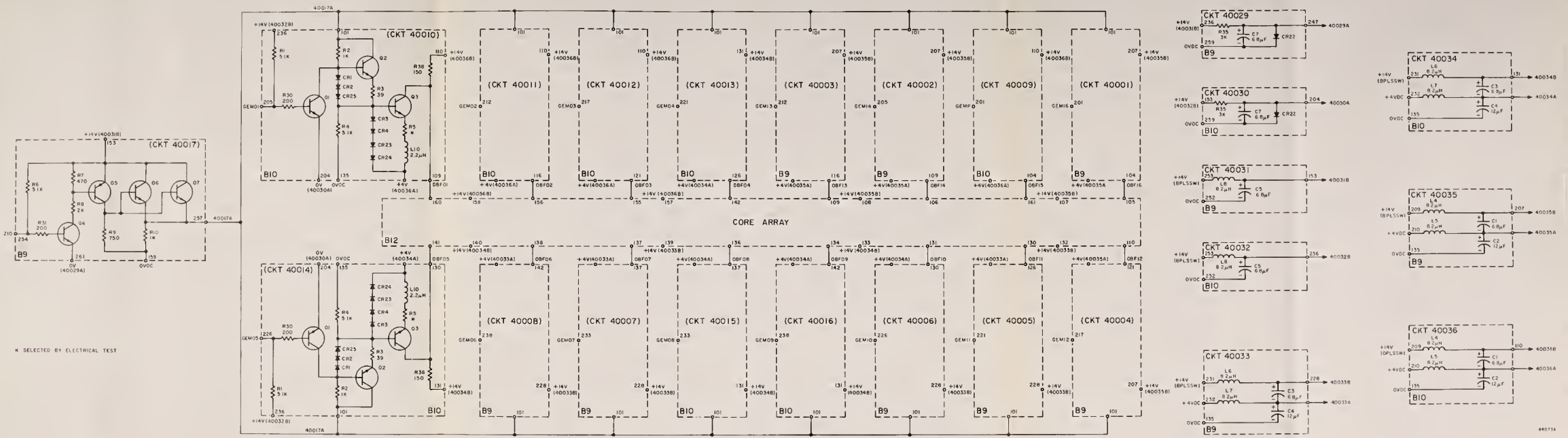


Figure 4-203. Inhibit Line Drivers

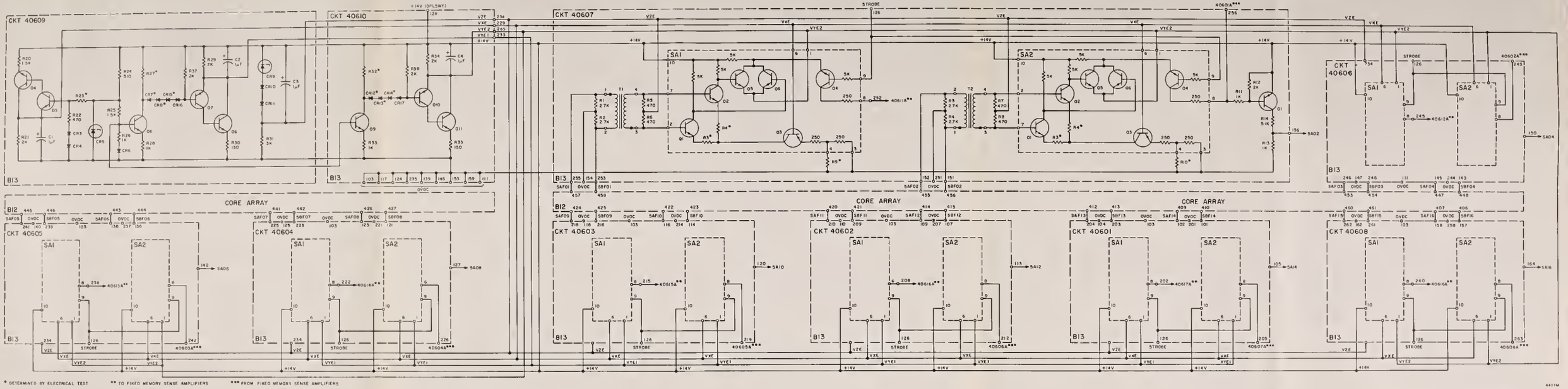
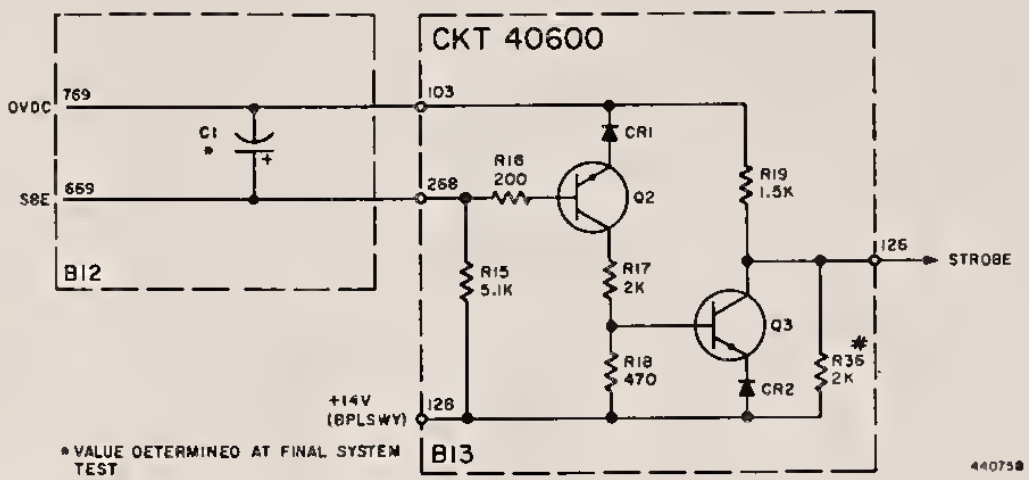


Figure 4-204. Sense Amplifier and Voltage Source

Voltages VXE, VYE1, VYE2, and VZE, which are required for sense amplifier operation, are provided by a constant voltage source (circuits 40609 and 40610). Base bias voltage VZE is maintained at a constant value by zener diode CR9, diodes CR10 and CR11, and resistor R31. Zener diode CR5, diodes CR3 and CR4, and resistor R23 set the operating point for voltage VXZ. The value of VYE1 is kept relatively constant by diodes CR7, CR8, CR15, and CR16, and resistors R27 and R37. The value of VYE2 is controlled by diodes CR12, CR13, CR14, and CR17 and resistors R32 and R38.

The strobe driver (figure 4-205) receives erasable memory strobe signal SBE from the memory cycle timing circuits. The strobe signal is amplified and supplied to the appropriate sense amplifiers as signal STROBE. This signal enables data to be transferred from the sense amplifiers to the fixed memory sense amplifiers or register G.

Capacitor C1, which is determined at factory final electrical test, adjusts the timing of the erasable memory strobe signal. As a result of this change, modules B12 (erasable memory), B13 (sense amplifier), and B9, B10 (erasable driver) become a matched set of modules. The above modules cannot be replaced or interchanged without repeating the nominal selection procedure performed at factory final electrical test.



#In module P/N 2003982-031 and above, R36 is replaced by zenner diode CR18.

Figure 4-205. Strobe Driver, Erasable

4-5.8.4 Fixed Memory Detailed Description. Fixed memory is a nondestructive, random-access storage device. Data is wired into fixed memory; therefore, it cannot be altered electrically. Fixed memory consists of core ropes, memory cycle timing, selection circuits, driver and return circuits, and sense amplifiers.

4-5.8.4.1 Core Ropes. A core rope is a storage device in which information is stored by wiring the cores in a unique manner. There are three core ropes R, S, and T (mdoules B1 and B2, B3 and B4, and B5 and B6, respectively) in fixed memory. Each core rope module contains four 128-core planes for a total of 512 cores in a rope module.

Each core in a rope module stores twelve 16-bit words. Thus, a total storage capacity of 36,864 sixteen bit words is provided by fixed memory. A core is threaded or bypassed by set, reset, inhibit, and sense lines (one per bit). In addition, each core in fixed memory is threaded by a clear rope signal. The effect of currents passing through a core through the set, reset, and inhibit lines is additive. The currents in the set lines and the inhibit lines are of opposite polarity; therefore, the set current is cancelled by the inhibit current when the currents are time-coincident. Thus, a core changes state at set time if none of the inhibit lines tbreading the core are carrying current. When a core changes state, current is induced into all the sense lines threading the core. The sense lines bypassing the core receive no current. In this manner the sense lines associated with each core receive the same words each time the core is set. A core is reset when current flows througb the reset line. Also at reset time, a 16 bit word is read out of memory by enabling the sense amplifiers.

If the program in progress is working with fixed memory and it wishes to switch operation to erasable memory, such as to compare information, both fixed and erasable information may be present on the write lines. To eliminate this, a clear rope signal appears when the switching action takes place and prevents further transfer of information out of fixed memory.

Inhibit signals IL01 through IL07 and their complements are sufficient to select one core in each plane. A core is selected by inhibiting all but one core in each plane. Inhibit signals ILP and $\overline{\text{ILP}}$ ensure that all but the selected core are inhibited by at least two signals and thus the noise in the sense lines is reduced.

Two set lines thread each core rope, and each set line threads all cores of two planes in each rope module. Only one set signal is present at set time, and that signal is selected by address.

Four reset lines thread each core rope, and each reset line threads all cores of one plane in each rope module. Only one reset signal is present at reset time, and that signal is also selected by an address.

One clear line threads all cores in a core rope. All three clear lines are present when enabled by the clear enable signal from the fixed memory cycle timing circuits.

The sense lines tbreading or bypassing each core are grouped into strands. A strand consists of the sense lines necessary to detect one 16-bit word. There are 12 strands per rope module, for a total of 72 strands in fixed memory. With the application of a module select signal (one of six) and a strand select signal (one of twelve) a particular strand (one of seventy two) is selected.

4-5.8.4.2 Fixed Memory Cycle Timing. Fixed memory cycle timing (figure 4-206) consists of several flip-flops and gates which produce the timing signals necessary to perform the set, reset, inhibit, and sensing functions in fixed memory. As in erasable memory, all the timing pulses are generated in one memory cycle time (11.97 μsec). A logic ONE in either bit position 11 or 12, or both, indicates that fixed memory is addressed. This condition produces rope condition signal $\overline{\text{ROP}}$. Signal $\overline{\text{ROP}}$ must be present to generate all fixed memory timing signals except signal CLROPE which will only be present when signal ROP is equal to a logic ONE.

The waveforms for fixed memory cycle timing are illustrated in figure 4-197. At time 8, when slgnals T08 and PHS3 are coincident, signal IHENV is generated. It is present until flip-flop 42107-42109 is reset which occurs when signals $\overline{\text{T01}}$ and $\overline{\text{PHS3}}$ are coincident. Signal IHENV enables the inhibit drivers in the driver and return circuits to allow inhibit current to flow through tbe selected inhibit line. When signals $\overline{\text{T10}}$ and $\overline{\text{PHS4}}$ are coincident flip-flop 42112-42111 is set and generates the set selector enable signal which is used for conditioning the set selector gates. This signal is also terminated when signals $\overline{\text{T01}}$ and $\overline{\text{PHS3}}$ are coincident. The reset selector enable signal is generated wben signals $\overline{\text{T05}}$ and $\overline{\text{PHS3}}$ are coincident and terminated at time 8. It is used for conditioning the reset selector gates. At time $\overline{\text{T02}}$ flip-flop 42145-42146 ls set and generates signal STRGAT which is used for conditioning the strand selector gates. It is terminated by signal T08. When signals $\overline{\text{T06}}$, $\overline{\text{PHS4}}$, DV3764, and MP1 are coincident, flip-flop 42123-42124 will be set and will generate signal SBF which, in turn, will enable the sense amplifiers. Signal SBF is terminated when signals $\overline{\text{T07}}$ and $\overline{\text{PHS3}}$ are coincident.

When signals $\overline{\text{ROP}}$ and $\overline{\text{T10}}$ are coincident, FF 42155-42156 will be set and at time $\overline{\text{T02}}$ when signal $\overline{\text{ROP}}$ is a logic ONE, gate 42148 will yield a ONE and set FF 42150-42151, which will generate signal CLROPE. At time T03, FF 42155-42156 will be reset, and through gates 42148 and 42149, signal CLROPE will become a logic ZERO; FF 42150-42151 is reset by timing signal T06. Thus, signal CLROPE is only generated when fixed memory is not being addressed.

The flip-flops which produce the set selector enable signal and signal IHENV can also be reset by signal T1MR from the erasable memory cycle timing circuits. All other timing signals can also be reset by signal GOJAM.

4-5.8.4.3 Selection Circuits. The selection circuits convert the contents of register S and the address generator, in the central processor, into the various signals necessary to select the addressed storage location.

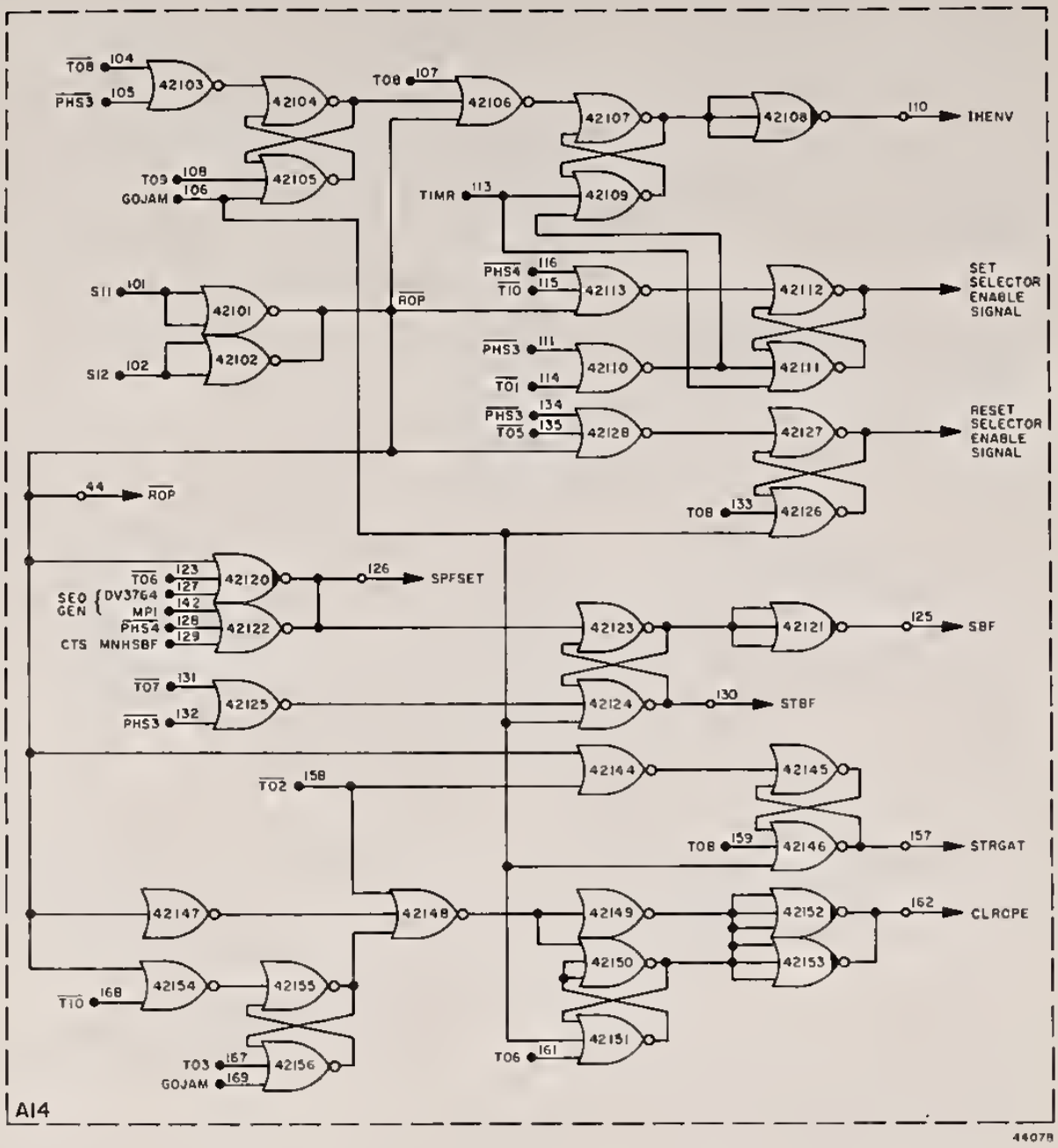


Figure 4-206. Memory Cycle Timing, Fixed

The seven low-order bits (ST01 through ST07) of register S and their complements are inverted by the inhibit gates (figure 4-207) and are applied to the inhibit lines through driver circuits. The combination of XB, YB, and XT selection signals control the generation of the parity inhibit signal (1LP) and its complement (figure 4-207). The parity inhibit lines thread the cores, through driver circuits, to reduce noise in the sense lines.

The set and reset selector (figure 4-208) gates signals S08 and $\overline{S08}$ from register S with signals S09 and $\overline{S09}$, also from register S, and the set and reset enabling signals from fixed memory cycle timing. The various combinations will yield one of two set signals (SETAB or SETCD) and one of four reset signals (RESETA, RESETB, RESETC, or RESETD). The selected set and reset signals are applied to their respective set and reset lines through driver circuits.

The strand, module, and rope selector gates (figure 4-209) receive signals S10 and $\overline{S10}$ from register S and signals F11 through F16 and their complements from the address generator. Subject to timing signal STRGAT, one of four signals (STR412, STR311, STR210, or STR19) will be generated. By combining one of these four signals with one of three other signals (STR14, STR58, or STR912), a single strand (one of twelve) will be selected. The module selector gates will generate one of two signals (LOMOD or HIMOD) which, along with one of three rope selection signals (ROPER, ROPRS, or ROPET), will select one of six modules. The actual selection takes place in the strand and module selection circuits.

Since 72 strands are in fixed memory and 12 strands thread each rope module, a selection system is required to select the proper rope module and strand to read out data. This selection process is performed by the strand and module selection circuits (figure 4-210). Three identical strand selector circuits eacb contain four gates. Each gate receives one of four signals (SE19, SE210, SE311 or SE412) and each selector circuit receives one of three signals (STR14, STR58, or STR912). This 3 by 4 combination selects the proper strand from among 12 possibilities. In addition, there are two identical module selector circuits each containing three gates. Each gate receives one of three rope selection signals (RPR, RPS, or RPT) and a module selector receives either signal LOMOD or HIMOD. This 2 by 3 combination selects the proper module from 6 possibilities. This 6 by 12 combination (module and strand) selects the proper strand from the 72 possibilities that make up fixed memory. For simplification, only circuits 40611, 40601, 40615, and 40631 are discussed. Assuming STR19 (circuit 40611) to be a logic ONE, transistor Q7 will conduct which results in signal SE19 (0 vdc) being applied to the three strand selectors. If signal STR14 (circuit 40601) is a logic ONE, transistors Q1 and Q2 will conduct and supply +14 volts to diodes CR2 through CR5. With signal SE19 a logical ZERO, transistor Q3 conducts and strand STR01 is selected. Thus, STR01 is applied to the six rope modules (B1 through B6). Assuming signal ROPER (circuit 40615) to be a logic ONE, signal RPR (0 vdc) is applied to the two module selectors. If signal LOMOD (circuit 40631) is a logic ONE, transistors Q8 and Q9 conduct and supply +14 volts to diodes CR8, CR12, and CR16. With signal RPR a logic ZERO, transistor Q10 conducts which causes transistor Q11 to conduct and apply 0 vdc as signal MODR1 to module B1. Thus, a return path is provided for strand STR01 but only in module B1. Signals RPR, RPS, and RPT are also used in the driver and return circuits.

4-5.8.4.4 Driver and Return Circuits. The set, reset, and inhibit lines threading or bypassing the three ropes are connected in parallel, but return to three separate rope return circuits (figure 4-196). Each line is driven by a separate driver circuit and all lines which are common to a particular rope are returned to an associated circuit. There are 16 inhibit drivers, 2 set drivers, and four reset drivers.

The 16 inhibit drivers (figure 4-211) are enabled subject to signals IL01 througb 1L07, ILP, and their complements, and signals 40331A and 40332A (+14 vdc). Signal 40331A (circuit 40331) is generated subject to timing signal IHENV. Input signal IHENV turns transistor Q19 on which, in turn, causes transistor Q20 to conduct and supply +14 vdc to the base of emitter follower Q21. The output of Q21 (40331A) is supplied to eight inhibit drivers. Operation of circuit 40332 is identical. Signal 40332A (+14 vdc) is supplied to the other eight inhibit drivers. For simplification only one inhibit driver (circuit 40311) and one inhibit return (circuit 40353) is discussed.

Assuming signal IL01 (circuit 40311) to be a logic ZERO and assuming signal 40331A is present, transistor Q13 is cut off by signal IL01 and transistor Q14 is turned on by signal 40331A. Simultaneously, signal RPT (circuit 40353) is a logic ZERO and transistor Q9 is turned on, which then turns on emitter follower transistors Q10 and Q11 and supplies +14 vdc to diodes CR23 through CR30. Tbus, the operation provides a current path from +14 vdc (through transistor Q10, diode CR23, core rope T, transistor Q14, resistor R29, and inductor L1) to +4 vdc.

The four reset drivers (figure 4-212) are enabled subject to signals RESETA, RESETB, RESETC, and RESETD. For simplification, only one reset driver (circuit 40362) and one reset return (circuit 40351) are discussed.

Assuming signal RESETA (circuit 40362) to be a logic ONE, transistor Q15 will conduct and turn on transistor Q16. Transistor Q16 then turns transistor Q17 and Q18 on which connects signal XRSTAN to the three core ropes and to three of the six return circuits. Signal XRSTAN is connected to the return circuits for reduction of noise on the reset lines. Simultaneously, signal RPR (circuit 40351) is a logic ZERO and transistor Q1 is turned on whicb then turns on emitter follower transistor Q4 and supplies +14 vdc to diodes CR9 and CR10. Thus, the operation provides a current path from +14 vdc (through transistors Q1 and Q4, diode CR9, core rope R, transistors Q17 and Q18, resistors R36 and R37, and inductors L2 and L3) to 0 vdc.

The two set drivers (figure 4-213) are enabled subject to signals SETAB and SETCD. The operation of the set circuits and the reset circuits is similar. Set circuits 40361 and 40354 function the same as reset circuits 40362 and 40351, respectively. One difference exists - a set line (XSETAD or XSETCD) threads two planes in a particular module of each rope. In the reset circuits, one of four reset lines threads only one plane in a particular module of each rope.

The two clear drivers (figure 4-214) are enabled simultaneously by signal CLROPE. The operation of driver circuits 40369 and 40370 is similar to tbeir counterparts in the set and reset driver circuits. One difference exists - the collectors of the two output transistors are not tied together and therefore only two modules are needed for three clear lines. Also, each line threads all cores of both modules and is tied directly to +14 volts.

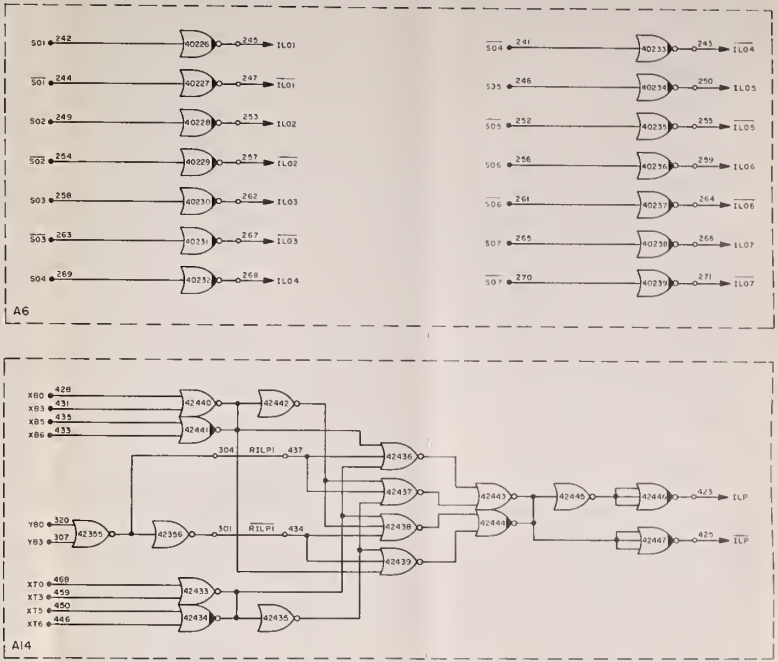


Figure 4-207. Inhibit and Parity Gates

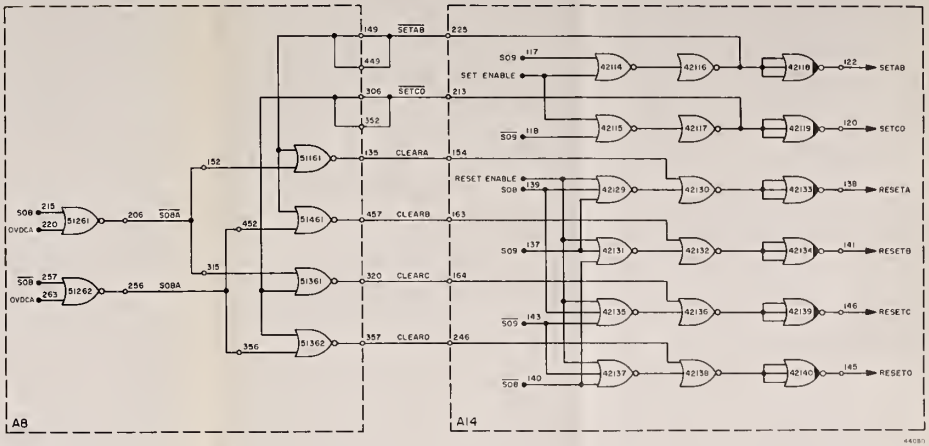


Figure 4-208. Set and Reset Selector Gates

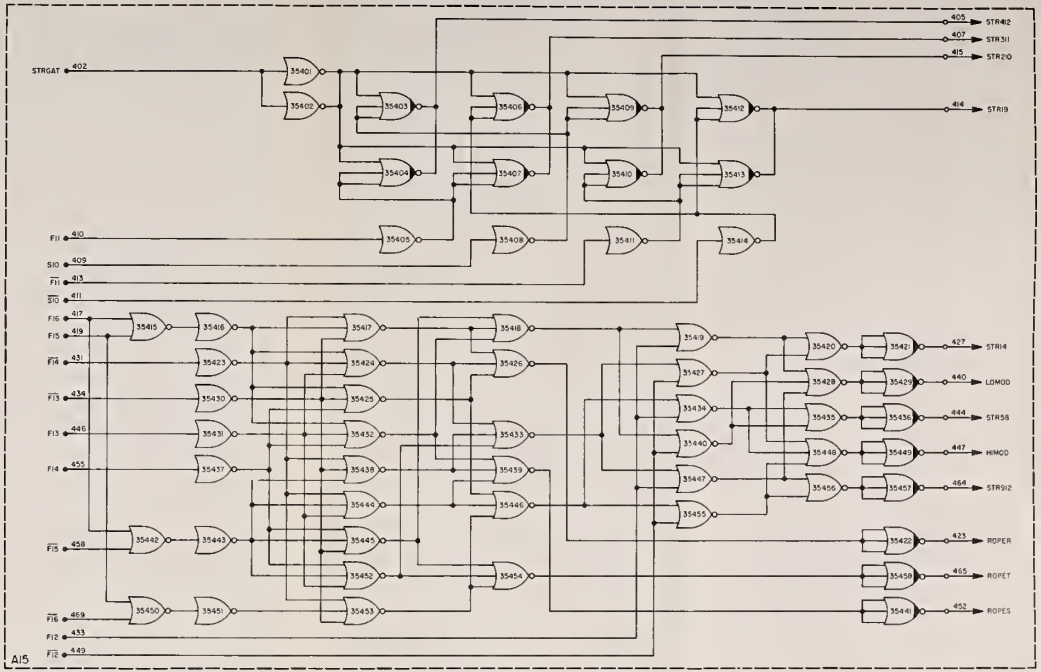


Figure 4-209. Rope, Module, and Strand Selector Gates

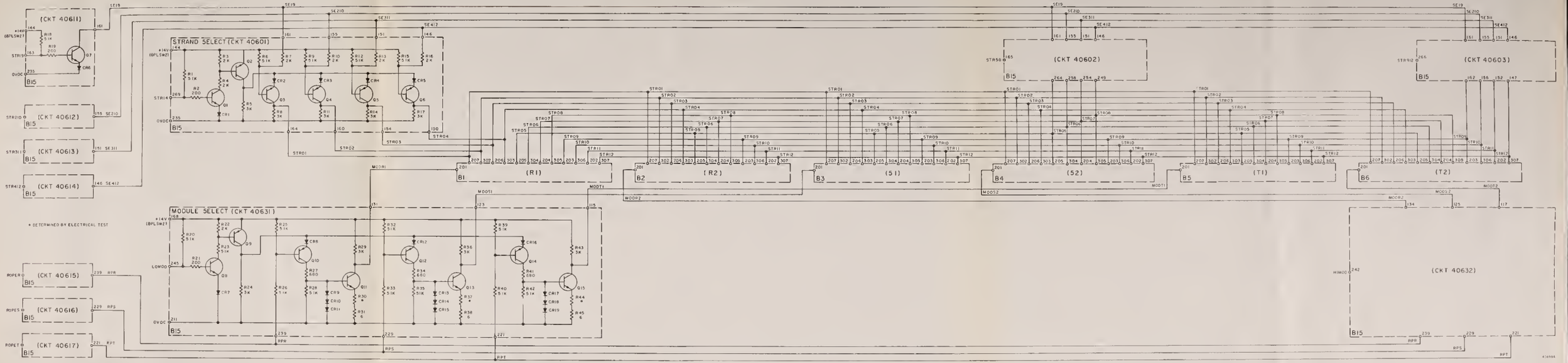


Figure 4-210. Strand and Module Selection Circuits

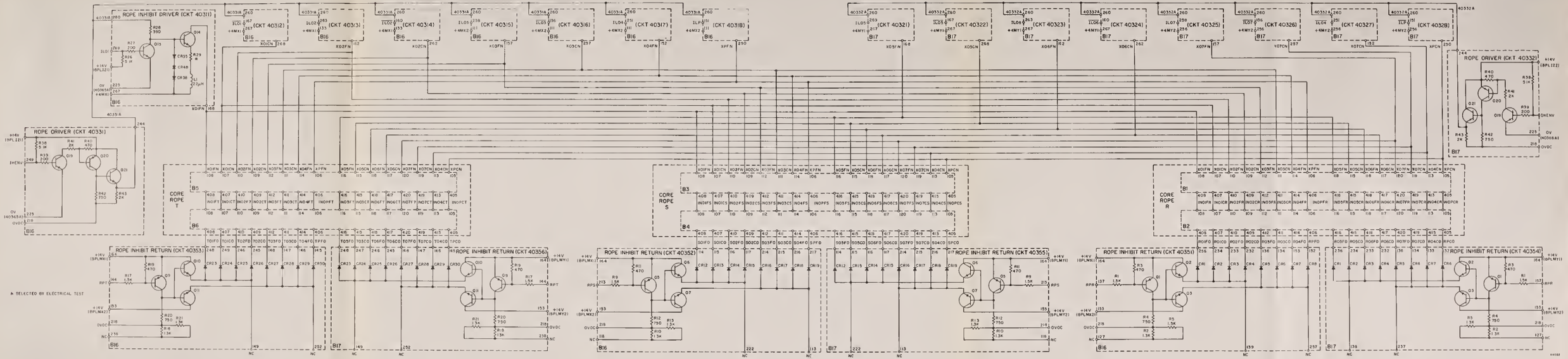


Figure 4-211. Inhibit Drivers and Return Circuits

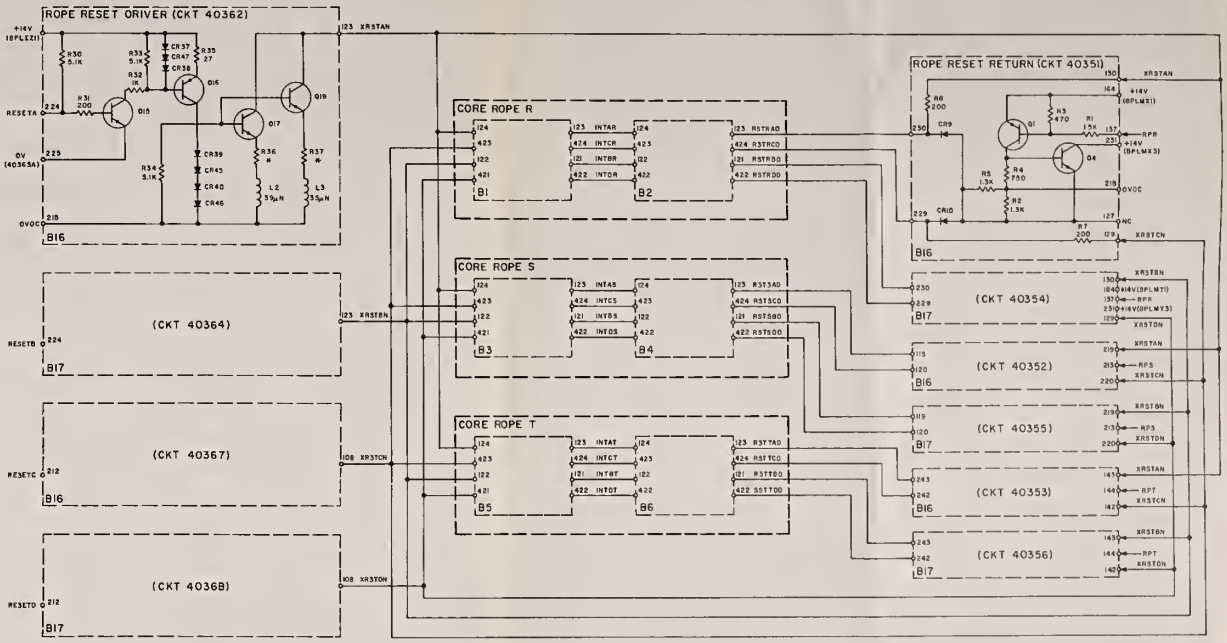


Figure 4-212. Reset Drivers and Return Circuits

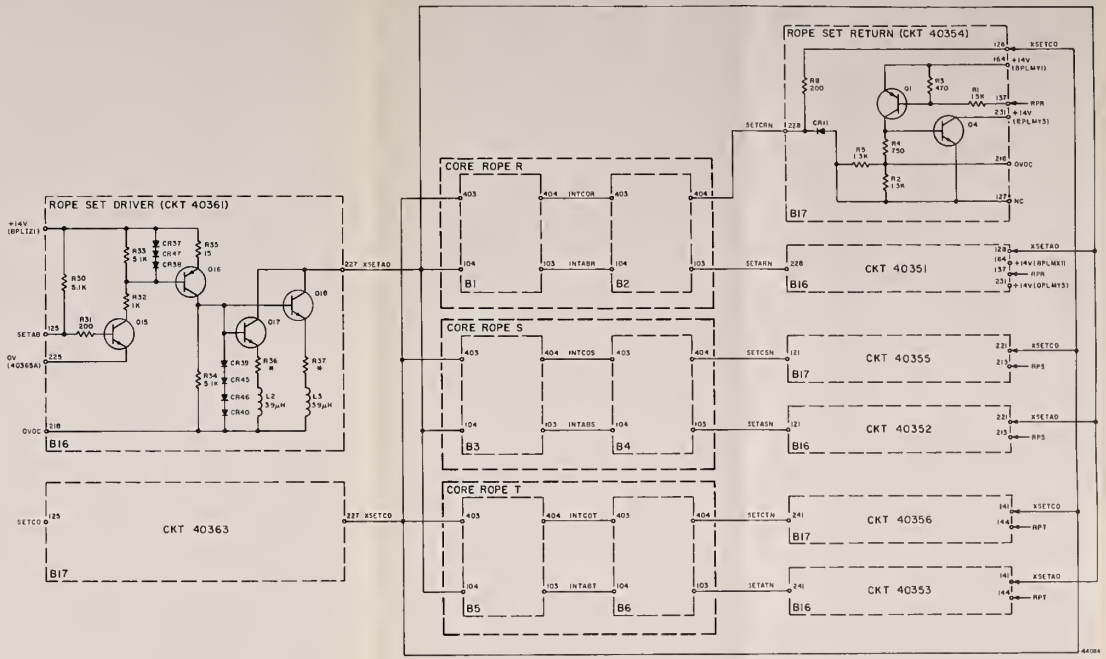


Figure 4-213. Set Drivers and Return Circuits

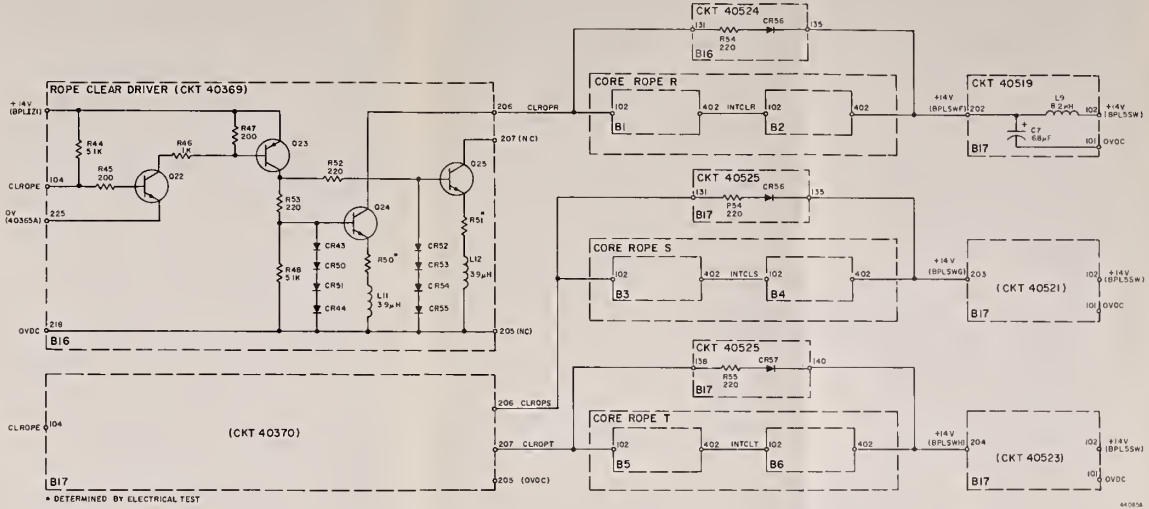


Figure 4-214. Rope Clear Driver Circuits

The clear lines in the fixed memory module run parallel to the set and inhibit lines. Mutual coupling could occur and cause a voltage to be induced on the clear lines when the selection lines are switched. To eliminate this possibility, a series resistor and diode are placed across each clear line in fixed memory (R54 and CR56 in figure 4-214). The polarity of the diode causes the induced voltage to be dissipated in the resistor, eliminating any coupling.

4-5.8.4.5 Sense Amplifiers. Sixteen sense amplifiers are associated with fixed memory. These amplifiers operate similar to those in erasable memory. The difference occurs in the input circuit (figure 4-215). The inputs to transformers T1 and T2 are returned to +14 vdc through resistors R1 and R2 to provide a return path for the sense lines. Output signals 40601A through 40608A from the SA1's are strobed to the sense amplifier output circuits (base of emitter follower Q1) in erasable memory (refer to figure 4-204) and become signals SA02, SA04, SA06, SA08, SA10, SA12, SA14, and SA16. These signals are then applied to register G.

Simultaneously output signals SA01, SA03, SA05, SA07, SA09, SA11, SA13, and SA15 are strobed through the fixed memory sense amplifiers (SA2's) and applied to register G. Thus, eight bits of fixed memory information from both the fixed and erasable sense amplifiers are applied to register G simultaneously.

The strobe driver (figure 4-216) receives fixed memory strobe signal SBF from the memory cycle timing circuits. The strobe signal is amplified and supplied to the fixed memory sense amplifiers as signal STROBE. This signal enables data to be transferred to the erasable memory sense amplifiers or register G.

4-5.9 POWER SUPPLY. Power required for operation of the computer is provided by two mechanically identical and electrically interchangeable power supplies. Conversion is accomplished by tray wiring. The power supply (figure 4-217) consists of a +4 vdc power supply, +14 vdc power supply, standby circuits, and alarm detection circuits.

4-5.9.1 +4 VDC and +14 VDC Power Supplies Functional Description. The +4 vdc and +14 vdc power supplies each consist of a voltage regulator, power input and output circuits, and a standby switching circuit. The voltage outputs (+4 vdc and BPLUS) are determined by minor circuit changes and sync signals from the timer.

Primary power of +28 vdc (+28 DCB) from the spacecraft electrical power system is applied to the power input circuit of the +4 vdc power supply, filtered and applied to the power output circuit. A second filter supplies output +28 COM to the interface circuits of tray A, alarm detection circuits of tray B and the DSKY. A zener diode regulator in the power input circuit supplies +9.2 vdc to the voltage regulator. The voltage regulator is a parallel regulator which operates on a 50 kc sync signal from the timer ($\overline{\text{SYNC4}}$). $\overline{\text{SYNC4}}$ triggers a multivibrator circuit in the voltage regulator, the output of which is of sufficient duration to provide 4 vdc to the power output circuit. The 4 vdc output is regulated by feedback from the power output circuit to the voltage regulator. Input signal CNTRL 1 allows simulated failure of the power supply under

control of the CTS during subsystem test. Standby operation, which is initiated by the STBY button on the DSKY, allows the computer to conserve power by operating in a low power mode. Power supply output +4 SW is disabled during the standby mode of operation by signal $\overline{\text{SBYREL}}$.

Operation of the +14 volt power supply is identical to the +4 volt power supply with the exception that a 100 kc sync signal ($\overline{\text{SYNC 14}}$) is used instead of 50 kc and the power source is +28 DCA instead of +28 DCB. The +14 volt output is regulated by feedback of the BPLUS output to the voltage regulator. During standby operation power supply output BPLSSW is disabled by signal $\overline{\text{SBYREL}}$.

4-5.9.2 Alarm Detection Circuits Functional Description. The alarm detection circuits consist of voltage, oscillator, scaler, and double frequency scaler alarm circuits, a warning integrator, a memory clamp (MYCLMP) circuit, and associated logic circuits. These circuits are included at this time because their operation depends directly on the presence of outputs from the power supplies.

The voltage alarm circuit monitors the +28 COM, BPLUS, and +4 vdc outputs and generates a signal VFAIL for an out-of-limits condition or complete failure of any one of these power supply outputs. Signal VFAIL conditioned by timing signals $\overline{\text{F05A}}$ and $\overline{\text{F05B}}$, will generate signal STRT1 from the logic circuits, provided it is not inhibited by interface signal NHVFAL. Signal STRT1, when applied to priority control, causes a GOJAM condition. Simultaneously, if the computer is in the standby mode, an input to the warning integrator (FILTIN) is generated. This input is controlled by signal $\overline{\text{STNDBY}}$.

The oscillator alarm circuit generates signal STRT2 if the computer oscillator (signal Q2A) fails or if the computer is in the low power mode (STANDBY). A delay circuit in the oscillator alarm assures a GOJAM condition, through STRT2 to priority control, until the oscillator starts running during a powerup condition. STRT2 will also cause the generation of signal OSCALM from the logic circuits.

There are two scaler alarm circuits in the computer, scaler alarm and double frequency scaler alarm. The scaler alarm circuit provides a check on scaler stage 17 (signal SCAS17 conditioned by signal FS17 from the timer) and generates signal SCAFAL should stage 17 fail to produce pulses. Signal SCAFAL generates signals AGCWAR and CGCWAR directly from the logic circuits. Signal DOSCAL from the CTS is used to test the operation of the scaler alarm via signal SCAS17. Double frequency scaler alarm generates signal 2FSFAL if the 100 pps scaler stage (signal SCAS10 from the logic circuits conditioned by signals FS09, and FS10 from the timer) should fail. Signal 2FSFAL provides an input to signal FILTIN which causes signals AGCWAR and CGCWAR to be generated from the logic circuits via signal FLTOUT. Signal DBLTST from the CTS is used to test the operation of the double frequency scaler alarm via signal SCAS10.

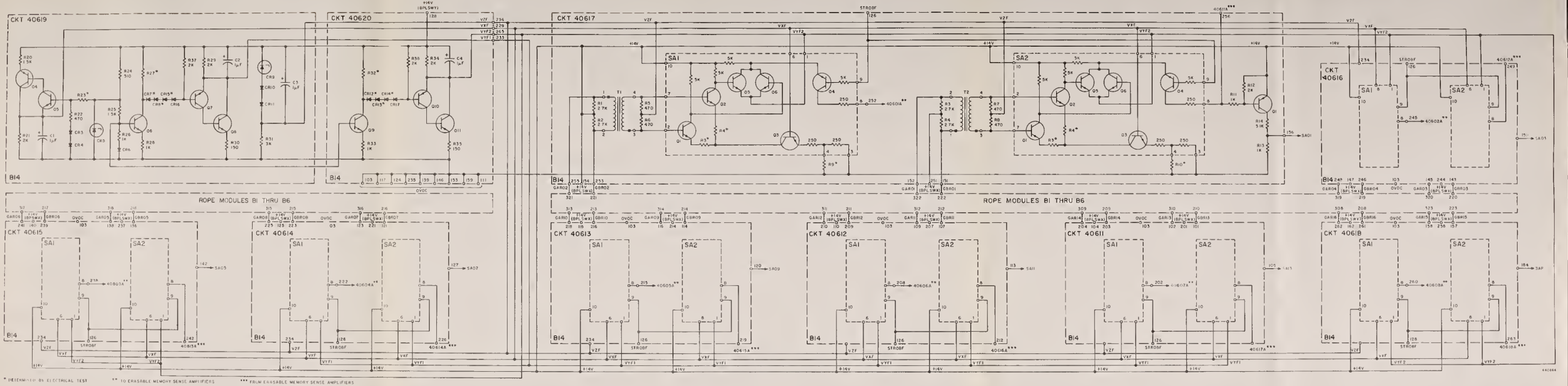
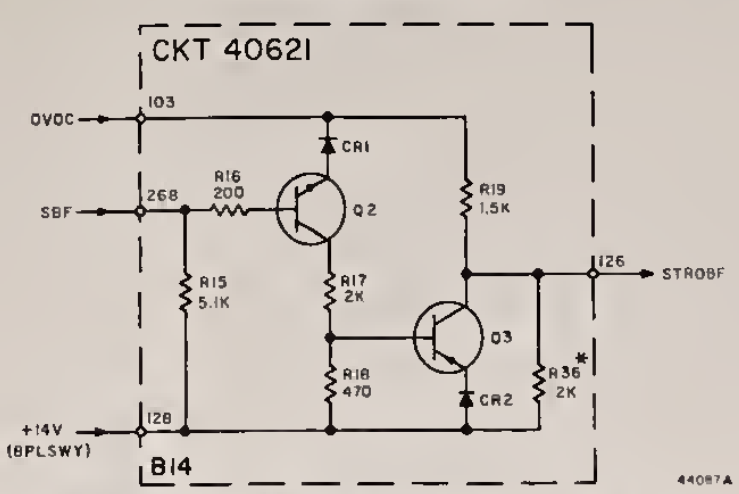


Figure 4-215. Sense Amplifiers and Voltage Soureo



* In module P/N 2003981-031 and above, R36 is replaced by zenner diode CR18.

Figure 4-216. Strobe Driver, Fixed

The warning integrator initiates the generation of warning signals AGCWAR and CGCWAR simultaneously from the logic circuits. Input signal F1LT1N, conditioned by timing signals $\overline{SB0}$, $\overline{SB2}$, F08B, and F14B represents restart or counter fail signal (DOF1LT), voltage fail in the standby mode, alarm test signal (ALTEST), or double frequency scaler alarm.

The MYCLMP circuit output, signal STRT2, inhibits access to memory should either power supply be out of its specified limits, fail completely, or be in the low power mode.

The incorporation of a +5 vdc source within the alarm detection circuits eliminates the need for more semiconductors and components normally used where a reference voltage is required such as in the scaler alarm, double frequency scaler alarm, warning integrator, and MYCLMP circuits.

4-5.9.3 Standby Circuits. The standby circuits (figure 4-218) are used for placing the CSS in a low power mode to conserve power. The standby mode of operation is initiated by entering verb 60 and depressing the STBY key, for a maximum of 1.92 seconds, on either DSKY. Verb 60, subsequently causes signals $\overline{WCH13}$ and $\overline{CHWL11}$ to be generated, and set FF 45138-45139 of module A18 to generate signal ENSTBY as a logical zero. The STBY key must be depressed for a maximum of 1.92 seconds because of the period between timing signals F17A and F17B, which is approximately 1.3 seconds. When depressed, the STBY key applies +28 volts to interface module A25 where it is divided by resistors R4 and R5. Signal SBYBUT, which occurs as a logic ONE, is then applied to module A18 where it is inverted (45141) and sets FF 45145-45144 through gate 45143 coincident with timing signal $\overline{F17A}$. The reset output of FF 45145-45144 coincident with timing signal $\overline{F17B}$ in turn sets FF 45142-45146. The output of this flip-flop is applied to gates 45152, 45151, and 45149. With signals ENSTBY and GOJAM also at

a logic ZERO level, FF 45150-45151 is set by the output of gate 45149. This in turn sets FF 45154-45155. The ONE output from gate 45155 is inverted by gates 45153 and 45156. These two outputs are again inverted and appear as signals SBY and SBYLIT. Signal SBY is inverted by gate 42457 and applied as signal $\overline{\text{SBYREL}}$ to the standby switching circuits of the +4 and +14 volt power supplies. Signal SBYLIT turns on transistor Q2 of interface module A25 and supplies a level of 0 vdc to the DSKY display indicator circuit for lighting the STBY indicator. Signal ALTEST will also cause the STBY indicator to light.

When the STBY key is released FF's 45145-45144, 45142-45146, and 45150-45151 are reset. This action does not affect FF 45154-45155. Signal GOJAM also occurs at this time.

To return to normal operation, the STBY key is pressed for a maximum of 1.92 seconds and then verb 61 is entered. When the STBY key is pressed, FF's 45145-45144, and 45142-45146 are set. This enables gates 45149, 45151, and 45152. With signal GOJAM a ONE, and FF 45150-45151 reset, gate 45152 generates a ONE which resets FF 45154-45155 and causes signals SBY and SBYLIT to revert to ZERO. Verb 61 causes signal CCH13 to be generated which then resets FF 45138-45139.

4-5.9.4 +4 VDC Power Supply Detailed Description. The +4 vdc power supply consists of a power input circuit, voltage regulator, power output circuit, and standby switching circuit.

The +4 vdc power supply, P/N 2003953-021, is illustrated in figure 4-219. The +4 vdc power supply, P/N 2003887-011, is illustrated in figure 4-219A. The differences between these two configurations, which occur in the power input circuit and the standby switching circuit, are as follows:

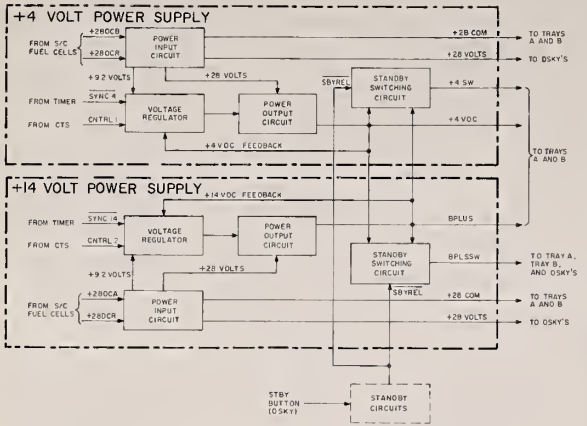
1) The +4 vdc power supply, P/N 2003953-021, contains a regulated power supply (consisting of stages Q17 and Q18 and associated components) which was formerly used to provide approximately 26.5 volts to the DSKY. These components are shorted out by a jumper on the tray A wire assembly (pin 144 to 145).

In the +4 vdc power supply, P/N 2003887-011, the DSKY regulator components are removed.

2) The value of resistor R43 in P/N 2003887-011 is changed to 2.2K. This change compensates for loss of margin under worst case low margin operation.

Primary power of +28 vdc B (WD168) from the spacecraft is applied through diode CR10 and inductor L3 to two filter networks and two regulator circuits of the power input circuit. The first filter network (C19-22) supplies output +28 COM to the alarm detection circuits. The second filter network (C8-C12, L2) supplies +28 vdc to the power output circuit. 28 vdc is routed through resistor R39, zener diode CR7, and emitter follower Q14 to supply 9.2 vdc for powering the voltage regulator circuit.

Transistor Q1 in the voltage regulator circuit is a differential amplifier which acts as a regulating device on the free running multivibrator circuit consisting of transistors Q6 and Q7. Zener diode CR1 and its associated circuitry establish a constant voltage reference at the base of Q1A. A portion of the +4 vdc output from the power supply is fed back to the base of Q1B. Resistor R13 is shunted by tray wiring to establisb the reference level. Any difference between the reference voltage applied to the base of Q1A and the feedback voltage applied to the base of Q1B affects the pulse width output of the multivibrator, via transistor Q2, and opposes any change in the +4 vdc output. Input CNTRL 1, from the CTS, is applied to the base of Q1B and allows simulated failure of the +4 vdc power supply during subsystem test. Input W-910, from automatic checkout equipment (ACE), is applied to the base of Q1A and allows simulated failure of the +4 vdc power supply during spacecraft test. This signal may also be used during subsystem test by the CTS.



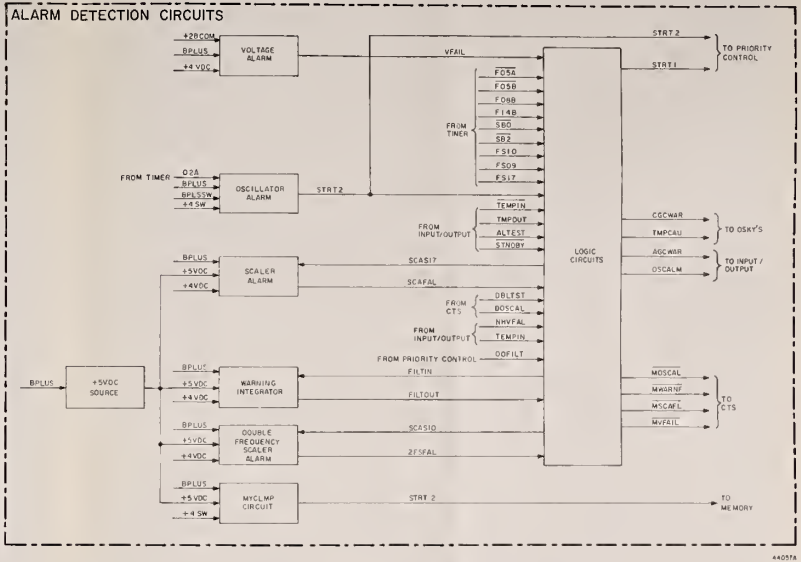


Figure 4-217. Power Supply Functional Diagram

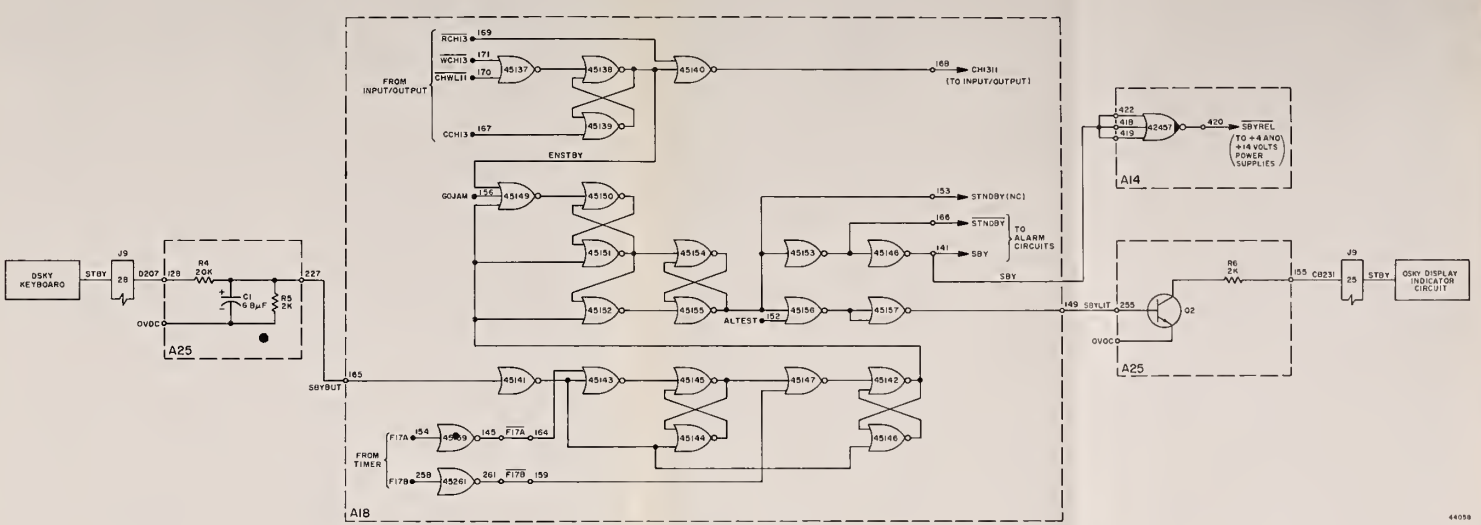
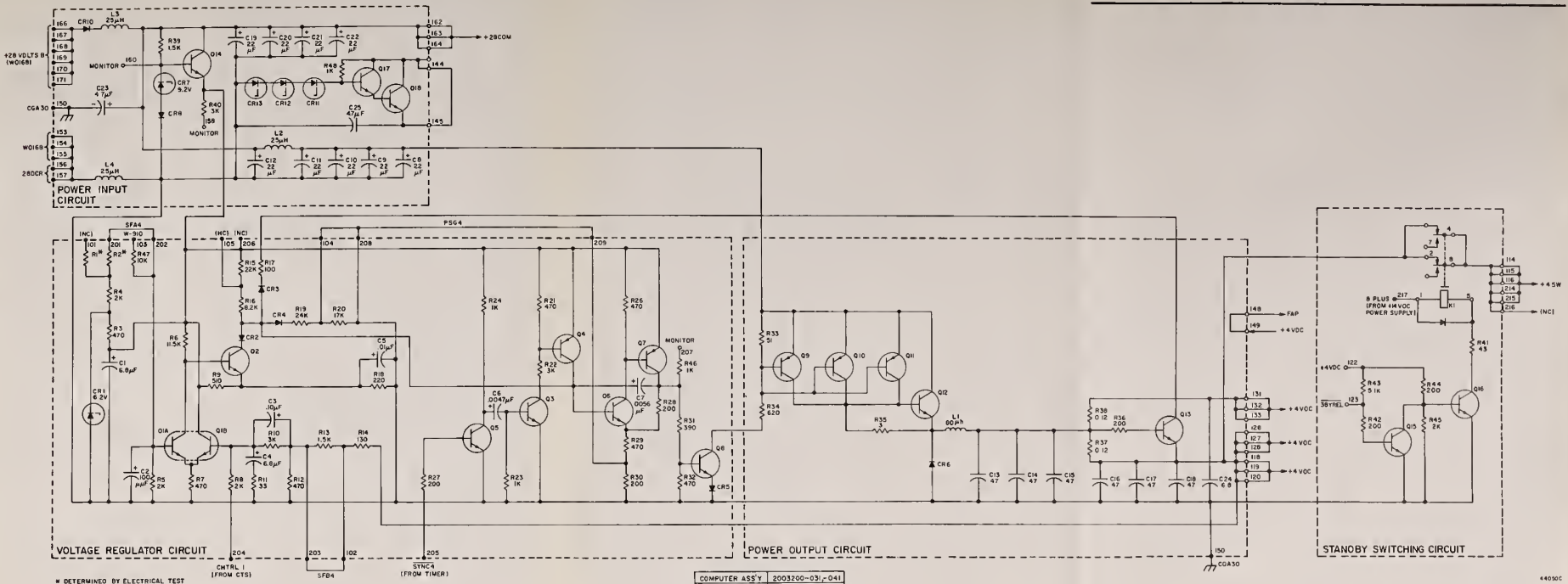


Figure 4-218. Standby Circuits



COMPUTER ASS'Y	2003200-031, -041
A30 ASS'Y	200395-021
A30 SCHEM	2005945

Figure 4-219, +4 VDC Power Supply, PN 2003953-021, Schematic Diagram

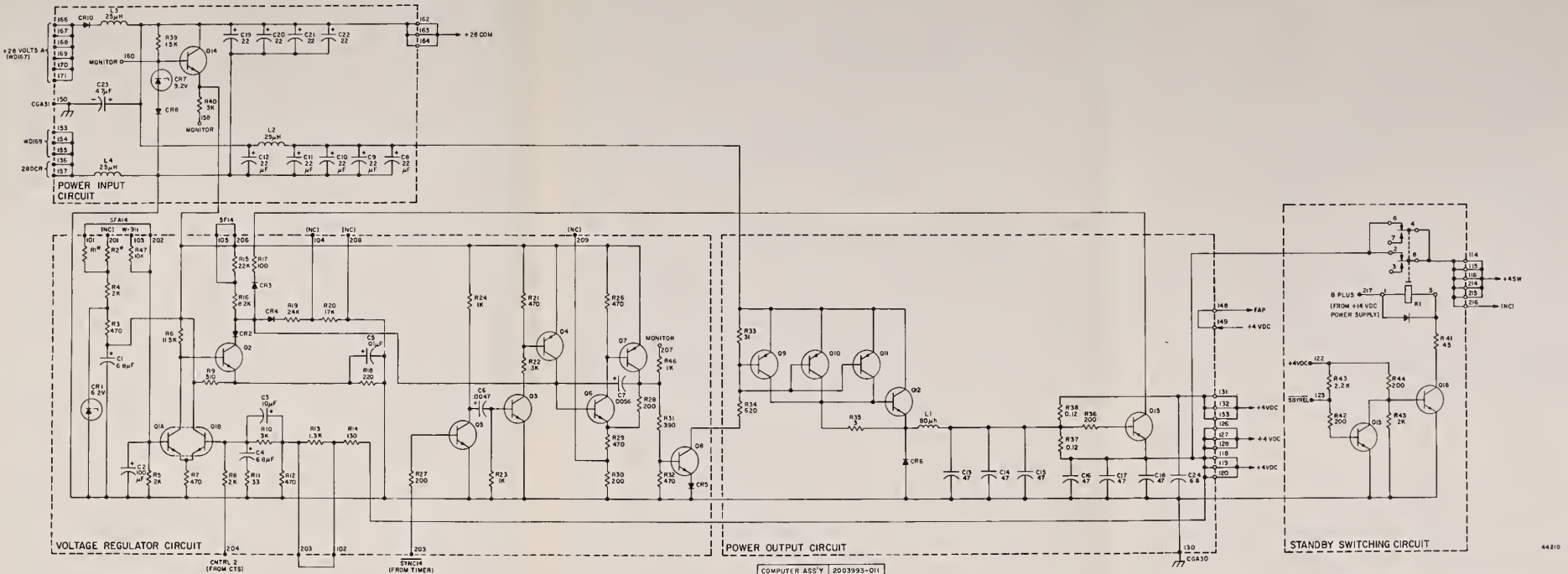


Figure 4-219A. +4 VDC Power Supply, PN 2003887-011, Schematic Diagram

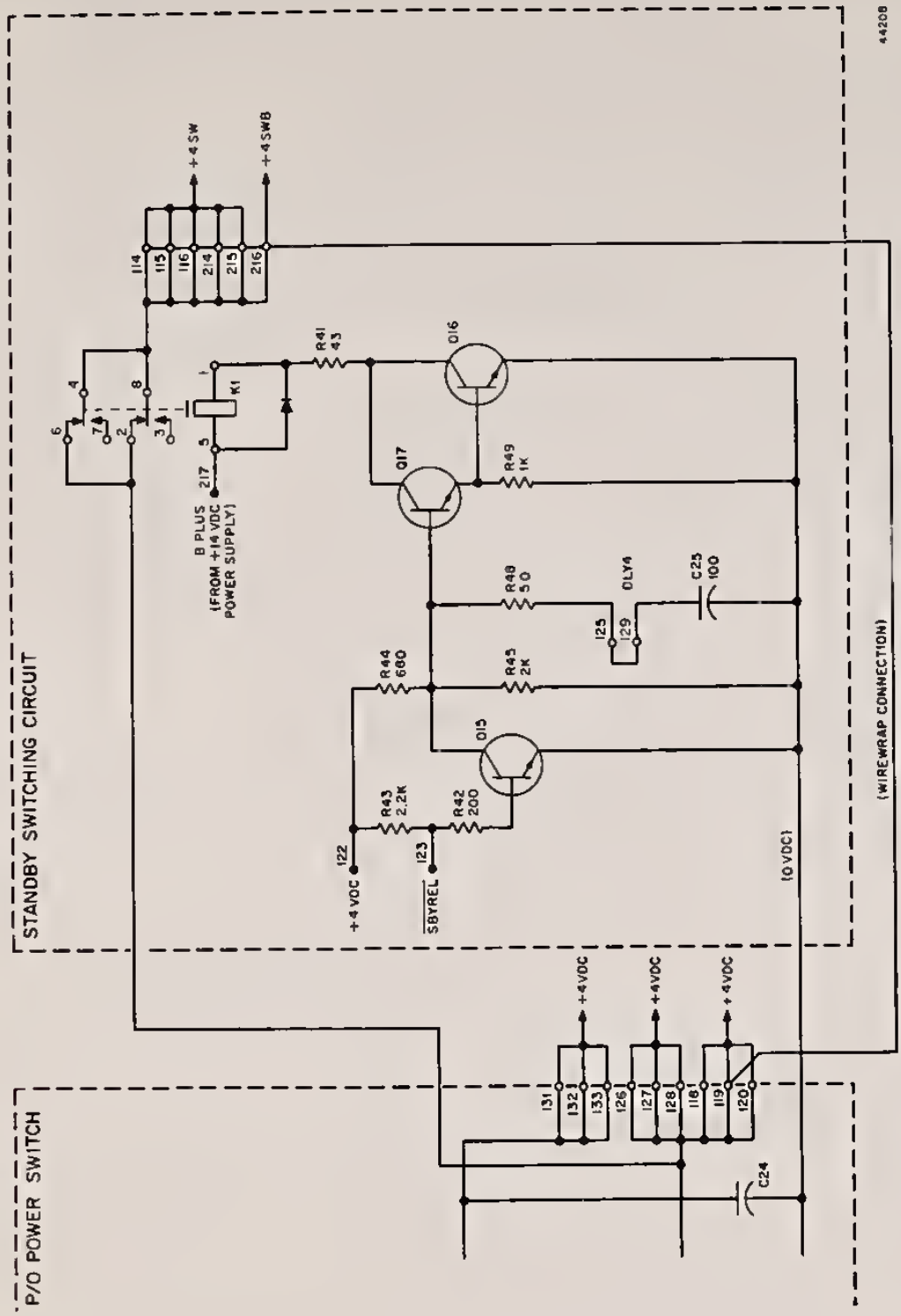


Figure 4-219B. +4 VDC Power Supply, PN 2003892-011, Schematic Diagram

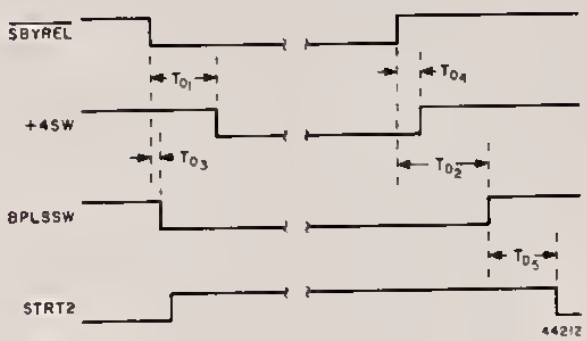


Figure 4-219C. Standby Mode Switching Sequence

Input signal $\overline{\text{SYNC4}}$ (50 kc) is applied to the sync circuits (Q3, Q4, and Q5) and fixes the frequency of the output pulses from the free running multivibrator. The level of the +4 vdc regulator output, from Q8, is established by resistor R2 and by shunting out resistors R13, R20 and R30.

The regulator output pulses are applied to transistor power amplifier drivers Q9, Q10, and Q11 of the power output circuit. The output of these parallel transistors is fed through power amplifier Q12, filtered (C13-C15 and L1), and applied to output transistor Q13. Resistors R37 and R38 are connected in parallel by tray wiring for the +4 vdc power supply. The output of Q13 is the +4 vdc power supply output. The output of +4 vdc is also applied from charging network C16-C18 to the standby switching circuit.

The standby mode, which is used to conserve power, is controlled by the STBY pushbutton on the DSKY. In the +4 vdc power supply shown in figures 4-219 and 4-219A (P/N 2003953 and P/N 2003887), pressing the STBY pushbutton causes signal $\overline{\text{SBYREL}}$ to turn off transistor Q15 in the standby switching circuit, which causes transistor Q16 to turn on. This action energizes relay K1 and disables output +4SW. The voltage output BPLUS from the +14 vdc power supply energizes the coil of K1. With output signal +4SW disabled during the standby mode, the only computer circuits operating are the power supplies (outputs +4 vdc and BPLUS), oscillator, interface, and the scaler and clock divider circuits. These circuits are necessary for keeping track of real time and supplying synchronization signals to other spacecraft systems.

A portion of the +4 vdc power supply, P/N 2003892, is illustrated in figure 4-219B. This power supply configuration is identical to the configuration described above except for the standby switching circuit. In figure 4-219B, transistor Q17, resistors R48 and R49, and capacitor C25 are added to the circuit. These components delay the +4SW output with respect to BPLSSW when entering or leaving the standby mode. The combination of R48 and C25 provides the necessary delay for the +4SW signal when entering standby. This action, illustrated in figure 4-219C, prevents undesirable transients and signal dropout to the power supply sync logic. An additional output in this power supply configuration, +4SWB, provides a small bias for the switched loads on tray A during standby to minimize the overloading of the inputs signals to the sync logic.

Power distribution for tray A is shown in table 4-XCIX.

4-5.9.5 +14 VDC Power Supply Detailed Description. The +14 vdc power supply configurations are illustrated in figures 4-220, 4-220A, and 4-220B. Operation of this power supply is identical to that of the +4 vdc power supply with the following exceptions:

1) The level of the regulator circuit output is established by resistor R1 and by shunting resistor R15.

2) Inputs W-911 and CNTRL 2 allow simulated failure of the +14 vdc power supply during test.

3) Input $\overline{\text{SYNC14}}$ (100 kc) fixes the frequency of the output pulses from the free running multivibrator.

4) In the +14 vdc power supply, P/N 2003892, resistor R48 is not connected. Capacitor C25 is connected between the base of Q15 and the 0 vdc line.

4-5.9.6 Alarm Detection Circuits Detailed Description. The alarm detection circuits (figure 4-221) monitor the outputs of the power supply, oscillator, scaler, and priority control and generate a restart, failure, caution, or warning signal if any of the outputs should fail.

The voltage alarm circuit consists of a constant current source (Q1 and Q2), voltage divider (R11 thru R19), five differential amplifiers (Q3 thru Q7), and output transistors (Q8 thru Q10). The +28 COM input from both the +4 and +14 volt power supplies is applied to parallel transistors Q1 and Q2 where a constant current source is established. Zener diodes CR4 and CR5 in the collector circuit of Q2 supply +12.4 volts as a reference voltage to the voltage divider and differential amplifiers. Capacitor C1 acts as a storage device and is capable of powering the voltage alarm for a short period of time should the +28 volt supply fail abruptly or decay rapidly. The +28 COM input is also filtered by R3, R4, R5 and C4 and applied to detector Q7. Normally, Q7A is off, Q7B is on, and output transistor Q10 is off. If the +28 COM input should decrease below approximately +18 volts, Q7A will conduct, turn transistor Q10 on and generate output VFAIL. Similar operation occurs for the +4 and +14 volt detector circuits. BPLUS is divided and filtered (R1, R7, and C2) before being applied to detectors Q3 and Q4. Transistors Q3 and Q4 are the high and low limit detectors respectively for the +14 volt power supply. If the +14 volt power supply measures approximately +16 volts Q3A will conduct, turn on transistor Q8 and generate VFAIL. If the +14 volts decreases to approximately +12 volts Q4A will conduct, turn on transistor Q9 and generate VFAIL. +4 vdc is filtered by R2 and C3 before being applied to detectors Q5 and Q6. Transistors Q5 and Q6 are the high and low limit detectors respectively for the +4 volt power supply. If the +4 volt power supply increases to approximately +4.5 volts, transistor Q5A will conduct, turn on transistor Q8 and generate VFAIL. If the +4 volt input decreases to approximately 3.5 volts transistor Q6A will conduct, turn on transistor Q9 and generate VFAIL. Signal VFAIL is applied to the voltage alarm circuit where it will generate signal STRT1, subject to timing signals $\overline{\text{F05A}}$ and $\overline{\text{F05B}}$ and if not inhibited by interface signal NHVFAL. Signal STRT1, when applied to priority control, causes signal GOJAM.

The oscillator alarm inputs are a 1.024 megacycle square wave (Q2A) from the timer and +14 volts (BPLSSW), +4 volts (+4SW) and BPLUS from the power supply. Normally, transistors Q12, Q16, and Q17 are off, Q13, Q14, and Q15 are on, and C7 is fully charged to +14 volts. If Q2A, +4SW, or BPLSSW is not present, Q12 is turned on and C7 discharges. Transistors Q13, Q14, and Q15 are off; transistors Q16 and Q17 are on, generating signal STRT2. However, because of the time it takes for the alarm circuit to recover (approximately 250 milliseconds), erasable memory information may be lost as it comes out of standby. Therefore, positive feedback from the collector of Q17 to the base of Q16 is used to provide instant switching. When the inputs are all present again it will take approximately 250 milliseconds for the complete circuit to be operable. This is accomplished by the time it takes to change capacitor C7. The same situation occurs when the computer is initially turned on or when the computer is switched from standby to operate. Signal STRT2, when applied to priority control, causes signal GOJAM. Signal STRT2, when applied to the oscillator alarm logic circuit in module A13, causes signal OSCALM to be generated and applied to input-output. Signal CCH33 from input-output is a clear signal for flip-flop 41232-41233.

The +5 vdc voltage source provides a reference voltage to the detector circuits in the scaler alarm, double frequency scaler alarm, warning integrator, and MYCLMP circuits.

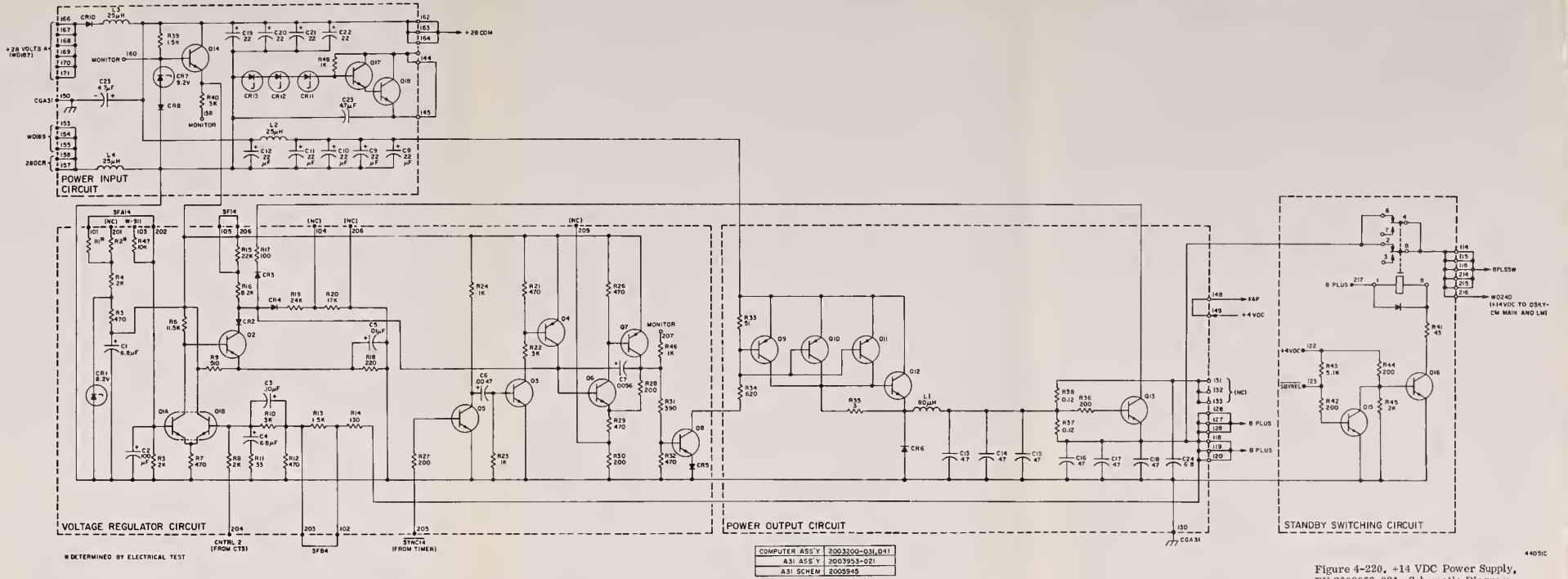
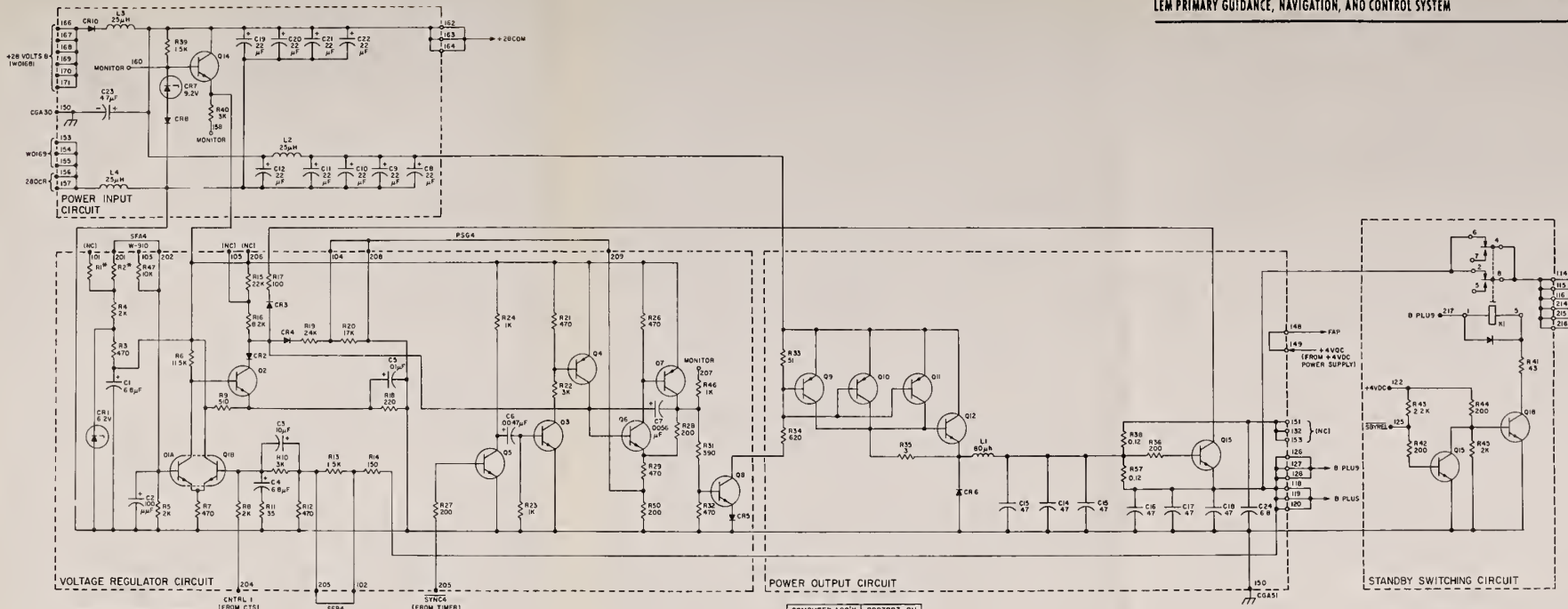


Figure 4-220. +14 VDC Power Supply, PN 2003953-021, Schematic Diagram



COMPUTER ASS'Y	2003993-011
A31 ASS'Y	2003887-011
A31 SCHEM	2005936

Figure 4-220A. +14 VDC Power Supply PN 2003887-011, Schematic Diagram

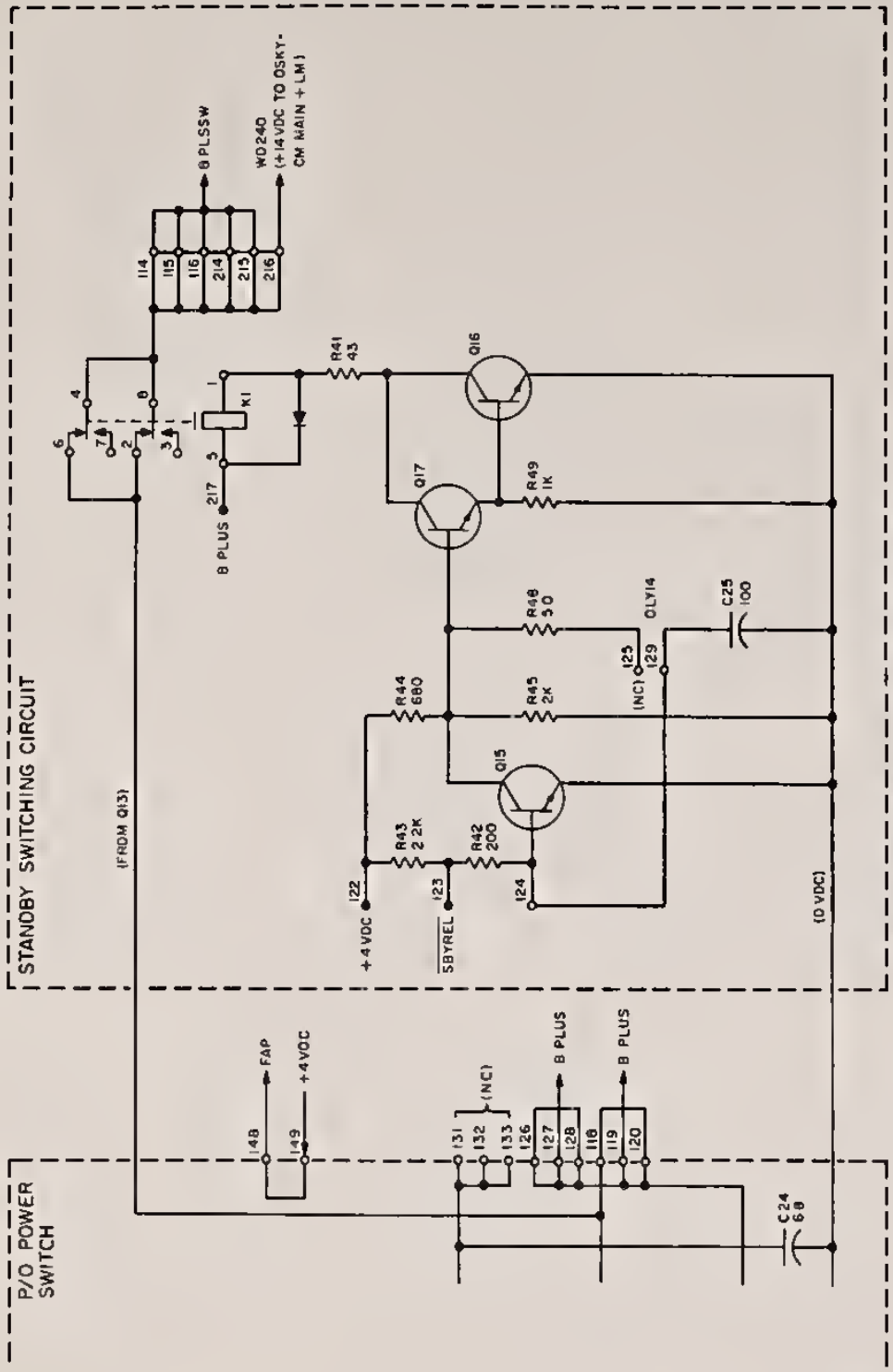


Figure 4-220B. +14 VDC Power Supply, PN 2003892-011, Schematic Diagram

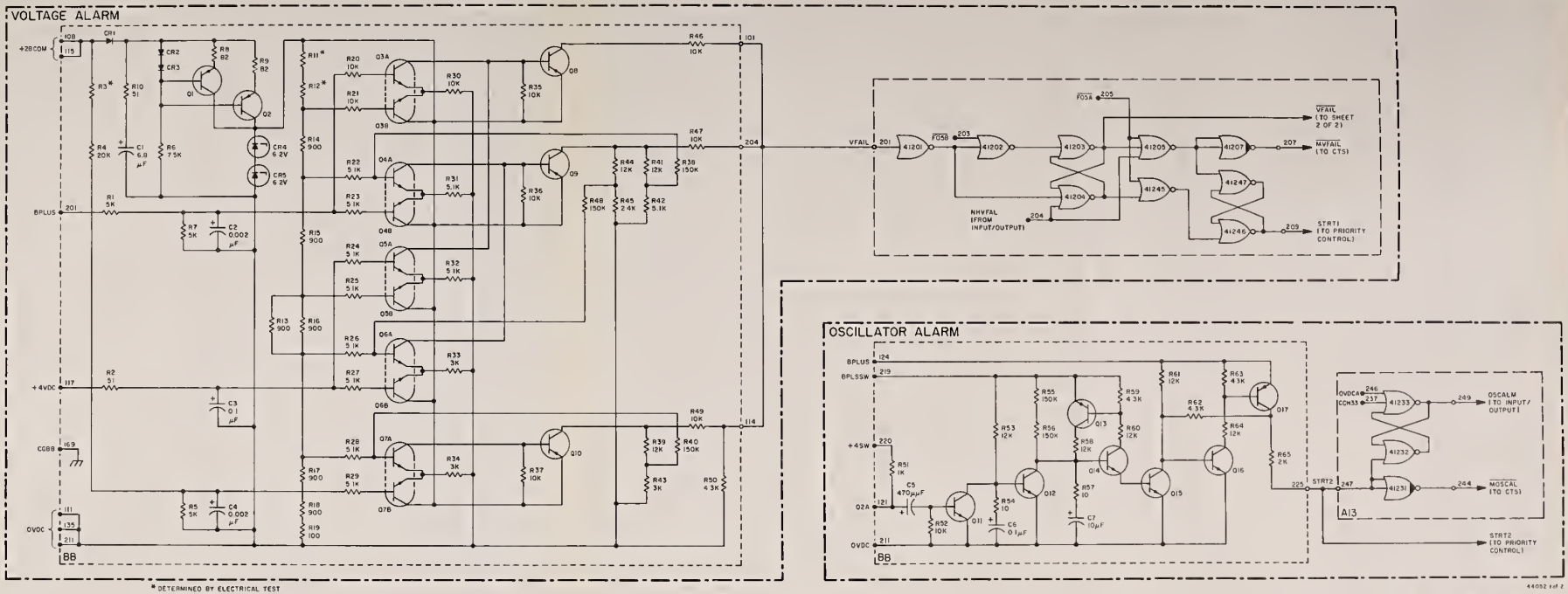


Figure 4-221. Alarm Detection Circuits, Schematic Diagram (Sheet 1 of 2)

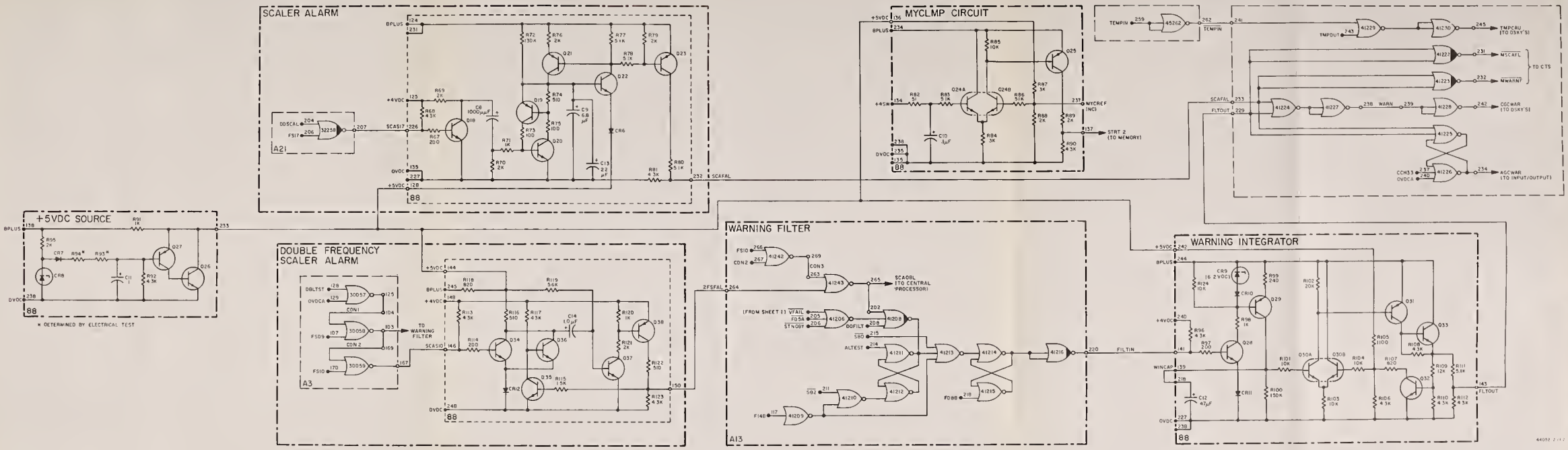


Figure 4-221. Alarm Detection Circuits, Schematic Diagram (Sheet 2 of 2)

The scaler alarm circuit receivcs input FS17 (0.78125 pps) from the timer and produces signal SCAS17 from logic gate 32258. Signal DOSCAL, from the CTS, is used for testing the scaler alarm circuit. Normally transistor Q18 is on, and transistors Q19 and Q20 are off. The voltage present in parallel capacitors C9 and C13 is less than the turnon voltage required for Q22; therefore, transistors Q21, Q22, and Q23 are off and signal SCAFAL is approximately 0 vdc. If the scaler should fail, transistor Q18 is turned off, and the signal at its collector is differentiated by C8 and R70 and fed to Q20. Transistor Q20 is turned on, which turns Q19 on and supplies the base drive required to keep Q20 on. Transistor Q21 is on and supplies the drive necessary to turn Q22 on. Reference voltage (+5 VDC) is supplied through CR6 and Q22, and applied to Q21 and Q23 where it clamps Q21 on, turns Q23 on and generates signal SCAFAL to a logic circuit which in turn will generate a warning signal to the DSKY and input-output.

The double frequency scaler alarm monitors signal SCAS10 (100 pps) from its logic circuit in module A3. However, signal SCAS10 is not equal in duty cycle to FS10. Signal SCAS10 has a 25% duty cycle generated as a result of combining signals FS09 and FS10 from the timer. Signal CON 2 from module A3 is applied to warning filter module A13 where, when combined with signal FS10, will generate signal CON 3. Thus, signal SCAS10 is equal to signal CON 3. Signal DBLTST, from the CTS, is used for testing the double frequency scaler alarm circuit. Transistors Q35, Q37, and Q38 are normally on and Q36 is normally off. When transistor Q34 is on a negative going transition will be coupled through capacitor C14. This transition will be routed through Q37 and Q38. The pulse width of this change is determined by time constant C14 and R119. The output of Q38 is supplied as signal 2FSFAL to the warning filter where it is compared with signal CON 3 at the input of gate 41243. Normally gate 41243 yields a ZERO as its output. However, if signal SCAS10 increases to approximately 200 pps, the output will be a series of ONE's.

The MYCLMP circuit operates identical to that of a voltage alarm circuit. The differential amplifier Q24 has reference voltage (+5 vdc) applied to one side (Q23B) and +4SW applied to the other side (Q24A). Normally transistor Q25 is off and output signal MYCLMP is approximately 0 vdc. If the +4 volt power supply should fail or the computer is put into the standby mode, the +4SW is decreased to 0 vdc and Q24A cuts off. Q24B then conducts causing Q25 to turn on and generate signal STRT2 to memory where it inhibits any access to the memory circuits.

The warning filter performs logic gating for the following inputs:

(1) $\overline{\text{VFAIL}}$ and $\overline{\text{STNDBY}}$.

(2) 2FSFAL.

(3) DOFILT.

(4) ALTEST.

Any one of the above conditions sets flip-flop 41211-41212. The flip-flop output is applied through gate 41213 and in turn sets flip-flop 41214-41215, subject to timing signals $\overline{SB0}$ and $\overline{F14B}$. The output of flip-flop 41214-41215, FILTIN, is applied to the warning integrator. All occurrences of these input conditions are stretched so that no more than one input to the warning integrator is generated in each 160 millisecond period. This is controlled by timing signal F14B. Thus, the output signal FILTIN has a maximum rate of 6 pps.

Each of the pulse inputs to the warning integrator has a duration of 1.125 milliseconds, and because of this the warning integrator will not receive an input pulse each time a restart is called for by the computer. Normally transistors Q28 through Q33, with the exception of Q30B, are off. A positive pulse turns on transistor Q28 which will turn on constant current source Q29 and supply a charge to capacitor C12. Resistor R97 controls the amount of charge. This charge will add a voltage step to C12. When five successive pulses are received it will cause the voltage on C12 to overcome the threshold voltage (approximately +4 volts) of Q30A. Turning Q30A on will turn Q21, Q32, and Q33 on which will make the detector regenerative. Signal FLTOUT will remain high as an output as long as pulses are forthcoming. However, if only the above occurs it would take approximately five seconds for C12 to discharge througb R100. Thus, signal FLTOUT is present for approximately 5 seconds. Resistor R124 assures that C12 will not be charged, through transistor parameter action, due to high temperatures.

Signal FLTOUT from the warning integrator and signal SCAFAL from the scaler alarm are applied to gates 41222 through 41224 and flip-flop 41225-41226 where, if either or both is high, signals $\overline{MSCAFL}$, $\overline{MWARNF}$, LGCWAR, and AGCWAR will be generated. Signal CCH33 is a clear signal for flip-flop 41225-41226.

If the IMU stable member temperature exceeds its design limits signal TEMPIN conditioned by signal TMPOUT will generate signal TMPCAU.

All AGC alarms are inhibited during the standby mode with tbe exception of AGCWAR and CGCWAR, which can be caused by a voltage fail or scaler fail, and TMPCAU, which is caused by an IMU temperature alarm.

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A1	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 38100 and 38200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 38300 and 38400 series gates.
	+4 VDC	122, 150, 222, 250	To pin V of 38100 and 38200 series gates except those gates tied to FAP pin (234).
	+4 VDC	322, 350, 422, 450	To pin V of 38300 and 38400 series gates except those gates tied to FAP pin (338).
A2	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs to 37100 and 37200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 37300 and 37400 series gates.
	+4 VDC	122, 150, 222, 250	To pin V of 37100 and 37200 series gates except those gates tied to FAP pin (144).
	+4 SW	324, 348, 424, 448	To pin V of 37300 and 37400 series gates except those gates tied to FAP pin (445).

(Sheet 1 of 12)

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A3	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 30000 and 30100 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 30300 and 30400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 30000 and 30100 series gates except those gates tied to FAP pin (247).
	+4 SW	324, 348, 424, 448	To pin V of 30300 and 30400 series gates except those gates tied to FAP pin (409).
A4	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 36100 and 36200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 36300 and 36400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 36100 and 36200 series gates except those gates tied to FAP pin (135).
	+4 SW	324, 348, 424, 448	To pin V of 36300 and 36400 series gates except those gates tied to FAP pin (337).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A5	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 39100 and 39200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 39300 and 39400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 39100 and 39200 series gates except those gates tied to FAP pin (145).
	+4 SW	324, 348, 424, 448.	To pin V of 39300 and 39400 series gates except those gates tied to FAP pin (447).
A6	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 40100 and 40200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 40300 and 40400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 40100 and 40200 series gates except those gates tied to FAP pin (232).
	+4 SW	324, 348, 424, 448	To pin V of 40300 and 40400 series gates except those gates tied to FAP pin (440).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A7	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 33100 and 33200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 33300 and 33400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 33100 and 33200 series gates except those gates tied to FAP pin (237).
	+4 SW	324, 348, 424, 448	To pin V of 33300 and 33400 series gates except those gates tied to FAP pin (337).
A8	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 51100 and 51200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 51300 and 51400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 51100 and 51200 series gates except those gates tied to FAP pin (157).
	+4 SW	324, 348, 424, 448	To pin V of 51300 and 51400 series gates except those gates tied to FAP pin (427).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A9	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 52100 and 52200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 52300 and 52400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 52100 and 52200 series gates except those gates tied to FAP pin (157).
	+4 SW	324, 348, 424, 448	To pin V of 52300 and 52400 series gates except those gates tied to FAP pin (427).
A10	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 53100 and 53200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 53300 and 53400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 53100 and 53200 series gates except those gates tied to FAP pin (157).
	+4 SW	324, 348, 424, 448	To pin V of 53300 and 53400 series gates except those gates tied to FAP pin (427).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A11	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 54100 and 54200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 54300 and 54400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 54100 and 54200 series gates except those gates tied to FAP pin (157).
	+4 SW	324, 348, 424, 448	To pin V of 54300 and 54400 series gates except those gates tied to FAP pin (427).
A12	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 34100 and 34200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 34300 and 34400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 34100 and 34200 series gates except those gates tied to FAP pin (237).
	+4 SW	324, 348, 424, 448	To pin V of 34300 and 34400 series gates except those gates tied to FAP pin (431).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A13	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused input of 41100 and 41200 series gates.
	+4 VDC	222, 250	To pin V of 41200 series gates except those gates tied to FAP pin (213).
	+4 SW	124, 148	To pin V of 41100 series gates except those gates tied to FAP pin (213).
A14	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 42100 and 42200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 42300 and 42400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 42100 and 42200 series gates except those gates tied to FAP pin (243).
	+4 SW	324, 348, 424, 448	To pin V of 42300 and 42400 series gates except those gates tied to FAP pin (333).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A15	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 35100 and 35200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 35300 and 35400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 35100 and 35200 series gates except those gates tied to FAP pin (257).
	+4 SW	324, 348, 424, 448	To pin V of 35300 and 35400 series gates except those gates tied to FAP pin (430).
A16	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 43100 and 43200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 43300 and 43400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 43100 and 43200 series gates except those gates tied to FAP pin (132 and 239).
	+4 SW	324, 348, 424, 448	To pin V of 43300 and 43400 series gates except those gates tied to FAP pin (435).

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Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A17	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 44100 and 44200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 44300 and 44400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 44100 and 44200 series gates except those gates tied to FAP pin (234).
	+4 SW	324, 348, 424, 448	To pin V of 44300 and 44400 series gates except those gates tied to FAP pin (334).
A18	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 45100 and 45200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 45300 and 45400 series gates.
	+4 VDC	150, 250	To pin V of gates 45137 through 45157, 45159, 45261, and 45262.
	+4 SW	124, 148, 224, 248	To pin V of 45100 and 45200 series gates except those gates tied to FAP pin (233) or +4 VDC.
	+4 SW	324, 348, 424, 448	To pin V of 45300 and 45400 series gates except those gates tied to FAP pin (433).

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Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A19	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 46100 and 46200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 46300 and 46400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 46100 and 46200 series gates except those gates tied to FAP pin (252).
	+4 SW	324, 348, 424, 448	To pin V of 46300 and 46400 series gates except those gates tied to FAP pin (437).
A20	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 31100 and 31200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 31300 and 31400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 31100 and 31200 series gates except those gates tied to FAP pin (246).
	+4 SW	324, 348, 424, 448	To pin V of 31300 and 31400 series gates except those gates tied to FAP pin (445).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A21	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 32000 and 32200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 32500 and 32600 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 32000 series gates except those gates tied to FAP pin (237).
	+4 SW	324, 348, 424, 448	To pin V of 32500 and 32600 series gates except those gates tied to FAP pin (454).
A22	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 47100 and 47200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 47300 and 47400 series gates.
	+4 VDC	222	To pin V of gates 47227 and 47256.
	+4 SW	124, 148, 224, 248	To pin V of 47100 and 47200 series gates except those gates tied to FAP pin (269) or +4 VDC.
	+4 SW	324, 348, 424, 448	To pin V of 47300 and 47400 series gates except those gates tied to FAP pin (332).

Table 4-XCIX. Power Distribution

Module	Voltage	Pins	Distribution
A23	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 48100 and 48200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 48300 and 48400 series gates.
	+4 SW	124, 148, 224, 248	To pin V of 48100 and 48200 series gates except those gates tied to FAP pin (126).
	+4 SW	324, 348, 424, 448	To pin V of 48300 and 48400 series gates except those gates tied to FAP pin (355).
A24	0 VDCA	112, 136, 160, 212, 236, 260	To pin G and unused inputs of 49100 and 49200 series gates.
	0 VDCA	312, 336, 360, 412, 436, 460	To pin G and unused inputs of 49300 and 49400 series gates.
	+4 VDC	250, 222	To pin V of gates 49201 through 49234 and 49255.
	+4 SW	124, 148, 224, 248	To pin V of 49100 and 49200 series gates except those gates tied to FAP pin (127).
	+4 SW	324, 348, 424, 448	To pin V of 49300 and 49400 series gates except those gates tied to FAP pin (339).

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4-5.10 DISPLAY AND KEYBOARD (DSKY).

The DSKY provides a means of communicating with the computer. It allows the operator to load information into the computer, request information, initiate various programs stored in memory, and perform tests on the computer and other subsystems of the PGNCS system. The DSKY also provides an indication of status and caution changes which may occur within the computer.

The LGC has one DSKY located on the front wall of the LEM cabin. The CMC has two associated DSKY's - one is mounted on the main display and control panel (main DSKY) in the lower equipment bay of the command module, the second is mounted on the navigation display and control panel (navigation DSKY). All three DSKY's are electrically identical. As such, the two in the command module are interchangeable.

4-5.10.1 DSKY Functional Description. The DSKY (figure 4-222) consists of a keyboard, power supply, decoder, relay matrix, status and caution circuits, and displays.

The keyboard contains the key controls with which the astronaut operates the DSKY. Each of the key controls is illuminated by 115 vac at 400 cps. Inputs to the computer initiated from the keyboard are processed by the program. The results are supplied to either the decoder and relay matrix or the status and caution circuits for display. Each key when pressed, with the exception of STBY, will produce a 5 bit code. The keycode is entered into the computer and initiates an interrupt to allow the data to be accepted. The key reset signal (+28 volts) is generated each time a key is released, the signal conditions the computer to accept another keycode. The reset code and reset signal (+28 volts) is used when the operator wishes to extinguish certain display indicators. It also allows a check to determine whether a particular indication is transient or permanent. The clear code is used when the operator wishes to clear displayed sign and digit information. Key release turns the control of displaying information on the DSKY over to the computer. The standby signal (+28 volts) initiates placing the computer into the standby mode and into the operate mode when pressed a second time.

The power supply utilizes +28 volts and +14 volts from the computer power supply and an 800-cps sync signal from the timer to generate a 250 vac, 800 cps display voltage. The display voltage is applied to the displays through the relay matrix and status and caution circuits.

The decoder receives a four bit relay word (bits 12 through 15) from channel 10 in the computer. The decoded relay word, in conjunction with relay hits 1 through 11 from channel 10, energizes specific relays in the matrix. The relays are energized by the coincidence of two signals: a selection signal from the diode matrix in the decoder which produces a row selection signal and relay bits which produce column selection signals. Relay selection allows the display voltage (250 vac) from the DSKY power supply to be routed to the proper sign and digit indicators. Relay selection also allows the alarm common (0 vdc) or +5 volts from the PGNCS system or the spacecraft

to be routed through the relay to one of the following: PGNCS system (caution signals), the spacecraft (caution signals), or proper status and caution indicators. The PGNCS caution signals from the relay matrix, represented by 0 vdc, are PGNS CAUTION, TRACKER, and GIMBAL LOCK. The status and caution indicators, illuminated by the +5 volts are: PROG, TRACKER, GIMBAL LOCK, and NO ATT. All relays associated with the relay matrix are latching type relays.

The status and caution circuits receive all status and caution signals from the computer. Each signal is applied to a driver circuit and associated relay. When a relay is energized, it allows the voltage from the DSKY power supply (250 vac), or +5 volts or 0 vdc from the PGNCS or spacecraft to be routed to the proper display indicators or equipment. The voltage from the power supply is routed through a relay to the computer activity indicator (COMP ACTY). The +5 volts is routed through relays to the following status and caution indicators: UPLINK ACTY, RESTART, OPR ERR, KEY REL, and TEMP.

The LGC status and caution signals, represented by 0 vdc or an open circuit, are ISS WARNING, STBY, LRDR POS CMD, RR AUTO TRACK ENABLE, LGC WARNING, and PGNS CAUTION.

In the CMC, the status and caution signals, represented by 0 vdc or an open circuit, are ISS WARNING, STBY, SIVB INJ. SEQ START, SIVB CUT-OFF, CMC WARNING, and PGNS - G/N CAUTION.

All relays associated with the status and caution circuits are non-latching.

The displays consist of sign and digital (operational and data display) and status and caution indicators. The sign and digital indicators allow the astronaut to observe the data entered or requested from the keyboard. The status and caution indicators present an indication of any variance from certain normal operations.

4-5.10.2 DSKY Detailed Description. The DSKY consists of a keyboard and display section, decoder, relay matrix, status and caution circuits, and power supply.

4-5.10.2.1 Keybord and Display. The keyboard section (figure 4-223) contains 10 digit keys (0 through 9) and 9 operational keys (VERB, NOUN, CLR, PRO, KEY REL, ENTR, RESET, +, and -). Except for operational key PRO, all of the keys, when pressed, generate different five-bit binary keycode which is applied to an input channel of the input-output section. In the LGC, the keycode is applied to channel 15 of the input/output section. In the CMC, the keycode from the main DSKY is applied to channel 15; the keycode from the navigation DSKY is applied to channel 16. The keycodes are shown beside their respective keys on figure 4-223. The PRO key, when pressed, generates +28 volts through key contacts to the standby circuits in the computer. This key is also used to allow the program to proceed without data in lieu of entering VERB 33. Each of the 18 keys is illuminated by 115 vac, 400 cps from the spacecraft.

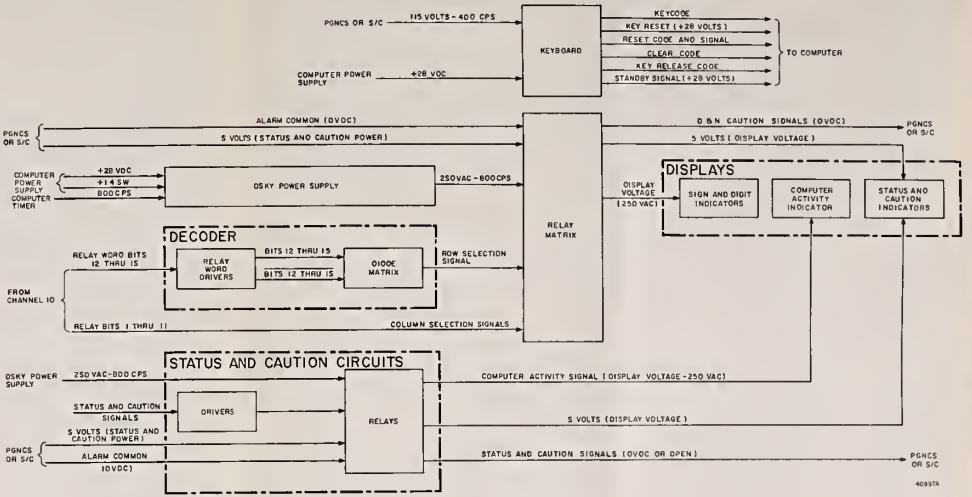


Figure 4-222. DSKY Functional Diagram

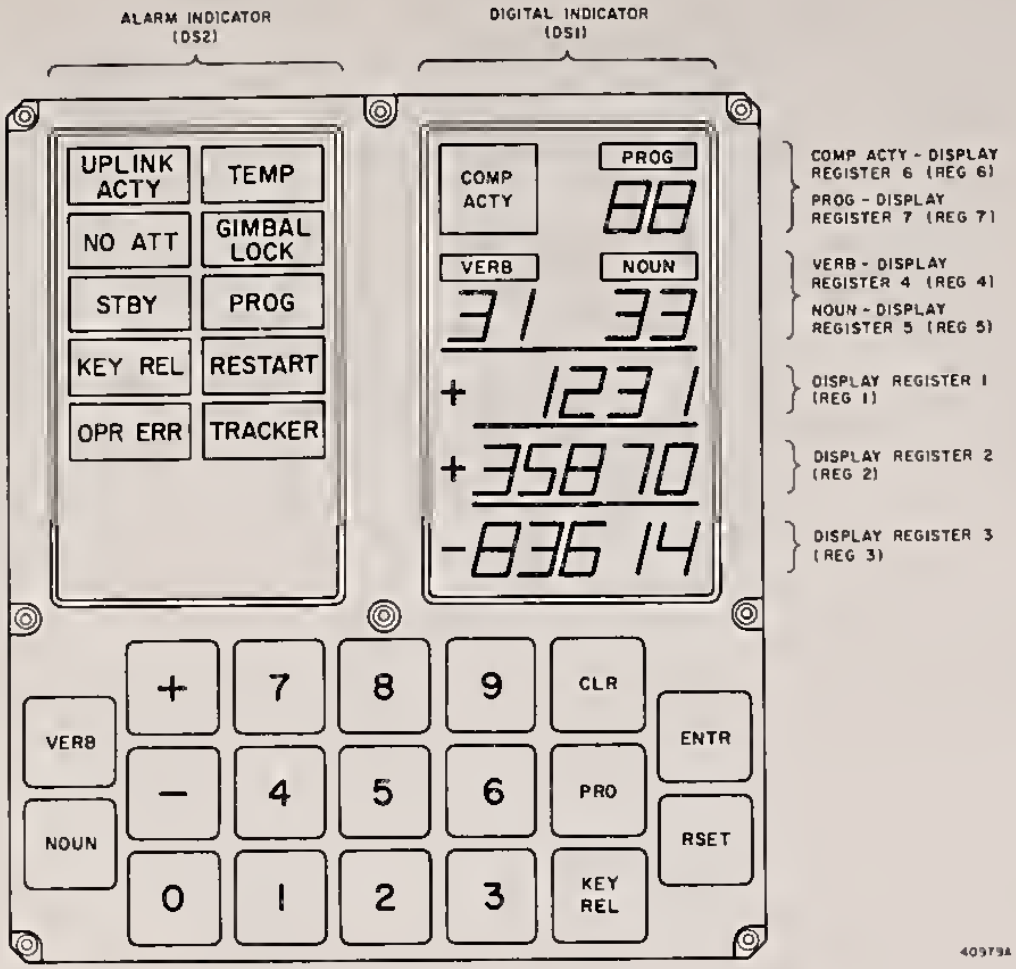


Figure 4-223. Keyboard and Display Front Panel

The key contacts (figure 4-224) are connected in series to ensure that only one keycode will be produced at one time. The binary keycode is produced by applying +28 volts through the key contacts to a diode network. The keycode initiates a program interruption (KEYRUPT) in the computer. When a key is released, signal KEYRST resets the input channel, thus clearing it for the acceptance of another keycode. A key must be released before another key is pressed to have information processed by the computer.

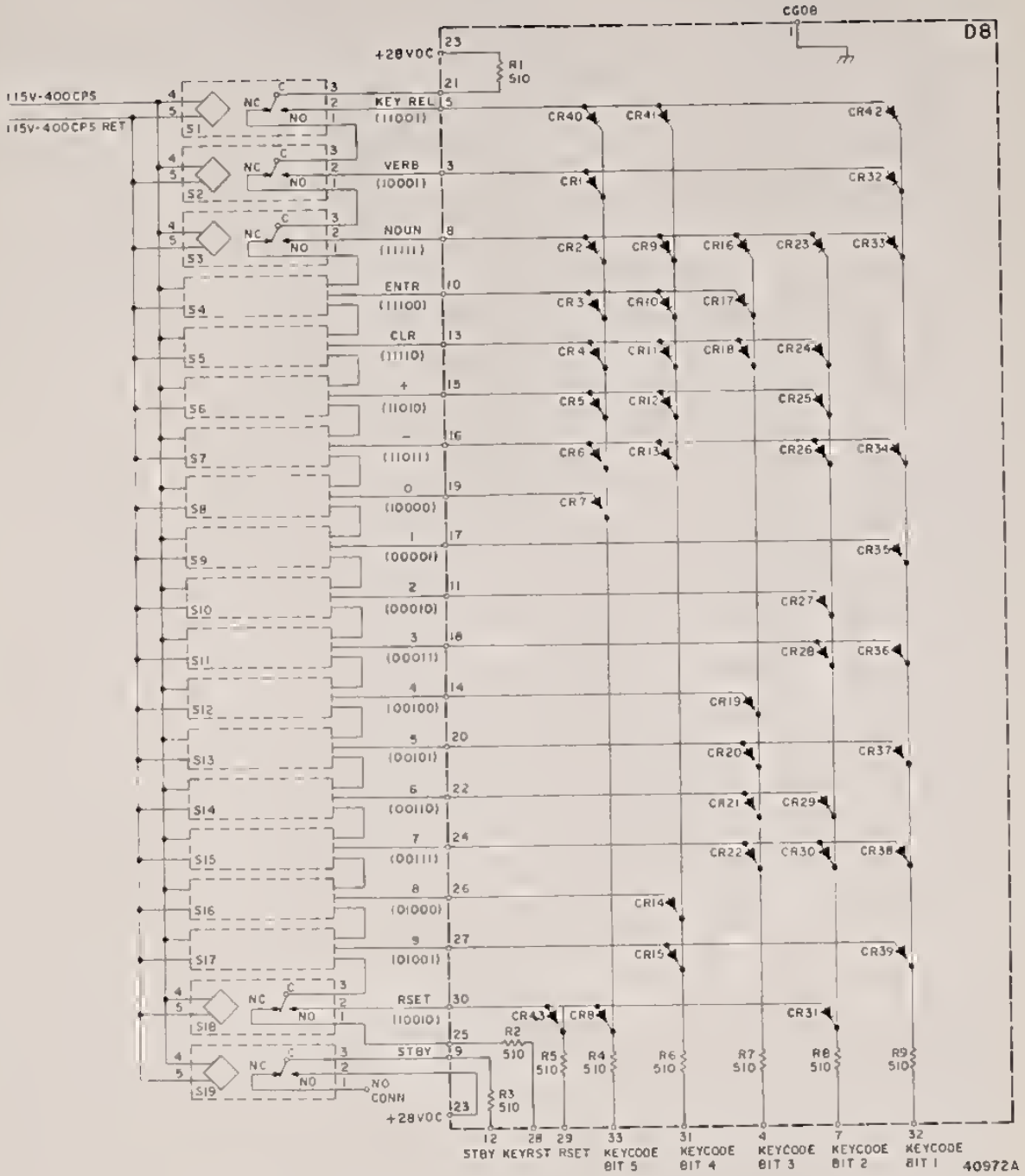


Figure 4-224. DSKY Keyboard Schematic Diagram

The display section (figure 4-223) contains 24 digit displays (21 for numerical and 3 for sign) and 15 indicators (spare included). The 24 digit displays (DS1 except COMP ACTY) and 15 indicators (DS2 plus COMP ACTY) are arranged as shown in figure 4-223. The displays and indicators are luminescent-coated-glass assemblies which glow when a voltage is applied to the coating. The displays (digit and sign) are segmented, and a display voltage of 250 vac from the DSKY power supply is applied to each segment through contacts in the relay matrix. The indicators are made in one piece. Except for COMP ACTY which receives 250 vac, all the indicators receive a display voltage of +5 volts from the spacecraft through relay contacts. The brightness of certain displays (digit, sign, and COMP ACTY) varies as a function of the voltage and frequency applied to the coating. The voltage can be varied using the brightness control on the astronauts control panel in the PGNCS. The operating controls and indicators, and their functions, are listed in table 3-VIII.

The standard procedure for communicating with the computer is to press seven keys in the following sequence: VERB-DIGIT-DIGIT, NOUN-DIGIT-DIGIT, and ENTR.

Pressing the VERB key on the keyboard clears the VERB displays on the display and indicators. The two digits punched in next are interpreted as a VERB code and displayed in the VERB section. This same operation occurs using the NOUN and two digits. The operation of the VERB-NOUN code is not initiated in the computer until key ENTR is pressed. If an error is noticed in either the VERB or NOUN before ENTR is pressed, it may be corrected by repunching either the VERB or NOUN key and the correct code.

If the VERB-NOUN combination punched in requires additional data to be furnished by the operator, the VERB and NOUN displays flash once every 1.5 seconds after the ENTR key has been pressed. The flashing indicates that the operator should punch-in the required data on the keyboard. After punching in the required data and the ENTR key, the flashing ceases.

Octal and decimal data words can be punched in. The computer assumes that an octal data word will be entered if a sign key (+ or -) is not pressed. If digit key 8 or 9 is pressed while loading an octal data word, indicator OPR ERR flashes once every 1.5 seconds. Whenever key (+) or key (-) is pressed, the corresponding signal is displayed and the computer assumes that a decimal word is to be entered. If an error is noticed while punching in either octal or decimal data, the CLR key can be pressed and the correct entry can be made if the ENTR key has not been pressed. All data words entered must be either octal or decimal; combinations of octal and decimal are not permitted.

To eliminate the flashing of indicator OPR ERR due to irregular keyboard entrys, key RSET must be pressed. In addition to the keycode, a hard wired signal (+28 vdc) is applied to the computer. Both the keycode and hard wire signal extinguish the status indicator OPR ERR as well as the five caution indicators: TEMP, GIMBAL LOCK, PROG, RESTART, and TRACKER. Thus, key RSET may also be used to test for the presence of a continuous caution rather than a transient caution condition.

4-5.10.2.2 Decoder. The decoder (figure 4-225) contains four relay word drivers (circuits 002 and 003 make up one driver), a diode matrix, and 12 row select drivers. The relay word drivers receive bits 15 through 12 of channel 10. Combinations of these

4 bits select 1 of 12 rows of relays in the relay matrix. The 12 code combinations from channel 10, are shown beside their particular row selection number on figure 4-225. For simplification only the selection of row 1 is discussed. The code for row 1 selection (0001) is inverted in the interface circuits (A25) and applied to DSKY connector J9 as signals CE228 through CE225. To identify row 1, signals CE228 through CE226 are logic ONE's and signal CE225 is a logic ZERO. A logic ONE shuts transistor Q1 off, which holds transistor Q2 off and allows transistor Q3 to conduct. Therefore, the X outputs of circuits controlled by signals CE228 through CE226 are logic ONE's, and the Y output of the circuit controlled by signal CE225 is a logic ONE.

The diode matrix receives the 8-bit output from the four relay word drivers. The matrix is wired so each 8-bit input produces a logic ONE on only one output line to the word drivers. For row 1 selection, diode CR53 of modules D2, D3, and D4, and diode CR63 of module D5 must be reverse biased. When these diodes are not conducting, row select driver circuit 004 on module D1 is activated. A current path is provided from +28 volts of the row selection driver voltage source (through transistor Q1, R8 of CKT 004, CR44, R9) to 0 vdc. Thus, parallel transistors Q4 and Q5 conduct and supply 0 vdc, representing row 1 selection, to the relay matrix.

The bottom row of diodes in the diode matrix (CR54 of modules D2 through D5) are used to detect the presence of logic ZERO's in bits 12 through 15 of channel 10. During normal operation at least one of the four diodes is forward biased and applies 0 vdc to the row selection driver voltage source. This 0 vdc is needed to supply a row selection signal (0 vdc) to the relay matrix as discussed previously. If the four most significant bits of channel 10 are ZERO's, all four diodes are reverse biased and +28 volts (+28 BCR) are applied to the input of the row selection driver voltage source. An input of +28 volts turns transistor Q2 on which in turn keeps transistor Q3 off. With no output from Q3, transistor Q1 is held off and the output of transistor Q1 is effectively an open circuit. Thus, there is no voltage source for circuit operation of any row selection driver circuit.

The indicator driver module circuits (figure 4-226) are used in making up the decoder, relay matrix, and status and caution circuits. They are introduced at this time to assist in better understanding the previously mentioned areas. All six indicator driver modules (D1 through D6) are identical and interchangeable.

4-5.10.2.3 Relay Matrix. The relay matrix (figure 4-227) consists of 11 relay bit drivers and 12 rows of latching relays.

Each relay bit driver accepts 1 of 11 bits (11 through 1) of channel 10. For simplification only bit 11 (circuit 006 on module D6) is discussed. When bit 11 of channel 10 is a ONE, it is inverted in the interface circuits (A25) and applied to DSKY connector J9 as signal CE224. A ZERO input to circuit 006 turns transistor Q8 on which switches transistor Q9 off. Thus, +28 volts is present on pin 10 (TURN-ON) of the column of relays dealing with the plus and minus sign display. With a row selection signal from the diode matrix (0 vdc) and a column select signal from a relay bit driver (+28 volts), a single relay within the relay matrix is controlled.

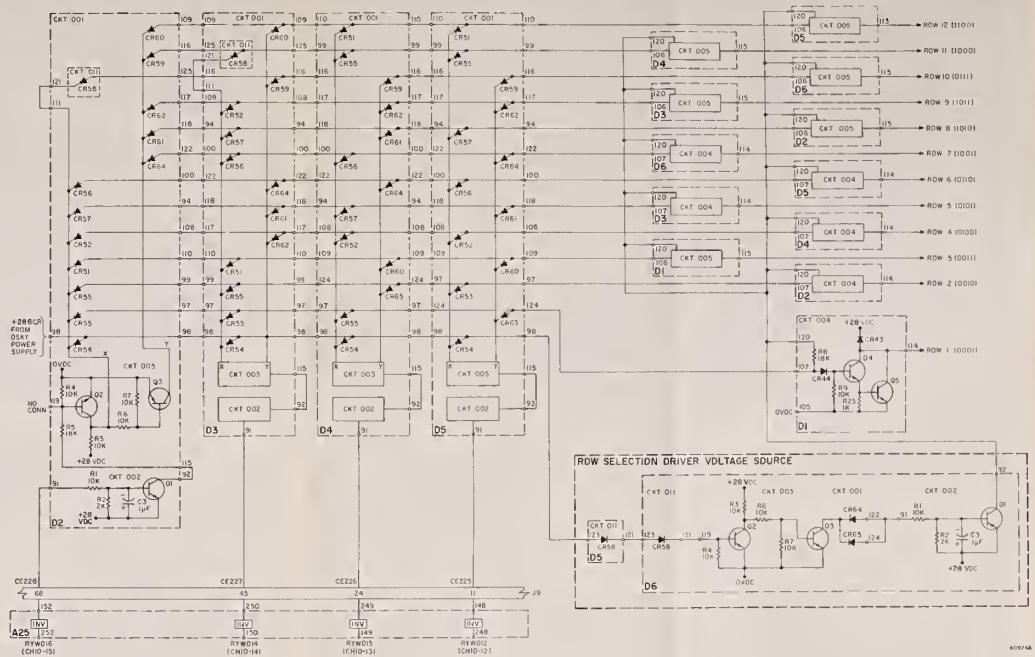


Figure 4-225. DSKY Decoder Schematic Diagram

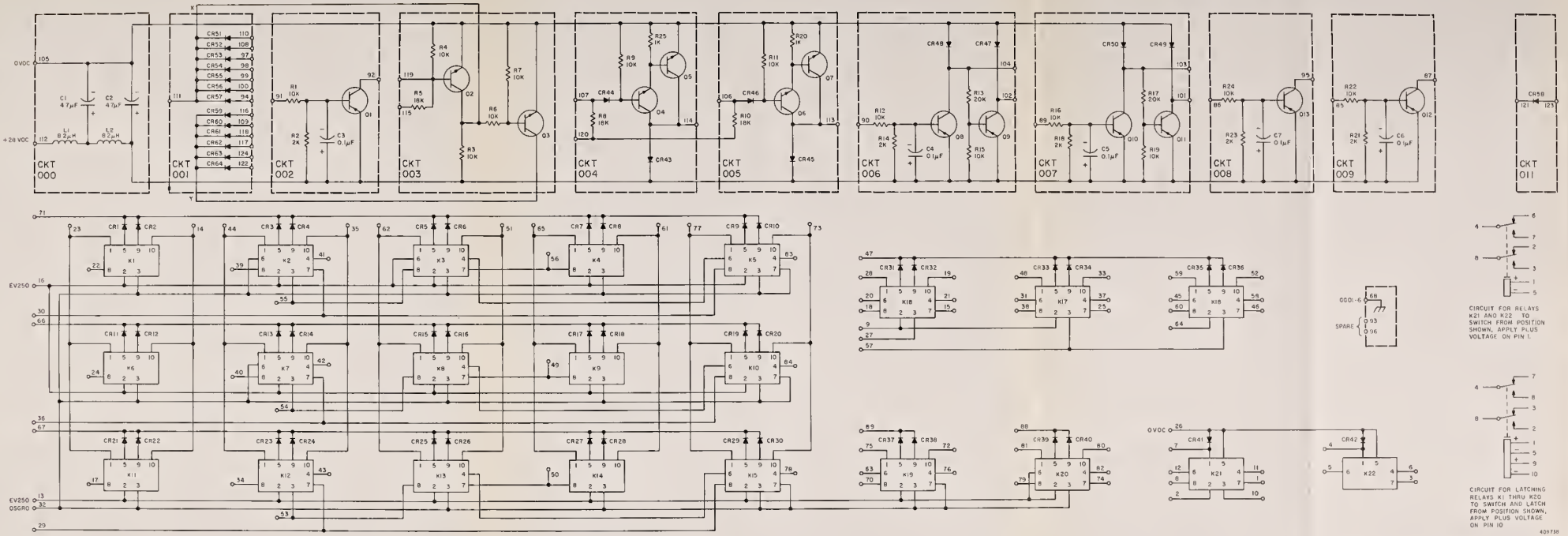


Figure 4-226. DSKY Indicator Driver Modules (D1-D6)

All of the relays in the relay matrix control the DSKY displays. Row 12 controls the indicators associated with the status and caution indicators (DS2) and, in addition, supplies a PGNS CAUTION signal to the display and control section of the PGNCS. Table 4-C relates the content of channel 10 to the row and column selected and the digit or indicator display controlled by the individual relay. Five relays are required to display one digit. Relay bit drivers 10 through 6 control the display of one digit and relay bit drivers 5 through 1 control the display of a second digit. Relay bit driver 11 causes the display of a plus or minus sign. The five-bit code necessary to display digits 0 through 9 in any display location is listed in table 4-CI. The relays representing REG3-POS1 of row 1 are used as an example. A logic ONE indicates that the relay is energized. For identification of display locations refer to figure 4-228.

Energizing the proper relays within the relay matrix (rows 1 through 11) allows approximately 250 vac from the DSKY power supply to be routed through the relay contacts to the various segments of the electroluminescent digit and sign indicators. Figure 4-229 illustrates the relays, their codes, and a display coding key.

Energizing a relay in row 12 allows +5 volts from the electrical power system in the spacecraft to be routed through the relay contacts to a status or caution indicator. Relays K16, K17, and K18 are spares. In addition, relays PROG, TRACKER, and GIMBAL LOCK receive the signal alarm common from the spacecraft and, when energized, supply signal PGNS CAUTION to the PGNCS.

Row Select	CHANNEL 10 BITS														
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	RLY WD				RLY BITS										
1	0	0	0	1	R3 -	Reg 3		Pos 2			Reg 3		Pos 1		
2	0	0	1	0	R3 +	Reg 3		Pos 4			Reg 3		Pos 3		
3	0	0	1	1		Reg 3		Pos 1			Reg 3		Pos 5		
4	0	1	0	0	R2 -	Reg 2		Pos 3			Reg 2		Pos 2		
5	0	1	0	1	R2 +	Reg 2		Pos 5			Reg 2		Pos 4		
6	0	1	1	0	R1 -	Reg 1		Pos 2			Reg 1		Pos 1		
7	1	0	0	1		Noun		Pos 2			Noun		Pos 1		
8	1	0	1	0		Verb		Pos 2			Verb		Pos 1		
9	1	0	1	1		Program		Pos 1			Program		Pos 2		
10	0	1	1	1	R1 +	Reg 1		Pos 4			Reg 1		Pos 3		
11	1	0	0	0		Spares					Reg 1		Pos 5		
12	1	1	0	0			Program	Tracker	Spare	Gimbal Lock	Spare	No Att	Spare	Spare	Spare

44144

Table 4-C. Relay Matrix Codes

Table 4-C1. Digit Code

Relays					Digit Displayed
K5	K4	K3	K2	K1	
0	0	0	0	0	Blank
1	0	1	0	1	0
0	0	0	1	1	1
1	1	0	0	1	2
1	1	0	1	1	3
0	1	1	1	1	4
1	1	1	1	0	5
1	1	1	0	0	6
1	0	0	1	1	7
1	1	1	0	1	8
1	1	1	1	1	9

4-5.10.2.4 Status and Caution Circuits. The status and caution circuits for the LGC (figure 4-230) consist of driver circuits and associated non-latching relays. For simplification only circuit 008 on module D4 is discussed. When signal ISS WARNING is a logic ZERO it will turn on transistor Q13 and supply +28 volts to associated relay K21. Relay K21 energizes and routes input signal ALARM COMMON through its contacts to the display and control section of the PGNCS as signal ISS WARNING. The driver circuits and relays associated with signals LGC WARNING, TEMP CAUTION, and RESTART also receive signal ALARM COMMON. Signal TEMP CAUTION or RESTART causes the generation of signal PGNS CAUTION which is applied to the PGNCS and also causes +5 volt caution power to be applied to the respective indicators on the DSKY front panel.

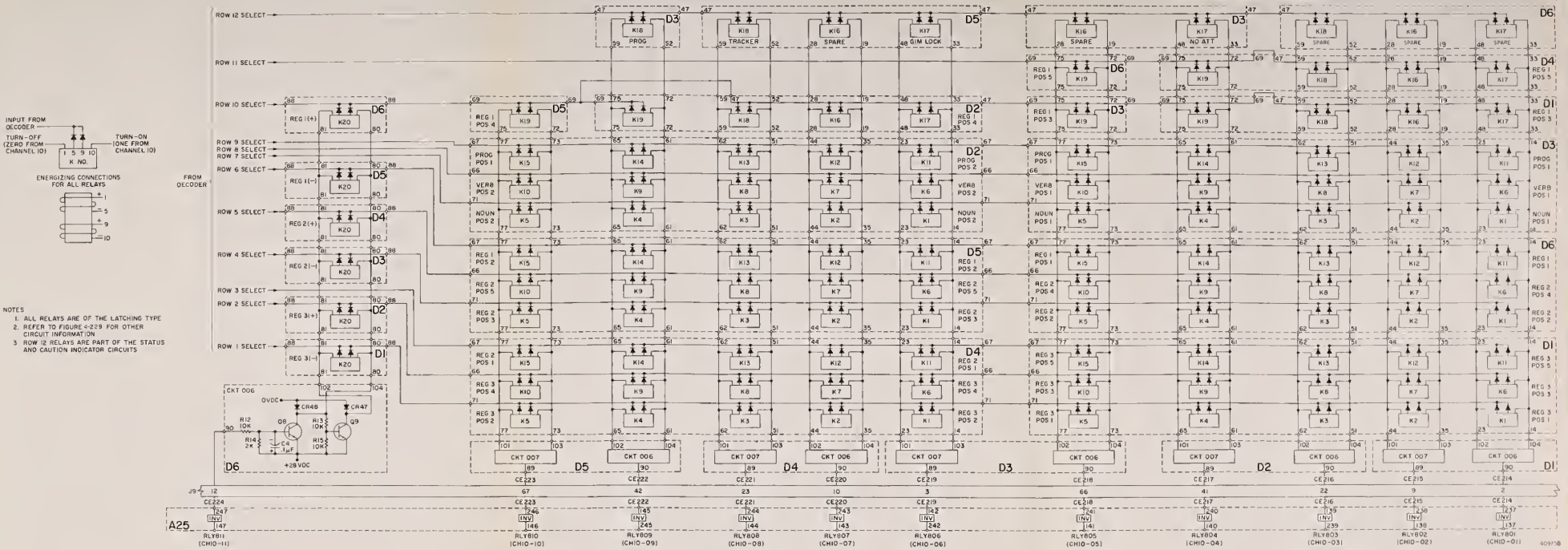


Figure 4-227. Relay Matrix Schematic Diagram

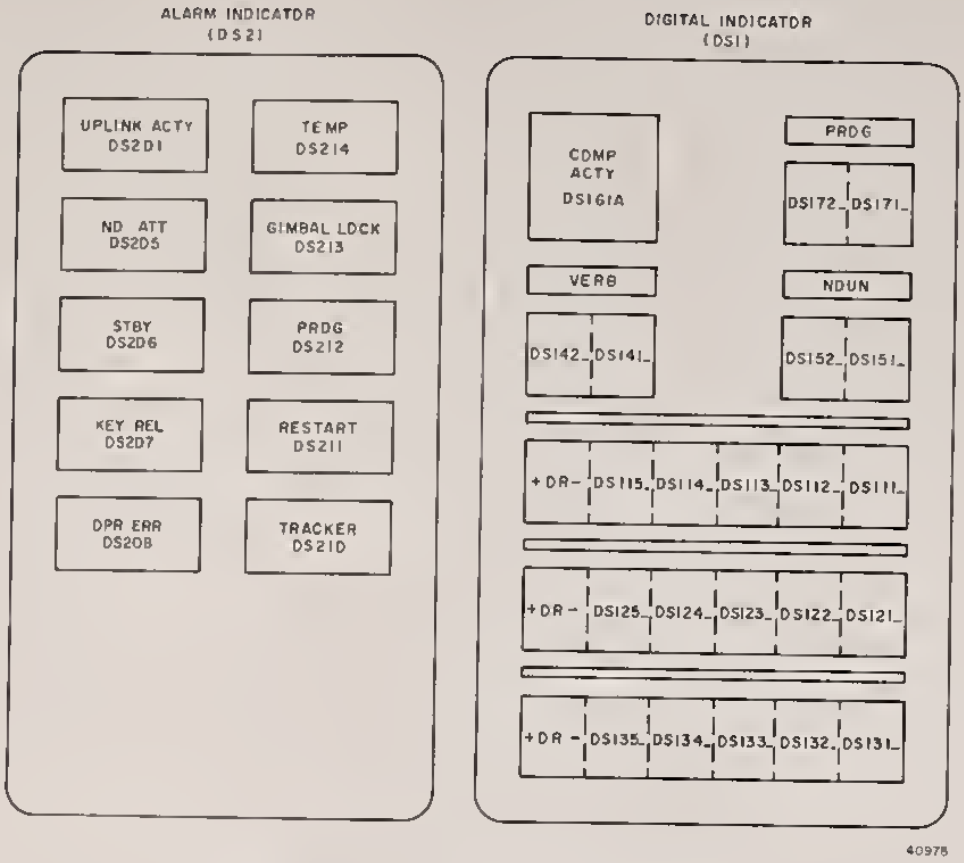


Figure 4-228. DSKY Display Locations

The driver circuits and relays associated with signals UPLINK ACTY, OPR ERROR, KEY REL, and STBY will apply, when activated, +5 volt status power to their respective indicators on the DSKY front panel. Indicators OPR ERR and KEY REL flash at a 1.5 cps rate. Indicator COMP ACTY is physically a part of digital indicator DSI. However, electrically it is part of the status circuits. When signal COMP ACTY is present, 250 vac is routed through the relay contacts to its indicator. Circuits dealing with signals RR ENABLE LOC ON, LGC WARNING, LRDR POS CMD, and ISS WARNING do not have visual indications on the front panel of the DSKY.

The verb-noun flash causes the verb-noun indicators to flash by interrupting, at a 1.5 cps rate, what normally is 250 vac being applied to the verb-noun relays in the relay matrix.

The status and caution circuits for the CMC are illustrated on figure 4-231. These circuits are identical in operation to those in the LGC. Several interface differences exist, however. These can be determined by examining the inputs and outputs to the status and caution circuits for the CMC on figure 4-231.

4-5.10.2.5 Power Supply. The DSKY power supply (figure 4-232) utilizes +28 vdc and +14VSW from the computer power supply, and 800 cps from the timer to generate a display voltage of approximately 250 vac, 800 cps. The power supply contains three transformer-coupled, push-pull amplifiers. The input to the first stage is an 800-cps square wave varying about a +14 vdc level. The dc level is controlled by the brightness control on the astronauts' control panel. Transformers T1 and T2 step up the voltage applied to their primary windings. The output from the third push-pull stage is applied to saturable reactor L2.

Reactor L2 and its associated circuit regulate the voltage applied to the displays. The displays act as a variable capacitive load that varies as a function of the number of indicators that are on. Changes in the load are reflected back to the control winding of L2 through the full-wave bridge rectifier, CR1 through CR4. As the number of indicators which are on increases, the voltage applied to the control winding is increased. An increase in voltage through the control winding drives reactor L2 further into saturation and keeps the output relatively constant. If the load decreases, the voltage through the control winding decreases, and L2 is less-saturated.

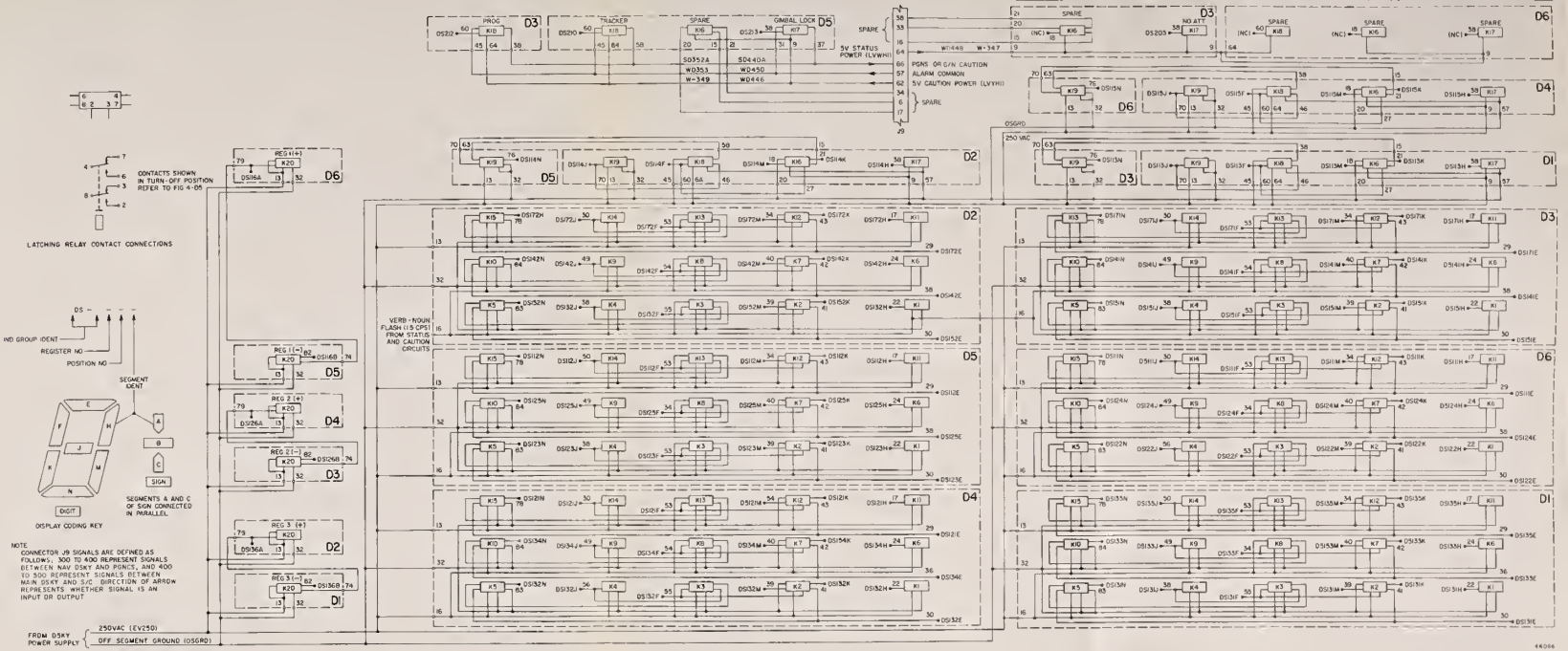
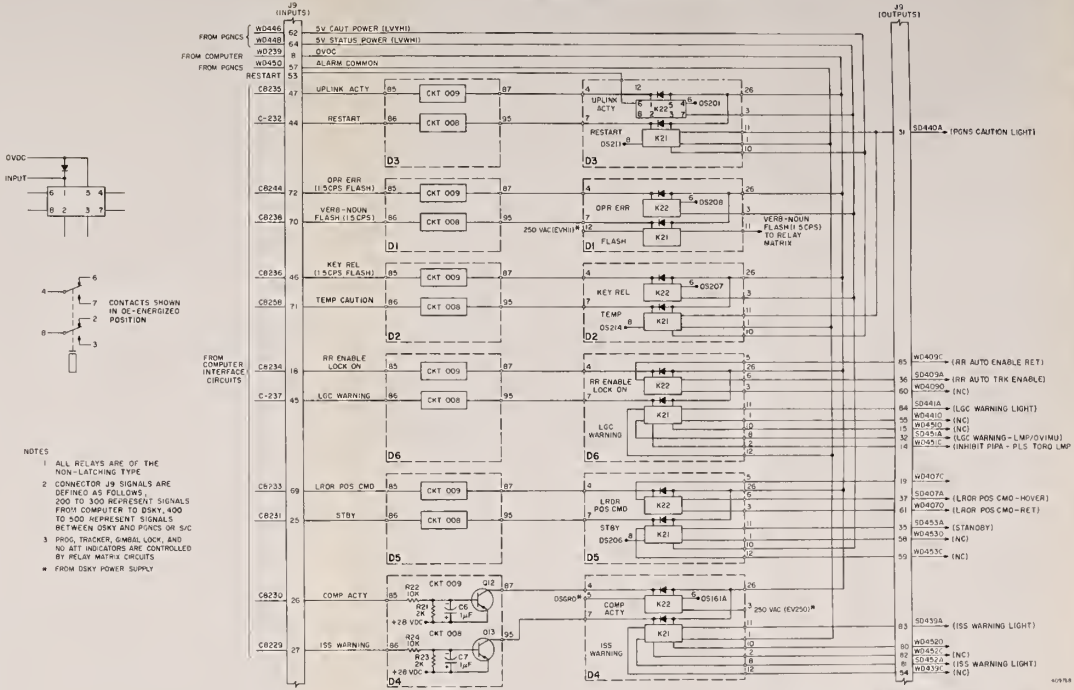


Figure 4-229. Relay Matrix Signal Flow Schematic Diagram



NOTES

1. ALL RELAYS ARE OF THE NON-LATCHING TYPE
2. CONNECTOR J9 SIGNALS ARE DEFINED AS FOLLOWS, 200 TO 300 REPRESENT SIGNALS FROM COMPUTER TO DSKY, 400 TO 500 REPRESENT SIGNALS BETWEEN OSKY AND PGNCS OR S/C
3. PROG, TRACKER, GMBAL LOCK, AND NO ATT INDICATORS ARE CONTROLLED BY RELAY MATRIX CIRCUITS

* FROM DSKY POWER SUPPLY

Figure 4-230. Status and Caution Circuit Schematic Diagram (LGC)

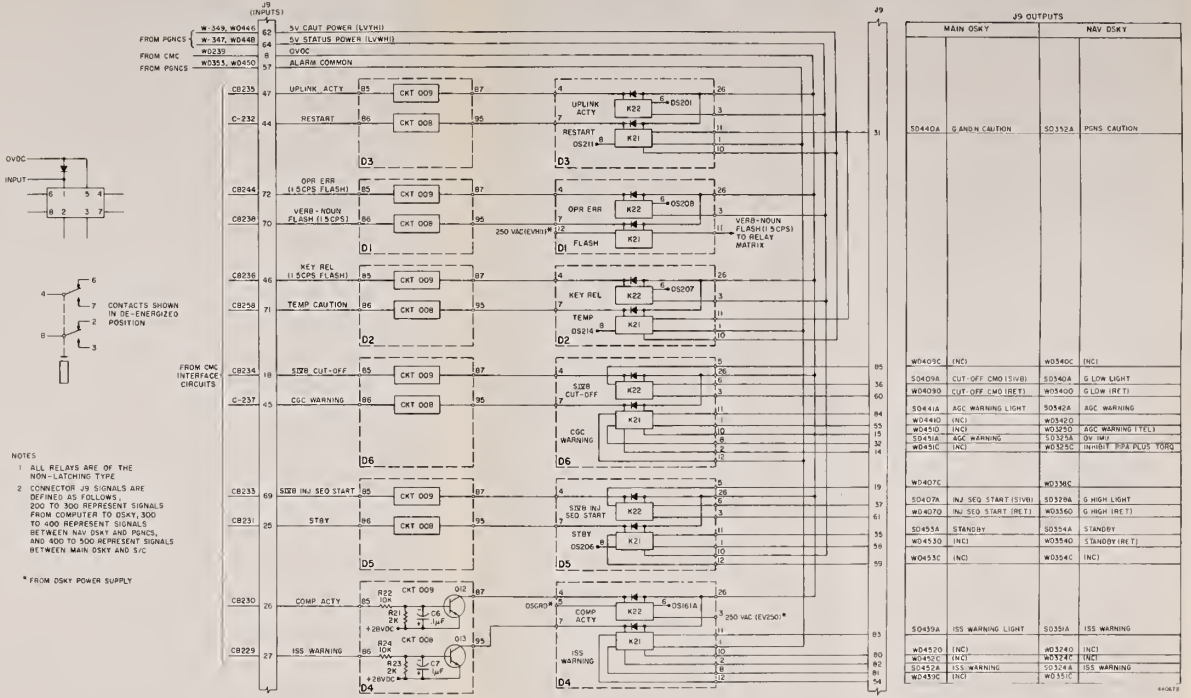


Figure 4-231. Status and Caution Circuit Schematic Diagram (CMC)

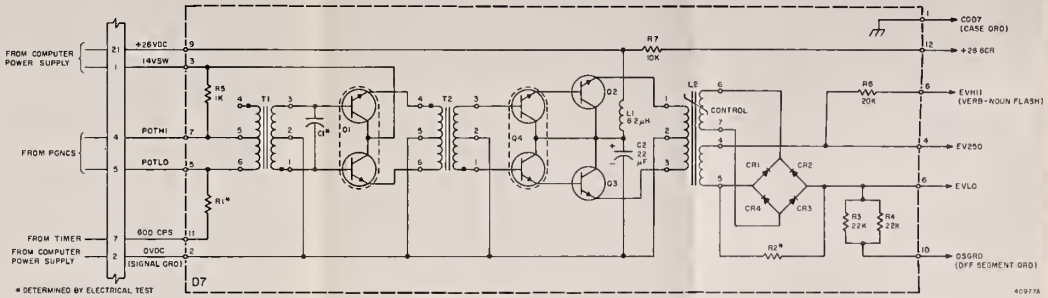


Figure 4-232. DSKY Power Supply Schematic Diagram

4-6 SIGNAL CONDITIONER ASSEMBLY

The signal conditioner assembly (SCA) receives PGNCS signals and converts each signal to a common impedance and voltage range (0 to 5 volts) acceptable to the spacecraft pulse code modulated (PCM) multiplexer or encoder. The multiplexer then transforms the conditioned signals into a form suitable for telemetry transmitter modulation. The SCA also provides isolation between the component or circuit being monitored and the telemetry system.

The SCA coneiete of either four or six modules and a mounting frame aesembly on which the modules are mounted. Two configurations of SCA ars ussd: the flight qualification SCA and the operational SCA. The primary difference bstween the two configurations is the larger number of modules in the flight qualification SCA. The flight qualification SCA contains six modules and conditions 42 PGNCS signals. The operational SCA contains four modules and conditions 26 PGNCS signals.

In addition to conditioning PGNCS signals, the SCA provides signal interface between the PSA and the PSA adapter module (PSAAM) during post-installation testing. Signals from the PSA, which are available at the SCA input connector, are hard-wired through the SCA to the PSAAM. The PSAAM, which conditions signals in a manner similar to that of the SCA, receives signals and operating voltages from the PSA. The flight qualification SCA routes 40 unconditioned PSA signals to the PSAAM, and the operational SCA routes 41 PSA signals to the PSAAM. In addition to this hard wiring, each SCA contains seven buffer resistors through which seven voltages from the PSA are routed to the PSAAM.

The SCA receives its principal operating voltages from the PSA. These operating voltages include 28 volts dc used for B+ voltage in the SCA circuits, and reference voltages consisting of ISS 800 cps and the 3,200 cps 1% feedback voltage from the IMU. Three additional reference voltages, generated in circuits within the SCA, are 2.5 volt dc bias, an 800 cps square wave, and a 3,200 cps square wave.

4-6.1 SIGNAL CONDITIONER MODULES. Each module in the SCA is designed to condition one or more types of PGNCS signals. The six modules in the flight qualification SCA are:

1) DAC, PIPA temp, and 2.5 vdc bias signal conditioner.

2) IRIG and PIPA signal conditioner.

3) Gimbal resolver signal conditioner.

4) Radar resolvers and 120 v PIPA supply signal conditioner.

5) Torque motor and 1X sine gimbal resolver signal conditioner.

6) CDU fine errors and IRIG temp signal conditioner.

The four modules in the operational SCA are:

1) DAC, PIPA temp, and 2.5 vdc bias signal conditioner.

2) IRIG and PIPA signal conditioner.

3) Gimbal resolver signal conditioner.

4) Radar resolvers and 120 v PIPA supply signal conditioner.

Table 4-CII lists the PGNCS signals conditioned by each module, the type of circuit which conditions each signal, the type of signal conditioned, and the nominal SCA output voltage for each signal conditioned.

Figure 4-233 is a block diagram showing signal flow in the operational SCA. Figure 4-234 shows signal flow in the flight qualification SCA.

4-6.2 SIGNAL CONDITIONING CIRCUITS. The modules used in the flight qualification SCA and operational SCA contain nine types of circuits. Six types of circuits condition the PGNCS signals, and three types of circuits provide reference voltages required to operate the signal conditioning circuits. The six types of signal conditioning circuits are:

1) Chopper-amplifier-demodulator.

2) Amplifier-demodulator.

3) Blocking oscillator-rectifier-filter.

4) Transformer-rectifier-filter.

5) Temperature sensor amplifier.

6) Temperature sensor voltage divider.

A 2.5 volt dc bias is applied to the output of each amplifier-demodulator and chopper-amplifier-demodulator circuit in the SCA. These circuits, which condition 0 or pi phase signals and bipolar dc signals, have an output range of -2.5 to +2.5 volts instead of the 0 to 5 volt range required for all telemetry signals. The required 0 to 5 volt output is obtained from these circuits by connecting the 2.5 volt dc bias in series with the output of each circuit, so that the 2.5 volt dc bias low becomes the common low to the telemetry system (see figures 4-233 and 4-234). The 2.5 volt dc bias high is connected to the signal output low and becomes the reference point for the 0 to 5 volt output of these circuits. In this manner a zero phase signal, after conditioning, may be represented as a dc voltage above the 2.5 volt reference. A pi phase signal, after conditioning, may be represented as a dc voltage below the 2.5 volt reference. Bipolar dc signals from the PGNCS, which may be positive or negative and have a zero volt reference, may, after conditioning, be represented in a similar manner. Positive voltages may be represented as a voltage above the 2.5 volt dc reference and negative voltages may be represented as a voltage below the 2.5 volt dc reference.

Table 4-CII. Circuits in SCA Modules

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
DAC, PIPA temp, and 2.5 vdc bias	PITCH ATTITUDE ERROR ROLL ATTITUDE ERROR YAW ATTITUDE ERROR	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc
	PIPA TEMP	Temperature sensor amplifier	Variable resistance of PIPA temperature sensor	0 to 5 vdc
	+28 VDC STANDBY +28 VDC LGC	Blocking oscillator-rectifier-filter	0 or 28 vdc discrete	0 or 4.4 vdc
	ISS 800 CPS 1%	Transformer-rectifier-filter	ISS 28 v, 800 cps power	4.3 vdc (at 28 v input)
	2.5 VDC BIAS	2.5 vdc bias supply	ISS 28 v, 800 cps power	2.5 vdc
	(two spare channels)	Transformer-rectifier-filter	None	None

(Sheet 1 of 5)

Table 4-CII. Circuits in SCA Modules (cont)

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
IRIG and PIPA	X PIPA Y PIPA Z PIPA IG SERVO MG SERVO OG SERVO	Amplifier-demodulator	3,200 cps, -45 or +135 degree phase	0 to 5 vdc
	3,200 CPS TELEM	Transformer-rectifier-filter	3,200 cps signal from isolation amplifier	4.3 vdc
	3,200 cps sine wave and 3,200 cps square wave used internally in SCA	3,200 cps isolation amplifier and multivibrator	Low voltage 3,200 cps sine wave	3,200 cps sine wave reference and 3,200 cps square wave reference
Gimbal resolver	SIN AIG 1X COS AIG 1X SIN AMG 1X COS AMG 1X SIN AOG 1X COS AOG 1X	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc

Table 4-CII. Circuits in SCA Modules (cont)

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
Radar resolvers and 120 v PIPA supply	120 V PVR	Chopper-amplifier-demodulator	High voltage dc	0 to 5 vdc
	RR SHAFT 1X SIN RR SHAFT 1X COS RR TRUN 1X SIN RR TRUN 1X COS	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc
	800 cps reference voltage used internally in SCA	Square wave generator	800 cps sine wave reference	800 cps square wave reference
Torque motor and 1X sine gimbal resolver	IMU HEATER CURRENT	Blocking oscillator-rectifier-filter	0 or 28 vdc discrete	0 or 4.4 vdc
	IMU BLOWER CURRENT	Transformer-rectifier-filter	28 v, 800 cps	4.3 vdc (at 28 v input)
	IG RSVR SIN MG RSVR SIN OG RSVR SIN	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc

Table 4-CII. Circuits in SCA Modules (cont)

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
Torque motor and 1X sine gimbal resolver (cont)	RR SHAFT FINE ERROR RR TRUN FINE ERROR			
	IG TORQUE MOTOR MG TORQUE MOTOR OG TORQUE MOTOR	Chopper-amplifier-demodulator	Positive or negative dc	0 to 5 vdc
	2.5 VDC BIAS	2.5 vdc bias supply	ISS 28 v, 800 cps power	2.5 vdc
CDU fine errors and IRIG temp	IG CDU FINE ERROR MG CDU FINE ERROR OG CDU FINE ERROR	Amplifier-demodulator	800 cps, 0 or pi phase	0 to 5 vdc

Table 4-CII. Circuits in SCA Modules (cont)

Name of Module	Name of Signal	Type of Signal Conditioning Circuit	Type of Signal Conditioned	Nominal Output Voltage Range
CDU fine errors and IRIG temp (cont)	IRIG TEMP	Temperature sensor amplifier	Variable resistance of IRIG temperature sensor	0 to 5 vdc
	PIPA CAL MOD TEMP	Temperature sensor voltage divider	Variable resistance of PIPA calibration module temperature sensor	0 to 5 vdc

(Sheet 5 of 5)

No bias is required for the blocking oscillator-rectifier-filter, transformer-rectifier-filter, temperature sensor amplifier, and temperature sensor voltage divider circuits. The normal output of these circuits is within the 0 to 5 volt range required by the telemetry system.

4-6.2.1 Chopper-Amplifier-Demodulator. The chopper-amplifier-demodulator circuit conditions negative or positive dc signals. The incoming signal is applied to a chopper circuit consisting of two dual-emitter chopper/switch transistors. The chopper modulates an 800 cps square wave reference with the dc input. The modulated square wave, which is representative of the magnitude and polarity of the dc input, is transformer-coupled to an amplifier. The amplified signal is transformer-coupled to a phase-sensitive demodulator circuit consisting of two dual-emitter chopper/switch transistors. The switching action of the transistor pairs in both the chopper circuit and the demodulator circuit is controlled by a switch drive circuit consisting of an 800 cps reference applied through a transformer to the base-collector junction of each transistor. The switch drive alternately turns on one transistor while the other transistor is turned off. The output of the demodulator is a pulsating dc signal whose magnitude and polarity are dependent upon the magnitude and polarity of the input signal. The output of the demodulator is filtered and then biased at 2.5 volts dc. This output, which could vary from +2.5 to -2.5 volts at a zero reference, as a result of the 2.5 volt reference, remains in a 0 to 5 volt range.

4-6.2.2 Amplifier-Demodulator. The amplifier-demodulator signal conditioning circuit conditions ac signals of 0 or pi phase. The circuit contains an ac amplifier and a phase-sensitive demodulator. The inputs to the amplifier and demodulator are transformer-coupled. The operation of the demodulator is similar to that in the chopper-amplifier-demodulator circuit described above. The magnitude and polarity of the demodulator output, however, is dependent upon the magnitude and phase of the ac signal, respectively. The output of the demodulator is biased at +2.5 volts dc to produce an output of 0 to 5 volts dc.

4-6.2.3 Blocking Oscillator-Rectifier-Filter. The blocking oscillator-rectifier-filter circuit conditions a 0 or 28 volt dc discrete without loading down the discrete. The PGNCS discrete is applied to a voltage-controlled blocking oscillator which includes one transistor and a three-winding pulse transformer. When the 28 volt discrete is present at the base of the transistor, the blocking oscillator goes into oscillation and produces an ac voltage across the output winding of the pulse transformer. This ac voltage is regulated at approximately 5.6 volts peak by a zener diode, rectified by a half-wave rectifier, and then filtered into an output of approximately 4.3 volts dc. When the input discrete is not present, the output of the circuit is 0 volt.

4-6.2.4 Transformer-Rectifier-Filter. This type of circuit conditions 28 volt, 800 cps or 3,200 cps power into a dc output. The ac input is applied to a stepdown transformer, rectified by a half-wave rectifier, and filtered into a dc output. The dc output voltage is representative of the magnitude of the ac input.

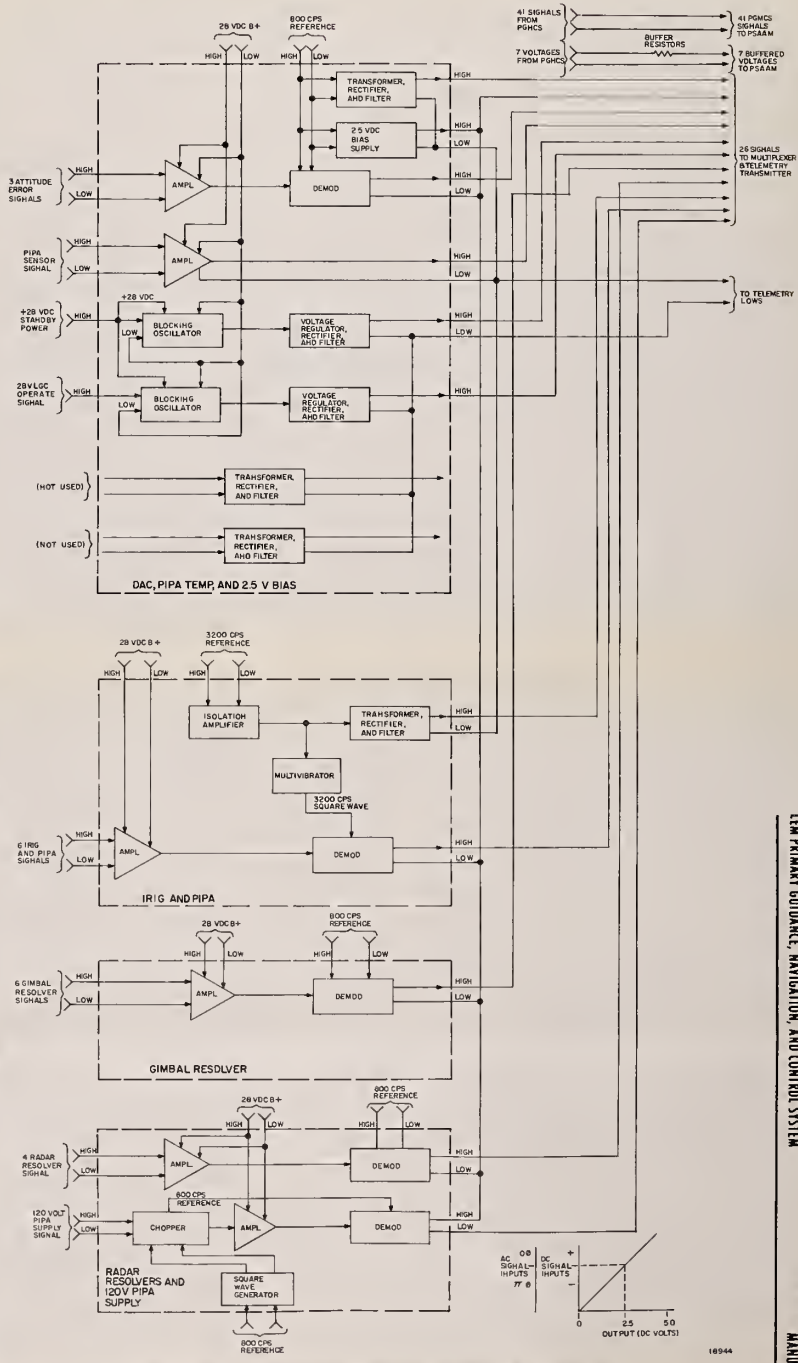


Figure 4-233. Operational Signal Conditioner Assembly, Block Diagram

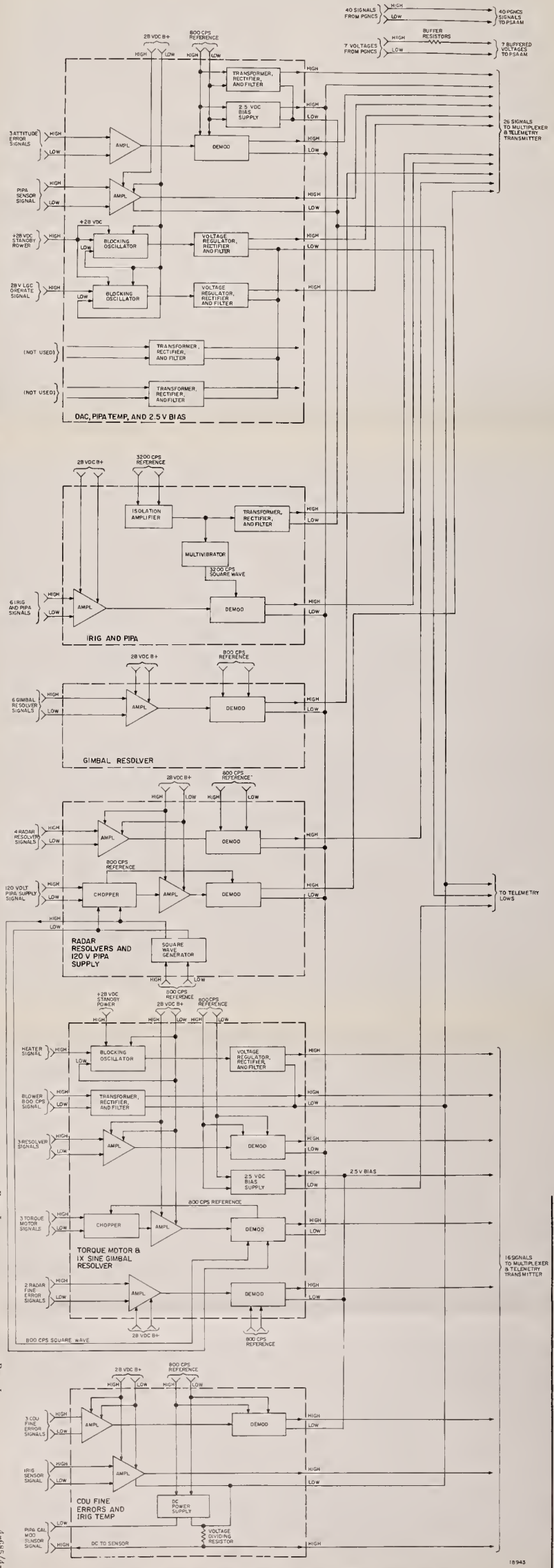


Figure 4-234. Flight Qualification Signal Conditioner Assembly, Block Diagram

4-6.2.5 Temperature Sensor Amplifier. This amplifier circuit converts the resistance value of a temperature sensor in the IMU to a representative voltage. Each temperature sensor amplifier consists of a small encapsulated module which contains an ac/dc power supply and a magnetic amplifier. The ac/dc power supply converts 28 volt dc power into ac and dc voltages required to operate the magnetic amplifier. As the resistance applied to the amplifier input varies, the amplifier produces an output in the 0 to 5 volt dc range.

4-6.2.6 Temperature Sensor Voltage Divider. This circuit produces a dc output voltage which represents the resistance value of a temperature sensing thermistor in the PIPA calibration module. The circuit consists of two functional parts: a voltage divider, and a regulated power supply which applies a fixed low voltage dc to the voltage divider.

The voltage divider consists of the thermistor in the PIPA calibration module connected in series with a resistor in the CDU fine error and IRIG temp module. The current through this series circuit varies as the thermistor resistance varies with temperature change. The output of the voltage divider is the voltage drop across the resistor in the series circuit. This output is in the 0 to 5 volt dc range.

The power supply portion of the circuit converts 28 volt, 800 cps power to a regulated dc output. The ac input is applied to a step-down transformer, rectified by a half-wave rectifier, and voltage-regulated by a zener diode. Regulated dc from the zener diode is applied to the base and collector of a transistor output stage, in which the voltage divider is connected as an emitter follower. This emitter-follower circuit maintains approximately 6 volts dc across the voltage divider.

4-6.3 REFERENCE VOLTAGE CIRCUITS. Reference voltages required to operate the signal conditioning circuits are developed in the following three types of circuits:

1) 2.5 volt dc bias supply.

2) 800 cps square wave generator.

3) 3,200 cps isolation amplifier and multivibrator.

4-6.3.1 2.5 Volt DC Bias Supply. The 2.5 volt dc bias supply provides dc bias voltage for the phase-sensitive demodulator circuits. Each 2.5 volt dc bias supply is a transformer-rectifier-filter circuit which converts 28 volt, 800 cps power into a regulated 2.5 volt dc output. The ac input is applied to a stepdown transformer, rectified by a half-wave rectifier, voltage-regulated by a zener diode, and filtered into a regulated 2.5 volt dc output.

The flight qualification SCA contains two 2.5 volt dc bias supplies which provide bias to 31 demodulator circuits. The operational SCA contains one bias supply which provides bias to 20 demodulators. The output of each bias supply is also routed to the telemetry system, so that each bias voltage may be monitored by telemetry.

4-6.3.2 800 CPS Square Wave Generator. The 800 cps square wave generator converts an 800 cps sine wave reference into an 800 cps square wave reference. The sine wave input is transformer-coupled to a two stage amplifier. The output stage of this amplifier is an emitter-follower transistor circuit which is driven to saturation, producing a square wave output. The square wave is used as a reference in the switching circuits in the chopper-amplifier-demodulator circuits.

4-6.3.3 3,200 CPS Isolation Amplifier and Multivibrator. This circuit converts a low voltage, high impedance 3,200 cps reference sine wave to a higher voltage 3,200 cps sine wave, and in addition provides a 3,200 cps square wave output. The input to this circuit, which is the 3,200 cps 1% feedback voltage from the IMU, is transformer-coupled to an amplifier consisting of a dual section transistor. The amplified signal is transformer-coupled to another dual section transistor which is in an emitter-follower circuit. The output of the emitter-follower circuit, which is in phase with the 3,200 cps input to the amplifier, is applied to a multivibrator circuit, and also is routed to a transformer-rectifier-filter circuit which conditions the 3,200 cps signal into a dc output for telemetry monitoring.

The multivibrator, which otherwise would free-run, is synchronized at 3,200 cps by the amplified sine wave input and produces a square wave output. This 3,200 cps square wave is used as a reference signal in the phase sensitive demodulators in the IRIG and PIPA signal conditioning circuits.

Chapter 5

MISSION OPERATIONS

5-1 SCOPE

This chapter describes the mission operations accomplished by the LEM PGNCS. These operations include lunar descent, landing, pre-launch, launch, rendezvous, and docking with the CSM. Figure 5-1 is an overall depiction of the LEM mission.

5-2 IMU COARSE ALIGNMENT

Before separation of the LEM and CSM, the gimbals in the IMU are coarse aligned using CSM position data and the LGC is synchronized with the CMC. To initiate IMU coarse alignment, the astronaut selects a precomputed alignment program in the LGC by pressing the required keys on the DSKY. (See figure 5-2). The LGC sends digital pulses, representing the required amount of change in gimbal angle, to a counter in the CDU. The CDU converts these pulses into an analog error signal applied to the gimbal servo amplifier which in turn drives the gimbal torque motors. As the gimbal angle changes, the gimbal resolver signal is applied to the CDU and converted to digital pulses. These digital pulses are used to cancel the LGC pulses stored in the CDU counter. As the counter is decremented to zero, the CDU analog error signal decreases to zero and the servo amplifier stops driving the gimbals. The CDU also sends digital pulses, representing the change in actual gimbal angles, to the LGC.

5-3 IMU FINE ALIGNMENT

After acceptable operation of all LEM systems is verified and the IMU is coarse aligned, the LEM is separated from the CSM. After separation, IMU fine alignment is initiated. (See figure 5-3.) The astronaut selects the fine alignment program in the LGC through the DSKY. To accomplish IMU fine alignment, the astronaut must use the AOT to sight on at least two stars. The IMU gimbals, having already been coarse aligned, are at this time relatively close to their desired angles in relation to the star coordinates. To refine the gimbal angles, the LGC sends gyro torquing signals to the IMU. The CDU interprets gimbal angle analog signals, converts them to digital pulses. and relays them to the LGC as gimbal error signals. As the gimbals are being aligned, the FDAI receives total attitude information from the IMU resolvers and attitude error information from the CDU.

5-4 TRANSFER ORBIT

Prior to powered descent to the lunar surface, the LEM must descend in coasting flight to a lower altitude. A Hohmann (minimum energy) descent orbit is commanded by the LGC after the crew has requested it through the DSKY keyboard. The LGC supplies an ON discrete to the descent engine which fires until the LEM velocity has decreased by some predetermined amount. This change in velocity (ΔV) places the LEM in a new orbit with a perilune of 50,000 feet. The accelerometer loop in the IMU senses the ΔV, and when the required velocity has been reached, the LGC furnishes an OFF discrete to the descent engine.

5-5 POWERED DESCENT

5-5.1 PHASE I - BRAKING. The crew uses the DSKY to select the powered descent program in the LGC when it is apparent that the descent orbit is successful. Braking is started approximately 200 nautical miles from the point of touchdown and is terminated approximately ten nautical miles from touchdown at an altitude of approximately 11,000 feet. (See figure 5-4.) The LGC, being constantly informed by the IMU of velocity and position, sends on-off, thrust level, and gimbal trim discretes to the Descent Engine Control Assembly (DECA). The descent engine controls the rate of descent. The gimbal trim feature of the descent engine is used to control LEM trajectory and is aided by the RCS. The inertial components in the IMU sense changes in velocity and send this data to the LGC which constantly computes new thrust level commands and gimbal trim commands. The CDU converts IMU gimbal angles into digital pulses which represent LEM attitude. The FDAI presents a constant display of LEM total attitude and attitude error.

Shortly after initiation of the braking phase, the LR begins to supply forward velocity and altitude information to the LGC to supplement and update inertially derived data. The LGC displays LR data on the ALT/ALT RATE indicator on the main control panel.

5-5.2 PHASE II - FINAL APPROACH. The final approach phase is a continuation of the braking phase with the addition of supplemental manual controlling of the LEM. More credence is placed in LR data as the LEM nears the lunar surface, where this data becomes more reliable.

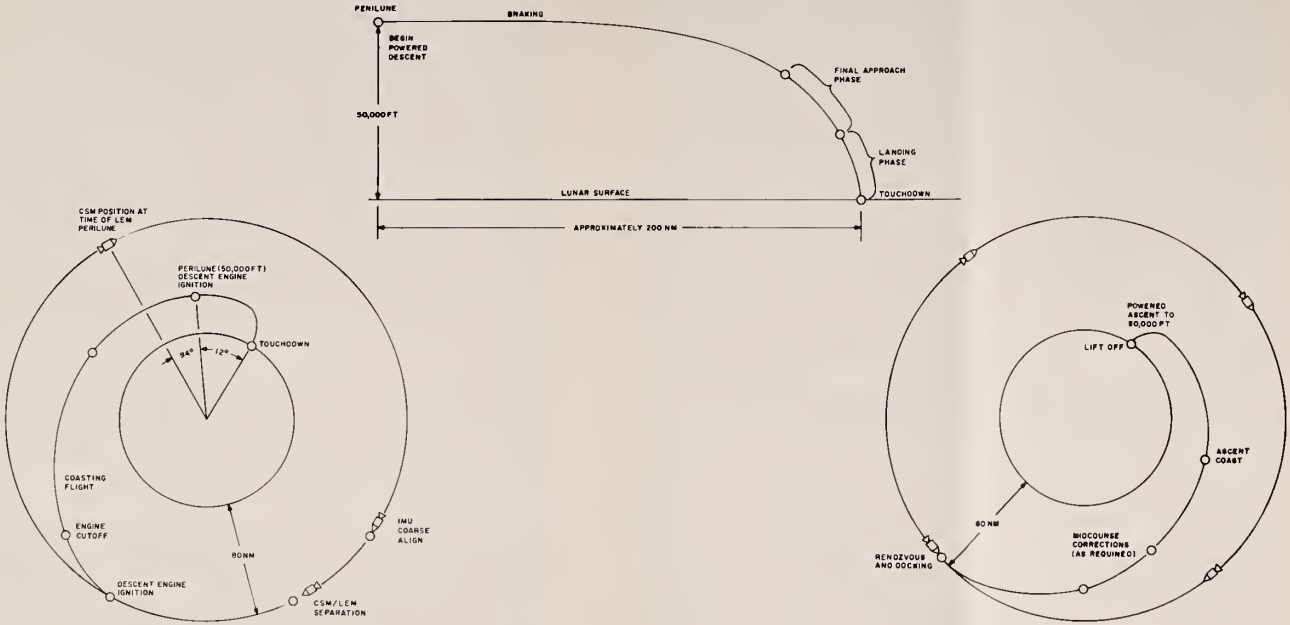


Figure 5-1. LEM Mission

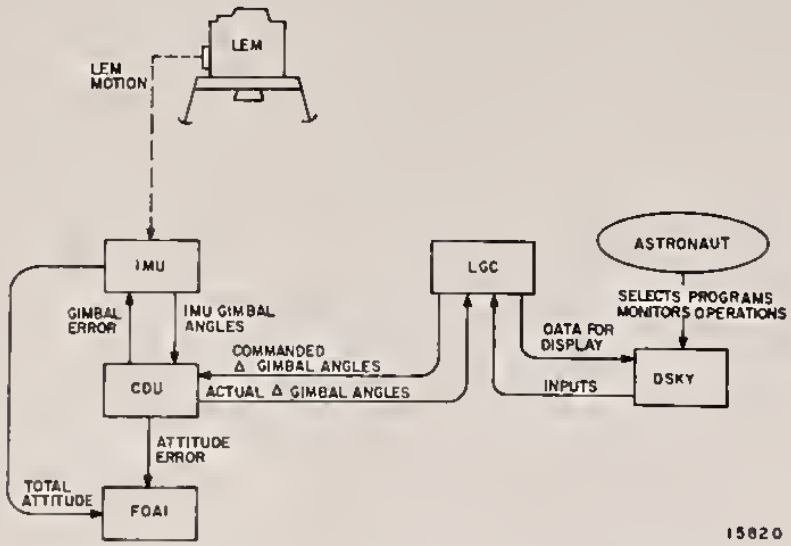


Figure 5-2. LEM IMU Coarse Alignment

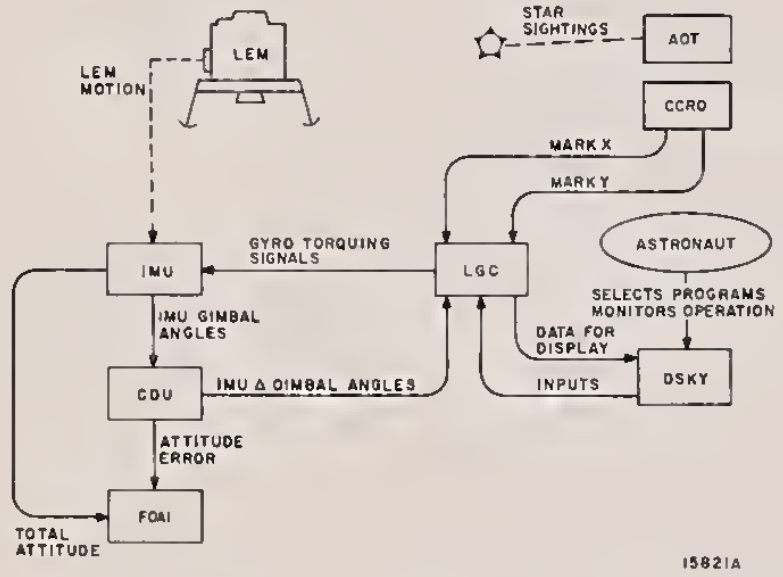


Figure 5-3. LEM IMU Fine Alignment

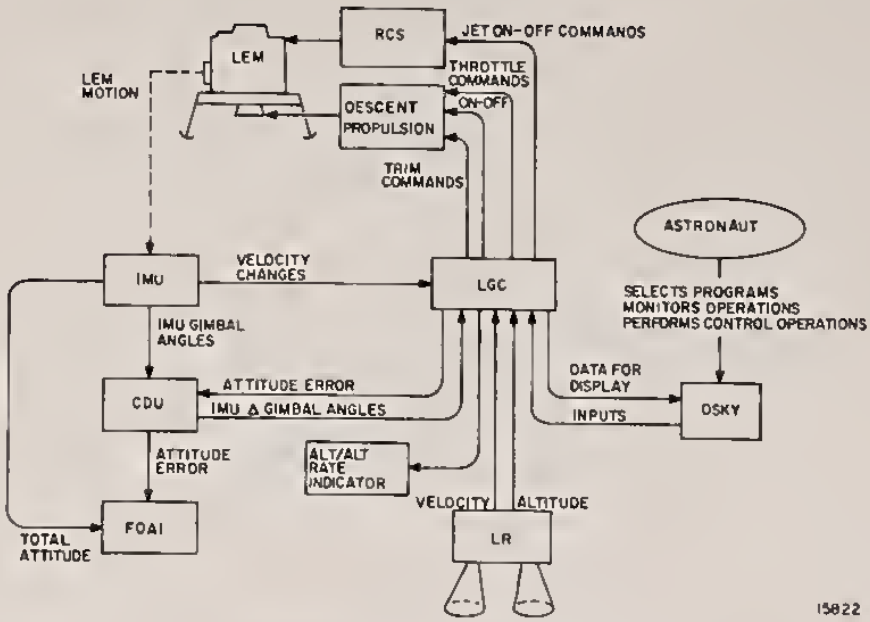


Figure 5-4. Powered Descent

Manual control of the LEM is provided by two hand controls at each crew member's station. The right hand controls, attitude controllers, are coupled through the LGC to the RCS. They are connected to the RCS in such a manner that defection of the control in any direction will fire the RCS thrusters in pairs to move the LEM about its pitch (Y), roll (Z), or yaw (X) axis. The left hand controls, integrated thrust translation controllers, serve two functions. They control translation along the LEM axes by firing the RCS thrusters and control descent by throttling the descent engine between 10 percent and 100 percent of thrust. When the two-position lever is in the JETS position, up and down movement of the control will fire a set of RCS thrusters to cause translation along the X axis. When the lever is in the THROTTLE position, up and down movement will control the thrust of the descent engine. With the lever in either position, left-right or forward-aft movement of the control will cause translation along the Y and Z axes, respectively.

> NOTE: Deflection of either of the two hand controls to their limits will provide an override capability for RCS thrusting. Limit switches at all control limits are wired directly to RCS logic circuitry.

5-5.3 PHASE III - LANDING. This phase is a continuation of the final approach phase. The LEM is positioned over the desired landing spot by controlling the rate of descent, attitude, and lateral movement. The LEM positioning is accomplished automatically or, if desired, the astronaut may assume partial or complete control by utilization of the hand controls as in phase II. Engine on-off signals are issued when zero velocity and vertical attitude is achieved at an altitude of approximately three feet, allowing the LEM to free-fall to the lunar surface.

5-6 LUNAR STAY

Immediately after landing, the astronauts perform a complete checkout of all equipment required for ascent and rendezvous with the CSM. The PLSS is checked and the surrounding lunar landscape is examined before the LEM is depressurized and the hatch is opened. One astronaut exits to perform scientific experiments and gather lunar samples. Subsequent to lunar exploration, the astronauts prepare the LEM for ascent and rendezvous with the CSM. The IMU is aligned and the ascent trajectory and launch time is determined by the LGC based on the position of the orbiting CSM.

5-7 ASCENT

A powered ascent beginning with a vertical rise and followed by a pitch maneuver will be initiated at the proper time to insert the LEM into an ascent coast trajectory to intercept the orbiting CSM. The ascent engine is a constant thrust engine with a fixed nozzle; therefore, the direction of the thrust vector is determined by the attitude of the LEM which, in turn, is controlled by the RCS upon receipt of signals from the LGC. (See figure 5-5.) Throughout the powered ascent phase, the LGC receives changes in velocity from the IMU and IMU Δ angles from the CDU. The LGC calculates the attitude errors and generates signals to position the FDAI attitude error needles and to control the RCS operation. The LGC also continues to calculate the ascent engine termination time based on the relative positions of the LEM and CSM and the calculated ascent trajectory.

5-8 RENDEZVOUS AND DOCKING

During the ascent coast period, the PGNCS remains in an inertial reference condition. The LGC receives velocity changes from the IMU accelerometer loops and IMU gimbal angles from the CDU. The PGNCS continues to calculate the actual LEM coast trajectory and issue signals to the RCS to maintain the LEM on a CSM intercept trajectory. When the LEM approaches the CSM, braking thrust maneuvers are initiated by the PGNCS utilizing the RCS, to reduce the velocity between the LEM and CSM to zero. The astronaut will then utilize the hand controls to perform the required docking maneuvers. The required thrusting during these maneuvers will be provided by the RCS.

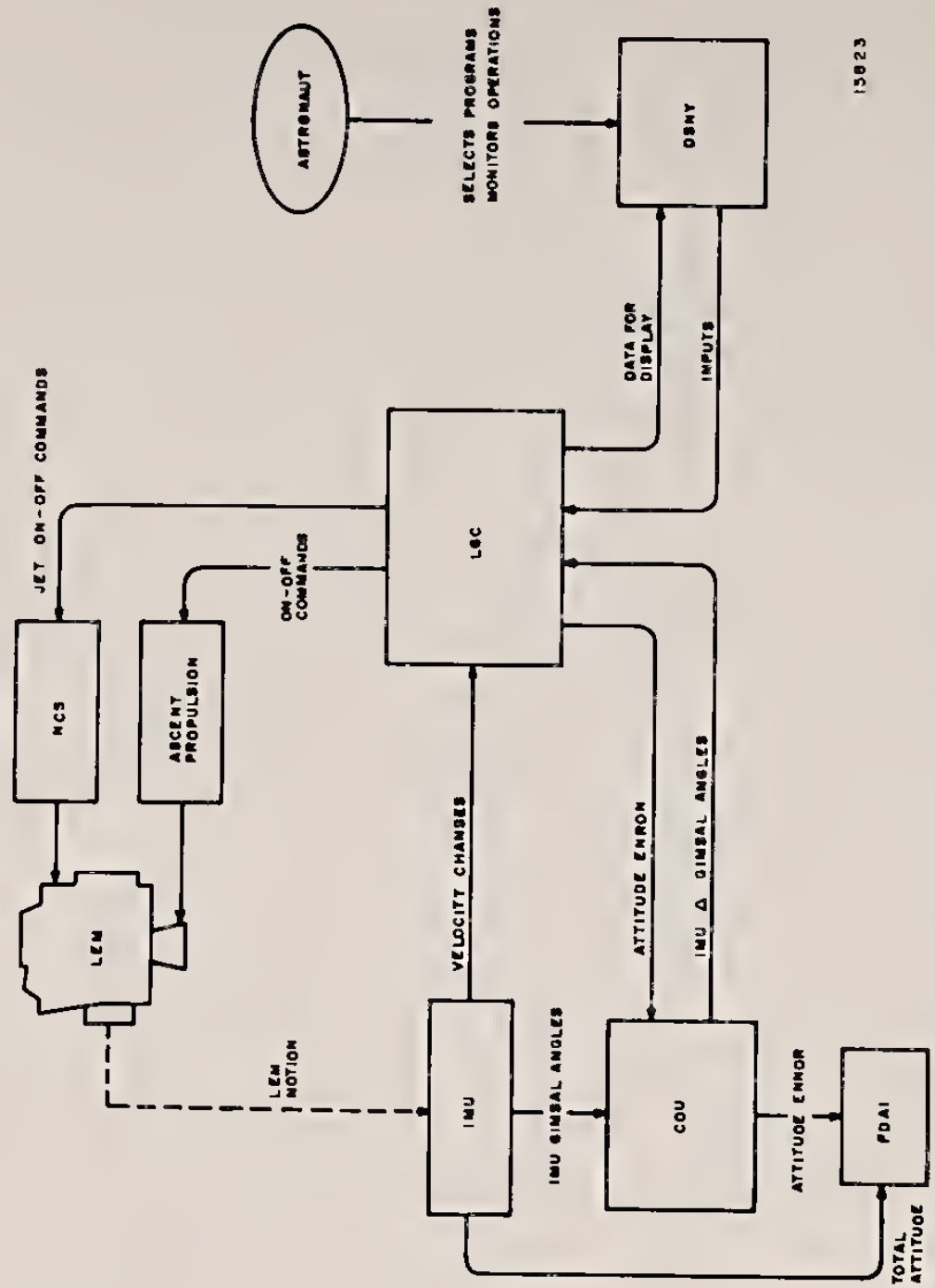


Figure 5-5. Powered Ascent

Chapter 6

CHECKOUT AND MAINTENANCE EQUIPMENT

6-1 SCOPE

This chapter contains a list of test equipment and tools necessary to complete checkout of the LEM PGNCS and the PGNCS subsystems. The test equipment is listed in alphabetical order in table 6-I. The tools are listed in alphabetical order in table 6-II. Operation and front panel calibration procedures for the GSE are contained in the job description cards (JDC's) listed in table 6-III. The layout of equipment in a typical universal test station is shown in figure 6-1. The test station is environmentally controlled and provides for precision checkout of the PGNCS and the PGNCS subsystems.

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
Apollo guidance computer (AGC) auxiliary calibration console, 2014059-021	Auxiliary calibration system	Checks calibration of LGC clock oscillator.
AGC CTS operation console, 2014024-021	AGC/OC	Provides mounting and cooling surfaces, power and test connections for checking out CSS.
AGC/GSE interconnect set, PGNCS, 2014255-041 and -051	AGC/GSE interconnect cables, PGNCS	Provides cables and buffer circuits to interconnect LGC to GSE during PGNCS checkout.

(Sheet 1 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
AGC/GSE interconnect set, subsystem, 2014268-031	AGC/GSE interconnect cables, CSS	Provides cables and mounting braeket to interconnect LGC to GSE during CSS checkout.
AGC handling fixture, 2014282-031	AGC handling fixture	Provides mounting and protection for LGC prior to installation and during handling.
AGC test set, 2014042-061 and -071	Computer test set (CTS)	Checks operation of CSS.
AGC universal DSKY handling fixture 2014013-011	DSKY handling fixture	Provides protection and handling capability of DSKY during transfer, test, and storage. Also provides a means of mounting DSKY in AGC/OC.
AGC calibration system console, 2014049-021	Calibration system	Checks calibration of LGC clock oscillator and provides frequency reference to auxiliary calibration system.
Alignment optical telescope tester, 6014003	AOTT	Provides optical targets and functional references for alignment ehecks of AOT.
Alignment optical teleseope tester assembly certification kit, 6014008	AOTT cert kit	Provides calibrated mechanical and optical references required for setup and alignment.
AOT lens covers, 6014056-011	AOT lens covers	Protects AOT lens from external damage.
AOT conneetor cover, 6014319-011	AOT conneetor eover	Protects AOT conneetor P1 during shipping or when eonnector is not connected to a cable assembly.

(Sheet 2 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
Component mounting plate, 6900007-021	Component mounting plate	Provides mounting for DSKY and support and cooling capability for LGC, CDU, and PSA during testing.
Computer simulator, 2014048-011	Computer simulator	Simulates LGC signals, loads, and outputs for ISS checkout.
Connector cover set, 6900001-031	Connector covers	Provides protection for electrical connectors of PGNCS harness.
Degausser, 1900299-021	Degausser	Demagnetizes ducosyns of 16 PIP's and 25 IRIG's during ISS checkout.
Electrical adapter cable assembly set, 2901075-021 and 6900077-011		Provides cable breakout capability for signal monitoring, and resistance and continuity testing.

(Sheet 2A of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
G and N transport cart, 1900009-041	G and N transport cart	Used for local transportation of PGNCS components.
G and N coolant and power console, 1902134-031	Coolant and power console	Provides cooling, power and precision voltage monitoring during PGNCS and ISS checkout.
GSE coolant interconnect hose set, ISS/OSS, 2900405-011	GSE coolant hoses	Connects PGNCS components and coldplates to coolant and power console.
GSE distribution box, 2900024-031	GSE distribution box	Provides test interconnection for use during PGNCS and subsystem checkout.
IMU lifting and handling fixture, I015462-011	IMU lifting fixture	Provides means of positioning IMU and IMU mounting fixture on rotary table.
IMU lifting temperature controller, 2900063-031	LTC	Provides heater power to IMU inertial components during LEM stacking.
IMU mounting fixture, 2900000-021	IMU mounting fixture	Mounts IMU to rotary table for ISS checkout.
IMU pressure seal tester 1900804-011	IMU pressure seal tester	Checks for leakage of pressure seals in IMU case during PGNCS checkout.
IMU snap-on bellows, 1900802-011	IMU snap-on bellows	Allows for expansion of coolant in IMU case during transportation when filled.
Interconnect cable set, 2900025-031	Interconnect cables	Interconnects PGNCS components and GSE during PGNCS and subsystem checkout.
Interconnect cable set, special (LEM), 6900043-051	Interconnect cables	Interconnects PGNCS components and GSE during PGNCS and subsystem checkout.

(Sheet 3 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
LGC connector covers, 2014399-011 1006425-006	LGC connector covers	Provide protection for LGC and DSKY electrical connectors during transit or storage.
Lifting battery pack, 2900812-031	LBP	Part of IMU lifting temperature controller to provide backup heater power.
Optics cleaning kit, 1019984-021	Optics cleaning kit	Used to clean AOT optics.
Optics-inertial analyzer, 2900023-051	OIA	Provides control signals and monitoring and measurement facilities for PGNCS and subsystem checkout.
Oscillograph console, 1900000-021	Oscillograph	Monitors and records signals from OIA.
Portable temperature controller, 2900060-031	PTC	Provides power for IMU temperature control when normal power is not applied.
PSA adapter module, 6900088-031	PSAAM	Buffer between PGNCS and ACE for post-installation testing.
PSA test point adapter, 2900037-031	PSA test point adapter	Provides test interconnections for use with OIA for monitoring purposes.
Programmer and monitor interconnect set, 2014064-011	P and M interconnect set	Provides extra set of cables to connect CTS to buffer circuit assembly at a universal test station.
PTA/PEA mounting fixture, 2900066-021	PTA/PEA mounting fixture	Provides mounting for PTA on rotary table during PGNCS and ISS testing.
PTA/PEA test point adapter, 2900145-011	PTA/PEA test point adapter	Provides signal select capability for monitoring signals from PTA during PGNCS and ISS testing.
Purging and filling fixture, 1902371-011	Purging and filling fixture	Purges and fills IMU and GSE coldplates requiring coolant.

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
Resolver circuit tester, 2900708-011	Resolver circuit tester	Provides simulated resolver signals and monitoring facilities for testing PGNCS resolver circuits.
Rotary table 1900926-021	Rotary table	Serves as a mounting and test platform for selected PGNCS components during PGNCS and ISS testing.
Rotary table calibration set, 1900810-011	Rotary table calibration set	Contains all equipment necessary to perform rotary table calibration.
Signal conditioner assembly and PSA adapter module calibration unit, 2900895-041	SPCU	Provides regulated dc excitation source, simulated load and input source impedance, scales input signals, and regulates 800 cps and 3200 cps signals for testing five types of signal conditioner assemblies.
Subsystem mounting fixture, 2900070-021	Subsystem mounting fixture	Supports portions of PGNCS and GSE during ISS and PGNCS testing.
Theodolite, 1017444	DKM 3X	Serves as telescope and autocollimator to measure and transfer bearings.

(Sheet 5 of 5)

Table 6-II. Checkout and Maintenance Tools

Equipment and Part Number	Short Nomenclature	Description and Use
AGC sling; MY-4 Abbot Jordan Hoist Co., Brighton, Mass.	computer sling	Connects lifting hoists to LGC when transporting LGC outside of LGC shipping container.
Allen adapter; 5/32 inch, JO Line, or equivalent	allen adapter	Adapts torque wrench to LGC module inserts.

(Sheet 1 of 2)

Table 6-II. Checkout and Maintenance Tools

Equipment and Part Number	Short Nomenclature	Description and Use
Torque wrench; 17 inch-pound, JO Line, or equivalent	torque wrench	Torque LGC modules onto LGC trays.
Tool kit	tool kit	Contains general usage tools required to support maintenance activities in G and N laboratory and stockroom.

(Sheet 2 of 2)

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Auxiliary input panel	18050	Operation - general
	18103	Operating primary signal selector and auxiliary input panels to apply auxiliary signals to digital voltmeter, phase angle voltmeter, dual beam oscilloscope and counter.
	18104	Applying PSA test point adapter signals to dual beam oscilloscope through auxiliary input panel.
	18204	Applying PSA test point adapter and PTA/PEA test point adapter signals to dual beam oscilloscope through auxiliary input panel.

(Sheet 1 of 7)

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Counter	18017	Forward and reverse count.
	18018	Count number of input events that occur during any preselected time interval.
	18019	Count number of input events that occur during interval determined by "D" input events.
	18020	Count clock frequency pulses that occur during interval determined by "D" input events.
	18021	Determine correct operation of N_1 switches, time-base circuitry, and count-chain circuitry.
	18022	Determine correct operation of N_2 switch.
	18103	Applying auxiliary signals.
	19261	Performance verification.
Current source monitor panel	18216	Measure voltages.
Digital recorder	18043	Operation and interpretation of data.
Digital voltmeter	18000	Applying internal signals.
	18002	Applying PSA test point adapter signals.
	18037	Automatic measurement of ac or dc voltage.
	18103	Applying auxiliary signals.
	18202	Applying PTA/PEA test point adapter signals.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Digital Voltmeter (cont)	18235	Measurement of dc voltage.
	18236	Measurement of ac voltage.
	19260	Performance verification.
Dual beam oscilloscope	18000	Applying internal signals.
	18001	Applying reference signals.
	18002	Applying PSA test point adapter signals.
	18005	Voltage measurements using upper beam differential amplifier.
	18006	Phase shift measurements using upper beam differential amplifier.
	18007	Time measurements.
	18008	Frequency measurements.
	18009	Pulse monitoring using scope B, channel 1.
	18010	Applying two signals simultaneously to scope B.
	18011	Applying oscillograph signals to scope B, channel 2.
	18103	Applying auxiliary signals.
	18104	Applying PSA test point adapter signals.
	18202	Applying PTA/PEA test point adapter signals.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Dual Beam Oscilloscope (cont)	18204	Applying PSA test point adapter and PTA/PEA test point adapter signals.
	19263	Performance verification.
	19360	Adjustment of scope B lower beam vertical plug-in unit.
	19361	Adjustment of scope B lower beam vertical plug-in unit.
	19362	Adjustment.
Electrical adapter cable assembly set	18053	Signal monitoring and continuity testing.
Fill and purge fixture	18045	Fill and purge G and N system components.
Galvanometer	18216	Measure voltages.
G and N coolant and power console	18046	Operation and interconnections for G and N system, ISS and OSS testing.
Gimbal position control panel	18244	General operation.
Inertial components temperature controller	18049	Provide IMU heat.
Oscillograph	18011	Applying signals to dual beam oscilloscope, scope B, channel 2.
	18023	Electric writing.
	18024	Ink writing.
	18026	Operation of dc amplifiers.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Oscillograph (cont)	18027	Adjustment of phase sensitive demodulators (800 cps reference).
	18028	Adjustment of phase sensitive demodulators (3200 cps reference).
	18031	Operation of phase sensitive demodulators.
	18032	Installation of ink cartridge.
	18033	Installation of ink pen.
	18034	Installation of paper.
	19264	Performance verification of dc amplifiers.
	19265	Performance verification of phase sensitive demodulators.
	19268	Performance verification of phase sensitive demodulators.
Phase angle voltmeter	18000	Applying internal signals.
	18002	Applying PSA test point adapter signals.
	18038	Measurement of total rms voltage.
	18039	Measurement of fundamental rms voltages.
	18040	Measurement of phase angle.
	18041	Measurement of in-phase and quadrature components.
	18042	Indication of phase sensitive null.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Phase Angle Voltmeter (cont)	18103	Applying auxiliary signals.
	18202	Applying PTA/PEA test point adapter signals.
	19262	Performance verification.
	19266	Performance verification.
Primary signal selector panel	18000	Applying internal signals to digital voltmeter, phase angle voltmeter, and dual beam oscilloscope.
	18001	Applying reference signals to dual beam oscilloscope.
	18002	Applying PSA test point adapter signals to dual beam oscilloscope, phase angle voltmeter, and digital voltmeter.
	18005	Voltage measurement on dual beam oscilloscope of signals through primary signal selector panel.
	18103	Applying auxiliary signals through auxiliary input panel to digital voltmeter, phase angle voltmeter, dual beam oscilloscope, and counter.
	18104	Applying PSA test point adapter signals through auxiliary input panel to dual beam oscilloscope.
	18202	Applying PTA/PEA test point adapter signals to dual beam oscilloscope, phase angle voltmeter, and digital voltmeter.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Primary signal selector panel (cont)	18204	Applying PSA test point adapter and PTA/PEA test point adapter signals through auxiliary input panel to dual beam oscilloscope.
PSA test point adapter	18002	Applying signals through primary signal selector panel to digital voltmeter, phase angle voltmeter, and dual beam oscilloscope.
	18104	Applying signals through auxiliary input panel and primary signal selector panel to dual beam oscilloscope.
	18204	Applying PSA test point adapter and PTA/PEA test point adapter signals through primary signal selector panel and auxiliary input panel to dual beam oscilloscope.
Signal generator	18012	Signal generator adjustment.
	18013	Signal generator operation.

(Sheet 7 of 7)

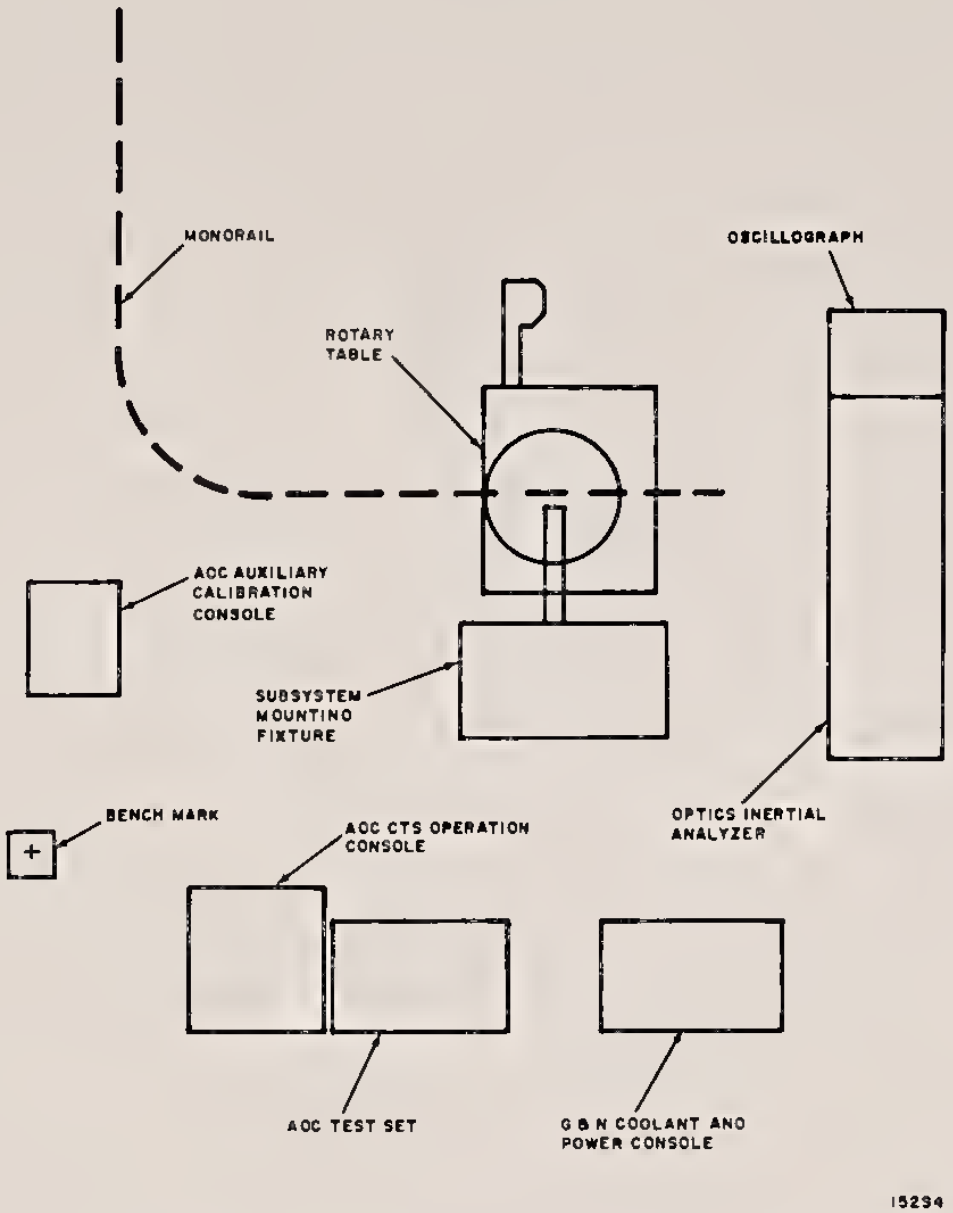


Figure 6-1. Typical Universal Test Station Layout

Chapter 7

CHECKOUT

7-1 SCOPE

This chapter contains flowgrams which outline checkout procedures for the LEM PGNCS and the PGNCS subsystems. Checkout is performed at the G and N laboratories of North American Aviation (NAA), Kennedy Space Center (KSC), Grumman Aircraft Engineering Coproration (GAEC), and the Manned Spacecraft Center (MSC). A master flowgram for the PGNCS and one for each of the PGNCS subsystems precedes more detailed preparation and checkout flowgrams. Each master flowgram references the detailed flowgrams which, in turn, reference the job description cards (JDC's) required to fulfill the checkout function. The detailed flowgrams also refer to JDC's which describe setup and operation of GSE. Flowgrams and JDC references are also provided for pre-installation acceptance (PIA) tests.

Information regarding packing, shipping, handling, and storage of any component of the PGNCS will be found in Packing, Shipping, and Handling Manual, ND-1021038.

7-2 PRIMARY GUIDANCE, NAVIGATION AND CONTROL SYSTEM

7-2.1 PREPARATION. Table 7-I lists PGNCS components and GSE required for PGNCS and subsystem checkout. Tables 7-IA and 7-II list required system and GSE interconnect cabling.

7-2.2 CHECKOUT. The PGNCS master flowgram (figure 7-1) specifies the conditions leading to a PGNCS checkout and displays the mandatory sequence to be followed. Detailed flowgrams (figures 7-2 and 7-3) give sequential listings of JDC's to be performed.

7-2.3 TEST DESCRIPTIONS. Detailed descriptions of the PGNCS checkout tests performed by using the JDC's are provided in the following paragraphs.

7-2.3.1 Master Initialization. This procedure establishes proper initial conditions, after system turn-on, required for the performance of various system tests.

The temperatures of the IRIG and PIPA are measured in voltages, each volt being equivalent to 2^{o}F. The 2 volt, 3200 cps GSE ducosyn frequency and voltage comparator, the 28 vdc prime power voltage comparator, and the 60 cycle, 3 phase voltage

comparator are measured to insure that they are within tolerances. By entering a sequence of instructions into the DSKY, all erasable locations are zeroed and the IMU gimbals are coarse aligned at zero.

7-2.3.2 Standby Control Test. During this test the 28 vdc standby bus voltage, 3200 cps suspension power, LGC master clock sync, +4 and +14 vdc LGC power supplies, and IRIG and PIPA standby temperatures are checked.

Initialization of this test consists of applying power to the LGC, placing the ISS in the standby mode, and obtaining an input bus voltage of 28 vdc. This primary 28 vdc input bus voltage is obtained by setting the CROSSBAR CONTROL switches on the primary signal selector panel and adjusting the G & N POWER ADJUST control on the test control panel.

The IMU standby bus voltage is measured to insure that voltage is available for use in the IMU temperature control system, the magnetic suspension system, and the LGC.

The IRIG and PIPA temperatures and the difference between the temperatures are obtained by measuring the temperature deviation voltage. One hour after entering the standby mode, which allows time for the IRIG and PIPA temperatures to stabilize, the CROSSBAR CONTROL switches are set and the IRIG and PIPA instantaneous temperature deviation voltages are recorded. These voltages are equivalent to two degrees per volt. The calculated temperature is added to the nominal IRIG temperature and nominal PIPA temperature to obtain the actual IRIG and PIPA temperatures. The absolute temperature difference is then obtained by subtracting the actual PIPA temperature from the actual IRIG temperature.

Proper operation of the ducosyn magnetic suspension system must be verified before power can be applied to the IRIG wheel motors. Verification is accomplished by setting the COUNTER INPUT "D" SIGNAL selector switch on the primary signal selector panel and measuring the 3200 cps suspension power frequency on the counter. A counter indication of 1,000,000 counts corresponds to the magnetic suspension power frequency of 3200 cps. The CROSSBAR CONTROL switches are then set to measure the 3200 cps suspension power feedback voltage.

The LGC master clock sync, which supplies synchronization pulses to the PGNCS power supplies, is checked. The LGC master clock sync is connected to the computer test set (CTS) counter and the frequency is monitored for 15 minutes (9 printouts on the printer) to insure that the frequency does not deviate by more than the amount specified by the JDC. Printouts of 1024000 correspond to the LGC master clock frequency of 1024 kcps. The LGC master clock sync is then connected to the CTS oscilloscope and the amplitude, width, rise time, and noise of the signal are measured to insure that proper synchronization pulses are being developed by the LGC.

The LGC +4 and +14 vdc power supply outputs are used within the LGC to provide necessary power for LGC operation. If the LGC is in the standby mode, the power

supplies are inhibited and should not produce outputs. When the LGC is placed in the operate mode, the power supplies are enabled and should produce outputs which are then measured on the DVM by setting the CROSSBAR CONTROL switches on the primary signal selector panel.

7-2.3.3 Operate Control Test. This test provides an operate control test for IMU time delay; gimbal ambiguity; 1X sine and cosine signals; standby to operate temperature transient; 800 cps power supply thermistor; temperature monitor 1 thermistor; PIPA calibration module thermistor; auto cage, inertial temperature control point; heater telemetry discrete; blower telemetry discrete; and normalization.

Prior to starting this test, the ISS must be in the standby mode with the LGC power on for a minimum of 2 hours. This warmup allows time for the ISS to be temperature stabilized. The prime power is adjusted for 28 vdc. The IMU time delay test is performed by measuring the time required for the ISS to upmode from standby to operate. This time delay, which is gyro runup time, should be 90 seconds with tolerance specified in the JDC. During the 90 second delay period, the IRIG and PIPA pulse torque power supply is inhibited. Loss of +28 vdc LGC prime power at any time causes the power supply to be inhibited.

During automatic caging and CDU ambiguity operation, the IMU gimbal resolvers drive the 1X sine signals to zero volt rms and the 1X cosine signals to 28 volts rms, with the IMU gimbal angles initially at 225°.

With the ISS in the operate mode and the IMU gimbals coarse aligned to 0°, the PIPA temperature is checked during the first 15 minutes after switching from the standby to the operate mode. The PIPA temperature must be within 0.5° of its stabilized value. The IRIG temperature is checked 30 minutes after switching to the operate mode. The IRIG temperature must also be within 0.5° of its stabilized value. The stabilized values of the PIPA and IRIG temperature must be 130.5°F and 135°F respectively plus tolerances specified in the JDC. The temperature is considered stabilized when it changes less than 0.1°F in 30 minutes.

In order to test the 800 cps power supply, the temperature monitor 1, and the PIPA calibration module thermistors, the resistances of the following thermistors are measured:

Thermistor	Location	PSA TPA	Tol (ohms)
800 cps, 5%, P/S	PSA	TB5-12 and 13	2.21K to 8.37K
Temp mon 1	LGC (erasable driver)	TB5-14 and 15	1.4K to 13.25K
PIPA cal mod	PIPA cal mod	TB1-31 and 27	3.65K to 13.25K

The heater telemetry discrete is checked during the ON cycle. Voltage at the interface is 26.5 vdc with tolerance specified in the JDC. The blower telemetry discrete cycles on and off with a heater duty cycle of approximately 45 percent. The ON state is 0 volt rms and the OFF state is 28 volts rms.

7-2.3.4 G&N System Operational Test. This test is a gross check of the PGNCS operation. The test consists of a computer/DSKY interface test (performance of a computer controlled DSKY test to verify correct DSKY character displays), a manual DSKY keyboard test (verification of correct key-character display operation), an alarm and interrupts test (checks computer program error sensing capabilities), and a computer controlled test of PIPA and IRIG operation. The PIPA's are checked by positioning the OG, IG, and MG at 45^{o}; each PIPA then senses a portion of local gravity. The cumulative reading should be the value of local gravity. IRIG performance is checked by measuring the horizontal component of earth rate (cos λ). The PIPA and IRIG tests are performed at normal, low, and high prime power voltage levels with the LGC self check being performed concurrently.

The tests are initiated with the system in ISS standby and the computer operating. The computer/DSKY interface test, which is the ±11 option of the self check, checks the electroluminescent displays on the DSKY. This list is initiated by entering VERB 21 (load component 1), NOUN 27 (self test on/off switch), and 00011 into the DSKY. The test illuminates all operation and data display elements on the DSKY for 5 seconds each. The operator must watch the DSKY for the proper displays specified in the JDC. Next, VERB 35 (test lights) is entered into the DSKY to illuminate all DSKY caution and alarm display panel lights concurrently for 5 seconds, after which the caution and alarm lights go out, leaving ±88888 in row 1, row 2, and row 3.

The manual DSKY keyboard test is initiated by entering VERB 24 (load component 1, 2), NOUN 01 (specify address, fractional), address 01700, +12345, and -67890. The DSKY is observed for the following display: +12345 in row 1 and -67890 in row 2. The test is completed by pressing CLR twice so that row 1 and 2 are blank.

The alarm and interrupts test checks the following LGC detection circuits using appropriate DSKY inputs:

Parity fail

Rupt lock

TC trap

Night watchman.

Each detection circuit generates a restart in the LGC when an error is detected. The restart is displayed as follows: RESTART condition, PGNCS, and G/N CAUTION lamps lighted; DSKY row 1, row 2, and row 3 display 00000. The RSET pushbutton is pressed and VERB 36 (fresh start) is entered into the DSKY after each detection circuit is checked.

The PIPA and IRIG tests are initiated by placing the ISS in the operate mode and adjusting prime power to 28 vdc as measured at the PSA input by the DVM. The LGC self check is performed during the 90 second standby to operate time delay by entering

VERB 21, NOUN 27, and address 77767. After the 90 second time delay has been completed, the closure of the PIPA loop is verified by (observing) a butterfly pattern on the PIPA monitor oscilloscope. Then the test is continued by entering VERB 57 (perform system test) and address 00004 (IMU check).

In approximately 12 minutes VERB 06 (decimal display) and NOUN 66 (system test results) flash, and row 1 and row 2 display the local gravity vector (cm/sec^2) measured by the PIPA's. VERB 33 (proceed without data) is entered, and when VERB 06 and NOUN 66 flash again the horizontal component of earth rate (cos λ), as measured by the IRIG's, is displayed in row 1 and row 2. The local gravity and earth rate indications are recorded and compared with specification tolerances. The PIPA and IRIG test is repeated with the prime power adjusted to the low voltage limit, and to the high voltage limit.

7-2.3.5 LEM PGNCS Power Supply Test. This test checks the amplitude, frequency, and phase relationship, as applicable, of the LEM PGNCS power supplies.

A master initialization condition is established per JDC 12613 to zero the IMU gimbals and eliminate the possibility of LGC operation while this test is being performed. Prime power is adjusted to 28 vdc and the system is allowed to operate for 15 minutes to stabilize the prime power. The CROSSBAR CONTROL and DVM are used to measure the following voltages:

1) 28 volts, 800 cps, 1%
2) 28 volts, 800 cps, 5%, AØ, BØ
3) ECDU +4 vdc
4) -28 vdc
5) X, Y, Z PIPA 28 vdc
6) 28 volts, 3200 cps, 1%
7) LGC +4 vdc
8) LGC +14 vdc
9) 28 vdc LGC operate
10) 28 volts, 800 cps reference voltage
11) 120 vdc pulse torque electronics.

Using the counter, test point adapter 2, and primary signal selector panel, the frequencies of the following voltages are measured to insure that they are within tolerance: the IMU 28 volt, 800 cps, 1% power supply output and the 28 volt, 3200 cps feedback signal. The peak-to-peak amplitude of the 3200 cps, 1% power supply is measured using the auxiliary panel and the dual beam oscilloscope. The time difference is measured between the leading edge of the 3200 pps set pulse (ØA -3 usec) input to the 3200 cps power supply and the first positive going zero crossover of the 28 volt, 3200 cps power supply output.

Using the phase angle voltmeter and test point adapter 2, the phase angle between phase A and phase B of the IMU 28 volt, 800 cps, 5% power supply is measured, where phase A = -90^{o} and phase B = -180^{o}. The above voltages and frequencies are measured twice, once at the lower limit and once at the upper limit of prime power input.

The LGC +4 and +14 vdc power supplies are checked at the test selector for out of tolerance outputs, using the interface load test and the CROSSBAR CONTROL.

7-2.3.6 Gimbal Response Test. The gimbal response test measures the amount of torque motor current required to keep a gimbal moving and detects the frictional restraints of a gimbal. Also included with the gimbal response test is a step response test used to verify stabilization loop response after displacing the IRIG floats from null.

A master initialization is established per JDC 12613. To prevent unnecessary cycling of the gyro torque enable relay, bit 2 of location 00370 is set to logic 1 (continuous gyro torque enable).

Before gimbal torquing begins, static loop parameters of the following signals are measured: the in-phase gimbal error signal for each gimbal and the total voltage of the gimbal torque drive amplifiers for each gimbal.

IRIG torquing signals are supplied by the LGC through commands received through the DSKY, and the outer and inner gimbals are rotated plus and minus 360 degrees and the middle gimbal is rotated plus and minus 135 degrees. During the slew periods the fine and coarse CDU errors and gimbal torque motor current are monitored on the oscillograph to verify gimbal response and CDU operation.

The IRIG floats are initially displaced from null by applying 10, 5, and 5 vdc step inputs to the test input of the gimbal servo amplifier. The signal is removed after reaching a steady state. The time required for the servo error to reach a constant value is measured as an indication of loop response (within 5% of steady state value not exceeding 0.1 second). The number of overshoots after the test signal is removed are counted as a measure of loop stability. The number of oscillation peaks occurring before reaching and staying within the 5% band are measured. To measure response time and number of oscillations (a measure of damping coefficient), the oscillograph is set to a sensitivity which gives a 1 mm deflection equal to 5% of the steady state value.

7-2.3.7 LEM Signal Conditioner Functional Test. This test description will be incorporated upon completion of in-process revisions.

7-2.3.8 LGC Output Test. This test checks the discrete outputs of the RCS jet and SCS command interface, and the pulse train outputs of the main engine command, altitude meter, landing radar, rendezvous radar, and downlink interface.

The semi-automatic interface check and high speed radar sampling test routines check a portion of the input-output control circuitry. Evaluation of these checks is

performed by observing the frequency and waveform measurements on the CTS and observing the DSKY and DCVM. Interfaces checked during the semi-automatic interface test are as follows:

1) Pitch, yaw, and roll RCS jets

2) Engine on and engine off

3) Pitch and roll gimbal trim

4) LR position command

5) RR enable automatic track

6) Increase and decrease throttle rate for descent engine commands

7) Altitude meter

8) Altitude rate meter

The sequence for checking these interfaces is programmed so that, once the test is initiated, the test advances from one phase to another by pressing ENTR.

During the high speed radar sampling test, the LGC/LR and LGC/RR waveforms and frequencies are measured. The CTS oscilloscope and counter are used to measure waveform characteristics and time lag between various pulses. All signals measured are selected on the channel S and T signal selector switches of the CTS XY interface panel. In addition to waveform and time lag measurements, the LR and RR range and velocity data counters are addressed and the data is displayed on registers 1 and 2.

The CTS oscilloscope and counter are also used to measure waveform characteristics and time lag between various pulses of the downlink telemetry.

7-2.3.9 LGC Input Test. This test checks all LEM S/C inputs to the LGC. All S/C inputs to in-bits of channels 16, 30, 31, 32, and 33 as well as the rotational hand controller and uplink data inputs are simulated by the CTS at the S/C interface. The results are checked by interrogation of LGC channels and registers.

After master initialization per JDC 12613, all spacecraft input signals to in-bits of channels 30, 31, 32, 33 and 16 are simulated by the CTS at the S/C interface. This test is to insure that the S/C input signals are received by the LGC and, also, to insure that the signals create the desired response within the G&N system. Rotational hand controller input signals are also simulated by the CTS and the reaction within the G&N system is monitored for each signal.

The uplink data input signals are tested by preparing an inlink tape, using the keyboard in the tape prepare mode. The tape is prepared per instructions given in the

JDC. The tape is read (press EXECUTE) into the LGC inlink counter (erasable assignment 00045). When overflow occurs (bit 16-1), pinball will display the contents on the DSKY. This test verifies that the uplink telemetry is being received by the LGC and that the G&N system is reacting accordingly.

7-2.3.10 Semiautomatic Mode Test. This test is designed to verify the IMU CDU and RR CDU moding, CDU repeating accuracy, CDU command accuracy, CDU command rate, FDAI linearity test, and RR velocity meter test. The test is under LGC program control but provides operator control intervals to make analog measurements.

The test is initiated by performing JDC 12613 and by entering sequence number 00010 allocated for the semiautomatic mode check. VERB 33 always appears in the VERB window during the test; the NOUN window indicates the number of the program sequence being accomplished. The program is moved from one sequence to the other by pressing ENTR. NOUN 03 flashing indicates that the IMU has been coarse aligned to 0^{o}.

The IMU 1X resolver sine in-phase and total nulls are checked first. The IMU 1X resolver sine and cosine outputs are checked at gimbal angles of 45^{o}. (NOUN 04 flashes when the gimbals are coarse aligned to 45^{o}.) The phase angle of each output with respect to the 800 cps reference and the phase difference between the sine and cosine outputs are determined. The CDU repeating accuracy at 45^{o} is checked by placing the system in the fine align mode, waiting 90 seconds, and then reading the CDU angles. The IMU zero mode is entered after which the IMU is returned to the fine align mode. The difference in the initial and present CDU angles is a measure of the CDU repeating accuracy. Entering VERB 33 now causes the IMU gimbals to be coarse aligned to 90^{o} in order to check the IMU gimbal 1X resolver cosine in-phase and total nulls.

The CDU command accuracy test at 135^{o} is now entered by pressing ENTR. The IMU gimbal angles are displayed on the DSKY, verifying that the CDU's can be commanded to 135^{o}. Pressing ENTR again causes the IMU gimbals to coarse align so that the outer and inner gimbals are at 135^{o} and the middle gimbal is at 45^{o}, in preparation for the CDU repeating accuracy test. Note that gimbal lock is avoided. Pressing ENTR again results in the same sequence as that given above for CDU repeating accuracy for 45^{o}. Entering VERB 33 at this point causes the middle gimbal to coarse align to 71^{o} to check gimbal lock limit. The CDU command accuracy at 225^{o} is checked by pressing ENTR. When the IMU gimbals are coarse aligned to 225^{o}, NOUN 13 flashes. The phase of the IMU 1X resolver outputs with respect to the 800 cps reference is determined. After pressing ENTR again, NOUN 14 flashes, indicating that the IMU gimbals are coarse aligned to 0^{o} in preparation for the CDU command rate test.

ENTR is pressed again to initiate the IMU CDU command rate test. The middle gimbal is commanded to coarse align at 170^{o} during which time the program determines the average command rate. This rate is determined by measuring the time lapse between the first CDU read counter pulse at 10^{o} and the last at 160^{o}. The CDU

command rate is then calculated by dividing the differences in CDU indications by the elapsed time between the two angles. The results are displayed and the test is repeated for the other two CDU's.

CDU command accuracy test at 315° is initiated by entering VERB 33. The IMU gimbals are coarse aligned to 315° and then NOUN 20 flashes. Pressing ENTR again results in the same sequence as that stated above for CDU repeating accuracy at 45°.

Entering VERB 33 causes the inner and outer gimbals to coarse align to 225° and the middle gimbal to coarse align to 289°. This sequence checks the gimbal lock limit. If the system under test uses Aurora 85, pressing ENTR results in a CDU repeating accuracy test at 225°. The sequence for this test is the same as that stated above for CDU repeating accuracy at 45°. If the system under test uses Aurora 88, an extra step has been included which first coarse aligns the middle gimbal to 0° while the inner and outer gimbals are coarse aligned at 225°. VERB 33 and NOUN 23 flash when the gimbals are coarse aligned with the outer and inner gimbals at 225° and the middle gimbal at 0°. Pressing ENTR then tests the CDU repeating accuracy at 225°. VERB 05 and NOUN 30 flash when the repeatability test is complete.

Entering VERB 33 causes the system to proceed to the IMU CDU fine fail test. In this test the IMU gimbal angles are coarse aligned to zero and the CDU's are zeroed. The operator then commands the IMU to fine align to 1°. The zero CDU discrete is set causing the CDU fine error fail gate to energize and set bit 12 of channel 30 (IMU CDU FAIL) to zero. Entering VERB 33 causes the system to proceed to the IMU CDU coarse fail test. When the program requests, the operator loads into the DSKY tbe gimbal angles to which the IMU is to be aligned (37.5°). The IMU is then fine aligned to this angle. The CDU under test is zeroed causing the CDU coarse error fail gate to energize and set bit 12 of channel 30 to zero.

Entering VERB 33 causes the system to proceed to the FDAI linearity test. In this test the IMU CDU's are moded to error counter enable so that the LGC can command the FDAI interface through the CDU DAC's. The first angle command (17°) is then issued to the CDU DAC's. The three IMU CDU DAC outputs are independently monitored on the PAVM for each of the angular commands (+17°, +6°, 0°, -6°, -16°, -17°) issued by the LGC. The angular commands are selected to demonstrate the saturation limits and linearity of the DAC's. The phase of the DAC output is determined with respect to the 800 cps reference at +6° in accordance with interface control documents.

The RR CDU command accuracy test is the next test. However, this test is not performed in the lab since the gimbal resolver circuit tester can only command either the shaft or trunnion, but not both; the program commands both. VERB 21, NOUN 01 and addresses 02550 and 00041 (00042 for Aurora 88) are entered, causing the LGC to skip the program controlled sequences for this test. A manual RR CDU command accuracy test is performed at the end of the programmed semiautomatic mode test.

Pressing ENTR initializes the RR velocity meter test. For this test, bit 6 of channel 30 (display inertial data discrete) must be set on the computer test set to switch the RR CDU dc outputs to the velocity meter interface. Each velocity command is initiated by pressing ENTR.

7-2.3.11 IMU Performance Test. This test determines three IRIG coefficients: bias drift (BD), drift due to acceleration along the input axis (ADIA), and drift due to acceleration along the spin reference axis (ADSRA). In addition, the PIPA scale factor (SF) and PIPA bias (A_B) are determined. The PIPA precision voltage reference (PVR) and PIPA torque current are measured. The test is computer controlled and requires six IMU positions to determine all parameters.

After a master initialization has been established per JDC 12613, with the rotary table tilt axis set to 90^o and the rotary axis set to 150^o (simulates spacecraft attitude), the PIPA PVR and the PIPA torque current are measured. VERB 57 (perform system test) and 00001 are entered into the DSKY; the computer is programmed to display on the DSKY an azimuth of 0 degree (row 1) and the latitude of the site where the test is being performed (row 2). VERB 33 (proceed without data) is entered into the DSKY, initializing the computer for test position 1. The DSKY indicates +00600 in row 1 (time of horizontal drift test), +00000 in row 2 (indicating the navigation base is in the spacecraft orientation), and +00001 in row 3 (test position 1). Again VERB 33 is entered into the DSKY, causing the computer to fine align the IMU to test position 1 orientation for the +NBDY test (IGA = 0^o, MGA = 0^o, and OGA = $+90^o$). After approximately 12 minutes, VERB 06 and NOUN 66 flash and the Y IRIG bias drift is displayed in row 2 of the DSKY in meru. VERB 33 is entered into the DSKY again, this time initializing the computer for the +X PIPA scale factor test. In approximately 300 seconds, VERB 06 and NOUN 66 flash, the +X PIPA output is measured, and the results are displayed on DSKY registers row 1 and row 2 in cm/sec^2. VERB 34 (terminate) is entered into the DSKY, causing the computer to terminate test position 1 and advance to test position 2. After VERB 06 and NOUN 66 flash, the DSKY indicates +00600 in row 1, +00000 in row 2, and +00002 in row 3. The program is advanced again by entering VERB 33, fine aligning the IMU to test position 2 orientation for the $+BD_Z$ test (IGA = $+180^o$, MGA = 0^o, and OGA = $+180^o$). After approximately 12 minutes, VERB 06 and NOUN 66 flash and the Z IRIG bias drift is displayed in row 2 of the DSKY. VERB 33 is entered into the DSKY, programming the computer for the -X PIPA scale factor test. In approximately 300 seconds VERB 06 and NOUN 66 flash, the -X PIPA output is measured, and the results are displayed in DSKY registers row 1 and row 2 in cm/sec^2. Again VERB 33 is entered into the DSKY, advancing the program for measurement of the vertical coefficient of the X IRIG ($-BD_X + ADIA_X$). Approximately 67 minutes later, VERB 06 and NOUN 66 flash and the X IRIG term is displayed on DSKY register row 2 in meru.

Test positions 3 and 4 are similar to test positions 1 and 2. In test position 3, the horizontal coefficient $-BD_X$ is calculated and the +Z PIPA scale factor is calculated. In position 4, the horizontal coefficient $+BD_Y + ADSRA_Y$ is calculated, the -Z PIPA scale factor is calculated, and the vertical coefficient of the Z IRIG ($+BD_Z + ADIA_Z$) is calculated. In position 3, the IMU is fine aligned to IGA = -90^o, MGA = 0^o, and OGA = $+180^o$. In position 4, the IMU is fine aligned to IGA = $+90^o$, MGA = 0^o, and OGA = $+90^o$.

Test positions 5 and 6 again are similar to test positions 1 and 2. However, for test positions 5 and 6, the rotary table tilt axis is set to 0 degree. In test position 5, the horizontal coefficient $+BD_Z - ADSRA_Z$ is calculated and the +Y PIPA scale factor is calculated. In position 6, the horizontal coefficient $+BD_X + ADSRA_X$ is calculated, the -Y PIPA scale factor is calculated, and the vertical coefficient $-BD_Y + ADIA_Y$ is calculated. In position 5, the IMU is fine aligned to IGA = -90^o, MGA = 0^o, and OGA = $+90^o$. In position 6, the IMU is fine aligned to IGA = $+180^o$, MGA = 0^o, and OGA = -90^o.

7-2.3.12 RR/CDU Moding Test. This test provides procedures that check RR/CDU zero accuracy, RR/CDU designate capability, RR/CDU tracking accuracy and ambiguity, RR/CDU resolver and coarse-fine error interface, and RR/CDU fail. The RR/CDU moding test is evaluated by interrogating LGC channels and by measuring ECDU outputs using the resolver circuit tester (RCT) to simulate RR inputs.

The RR designate capability test is initiated by setting the RCT resolver angle transmitter to simulate trunnion CDU angles of 45^o, 240^o, and 315^o. RR coarse align is commanded for each angle, and incrementing pulses equivalent to the respective angles are transmitted from the LGC to the CDU causing the CDU error counter to develop a D/A error output. The RCT resolver angle transmitter output is then applied to the CDU, and the read counter counts up or down to repeat the RCT resolver angle. As the read counter counts, feedback pulses are supplied to the CDU error counter causing it to count down and reduce the D/A error output. When the coarse align process is completed as indicated by the DSKY displaying VERB 33, the D/A error counter should have returned to its null value. The selector switch on the RCT is moved to simulate shaft angles of 45^o, 240^o, and 315^o and the above procedure is repeated.

The RR/CDU tracking accuracy and ambiguity is checked with the resolver angle transmitter set to simulate RR shaft and trunnion angles of 240^o. RR coarse align to 240^o is commanded and the RR/CDU shaft and trunnion channels must be capable of repeating the simulated 240^o angle within tolerances specified by the JDC. Also, the shaft and trunnion counters in the LGC must indicate the simulated 240^o angle to the tolerance specified by the JDC.

The RR/CDU resolver and coarse-fine error interface test is initiated with the RCT resolver angle transmitter set to simulate a shaft angle of 240^o. The RR shaft 1X sine and 1X cosine and the shaft coarse error signals are measured at TPA-2. The 1X sine and cosine signals must be -24.2 volts rms and -14.0 volts rms respectively. The shaft coarse error signal should be at null. The selector switch on the RCT is moved so that a trunnion angle of 240^o is simulated and the above measurements are repeated. The requirements are the same for both shaft and trunnion.

To initiate the shaft and trunnion 16X resolver interface test, the RCT resolver angle transmitter is set to simulate a shaft angle of 2.812^o. The RR shaft 16X sine and 16X cosine and the RR shaft fine error signals are measured at TPA-2. The 16X sine and cosine signals must be 3.535 volts rms with tolerances specified by the JDC. The shaft fine error signal should be at null. The selector switch on the RCT is

set so that a trunnion angle of 2.812° is simulated and the above measurements are repeated. The requirements are the same for both shaft and trunnion.

The RR/CDU fail test determines that CDU fail occurs with a difference of 1.0° (fine error) or 33.75° (coarse error) between the CDU read counter and the RR gimbal resolver. This test is accomplished by setting the RCT resolver angle transmitter to simulate CDU shaft and trunnion angles of 1.0°. RR coarse align to 1.0° is commanded. By performing DSKY operations indicated in the JDC and by rotating the resolver angle transmitter control to approximately +22.5°, bit 7 of channel 30 is at a "0" state and row 1 of DSKY indicates XX3XX. This indication verifies that the RR/CDU fail occurred within specifications.

7-2.3.13 IRIG Scale Factor Test. The IRIG scale factor test determines the accuracy of stable member response to torquing. IRIG scale factor is defined as the amount of stable member angular rotation about an IRIG input axis resulting from a known IRIG torque input from the LGC.

During this test the effect of earth rate on an IRIG is minimized by aligning the IRIG input axis to be tested along an east or west direction. The test is run three times, and the average plus and minus scale factor error is calculated for each gyro.

The test is initiated by entering VERB 57 (perform system test) and 00005 (IRIG scale factor test) into the DSKY. The selected program displays the following on the DSKY: VERB 6 (decimal display), NOUN 61 (target azimuth and elevation), navigation base azimuth in row 1, and the site latitude in row 2. If the navigation base azimuth and site latitude are correctly displayed, VERB 33 (proceed without data) is entered into the DSKY. If the information is incorrect, it is updated before entering VERB 33.

After an IRIG test position is entered into the DSKY, the gyro drift enable discrete (bit 6 of channel 14) is set to turn on the gyro power supply and allow computer pulsing of the gyros. The system is automatically sequenced through CDU zero, coarse align, and fine align ending with the selected IRIG aligned east or west, another IRIG aligned north or south, and the remaining IRIG in a vertical alignment.

The computer loads the gyro counter with 16,383 pulses (equivalent to 2.8125 degrees of stable member rotation). Each gyro torquing pulse issued decrements the gyro counter by one.

At the first loading of the gyro counter, the computer allows the IRIG to be pulsed for two periods of 320 milliseconds each and reloads the gyro counter with the first set of pulses between the two loading periods. This operation allows a total of 2048 pulses or 0.3515 degree of gimbal rotation and insures that the CDU is on the linear portion of the CDU error curve when the test starts.

The computer CDU counter is zeroed and the CDU is monitored for the first pulse resulting from the above torquing. When the first CDU pulse is detected, the contents of the gyro counter are stored and 2048 CDU counts (with a polarity opposite that of the

first pulse) are placed in the CDU counter. Note: Aurora 85 stores 2047 CDU counts. Thus, as the IRIG is pulsed by the gyro counter causing a change in stable member orientation and CDU angle, the CDU counter approaches zero. 2048 CDU pulses correspond to 22.5 degrees of gimbal movement.

Tbe IRIG that is aligned north or south and the IRIG that is aligned vertically sense calculable portions of earth rate and the loop response forces the stable member to move, thus causing the IRIG under test to be moved from its east or west alignment. This results in the IRIG under test sensing a portion of earth rate and introduces an error into scale factor measurements. Therefore, after the first gyro counter decrementing and every other time thereafter, the computer returns the north or south IRIG and the vertical IRIG to their original positions.

During the entire test, the gyro counter is reloaded with I6,383 pulses for eight or nine times after it decrements to zero. By the end of this time, the gimbal should have moved 22.5 degrees and the CDU counter should have decremented to zero. If the CDU counter does not go to zero after the gyro counter is reduced the ninth time, alarm number 1411 is displayed to indicate that the scale factor error is too large or the CDU does not function.

If the CDU counter goes to zero on the eighth or ninth time, the gyro counter content is saved. With a perfect IRIG scale factor, the final content of the gyro counter equals the initial content and the scale factor error is zero. The difference between the initial and final gyro counter content is obtained and the scale factor error is calculated as follows:

The +scale factor error is equal to initial gyro counter error minus final gyro counter content times 1/7.6.

The -scale factor error is equal to 37777 minus difference between the initial and final gyro counter content times 1/7.6.

where I/7.6 is the scale factor constant that converts the difference in initial and final gyro counter readings to parts per million error.

The DSKY displays VERB 06 and NOUN 66 with the ± scale factor (in parts per million) displayed in row 1.

The three tests are averaged; for Aurora 85 they are also corrected by subtracting a constant of 556 from the average.

7-3 INERTIAL SUBSYSTEM

7-3.1 PREPARATION. Table 7-III lists the cables and interconnections required of the ISS. Refer to Table 7-I for a listing of PGNCS components and GSE necessary to perform an ISS test.

7-3.2 CHECKOUT. The ISS master flowgram (figure 7-4) specifies the conditions leading to an ISS checkout. Detailed flowgrams (figures 7-5 and 7-6) give sequential listings of JDC's to be performed. Refer to table 6-III for JDC's to be used if operating procedures for GSE test equipment are required during performance of lSS checkout JDC's.

7-4 COMPUTER SUBSYSTEM

7-4.1 PREPARATION. Refer to table 7-I for a listing of PGNCS components and GSE required to perform a CSS checkout. Table 7-IV lists the cables and interconnections used to connect the CSS and GSE during CSS checkout.

7-4.2 CHECKOUT. The CSS master flowgram (figure 7-7) specifies the conditions leading to a CSS checkout. Detailed flowgrams give sequential listings of JDC's to be performed.

7-5 ALIGNMENT OPTICAL TELESCOPE

7-5.1 PREPARATION. Refer to table 7-I for equipment required to perform an AOT checkout.

7-5.2 CHECKOUT. The AOT master flowgram (figure 7-10) specifies the conditions leading to an AOT checkout. Detailed flowgrams (figures 7-11 and 7-12) give sequential listings of JDC's to be performed.

7-6 SIGNAL CONDITIONER ASSEMBLY

7-6.1 PREPARATION. Refer to table 7-I for equipment required to perform an SCA checkout.

7-6.2 CHECKOUT. The SCA master flowgram (figure 7-13) specifies the conditions leading to an SCA checkout and gives sequential listings of JDC's to be performed. Upon completion of checkout, prepare the SCA for storage or PGNCS checkout in accordance with figure 7-13.

7-7 PRE-INSTALLATION ACCEPTANCE

PIA tests are performed on all spare components prior to installing the spare in the spacecraft. PIA tests are not required for spare components to be installed in a PGNCS in the laboratory. PIA tests and procedural requirements are listed in table 7-V. Perform the procedures in the sequence given for the applicable component. Auxiliary airborne equipment can be used to complete a test setup. (See paragraph 8-11.)

Table 7-I. Equipment Required for Checkout

Equipment	Used in				
	PGNCS	ISS	CSS	AOT	SCA
PGNCS COMPONENTS					
AOT				X	
CDU	X	X			
CCRD	X				
PGNCS interconnect harness group (LEM)	X				
IMU and PTA	X	X			
LGC	X		X		

(Sheet 1 of 3)

Table 7-I. Equipment Required for Checkout

Equipment	Used in				
	PGNCS	ISS	CSS	AOT	SCA
DSKY	X		X		
PSA	X	X			
SCA	X				X
GSE					
AGC/GSE interconnect cables, PGNCS	X				
AGC/GSE interconnect cables, CSS			X		
AGC handling fixture	X		X		
AGC/OC			X		
AOT certification kit				X	
AOTT				X	
AOT lens covers				X	
AOT transparent dome protector				X	
Auxiliary calibration system			X		
Calibration system			X		
Component mounting plate	X	X			
Computer simulator		X			
Coolant and power console	X	X			
Connector cover set	X	X			
Connector covers				X	
CTS	X		X		
Degausser	X	X			
DSKY handling fixture	X		X		
DSKY pedestal mount	X				
G and N transport cart	X	X			
GSE coolant hoses	X	X			
GSE distribution box	X	X			
IMU lifting and handling fixture	X	X			
Lifting temperature controller	X	X			
IMU mounting fixture	X	X			
IMU pressure seal tester	X				

(Sheet 2 of 3)

Table 7-I. Equipment Required for Checkout

Equipment	Used in				
	PGNCS	ISS	CSS	AOT	SCA
IMU snap-on bellows	X	X			
Interconnect cables	X	X			
Interconnect cables special (LEM)	X	X			
OIA	X	X			
Oscillograph	X	X			
P and M interconnect set	X		X		
PSA test point adapter	X	X			
PTA/PEA mounting fixture	X	X			
PTA/PEA test point adapter	X	X			
Purging and filling fixture	X	X			
Resolver circuit tester	X	X			
Rotary table	X	X		X	
Rotary table calibration set	X	X			
SPCU	X				X
Subsystem mounting fixture	X	X			
Theodolite	X			X	

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Table 7-IA. PGNCS Interconnect Harness Group Connections
(PGNCS Checkout)

From		To	
Harness	Connector	Connector	Equipment
PGNCS interconnect harness A	56P1	J1	SCA breakout
	56P2	45J19	PSA
	56P3	40J53	CDU
	56P4	05A1J1*	LGC
	56P5 (J221)	P3	Cable W143

(Sheet 1 of 2)

Table 7-IA. PGNCS Interconnect Harness Group Connections
(PGNCS Checkout)

From		To	
Harness	Connector	Connector	Equipment
PGNCS interconnect harness B	56P6 (J220)	P5	Cable W131
	56P7 (J219)	P6	Cable W131
	56P8 (J222)	J1	Cable W137
	56P9 (J218)	P2	Cable W131
	56P10 (J217)	P4	Cable W131
	56P11 (J223)	P8	Cable W132
	56P12 (J224)	P3	Cable W131
	56P13 (J215)	P2	Cable W134
	56P14 (J216)	P7	Cable W132
	56P15 (J226)	P4	Cable W132
	56P16	P2	Cable W132
	56P17	P3	Cable W132
	56P18	P1	Cable W134
	56P19	35A2J19	PTA
	56P20	35A1J2	IMU
	56P21	35A1J1	IMU
	56J1	P2**	Cable W120

* May be designated as A51
** This connection shall only be made as specified in the applicable JDC.

(Sheet 2 of 2)

Table 7-II. GSE Interconnect Cable Connections (PGNCS Checkout)

From			To	
Cable Designation	Part Number	Plug	Jack	Equipment
W1	1900886	P1 P2	J1 J1	OIA Oscillograph
W2	1900669	P1 P2	J2 J2	OIA Oscillograph
W3	1900670	P1 P2	J3 J3	OIA Oscillograph
W4	1900671	P1 P2	J4 J4	OIA Oscillograph
W19	1900873	P1 P2	J20 J3	OIA Coolant and power console
W22	1902610	P1 P2	J23 J6	OIA CTS (Diagnostic tests only)
W26	1900921	P1 P2	A30J1 facility	OIA (ac power protection panel) Wall power
W27	1900871	P1 P2	A30J2 J1	OIA (ac power protection panel) Coolant and power console
W28	1900872	P1 P2	J2 facility	Coolant and power console Wall power
W33	1901404	P1 P2	E1 E4	OIA Oscillograph
W37	1901662	Connected between E300 on rotary table and facility ground.		
W64	1901676	P1 P2	E1 E300	G and N mounting fixture base Rotary table
W65	1900739	P1 P2	J4 J15	Current source monitor PTA test point adapter
W66	1901677	Connected between E2 on G and N mounting fixture cradle and E1 on G and N mounting fixture base.		
W68	1902284	Connected between E1 on PTA/PEA coldplate and E300 on rotary table.		

(Sheet 1 of 6)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W4	1900671	P1/J4 P2/J4	OIA Oscillograph
W19	1900873	P1/J20 P2/J3	OIA Coolant and power console
W22	1900959	P1/J23 P2/J5	OIA CTS

(Sheet 1A of 6)

Table 7-II. GSE Interconnect Cable Connections (PGNCS Checkout)

From			To	
Cable Designation	Part Number	Plug	Jack	Equipment
W85	1901960	P1	A30J5	OIA (ac power protection panel)
		P2	facility	Emergency wall power
W120	2900456	P1	J19	OIA
		P2	56J1	PGNCS interconnect harness B
W121	2900257	P1	J8	OIA
		P2	J9	OIA
		P3	J13	OIA
		P4	J14	OIA
		P5	J15	OIA
		P6	J57	GSE distribution box
W122	2900378	P1	J18	OIA
		P2	J17	OIA
		P3	J16	OIA
		P4	J22	OIA
		P5	J55	GSE distribution box
		P6	J59	GSE distribution box
		P7	J62	GSE distribution box
		P8	J58	GSE distribution box
W123	2900379	P1	J21	OIA
		P2	J24	OIA
		P3	J25	OIA
		P4	J26	OIA
		P5	J60	GSE distribution box
		P6	J63	GSE distribution box
		P7	J66	GSE distribution box
		P8	J67	GSE distribution box
W124	2900380	P1	J5	OIA
		P2	J6	OIA
		P3	J7	OIA
		P4	J64	GSE distribution box
		P5	J61	GSE distribution box
		P6	J65	GSE distribution box

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Table 7-II. GSE Interconnect Cable Connections (PGNCS Checkout)

From			To	
Cable Designation	Part Number	Plug	Jack	Equipment
W125	2901389	P1	J28	OIA
		P2	J29	OIA
		P3	J30	OIA
		P4	J50	GSE distribution box
		P5	J51	GSE distribution box
		P6	J54	GSE distribution box
W126	2900381	P1	J10	OIA
		P2	J11	OIA
		P3	J12	OIA
		P4	J52	GSE distribution box
		P5	J53	GSE distribution box
		P6	J56	GSE distribution box
W127 (2 required)	2900327	First cable connected between E1 on OIA and E300 on rotary table. Second cable connected between E80 on OIA and E1 on GSE distribution box.		
W128 (2 required)	2900458	First cable connected between E2 on GSE distribution box and E300 on rotary table. Second cable connected between E1 on subsystem mounting fixture and E300 on rotary table.		
W129 (2 required)	2900459	First cable connected between E1 on subsystem mounting fixture and E3 on GSE distribution box. Second cable connected between E1 on subsystem mounting fixture and E2 on component mounting plate.		
W130	2900460	Connected between E1 on coolant and power console and E300 on rotary table.		

(Sheet 3 of 6)

Table 7-II. GSE Interconnect Cable Connections (PGNCS Checkout)

From			To	
Cable Designation	Part Number	Plug	Jack	Equipment
W131	6900144	P1	J13	GSE distribution box
		P2	J16	GSE distribution box
		P3	J224 (56P12)	SMF
		P4	J217 (56P10)	SMF
		P5	J220 (56P6)	SMF
		P6	J219 (56P7)	SMF
		P7	J2	CTS
		P8	J3	CTS
		P9	J218	SMF
		P10	J15	GSE distribution box
W132	2901238	P1		Not used
		P2	56P16	PGNCS interconnect harness B
		P3	56P17	PGNCS interconnect harness B
		P4	56P15 (J226)	PGNCS interconnect harness B
		P5	J2	PTA test point adapter
		P6		Not used
		P7	56P14 (J216)	PGNCS interconnect harness B
		P8	56P11 (J223)	PGNCS interconnect harness B
		P9	J14	GSE distribution box
		P10	J18	GSE distribution box
W134	2901237	P1	56P18	PGNCS interconnect harness B
		P2	56P13 (J215)	PGNCS interconnect harness A
W135	6900024	P1	J27	GSE distribution box
		P2	P1	CCRD
		P3	J1	CCRD
W136	2900461	P1	J24	GSE distribution box
		P2	J28	GSE distribution box
		P3	J3	PSA test point adapter
		P4	J4	PSA test point adapter
W137	6900099	P1	J33	GSE distribution box
		J1	56P8 (J222)	PGNCS interconnect harness A
W138	6900134	P1	J26	GSE distribution box
		P2	A	Sig cond module brk-out box

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Table 7-II. GSE Interconnect Cable Connections (PGNCS Checkout)

From			To	
Cable Designation	Part Number	Plug	Jack	Equipment
W139	6900004	P1	J15	GSE distribution box
		P2	56P9	PGNCS interconnect harness A
W140	2900457	P1	J4	Coolant and power console
		P2	J34	GSE distribution box
W142	6900137	P1	J4 or	Sig cond module brk-out box
		P1	P2	or W157
		P2	J1	PSA test point adapter
		P3	J2	PSA test point adapter
W143	6900025	P1	J9	DSKY
		P2	J29	GDB
		P3	56P5 (J221)	PGNCS interconnect harness A
W144	6900006	P1	J1	PTA test point adapter
		P2	35A2J18	PTA
W157	6900153	P1	30J1	Signal conditioner module
		P2	P1	W142
W226	2014137-021	P1	Test Conn (A52)	LGC
		P2	J4	Buffer circuit assembly
		P3	J5	Buffer circuit assembly
		P4	J6	Buffer circuit assembly
W232	2014483-011	P1	P7	W131
		P2	J2	CTS
		P3	J7	CTS
W233	2014484-011	P1	P8	W131
		P2	J16	CTS
		P3	J10	CTS
		P4	J4	CTS
W236	2014463-011	P1	J1	Buffer circuit assembly
		P2	J5	CTS

Table 7-II. GSE Interconnect Cable Connections (PGNCS Checkout)

From			To	
Cable Designation	Part Number	Plug	Jack	Equipment
W237	2014462-011	P1	J2	Buffer circuit assembly
		P2	J11	CTS
W238	2014462-021	P1	J3	Buffer circuit assembly
		P2	J17	CTS
W239	2014462-031	P1	J9	Buffer circuit assembly
		P2	J18	CTS
W259	2014470-011	P1	CP1	Calibration system
		P2	(hi)	Digital ohmmeter
		P3	(lo)	Digital ohmmeter
		P4	J7	LGC buffer assembly
		P5	J8	LGC buffer assembly
		P6	J4	W232
		P7	(hi)	Digital ohmmeter
		P8	(lo)	Digital ohmmeter

(Sheet 6 of 6)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W1	1900886	P1/J1	OIA
		P2/J1	Oscillograph
W2	1900669	P1/J2	OIA
		P2/J2	Oscillograph

(Sheet 1 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W3	1900670	P1/J3	OIA
		P2/J3	Oscillograph
W4	1900671	P1/J4	OIA
		P2/J4	Oscillograph
W19	1900873	P1/J20	OIA
		P2/J3	Coolant and power console
W26	1900921	P1/A30J1	OIA (ac power protection panel, FTR)
		P2/facility	Wall power
W27	1900871	P1/A30J2	OIA (ac power protection panel, FTR)
		P2/J1	Coolant and power console
W28	1900872	P1/J2	Coolant and power console
		P2/facility	Wall power
W33	1901404	P1/E1	OIA
		P2/E4	Oscillograph
W37	1901662	P1/facility	Facility ground
		P2/E300	Rotary table
W64*	1901676	P1/E1	G and N mounting fixture
		P2/E300	Rotary table
W65	1900739	P1/J4	Current source monitor
		P2/J15	PTA test point adapter
W85	1901960	P1/A30J5	OIA (ac power protection panel, FTR)
		P2/facility	Emergency wall power
W120	2900456	P1/J19	OIA
		P2/J1	W146
W121	2900257	P1/J8	OIA
		P2/J9	OIA
		P3/J13	OIA
		P4/J14	OIA
		P5/J15	OIA
		P6/J57	GSE distribution box

* Not used at GAEC

(Sheet 2 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W122	2900378	P1/J18	OIA
		P2/J17	OIA
		P3/J16	OIA
		P4/J22	OIA
		P5/J55	GSE distribution box
		P6/J59	GSE distribution box
		P7/J62	GSE distribution box
		P8/J58	GSE distribution box
W123	2900379	P1/J21	OIA
		P2/J24	OIA
		P3/J25	OIA
		P4/J26	OIA
		P5/J60	GSE distribution box
		P6/J63	GSE distribution box
		P7/J66	GSE distribution box
		P8/J67	GSE distribution box
W124	2900380	P1/J5	OIA
		P2/J6	OIA
		P3/J7	OIA
		P4/J64	GSE distribution box
		P5/J61	GSE distribution box
		P6/J65	GSE distribution box
W125	2901389	P1/J28	OIA
		P2/J29	OIA
		P3/J30	OIA
		P4/J50	GSE distribution box
		P5/J51	GSE distribution box
		P6/J54	GSE distribution box
W126	2900381	P1/J10	OIA
		P2/J11	OIA
		P3/J12	OIA
		P4/J52	GSE distribution box
		P5/J53	GSE distribution box
		P6/J56	GSE distribution box

(Sheet 3 of 5)

Tabls 7-III. Insrtial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W127 (2 required)	2900327	First cable connected between E1 on OIA and E300 on rotary tabls.	
		Second cable connected between E80 on OIA and E1 on GSE distribution box.	
W128 (2 required)	2900458	First cable connected between E2 on GSE distribution box and E300 on rotary table.	
		Second cable connected between E1 on subsystem mounting fixture and E300 on rotary tabls.	
W129 (2 required)	2900459	First cable connected between E1 on subsystem mounting fixture and E3 on GSE distribution box.	
		Second cabls connected between E1 on subsystem mounting fixture and E2 on subsystem mounting fixturs.	
W130	2900460	P1/E1	Coolant and powsr console
		P2/E300	Rotary tabls
W132	2901238	P1	Not used
		P2/P16	W146
		P3/P17	W146
		P4/P15	W146
		P5/J2	PTA test point adapter
		P6	Not used
		P7/J10	GSE distribution box
		P8/J17	GSE distribution box
		P9/J14	GSE distribution box
		P10/J18	GSE distribution box
W133	6900161	P1/J11	GSE distribution box
		P2/J19	PSA
		P3/J53	CDU
		P4/J12	GSE distribution box
		P5/J16	GSE distribution box
		P6/J15	GSE distribution box
		P7/J23	GSE distribution box
		P8/J19	GSE distribution box

(Sheet 4 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W133 (cont)		P9/J20	GSE distribution box
		P10/J33	GSE distribution box
		P11/J26	GSE distribution box
		P12/J1	PSA test point adapter
		P13/J215	Subsystem mounting fixture
		P14/J2	PSA test point adapter
W134	2901237	P1/P18	W146
		P2/J215	Subsystem mounting fixture
W136	2900461 or 2907032	P1/J24	GSE distribution box
		P2/J28	GSE distribution box
		P3/J3	PSA test point adapter
		P4/J4	PSA test point adapter
W140	2900457	P1/J4	Coolant and power console
		P2/J34	GSE distribution box
W141	2901153	P1/A1J3	GSE distribution box
		P2/	IMU
		P3/J2	PTA coldplate
		P4/J1	Not used
		P5/J1	CDU coldplate
		P6/J1	PSA coldplate
W144	6900006	P1/J1	PTA test point adapter
		P2/35A2J18	PTA
W146	2900351	P15/P4	W132
		P16/P2	W132
		P17/P3	W132
		P18/P1	W134
		P19/35A2J19	PTA
		P20/J2	IMU
		P21/J1	IMU
		J1/P2	W120

(Sheet 5 of 5)

Table 7-IV. Computer Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W212	1006482-001	P1/J7 P2/J1	AGC/OC CTS
W213	1006482-002	P1/J8 P2/J7	AGC/OC CTS
W214	1006482-003	P1/J9 P2/J13	AGC/OC CTS
W215	1006482-004	P1/J4 P2/J2	AGC/OC CTS
W216	1006482-005	P1/J5 P2/J8	AGC/OC CTS
W217	1006482-006	P1/J6 P2/J14	AGC/OC CTS
W218	1006482-007	P1/J11 P2/J3	AGC/OC CTS
W219	1006482-008	P1/J12 P2/J9	AGC/OC CTS
W220	1006482-009	P1/J10 P2/J15	AGC/OC CTS
W221	1006482-010	P1/J1 P2/J10	AGC/OC CTS
W222	1006482-011	P1/J2 P2/J16	AGC/OC CTS
W223	1006482-012	P1/J3 P2/J4	AGC/OC CTS
*W226	2014137-021	P1/Test Conn. P2/J4 P3/J5 P4/J6	LGC Buffer circuit assembly Buffer circuit assembly Buffer circuit assembly

*This cable part of G and N Test Interconnection Set (2014255-051)

(Sheet 1 of 2)

Table 7-IV. Computer Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W227	2014199-021	P1/S/C Conn.	LGC
		P2/J2	AGC/OC junction panel assembly
		P3/J3	AGC/OC junction panel assembly
		P4/J4	AGC/OC junction panel assembly
		P5/J5	AGC/OC junction panel assembly
		P6/J1	AGC/OC junction panel assembly
*W236	2014463-011	P1/J1	Buffer circuit assembly
		P2/J5	CTS
*W237	2014462-011	P1/J2	Buffer circuit assembly
		P2/J11	CTS
*W238	2014462-021	P1/J3	Buffer circuit assembly
		P2/J17	CTS
*W239	2014462-031	P1/J9	Buffer circuit assembly
		P2/J18	CTS
*W259	2014470-011	P1/CP1	Calibration system
		P2/HI	Digital ohmmeter
		P3/LO	Digital ohmmeter
		P4/J7	Buffer circuit assembly
		P5/J8	Buffer circuit assembly
		P6/J6	AGC/OC junction panel assembly
		P7/HI	Digital ohmmeter
		P8/LO	Digital ohmmeter
W268	2014486-021	P1/J9	DSKY
		P2/J1	AGC/OC

*These cables part of G and N Test Interconnection Set (2014255-051)

(Sheet 2 of 2)

Table 7-V. PIA Requirements

Component	Procedures for Subsystem Configuration	Procedures for System Configuration
AOT	Prerequisite: AOT checkout preparation, figure 7-11. PIA test: figure 7-12.	None
CCRD	Perform JDC 18830.	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12689.
CDU	Prerequisite: ISS test preparation, figure 7-5. PIA test: figure 7-14.	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12685.
IMU and PTA	Prerequisite: ISS test preparation, figure 7-5. PIA test: figure 7-15.	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12688.
LGC and/or DSKY	Prerequisite: CSS test preparation, figure 7-8. PIA test: figure 7-9.	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12686 for LGC and/or JDC 12687 for DSKY.
PGNCS interconnect harness "A"	None	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12692.
PGNCS interconnect harness "B"	None	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12693.

(Sheet 1 of 2)

Table 7-V. PIA Requirements

Component	Procedures for Subsystem Configuration	Procedures for System Configuration
PSA	Perform the following steps: 1. Perform 28 VDC Filter Test, JDC-18831. 2. Prerequisite: ISS test preparation, figure 7-5. 3. PIA test: figure 7-16.	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12691.
SCA	Perform SCA checkout in accordance with figure 7-13.	Prerequisite: PGNCS checkout preparation, figure 7-2. PIA test: Perform JDC 12620.

(Sheet 2 of 2)

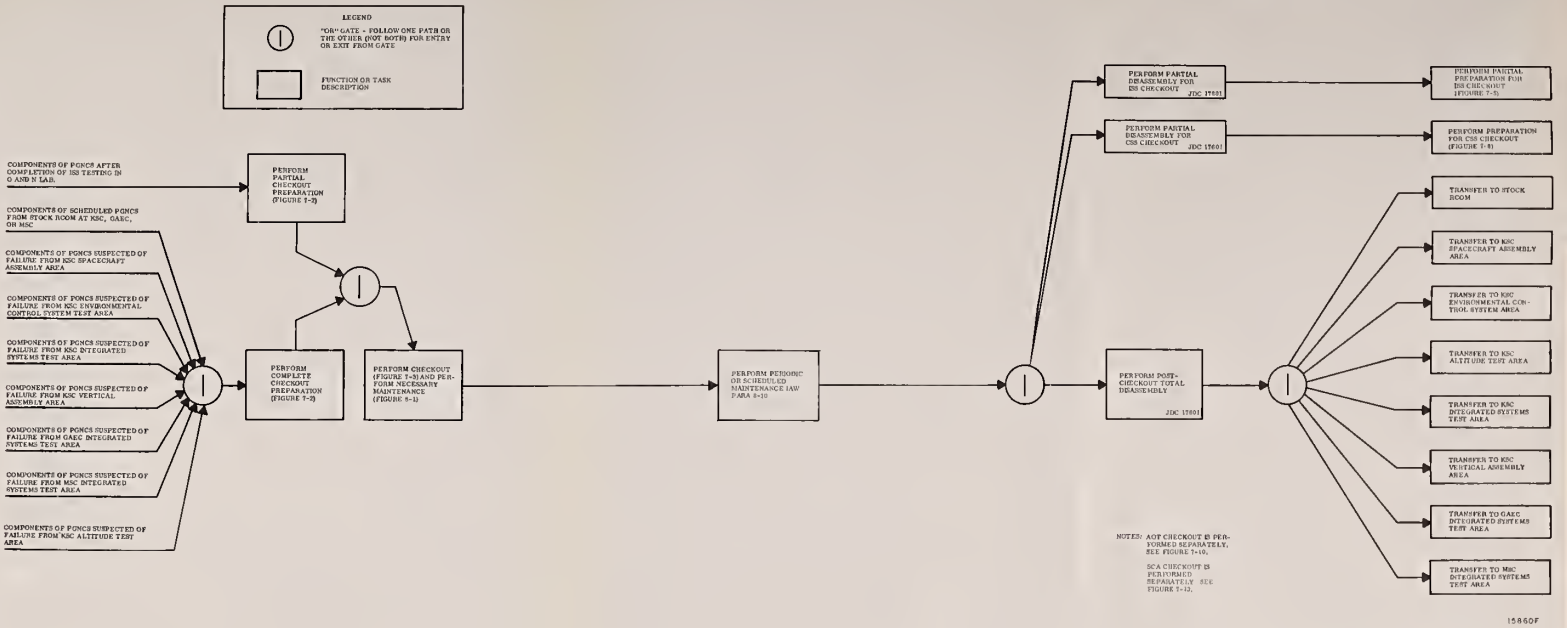

Figure 7-1. Primary Guidance, Navigation, and Control System Master Checkout Flowgram

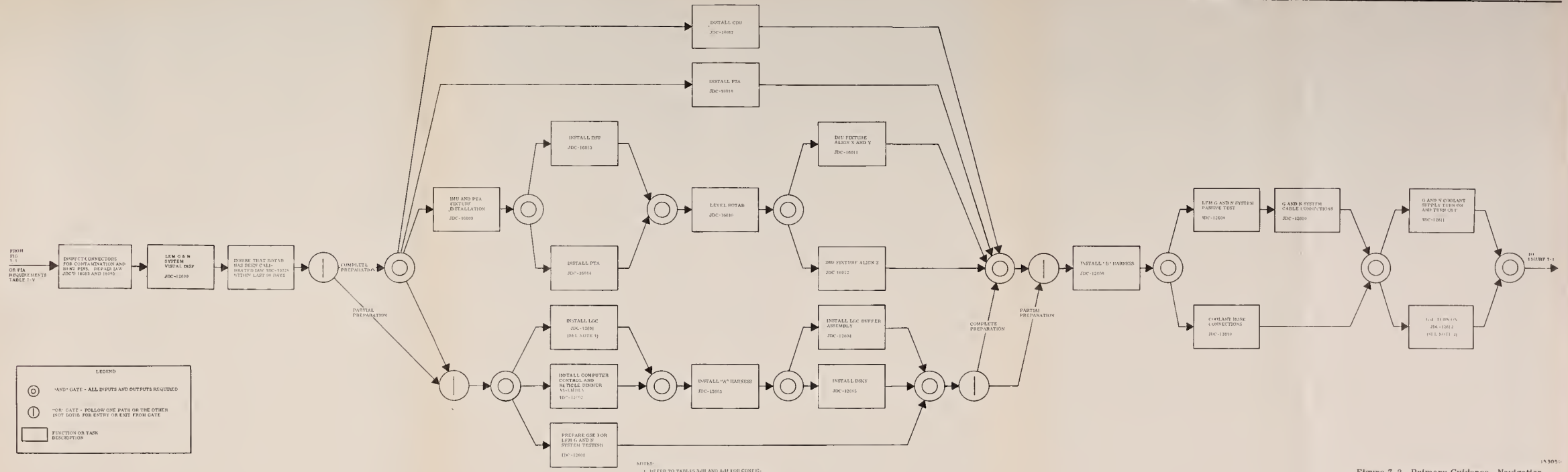

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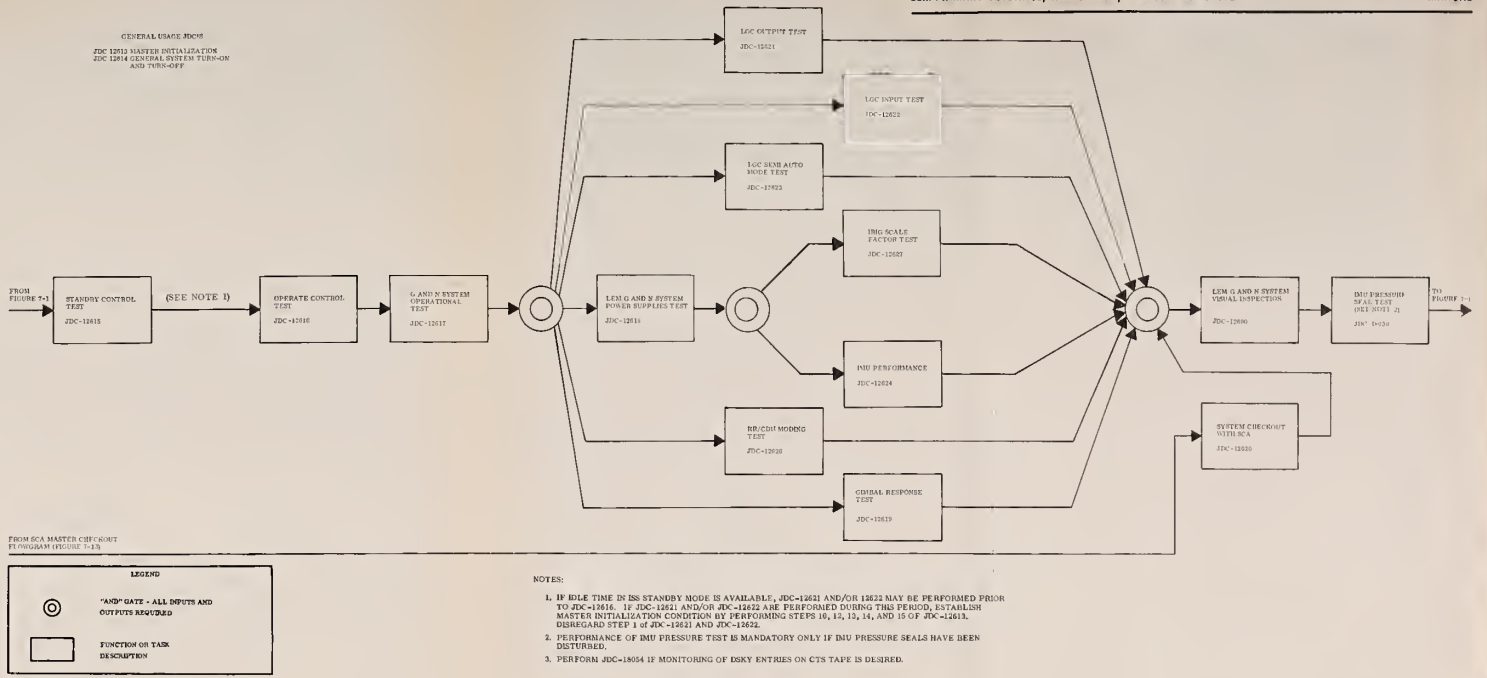
Figure 7-2. Primary Guidance, Navigation, and Control System Checkout Preparation Flowgram

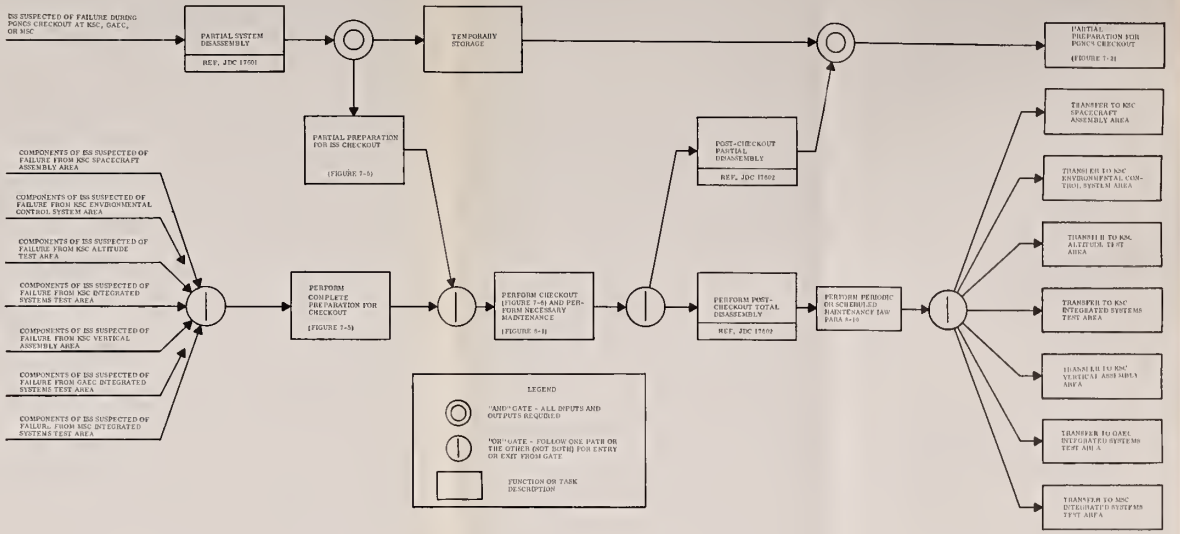


NOTES:

1. IF IDLE TIME IN ISS STANDBY MODE IS AVAILABLE, JDC-12621 AND/OR 12622 MAY BE PERFORMED PRIOR TO JDC-12616. IF JDC-12621 AND/OR JDC-12622 ARE PERFORMED DURING THIS PERIOD, ESTABLISH MASTER INITIALIZATION CONDITION BY PERFORMING STEPS 10, 12, 13, 14, AND 15 OF JDC-12613, DISREGARD STEP 1 of JDC-12621 AND JDC-12622.
2. PERFORMANCE OF IMU PRESSURE TEST IS MANDATORY ONLY IF IMU PRESSURE SEALS HAVE BEEN DISTURBED.
3. PERFORM JDC-18054 IF MONITORING OF DSKY ENTRIES ON CTS TAPE IS DESIRED.

15107C

Figure 7-3. Primary Guidance, Navigation, and Control System Checkout Flowgram



156610

Figure 7-4. Inertial Subsystem Master Checkout Flowgram

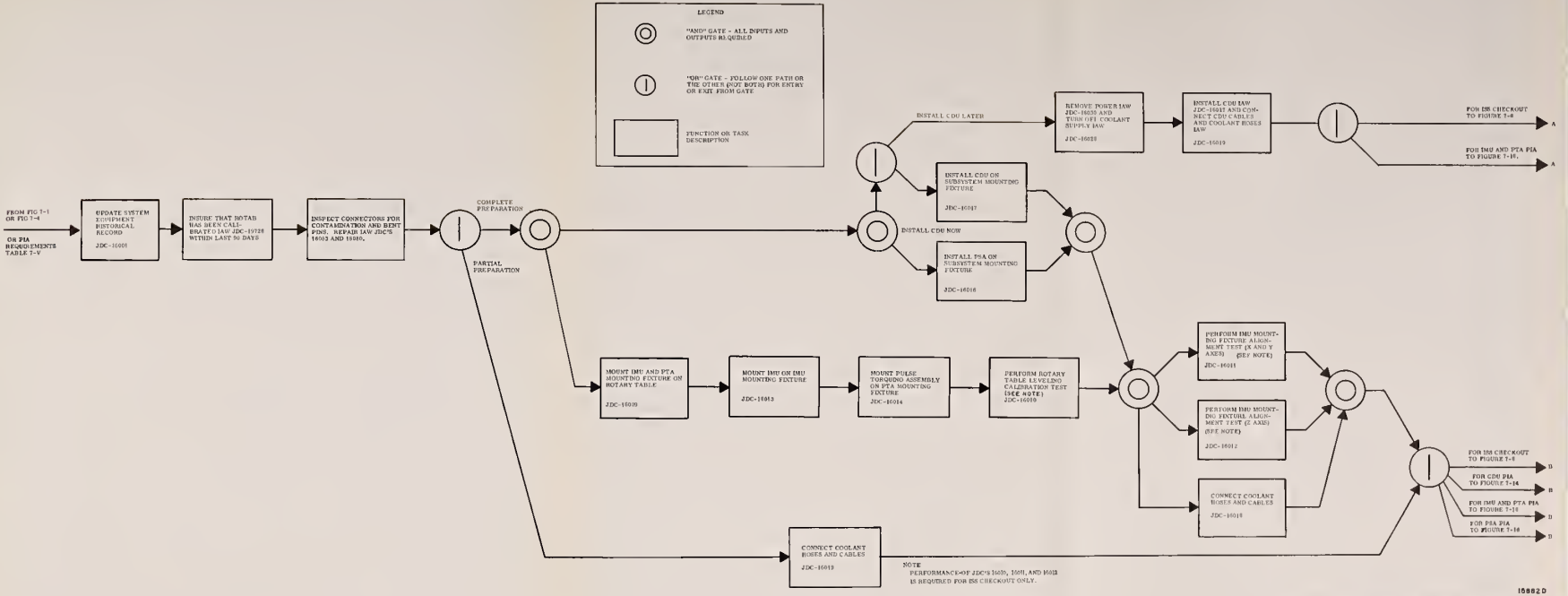


Figure 7-5. Inertial Subsystem Checkout Preparation Flowgram

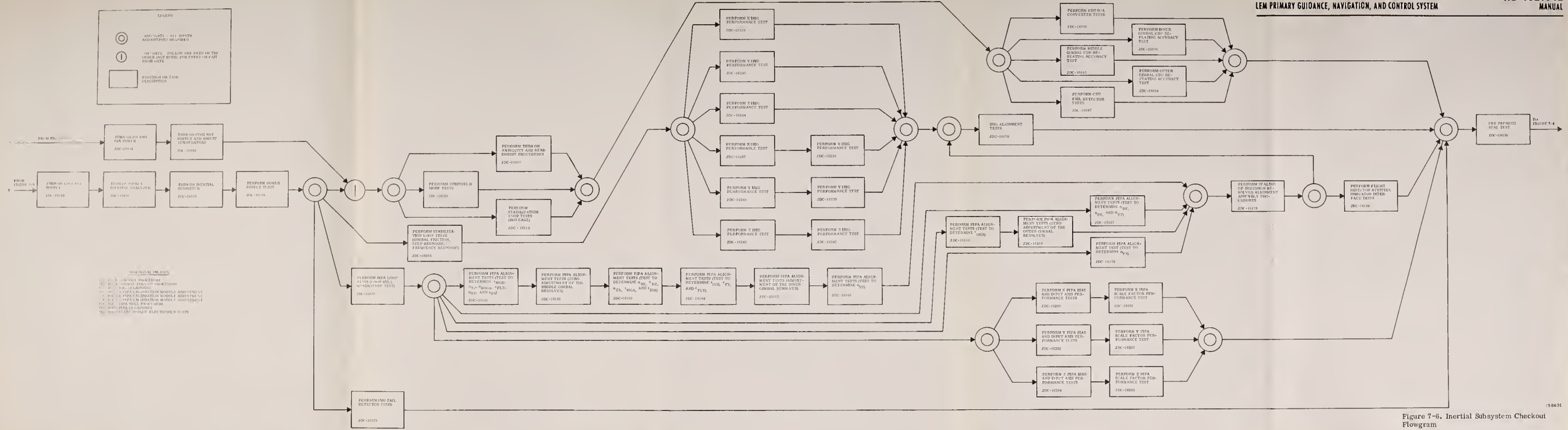


Figure 7-6. Inertial Subsystem Checkout Flowgram

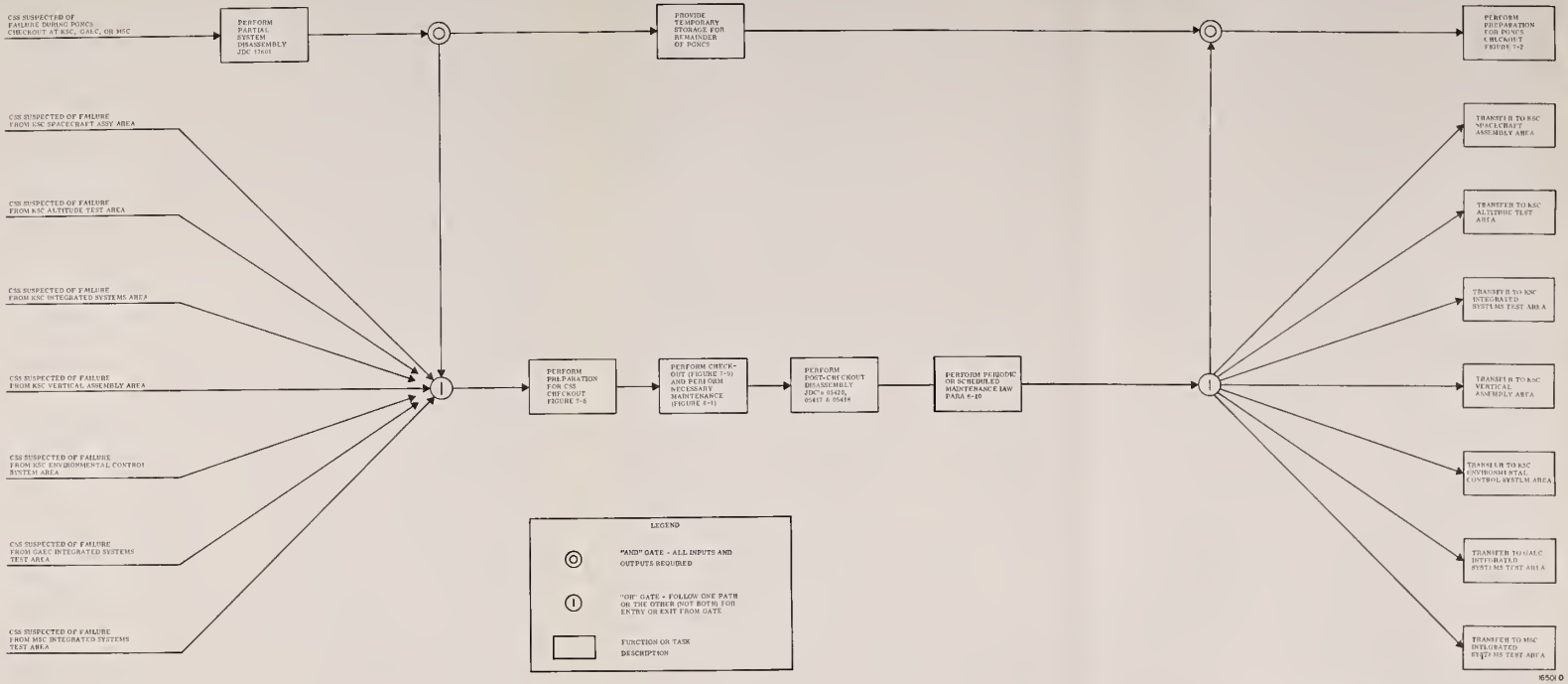


Figure 7-7. Computer Subsystem Master Checkout Flowgram

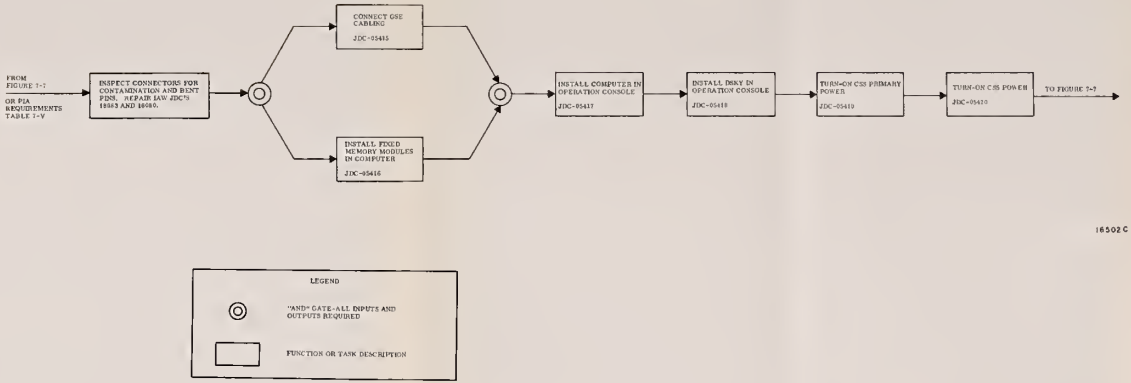


Figure 7-8. Computer Subsystem Checkout Preparation Flowgram

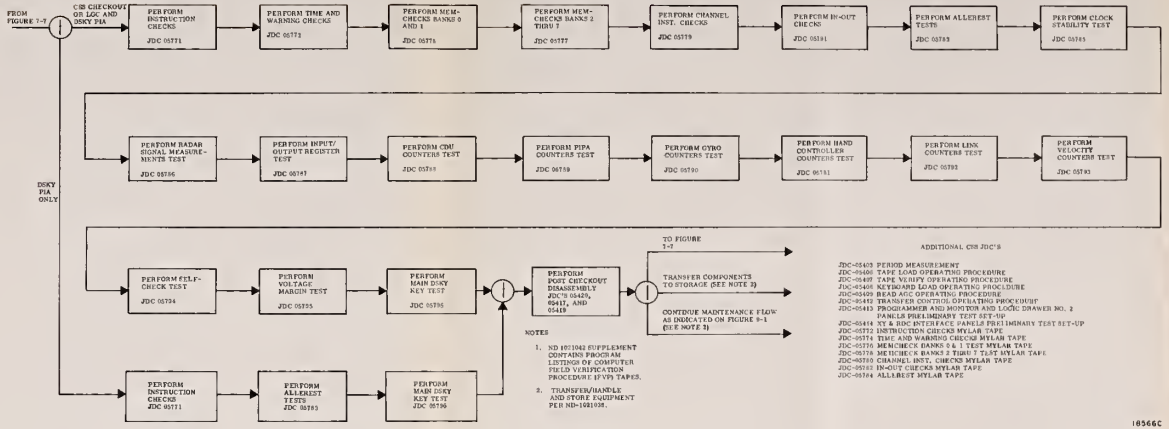


Figure 7-9. Computer Subsystem Checkout Flowgram

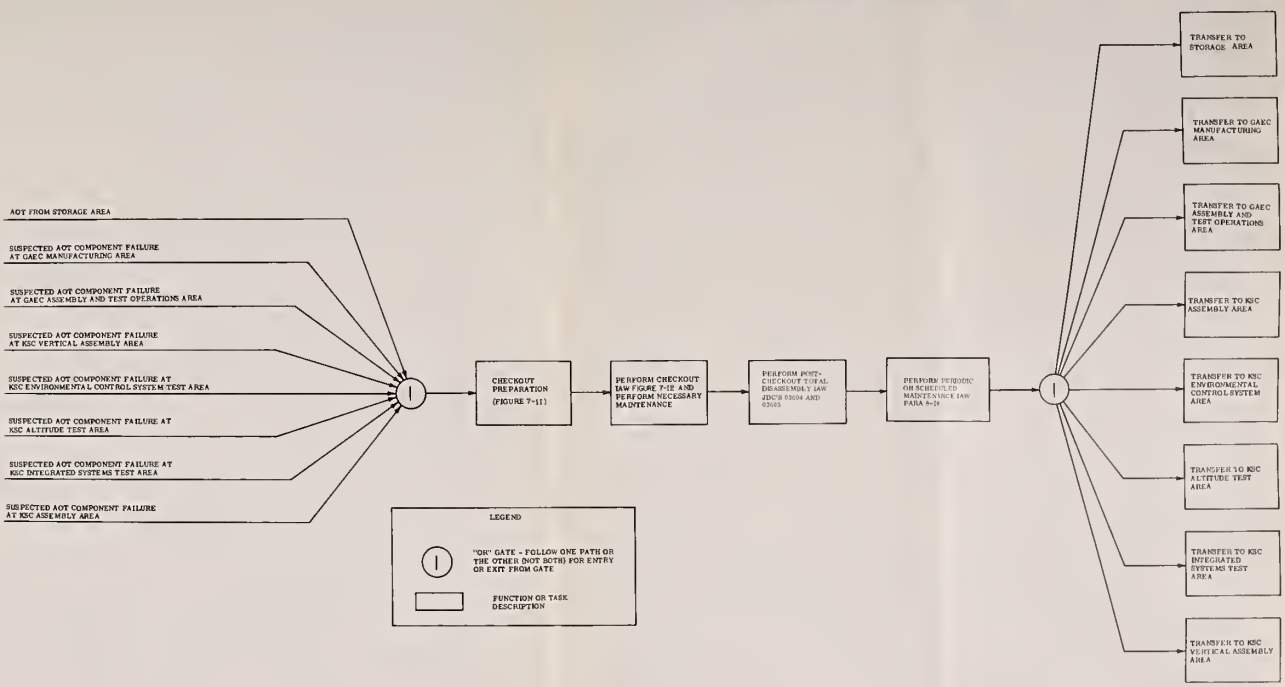


Figure 7-10. AOT Master Checkout Flowgram

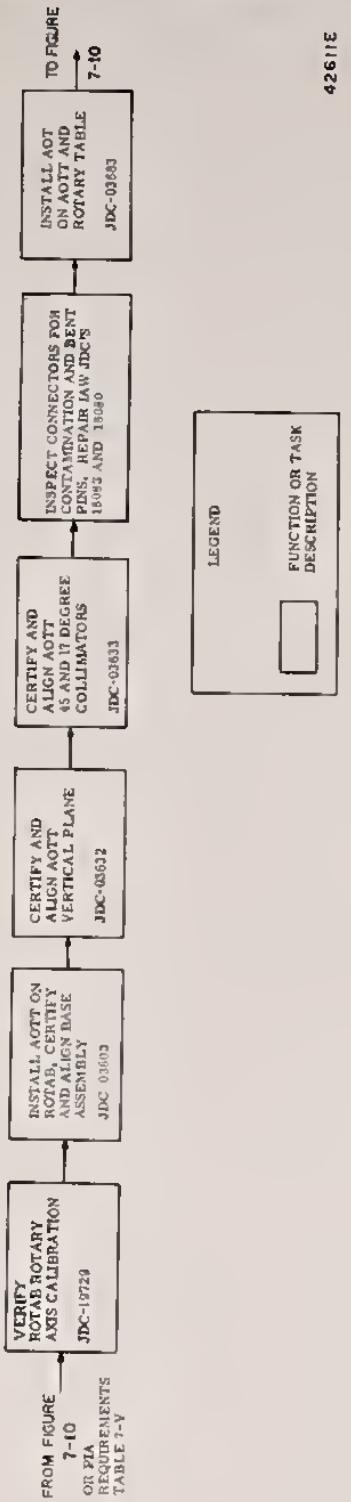


Figure 7-11. AOT Checkout Preparation Flowgram

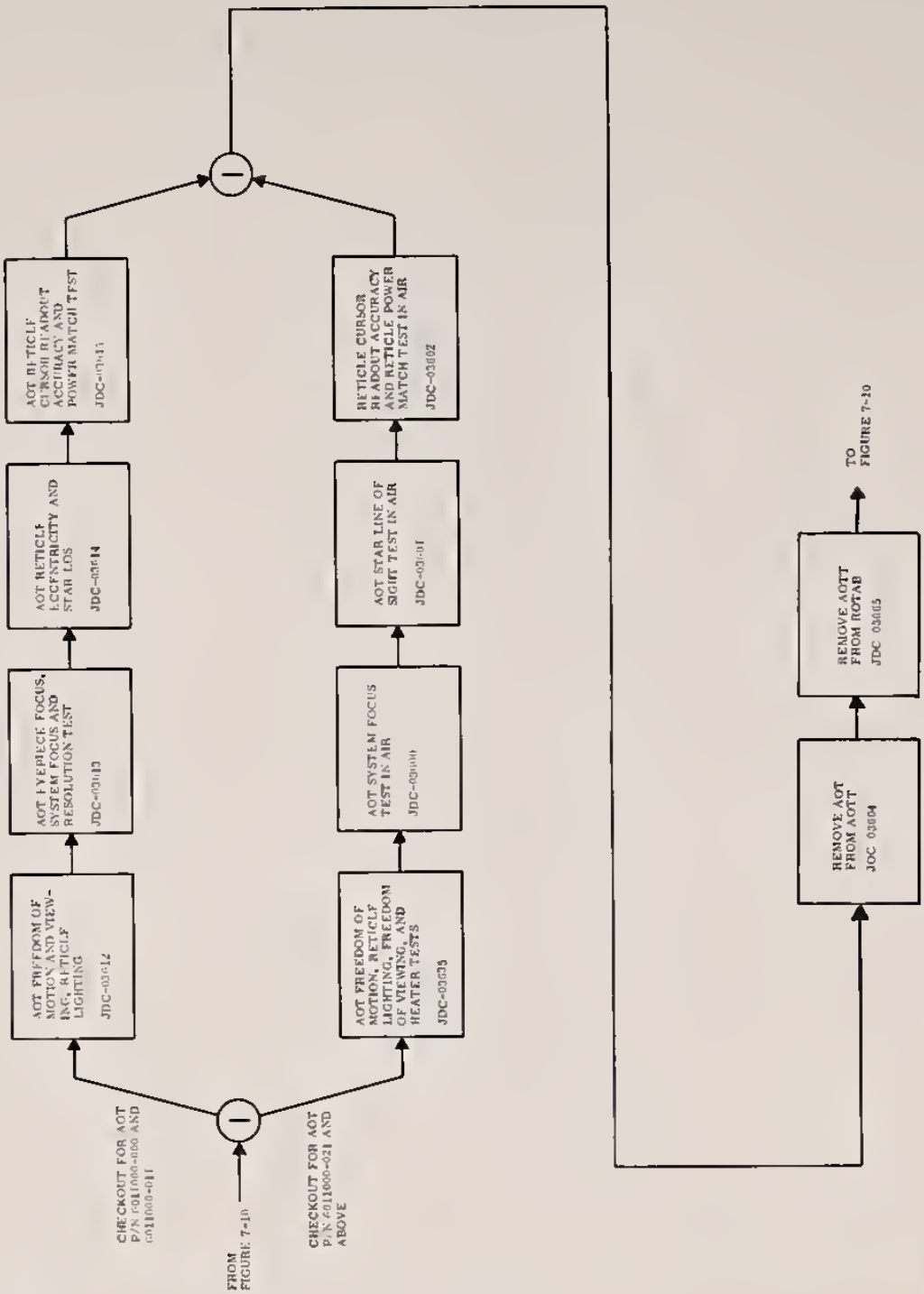


Figure 7-12. AOT Checkout Flowgram

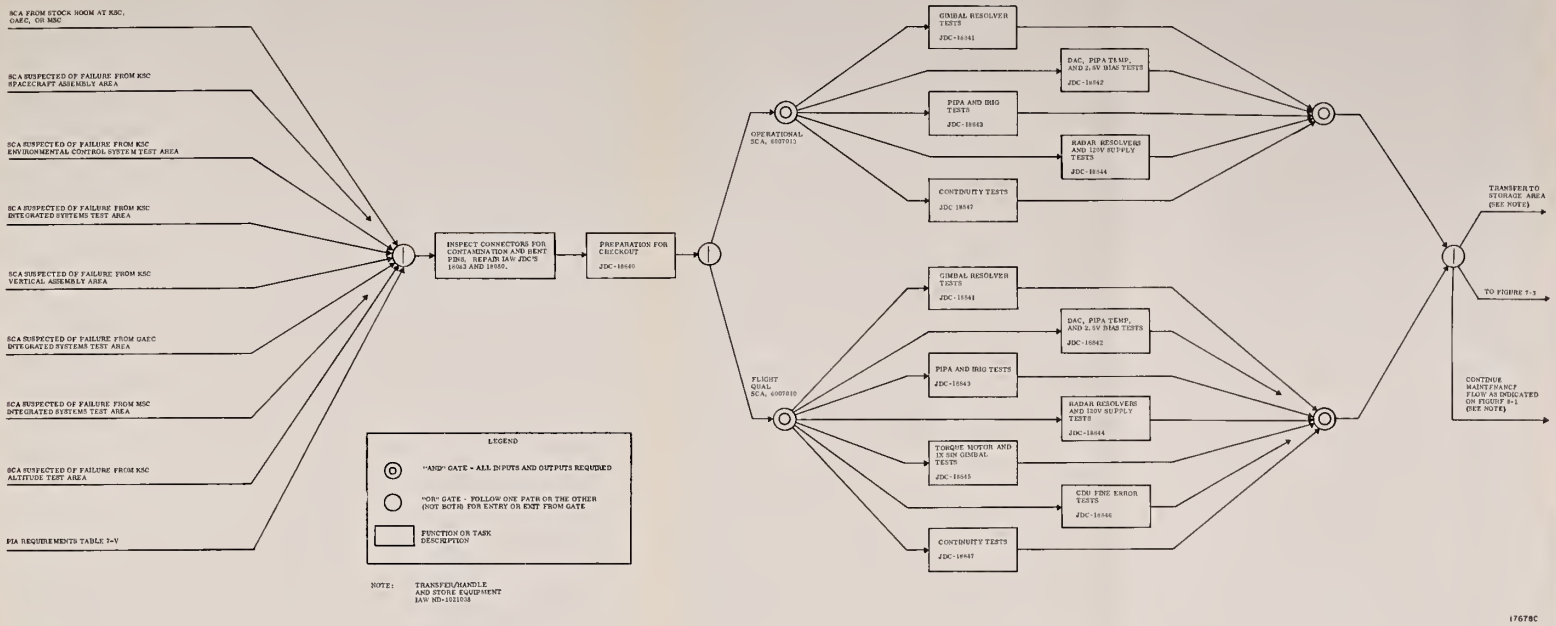


Figure 7-13. SCA Master Checkout Flowgram

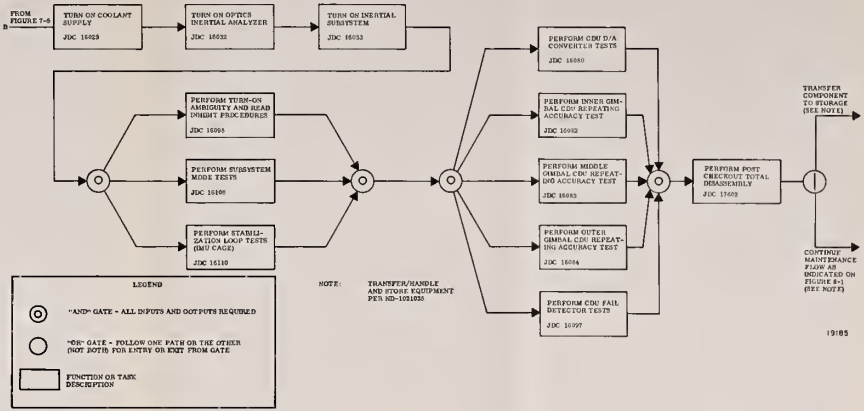


Figure 7-14. CDU Pre-Installation Acceptance Test Flowgram

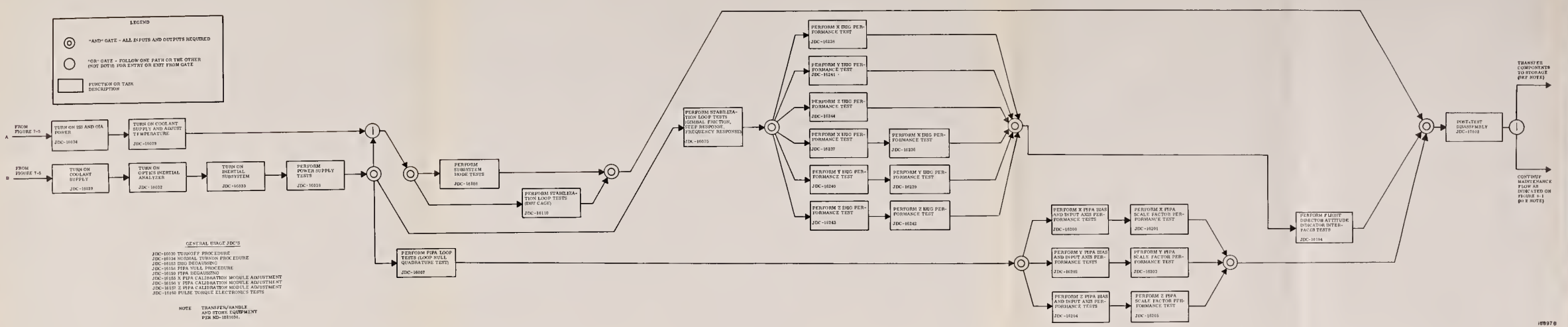


Figure 7-15. IMU and PTA Pre-Installation Acceptance Test Flowgram

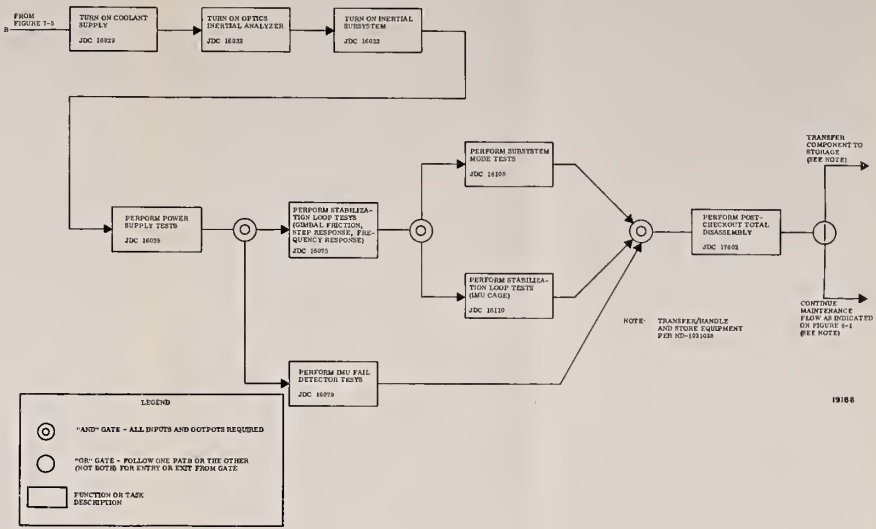


Figure 7-16. PSA Pre-Installation Acceptance Test Flowgram

Chapter 8

MAINTENANCE

8-1 SCOPE

This chapter describes the procedures performed in the G & N laboratory for malfunction isolation, removal and replacement, repair verification, pre-power assurance (PPA), and malfunction verification in accordance with the maintenance concept. References to JDC's are included for removal and replacement procedures, PPA tests, malfunction verification tests, and repair verification requirements. Included in this chapter are lists of schematic diagrams and mechanization drawings for malfunction isolation. (Refer to tables 8-I and 8-II.)

8-2 MAINTENANCE CONCEPT

Figure 8-1 presents, in flow diagram format, the maintenance concept for the PGNCS. Paragraph references identify the supporting text for the various maintenance tasks depicted on the flowgram.

Repair of the PGNCS consists of isolating a malfunction to the lowest replaceable item spared and replacing that item with a spare item that has received a PIA test. Repair of the PGNCS is limited to replacement of the following items:

(1) LGC
(2) DSKY
(3) flight ropes or test ropes
(4) CDU
(5) PSA
(6) IMU and PTA
(7) AOT
(8) PGNCS interconnect harness A
(9) PGNCS interconnect harness B
(10) CCRD

(11) nav base

(12) signal conditioner

(13) signal conditioner modules

(14) DSKY EL and IL indicators

When a malfunction cannot be isolated to a single component, the suspected components shall be removed and subjected to ISS, CSS, or AOT checkout, whichever is applicable. After identification of the discrepant component(s), the remaining components may be re-installed in the spacecraft without requiring PIA testing. Before the replacement for the malfunctioned item is operated in the spacecraft, the malfunctioned component must be subjected to malfunction verification testing.

The spare item or component must have received a PIA test prior to installation in the spacecraft. When a spare item is to be installed in a PGNCS in the laboratory, however, it need not be subjected to PIA testing since the PGNCS must be subjected to repair verification testing.

8-3 MALFUNCTION ISOLATION-ANALYSIS

Malfunction isolation consists of employing troubleshooting techniques to isolate a malfunction to the lowest replaceable item spared. The following aids will prove helpful for troubleshooting a LEM PGNCS:

(1) Electrical adapter cable assembly set used for signal monitoring and continuity and resistance testing in conjunction with JDC 18053.

(2) PGNCS and ISS loop diagrams and schematics (see Table 8-I).

(3) CSS logic diagrams and schematics (see table 8-II).

(4) Engineering data.

(5) ND 1021040, Supplement B.

Malfunction isolation of PGNCS laboratory test configurations can be accomplished using the above aids, but in particular by using ND 1021040, Supplement B and the electrical adapter cable assembly set.

8-3.1 ELECTRICAL ADAPTER CABLE ASSEMBLY SET. The electrical adapter cable assembly set is used to monitor signals and perform continuity tests for malfunction isolation of PGNCS components. The electrical adapter cable assembly set can be used in conjunction with monitor circuit diagrams (MCD's) and loop diagrams located in ND 1021040, Supplement B and also with engineering mechanization diagrams, schematics, and interconnect diagrams listed in table 8-1 of ND 1021042. Operating instructions and cable break-in information for use of the electrical adapter cable

assembly set to monitor signals during system and ISS testing are given in JDC 18053. Instructions for airborne cable continuity testing and airborne component continuity and resistance testing are also provided in JDC 18053.

8-3.2 ARRANGEMENT OF ND 1021040 SUPPLEMENT B. Supplement B is generally arranged by type of information (i.e. loop diagrams, MCD's, networks, etc.). It is not component oriented. Each type of information is grouped together and has one or more tab cards associated with it providing a skeletal index to the information.

8-3.2.1 Monitor Circuit Diagrams (MCD's). MCD's show the detailed routing of all airborne and GSE signals monitored by the OITS and associated BM-GSE. With an MCD, a monitored signal displaying an abnormal indication can be traced from its monitoring device in the OITS (such as the DVM), through the GSE selection circuitry (such as the crossbar switch), to its source in the airborne G & N system, ISS, or GSE. The MCD's often reference related loop diagrams for additional aid in trouble analysis.

Refer to chapter B10 in ND 1021040 for detailed instructions on MCD usage. Tables B10-I through B10-VII index specific MCD's for each test point or switch position on the OITS and associated BM-GSE. Table B10-I, for example, references a specific MCD for each position of the crossbar switch.

The MCD shows the jack and pin numbers of the airborne interface and includes additional airborne circuitry to illustrate the signal source. A malfunction can be isolated to either an airborne component or GSE equipment by monitoring the signal at the airborne interface, using the electrical adapter cable assembly set as specified in JDC 18053.

8-3.2.2 LEM GSE Signal Selection List. The LEM GSE signal selection list, table B10-X in ND 1021040, lists the name and test point location of all LEM airborne signals which can be monitored by the OITS and associated BM-GSE during system or ISS testing. In the event of a malfunction, table B10-X can be used to locate test points at which airborne and GSE signals related to the malfunction can be monitored. If a monitored signal displays an abnormal indication, the applicable MCD for that test point can be located by referring to the MCD index.

8-3.2.3 Loop Diagrams. The loop diagrams listed in ND 1021040, Supplement B are detailed schematics of the OITS and associated BM-GSE circuitry, including the related airborne interface circuitry. The loop diagrams illustrate how various components of the OITS and BM-GSE operate together to control or test the airborne system or ISS test configurations; these diagrams also show the power and loading circuitry used to simulate normal airborne operational environment. Associated loops and MCD's are referenced on the loop diagrams as further aids for trouble analysis. The loop diagrams depict the jack and pin numbers of the airborne interface and additional airborne circuitry to aid in understanding loop operation. A malfunction can be isolated to either an airborne component or GSE equipment by monitoring loop signals at the airborne interface, using the electrical adapter cable assembly set as specified in JDC 18053.

Refer to chapter B9 in ND 1021040 for detailed information on loop diagram usage, and table B9-III for a listing of loop diagrams associated with LEM testing. Also, chapter B6 contains a functional description of each LEM loop diagram as a further aid to understanding loop operation.

8-3.2.4 MCD and Loop Diagram Selection. Refer to table 8-IA for a general guide to the selection of MCD's and loop diagrams in the event of an abnormal indication. It is assumed that the abnormal indication has occurred during the performance of a JDC for system or ISS testing.

8-3.2.5 Blade Blocks. Blade blocks and mating connectors are used as tie points in the OIA and GDB wire harnesses. Each blade block section mates with a correspondingly numbered and lettered connector (i.e. J109A mates with P109A). In the MCD's, the complete unit, including blade block and mating connector, is identified only by the mating connector P number. The blade blocks provide a convenient location to verify the presence of a signal. Refer to paragraph B10-14 in ND 1021040, Supplement B for detailed information on the usage of blade blocks.

8-3.2.6 Network Lists. The network lists are a special version of the OIA backwall running list. Each network consists of a grouping of points (connector pins, terminal board terminals, etc.) which are electrically tied together within the OIA backwall wire harness. The networks are convenient for tracing a circuit through the backwall harness and for isolating malfunctions since they show all points at which signals can be monitored. Refer to chapter B12 in ND 1021040, Supplement B for detailed information on network usage.

8-3.3 TEST POINT SIGNAL CHARACTERISTICS. Chapter 3 in ND 1021042 will be expanded to provide a tabular listing of test point signal characteristics. The test point signal characteristics will aid in identifying and isolating malfunctions during signal monitoring with the electrical adapter cable assembly set or using the OITS and associated BM-GSE signal monitoring capability.

8-3.4 CSS MALFUNCTION ISOLATION. Program listings of CSS test tapes have been provided as a supplement to ND 1021042 for use during testing and during malfunction isolation of CSS problems. If a malfunction occurs, analysis can proceed with the use of the program listings; loop, schematic, and logic diagrams listed in table 8-II; and computer theory of operation in chapter 4.

8-4 REMOVAL AND REPLACEMENT

Removal and replacement procedures for use in the G and N laboratory test configurations are given in JDC's listed in table 8-III.

8-5 REPAIR VERIFICATION

After installation of a spare component in the PGNCS at the G & N laboratory, a partial system checkout is performed to verify that the system is repaired. Refer to

table 8-IV for retest requirements to insure that satisfactory system performance may be attained and to verify tbat the previously observed malfunction has been corrected. Refer to table 8-IVA for SCA retest requirements after module replacement.

If no malfunction occurs during repair verification, the system is considered to be repaired and system checkout may be resumed at the JDC at which the malfunction originally occurred.

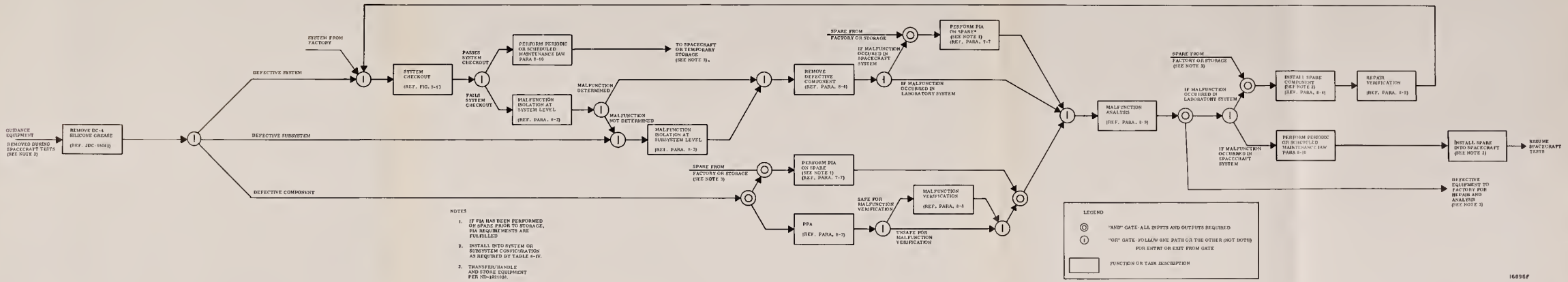


Figure 8-1. Master Maintenance Flowgram

Table 8-1. PGNCS and 1SS Loop Diagrams and Schematics

Title	NASA Drawing
LEM +28 VDC Power Distribution	6015570
LEM 0 VDC Power Distribution	6015571
LEM +28 VDC 800 ~ Power Distribution	6015572
PTPS Output	6015573
Apollo Stab Loop - LEM	6015564
Apollo PIPA Loop - LEM	6015563
IMU-R/R CDU Block Diagram-Block II	2015566
LEM 5-Axis Moding Diagram	6015562
IMU Temperature Control System-Block II	
Two Wire Mechanization Diagram	2001452
Schematic Diagram	2001463

Table 8-1A. MCD and Loop Diagram Selection

Abnormal Indication	Reference Source	MCD or Loop Diagram Selection
Abnormal indication displayed on OITS monitoring device (such as an out-of-tolerance voltage indication on DVM, PAVM, oscillograph, oscilloscope, etc.)	Refer to MCD index, tables B10-1 through B10-VII in ND 1021040, Supplement B, to locate applicable MCD.	Select MCD and associated loop diagrams referenced from MCD.
Failure associated with OITS pushbutton or control (such as failure of ISS OPERATE pushbutton to light as specified in JDC).	a. Select loop diagram by relating OITS pushbutton or control (nomenclature or function) with loop titles in list of LEM loops (table B9-III in ND 1021040, Supplement B).	Select loop diagrams and associated MCD's referenced from loop diagram.
	b. If OITS pushbutton or control cannot readily be associated with a particular loop title in table B9-III, refer to panel control and indicator descriptions in chapter B2 of ND 1021040 for additional information that will aid in loop diagram selection.	Select loop diagrams and associated MCD's referenced from loop diagrams.

Table 8-IA. MCD and Loop Diagram Selection

Abnormal Indication	Reference Source	MCD or Loop Diagram Selection
	c. If failure can be associated with a relay in an OITS panel, refer to relay operation charts in chapter B11 of ND 1021040, Supplement B.	Select applicable loop diagram or MCD referenced in relay operation chart.
Abnormal indication displayed on DSKY when performing JDC during system testing (such as an incorrect data display indication), or any other abnormal indication displayed during system testing.	a. Refer to ND 1021042 for the following information to determine area of malfunction: (such as computer subsystem, PIPA loop, stabilization loop, etc.): (1) JDC test descriptions listed in chapter 7. (2) System and subsystem functional analysis in chapter 2. (3) Component and module functional descriptions and test point signal characteristics in chapter 3.	

Table 8-IA. MCD and Loop Diagram Selection

Abnormal Indication	Reference Source	MCD or Loop Diagram Selection
	(4) Component and module detailed theory of operation in chapter 4. (5) List of system mechanization drawings, schematics, and logic diagrams in tables 8-1 and 8-II in chapter 8.	
	b. After determining area of malfunction, refer to LEM signal selection list, table B10-X, in ND 1021040, Supplement B to locate test points at which airborne signals related to the malfunction can be monitored.	
	c. If monitored signal(s) displays an abnormal indication, refer to MCD index, tables B10-I through B10-VII, in ND 1021040, Supplement B to locate applicable MCD.	Select MCD's and associated loop diagrams referenced from MCD's.

(Sheet 3 of 4)

Table 8-IA. MCD and Loop Diagram Selection

Abnormal Indication	Reference Source	MCD or Loop Diagram Selection
Failure associated with relay in OITS panel.	Refer to relay operation charts in chapter B11 of ND 1021040, Supplement B for reference to applicable loop diagrams or MCD.	Select loop diagrams or MCD.

(Sheet 4 of 4)

Table 8-II. CSS Logic Diagrams and Schematics

Title	Drawing Number		
	Tray A Subassembly		
	LGC 2003100	LGC 2003200	LGC 2003993
Module A1	2005059	2005259	2005259
Module A2	2005060	2005260 2005266 with ECP 564*	2005260
Module A3	2005051	2005251	2005251
Module A4	2005062	2005262	2005262
Module A5	2005061	2005261	2005261
Module A6	2005063	2005263	2005263
Module A7	2005252	2005252	2005252
Module A8	2005055	2005255	2005255
Module A9	2005056	2005256	2005256
Module A10	2005057	2005257	2005257
Module A11	2005058	2005258	2005258
Module A12	2005053	2005253	2005253
Module A13	2005069	2005269	2005269
Module A14	2005074	2005264	2005264
Module A15	2005065	2005265	2005265
Module A16	2005066	2005266	2005266
Module A17	2005067	2005267	2005267
Module A18	2005068	2005268	2005268
Module A19	2005070	2005270	2005270
Module A20	2005054	2005254	2005254
Module A21	2005050	2005250	2005250
Module A22	2005071	2005271	2005271
Module A23	2005072	2005272	2005272
Module A24	2005073	2005273	2005273
Interface A25, A26	2005021	2005021 2005928 with ECP's 501 & 505*	2005928
Interface A27 to A29	2005020	2005912 2005933 with ECP's 501 & 505*	2005933
Power supply module A30, A31	2005010	2005916 2005945 with ECP 486* 2005971 with ECP 518*	2005936 2005971 with ECP 518*

*See table 3-IE for effectivity.

Table 8-II. CSS Logic Diagrams and Schematics

Title	Drawing Number		
	Tray B Subassembly		
	LGC 2003100	LGC 2003200	LGC 2003993
Rope memory module B1 to B6			
Oscillator module B7	2005003	2005003 2005930 with ECP's 501 & 505*	2005930
Alarm module B8	2005028	2005927 2005975 with ECP 719*	2005927 2005975 with ECP 719*
Erasable driver module B9, B10	2005915	2005104 2005934 with ECP's 501 & 505*	2005934
Current switch module B11	2005005	2005005 2005925 with ECP's 501 & 505*	2005925
Erasable memory module B12	2005006	2005106 2005931 with ECP 505*	2005931
Sense amplifier module B13	2005914	2005920 2005932 with ECP's 501 & 505* 2005970 with ECP 483*	2005932 2005970 with ECP 483*
Sense amplifier module B14	2005914	2005919 2005929 with ECP's 501 & 505*	2005929 2005969 with ECP's 501 & 505*
Strand select module B15	2005009	2005924 2005926 with ECP's 501 & 505*	2005926
Rope driver module B16, B17	2005913	2005100 2005942 with ECP 440* 2005938 with ECP's 501 & 505*	2005938

*See table 3-IE for effectivity.

Table 8-II. CSS Logic Diagrams and Schematics

Title	Drawing Number		
	DSKY		
	DSKY 2003985	DSKY 2003950	DSKY 2003994
DSKY interconnection dwg	2005950	2005953	2005954
Indicator driver module D1 to D6	2005952	2005952	2005973
Keyboard module D8	2005903	2005903	2005939
Power supply module D7	2005904	2005921	2005937

(Sheet 3 of 3)

Table 8-II. CSS Logic Diagrams and Schematics

Title	NASA Drawing	
Tray B Subassembly		
	LGC 2003100	LGC 2003200
Rope Memory Module B1-B6	2005012	2005012
Oscillator Module B7	2005003	2005003
Alarm Module B8	2005028	2005922
Erasable Driver Module B9, B10	2005915	2005104
Current Switch Module B11	2005005	2005005
Erasable Memory Module B12	2005006	2005106
Sense Amplifier Module B13, B14	2005914	2005919
Strand Select Module B16	2005009	2005009
Rope Driver Module B16, B17	2005913	2005100
DSKY		
	DSKY 2003985	DSKY 2003950
DSKY Assembly	2005950	2005953
Indicator Driver Module D1-D6	2005952	2005952
Keyboard Module D8	2005903	2005903
Power Supply Module D7	2005904	2005921

(Sheet 2 of 2)

Table 8-III. List of Removal and Replacement JDC's

Title	Number
Remove and Replace PGNCS Components (LEM)	17601
Remove and Replace Inertial Subsystem Components (LEM)	17602
Installation Of The Alignment Optical Telescope Tester On The Rotary Table	03624
Remove AOT From AOTT	03604
Installation Of The Alignment Optical Telescope On The Alignment Optical Telescope Tester	03683
Remove AOTT From ROTAB	03605
Installation And Removal Of Fixed Memory Modules And Fixed Memory Jumper Modules-Block II And LEM	05416
Computer Installation And Removal Procedure-Block II And LEM	05417
DSKY Installation And Removal Procedure-Block II And LEM	05418
Remove and Replace SCA Modules	17603
DSKY E/L Installation and Removal Procedure-Block II	05798
DSKY I/L Installation and Removal Procedure-Block II	05799

Table 8-IV. Retest Requirements

Component Replaced	Retest JDC Number
PGNCS interconnect harness "A"	12692
PGNCS interconnect harness "B"	12693
CDU	12685
IMU and PTA	12688
PSA	12691
LGC	12686
DSKY	12687
CCRD	12689
SCA*	12620

*For SCA module retest requirements, see table 8-IVA.

Table 8-IVA. SCA Retest Requirements

SCA Module Replaced	SCA JDC'S							
	12620	18840	18841	18842	18843	18844	18845	18846
Gimbal resolver	X	X	X					
IRIG and PIPA	X	X			X			
DAC, PIPA temp, and 2.5V bias	X	X		X				
Torque motor and 1X sine gimbal resolver	X	X					X	
CDU fine error and IRIG temp	X	X						X
Radar resolver and 120V PIPA supply	X	X				X		

8-6 DELETED.

(See paragraph 7-7.)

Pages 8-9, 8-10, and 8-11/8-12 (table 8-V and figure 8-2) deleted.

8-6 PRE-INSTALLATION ACCEPTANCE

PIA tests shall be performed on all spare components prior to installation in the spacecraft. PIA tests are not required for spare components to be installed in a PGNCS in the laboratory. PIA test procedures are given in JDC's listed in table 8-V. Perform the procedures in the sequence given for the applicable component. Auxiliary airborne equipment can be used to complete a test setup. (See paragraph 8-11).

Table 8-V. Procedures for Components Requiring PIA Tests

Component	Procedures
AOT	Perform AOT checkout in accordance with figure 7-10.
CDU	1. Perform test preparation procedures in accordance with figure 7-5. 2. Perform following JDC's in sequence listed: 16097 16080 16098 16108 16110 16082 16083 16084 3. Disassemble test setup per JDC 17602.
Computer control and reticle dimmer assembly	Perform JDC 18830.
DSKY	Perform following JDC's in sequence listed: 05415 05417 05418 05419 05420 05771 05783
IMU and PTA	1. Perform complete test preparation procedures in accordance with figure 7-5. 2. Perform checkout in accordance with figure 8-2.
LGC and DSKY	Perform CSS checkout in accordance with figure 7-8.

(Sheet 1 of 2)

Table 8-V. Procedures for Components Requiring PIA Tests

Component	Procedures
PGNCS interconnect harness	Perform PGNCS checkout in accordance with figure 7-2.
PSA	1. Perform complete test preparation in accordance with figure 7-5. 2. Perform following JDC's in sequence listed: 18831 16039 16079 16108 16110 16075 3. Disassemble test setup per JDC 17602.
SCA	Perform SCA checkout in accordance with figure 7-13.

(Sheet 2 of 2)

8-6 PRE-INSTALLATION ACCEPTANCE

PIA tests shall be performed on all spare components prior to installation in the spacecraft. PIA tests are not required for spare components to be installed in a PGNCS in the laboratory. PIA test procedures are given in JDC's listed in table 8-V. Perform the procedures in the sequence given for the applicable component. Auxiliary airborne equipment can be used to complete a test setup. (See paragraph 8-11).

Table 8-V. Procedures for Components Requiring PIA Tests

Component	Procedures
AOT	Perform AOT checkout in accordance with figure 7-10.
CDU	1. Perform test preparation procedures in accordance with figure 7-5. 2. Perform following JDC's in sequence listed: 16097 16080 16098 16108 16110 16082 16083 16084 3. Disassemble test setup per JDC 17602.
Computer control and reticle dimmer assembly	Perform JDC 18830.
IMU and PTA	1. Perform complete test preparation procedures in accordance with figure 7-5. 2. Perform checkout in accordance with figure 8-2.
LGC and DSKY	Perform CSS checkout in accordance with figure 7-8.

(Sheet 1 of 2)

Table 8-V. Proccdures for Components Requiring PIA Tests

Component	Procedures
PGNCS interconnect harness	Perform PGNCS checkout in accordance with figure 7-2.
PSA	1. Perform complete test preparation in accordance with figure 7-5. 2. Perform following JDC's in sequence listed: 18831 16039 16079 16108 16110 16075 3. Disassemble test setup per JDC 17602.
SCA	Perform SCA checkout in accordance with figure 7-13.

(Sheet 2 of 2)

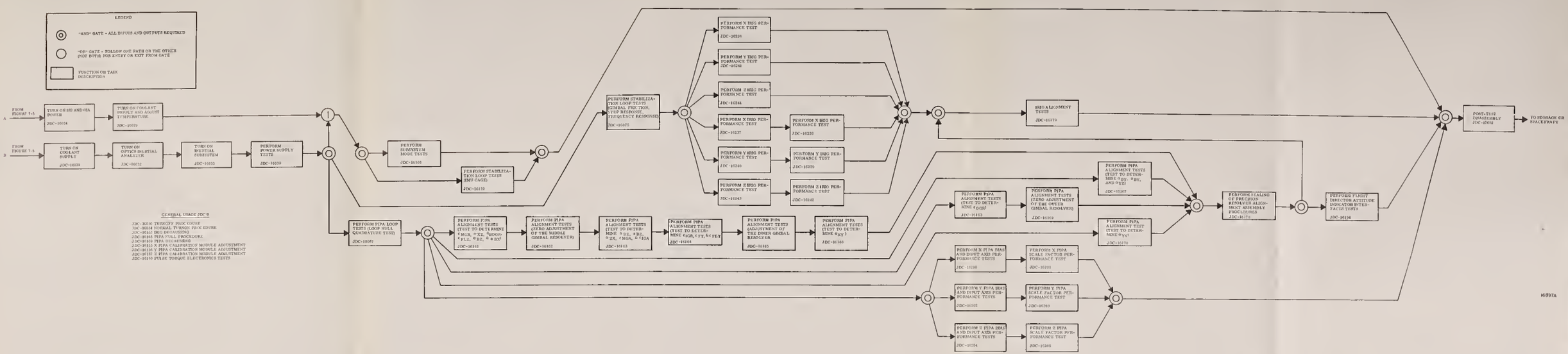


Figure 8-2. IMU and PTA Pre-Installation Acceptance Test Flowgram

8-7. PRE-POWER ASSURANCE

PPA tests shall be performed on all suspected malfunctioned components removed from a spacecraft installation to assure that the PGNCS or subsystem used for malfunction verification will incur no damage. PPA test procedures are given in table 8-VI. Components not successfully passing PPA testing will be evaluated for final verification and/or disposition.

Table 8-VI. PPA JDC's

Component	JDC Number
AOT	N/A
CDU	18874
CCRD	N/A
IMU and PTA	18872
LGC and DSKY	N/A
PGNCS interconnect harness	N/A
PSA	18873
Signal conditioner	N/A

8-8 MALFUNCTION VERIFICATION

Prior to operation of a spare component in the spacecraft, the malfunction must be verified in the removed component. Malfunction verification for all components other than the PGNCS interconnect harness consists of performance of the PIA tests listed in table 8-V. The PIA tests are to be completed only to the point where the malfunction is verified. Auxiliary airborne equipment can be used to complete a test setup. (See paragraph 8-11.) Malfunction verification for the PGNCS interconnect harness consists of performing continuity checks on those parts of the harness which are related to the malfunction. PPA tests are required as a prerequisite to malfunction verification for those components listed in table 8-VI when those components are removed from the spacecraft.

8-9 MALFUNCTION ANALYSIS

After a malfunction has been verified, an analysis is performed to determine if the malfunction was caused by another PGNCS failure, or if the malfunction could have caused other damage in the PGNCS. If the analysis indicates other malfunctions may exist, further malfunction isolation and malfunction verification testing are required.

The results of the malfunction analysis are returned to the factory, along with the failed component, to aid in factory analysis of the malfunction. A malfunction analysis is also required for non-recurring malfunctions and non-verified malfunctions.

8-10 MAINTENANCE SCHEDULE

Maintenance of electrical connectors involves special applications of anti-corrosion lubricants. Maintenance of the AOT requires special procedures, techniques, and equipment. Refer to table 8-VII for JDC's to be performed as specified.

Table 8-VII. Maintenance Schedule

Maintenance Operation	JDC No.	Schedule
Clean AOT	02820	As required with approval of responsible engineer
Purge AOT angle counter	03256	Every 6 months
Maintenance and inspection of AOT	03650	Every 6 months as specified in JDC 03650
Lubricate connectors	18079	As required
Lubricate connectors, pins, and contacts	18078	Prior to spacecraft installation
Straightening of pin contacts	18080	As required
Remove DC-4 silicone grease from airborne component connector contacts	18081	After removal of component from spacecraft
Moisture proof assembly screwheads	18082	As required
Clean connectors and components	18083	As required
Repair painted surfaces	18084	As required
Remove corrosion from magnesium surfaces	18085	As required
Perform mercury decontamination and handling safety procedure	18086	As required
Inspect microdot connector	18099	As required
Lubricate and clean component header helicoil inserts and engaging hardware	18100	Prior to each laboratory test setup and at the completion of all testing

8-10A REMOVAL OF ETHYLENE GLYCOL SOLUTION LEAKS AND SPILLS. Perform the appropriate JDC's as necessary in the event of ethylene glycol solution leaks or spills.

JDC 18087	Removal of Ethylene Glycol Solution Leaks and Spills — General Instructions
JDC 18088	Removal of Ethylene Glycol Solution Leaks and Spills — Airborne Harnesses
JDC 18089	Removal of Ethylene Glycol Solution Leaks and Spills — AOT
JDC 18090	Removal of Ethylene Glycol Solution Leaks and Spills — CDU, CMG, LGC, PSA, PTA, and PEA
JDC 18091	Removal of Ethylene Glycol Solution Leaks and Spills — DSKY
JDC 18092	Removal of Ethylene Glycol Solution Leaks and Spills — IMU
JDC 18093	Removal of Ethylene Glycol Solution Leaks and Spills — CCRD and Indicator Control Panel
JDC 18095	Removal of Ethylene Glycol Solution Leaks and Spills — SCA
JDC 18096	Removal of Ethylene Glycol Solution Leaks and Spills — Nav Base, and Eyepiece Storage Unit
JDC 18097	Removal of Ethylene Glycol Solution Leaks and Spills — GSE Components, and GSE Interconnect Harnesses

8-11 AUXILIARY AIRBORNE EQUIPMENT

Auxiliary airborne equipment (AAE) is defined as that equipment required to complete a system or subsystem test setup when the assigned components of the system or subsystem are not available. AAE can be composed of the following:

(1) Qualification test equipment (QUAL TEST)

(2) Evaluation test equipment (EVAL TEST)

(3) Flight equipment (equipment previous flown) (FLIGHT)

(4) Test articles (equipment specifically purchased for use as AAE).

The following conditions must be fulfilled to use AAE in a test setup.

(1) Qualification test equipment, evaluation test equipment, and equipment previously flown must be recycled through the factory manufacturing area and meet the functional requirements of the applicable procurement specification before it is designated AAE.

(2) Configuration of AAE must fulfill requirements of compatibility tables (chapter 3).

(3) AAE must be continually maintained in accordance with the functional requirements for operational airborne equipment.

Appendix A

LIST OF TECHNICAL TERMS AND ABBREVIATIONS

Term	Definition
a	Accelerometer
AAC	Automatic amplitude control
AAE	Auxiliary airborne equipment
ACA	Attitude controller assembly
ACCEL	Accelerometer
ACE	Automatic checkout equipment
ACTREQ	Action request
ACTY	Activity
A/D	Analog to digital
AD	Add
ADIA	Gyro drift due to acceleration along the input axis caused by an unbalance on the spin reference axis
ADSRA	Gyro drift due to acceleration along the spin reference axis caused by an unbalance on the input axis
AGC	Apollo guidance computer
AGC/OC	AGC CTS operation console
AGS	Abort guidance section
AIICR	Apollo integrated inventory and consumption report
AIG	Inner gimbal angle
αB	Hypothetical rotation of the PIP case about its output axis equivalent to bias. Subscripts (X, Y, or Z) may be added to denote a specific PIP case rotation

Appendix A (cont)

Term	Definition
αX, αY, or αZ	Misalignment of PIP case about stable member axis. Subscripts (X, Y, or Z) may be added to denote a specific PIP case misalignment
A_{MG}	Middle gimbal angle
A_{OG}	Outer gimbal angle
AOT	Alignment optical telescope
ATCA	Attitude and translation control assembly
ATP	Assembly test procedure
Att	Attitude
BAL	Bank Alarm
BD	Bias drift of IRIG. Subscripts (X, Y, or Z) may be added to denote a specific IRIG bias drift
BKTF	Block transfer
CA	Coarse align
CAGEN	Counter address generate
CCB	Configuration control board
CCRD	Computer control and reticle dimmer assembly
CCS	Count, compare and skip
CDU	Coupling data unit
CDU Z	CDU zero
CES	Control electronics section
CIS	Communications and Instrumentation System
CLR	Clear
CM	Command module
CMC	Command module computer
CS	Clear and subtract
CSM	Command and service module
CSS	Computer subsystem
CTRAL	Counter fail alarm
CTRDR	Request to increment counter
CTS	Computer test set

Appendix A (cont)

Term	Definition
CYL	Cycle left
CYR	Cycle right
D/A	Digital to analog
DAC	Digital to analog converter
DECA	Descent engine control assembly
DKEND	Downlink end
DLKHN	Downlink inhibit
DLNK	Downlink
DRB	Design review board
DSKY	Display and keyboard
DV	Divide
ECS	Environmental control system
EDS	Explosive devices subsystem
EEC	Enable error counter
ENC	Encoder
ENOFF	Engine off
ENON	Engine on
ENRST	Engine reset
EPS	Electrical power system
ERR	Error
E(Xg)	X gyro error signal
E(Yg)	Y gyro error signal
E(Zg)	Z gyro error signal
ϵIGA	Inner gimbal axis error
ϵIGR	Inner gimbal resolver error
ϵMGA	Middle gimbal axis error
ϵMGR	Middle gimbal resolver error
ϵOGR	Outer gimbal resolver error
FDAI	Flight director attitude indicator

Appendix A (cont)

Term	Definition
FINDVAC	Find vector accumulated data
FVP	Field verification procedure
g	Local gravity
GAEC	Grumman Aircraft Engineering Corporation
νX, γY, or γZ	Misalignment of IRIG case about stable member corresponding axis. (First subscript denotes a specific gyro, second subscript is added to denote a specific stable member axis about which the gyro input axis is misaligned.)
G and N	Guidance and navigation
GSE	Ground support equipment
GYRST	Gyro reset
IA	Input axis
IAW	In accordance with
ICTC	Inertial components temperature controller
IG	Inner gimbal
IIP	Interrupt in process
ILP	Parity inhibit
IMU	Inertial measuring unit
INC	Increase
INHINT	Inhibit interrupt
INKL	Counter increment request
IP	Interrogate pulse
IRIG	Inertial reference integrating gyro
IS	Instrumentation subsystem
ISS	Inertial subsystem
JDC	Job description card
K	Address or location
KEY RLSE	Key release
KRST	Key reset
KSC	Kennedy Space Center

Appendix A (cont)

Term	Definition
LBP	Lifting battery pack
LEM	Lunar excursion module
LER	Long eye relief
LGC	LEM guidance computer
LINK	Load location
LR	Landing radar
LSD	Least significant digit
LTC	Lifting temperature controller
MCT	Memory cycle time
MG	Middle gimbal
MINC	Minus increment
MIT/IL	Massachusetts Institute of Technology Instrumentation Laboratory
MKTRP	Mark trap
MNHRPT	Monitor inhibit interrupt
MP	Multiply
MSA & QR	Main summing amplifier and quadrature rejection module
MSC	Manned Spacecraft Center
MSD	Most significant digit
MSK	Mask
MSK K	Mask with data from K
MSTRT	Monitor start
N	Negative velocity pulse
NAA	North American Aviation
Nav	Navigation
nav base	Navigation base assembly
NBD	Normal bias drift
NDX	Index
NISQ	Next instruction sequence
NLT	Not less than

Appendix A (cont)

Term	Definition
NMT	Not more than
NOVAC	No vector accumulated data
OA	Output axis
OG	Outer gimbal
OIA	Optics-inertial analyzer
OINC	Display location
OITS	Optics-inertial test set
OPR	Operator
OUTCR	Out counter
OVCTR	Overflow counter
OVF	Overflow
P	Positive velocity pulse
P_I	Incrementing pulse
PA	Pre-amplifier
PA	Pendulum axis
PAC	Program analyzer console
PAL	Parity fail alarm
PCM	Pulse code modulated
PEA	PIPA electronics assembly
PGNCS	Primary guidance, navigation, and control system
ϕH_{MGA}	Corrected reading taken from the tilt axis optigon screen with rotary axis at θH_{OGA}, outer gimbal at precision zero, and middle gimbal axis in horizontal plane
ϕH_{RA}	Corrected reading taken from the tilt axis optigon screen with rotary axis in horizontal plane
P&M	Programmer and monitor
PIA	Pre-installation acceptance
PINC	Plus increment
PIP	Pulsed integrating pendulum
PIPA	Pulsed integrating pendulum accelerometer
PLSS	Portable life support system

Appendix A (cont)

Term	Definition
PPA	Prepower assurance
PRA	Pendulum reference axis
PROG	Program
PROG ALM	Program alarm
PSA	Power and servo assembly
PSAAM	Power and servo assembly adapter module
PTA	Pulse torque assembly
PTC	Portable temperature controller
PTPS	Pulse torque power supply
PVR	Precision voltage reference
RAGEL	Recommended Apollo Guidance Equipment List
RCS	Reaction control system
RDRST	Radar reset
REJ	Rejected
REL	Release
RF	Radio frequency
RGA	Rate gyro assembly
RIB	Retrofit instruction bulletin
RL	Read line
RLC	Resistance inductance capacitance
RLSE	Release
RLYBIT	Relay bit
RLYWD	Relay word
RPTAL	Interrupt lock alarm
RR	Rendezvous radar
RSET	Reset
S	Total gain from rotation about an IRIG input axis to voltage output of the preamplifier, (millivolts per milliradians). Subscripts (X, Y, or Z) may be added to denote a specific IRIG total gain voltage
SA	Servo amplifier

Appendix A (cont)

Term	Definition
S/C or SC	Spacecraft
SCA	Signal conditioner assembly
SCAFAL	Scalar fail alarm
SCS	Stabilization and control system
SF(A)	Scale factor of PIP. Subscripts (X, Y, or Z) may be added to denote a specific PIP scale factor
SFTG	Scale factor of torque generator, (milliradians per pulse). Subscripts (X, Y, or Z) may be added to denote a specific IRIG torque generator scale factor
SG	Signal generator
SHANC	Shift and add increment
SHINC	Shift increment
SIDL	System identification data list
SL	Shift left
SM	Stable member
SP	Switch pulse
SQG	Sequence generator
STBY	Standby
STD2	Standard subinstruction two
SU	Subtract
TC	Transfer control
TCA	Translation controller assembly
TCAL	Transfer control trap alarm
TDCR	Technical data change request
TDCR-RB	Technical data change request review board
TDRR	Technical data release or revision
TG	Torque generator
TM	Torque motor
TPA	Test point adapter
TS	Transfer to storage

Appendix A (cont)

Term	Definition
T/W	Thrust-to-weight
ULNK	Uplink
UNF	Underflow
UPTLM	Up telemetry
θH_{IGA}	Corrected reading taken from the rotary axis optigon screen with outer and middle gimbals at precision zero, and inner gimbal axis at local vertical
θH_{OGA}	Corrected reading taken from the rotary axis optigon screen with rotary axis horizontal and outer gimbal axis horizontal and east
θ + 1g	True table rotary axis angle which places PIP input axis opposite local vertical vector. Subscripts (X, Y, or Z) may be added to denote a specific PIP input axis
θ - 1g	True table rotary axis angle which places PIP input axis along local vertical vector. Subscripts (X, Y, or Z) may be added to denote a specific PIP input axis
V	Velocity or verb
WA	Write amplifier
WL	Write line
XCH	Exchange
XFMR	Transformer
ZID	Inhibit strobe

Appendix B

RELATED DOCUMENTATION

This appendix explains the function and relationship of the System Identification Data List (SIDL), the Apollo Integrated Inventory and Consumption Report (AIICR), the Aperture Card System, and the Technical Data Change Request Review Board (TDCR-RB) to the manual.

SIDL is an official release record for documents issued to impiement NASA contracts. SIDL identifies drawings, specifications, manuals and job description cards (JDC's), and other documents released to support the LEM Primary Guidance, Navigation, and Control System (PGNCS).

Manuals and JDC's are based upon the latest information available as of the publication freeze date. Manuals and JDC's are distributed after formal CCB approval. SIDL shall be consulted to determine which is the currently effective information. AC Electronics, Field Service Publications Department, will periodically revise the manuals and JDC's to the latest technical information releases.

The AIICR is a listing of all approved spare parts for the PGNCS and its associated ground support equipment (GSE).

The aperture card system is a compilation of documents in the Apollo program. Each aperture card consists of a mounted 35 MM microfilm copy of a complete document, with the exception that for manuals, only the title page, signature page, record of revisions page, and list of effective pages are included to identify the revision letter, change pages, and TDRR number.

Aperture card sets are maintained at all field sites and are used with the PGNCS manual to refer to schematics, wiring diagrams, and other drawings which are not included in the manual.

The TDCR-RB is a group composed of AC Electronics Publications, Engineering, Field Operations, MIT/IL, and NASA personnel. The board meets as required to process and disposition Technicai Data Change Requests (TDCR's).

Appendix C

LOGIC SYMBOLS

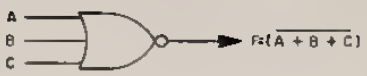
The computer contains NOR gates, extended NOR gates, and NOR gate flip-flops which are packaged in flat packs each containing two NOR gates. For a better understanding of the logic used in the computer, the logic symbols, terminology, and conventions used in logic descriptions in this chapter are discussed in detail in the following paragraphs.

The NOR gate (figure C-1) is a 3-input OR element with internal negation or inversion. This gate performs the logic function of $F = \overline{A + B + C}$, which is expressed as "neither A nor B nor C". From this the term NOR gate is derived.

The two more commonly used configurations of the NOR gate in the computer are the AND and OR functions, also illustrated on figure C-1. The AND function ($\bar{A} \cdot \bar{B} \cdot \bar{C}$) as expressed as "not A and not B and not C". Another way of expressing this function is to state than an output is present when not A and B and C are coincident. An actual application of the AND function will demonstrate still another way of describing this configuration. The gate shown has as inputs the negations $\overline{T09}$ and $\overline{XCH0}$. The output function is described as: signal RP2 is generated at time 9 during an Exchange instruction. This means of describing the AND function will appear more frequently in text than the others. An OR function is simply the inverted result of a NOR function. The output function F is present if either A or B is present. If neither A nor B is present, the function F is not present.

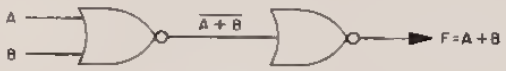
The extended NOR gate assumes the configuration shown on figure C-1. This is simply a method of increasing the number of inputs (fan-in) to produce a given function. On figure C-1 both gates are shown tangent to one another. They are drawn in this manner on many of the detailed logic drawings of this section since both gates follow in numerical sequence. However, both gates need not be, and on many drawings are not shown tangent to each other to produce the given function. The shaded portion of the lower gate indicates that it is an extension of the NOR gates shown above it through a common connection, which will be described in detail.

The dual NOR gate flat pack contains two NOR gates, each consisting of three NPN transistors with resistive inputs, as shown in figure C-2. The collector of each transistor is connected to a common load resistor, the other end of which is connected to

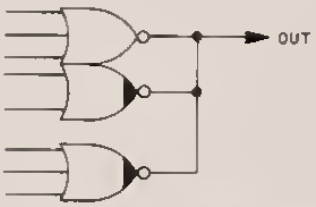


NOR GATE

AND FUNCTION



OR FUNCTION



EXTENDED NOR GATE

Figure C-1. NOR Gate Symbols

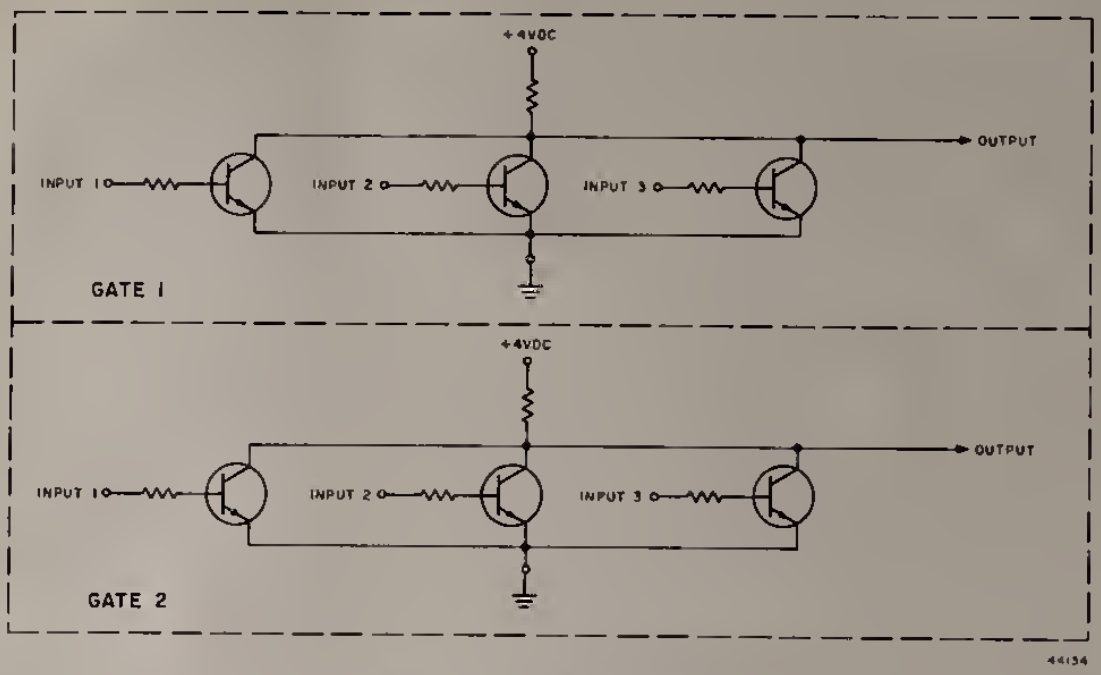


Figure C-2. Dual NOR Gate

the +4 vdc supply. All six emitters are common and are connected to ground. As a result of these connections, the logic levels for the computer can be defined (+4 vdc represents a logic ONE; approximately ground level represents a logic ZERO). Since an NPN transistor requires a positive transition for turn-on, a logic ONE at any one input or at all three inputs results in a logic ZERO at the output. To correlate this to the NOR gate symbol of figure C-1, consider that inputs A, B, and C are each a logic ONE. The output is logic ZERO or the inverted form of the input.

When all three inputs to the NOR gate are each logic ZERO, the transistors are cutoff. The output assumes the collector supply voltage (+4 vdc) or logic ONE. This latter condition can be correlated to the AND function of the NOR gate in figure C-1. When the two inputs ($\overline{T09} \cdot \overline{XCH0}$) are each logic ZERO, the output (RP2) is a logic ONE. In the detailed discussions which follow, a logic ZERO level is often referred to as enabling an associated input gate leg. For example, the negation input $\overline{T09}$ enables the gate coincident with $\overline{XCH0}$ (both inputs logic ZERO). An input gate leg is considered to be a logic ZERO if there is no connection to that particular leg. Each NOR gate has a capacity of three inputs. If connections are made to only two inputs, the third is considered to be logic ZERO, or the leg is enabled.

The fan-in capacity is increased to produce a given function using NOR gate expanders as shown in figure C-3. The extended gate has no connection through the common collector resistor to +4 vdc. Instead, the output from the extended gate is connected to the output line from the other gate (figure C-4). The collector resistor of this gate is now common to the transistors in both gates. This configuration does not change the logic ability of the gates. A logic ONE at any one or all of the six inputs results in a logic ZERO out. A logic ZERO at all six inputs results in a logic ONE out.

A NOR gate flip-flop consists of two NOR gates interconnected, as shown on figure C-5. The flip-flop is set by a logic ONE applied to the set input and is reset by a logic ONE applied to the reset input. The set pulse actually is applied to the reset side of the flip-flop; likewise the reset pulse is applied to the set side. This condition exists because of the characteristics of the NOR gate (a logic ONE at any input results in a logic ZERO out). The logic ZERO is applied to the input of the opposite side and holds that side off, which results in a logic ONE out. Thus, a set pulse applied to gate A of figure C-5 turns the gate on. The output of gate A (or the reset side) is a logic ZERO, which is applied to gate B and holds this gate off. The output of gate B (the set side) is a logic ONE.

The format used for each of the logic diagrams contained in the discussions in this manual is illustrated and explained on figure C-6.

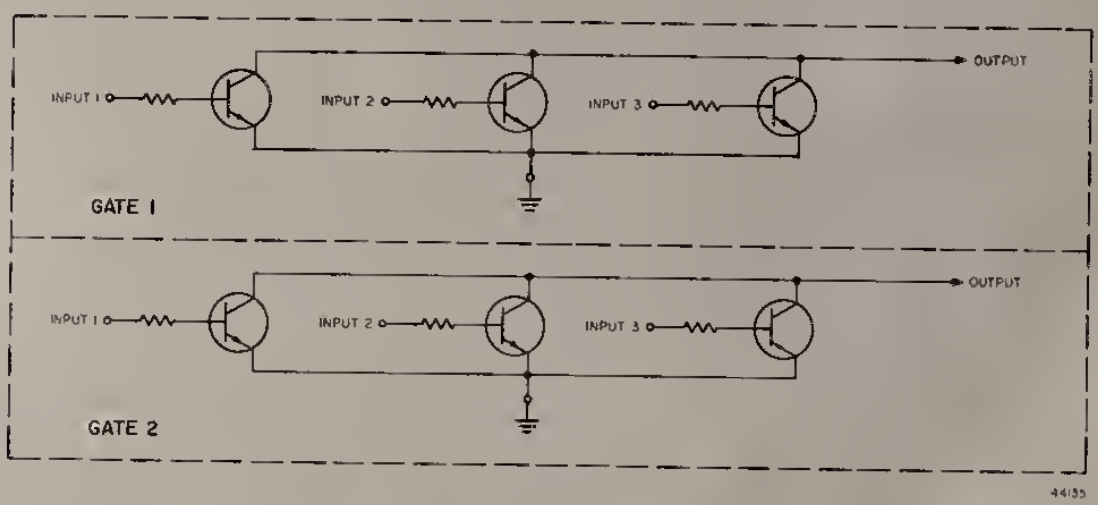
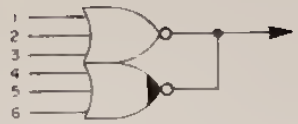


Figure C-3. Dual NOR Gate Expander



EXTENDED NOR GATE SYMBOL

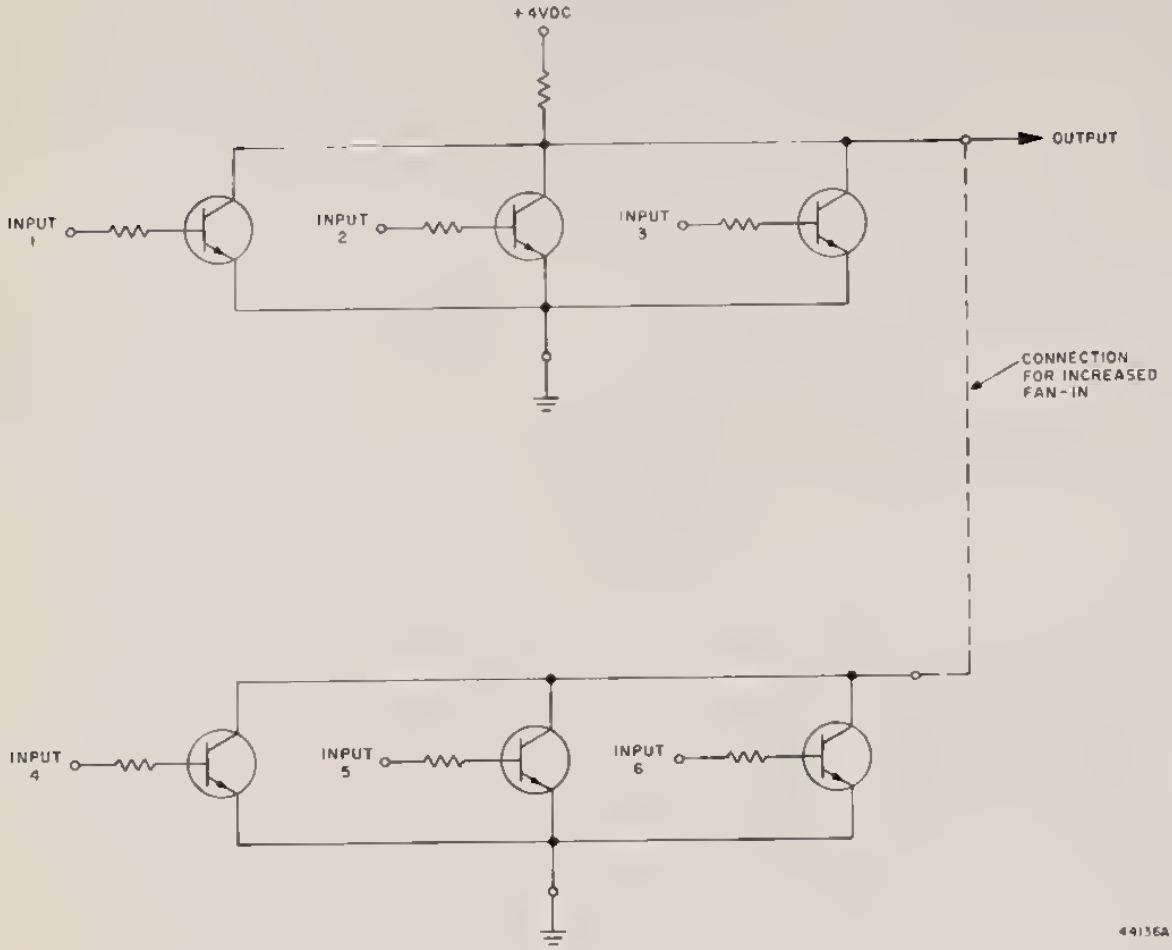
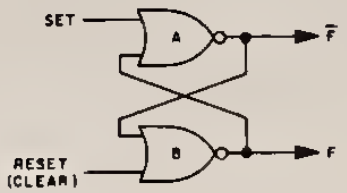
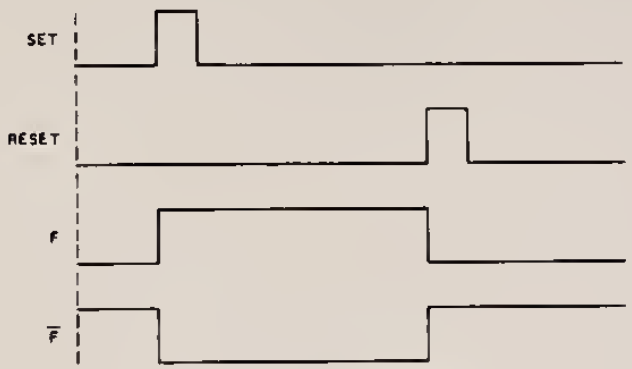


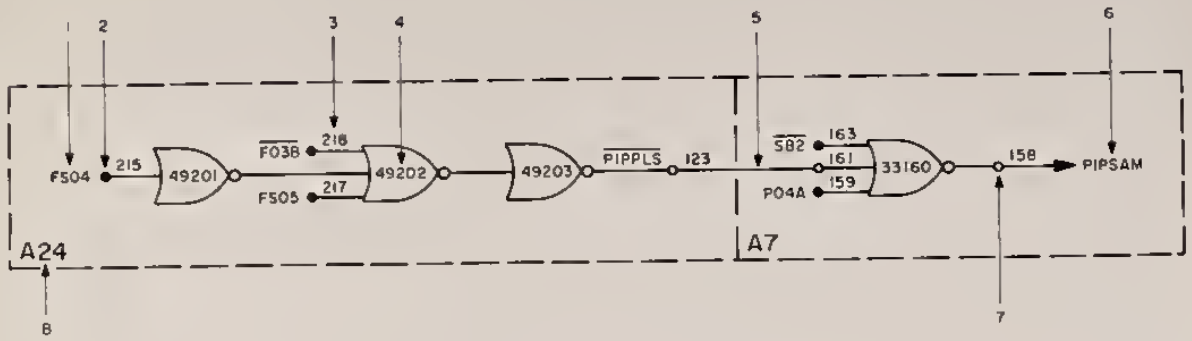
Figure C-4. Extended NOR Gate

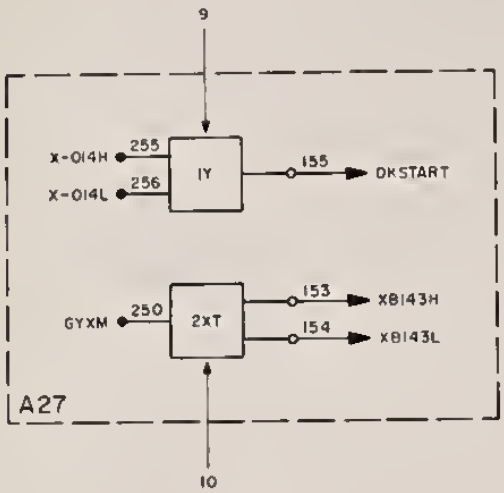




FLIP-FLOP WAVEFORMS 40624

Figure C-5. NOR Gate Flip-Flop





KEY	
INDEX NUMBER	FUNCTION
1	INPUT SIGNAL
2	MODULE INPUT TERMINAL
3	MODULE INPUT TERMINAL NUMBER
4	CIRCUIT NUMBER
5	CONNECTION BETWEEN TERMINALS
6	OUTPUT SIGNAL
7	MODULE OUTPUT TERMINAL
8	TRAY-MODULE DESIGNATION (LETTER DESIGNATES TRAY, NUMERAL DESIGNATES MODULE LOCATION)
9	INPUT INTERFACE CIRCUIT
10	OUTPUT INTERFACE CIRCUIT

44136

Figure C-6. Logic Diagram Symbols