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5/20/64

APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 10

FIXED MEMORY

FR-2-110

14 February 1964

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AGC INFORMATION SERIES

ISSUE 10

FIXED MEMORY

FR-2-110

10-1. INTRODUCTION

10-2. This is the tenth issue of the AGCIS, which is published to inform members of the technical staff at MIT/IL and Raytheon about the Apollo Guidance Computer. This issue is a description of Fixed Memory. Information pertaining to this issue was taken from NASA drawings 1006099, 1006119, 1006144, 1006147, 1006148, 1006541, 1006544, 1006553, and 1006559 and AGC-4 interconnection wirelist drawing 1006601 (revision E).

10-3. Fixed (F) Memory is a random access (within a bank), permanent storage device consisting of magnetic cores arranged in three core ropes. A core rope is a unique storage device in which the information stored is determined by the wiring of the cores. The three core ropes (R, S, and T) are capable of storing a total of 24,576 words. Fixed Memory is addressed by means of registers S and BNK and various selection circuits. Data are read out of F memory and supplied to register G by way of sixteen sense amplifiers (SAF of figure 1-11).

10-4. MAGNETIC CORE AND CORE ROPE

10-5. The characteristics of the magnetic core used in the Fixed Memory are similar to the ferrite core used in the Erasable Memory (paragraph 4-6). However, the rope core differs from the ferrite core in that it is fabricated from 1/8-mil Mo-perm ribbon wound on a steel bobbin. Use of the Mo-perm ribbon allows the size of the Fixed Memory core to

be large (core diameter is approximately 0.25 inch compared with 0.05 inch of the Erasable Memory core) without requiring large drive currents, as would be the case if ferrite were used. The larger size is needed to accommodate the number of wires required to thread the rope core (a maximum of 144 wires is needed compared with 4 wires in the ferrite core). Each rope core is threaded by set, reset, inhibit, and sense lines.

10-6. The core interrogation process in Fixed Memory may be divided into set time and reset time (figure 10-1). During set time both the set and inhibit lines carry current. Since the currents in the set and inhibit lines are of opposite polarity, the set current is cancelled by the inhibit current. Therefore, a core changes state at set time if none of the inhibit lines threading the core is carrying current. During reset time the switched core is returned to its normal state by current on the reset line.

10-7. The hysteresis characteristics of a typical rope core are shown in figure 10-2. If the core is in the normal state, an unopposed set current causes an excursion along the hysteresis curve from A to B. Removal of the set current results in an excursion from B to C. The reset current then causes an excursion from C to D, and removal of the reset

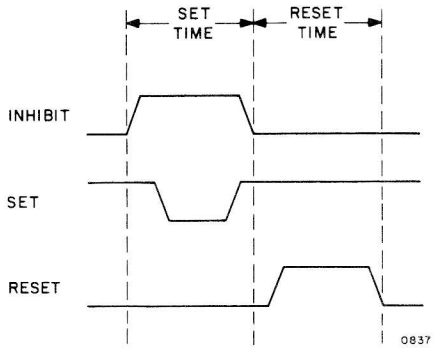

Figure 10-1. Set and Reset Time

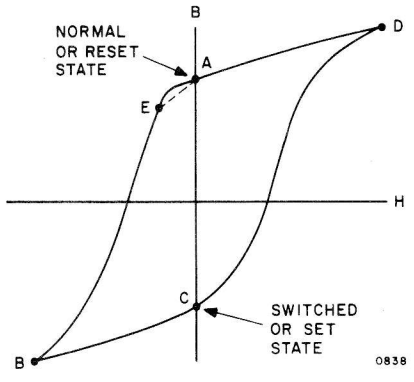

Figure 10-2. Rope Core Hysteresis Characteristics

current results in the core returning to the normal state. If at set time a core also receives an inhibit current, the core excursion is from A to E since the inhibit current is 175 ma as opposed to a set current of 400 ma. This small excursion results in noise on the sense lines. The problem is solved by adding another inhibit winding, called the inhibit parity winding. Thus each core to be inhibited receives at least two inhibit currents, and an excursion to the left of the B axis is avoided. The net result is a reduction of noise on the sense lines. A power savings is also realized with the parity inhibit winding since the individual inhibit currents can be less than the set current.

10-8. One hundred twenty-eight sense lines thread or bypass each core, which enables a core to store eight 16-bit words. When a core is set, current is induced into all the sense lines threading the core. The sense lines bypassing the core receive no current. In this manner the sense lines associated with each core receive the same words each time the core is set.

10-9. The various lines in a core rope are threaded through the cores in a way similar to that shown in figure 10-3. This figure represents a simplified four-address fixed memory in which each core represents an address containing one 2-bit word. To select address 00 (core 1), inhibit lines $\overline{1}$ and $\overline{2}$ must carry current. Since neither of these two inhibit lines threads core 1 and at least one line threads each of the remaining cores, core 1 is the only core which can be switched at set time. Switching core 1 induces current on sense lines A and B since both of these lines thread the core. Therefore, the contents of address 00 are 11. If address 01 (core 2) is selected, the data read out are 01, assuming sense line A detects the low-order bit.

10-10. The threading of a typical rope is shown in figure 10-4. The

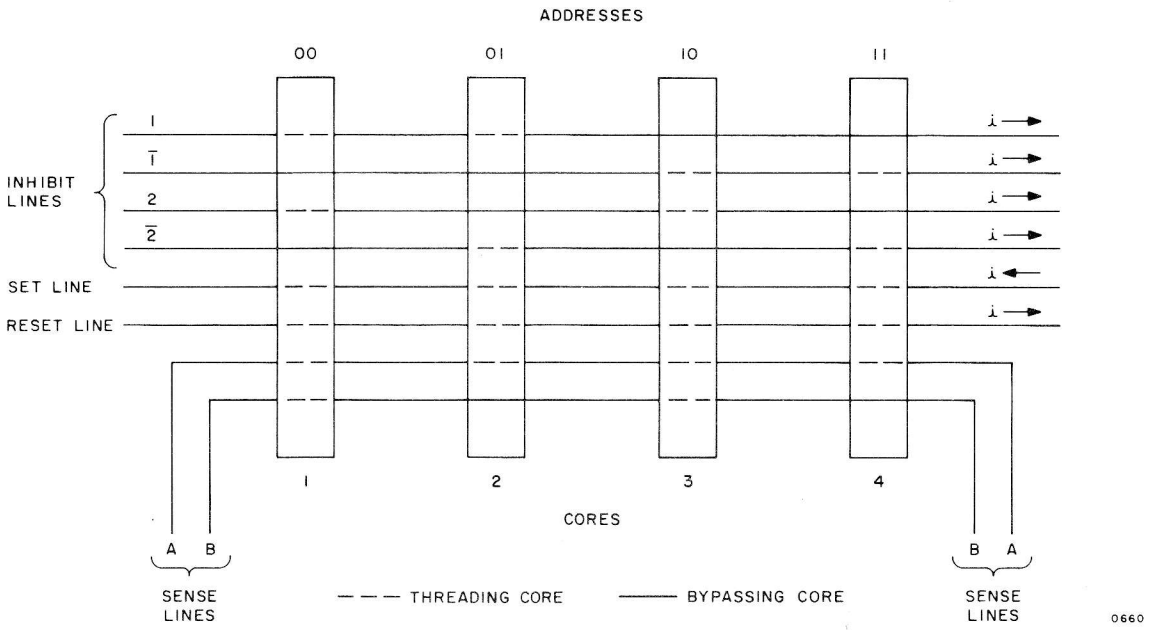

Figure 10-3. Simplified Core Rope Memory

vertical lines represent the eight 128-core sections. Set, reset, inhibit, and sense lines thread the cores of each section, as indicated by the cross-hatch marks on the figure. The cross-hatch marks also indicate current polarity: slant to the right for inhibit polarity and to the left for set polarity. Current in the sense lines can be of either polarity. Inhibit signals IL01 through IL07 and their complements are sufficient to select one core in a section. A core is selected by inhibiting all cores in a section but one. Inhibit signals ILP and $\overline{\text{ILP}}$ ensure that all but the selected core are inhibited by at least two signals to reduce noise in the sense lines.

10-11. Four set lines thread through each rope, and each set line threads two sections. Set C threads sections 1 and 5, set D threads sections 2 and 6, set A threads sections 3 and 7, and set B threads sections 4 and 8. Only one set signal is present at set time and that signal is selected by address.

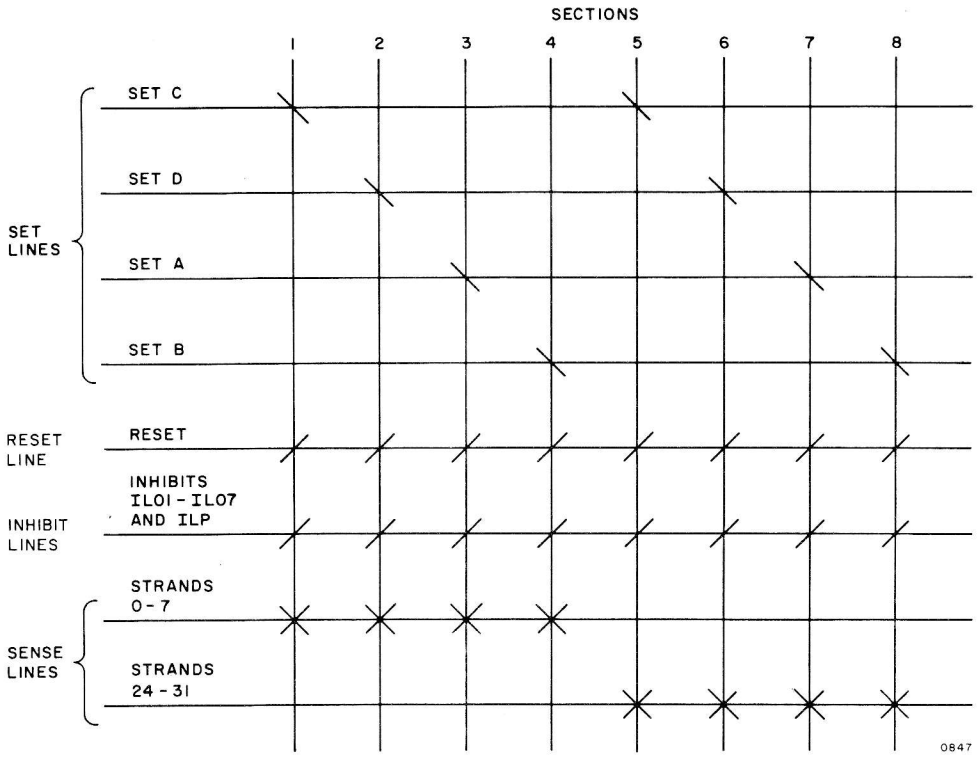

Figure 10-4. Rope Organization

10-12. The sense lines threading each core are grouped together into strands. A strand consists of 16 sense lines (one per bit), and there are 16 strands per rope, for a total of 48 strands in Fixed Memory. The strands are threaded through a rope such that eight strands thread only four sections of a rope, and these are common to the four set lines. For example, strands 0 through 7 are common to the set lines of sections 1 through 4 of rope R. Similarly, strands 24 through 31 are common to the set lines of sections 5 through 8. If the set C line is enabled, the addressed core in sections 1 and 5 of the rope switches, which induces current into the 16 strands threading the rope. A strand-selection technique determines which of the strands supplies data to be read out of Fixed Memory.

10-13. SELECTION STEERING

10-14. Four techniques are required to select one word from Fixed Memory. These techniques are as follows:

1. Rope Selection — Selection of 1 of the 3 core ropes R, S, or T (selecting 8192 words out of 24,576 words).
2. Set Selection — Selection of 2 out of 8 sections in the selected core rope (selecting 2048 words out of 8192 words).
3. Inhibit Selection — Selection of one core out of 128 cores (selecting 64 words out of 8192 words).
4. Strand Selection — Selection of 1 sense strand out of 16 sense strands (selecting 512 words out of 4096 words).

These four techniques are "AND'ed" in such a way to provide the selection of 1 word out of 24,576 words.

10-15. As previously discussed, Fixed Memory is composed of three core ropes. The drive lines (set, reset, and inhibit) threading the ropes are connected in parallel but return to three separate sets of rope return circuits. Consider the inhibit signal IL01; the three drive lines carrying IL01 (one per rope) are connected together at a common driver circuit but return at the other ends of the respective ropes to three different rope return circuits. Thus a particular rope can be selected by enabling the appropriate rope return circuit.

10-16. Each rope is divided into two modules, and each module is further divided into four sections. As shown in figure 10-4, each section is threaded by one set line. A set line threads a section in one module of a particular rope and also threads another section in the second module of the same rope. Thus by enabling one of the four set lines, two of the eight sections in a selected rope are selected by the enabled set line.

10-17. The inhibit lines select one core in each of the sections. Therefore the inhibit lines allow eight cores (one per section) in a selected rope to be set or switched. Since the set-selection technique allows only two sections to be enabled, then only two cores are switched, one in each of the selected sections. The number of inhibit lines (N) necessary to select one of 128 cores is found from the equation, $128 = 2^{N/2}$. Thus N, the number of inhibit lines required, is 14. The inhibit signals on these lines are labeled IL01 and $\overline{\text{IL01}}$ through IL07 and $\overline{\text{IL07}}$. The parity inhibit signals are labeled ILP and $\overline{\text{ILP}}$, but these are not needed for selection.

10-18. Each rope module, consisting of four sections, has separate sense lines. By enabling the sense lines in one particular module, a selection is made between the two cores set by the previous selection techniques. Since each core contains eight 16-bit words, a further selection is required to select one of the eight words. This final selection is accomplished by enabling only one of the strands (16 sense lines) threading the selected core. The outputs of the selected strand are detected and amplified by 16 sense amplifiers.

10-19. ADDRESSING

10-20. A word in Fixed Memory is addressed according to the contents of registers BNK and S. The contents of register BNK determine which rope return circuit is operated. The contents of register S determine which set, inhibit, and strand circuits are operated. Bits 12 and 11 of register S determine if Fixed-Fixed Memory or Fixed-Switchable Memory is addressed (paragraph 1-58). Bits 10 and 9 of register S and the bank address select one of 48 strands; bit 8 of register S and the bank address select the set signals; and bits 7 through 1 of register S select a particular core.

10-21. Register BNK (figure 10-5) is an addressable flip-flop register (address 0015) which consists of 5 bit positions (bits 11 through 15, table 1-6). The register is cleared by signal CBKG before data on the write line are entered into it. Signal CBKG is produced by the bank clear gates when location 0015 is addressed and control pulse $\overline{\text{WSC12}}$ is generated by the Central Processor. Signals $\overline{\text{WL11}}$ through $\overline{\text{WL14}}$ and $\overline{\text{WL16}}$ from the write amplifiers set the appropriate bit positions of register BNK (table 1-6). If a write line is carrying a logical ONE, the bank write gate associated with that bit is enabled by address 0015 and control pulse $\overline{\text{WSC234}}$, and the data are entered into register BNK. If an input bit is a ZERO, the associated bit position in register BNK remains cleared. The outputs of register BNK are labeled R0 through R4, R0 being the highest-order bit. These outputs are applied to the bank read gates and to the bank selector. When the bank read gates are enabled by address 0015 and control pulse $\overline{\text{RSC234}}$, the contents of register BNK are supplied to the Central Processor by the read gates.

10-22. The bank selector senses the state of R0 through R4 of register BNK and bits 12 and 11 of register S, and produces outputs subject to the timing of signal $\overline{\text{RGENV}}$. Signal $\overline{\text{RGENV}}$ and all timing signals pertaining to Fixed Memory are illustrated in figure 5-3. The bank selector produces signals RPG1 through RPG6, which are applied to the rope selector. Signals RPG1 through RPG6 are amplified and then sent to the strand selector as signals GTRS, GTSS, GTTS, GTUS, GTVS, and GTWS, respectively. The rope selector also produces the following signals for energizing the return circuit for ropes R, S, and T:

a. GATER for RPG1 or RPG4
b. GATES for RPG2 or RPG5
c. GATET for RPG3 or RPG6.

The bank selector also produces signal $\overline{\text{IL09A}}$, which is sent to the set selector, and signals IL10A and $\overline{\text{IL10A}}$, which are sent to the strand gates.

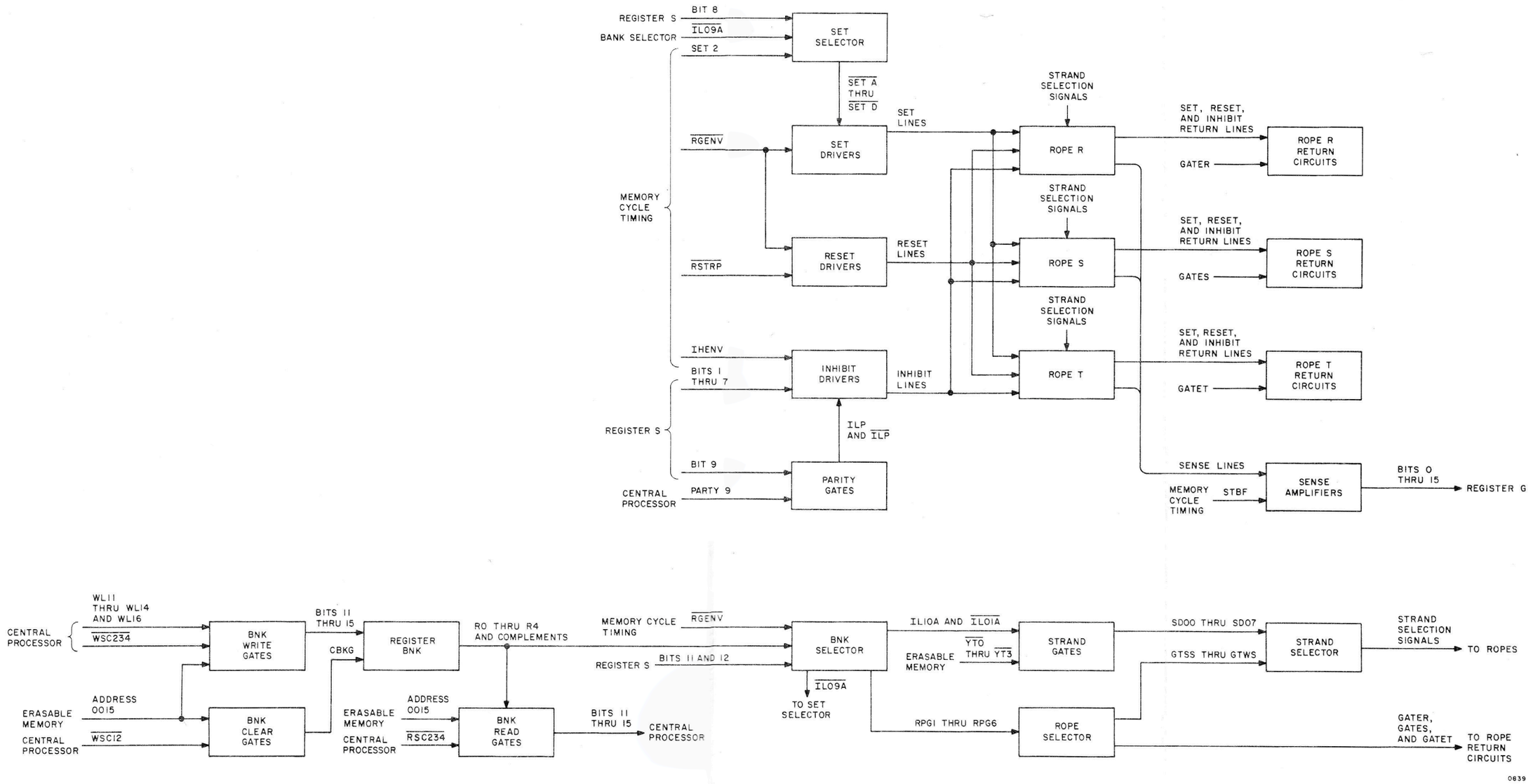

Figure 10-5. Fixed Memory

The relationships between the inputs and outputs of the bank selector and the selected bank are shown in table 10-1.

10-23. The set selector gates bit 8 of register S with signal $\overline{\text{IL09A}}$ during SET 2 time (figure 5-3). Signal $\overline{\text{IL09A}}$ is a logical ONE for signals $\overline{\text{SETA}}$ and $\overline{\text{SETB}}$ and a logical ZERO for signals $\overline{\text{SETC}}$ and $\overline{\text{SETD}}$. Bit 8 is a logical ZERO for signals $\overline{\text{SETA}}$ and $\overline{\text{SETC}}$ and a logical ONE for signals $\overline{\text{SETB}}$ and $\overline{\text{SETD}}$. Thus the four set signals are generated as the result of four possible combinations of bit 8 and signal $\overline{\text{IL09A}}$. The set signals are applied to the set lines via the set drivers.

10-24. The inhibit drivers receive bits 7 through 1 of register S. These bits are gated by signal IHENV and are sent to the three ropes via the inhibit lines. The parity inhibit signal (ILP) also is applied to the inhibit drivers. Signal ILP is produced by signal PARTY 9 from the Parity Block and bit 9 from register S. In the Parity Block (figure 10-6) signal PARTY 9 is produced from a combination of the nine low-order bits. The resultant signals are designated A through C and their complements (figure 3-11). Signal PARTY 9, representing odd parity of the nine low-order bits, is gated with bit 9 of register S. This action produces signal ILP, which ensures that each core receives

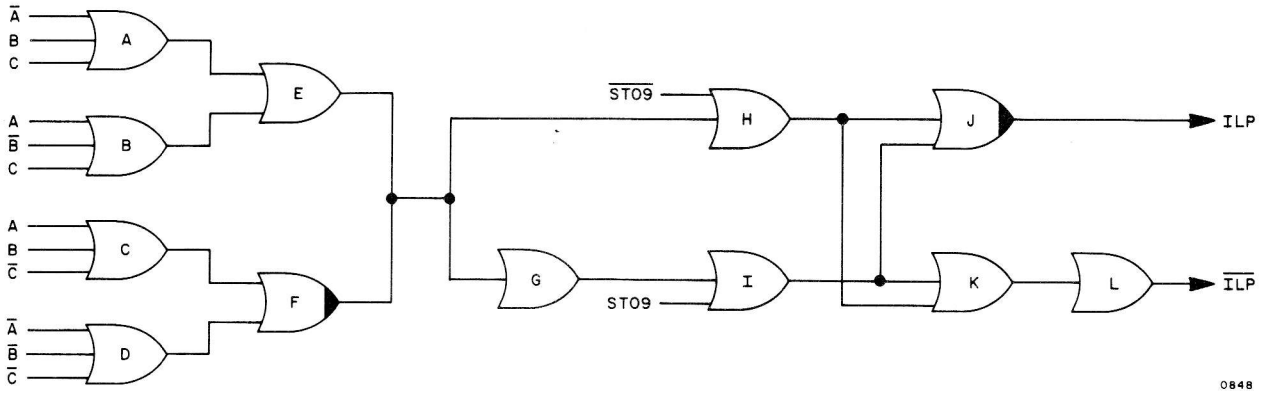

Figure 10-6. Parity Block and Inhibit Parity Gates

TABLE 10-1

BANK SELECTION

Register BNK					Register S		Inhibit Signals		Rope Control Signal	Bank
Input Bits										
15	14	13	12	11						
Output Signals					Bits					
R0	R1	R2	R3	R4	12	11	IL09	IL10		
x	x	x	x	x	0	1	1	0	RPG1	01
x	x	x	x	x	1	0	0	1	RPG1	02
0	0	0	x	x	1	1	1	1	RPG1	03
0	0	1	0	0	1	1	0	0	RPG1	04
0	0	1	0	1	1	1	1	0	RPG2	05
0	0	1	1	0	1	1	0	1	RPG2	06
0	0	1	1	1	1	1	1	1	RPG2	07
0	1	0	0	0	1	1	0	0	RPG2	10
0	1	0	0	1	1	1	1	0	RPG3	11
0	1	0	1	0	1	1	0	1	RPG3	12
0	1	0	1	1	1	1	1	1	RPG3	13
0	1	1	0	0	1	1	0	0	RPG3	14
1	0	0	0	1	1	1	1	0	RPG4	21
1	0	0	1	0	1	1	0	1	RPG4	22
1	0	0	1	1	1	1	1	1	RPG4	23
1	0	1	0	0	1	1	0	0	RPG4	24
1	0	1	0	1	1	1	1	0	RPG5	25
1	0	1	1	0	1	1	0	1	RPG5	26
1	0	1	1	1	1	1	1	1	RPG5	27
1	1	0	0	0	1	1	0	0	RPG5	30
1	1	0	0	1	1	1	1	0	RPG6	31
1	1	0	1	0	1	1	0	1	RPG6	32
1	1	0	1	1	1	1	1	1	RPG6	33
1	1	1	0	0	1	1	0	0	RPG6	34

x means 0 or 1.

two or more inhibit currents to prevent noise in the sense lines. The output from the parity gates is sent to the inhibit drivers, where it is gated by signal IHENV and sent to the ropes via the inhibit lines.

10-25. Signals IL10A and $\overline{\text{IL10A}}$ are gated with signals $\overline{\text{YT0}}$ through $\overline{\text{YT3}}$ to produce signals SD00 through SD07, which are sent to the strand selector. Signals SD00 through SD07 and signals GTRS through GTWS are then decoded by the strand selector to produce a strand-select signal. The strand-select signals SDR00 through SDR47 are applied to the ropes to enable the proper sense lines. The sense amplifiers detect the contents of the selected address and supply the data word (bits 0 through 15) to register G subject to sense strobe STBF. At reset time the reset drivers reset the cores to the normal state with the application of signals $\overline{\text{RSTRP}}$ and $\overline{\text{RGENV}}$.

10-26. DRIVERS AND AMPLIFIERS

10-27. As previously discussed, the set, reset, and inhibit lines threading a rope are connected in parallel but return to three sets of return circuits (figure 10-7). Each line is driven by a separate driver circuit, and all those lines common to a particular rope are returned to an associated return circuit. There are 4 set drivers, 2 reset drivers, and 16 inhibit drivers. The set and reset drivers are enabled subject to memory cycle timing signals RGENVX and IHENV. The application of these two signals to their respective gates supplies +13 vdc to the various drivers. Signal RGENVX supplies +13 vdc to the set and reset drivers; signal IHENV supplies +13 vdc to the inhibit drivers. In addition, signals GATER, GATES, and GATET from the rope selector enable the proper set of rope return circuits.

10-28. When signal GATER, GATES, or GATET is a logical ZERO, the

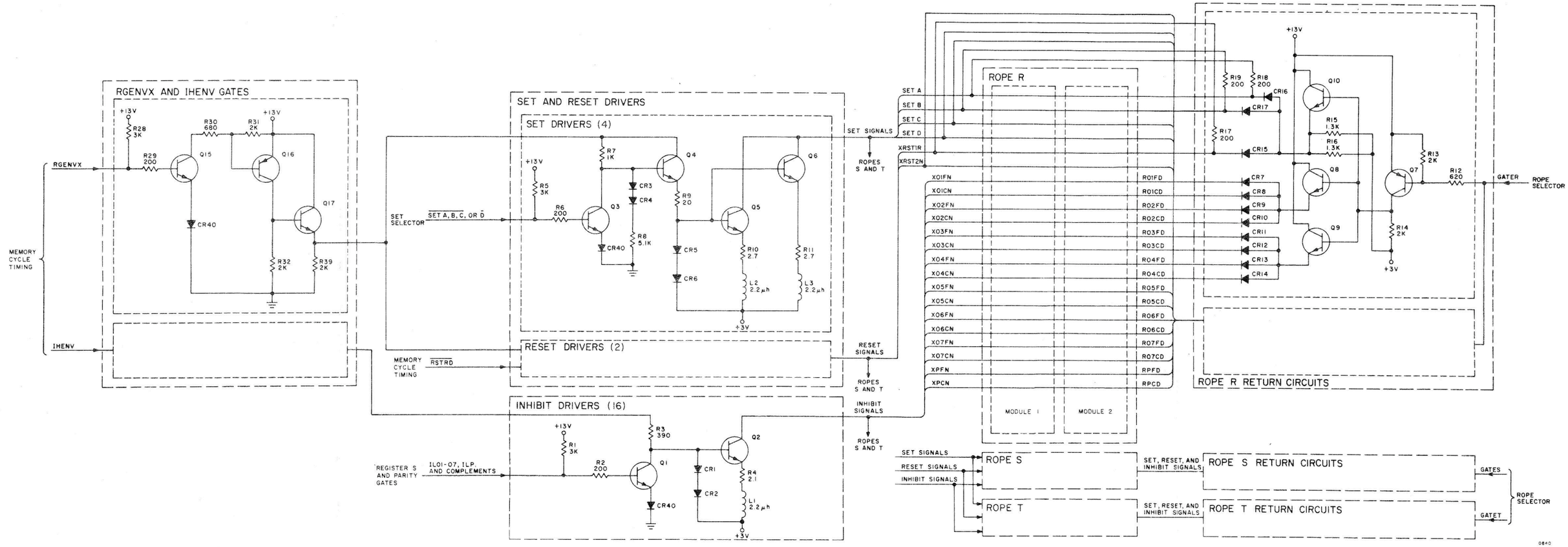

Figure 10-7. Drivers and Return Circuits

rope return circuits controlled by these signals are enabled. In this manner +13 vdc are applied to the right side of the drive lines threading the selected rope. Each return circuit services two set, one reset, and eight inhibit lines. Application of a set signal enables the selected set driver. This provides a current path from +13 vdc through Q10, the rope, Q5, and Q6 to ground. Simultaneously two or more inhibit signals are applied to the inhibit drivers, and a current path exists from +13 vdc through Q8 and Q9, the rope and Q2 to ground. Since the set and inhibit currents are opposite in polarity and therefore cancel each other, only those cores that receive a set current and no inhibit currents are switched.

10-29. At reset time the reset drivers are enabled by signal $\overline{\text{RSTRP}}$. The reset drivers function in the same way as the set drivers and provide a current path from +13 vdc to ground through the selected rope. The reset current switches all the cores to the reset (normal) state.

10-30. Since there are a total of 48 sense strands in Fixed Memory and eight strands thread each rope module (half of a rope), a selection system is required to select the proper half of the rope and strand to read out data. This selection process is performed by the rope and strand selector circuits (figure 10-8). There are three identical rope selector circuits, and each circuit receives two RPG signals. However, only one signal is present at a time. In addition, there are eight strand selector circuits, each consisting of six gates. A single strand selector receives one of eight SD signals from the strand gates and one of six GT signals from the rope selectors. This 6-by-8 combination selects the proper sense strand from among 48 possibilities. For simplification only one rope selector circuit and one strand selector circuit are discussed.

10-31. Assume RPG6 to be a logical ONE. Transistors Q2 and Q4 conduct, which results in the +13-vdc signal GTWS being applied to CR6 in

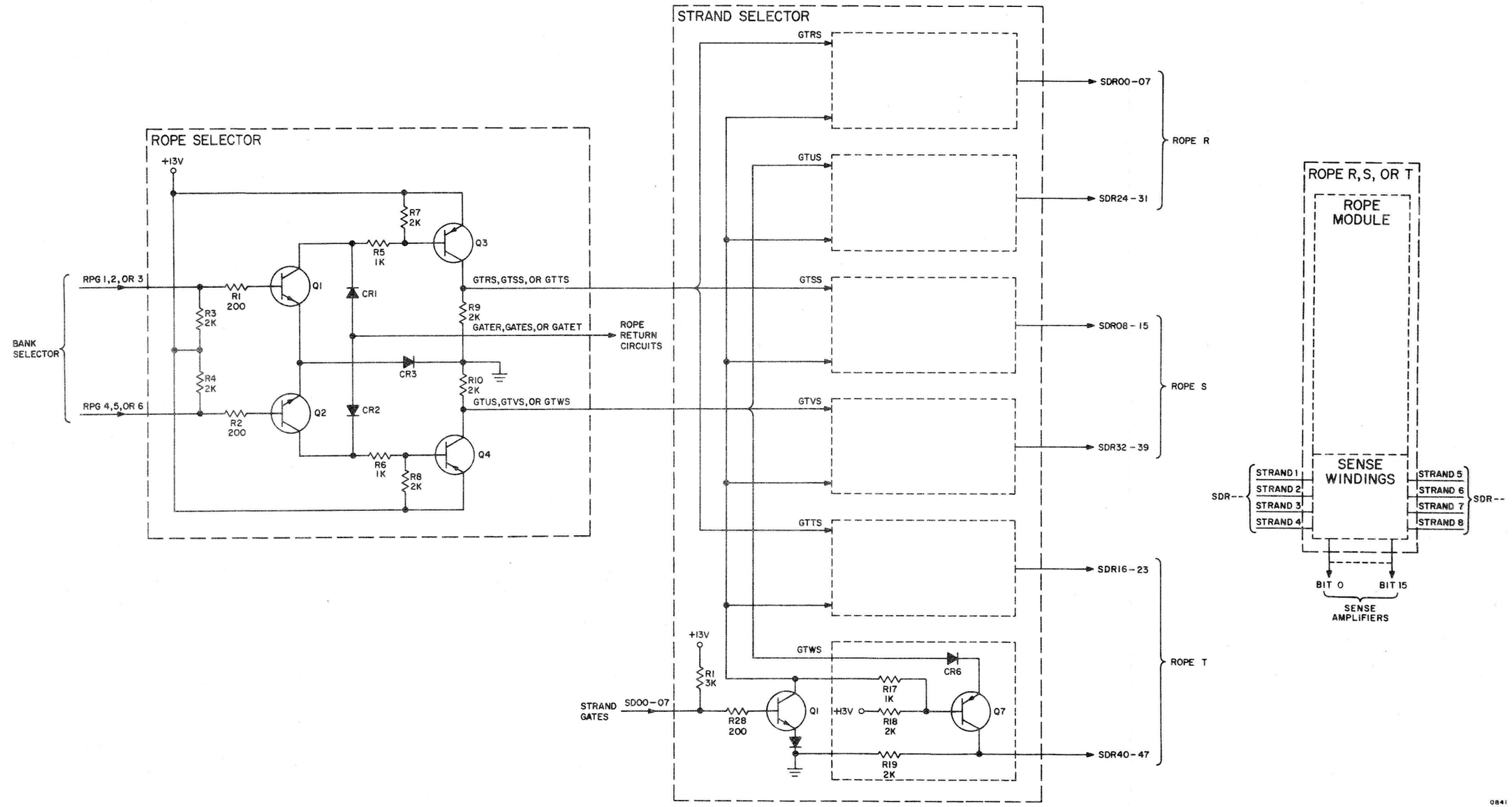

Figure 10-8. Rope and Strand Selectors

TABLE 10-2

ROPE- AND STRAND-SELECT SIGNALS

Rope Control	Rope Return	Strand Gate	Sense Strand
RPG1	GATER	SD00 through SD07	SDR00 through SDR07
RPG2	GATES	SD00 through SD07	SDR08 through SDR15
RPG3	GATET	SD00 through SD07	SDR16 through SDR23
RPG4	GATER	SD00 through SD07	SDR24 through SDR31
RPG5	GATES	SD00 through SD07	SDR32 through SDR39
RPG6	GATET	SD00 through SD07	SDR40 through SDR47

the strand selector. In addition, diode CR2 in the rope selector is forward-biased, which enables the rope T return circuits via signal GATET. Thus one rope return circuit is enabled and eight gates (one per strand selector) are conditioned to be enabled. The application of a strand gate signal determines which of the eight gates is enabled. If signal SD00 is a logical ONE, transistors Q1 and Q7 in the strand selector conduct and sense strand SDR40 is selected. The manner in which the 48 strand-select signals are produced as a result of combining the RPG and SD signals is shown in table 10-2.

10-32. Sixteen sense amplifiers are associated with Fixed Memory.

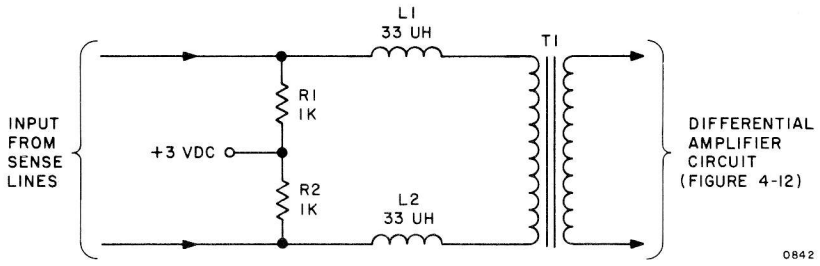

Figure 10-9. Sense Amplifier Input Circuit

These amplifiers operate similarly to those in Erasable Memory (paragraph 4-26). The difference occurs in the input circuit (figure 10-9). The inputs to transformer T1 are returned to +3 vdc through resistors R1 and R2 to provide a return path for the strand selector gates. Inductors L1 and L2 filter out noise picked up on the sense lines.