# AGC INFORMATION SERIES
# ERRATA SHEET 32-1
# 25 March 1966

1. Remove title page and insert new title page attached.
2. Remove pages 32-153/32-154 and insert new pages 32-153/32-154.
3. Remove pages 32-179/32-180 and insert new pages 32-179/32-180.
4. Remove pages 32-181/32-182 and insert new pages 32-181/32-182.

APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 32

# BLOCK II MACHINE INSTRUCTIONS

FR-2-132

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(3) Set c(Z) = b(Z)+1 = I+2.
(4) Restore c(I+1) = b(I+1) if (I+1) represents an address in E Memory.

Point (2) implies that instruction j is executed next.

32-222. Special Cases of READ H:

a. READ L and READ Q enter all sixteen bits of c(L) or c(Q) into A.

b. READ 003 and READ 004 enter fourteen bits of c(SCALER2) or c(SCALER1) into A.

c. Instructions READ H with $005 \leq H \leq 033$ follow the rules of paragraph 32-221.

d. Channels 034 and 035 (downlink channels) cannot be read by a Channel Instruction, therefore 000000 is entered into A.

32-223. When instruction READ H is executed, the quantity from channel H is entered into register B by action 4 of subinstruction READ0 (row 42 of table 30-4), and action 5 transfers the quantity to register A. Action 8 enters the address of the next instruction into register S and subinstruction STD2 calls forward the next instruction as usual.

32-224. Figure 32-48 illustrates the execution of subinstruction READ0 of instruction READ 015, channel 15 containing the quantity 00011, a keycode from the keyboard of the main panel DSKY.

32-225. INSTRUCTION WRITE H

32-226. Instruction WRITE H (Write H) is a Channel Instruction which is represented by order code 10.1 and a 9 bit channel address (table 30-5). Instruction WRITE H must be preceded by Special Instruction EXTEND which enters a ONE into bit position EXT of register SQ. Instruction WRITE H consists of subinstructions WRITE0 and STD2, the execution of which takes two MCT's.

32-227. Instruction WRITE H enters the content of register A into channel H. The operation WRITE H with $005 \leq H \leq 014$, or H is = 34, 35, can be formulated as follows:

(1) Set c(H) = c(A) whereby bit A15 is entered into bit position H15 and bit A15 is not transferred.
Keep c(A).

(2) Set c(B) = c(I+1) = j, I being the address of instruction WRITE H, and j being the instruction stored at location (I+1).
Set c(S) = relevant address of j.
Set c(SQ) = order code of j.
(3) Set c(Z) = b(Z) + 1 = I+2.
(4) Restore c(I+1) = b(I+1) if (I+1) represents an address in E Memory.

Point (2) implies that instruction j is executed next.

32-228. Special Cases of WRITE H

a. WRITE L and WRITE Q enter all sixteen bits of c(A) into L or Q.

b. SCALER2 and SCALER1 cannot be written into by a Channel Instruction.

c. Instruction WRITE H with $005 \leq H \leq 014$ follow the rules of paragraph 32-327.

d. Channels 15 through 33 cannot be written into by a Channel Instruction.

e. WRITE 034 and WRITE 035 enter bits A16, A14 through A1, and a parity bit into channel 034 or 035.

32-229. The execution of instruction WRITE H is similar to that of instruction READ H. (Compare rows 42 and 43 of table 30-4.) Action 5 of subinstruction READ0 transfers the channel information from register B to register A. Action 5 of subinstruction WRITE0 transfers the content of register A to the addressed channel.

32-230. INSTRUCTION RAND H

32-231. Instruction RAND H (Read and AND H) is a Channel Instruction which is represented by order code 10.2 and a 9 bit channel address (table 30-5). Instruction RAND H must be preceded by Special Instruction EXTEND which enters a ONE into bit position EXT of register SQ. Instruction RAND H consists of subinstructions RAND0 and STD2, the execution of which takes two MCT's.

32-232. Instruction RAND H performs the Boolean operation AND (symbol $\wedge$) with the contents of register A and channel H and stores the logical product in A. The truth table for each bit of c(A) and c(H) is shown below.

32-309. INSTRUCTION SHINC C

32-310. Instruction SHINC C (Shift Increment C) is a Counter Instruction which is executed at the occurrence of certain events (paragraph 30-137) without entering an order code into register SQ and is independent of the content of register SQ. Instruction SHINC C consists of subinstruction SHINC, the execution of which takes one MCT.

32-311. Instruction SHINC C shifts one place to the left the content of that serial data counter C in E Memory (location 0045, 0046, 0057, or 0060) the address of which is supplied by the Counter Priority Control. The operation SHINC C can be formulated as follows:

(1) Set c(C) = 2b(C) where b(C) is always a positive quantity and c(C) includes an overflow bit (instead of a sign bit) in bit position 15 in case of overflow.
(2) Retain c(B).
Retain c(S).
Retain c(SQ).
(3) Retain c(Z).

Point (2) implies that the instruction stored in B is executed next.

32-312. Instruction SHINC C is used for serial to parallel conversion. If SHINC 0045 is executed and the flag bit (a ONE) moves into bit position 16 of the Adder, the execution of instruction RUPT is requested. If SHINC 0046, SHINC 0057, or SHINC 0060 is executed, no flag bit is involved.

32-313. When instruction SHINC C is executed, action 1 of subinstruction SHINC (row 58 of table 32-4) enters into register S the counter address C provided by the Counter Priority Control. The content of the addressed counter is transferred to register G at time 4. Action 5 doubles the quantity and enters this doubled quantity into the Adder. Action 7 enters the doubled quantity into register G whereby any overflow bit is entered into bit positions 16 and 15 of G. At time 10 the content of register G is entered into the addressed counter. Action 8 re-enters into register S the relevent address contained in register B to re-establish the original conditions.

32-314. Figure 32-58 illustrates the execution of instruction SHINC 0045. Originally, counter 0045 which contained 05530 before the shifting operation, contains 013260 after the shifting operation. If quantity 25530 were contained originally, 53230 would be contained after shifting and the execution of instruction RUPT would be requested.

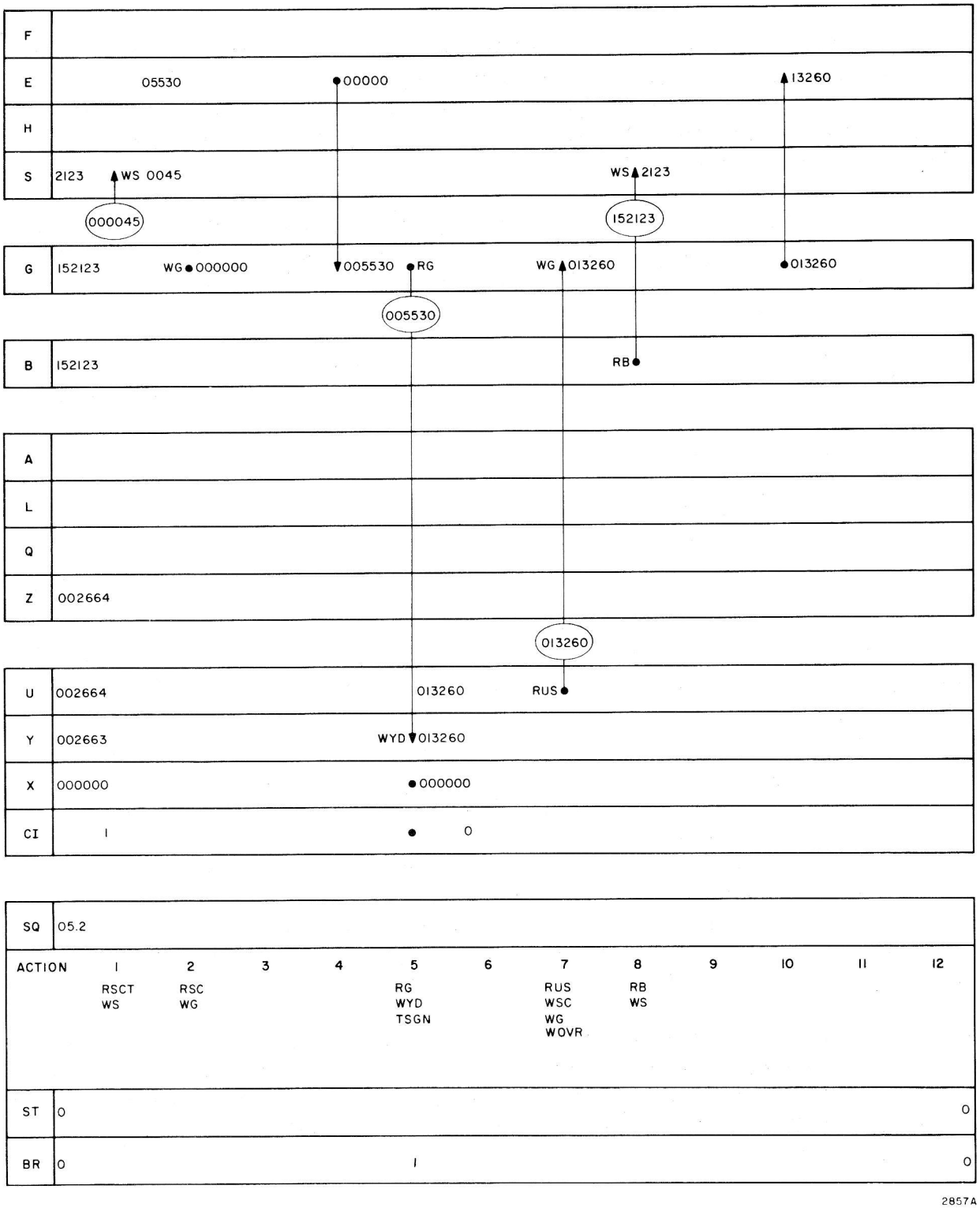


*Figure 32-58. Subinstruction SHINC*

32-315. INSTRUCTION SHANC C

32-316. Instruction SHANC C (Shift and Add Increment C) is a Counter Instruction which is executed at the occurrence of certain events (paragraph 30-137) without entering an order code into register SQ and is independent of the content of register SQ. Instruction SHANC C consists of subinstruction SHANC C, the execution of which takes one MCT.

32-317. Instruction SHINC C shifts one place to the left the content of that serial data counter in E Memory (0045 or 0046) the address of which is supplied by the Counter Priority Control and adds a ONE into bit position 1. The operation SHANC C can be formulated as follows:

(1) Set c(C) = 2b(C)+1 where b(C) is always a positive quantity and c(C) includes an overflow bit (instead of a sign bit) in bit position 15 in case of overflow.
(2) Retain c(B).
Retain c(S).
Retain c(SQ).
(3) Retain c(Z).

Point (2) implies that instruction stored in B is executed next.

32-318. Instruction SHANC C is also used for serial to parallel conversion similarly to instruction SHINC C. (Compare rows 58 and 59 of table 32-4.) Control pulse CI of action 5 adds the ONE into bit position 1 of the Adder; this ONE is later transferred to bit position 1 of the counter. If SHANC 0045 is executed and an overflow occurs, the execution of instruction RUPT is requested.