APOLLO GUIDANCE COMPUTER

Information Series

ISSUE 4

ERASABLE MEMORY

FR-2-104

AGC INFORMATION SERIES

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ISSUE 4

ERASABLE MEMORY

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4-1. INTRODUCTION

4-2. This is the fourth issue of the AGCIS published to inform members of the technical staff at MIT and Raytheon about the AGC and the Apollo G & N system. A brief description of the erasable memory is contained in Issue 1. This issue describes in detail the characteristics and operation of the erasable memory.

4-3. GENERAL

4-4. The erasable memory (E) is a random access (any location may be selected) storage with destructive readout. The E memory is comprised of ferromagnetic cores arranged in a three dimensional array, various selection circuits and sense amplifiers. The E memory is shown as part of the computer in figure 1-11. The core array (represented by a cube) consists of 16 bit planes. Each bit plane contains 1024 cores which are arranged (electrically, not physically) in 32 rows and 32 columns. Each bit plane stores one bit of each word stored in E memory. The x selection (x) serves to select a certain column of cores in all 16 bit planes for readout or write-in, and the y selection (y) serves to select a certain row. Selecting a column and a row simultaneously has the effect of selecting a certain core (the same) in all 16 bit planes. This is equivalent to selecting a certain word or location (consisting of 16 cores or bit positions) in E memory. The sense amplifiers (SAE) read the information out of a selected location, and the z drivers (z) cause information to be written into a selected location. The core array

has a storage capacity of 1024 words, however use is made of only 1008 locations since the first 16 addresses are allocated for flip-flop registers (refer to table 1-4).

4-5. The ferromagnetic core is a static storage element which does not require power to store information. Each bit information (ZERO or ONE) is stored as a direction of flux (plus or minus) in a core. A core remains magnetized in one direction until it is deliberately changed to another direction by application of an electric current. The magnetization characteristic of a core is such that existing magnetization will not be affected by a current of up to (and slightly over) one-half the amplitude of that required to change its direction of magnetization. The ferromagnetic cores are ring-shaped, therefore, magnetic effects from wires passing through the cores are additive. If two wires, passing through a core, are each carrying half the required current, the core magnetization will not be affected unless their currents coincide in direction and time.

4-6. FERRITE CORE AND CORE ARRAY

4-7. The ideal storage element for the E memory should have a hysteresis characteristic of nearly square shape, such as that shown in figure 4-1. Positive current causes magnetization in one direction; negative current causes magnetization in the opposite direction. These two states of magnetization are used to represent a binary ZERO or a binary ONE, respectively. Point A of the characteristic represents the neutral state of magnetic flux of a core. There are two remanent states (levels) representing opposite magnetization of the core; one at point C and one at point F. In order to change the magnetization of the core from level C to F, or vice versa, a current of approximately 600 ma must flow through a core. That is, 600 ma must flow through the core to change its binary state from ZERO to ONE or from ONE to ZERO.

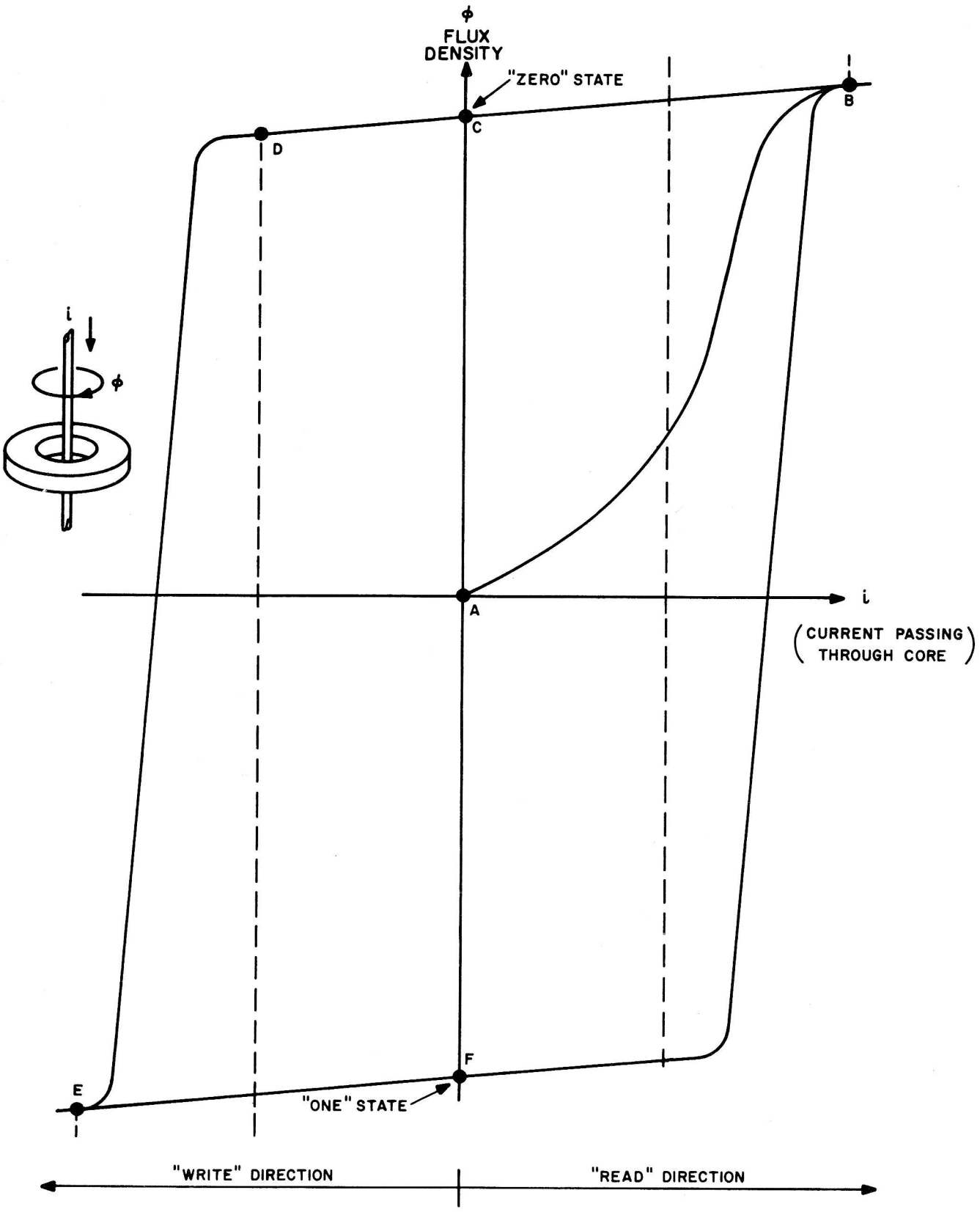

Figure 4-1. Ferrite Core Hysteresis Characteristics

4-8. Each memory core in a bit plane is threaded diagonally by a common sense line and vertically by a common inhibit line, as shown on figure 4-2. Furthermore, each core of the array is threaded by one x and one y selection line as indicated on figure 4-3. Each of the 32 x selection lines pass through all cores in a yz plane, and each of the 32 y selection lines pass through all cores in a xz plane.

4-9. Initially, a current of 600 ma is sufficient to bring a core from its neutral condition (A, figure 4-1) to a saturated condition (B). When the current is removed, the core retains a certain amount of remanent flux or magnetization represented by point C. A slight loss of magnetization occurs at current cutoff, but the amount is insignificant. Reapplication of the positive 600-ma current places the core back to condition B. Continued application of positive 600 ma pulses will cause the condition of the core to shift between points B and C with very little flux change occurring during these shifts. The core will therefore remain in the ZERO state. When a negative 600-ma pulse is applied to a core which is in the ZERO state, its condition changes along curve CDE, and its flux reverses, and the core switches into the ONE state (opposite saturation). This rapid reversal of the magnetic state causes a large flux change and induces a current in the sense line passing through the core. After this pulse the condition of the core shifts from point E to point F. When a negative pulse of approximately 300 ma is applied while the core is in the ZERO state, the condition of the core shifts to point D but not further. After this pulse, the core returns to condition C; a 300-ma pulse is not sufficient to change the state of a core. As the condition changes from point C to D, a comparatively small current is induced into the sense line which has no further effect. Switching a core from the ONE state into the ZERO state occurs in a similar way. Summarizing, a 600-ma pulse is required to switch a core from one state into the other. A negative 600-ma pulse switches the core into

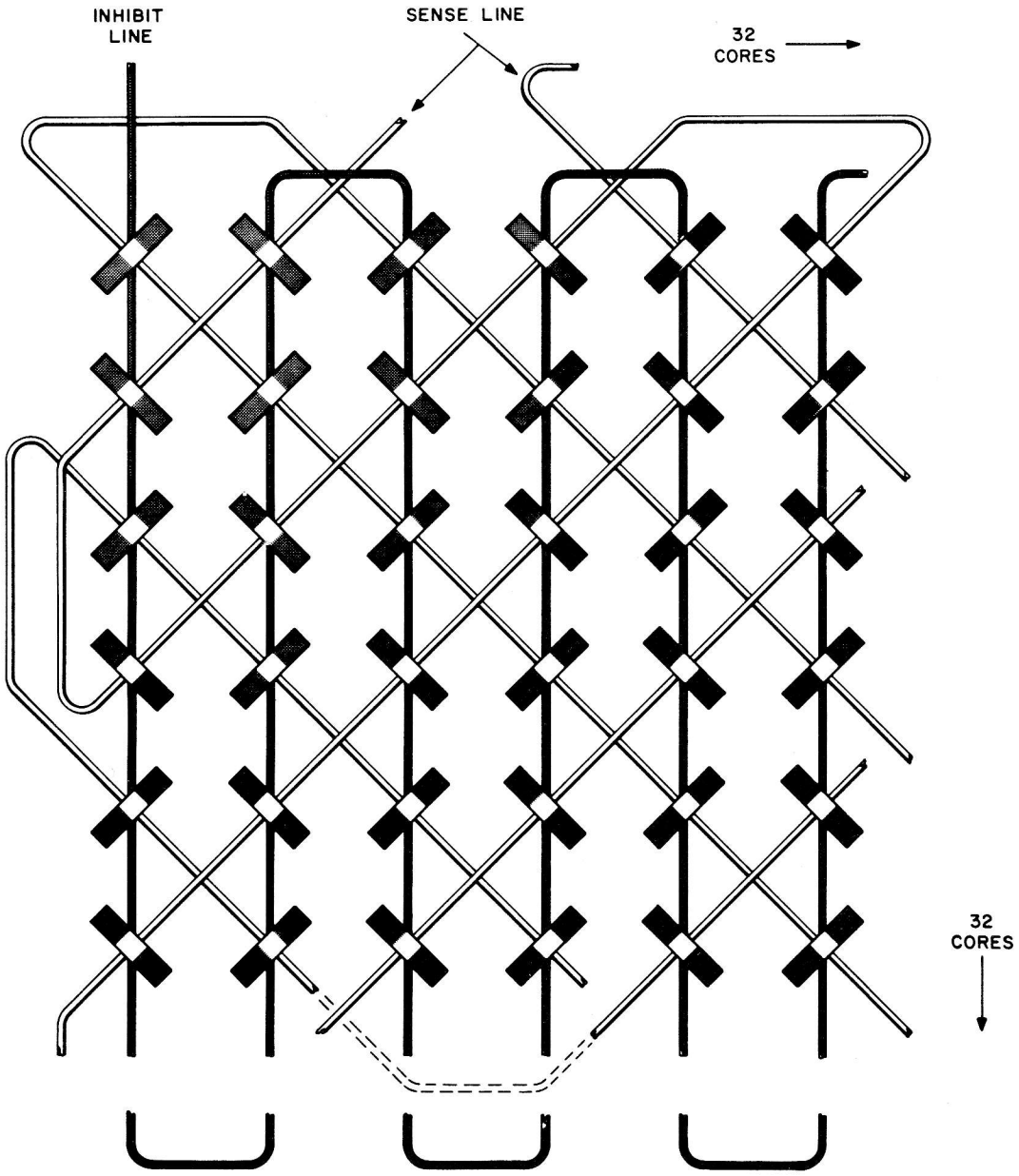

Figure 4-2. Bit Plane

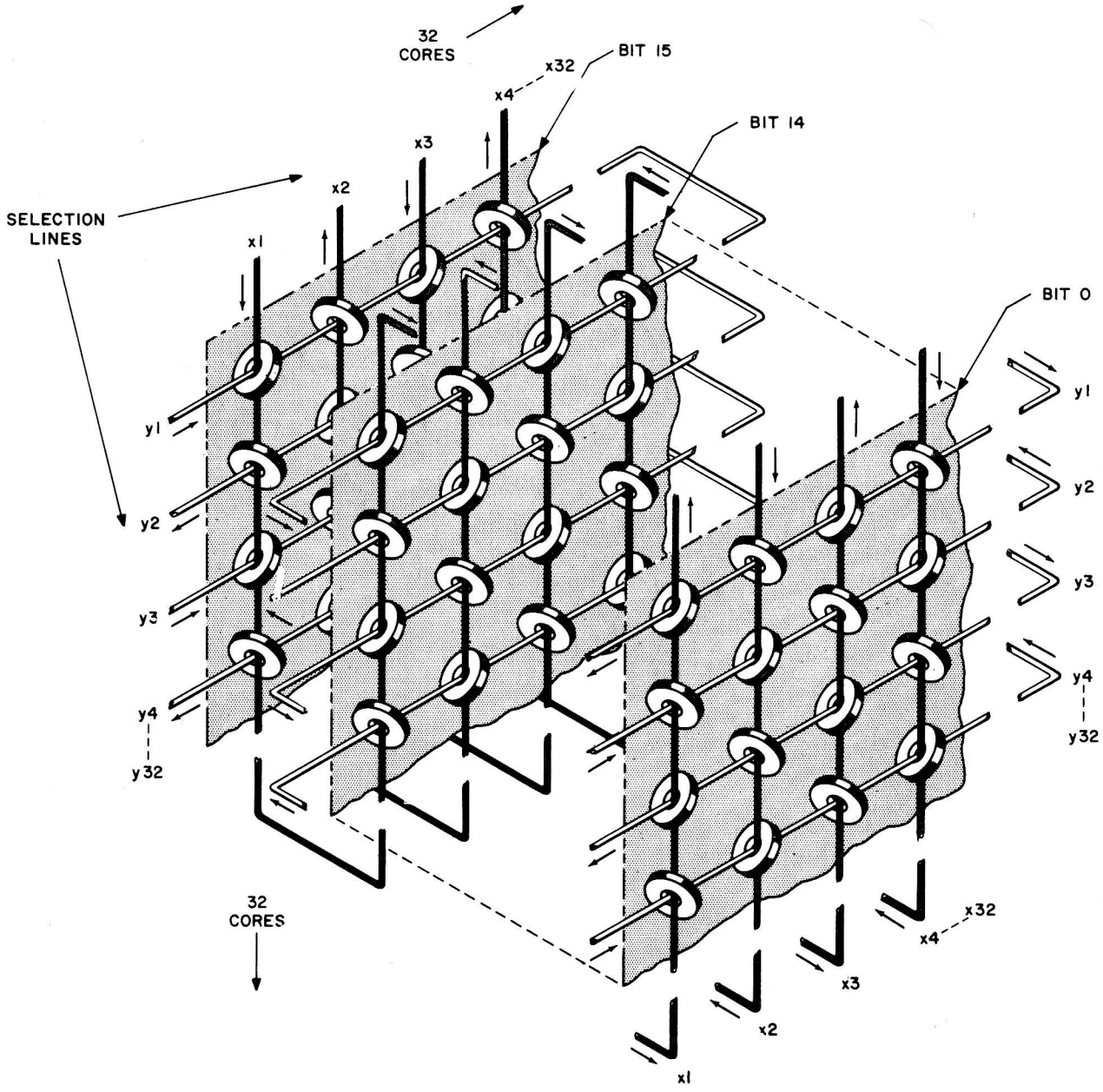

Figure 4-3. Core Array

the ONE state and a positive 600-ma pulse switches it into the ZERO state. A pulse of up to 300-ma is insufficient to switch state. The 600-ma current switch which is required to change the state of a core array is delivered by two lines each carrying 300-ma in the same direction.

4-10. A 300-ma current is passed through one column of cores in each of the 16 bit planes by an x selection line, and another 300-ma current is passed through one row of cores by a y selection line. Refer to figure 4-3. A summation to form the 600-ma core "state-changing" current can occur at only one core in each bit plane. That core is in the same location in each bit plane, that is, at the intersection of the x and y selection lines carrying current. The location of the intersection concurs with the address of a particular location in E memory. Inhibit lines link each core in a bit plane. Therefore introduction of a 300-ma current on an inhibit line which is opposite to the current in the selection lines, prevents the core from changing state. The only cores which change state are the ones that are driven simultaneously by a 300-ma current in the x and y selection lines and not inhibited by a 300-ma current in an inhibit line. Actually, because of core characteristics, the Z inhibit current is 324 ma, or 108 per cent of the x or y current.

4-11. Before writing into a location (register) in the E memory, the location must be cleared. This is accomplished by 300-ma currents driven through one x and one y selection line (which intersect at the addressed location) in the direction indicated by the arrows in figure 4-3. All the cores of the addressed location which are in the ONE state will change to the ZERO state; all other cores in the array will remain in their existing state. When writing into the particular (last cleared) location, 300-ma currents are sent through the same x and y selection lines as before but in an opposite direction. A 300-ma current is also fed into the inhibit lines of all bit planes in which no ONE is to be written (i.e., where a ZERO should remain in the addressed register). At

write time, several different current conditions exist for the various cores. Whenever a core is intersected by only one selection line (x or y) carrying 300 ma, the core (of a register not addressed) remains in its existing state. Whenever a core is intersected by one selection line (x or y) and an inhibit line, each carrying 300 ma, the effect of both currents cancel each other and the core remains in its existing condition. Whenever a core is intersected by two selection lines (one x line and one y line) and an inhibit line, all carrying 300 ma, the net effect of all three currents is equal to the effect of a single 300-ma select current (passing through a core of an addressed register which has been cleared) and the core remains in the ZERO state. Only if a core is intersected by two selection lines (one x line and one y line) carrying 300 ma (but not an inhibit line carrying 300 ma) will a core change from the ZERO to the ONE state.

4-12. Reading out a location in the E memory is accomplished by detecting the outputs of the sense lines during the clearing of that location. All the cores of the addressed location which are in the ONE state induce a current in a sense line when switching to the ZERO state. An extremely small current is induced by other cores of the array as the addressed register is cleared. The sense lines are connected to amplifiers which amplify the current in a sense line and provide the power necessary to write ONEs into register G (figure 1-11).

4-13. As stated in paragraph 4-8, all cores in a bit plane are threaded diagonally by a common sense line and vertically by a common inhibit line. Inductive coupling between selection lines and sense lines, and between inhibit lines and sense lines is kept at a minimum (effectively zero). The inhibit lines are unipolar since the inhibition of writing is in the read direction only. The sense lines are bipolar to obtain effective noise reduction. The arrangement of cores and wiring is such that

half the cores in a bit plane are sensed in one direction and the other half are sensed in the opposite direction. Cumulative noise within a bit plane is reduced and a ONE output (of either polarity) from a selected core can be distinguished more easily than a combined ZERO and noise output.

4-14. SELECTION STEERING

4-15. There are 32 x selection lines and 32 y selection lines, each of which thread the same column of cores or the same row of cores in each bit plane (figure 4-3). A location (register or word) is selected by its x and y coordinates. The x and y selections are accomplished by means of current steering circuits which are organized on the principle of coincident selection. Figure 4-4 shows 24 selection switches which are arranged in four different groups.

4-15a. The three lowest order bits (1, 2, and 3) contained in register S (see table 1-4) govern selection switches 1 through 8, bits 4 and 5 govern switches 9 through 12, bits 6, 7 and 8 govern switches 13 through 20 and bits 9 and 10 govern switches 21 through 24. Table 4-1 lists the conditions under which the various switches conduct. Ten bits select among the 1008 words as required. The signals which govern the switches are suppressed when register S contains a ONE in bit positions 11 and/or 12, or an address lower than octal 0020. Figure 4-5 illustrates the steering of the x selection lines. If a write current is to be initiated in selection line 25, selection switches 1 and 12 have to be energized. The steering of the y selection lines operates the same way. In normal operation of the AGC, a location (register) in the E memory is cleared before it is written into. Ferrite switch cores are built into the selection switches to enable the computer to remember the location last cleared, hence the one to be written into next.

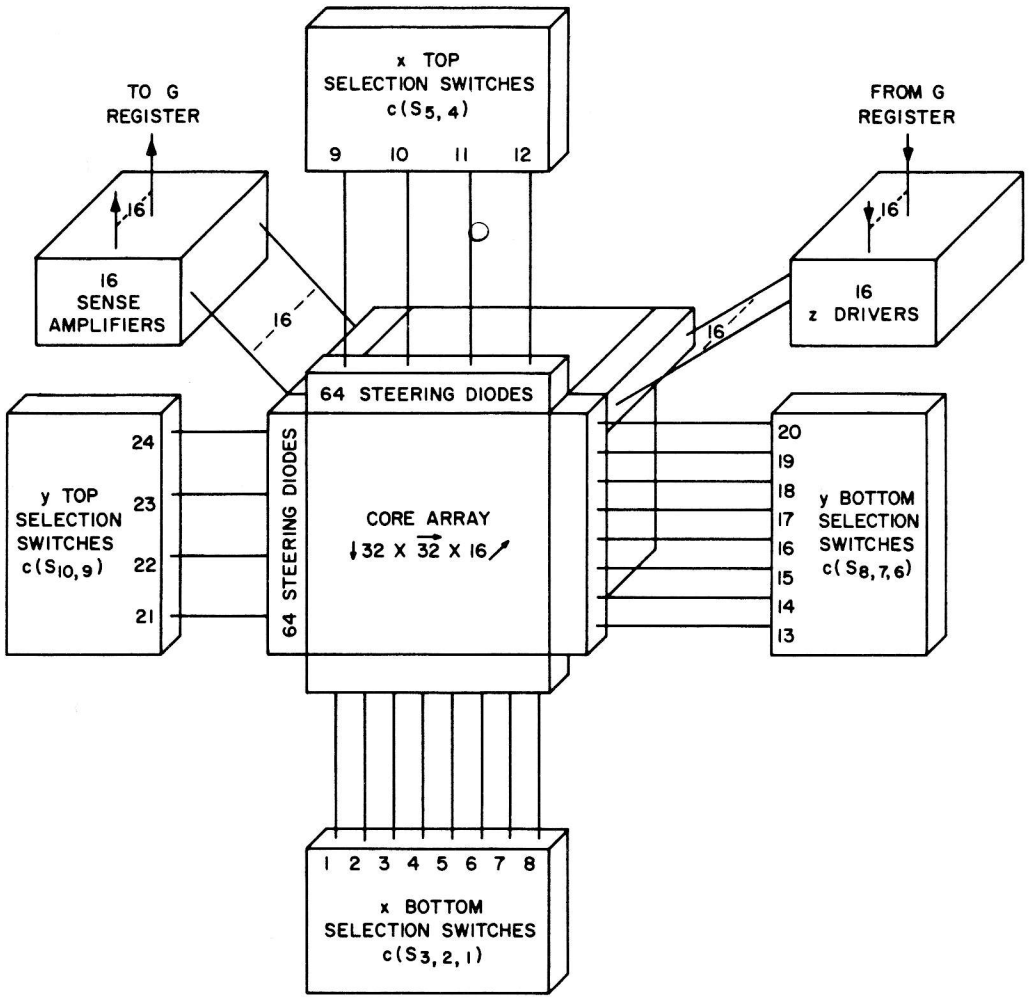

Figure 4-4. Addressing, Reading, and Writing into Core Array

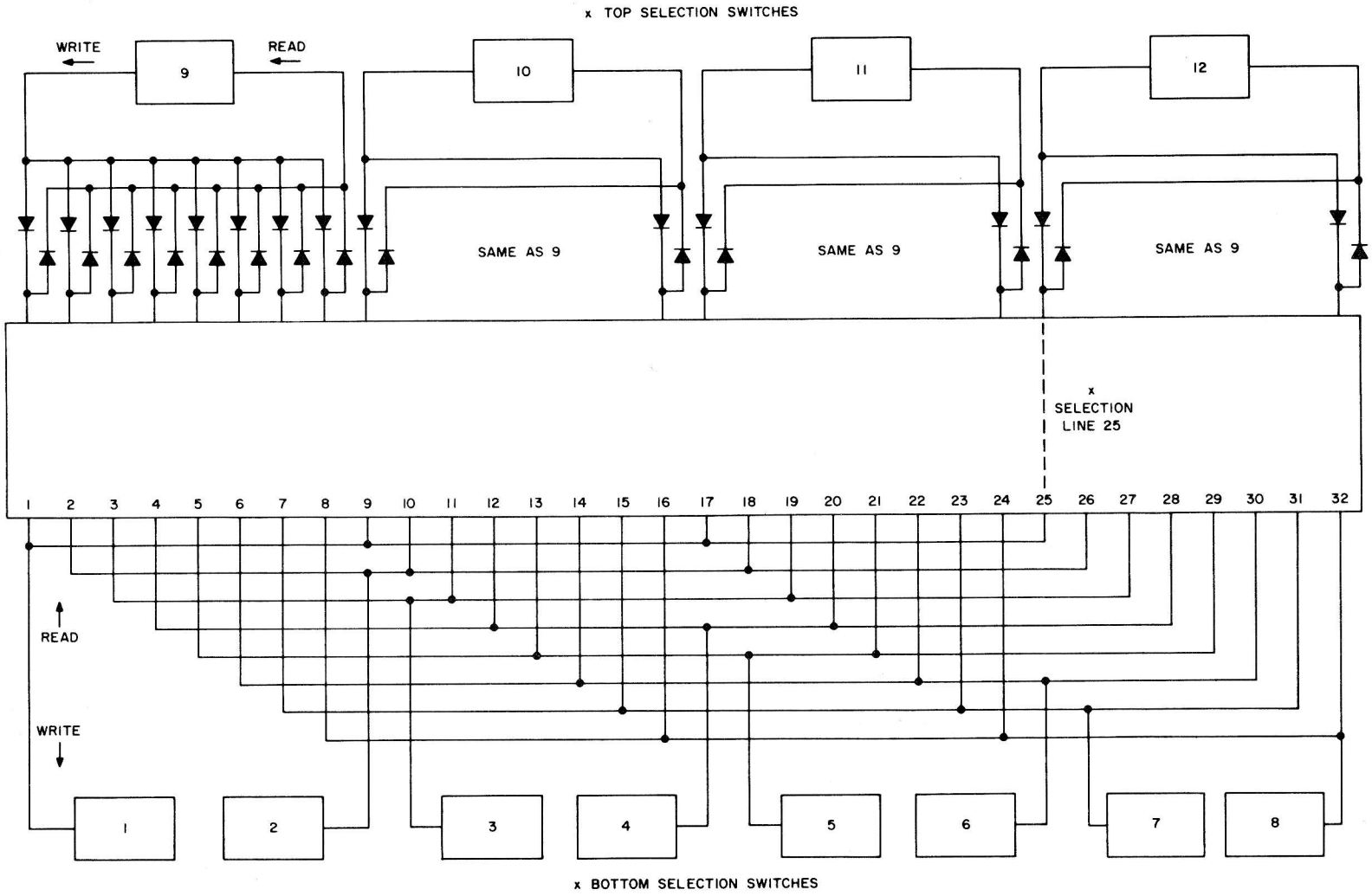

Figure 4-5. X Selection Steering

4-16. The timing of the erasable memory cycle (figure 4-6) is similar to conventional coincident-current memory cycles, except ample time is provided between read and write current pulses to allow full recovery of the magnetic cores after switching. A Memory Cycle Time (MCT) consists of twelve Actions and takes 11.7 μsec (paragraph 1-28). Once a selection has been made, a location in E memory is read out and cleared by driving the necessary currents through the proper x and y lines. The information stored in an addressed register is impressed upon the 16 sense lines and transferred to register G. Information read out of the E memory can be assumed to be available in the G register after Action 6. When a word is to be written into the memory, the desired pattern of ONEs and ZEROs is impressed on the inhibit lines (by the z drivers) after Action 9 and the memory is addressed by the proper x and y drive lines.

4-17. Figure 4-7 illustrates the operation of the selection switches. Only four of the 24 selection switches and four of the 128 steering diodes which control the x and y selection lines of the core array are shown. Each selection switch consists of a ferrite selection core with four windings (20, 30, 30 and 50 turns) and two medium-power transistors. One transistor forms a path for the read selection current and the other forms a path for the write selection current. In order to generate a current in one x and one y selection line for read-out or write in, one x-bottom, one x-top, one y-bottom and one y-top selection switch has to conduct. Normally, selection cores K1 through K24 are in the ZERO state and set to the ONE state at time of readout (of the core array) and reset to the ZERO state at time of write-in.

4-18. When x selection line 25 has to be energized for readout or write-in selection switches 1 and 12 have to be activated. The transistor of circuit 40251A conducts only if signal XB0 is present; when signal XB0

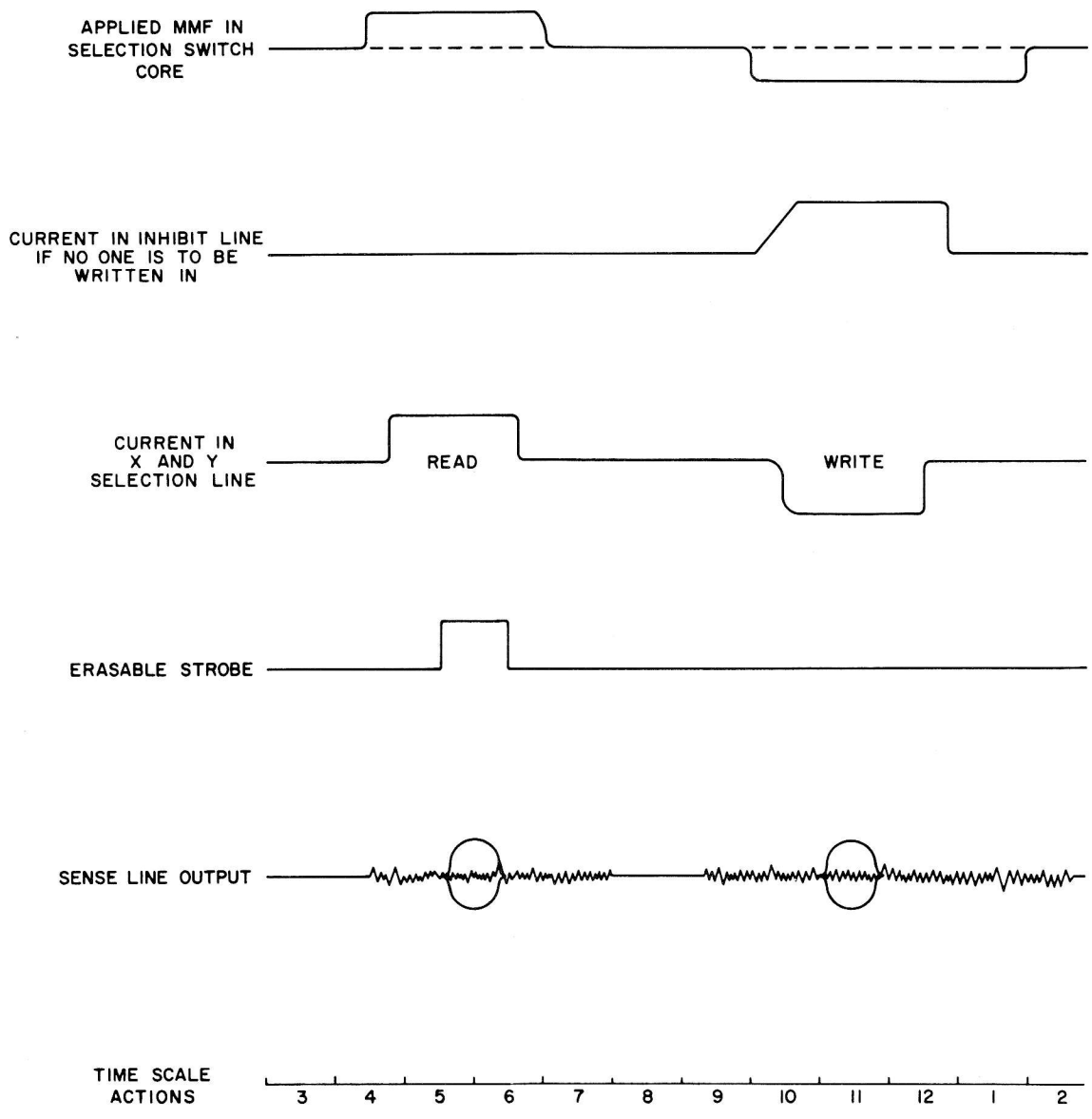

Figure 4-6. Erasable Memory Timing

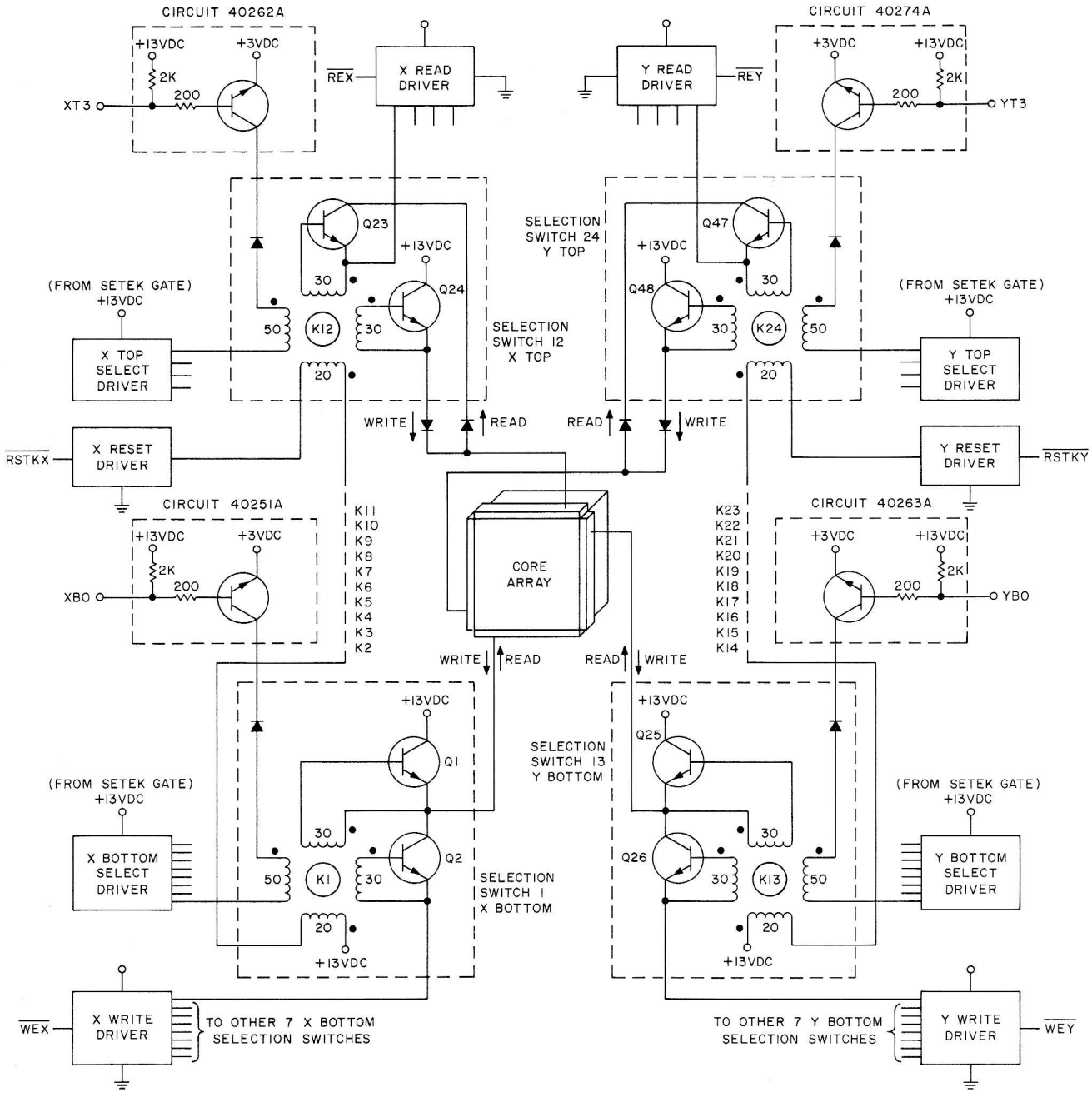

Figure 4-7. Selection Switches

is absent the input of the transistor remains at about 0.2 volt. Table 4-1 lists the control signals for circuits 40251A through 40274A which feed selection switches 1 through 24. Once circuit 40251A is conducting, and provided that the x-bottom select driver is energized, current flows through the 50-turn winding of core K1 and switches it to the ONE state. The select driver is energized by a +13 VDC signal from the SETEK gate which is turned on by signal SETEK, shown in figure 4-8. As K1 changes from a ZERO state to a ONE state, a current is induced in the upper 30-turn winding of K1 which causes transistor Q1 to conduct. The force induced in the other 30-turn winding opposes conduction of Q2. In a similar way, signal XT3 causes circuit 40262A to conduct and the x-top select driver sets core K12 into a ONE state. As K12 changes from a ZERO state to a ONE state, transistor Q23 turns on. At the time that transistors Q1 and Q23 conduct and control signal $\overline{\text{REX}}$ is applied to the 300-ma x-read driver, a 300-ma current will flow through selection line 25. At the same time, the 300-ma y-read driver forces a 300-ma read current through one of the y selection lines and control signal SBE causes the generation of signal STBE for gating the sense amplifiers.

4-19. Generating a write current in a selection line is very similar to generating a read current. Control signal $\overline{\text{RSTKX}}$ causes the 80-ma x-reset driver to generate a current which passes through the 20-turn winding of cores K12 through K1. Since this current resets any core which is in the ONE state to the ZERO state (in our example cores 1 and 12), transistors Q2 and Q24 will conduct. At the time that transistors Q2 and Q24 conduct and control signals $\overline{\text{WEX}}$ is applied to the 300-ma x-write driver, a 300-ma current will flow through selection line 25. At the same time, the 300-ma y-write driver forces a 300-ma write current through one of the y selection lines, and the z drivers (controlled by register G and control signal ZID) generate inhibit currents.

TABLE 4-1

CONTROL OF SELECTION SWITCHES

SELECTION SWITCH	CONTROL SIGNAL	BIT POSITIONS OF REGISTER S									
		10	9	8	7	6	5	4	3	2	1
1	XB0								0	0	0
2	XB1								0	0	1
3	XB2								0	1	0
4	XB3								0	1	1
5	XB4								1	0	0
6	XB5								1	0	1
7	XB6								1	1	0
8	XB7								1	1	1
9	XT0						0	0			
10	XT1						0	1			
11	XT2						1	0			
12	XT3						1	1			
13	YB0			0	0	0					
14	YB1			0	0	1					
15	YB2			0	1	0					
16	YB3			0	1	1					
17	YB4			1	0	0					
18	YB5			1	0	1					
19	YB6			1	1	0					
20	YB7			1	1	1					
21	YT0	0	0								
22	YT1	0	1								
23	YT2	1	0								
24	YT3	1	1								

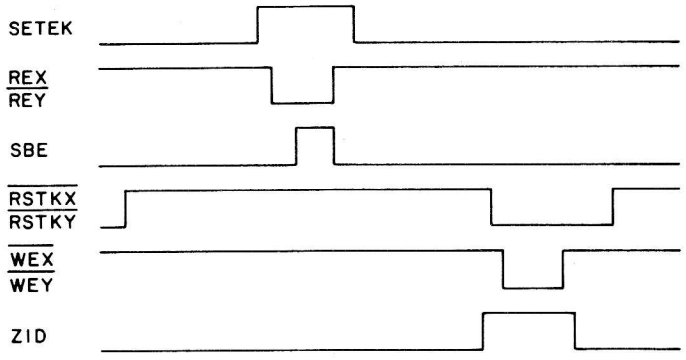

Figure 4-8. Selection Switch Gating

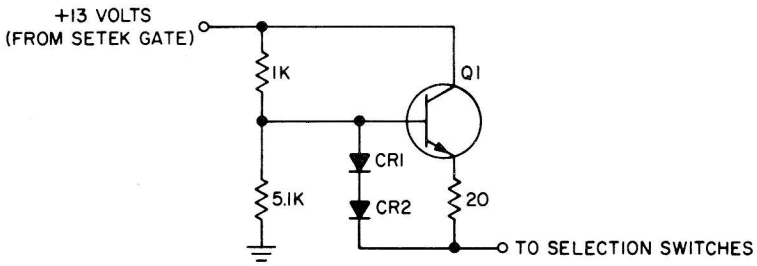

Figure 4-9. Select Driver Circuit

4-20. DRIVERS AND AMPLIFIERS

4-21. The various drivers shown in figure 4-7 are insensitive to power supply variations. The four select driver circuits (x-top, x-bottom, y-top, and y-bottom) are identical, each having an output of 40-ma. A select driver is illustrated on figure 4-9. The four drivers are energized simultaneously by application of a +13 volt (B Plus) signal from the SETEK gate. Diodes CR1 and CR2 maintain a constant voltage on the base of transistor Q1 and thus provide a constant current output, which is sent through the 50-turn winding of the proper selection switch.

4-22. The SETEK gate (not shown in figure 4-7) acts as a power switch for the select drivers by supplying +13 volts to them. The ZID gate (not shown in figure 4-7) acts as an enabling gate for the z inhibit drivers by supplying +13 volts to them.

4-23. Figure 4-10 illustrates one of the x-read, y-read, x-write, or y-write drivers. These drivers may be considered as current drivers due to their insensitivity to transistor parameters and power supply variations. Input signals $\overline{\text{WEX}}$, $\overline{\text{WEY}}$, $\overline{\text{REX}}$, or $\overline{\text{REY}}$ are inverted to positive functions by input transistor Q1. Diodes CR1 and CR2, transistor Q2, and the 20-ohm resistor stabilize Q3 base current and the current through diodes CR3, CR4, and CR5 by maintaining a constant voltage will appear across the 20-ohm resistor. Diodes CR3, CR4, and CR5 maintain a constant voltage on the base of transistor Q3. Collector current rise time is controlled by the inductance in the emitter lead of Q3. Collector current is independent of collector voltage provided Q3 remains unsaturated.

4-24. The x and y reset currents are supplied by a pair of identical reset drivers. Refer to figure 4-7. The x and y reset drivers supply 80 ma to the x and y selection cores, respectively. Input transistor Q1 (figure 4-11) is an interface stage which inverts the input to a positive function. Diodes CR1, CR2, and CR3 maintain a constant voltage on the base of Q2, thereby delivering a constant current output. The x-reset driver and y-reset driver are turned on by signals $\overline{\text{RSTKX}}$ and $\overline{\text{RSTKY}}$, respectively.

4-25. The z inhibit driver circuits are identical with the read and write drivers except that the z inhibit drivers have no inductance in the emitter lead of transistor Q3. The operation of the inhibit driver circuits is like that of the read and write drivers. (See paragraph 4-23.) An input signal from the G register is applied to the base of transistor Q1 and, provided the gated +13 volts from the ZID gate is present, an inhibit current is fed into the inhibit line of the particular bit plane of the erasable memory in which no ONE is to be written.

4-26. Sixteen sense amplifiers (one per bit position) accept bipolar signals from the erasable memory sense lines. (See figure 4-12) As stated in paragraph 4-12, a location in the E memory is read out by detecting and amplifying the outputs of the sense lines in each bit plane. When a core in the E memory switches from a ONE state to a ZERO state, a small current is induced in the sense line and applied to the input of transformer T1. The output of transformer T1 is connected to the input of the sense amplifier. Base bias voltage Vz is applied via resistors R1 and R2 to the sense amplifier input circuit. The input stage is a differential amplifier consisting of transistors Q1 and Q2 with associated resistors. Transistor Q3 is a constant current source for the differential amplifier which establishes the DC operating point and minimizes common-mode noise. The common-mode rejection is approximately

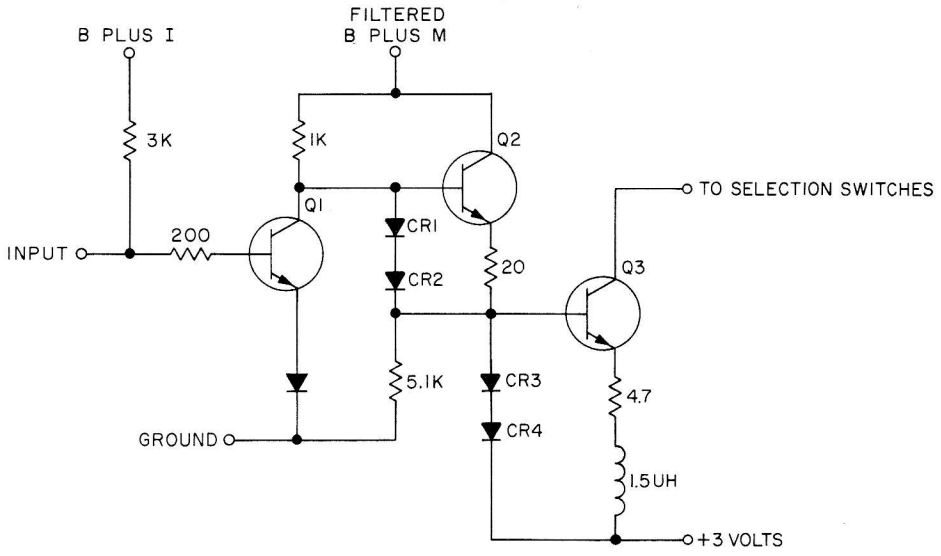

Figure 4-10. Read or Write Driver Circuit

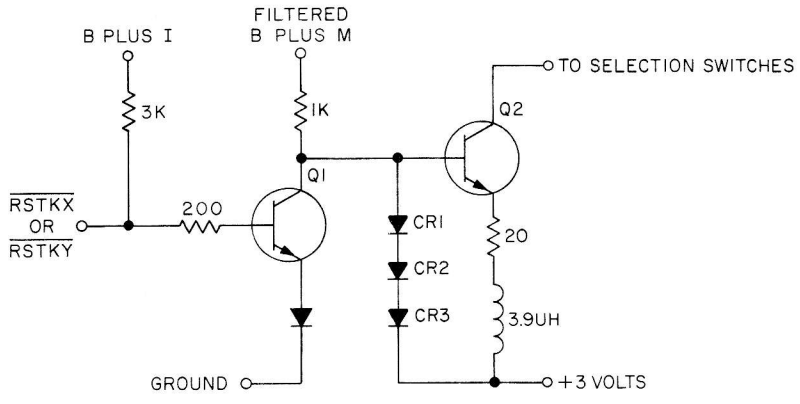

Figure 4-11. Reset Driver Circuit

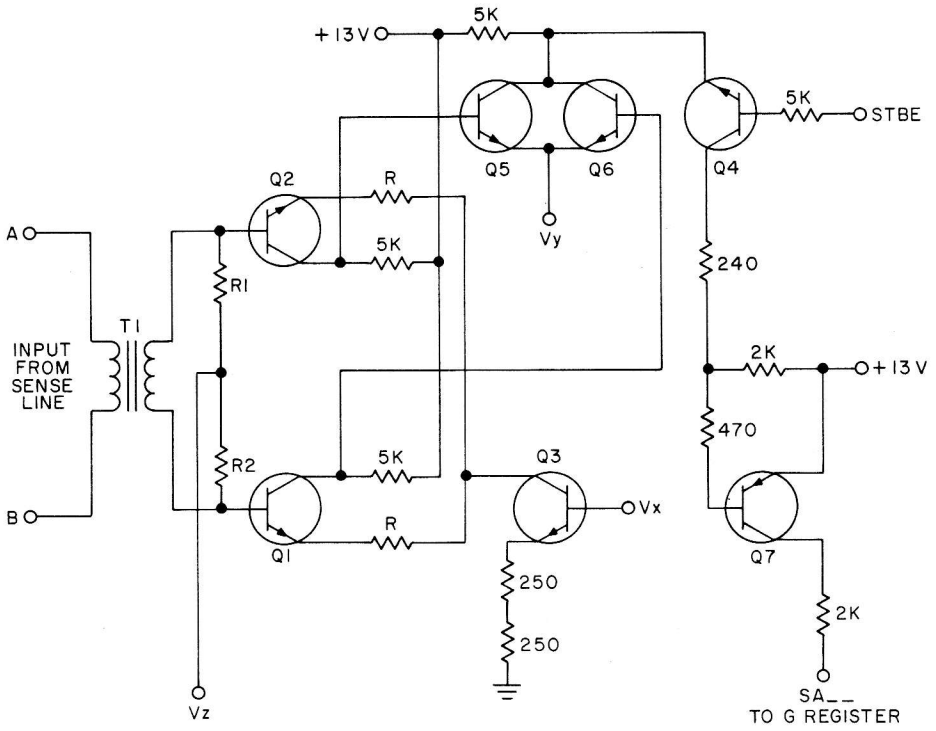

Figure 4-12. Sense Amplifier

one volt. The output of the differential amplifier connects to the inputs of the threshold detector which consists of transistors Q5 and Q6. The emitter leads of Q5 and Q6 connect to voltage Vy which is adjustable to set the sensing threshold for differential noise rejection. The differential noise input may be 10 mv for a 50-mv nominal input to the differential amplifier. Transistors Q5 and Q6 cannot be turned on unless their respective base drive exceeds a predetermined signal level established by voltage Vy. The base input of Q5 is obtained from the collector of Q2 and the base input of Q1 is obtained from the collector of Q6. This forms a single polarity output, even though the input waveform is bipolar in nature. The sense amplifier output is fed through interface transistor Q7 to the G register by strobing transistor Q4. If a ONE from the sense line causes Q5 or Q6 to be on, current will flow from the collector of Q4 through Q5 or Q6 to Vy. The erasable memory output is strobed, or gated, out of the sense amplifiers and into the G register. The pattern of ONEs and ZEROs depends on the word previously written into the erasable memory. Voltages Vx, Vy, and Vz which are required for sense amplifier operation, are provided by a temperature-compensated voltage source.