Lennon

APOLLO ENGINEERING MEMORANDUM AP-M NO. 16949

13 September 1967

TO: Mr. J. Wachholz

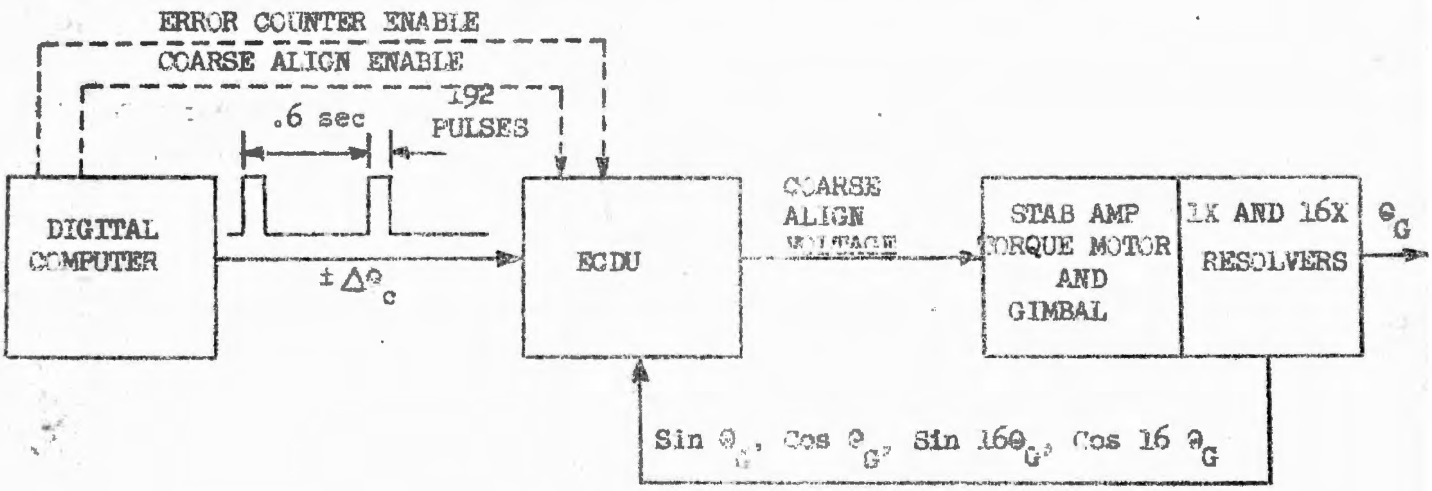
FROM: Mr. R. Vander Voort

cc: Messrs. H. Baumann, J. Beauregard, F. Box, H. Brady, R. Brandt, M. Cavalier, H. Cork, F. Dasse, D. Dettmann, D. Fischer, F. Gamber, D. Grassell, H. Hall, P. Headley, H. Herr, M. Johnson, E. Juel, J. Kaiser, R. Kraemer, R. Lingg, M. Lynn, J. Marquardt, D. Miller, L. Mosier, H. Neuville, R. Petryk, T. Postma, W. Ryan, J. Sudman, W. Swingle, W. Thomas, G. Tietmeyer, N. Yunk, V. Zak, D. Ziemer, DRF.

SUBJECT: NOTES ON THE BLOCK II COARSE ALIGN LOOP.

**INTRODUCTION:**

The servomechanism used to achieve coarse align of the Block II IMU is shown in figure 1.




IMU COARSE ALIGN LOOP

Figure 1

As shown in this figure, the three basic elements of the coarse align loop are;

1. THE DIGITAL COMPUTER - which issues angle commands and appropriate moding discretes.

2. THE ECDU - which encodes gimbal position and provides position and rate feedback for proper loop operation.

3. THE IMU

The role that each of the above elements plays in achieving coarse align is discussed in detail in this memorandum along with the total operation of the coarse align loop.

DISCUSSION

COMPUTER OPERATION The following sequence of events is performed by the computer each time the coarse align program is entered.

1. Issue Coarse Align Enable - The computer sets bit 4 of channel 12 which issues the "coarse align enable" discrete to the ECDU.

2. Issue Error Counter Enable - The computer sets bit 6 of channel 12 which issues the "error counter enable" discrete to all 3 IMU axis of the ECDU.

3. Determine Command Angle - The contents of the computer gimbal angle counters are read and differenced with the desired gimbal angle to determine the command angle.

4. Issue Command Angle - Gimbal angle commands are issued in bursts of 192 pulses (8.4°) at a rate of 3200 pulses/sec. Each burst requires 60 msec. The delay between bursts is 540 msec. If the command is not an integral multiple of 192 pulses, the remainder is issued as the last command. Gimbal commands are gated out of the computer by setting bits 13, 14 and 15 of channel 14. All 3 bits are set simultaneously thereby allowing all 3 gimbals to be slewed simultaneously.

5. Determine if Command Angle is Achieved - After gimbal commands have been issued, the computer reads gimbal position and compares the position achieved with the desired angle. If the difference is greater than 2.0° and alarm is issued.

Steps 1 through 5 above constitute a computer control process which positions gimbals in an open loop sense. The computer does not check final gimbal position such that corrective commands can be issued if the desired position has not been reached. The check on final gimbal position is used to determine if an alarm condition exists.

ECDU OPERATION The operation of the ECDU during coarse align of the IMU can be divided into two catagories, they are;

1. Moding control of the IMU

2. Servo control of the IMU

ECDU Moding Control ECDU moding control of the IMU is shown in figure II. The ECDU accepts moding discretes from the computer and processes them to control PSA moding as well as ECDU internal moding. The functions performed by the ECDU in response to moding commands from the computer are as follows:

ECDU response to coarse align enable When addressed by the coarse align enable discrete from the computer the ECDU;

1. Provides a ground to the PSA Coarse align input relays thereby switching the stab-amp inputs from IRIG outputs to the ECDU DAC output.

2. Supplies a ground for the PSA Stab Amp Demod relay thereby changing the reference excitation of the stab amp ring demodulators from 3200 hertz to 800 hertz.

3. Provides grounds for the coarse align relay in each of the stab amps thereby changing stab amp servo compensation.

4. Generates an internal moding signal which enables gimbal feedback pulses ($\Delta 2^2$) to increment the error counter. This signal also changes the read counter high speed pulse rate ($P_I$ pulses) from 12.8K pps to 6.4K pps.

ECDU Response to Error Counter Enable When addressed by the error counter enable discrete from the computer the ECDU;

1. Generates an internal moding signal which allows error counter pulses ($P_E = \Delta 2^2$ or $\Delta \theta_c$) to increment the error counter. Absence of this discrete zeros the error counter and holds it there.

2. The "Error Counter Enable" command (E) is combined with the Coarse Align discrete ($C_A$) and the "CDU Zero" command (CDUZ) to mode the read counter in accordance with the following logic equation.

$$Y = \overline{E} \cdot C_A + CDUZ$$

where;

a. The presence of Y inhibits $P_I$ pulses from incrementing the read counter

b. $\overline{E}$ = Error Counter Enable "not"

c. $C_A$ = Coarse Align Enable

d. CDUZ = CDU Zero discrete

e. $E \cdot C_A$ is an "and" operation

f. + is an "or" operation

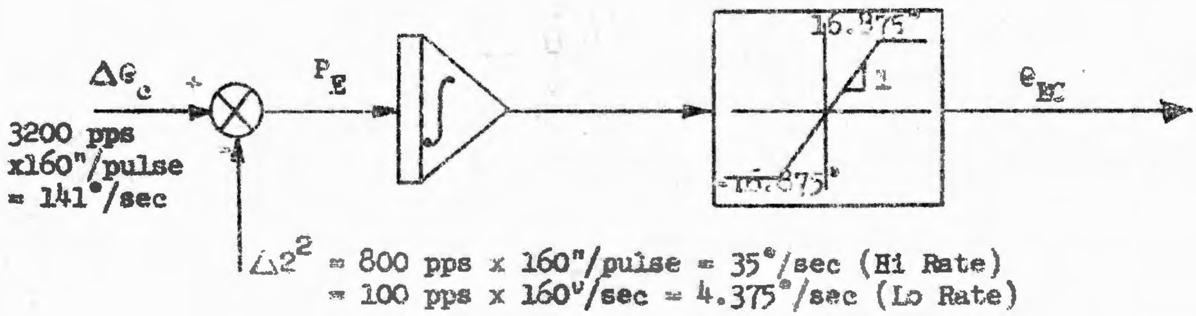
Inhibiting the read counter in this fashion will prevent gimbal drift due to residual voltages within the loop. The fine error will accumulate to a value such that the effect of residual voltages is cancelled.

ECDU Servo Control Servoing the IMU to the correct position as commanded by the computer is accomplished by the ECDU. Figure 3 is a functional block diagram which illustrates the multi-loop servoing role played by the ECDU. Figure 4 shows the manner in which each element of figure 3 may be modeled to evaluate the dynamic performance of the coarse align loop. Figure 5 is the schematic diagram from which the Algorithm's of figure 4 were derived. Each of the elements shown in figure 4 is derived as follows:

1. Error Counter The error counter provides digital differencing between gimbal commands and gimbal positions. Input pulses to the error counter are either position command pulses ($\Delta \theta_c$) from the computer or gimbal position feedback pulses ($\Delta 2^2$) from the read counter loop. Computer command pulses ($+\Delta \theta_c$) cause the error counter to count up. Read counter ($\Delta 2^2$) pulses will in turn count the error counter down thereby

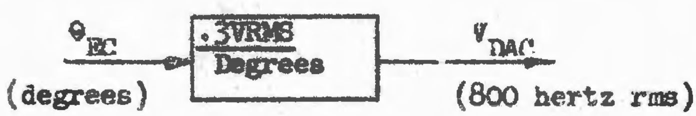
1. (continued)

producing negative feedback. The error counter is also mechanized to inhibit ($P_E$) pulses when bits 7 and 8 of the error counter are "1". The result is a limiting of the output at 11.25° + 5.625° or 16.875°. The total functional characteristic is shown below.



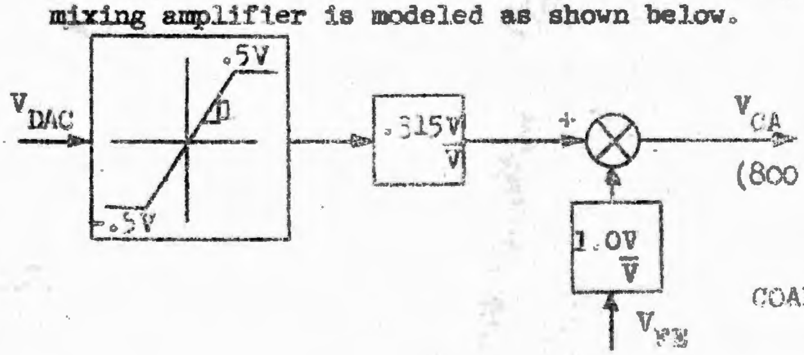

ERROR COUNTER

2. DAC - Digital to Analog Converter The DAC consists of logic switches driven by the error counter, a divide down resistive ladder network, and a scaling amplifier (figure 5). The function of the DAC is to provide an 800 hertz signal whose amplitude is proportional to the angle content of the error counter. DAC sensitivity is adjusted to 0.3 Vrms/degree by selecting the feedback resistor in the DAC scaling amplifier (figure 5). A functional block diagram of the DAC is shown below.



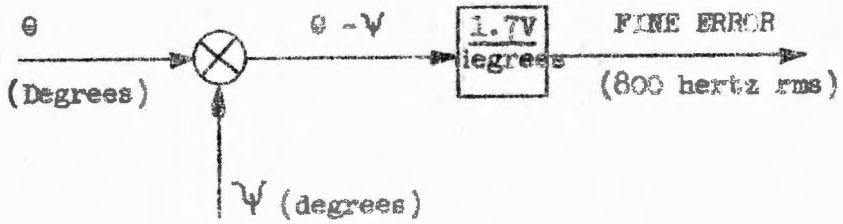

DIGITAL TO ANALOG CONVERTER

3. Coarse Align Mixing Amp The coarse align mixing amp is a high gain ac amplifier with feedback (figure 5). This amplifier adds the fine error voltage and the DAC output with a mixing ratio of 3 to 1 in favor of the fine error input. DAC outputs to the coarse align mixing amplifier are diode limited to 0.5Volts as shown in figure 5. The coarse align mixing amplifier is modeled as shown below.




COARSE ALIGN MIXING AMP

4. **Fine System Switch Selection Logic** The fine system switch selection logic is a network of weighting resistors, summing amplifiers and switches used to implement the trigonometric identity $-\sin(\theta - \psi) = -\sin\theta\cos\psi + \cos\theta\sin\psi$. Functionally this network compares the gimbal angle ($\theta$) as represented by the 16 speed resolver signals to the read counter angle ($\psi$) and generates an error signal used to drive the read counter loop. The error signal is $\sin(\theta - \psi)$. For small angles, $\sin(\theta - \psi) \approx \theta - \psi$. The functional equivalent of the "fine system switch logic" is as shown below.

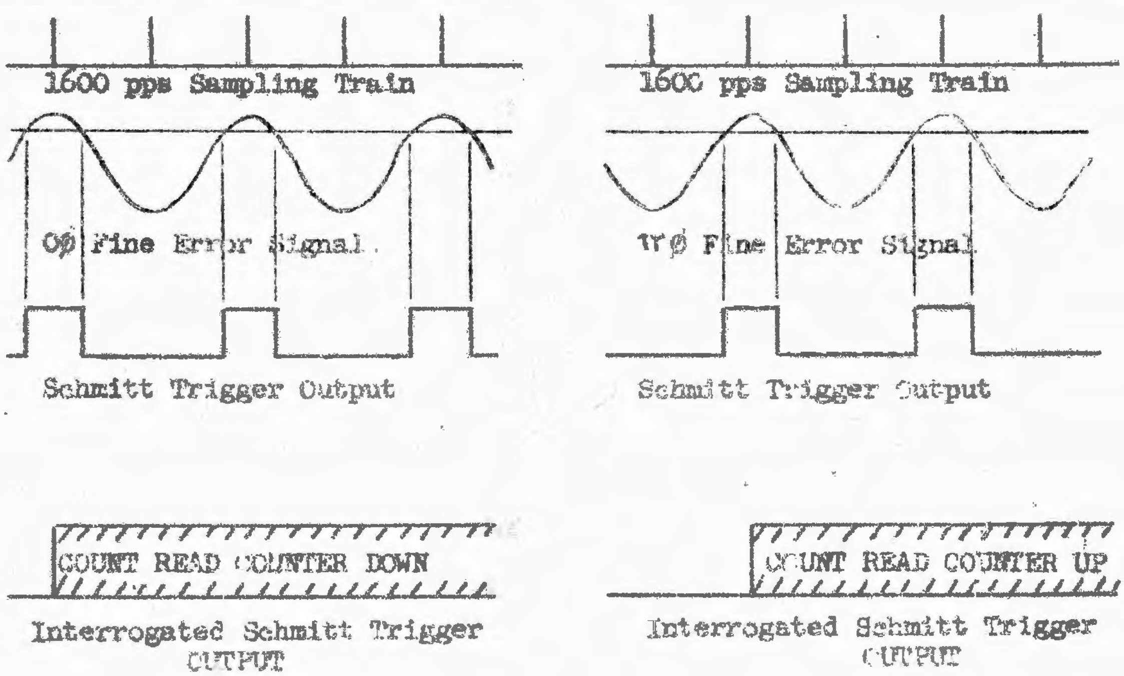



Fine System Switch Selector Logic

5. **Rate Select and Up/Down Logic** Rate select and up/down logic is generated from the fine error signal (an analog measure of the error between resolver angle and read counter angle) by schmitt trigger type level detectors. When the fine error signal is large, rate select logic will cause the read counter to count at a 6400 pps rate. Small fine error signals are counted down at 800 pps (figure 4).

The logic output of the Schmitt triggers is high (+6.2V) when the fine error 800 hertz input is above the trigger level, and low (0.0V) where the input is below the trigger level. The trigger threshold for the low speed count rate is 0.1Volts. The trigger threshold for the high speed count rate is 1.7 Volts. (figure 5)
1.2 volts

The output of the Schmitt triggers is interrogated by a 1600 pps pulse train which is in turn synchronized with the 800 hertz excitation. As shown by the time line below

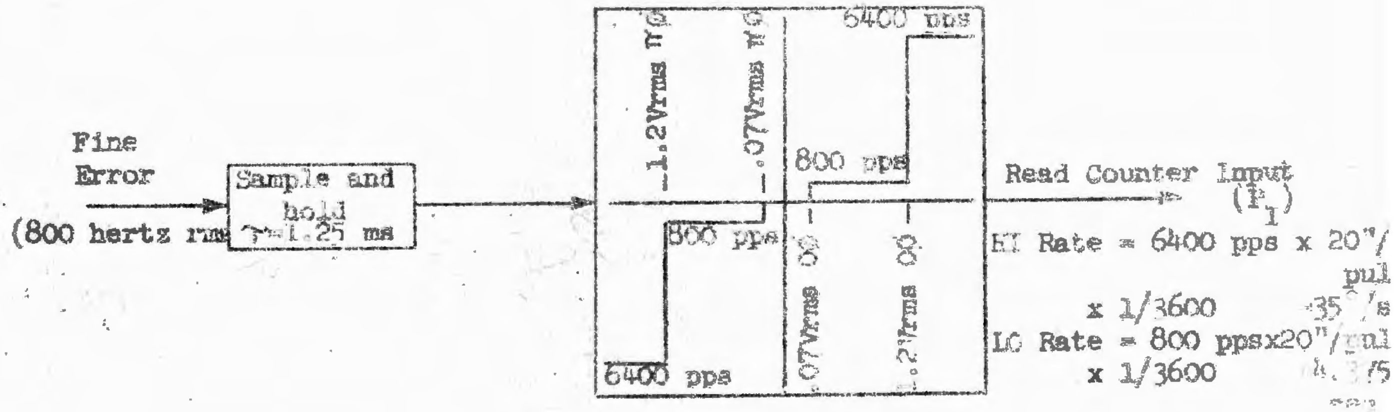


5. (continued)

The result is a sample and hold effect with a period of 1.25 msec which can detect either 0 phase or $\pi$ phase errors. The read counter loop is mechanized such that if $\theta > \psi$ a $\pi$ phase error will be generated by the fine system switching logic, this in turn will cause the read counter to count up.

The rate select and up/down logic processes the sampled output of the Schmitt triggers to determine at which rate the read counter should be incremented. If the high speed Schmitt is on the read counter is incremented at 6400 pps, if the fine Schmitt is on the rate is 800 pps. Thus in one sample time the read counter will be incremented 1 bit at low speed or 8 bits at high speec.

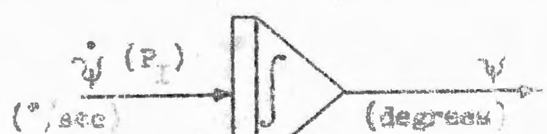
A functional representation of the Schmitt triggers and rate select logic is shown below.




6. <u>Read Counter</u> The read counter is a 16 stage digital counter with an IMU angle granularity of 20"/bit. Inputs to the read counter are controlled by rate select and up/down logic. The output is used by the fine system switch selection logic to produce the fine error signal (figure 5). Access to the contents of the read counter by both the computer and the error counter is serial only. Access by the computer is to the low order bit ($\Delta 2^0$). Access by the error counter is to the third order bit ($\Delta 2^2$). Because of the above, the count rate to the computer is four times faster than to the error counter. Computer bits however have one fourth the weight factor of those transferred to the error counter.

To comp 40 sec/bit
Error ctr 160 sec/bit

Functionally, the read counter is represented as an integrator with a count rate in °/second and an output in degrees.



7. <u>Stab Loop</u> The analog part of the coarse align servomechanism consists of the stab amp, torque motor and gimbal. These elements are functionally represented as follows:

STAB AMP

$$V_{CA}\ (800\text{ hertz rms}) \longrightarrow \boxed{\dfrac{15\left(\dfrac{S}{1.925}+1\right)\left(\dfrac{S}{24.3}+1\right)}{\left(\dfrac{S}{.125}+1\right)\left(\dfrac{S}{217}+1\right)}} \longrightarrow i_{TM}\ (\text{amps})$$

TORQUE MOTOR

$$i_{TM}\ (\text{amp}) \longrightarrow \boxed{1.12\ \dfrac{\text{ft lb}}{\text{amp}}} \longrightarrow T\ (\text{ft-lb})$$

GIMBAL

$$T\ (\text{ft-lb}) \longrightarrow \boxed{\dfrac{3438}{S^2}\ \dfrac{\text{Degrees}}{\text{ft-lb}}} \longrightarrow \theta_G\ (\text{Degrees})$$

The overall transfer function of the above three elements is as shown below.

$$V_{CA}\ (800\text{ hertz rms}) \longrightarrow \boxed{\dfrac{3580\left(\dfrac{S}{1.925}+1\right)\left(\dfrac{S}{24.3}+1\right)}{\left(\dfrac{S}{.125}+1\right)\left(\dfrac{S}{217}+1\right)S^2}} \longrightarrow \theta_G\ (\text{Degrees})$$

As shown in this figure, output of the DAC is differenced with the fine error signal to achieve gimbal rate limiting. The mechanism via which gimbal rate limiting is achieved is as follows:

1. If the DAC output is greater than 1.6 degrees, the corresponding signal commanding IMU position will be limited to 0.5 volts by diode clipping in the coarse align mixing amp. This signal is sufficient to saturate the stab amp and drive the gimbal at a high rate.

2. The fine error signal is an analog measure of the angular accuracy with which the read counter is tracking IMU resolver position. For high gimbal rates, the angular error between gimbal position and the read counter measurement of gimbal position will be large. The magnitude of the fine error signal is therefore related to gimbal rate.

3. If the fine error signal is mixed in a negative feedback sense with the DAC output, the net command to position the IMU is a function of their difference. Thus if the gimbal rate exceeds the maximum read counter rate the fine error increases to a value which will conceal the DAC output thereby limiting gimbal rate to a value equal to the maximum read counter rate. As a result, gimbal momentum is controlled such that the coarse align loop is stable and gimbal rate is limited to a maximum value of 35°/sec.

Analog Computer Simulation of Coarse Align The analog computer simulation of the block diagram shown in figure 4 is shown in figure 8. Loop response to normal command sequences is shown in figures 9, 10 and 11. Figure 9 is the response of the coarse align loop to a single burst of 192 pulses. The fine error signal shown is the output of the main summing amp and therefore will be 7.5 times less than the output of the error amp which is the ECDU test point.

Figure 10 is the response of the coarse align loop to normal computer outputs which consists of a sequence of pulse bursts each consisting of 192 bits. The response of coarse align to the GSE computer simulator output is shown in figure 11.

Figure 12 shows the effect of gimbal friction, stab-amp offset, and DAC residual on positioning accuracy. The initial conditions are 10 mv DAC residual, 15 mv stab amp offset, 38 ma gimbal friction and zero bits in the error counter.

Gimbal Positioning Accuracy The accuracy with which the coarse align loop can position the IMU is proportional to the uncertainty in the output of each of the major loop elements shown in figure 4. Total steady state stand-off error may be evaluated by using superposition ie. the uncertainty in output of each major loop element is regarded as a command reference input to which the loop will position itself. Table I is a tabular listing of each major error source and the corresponding stand-off in gimbal position that would occur if each element were acting alone.

Table II is an RSS summary of the zero to peak error sources shown in Table I.

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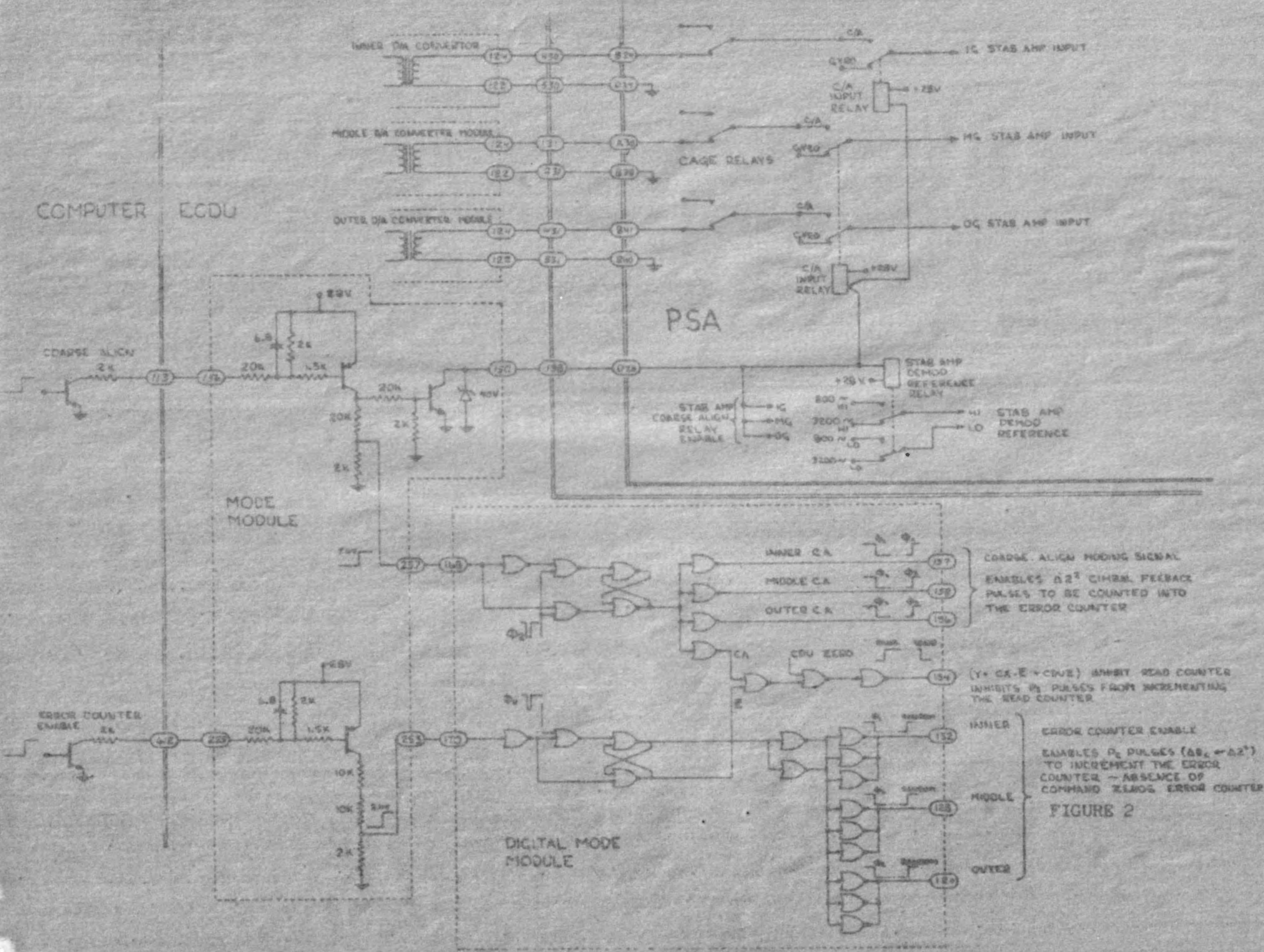
attachment

TABLE I

| ERROR SOURCE | ERROR SOURCE MAGNITUDE | SCALE FACTOR RELATING GIMBAL STAND OFF TO ERROR SOURCE (FIGURE 4) | PEAK GIMBAL STANDOFF |
|---|---|---|---|
| ERROR COUNTER GRANULARITY | 1 Bit | ERROR COUNTER WEIGHT FACTOR $\left\{\frac{.044°}{\text{Bit}}\right\}$ | .044° |
| DAC RESIDUAL | 10 mv (ATP 2015497) | $\frac{1}{\text{DAC SCALE FACTOR}} \left\{\frac{3.33 \text{ Degrees}}{\text{Volts}}\right\}$ | .033° |
| STAB AMP OFFSET | 15 mv | $\frac{1}{\text{(DAC SCALE FACTOR) (C/A MIXING AMP GAIN)}}$ <br> $\frac{1}{(.3\text{V/Degree})\ (.315\ \text{V/V})} = \frac{10.59 \text{ Degrees}}{\text{Volt}}$ | .159° |
| GIMBAL FRICTION | 125 ma (ATP 2015497) | $\frac{1}{\text{(DAC SCALE FACTOR)(C/A MIXING AMP)(STAB AMP)}}$ <br> $\frac{1}{(.3\text{V/Degree})(.315\ \text{V/V})(15\ \text{amp/volt})} =$ <br> $\frac{.705 \text{ Degrees}}{\text{Amp}}$ | .0885° |
| FINE ERROR VOLTAGE FEEDBACK | 9.35 mv | $\frac{1}{\text{(DAC SCALE FACTOR)(C/A MIXING RATIO)}}$ <br> $\frac{.43\text{V/V}}{(.3\text{V/Degree})(.315\ \text{V/V})} = \frac{4.45°}{\text{Volt}}$ | .0425° |

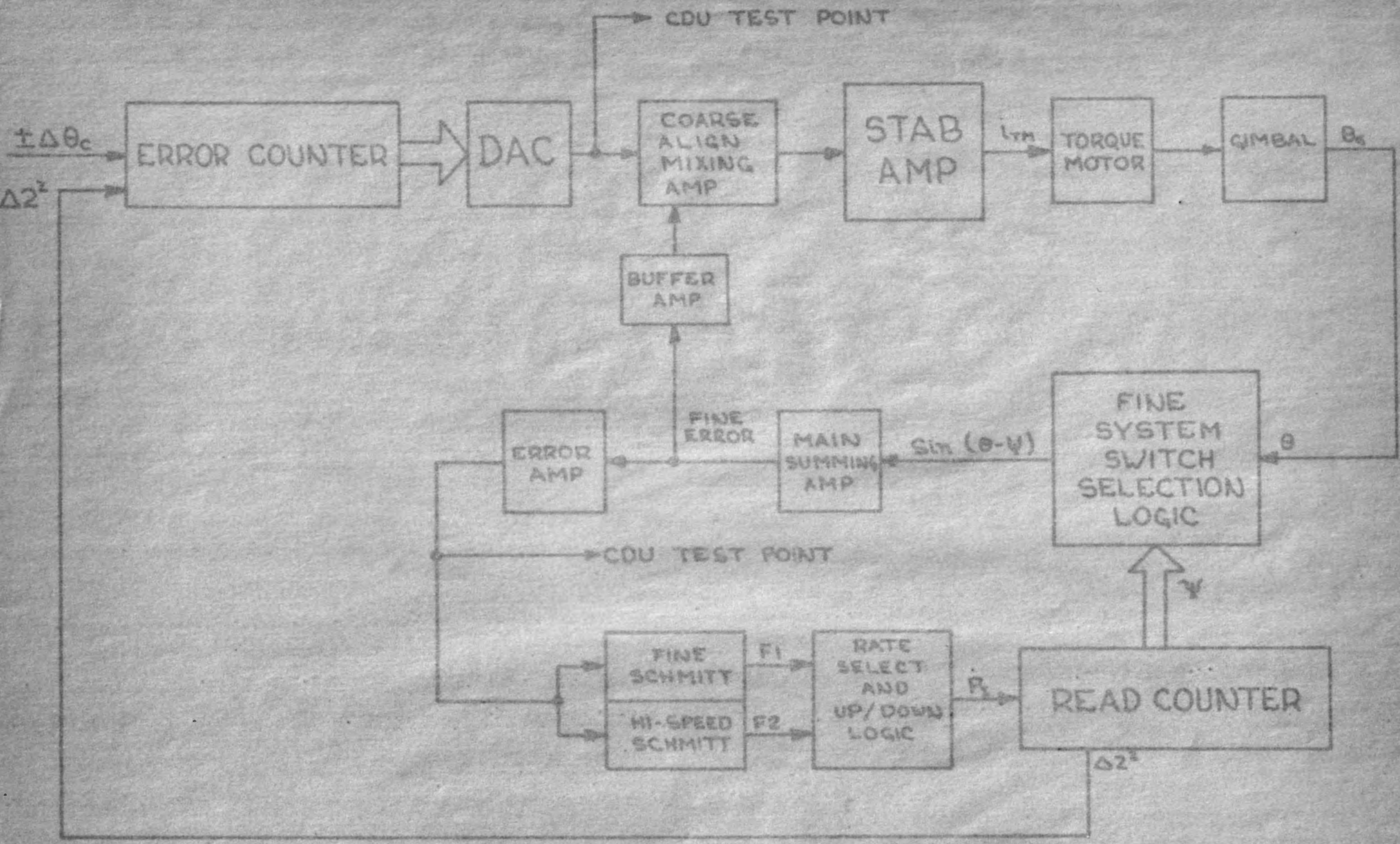
TABLE II

| RSS Summary of Errors | $1\sigma$ Errors |
|---|---|
| Error counter granularity | .0254° |
| DAC residual voltage | .0191° |
| Stab Amp Offset | .092° |
| Gimbal Stiction | .051° |
| Fine Error Feedback | .0245° |
| TOTAL $1\sigma$ error | .0356° |



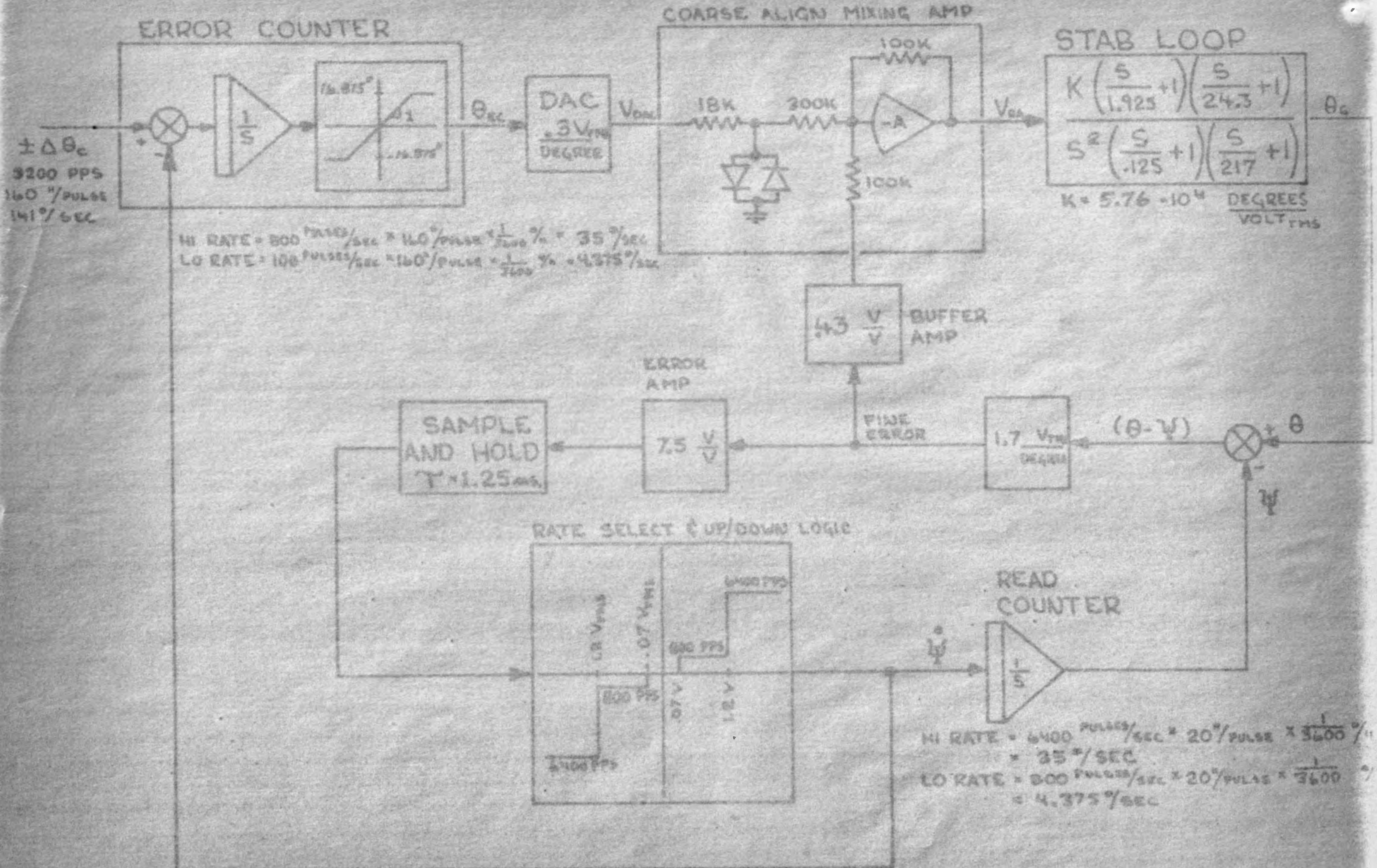
COMPUTER
ECDU
PSA
INNER D/A CONVERTER
MIDDLE D/A CONVERTER MODULE
OUTER D/A CONVERTER MODULE
CAGE RELAYS
IG STAB AMP INPUT
MG STAB AMP INPUT
OG STAB AMP INPUT
C/A INPUT RELAY
+28V
STAB AMP DEMOD REFERENCE RELAY
STAB AMP COARSE ALIGN RELAY ENABLE
STAB AMP DEMOD REFERENCE
COARSE ALIGN
MODE MODULE
ERROR COUNTER ENABLE
INNER C.A.
MIDDLE C.A.
OUTER C.A.
COARSE ALIGN MODING SIGNAL
ENABLES Δ2³ GIMBAL FEEDBACK PULSES TO BE COUNTED INTO THE ERROR COUNTER
CDU ZERO
INHIBITS P₂ PULSES FROM INCREMENTING THE READ COUNTER
ERROR COUNTER ENABLE
TO INCREMENT THE ERROR COUNTER — ABSENCE OF COMMAND ZEROS ERROR COUNTER
INNER
MIDDLE
OUTER
DIGITAL MODE MODULE


FIGURE 2



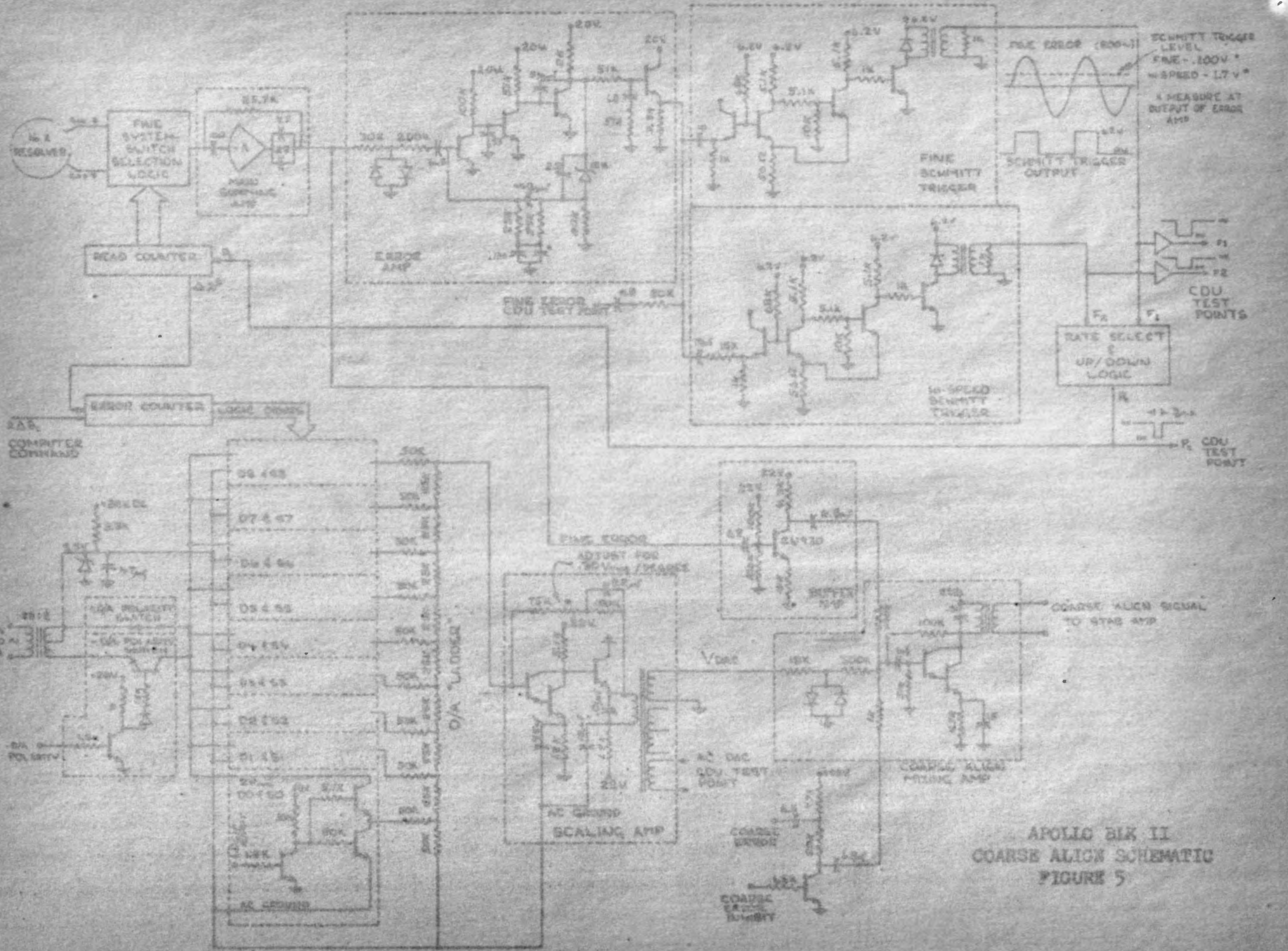

APOLLO
COARSE ALIGN
BLOCK DIAGRAM

FIGURE 3

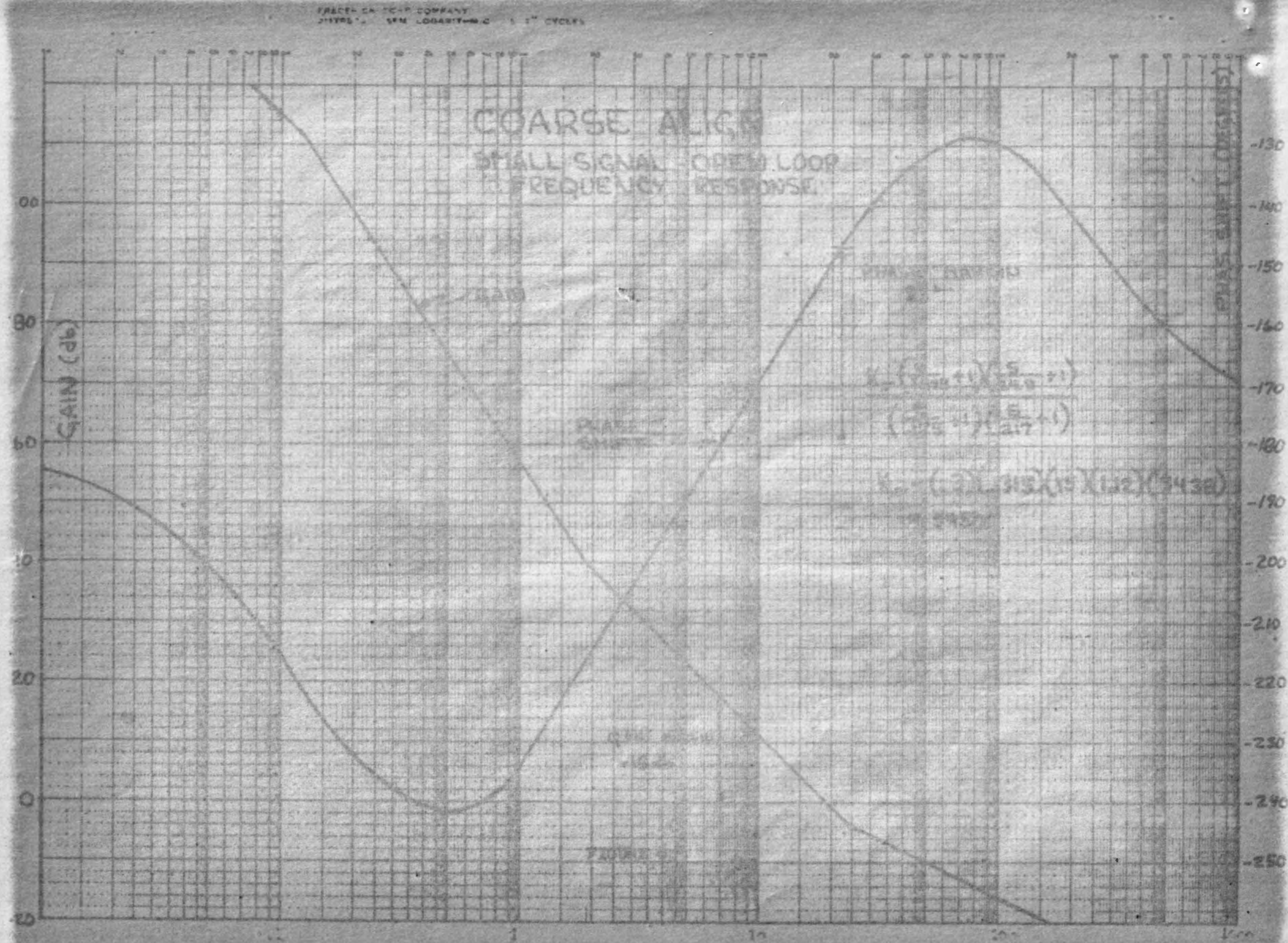



COARSE ALIGN
FUNCTIONAL BLOCK DIAGRAM

FIGURE 4




APOLLO BLK II
COARSE ALIGN SCHEMATIC
FIGURE 5



COARSE ALIGN
SMALL SIGNAL OPEN LOOP
FREQUENCY RESPONSE
GAIN (db)
PHASE SHIFT (DEGREES)
GAIN
PHASE SHIFT
80
60
20
0
-130
-140
-150
-160
-170
-180
-190
-200
-210
-220
-230
-240
-250
1
10

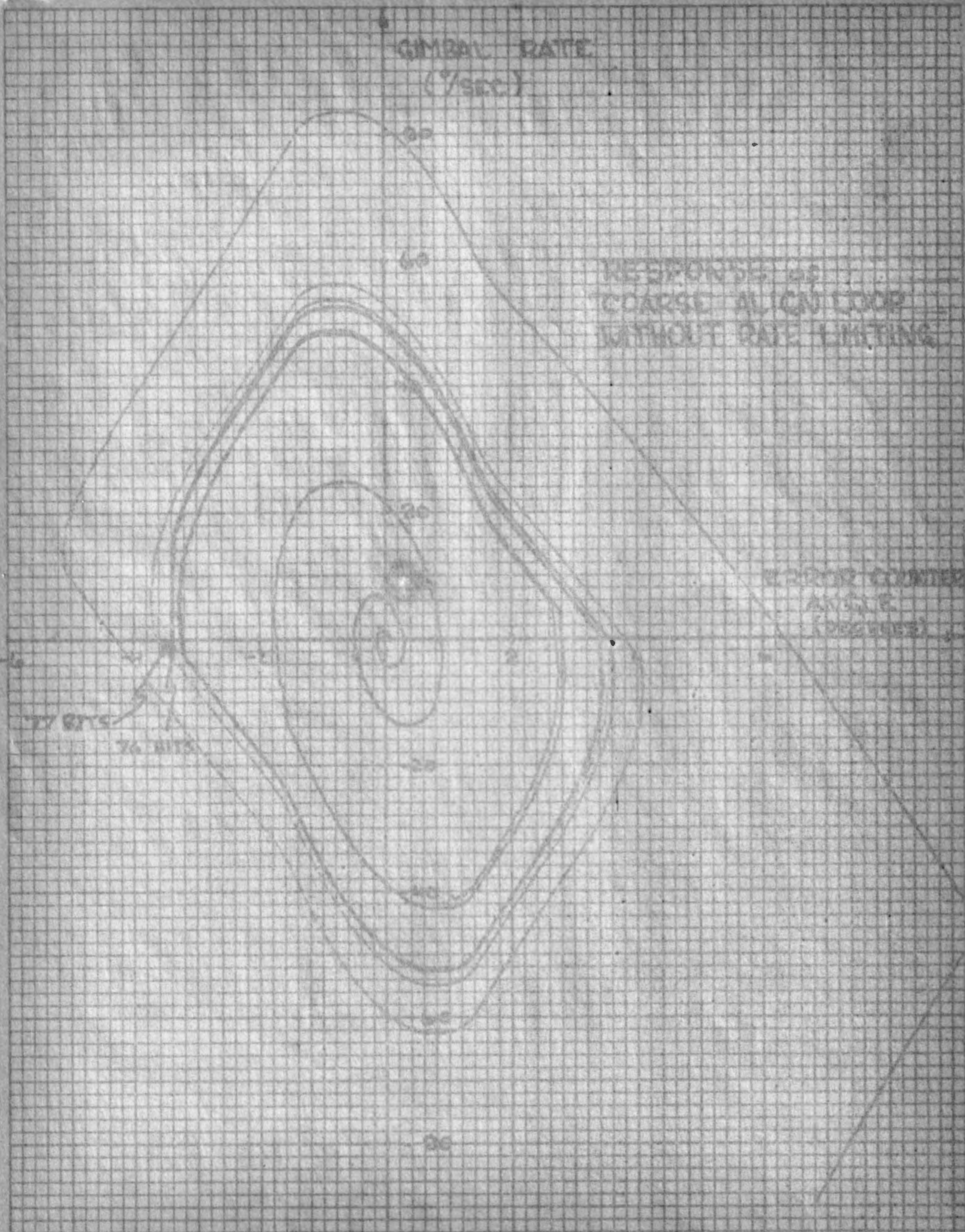



FIGURE 7

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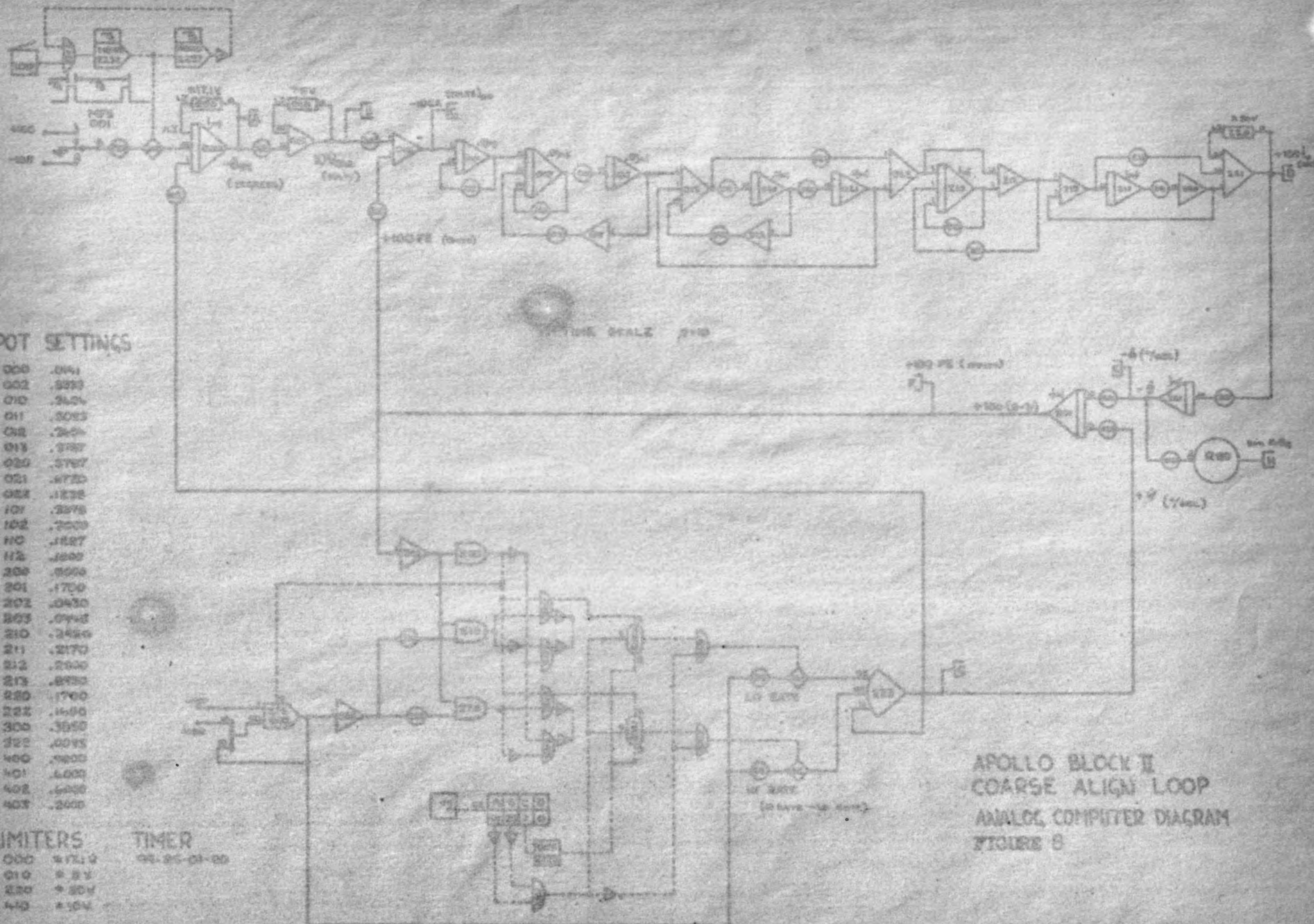


## POT SETTINGS

| | |
|---|---|
| 000 | .0141 |
| 002 | .3330 |
| 010 | .2404 |
| 011 | .3083 |
| 012 | .2404 |
| 013 | .1787 |
| 020 | .3767 |
| 021 | .4720 |
| 022 | .1838 |
| 101 | .3376 |
| 102 | .7000 |
| 110 | .1827 |
| 112 | .1000 |
| 200 | .8000 |
| 201 | .1700 |
| 202 | .0430 |
| 203 | .0443 |
| 210 | .3420 |
| 211 | .2170 |
| 212 | .2000 |
| 213 | .8950 |
| 220 | .1700 |
| 222 | .1400 |
| 300 | .3850 |
| 322 | .0095 |
| 400 | .9800 |
| 401 | .4000 |
| 402 | .6000 |
| 403 | .2000 |

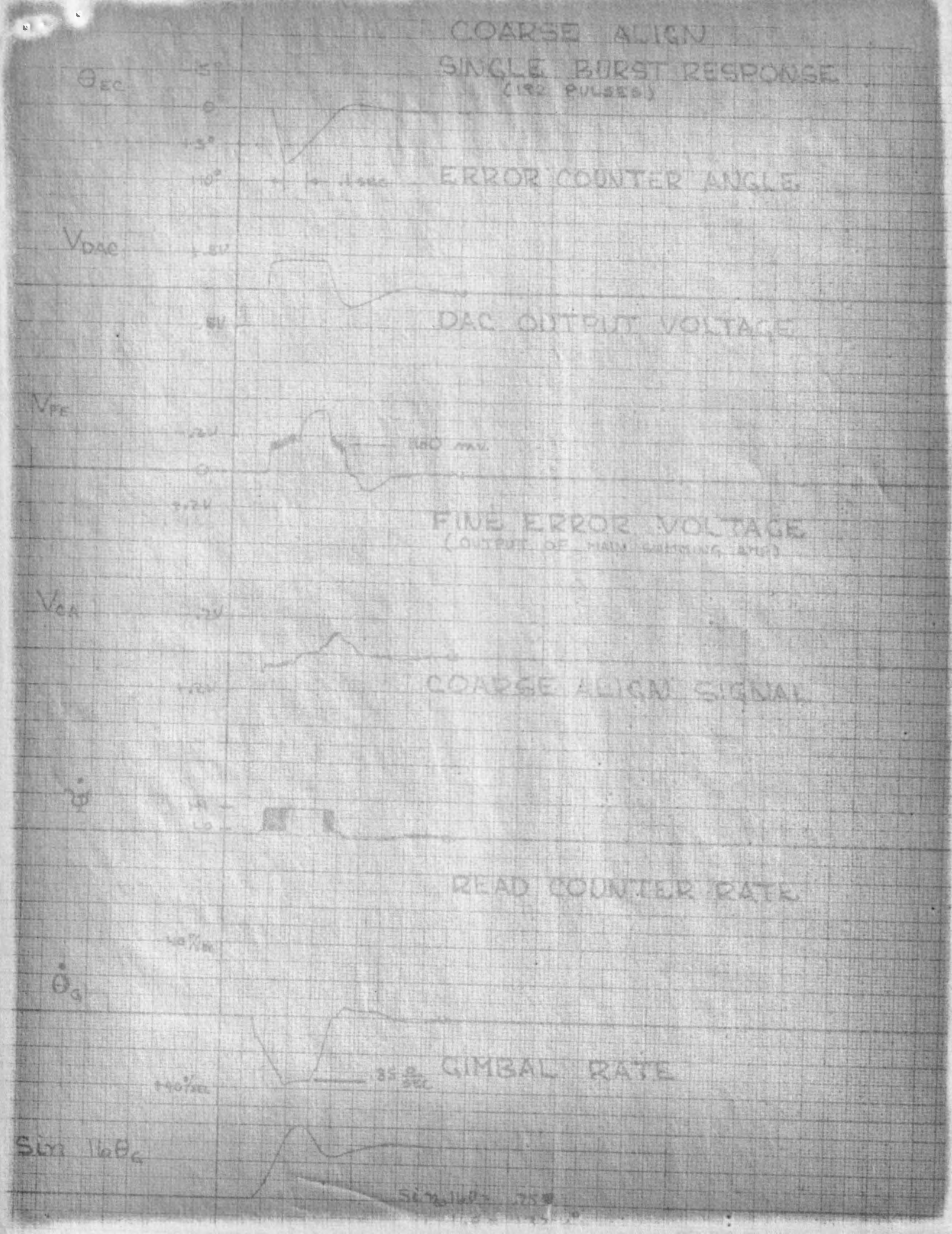
## LIMITERS

| | |
|---|---|
| 000 | ±17.2 |
| 010 | ± 8V |
| 220 | ± 20V |
| 440 | ± 10V |

## TIMER

98-95-01-00

APOLLO BLOCK II
COARSE ALIGN LOOP
ANALOG COMPUTER DIAGRAM
FIGURE 8



COARSE ALIGN
SINGLE BURST RESPONSE
(192 PULSES)
ERROR COUNTER ANGLE
DAC OUTPUT VOLTAGE
FINE ERROR VOLTAGE
COARSE ALIGN SIGNAL
READ COUNTER RATE
GIMBAL RATE

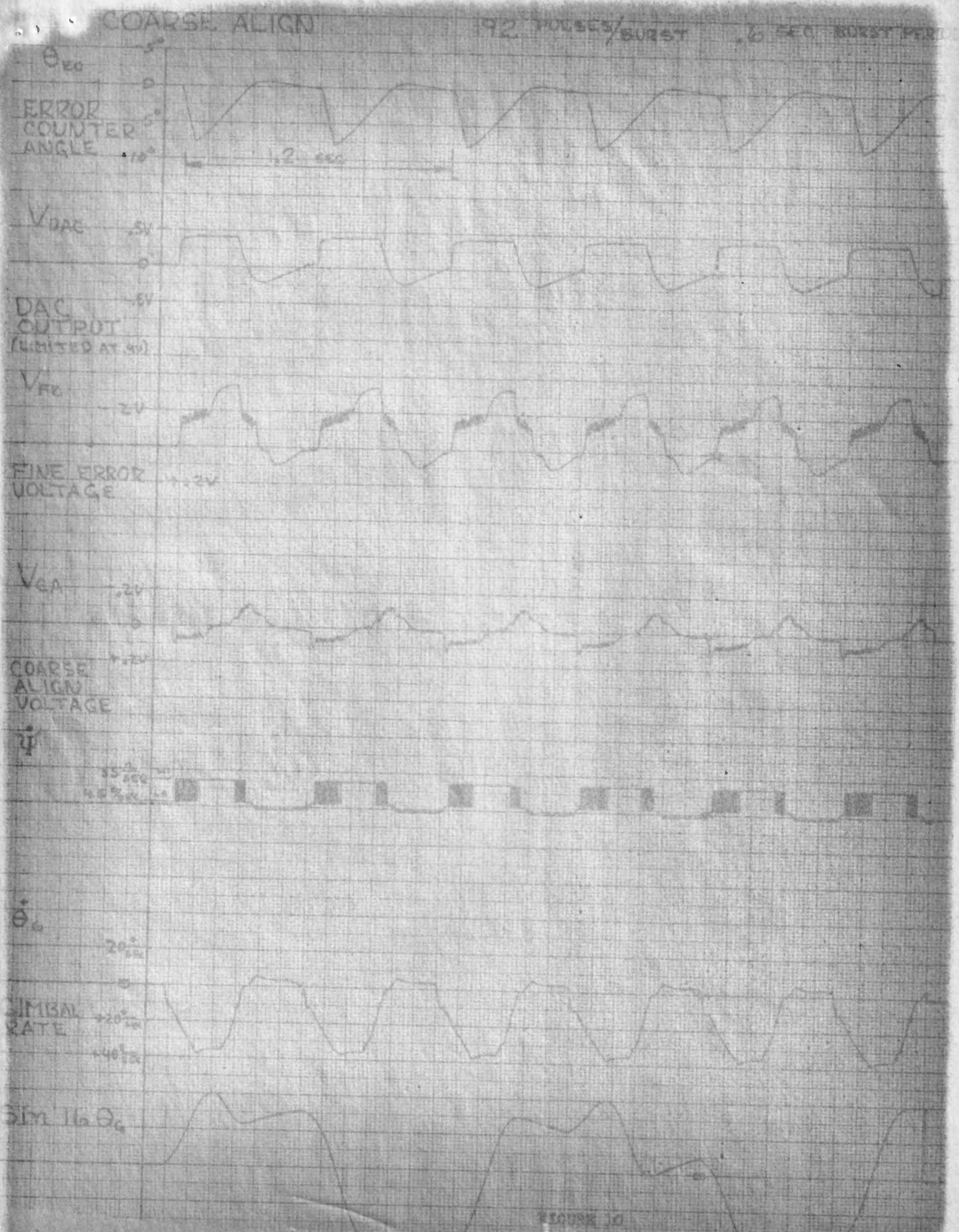

COARSE ALIGN
192 PULSES/BURST
.6 SEC BURST PERIOD
θEC
-5°
0
ERROR COUNTER ANGLE
+5°
+10°
1.2 sec
VDAC
.5V
0
-.5V
DAC OUTPUT (LIMITED AT .5V)
VFE
-.2V
FINE ERROR VOLTAGE
+.2V
VCA
-.2V
0
+.2V
COARSE ALIGN VOLTAGE
Ψ̇
55°/sec
45°/sec
θ̇G
20°/sec
0
GIMBAL RATE
+20°/sec
+40°/sec
GIM 16 θG

FIGURE 10

COARSE ALIGN 64 PULSES/BURST

.256 SEC BURST PERIOD