APOLLO ENGINEERING MEMORANDUM AP-M #4544

27 November 1964
Revision A

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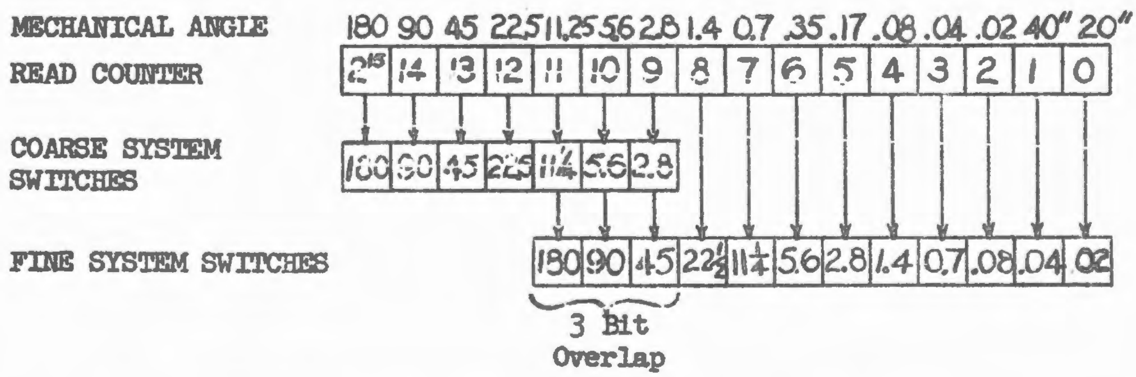
FROM: Mr. P. Grant

SUBJECT: THE COARSE SYSTEM OF THE ELECTRONIC COUPLING DATA UNIT (ECDU), (Paper II)

This is the second of a series of papers describing the electronic CDU. In this paper the coarse system will be explained and an hour talk given on Monday, October 5, 1964 at 2:00 PM in Conference Room #3.

The coarse system utilizes the seven most significant bits of the read counter. The relationship of the coarse and fine systems to the read counter and mechanical orientation is depicted in Figure 1 below.



READ COUNTER RELATIONSHIP WITH COARSE AND FINE SYSTEMS

FIGURE 1

A three bit overlap of the coarse and fine systems is used to obtain a smooth transfer from one system to the other.

An explanation of the coarse system will be given with reference to the enclosed block diagram. The coarse system resolver has a single speed with a 1:1 transformation ratio. It's primary is excited by the 28 V rms 800 cycle reference. The secondary of the resolver, which is the source of the sin Θ and cos Θ functions, excite the input transformers T1 and T2. (See the enclosed block diagram.) T3 is excited by the 28 V rms 800 cycle reference and all three input transformers have a transformation ratio of 28:5. Hence, the maximum voltage ever available at the secondary of the input transformers is 5 V rms. All angle information is contained in the amplitude of the sin Θ and cos Θ signals and their phase with respect to the 800 cycle reference. For example: With Θ equal to 150°, sin Θ at the secondary of T1 is equal to (5 V rms) (sin 150°) = 2.5 V rms and in phase with the 800 cycle reference. The cos Θ signal would be equal to (5 V rms) (cos 150°) = -4.33 V rms. The minus sign indicates that the signal is out of phase with the 800 cycle reference.

The functions sin Θ and cos Θ are switched through attenuation resistors (values of sin ψ and cos ψ) so that they are always out of phase with respect to each other at the summing junction. This is consistent with the system's nulling identity,

$$(1) \quad \pm \sin(\Theta - \psi) = \pm \sin\Theta \cos\psi \mp \cos\Theta \sin\psi$$

where Θ is the resolver angle and ψ the angle of the ECDU represented by the accumulation of bits in the seven most significant stages of the read counter. (See Figure 1.) Both phases of the input signals are available by use of the center tapped input transformers. The attenuated sin Θ and cos Θ voltages have approximately the same amplitude at the summing junction where they are summed together. The resultant voltage is nulled out by summing it with voltage increments of proper phase supplied by the ladder.

Switching to the appropriate attenuation resistors in the system is accomplished by switches S1 through S12. An explanation of the switching theory can best be accomplished by an illustrative example with reference to the enclosed coarse switching diagram and block diagram. Assume Θ, the resolver angle, is at an orientation of 28.1° (22.5° + 5.6°). By referring to the coarse switching diagram it is found that switches S3, S5 and the ladder are actuated. This is accomplished by the accumulation of bits in the read counter with bits in stages 2^{12} and 2^{10} corresponding to 22.5° and 5.6°. (See Figure 1.) The voltage at the secondary of T1 is equal to,

$$(5 \text{ V rms})(\sin 28.1°) = 2.36 \text{ V rms}$$

and that at the secondary of T2,

$$(5 \text{ V rms})(\cos 28.1°) = 4.41 \text{ V rms}.$$

With S3 actuated, the voltage at the secondary of T1 (2.36 V rms) is attenuated by a factor equivalent to the cos 22.5° and the result at the summing junction is 2.18 V rms and in phase with the reference. With S5 actuated the cos function is inverted by T2 and attenuated by a factor equivalent to the sin 22.5° and the result at the summing junction is -1.69 V rms, the minus sign indicating it being out of phase with the reference. The summation of the sin function and cos function at the summing junction is therefore, 2.18 -1.69 = 0.49 V rms and in phase with the reference. To null the system this in phase voltage must be summed with an out of phase signal. The out of phase signal is supplied by the ladder which is composed of switches. S10, S11 and S12 which in turn are controlled by stages 2^{11}, 2^{10} and 2^{9} of the read counter, respectively. With a bit in stage 2^{10}, S11 is actuated and an out of phase signal equivalent to (-5 V rms) (sin 5.6°) =-0.49 V rms is available from the reference at the summing junction and a null is accomplished.

A brief explanation of the operation of switch S9, which provides a reference signal to the summing junction, is in order. When the angle θ lies in those segments of the coarse switching diagram where S9 is actuated, the resultant voltage of the summation of the sin and cos functions at the summing junction is an out of phase signal. If the ladder bits, which provide out of phase voltage increments were to be summed with the out of phase signal at the summing junction, this would aggravate the unnulled condition. An in phase signal is required at the summing junction with which the ladder signals can be summed to obtain a null. This required in phase signal is provided by switch S9 and the + reference side of the transformer T3. It's effect is to add to the out of phase resultant from the sin θ and cos θ function and thus invert the voltage to an in phase signal so that out of phase ladder signals can accomplish a null.

An example illustrating the above operation will clarify the process. Assume θ is equal to 239.1° (225° + 11.25° + 2.8). Referring to the coarse switching diagram, it is determined that S2, S8, S9 and the ladder are actuated. The five voltages being summed at the summing junction are listed below. Refer to the enclosed block diagram

(S2)	(-5 V rms)	(sin 239.1°)	(cos 67.5°)	=	1.64 V rms
(S8)	(5 V rms)	(cos 239.1°)	(sin 67.5°)	=	-2.37 V rms
(S9)		(5 V rms)	(sin 22.5°)	=	1.91 V rms
(S10)		(-5 V rms)	(sin 11.25)	=	-0.98 V rms
(S12)		(-5 V rms)	(sin 2.8°)	=	-0.25 V rms

The minus signs in front of the 5 V rms signifies the out of phase portion of the input transformers are being utilized. The anticipated out of phase resultant of the sin and cos functions from S2 and S8 is realized and equivalent to -0.73 V rms. The remaining signals from the reference source provides the necessary in phase signal (0.68 V rms) to obtain a null.

With the system nulled the error voltage at the output of the summing amplifier, referred to as the coarse error signal, is less than 0.7 V rms. The error detector (Coarse Schmitt) will fire nominally at 1.33 V p-p and initiate the rate select logic in the error counter and logic module (EC + L) to send pulses at high speed (12.8 KC) to the read counter. An in phase Schmitt signal will cause the read counter to count down and an out of phase Schmitt will count the read counter up.

With the system not nulled the error signal will cause an in phase or out of phase Schmitt signal to occur. The Schmitt signal will effect a change in the read counter by initiating pulses from the EC and L module. The counter in turn will change the switching configuration of the system, choosing different values of attenuation ($\sin \psi$ and $\cos \psi$) until such time when $\Theta = \psi$ and the system will be nulled.

The next paper will present and explain "The Power Supply and Common Circuits of the Electronic Coupling Data Unit".

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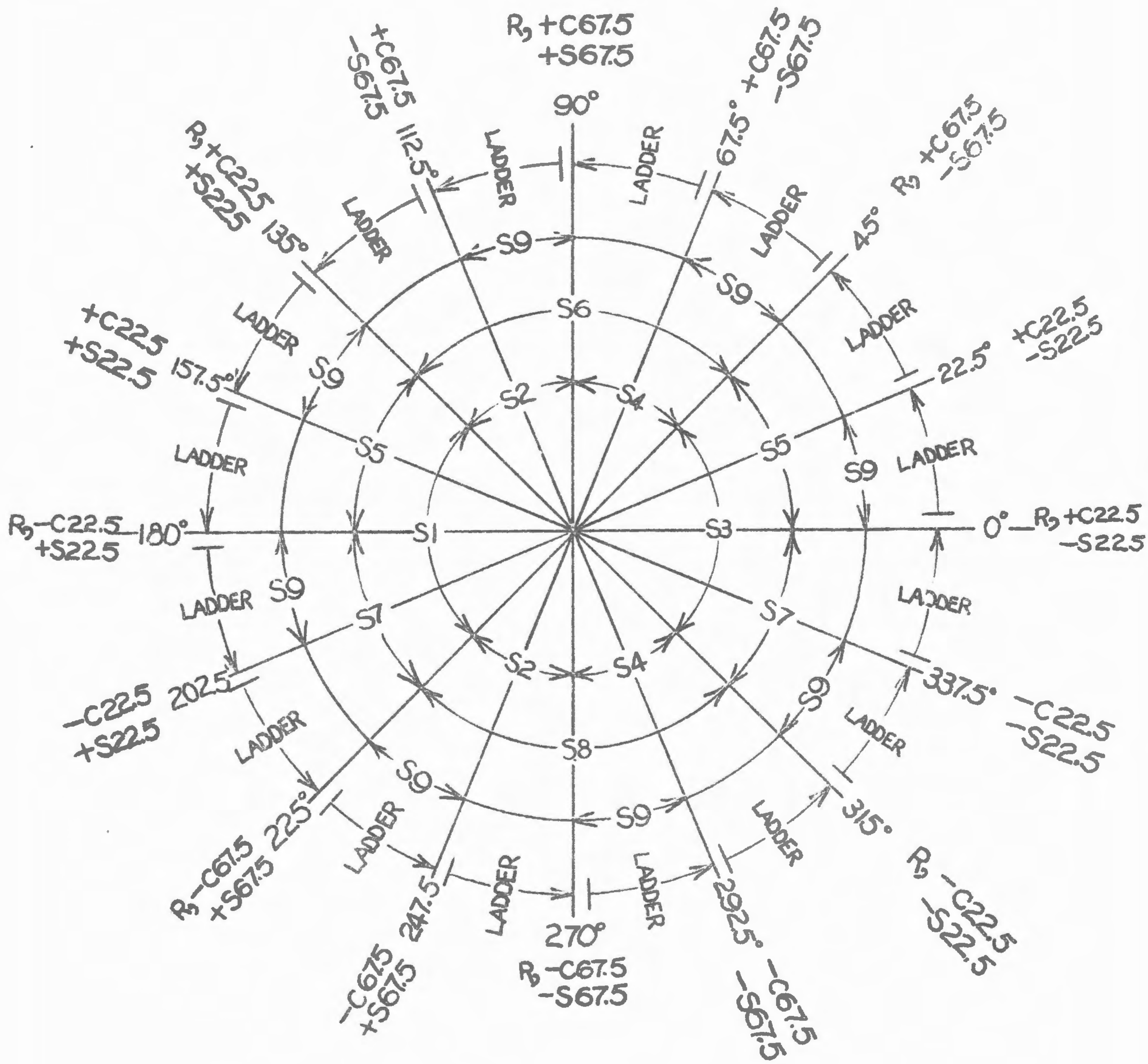
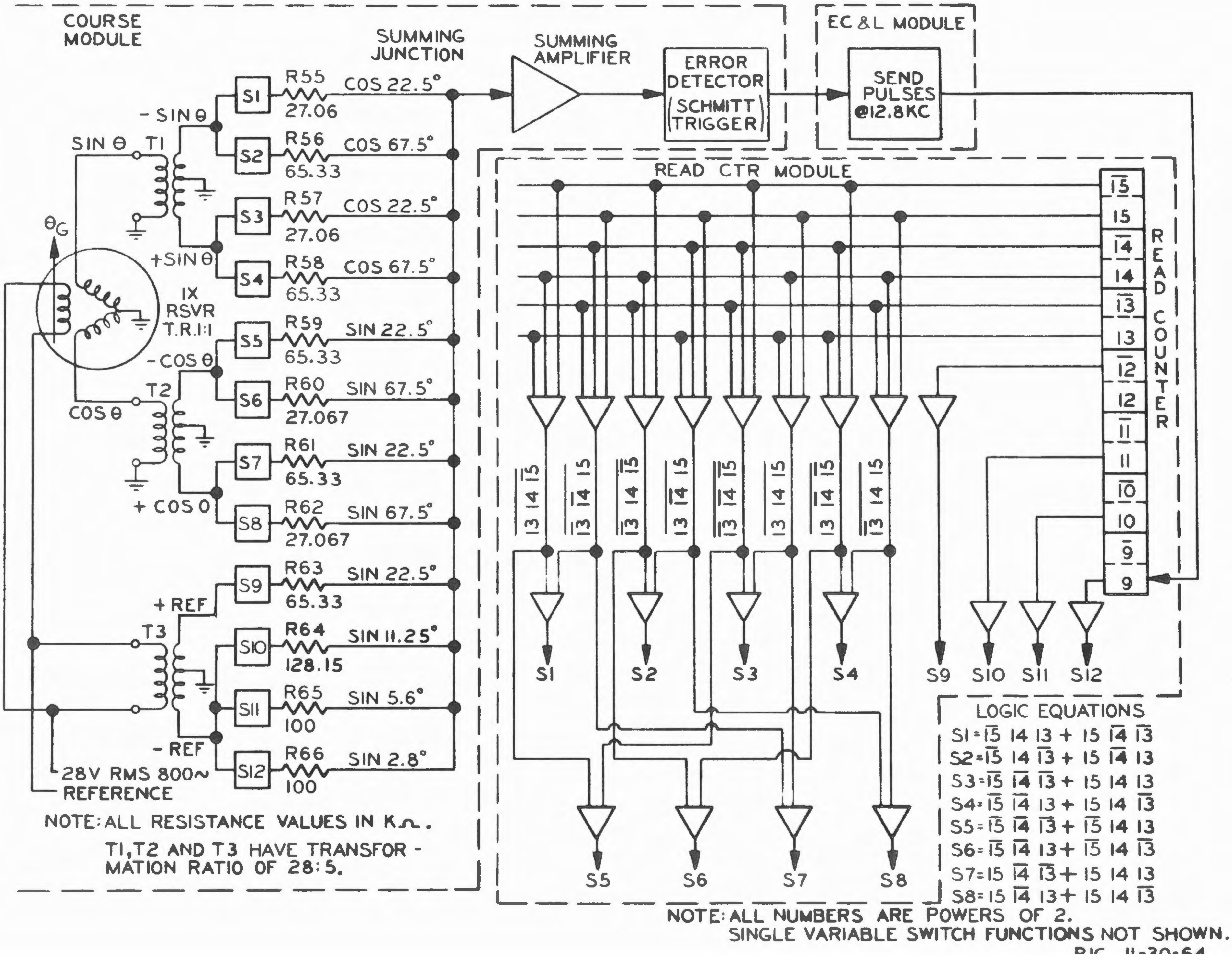


COARSE SWITCHING DIAGRAM

11/27/64
P.J.G.

ELECTRONIC COUPLING DATA UNIT
COURSE SYSTEM BLOCK DIAGRAM



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