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APOLLO ENGINEERING MEMORANDUM AP-M #4927

13 November 1964

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FROM: Mr. P. Grant

SUBJECT: THE FINE SYSTEM OF THE ELECTRONIC COUPLING DATA UNIT (ECDU) Part II (Paper V)

This is the fifth of a series of papers describing the electronic CDU. This paper will describe the Main Summing Amplifier Module and attempt to integrate its' functions with those of the Quadrant Selector Module in order to present a complete picture of the fine system. An hour long talk in support of this paper will be given on Friday, November 13, 1964 at 2:00 in the SAT Conference Room.

Apollo Engineering Memo AP-M #4850 entitled The Fine System of the ECDU, Part I should be reviewed prior to studying this paper. That memo described how the resolver signals were phased and switched to the appropriate attenuation resistors at the inputs to the main summing amplifier, sin and cos amplifiers by the operation of switches S1 through S8. Refer to the block diagram. The sin and cos amplifier, A5 and A6 respectively and six switches S9 through S14 are used to implement the reference equation

$$(1) \quad \cos(\theta - \psi) = \sin\theta \sin\psi + \cos\theta \cos\psi$$

Cos $(\theta - \psi)$ is an internally generated reference which is used to excite the ladder network.

In the development of the system equation

$$(2) \quad + \sin(\theta - \psi) = \pm \sin\theta \cos\psi \mp \cos\theta \sin\psi$$

It was necessary to phase the sin θ and cos θ signals from the resolver so that they were always out of phase with respect to each other. In solving the reference equation (1) it becomes necessary to rephase the out of phase sin θ and cos θ signals so that they are always in phase and consistent with equation (1). The rephasing is accomplished by amplifiers A5 and A6 and switches S9 through S14. The logic equations for the switches are listed on the block diagram and translated to electrical degrees by the Fine System Hardware Switching Diagram Figure 2.

There are two outputs from each of the sin and cos amplifiers, however, only one of the four is active at all times. Switches S11 and S14 switch the output of A5 to the input of A6 and the output of A6 to the input of A5, respectively. Hence, when S11 is closed (quadrants I and III) the output is taken from A6 and when S14 is closed (quadrants II and IV) the output is taken from A5. The effect is to invert the out of phase signal with respect to the 800 cycle reference from the quadrant selector to an in phase voltage, sum it with the other in phase signal of the quadrant selector and invert the resultant to an out of phase voltage at the output of A5 or A6. Switches S9 and S10 alternate on and off every 11 1/4 degrees in the second and fourth quadrants (S14 is closed) and S12 and S13 alternate on and off every 11 1/4 degrees in the first and third quadrants (S11 is closed). Hence, one output is always present at the input to the ladder amplifier and to one of the -11 1/4 bits or bias bits at the main summing junction. The input to the ladder amplifier is always an out of phase signal and its' output, the function cos ($\theta - \psi$), is thus always an in phase signal with respect to the 800 cycle reference and of approximately constant amplitude.

At this point the reader should have a "feel" for the signals that are being summed at the main summing junction. To recapitulate, two signals out of phase with respect to each other from the quadrant selector are always present at the main summing junction by the operation of switches S1 through S4. Secondly, there is always one input from A5 or A6 providing an out of phase voltage and finally, if ψ (the angle contained in the read counter) is anywhere between the 11 1/4 degree divisions, in phase voltage from the ladder is injected proportional to the accumulation of bits in the seven least significant stages of the read counter. The result, with the aid of the quadrature rejection network, is about a six millivolt RMS null at the output of the main summing amplifier.

An attempt will be made to "talk" through the integrated operation of the fine system. This entails a description of the individual voltages being summed at the main summing junction. The crux of the operation lies in the switching in or absence of the -11 1/4 bit and the phase of the resultant voltage from the quadrant selector. If ψ, the angle contained in the read counter, is between 0 and 11 1/4 degrees a relatively small sin θ signal is inverted in the quadrant selector, being in the first quadrant, and attenuated by a factor equivalent to the cos 11 1/4° at the main summing amplifier. The relatively large cos θ signal, being in phase, is attenuated by a factor equivalent to the sin 11 1/4° at the main summing junction. The resultant of these two signals from the quadrant selector is an in phase voltage which must be summed with an out of phase voltage to obtain a null. The ladder network, being controlled by the seven least significant stages of the read counter provides in phase voltage proportional to the difference between the 11 1/4 degree divisions and the angle ψ progressing in a counter clockwise direction in Figure 2. If in phase voltage from the ladder were summed with the resultant in phase voltage from the quadrant selector the effect would aggravate the unnulled condition. The necessary out of phase voltage necessary to accomplish a null is provided by the -11 1/4 bit input. The effect is to switch in this -11 1/4 bit out of phase voltage and null the resultant out of phase voltage with increments of in phase voltage from the ladder at the main summing junction.

The -11 1/4 bit voltage is always out of phase with respect to the 800 cycle reference and of constant amplitude. Either the -11 1/4 bit signal or the bias bit signal is always present at the main summing junction. These bias bit signals are used to minimize the error generated by the implementation of the cos ($\theta - \psi$) function. A similar bias is provided in the gain of the ladder amplifier ($\frac{25.76}{25}$) when the -11 1/4 bit signals are switched in.

If ψ is between 11 1/4 and 22 1/2 electrical degrees, S12 is open (the -11 1/4 bit is absent) and S13 is closed applying the bias bit to the main summing junction. The resultant voltage from the quadrant selector is an out of phase voltage at the main summing junction. The ladder bits provide increments of in phase voltage to null out this out of phase voltage and the bias bit provides minimization of error.

As ψ becomes greater the operation described above repeats with S12 and S13 alternating on and off. When ψ progresses to the second quadrant the operation continues with switches S9 and S10 alternating on and off. In the third quadrant S12 and S13 become operational and in the fourth quadrant switches S9 and S10 regain control.

This paper was scheduled to explain the quadrature rejection circuitry, however, the writer feels that a sufficient amount of material is included in this memo and the quadrature rejection network will be presented in a future paper. The next paper of this series is entitled, The Digital to Analog Converter of the Electronic Coupling Data Unit.

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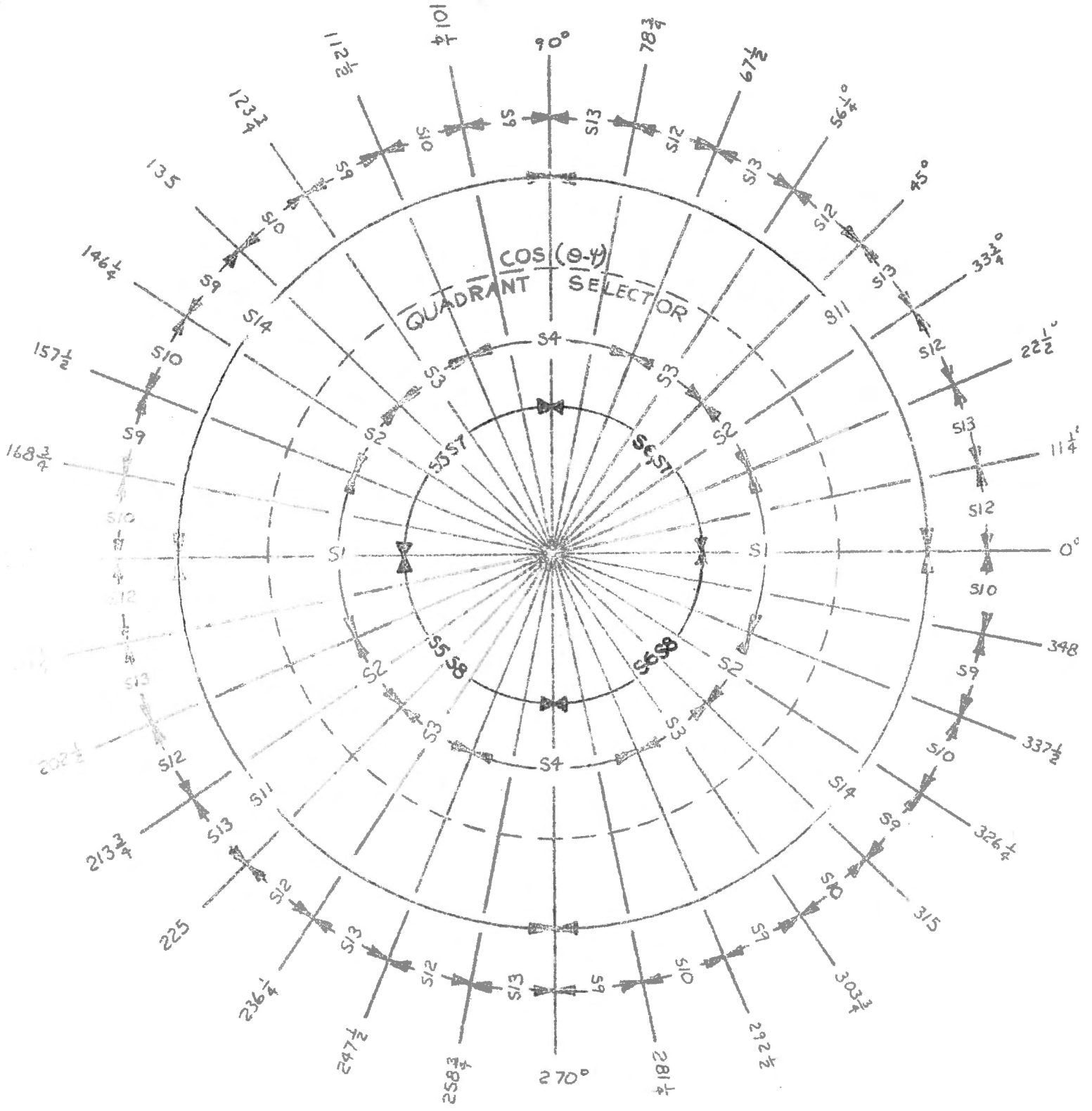
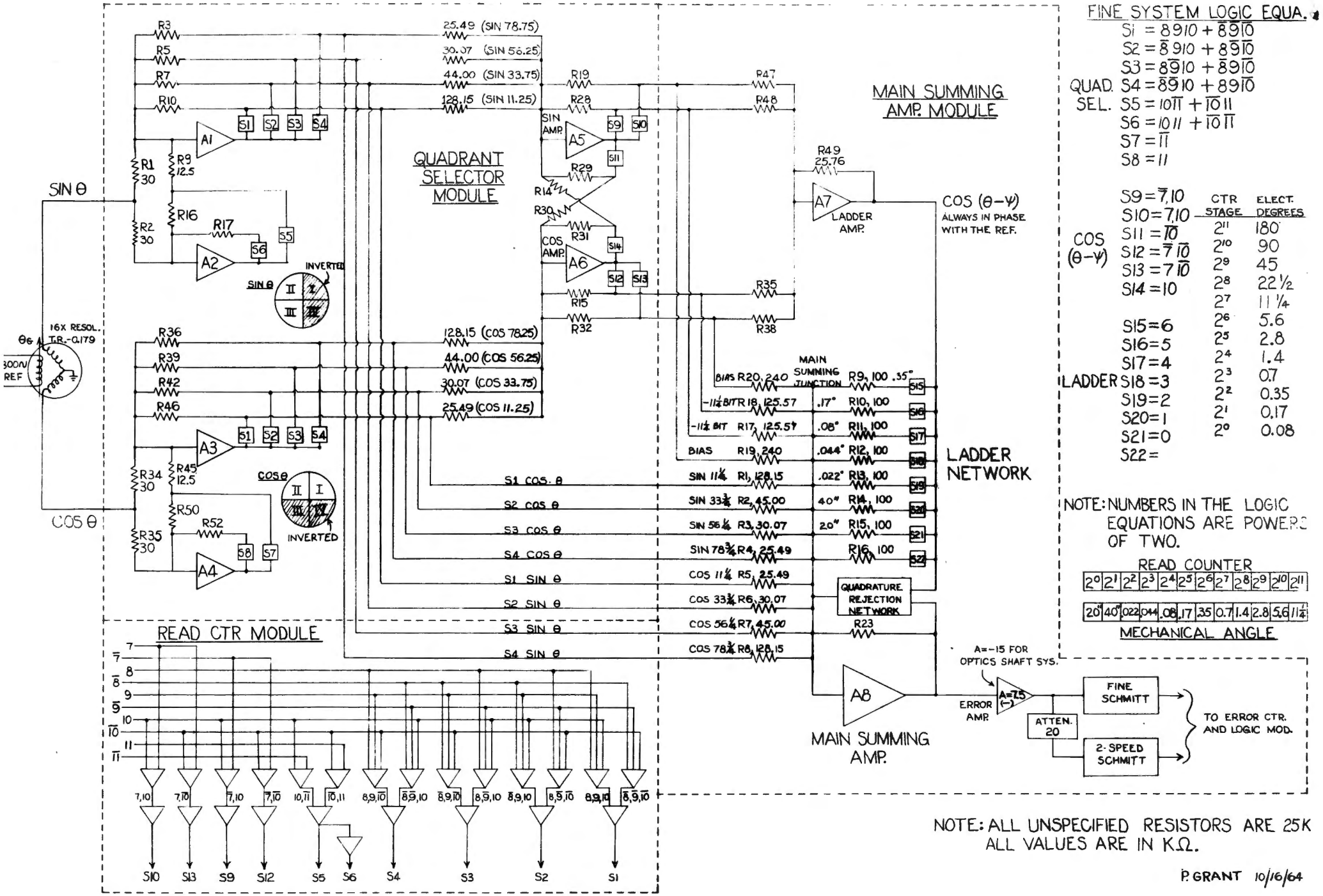


FINE SYSTEM HARDWARE
SWITCHING DIAGRAM

ECDU FINE SYSTEM BLOCK DIAGRAM



NOTE: SINGLE VARIABLE SWITCH FUNCTIONS NOT SHOWN.

FINE SYSTEM LOGIC EQUA.

$S1 = 8\,9\,10 + \bar{8}\,\bar{9}\,\bar{10}$
$S2 = \bar{8}\,9\,10 + 8\,\bar{9}\,\bar{10}$
$S3 = 8\,\bar{9}\,10 + \bar{8}\,9\,\bar{10}$
QUAD. SEL. $S4 = \bar{8}\,\bar{9}\,10 + 8\,9\,\bar{10}$
$S5 = 10\,\bar{11} + \bar{10}\,11$
$S6 = 10\,11 + \bar{10}\,\bar{11}$
$S7 = \bar{11}$
$S8 = 11$

COS (θ-Ψ)
$S9 = \bar{7},10$
$S10 = 7,10$
$S11 = \bar{10}$
$S12 = \bar{7}\,\bar{10}$
$S13 = 7\,\bar{10}$
$S14 = 10$

LADDER
$S15 = 6$
$S16 = 5$
$S17 = 4$
$S18 = 3$
$S19 = 2$
$S20 = 1$
$S21 = 0$
$S22 =$

CTR STAGE	ELECT. DEGREES
2^{11}	180
2^{10}	90
2^{9}	45
2^{8}	22½
2^{7}	11¼
2^{6}	5.6
2^{5}	2.8
2^{4}	1.4
2^{3}	0.7
2^{2}	0.35
2^{1}	0.17
2^{0}	0.08

NOTE: NUMBERS IN THE LOGIC EQUATIONS ARE POWERS OF TWO.

READ COUNTER

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	2^8	2^9	2^{10}	2^{11}
20'	40'	022.044	.08	.17	.35	0.7	1.4	2.8	5.6	11¼	

MECHANICAL ANGLE

NOTE: ALL UNSPECIFIED RESISTORS ARE 25K ALL VALUES ARE IN KΩ.

P. GRANT 10/16/64