G. Silver (MIT)

APOLLO ENGINEERING MEMORANDUM AP-M NO. 5009

25 November 1964

TO: Distribution

FROM: Mr. P. Grant

SUBJECT: THE QUADRATURE REJECTION NETWORK OF THE ELECTRONIC COUPLING DATA UNIT (ECDU). (PAPER VI)

This is the sixth of a series of papers describing the electronic CDU. This paper will explain the quadrature rejection network. An hour talk in support of this memo will be given on Monday, November 30, at 10:00 AM in the SAT conference room.

When the solution of the system equation

$$\pm \sin (\theta - \psi) = \pm \sin \theta \cos \psi \mp \cos \theta \sin \psi$$

is accomplished, the angle ψ of the ECDU, represented by the accumulation of bits in the read counter, equals the resolver angle θ to within forty seconds of arc and the system is said to nulled. At null the voltage at the output of the main summing amplifier is less than two bits of error signal or 2 x 6.39 m V rms = 12.78 m V rms. 6.39 m V rms is the theoretical least bit error voltage which correlates very closely to the measured value. This low null voltage can only be obtained with the aid of the quadrature rejection network shown in the enclosed schematic.

The effect of the quadrature rejection network is to accept the error voltage at the output of the main summing amplifier, demodulate it with the reference cos $(\theta - \psi)$ which has been phase shifted ninety degrees and integrate the result to a dc voltage. The dc voltage is then modulated (chopped) into a square wave and summed with the error voltage at the main summing junction which is 180° out of phase with the error voltage at the output of the main summing amplifier. The waveforms shown below give a pictorial presentation of the process. The resultant voltage of the summation of the error voltage and the square wave output of the quadrature rejection network is a signal rich in harmonics. These harmonics are filtered out by the 150 cycle band pass filter of the error amplifier before the error signal is detected by the Schmitt trigger.

WAVEFORMS OF QUADRATURE REJECTION NETWORK

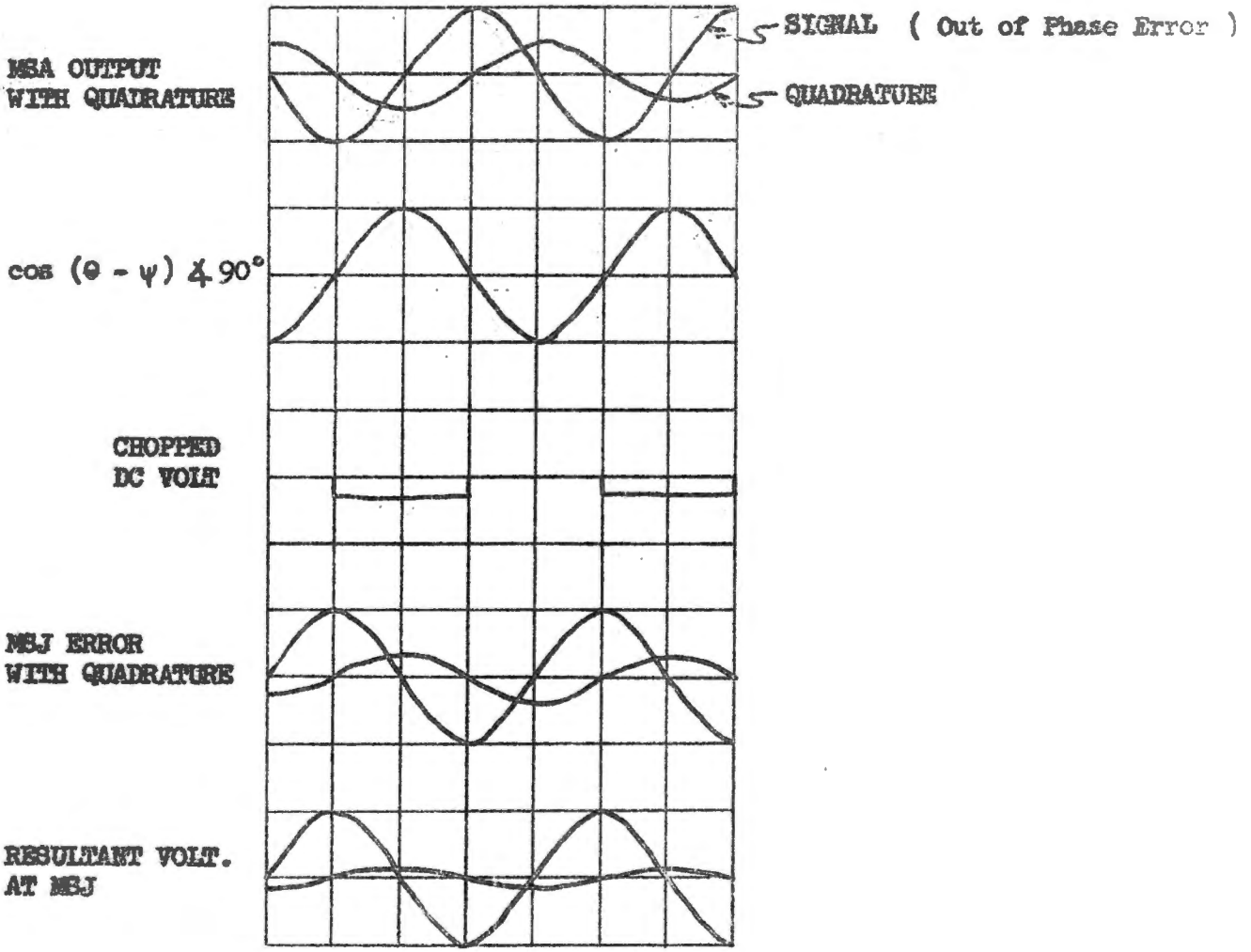
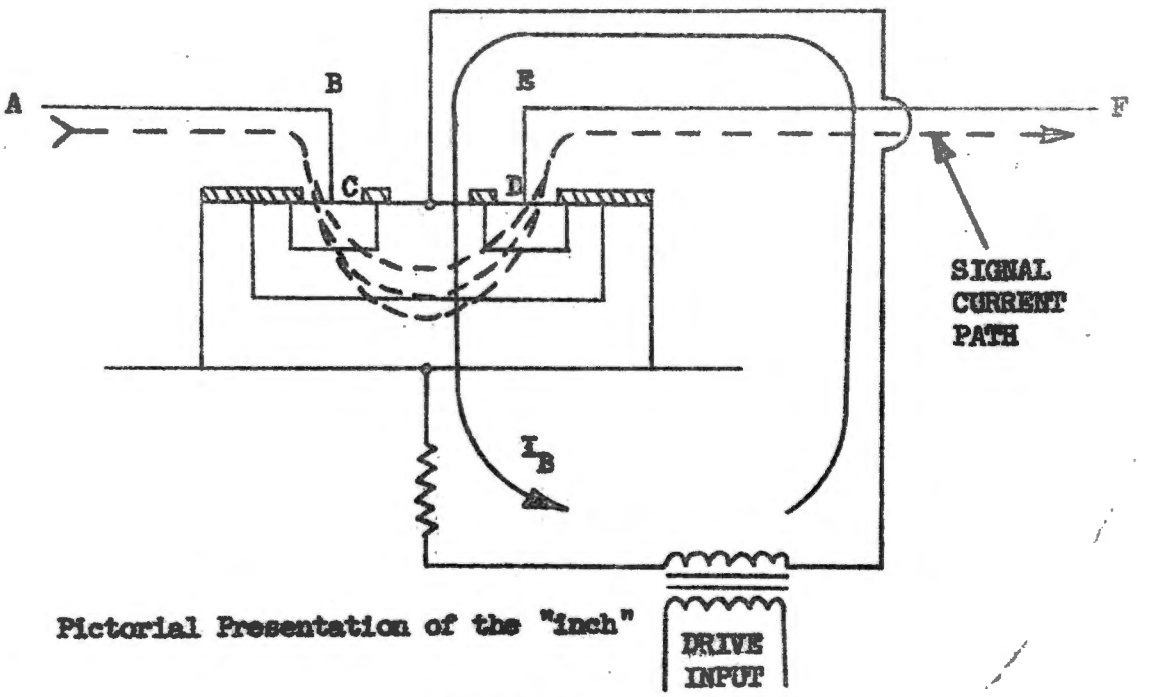


FIGURE 1

The demodulator, Q15, and modulator, Q16, utilize a fairly new semiconductor designated 3N68. The device is commonly referred to as an 'inch' which is a contraction for integrated chopper. Essentially, it is a switch which provides a low impedance path between emitters when the potential on its base is positive with respect to the collector. A pictorial representation of the inch is shown below.



Pictorial Presentation of the "inch"

FIGURE 2

The device is made by the oxide passivated, planar process and is contructed on a single dice of silicon. The device is designed to do the following:

1. Reduce the number of thermocouples in the signal path.

2. Eliminate the drive current from the signal path.

3. Reduce the total number of p-n junctions.

4. Reduce the possibility of thermal mismatch by having very closely spaced junctions.

5. Improve the stability of the chopper.

These objectives are accomplished in the following manner:

1. In Fig. 2, tracing the signal path through the chopper, the signal current flows into the emitter at point 'A', then through the points B, C, D, E, and F. The total number of thermocouples in the signal path (at points B, C, D, and E) are reduced from ten in the case of the matched pair chopper to four for the INCH. Also, since all the junctions are in the same package (TO-18 with four leads) a much closer temperature match can be achieved than if there were two different packages.

2. The signal current flows into the device at point C, across the emitter base junctions EB_1 and EB_2 (see Fig. 2) and out of point D. The drive current flows into the INCH at the base contact, across the collector base junction, and into the collector. This drive current, which is generally much larger than the signal current, does not generate a voltage gradient along the path of the signal current since the two current paths are normal to each other. Thus, variations in drive, or base current have negligible effects in generating IR drops in the signal path.

3. There is only one base-collector junction, compared to two in the matched pair chopper. This is an additional feature to ensure stability, since any change or degradation which may occur in the base-collector junction will tend to affect both 'Halves' of the INCH similarly, and the net effects on the offset voltages will tend to cancel. Thus, for this reason, as well as the advantages in stability of the passivated planar process, there is much more inherent stability built into this device than in the matched pairs of alloy transistors.

4. In order to reduce the effects of any possible thermal gradients, the two base-emitter junctions are made as close together as possible. Actual separation is in the order of 7 mils. This is obviously much closer spacing than can be achieved with separate transistors. Also, since there is only ONE base-collector junction, the possibility of thermally different base-collector junctions is eliminated.

5. The stability of V_0 is actually due to all of the above design features. This device can be temperature cycled, stored at elevated temperatures, run on life tests, and typical changes in V_0 will be in the order of a couple of microvolts. This represents orders of magnitude improvement over alloy, matched pairs.

In referring to the enclosed schematic of the quadrature rejection network, Q12 and Q13 comprise an amplifier with a voltage gain of approximately 165. Feedback is provided by C21 and R71 and dc bias stability is accomplished by R76, R72, R65 and their associated capacitors. Q14 is an emitter follower buffer with regeneration provided by C26 and R80. The output of the buffer is fed to the demodulator. The drive for the demodulator and modulator is the cos $(\theta - \psi)$ reference which has been phase shifted ninety degrees. The ninety degree phase shift is accomplished by Q18 and its feedback capacitor C18 which has an impedance of approximately 12K ohms at 800 cycles. With an input resistance of 24K the gain of this stage is set to about one half with a ninety degree phase shift. Q19 and T3 comprise a driver with negative feedback for Q19 provided by C30 and R89. The reference cos $(\theta - \psi)$ is 4.2 V rms when it is accepted by the phase shifter and at the secondary of T3 this reference has been attenuated to 2.1V rms and phase shifted ninety degrees.

When the voltage on the base of Q15 is positive with respect to its collector a low impedance path is provided between the two emitters E1 and E2. At this time capacitors C9 and C31 become charged to the instantaneous potential of emitter E1. In the case of an out of phase error signal at the output of the main summing amplifier, the voltage on capacitors C9 and C31 would be negative as shown in the

previous waveforms. With an in phase error at the main summing amplifier the charge on the capacitors would be a positive potential. The chopping is accomplished by Q16 which shorts the output to ground when activated (Note the polarity of the drive from T3). Q17 is an emitter follower buffer with regeneration provided by C33. The square wave output of the buffer is fed to the main summing junction through C34 and R62 to complete the loop back to the main summing amplifier.

The next exciting chapter of the series is entitled, 'The Digital to Analog Converter of the Electronic Coupling Data Unit'.

Paul Grant

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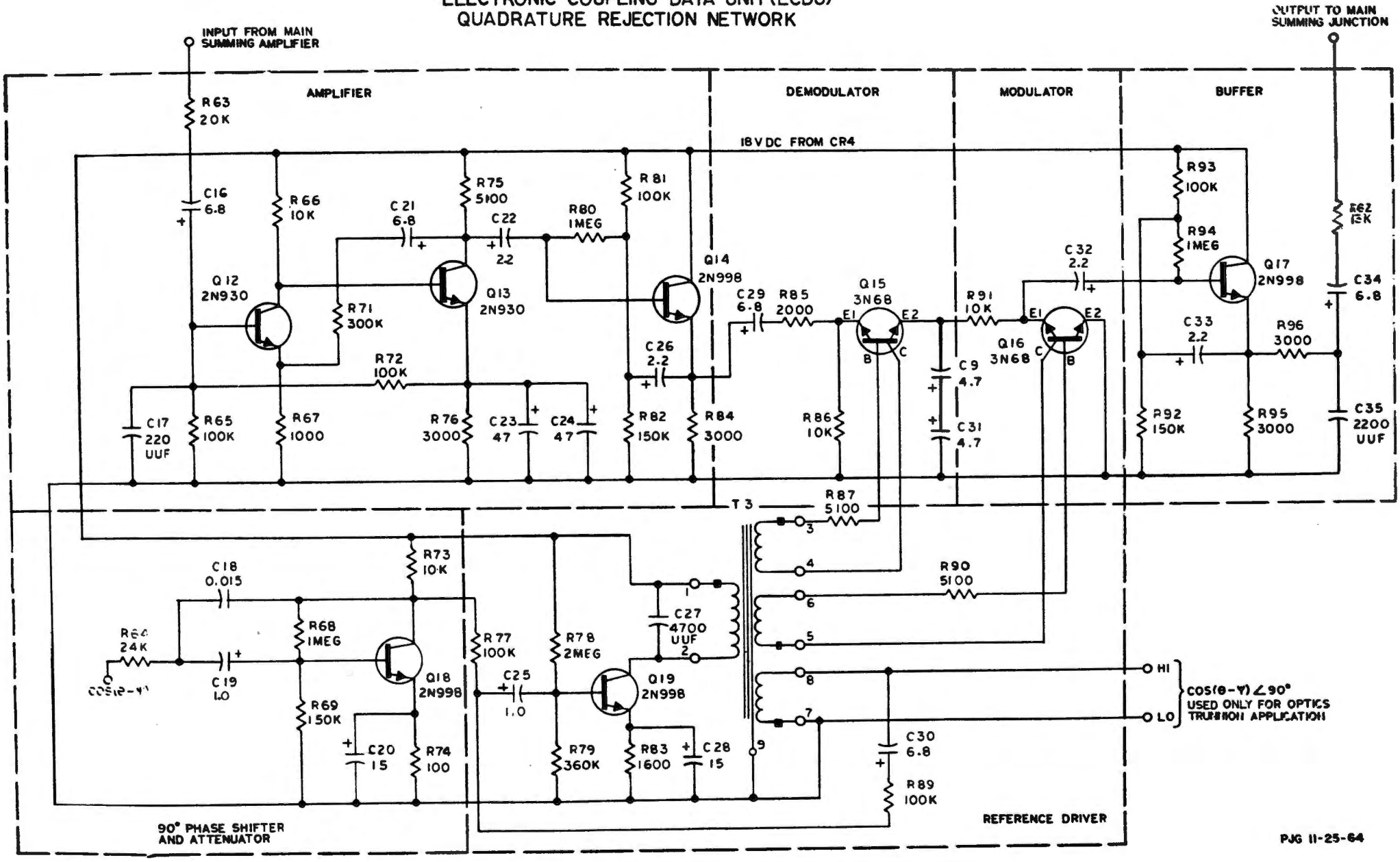
rc/

ELECTRONIC COUPLING DATA UNIT (ECDU)
QUADRATURE REJECTION NETWORK



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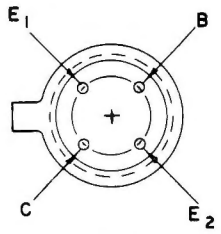
TECHNICAL DATA

3N68 - 3N69 - 3N70

INCH* (INTEGRATED CHOPPER)

APPLICATIONS

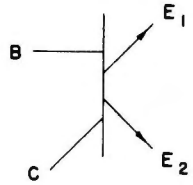
The inch is a stabilized integrated circuit specifically designed for low level electronic commutating, demodulating and chopper applications. This series is ideally suited for these applications because of extremely low offset voltage, low leakage currents, low saturated dynamic impedance and high speed switching characteristics. This series features excellent thermal stability with changes in environmental conditions.



BOTTOM VIEW

MECHANICAL OUTLINE

TO–18 Package - Collector in electrical contact with the base



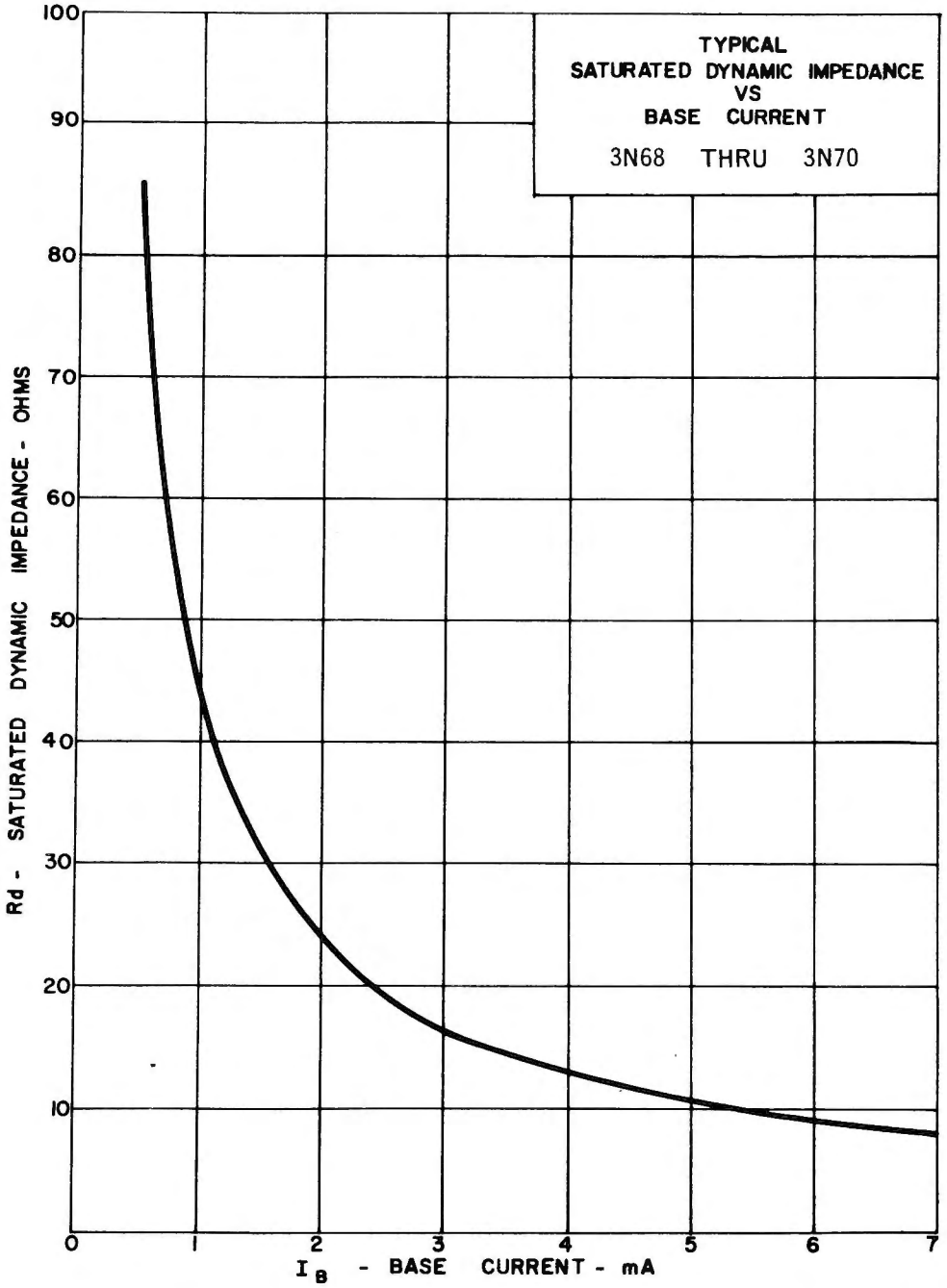
MAXIMUM RATINGS

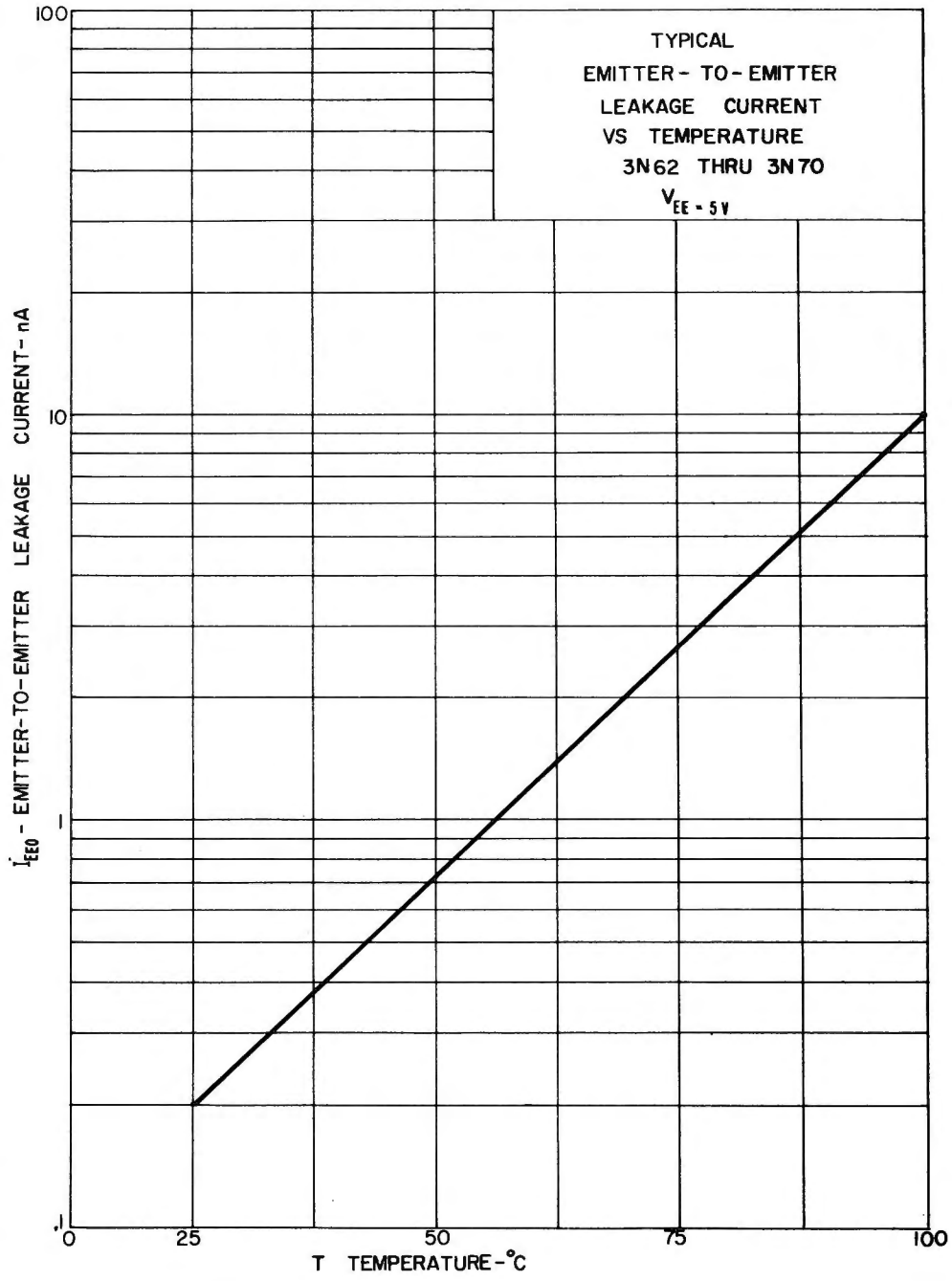
Total Device Dissipation–Free Air	100mW
Emitter Current	10mA
Base Current	10mA
Maximum Temperature–Operating and Storage	-65°C to +200°C

DESIGN CHARACTERISTICS AT 25°C (except as noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
$BV_{E_1E_2O}$	Emitter-Emitter Breakdown Voltage	$I_E = +10\mu A$ or $I_E = -10\mu A$	10	-	-	V
BV_{E_1BO}	Emitter-Base Breakdown Voltage	$I_E = 10\mu A$	12	-	-	V
BV_{E_2BO}	Emitter-Base Breakdown Voltage	$I_E = 10\mu A$	12	-	-	V
BV_{E_1CO}	Emitter-Collector Breakdown Voltage	$I_E = 10\mu A$	12	-	-	V
BV_{E_2CO}	Emitter-Collector Breakdown Voltage	$I_E = 10\mu A$	12	-	-	V
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 10\mu A$	10	-	-	V
$I_{E_1E_2O}$	Emitter Leakage Current	$V_{E_1E_2} = +5V$ or $V_{E_1E_2} = -5V$	-	0.2	5.0	nA
$I_{E_1E_2O}$	Emitter Leakage Current	$V_{E_1E_2} = +5V$ or $V_{E_1E_2} = -5V$, $T_A = +100°C$	-	10	100	nA
V_O	Offset Voltage	$I_B = 2mA$, $I_E = 0$, $T_A = -25°C$ to $+100°C$				
	3N68		-	-	±200	μV
	3N69		-	-	±100	μV
	3N70		-	-	±50	μV
R_d	Saturated Dynamic Impedance	$I_B = 2mA$, $I_E = 100\mu A$ Peak	-	-	50	Ω
$R_T = \frac{\Delta V_O}{\Delta I_B}$	Transfer Resistance	$I_B = 1.5mA$ to $2.5mA$				
	3N68		-	-	50	mΩ
	3N69		-	-	25	mΩ
	3N70		-	-	25	mΩ
C_{E_1B}	Emitter-Base Capacitance	$V_{E_1B} = 5V$	-	-	5	pf
C_{E_2B}	Emitter-Base Capacitance	$V_{E_2B} = 5V$	-	-	5	pf
t_{on}	"Turn-On" Time	$V_{on} = +16V$, $V_{off} = -5V$, $R_L = 1K$, $I_E = 100\mu A$, $R_B = 10K$	-	-	250	nsec
t_{off}	"Turn-Off" Time	$V_{on} = +16V$, $V_{off} = -5V$, $R_L = 1K$, $I_E = 100\mu A$, $R_B = 10K$	-	-	250	nsec
$\left\lvert\frac{\Delta V_O}{T}\right\rvert$	Thermol Offset Coefficient	$I_B = 2mA$, $I_E = 0$, $T_A = -25°C$ to $+100°C$	-	0.3	-	μV/°C

*TRADEMARK


TYPICAL
SATURATED DYNAMIC IMPEDANCE
VS
BASE CURRENT
3N68 THRU 3N70
Rd - SATURATED DYNAMIC IMPEDANCE - OHMS
100
90
80
70
60
50
40
30
20
10
0
1
2
3
4
5
6
7
I_B - BASE CURRENT - mA


TYPICAL
EMITTER - TO - EMITTER
LEAKAGE CURRENT
VS TEMPERATURE
3N62 THRU 3N70
V_{EE} - 5 V
I_{EEO} - EMITTER-TO-EMITTER LEAKAGE CURRENT - nA
100
10
1
.1
0
25
50
75
100
T TEMPERATURE - °C