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PROJECT APOLLO

COMMAND MODULE

GUIDANCE AND NAVIGATION SYSTEM MANUAL

VOLUME II

AC ELECTRONICS
DIVISION OF GENERAL MOTORS
MILWAUKEE, WISCONSIN

ND -1021041

REV LETTER ON VOL I

APOLLO

COMMAND MODULE

BLOCK I SERIES 100

GUIDANCE AND NAVIGATION SYSTEM MANUAL

VOLUME II OF II

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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4-8.6 MEMORY. Memory consists of an erasable memory with a storage capacity of 1024 words and a fixed core rope memory. Erasable memory is a random-access, destructuve readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a nondestructive storage device. Data stored in fixed memory is unalterable since the data is wired in.

Both memories contain magnetic-core storage elements. In erasable memory the storage elements form a core array; in fixed memory the storage elements form three core ropes. Erasable memory has a density of one word per 16 cores; fixed memory has a density of eight words per core. Each word is located by an address.

Addresses are assigned to instructions to specify the sequence in which they are to be executed, and blocks of addresses are reserved for data such as constants and tables. The information is then put into assigned locations in erasable memory with the CTS, the DSKY's, uplink, or program operation. Information is placed into fixed memory permanently by wiring patterns through the magnetic cores.

A common address register (register S) in the central processor is used with both memories. When register S contains an address pertaining to erasable memory, the erasable memory cycle timing is energized. Timing pulses sent to the erasable memory cycle timing then produce strobe signals for the read, write, and sense functions. The address decoder receives addresses from register S and produces selection signals for the core array. The selection signals allow a word to be written into or read out of the selected storage location. The selected word is strobed by the strobe signals and applied to the sense amplifiers. The sense amplifiers are also strobed and the word is entered into the memory buffer register (G) in the central processor.

Fixed memory contains an addition address register (bank register) which is necessary because of the increased number of locations. Register S addresses energize the fixed memory cycle timing when a location in fixed memory is addressed. The timing pulses sent to the fixed memory cycle timing produce the strobe signals for the read and sense functions. The selection logic receives addresses from registers S and the bank register (register BNK) and produces selection signals for the core ropes. Register BNK receives addresses from the centrol processor write lines when the register is addressed and when the proper control pulses from the sequence generator are present. The content of a storage location in fixed memory is strobed from the fixed memory sense amplifiers, through the sense amplifiers in erasable memory, and into register G in the central processor.

4-8.6.1 Erasable Memory Functional Description. Erasable (E) memory (figure 4-148) consists of a core array, memory cycle timing circuits, the address decoder, selection circuits, and sense amplifiers. The core array is the storage medium by which data is stored in erasable memory. The memory cycle timing circuits generate strobe signals which enable the selection circuits and the sense amplifiers. The address decoder converts the contents of register S into X and Y selection signals for addressing a storage location. The selection circuits select the addressed storage location under control of the selection signals from the address decoder and strobe signals from the memory cycle timing circuits. The sense amplifiers detect the contents of the selected storage location and supply this data to register G.

Erasable memory is addressed by the contents of register S, provided bits 11 and 12 are both logic ZERO's. (See table 4-XII) Only 1008 of a possible 1024 storage locations are utilized by erasable memory. The first 14 locations are reserved for the addressable flip-flop registers and are assigned octal addresses 0000 through 0015. Address 0016 and 0017 have no assigned location; these addresses are used by program to inhibit and release the inhibit of interrupt requests.

4-8.6.1.1 Core Array. The core array has 1024 word storage locations, contained in 16 bit planes and defined by the intersection of 32 X lines and 32 Y lines. Each bit plane contains 1024 cores. An individual bit in each plane is selected by the intersection of an X and Y line threading a core. The selection signals are generated by the address decoder subject to strobe signals from erasable memory cycle timing circuits. This occurs simultaneously in all 16 bit planes thus selecting one word storage location. Each core is also threaded by a sense line and an inhibit line. The sense line threads all cores in a particular bit plane, such that current is induced into the senseline if the state of any core in the plane is changed from ONE to a ZERO. Current through the inhibit line prevents any core in the bit plane from switching since it opposes the current on the X and Y selection lines. Thus, current on a combination of X, Y, and inhibit lines determines which cores are selected. Core selection is identical for both the read and write operations.

4-8.6.1.2 Erasable Memory Cycle Timing Circuits. The erasable memory cycle timing circuits consist of timing control and timing flip-flops, which generate strobe signals to sequence the operation of erasable memory. These strobe signals are generated during one memory cycle time (11.7 microsecond), subject to timing signals from the timer as shown in figure 4-149. The timing control generates the strobe signals subject to signal $\overline{\text{FER}}$. Signal $\overline{\text{FER}}$ is generated only when bits 11 and 12 of register S are both logic ZERO's, signal $\overline{\text{MC}}$ is present, and signal SCAD is not present. Bits 11 and 12 are logic ZERO's when the specified memory address is lower than 2000 (octal), which indicates that either an addressable register or erasable memory has been addressed. Signal $\overline{\text{MC}}$ is present, provided that a multiply or divide instruction is not in progress or signal GOJAM has not been initiated. Signal SCAD is a logic ONE when the specified address is lower than 0020 (this address indicates one of the addressable registers is being addressed). The timing control also generates signal TIMR when either signal STOP A (indicating a monitor stop) or signal STOP B (indicating an alarm) is present. Signal TIMR resets several timing flip-flops in erasable memory and inhibits the addressing of the ropes in fixed memory. Input MYCLMP inhibits access to memory (and avoids any loss of data) if the 3 volt power supply falls out of limits.

The timing flip-flops generate the various strobe signals which enable the selection circuits and sense amplifiers. The strobe signals generated are read, set, reset, write, inhibit, and sense. As previously discussed, several strobe signals are inhibited by signal TIMR; the remaining strobe signals are inhibited by signal GOJAM. Therefore, these two signals inhibit access to erasable and fixed memory when a monitor stop has been initiated by the CTS or when an alarm condition has occurred within the AGC.

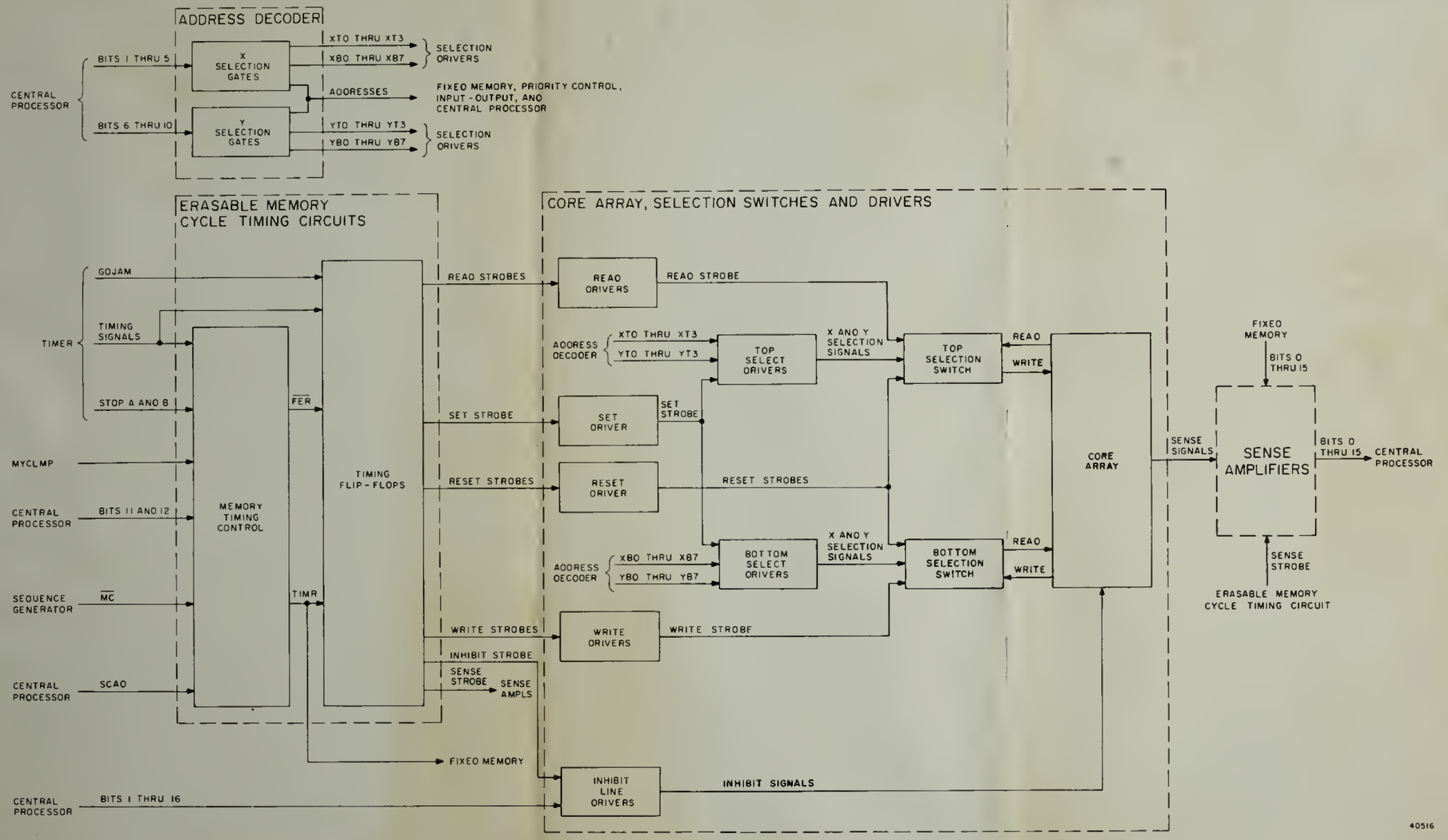


Figure 4-148. Erasable Memory, Functional Diagram

Table 4-XII. Addressing

Register Groups				Octal Address		Pseudo Address (Decimal)	Contents of BNK *					Contents of S *											
				Real	Pseudo		15	14	13	12	11	12	11	10	9	8	7	6	5	4	3	2	1
CP	A Q Z LP			0000 - 0003	Same	0 - 3	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	X	X
	IN			0004 - 0007	Same	4 7	X	X	X	X	X	0	0	0	0	0	0	0	0	0	1	X	X
	OUT			0010 - 0014	Same	8 - 12	X	X	X	X	X	0	0	0	0	0	0	0	0	1	X	X	X
	BNK			0015	Same	13	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1	0	1
	No Brt Locatron			0016 - 0017	Same	14 15	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1	1	X
E	Special			0020 0027	Same	16 23	X	X	X	X	X	0	0	0	0	0	0	0	1	0	X	X	X
	Spares			0030 - 0033	Same	24 27	X	X	X	X	X	0	0	0	0	0	0	0	1	1	0	X	X
	CTR			0034 - 0057	Same	28 - 47	X	X	X	X	X	0	0	0	0	0	0	X	X	X	X	X	X
	GE			0060 - 1777	Same	48 1023	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X
F	F_1	FF	BANK 01	2000 - 3777	Same	1024 2047	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X
			02	4000 - 5777	Same	2048 3071	X	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X	X
		FS	03	6000 - 7777	6000 7777	3072 - 4095	0	0	0	X	X	1	1	X	X	X	X	X	X	X	X	X	X
			04	6000 7777	10000 11777	4096 - 5119	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			05	6000 7777	12000 - 13777	5120 - 6143	0	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			06	6000 7777	14000 15777	6144 - 7167	0	0	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			07	6000 7777	16000 17777	7168 8191	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			10	6000 7777	20000 21777	8192 9215	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X
	F_2		11	6000 - 7777	22000 23777	9216 10239	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			12	6000 - 7777	24000 - 25777	10240 - 11263	0	1	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			13	6000 7777	26000 27777	11264 12287	0	1	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			14	6000 7777	30000 31777	12288 13311	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			21	6000 7777	42000 - 43777	17408 - 18431	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			22	6000 7777	44000 45777	18432 - 19455	1	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			23	6000 7777	46000 47777	19456 20479	1	0	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			24	6000 7777	50000 51777	20480 21503	1	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X
	F_3		25	6000 - 7777	52000 53777	21504 - 22527	1	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			26	6000 7777	54000 55777	22528 23551	1	0	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			27	6000 7777	56000 - 57777	23552 24575	1	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			30	6000 7777	60000 61777	24576 25599	1	1	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			31	6000 7777	62000 63777	25600 - 26623	1	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			32	6000 7777	64000 65777	26624 27647	1	1	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			33	6000 - 7777	66000 67777	27648 29671	1	1	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			34	6000 7777	70000 71777	28672 29695	1	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X

* X means 0 or 1

0687

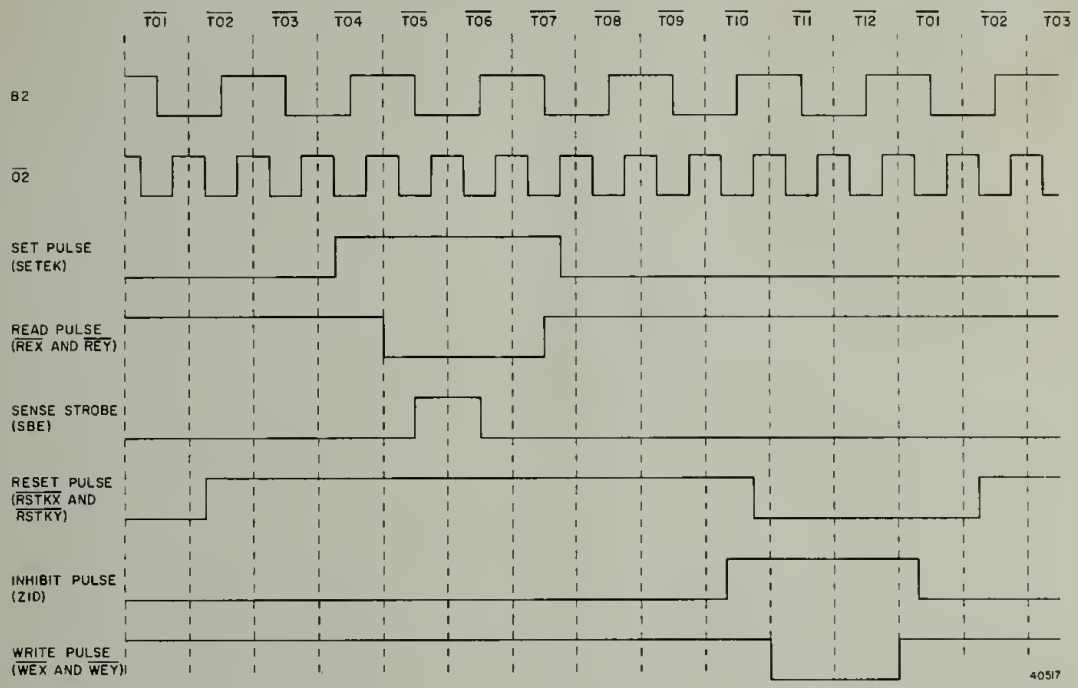


Figure 4-149. Erasable Memory, Timing Diagram

4-8.6.1.3 Address Decoder. Bits 10 through 1 of register S contain the address of the location in erasable memory being interrogated. The address decoder (figure 4-148) receives this address and produces signals which select the addressed storage location. Since each bit in a 16 bit storage location is selected by the intersection of an X and a Y selection line, and there are 32 X planes and 32 Y planes, a signal is needed to select each combination. The selection is accomplished by two 4-by-8 matrices, one for the Y lines. The X selection signals, derived from bits 5 through 1 of register S, are XT0 through XT3 and XB0 through XB7. The Y selection signals, derived from bits 10 through 6 of register S, are YT0 through YT3 and YB0 through YB7. The XT and YT signals are supplied to the top select drivers, and the XB and YB signals are supplied to the bottom select drivers. In addition, the two sets of selection signals are combined to form addresses which are forwarded to fixed memory for addressing the bank register, to input-output control for controlling parity test, and to the central processor for addressing the addressable registers. Counter addresses are sent also to the priority control and the sequence generator.

4-8.6.1.4 Selection Switches and Drivers. Selection signals from the address decoder are applied to the top and bottom select drivers. When these drivers receive the set strobe, the selection signals are supplied to top and bottom selection switches. The X and Y selection is accomplished by current steering circuits according to the coincident-current selection technique. Figure 4-150 is a simplified diagram of the selection circuits. Each selection signal, generated as a result of the address from register S, effectively closes one top or bottom selection switch. Any one of 32 lines can be selected by closing one top and one bottom selection switch. The +13 volts and ground connections are interchanged, depending upon whether a read or a write operation is being performed.

During the read operation, the X and Y selection signals are supplied to the selection switches through the select drivers (figure 4-148). The read strobe enables the top selection switches and allows current to flow from the bottom selection switches through the core array to the top selection switches. The current flowing through the X and Y lines coincides at the addressed storage location in the core array. When this occurs, the 16 cores in the storage location are switched to a logic ZERO if they were not previously set. Those cores previously set remain at a logic ZERO. As a result, current is induced into the sense lines which thread those cores that switched to a logic ZERO. The current on the sense lines is detected by the sense amplifiers and applied to register G when the sense strobe is generated.

The selection switches remain set until the reset strobe is received on the reset windings. When the selection switches are reset, current is induced on the X and Y selection lines within the core. The write strobe enables the bottom selection switches and allows current to flow from the top selection switches through the core array to the bottom selection switches. Again the current flowing through the X and Y lines coincides at the addressed storage location in the core array. The cores in the addressed location are switched to a logic ONE, provided they are not also receiving current on the inhibit lines. All cores receiving inhibit current remain in a logic ZERO. Inhibit current is governed by the content of register G. If an inhibit driver receives a bit containing a logic ONE, the driver is gated on by the inhibit strobe and inhibit current is supplied to a bit plane. There are 16 inhibit drivers, and each driver is connected to a bit plane. Thus, the content of register G determines which cores in a storage location are switched by the X and Y drive lines during the write operation.

4-8.6.1.5 Sense Amplifiers. There are 16 sense amplifiers in erasable memory. Each amplifier senses the contents of a bit location during the read operation. The bipolar sense signals are converted to single-polarity signals and forwarded to register G when the amplifiers are gated with the sense strobe. In addition, the word read out of fixed memory is also gated through the erasable memory amplifiers to register G.

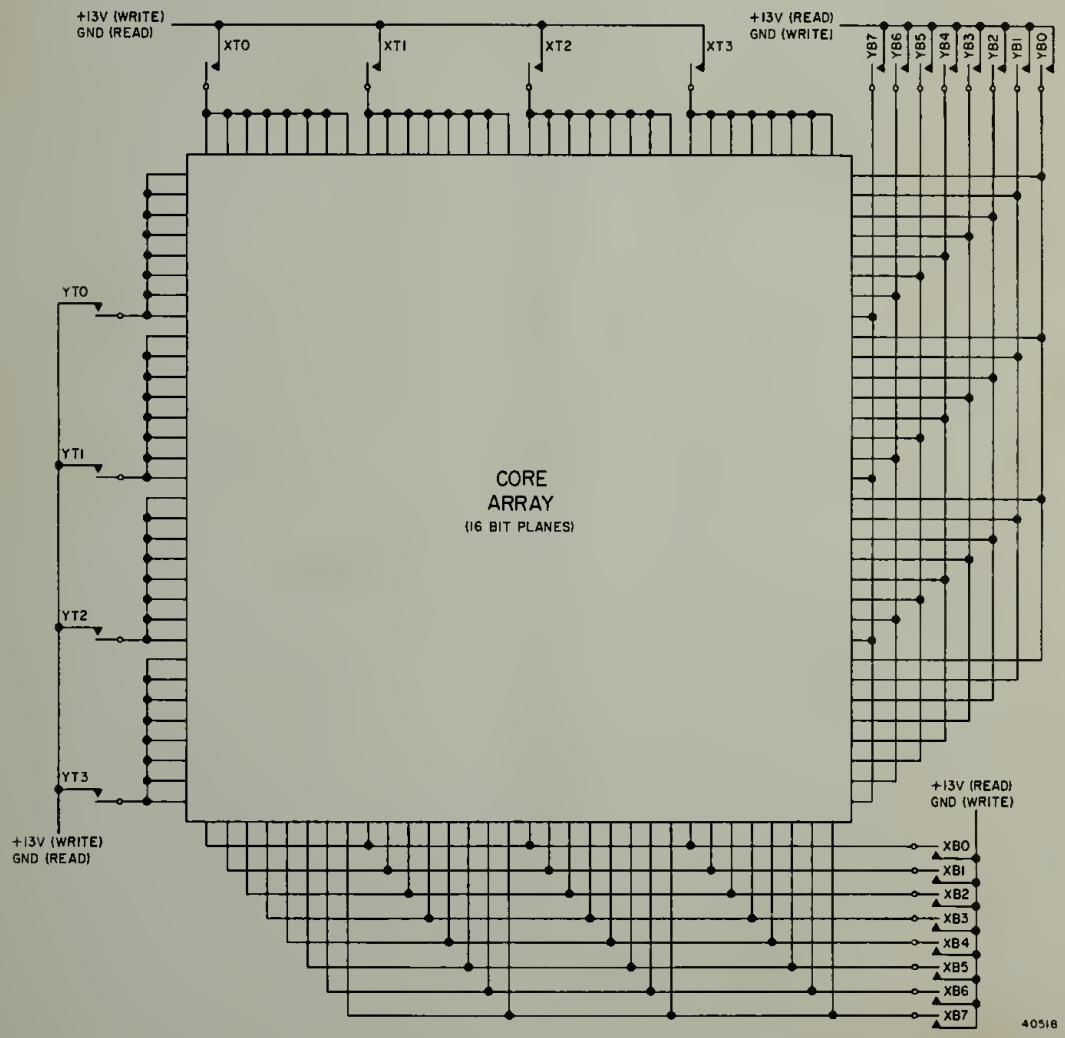


Figure 4-150. X and Y Selection, Simplified Diagram

4-8.6.2 Erasable Memory Detailed Description. The functional presentation of the core array, timing circuit, address decoder, selection circuits, and the sense amplifiers in erasable memory are detailed in the following paragraphs.

4-8.6.2.1 Core Array. The core array (figure 4-151) contains 16 bit planes. Each bit plane consists of 1024 cores arranged in 32 columns and 32 rows. An individual bit is selected by the intersection of X selection lines (XT, XB) and Y selection lines (YT, YB) threading a core. The selection lines are threaded through the cores so that one core on each bit plane is selected by a given X - Y combination. Each core selected is in the same location in every bit plane at the intersection of the X and Y selection lines carrying current. The location of the line intersection is determined by addressing via the selection circuits. The 16 selected cores, one per bit plane, constitute a word storage location. The direction in which current flows through the lines determines whether data is being written into or read out of a selected core.

In addition to the X and Y lines, each core in a bit plane (figure 4-152) is threaded by an inhibit line and a sense line. Current through the inhibit line is in opposition to the X and Y selection currents and prevents all unselected cores in the bit plane from being switched since it cancels one-half the selection current. Current is induced into the sense line if the state of any core is changed from a ONE to a ZERO; no current is induced if the core is already in a ZERO state. The sense lines are connected to 16 amplifiers which amplify the current in a sense line and provide the power necessary to write ONE's into register G of the central processor. It is in this manner that the contents of an erasable memory location are detected.

Before a storage location in erasable memory is written into, the location must be cleared. This is accomplished by applying reset signals to the selection switches. All the cores of the addressed location which are in the ONE state will change to the ZERO state; all cores in the ZERO state remain in that state. When the particular storage location is written into, current is sent through the X and Y selection lines as previously discussed but in the opposite direction. A current is fed also into the inhibit lines of all bit planes in which no ONE is to be written (i.e., where a ZERO should remain in a particular core). At write time several different current conditions exist for the various cores. Whenever a core is intersected by only one selection line (X or Y), the core remains in its existing state. Whenever a core is intersected by one selection line (X or Y) and an inhibit line, the effects of both currents cancel, and the core remains in its existing condition. Whenever a core is intersected by two selection lines (one X line and one Y line) and an inhibit line, the net effect of all three currents is equal to the effect of a single select current (passing through a core of an addressed location which has been cleared), and the core remains in the ZERO state. Only if a core is intersected by two selection lines (one X line and one Y line) but not an inhibit line will a core change from the ZERO to the ONE state. It is in this manner that a 16-bit word is entered into erasable memory.

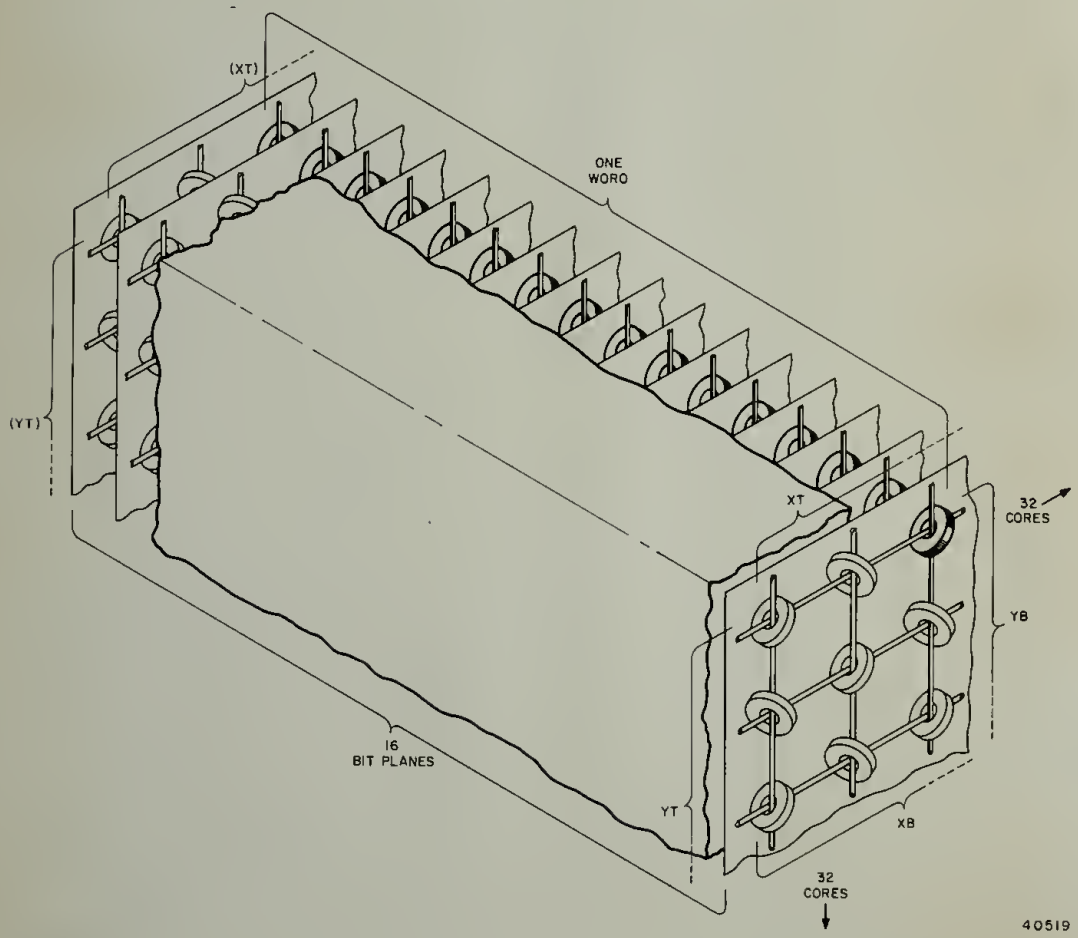


Figure 4-151. Core Array

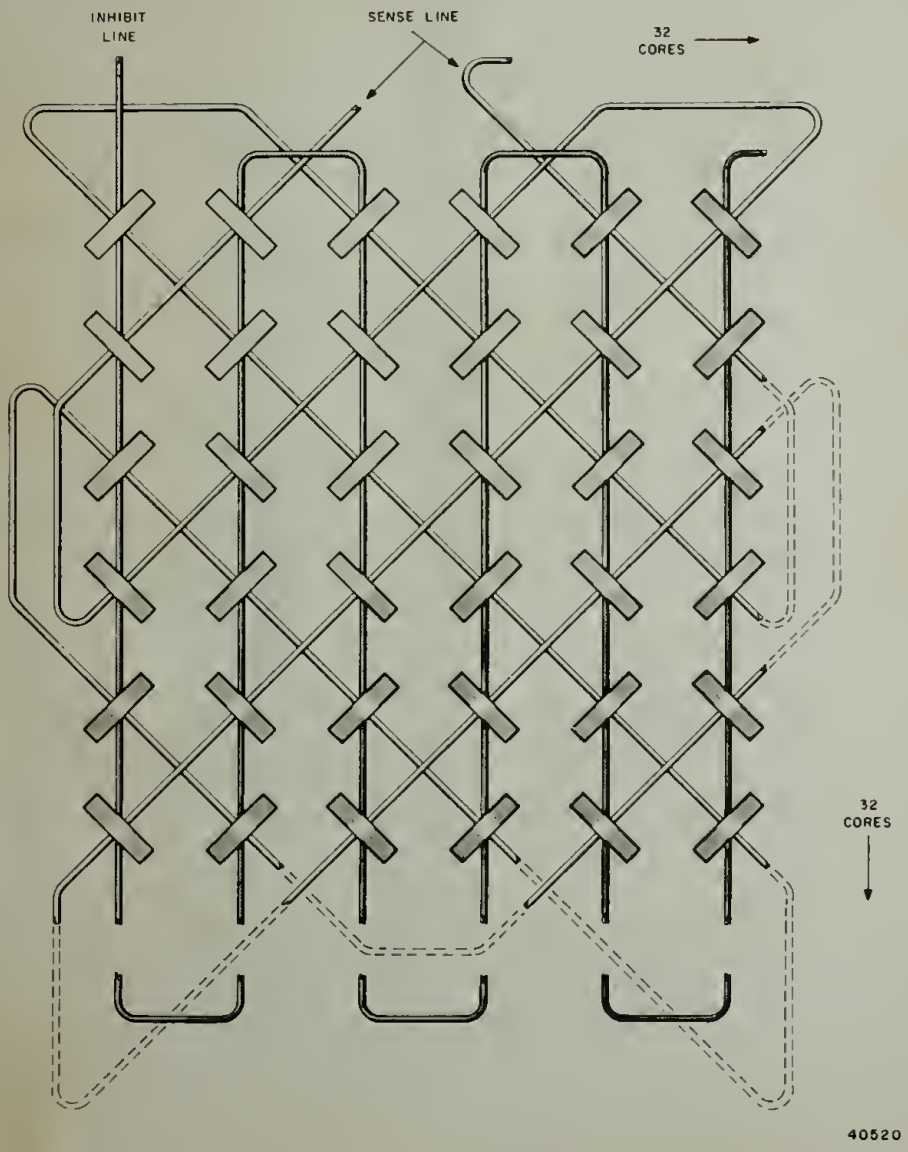


Figure 4-152. Bit Plane

4-8.6.2.2 Erasable Memory Cycle Timing. Erasable memory cycle timing (figure 4-153) consists of several flip-flop circuits, which produce the timing signals for erasable memory. These timing signals (refer to figure 4-149) are produced in one memory cycle time (T01 through T12). Bits 11 and 12 (ST11 and ST12) from register S are logic ZERO's when erasable memory is addressed. This condition, coincident with memory cycle signal ($\overline{MC}$), produces a ferrite gating signal ($\overline{FER}$), provided signal SCAD is a logic ZERO. A ONE in either bit position 11 or 12, or both, indicates an address in fixed memory. Signal SCAD is a logic ONE when a flip-flop register is addressed. The generation of $\overline{FER}$ allows the flip-flops to be set at the times indicated.

The set strobe (SETEK) is initiated when timing signals $\overline{T04}$ and $\overline{B2}$ are coincident and is terminated when signals $\overline{T07}$, B2, and Q2 are coincident (figure 4-153). Signal SETEK conditions the core selection switches to be addressed. The flip-flop formed by gates 53314 and 53315 produces strobe signal SBE, which enables the sense amplifiers to supply data to register G. The flip-flop is set by signal $\overline{T05}$ and B2 and reset by signals $\overline{T06}$ and $\overline{B2}$. Read strobes $\overline{REX}$ and $\overline{REY}$ enable data to be read out of erasable memory. These two strobes are generated simultaneously at time 5 and inhibited when signals $\overline{T07}$ and $\overline{Q2X}$ are coincident. The flip-flops associated with signals SETEK, SBE, $\overline{REX}$, and $\overline{REY}$ are also reset by signal GOJAM. Thus, data cannot be read out of erasable memory while signal GOJAM is present.

The inhibit strobe (ZID) gates the inhibit drivers when a ZERO is to be written into erasable memory. Signal ZID is generated by flip-flop gates 52303 and 52304 when signals $\overline{T10}$ and $\overline{Q2X}$ are coincident. The flip-flop is reset at time 1. The reset strobes $\overline{RSTKX}$ and $\overline{RSTKY}$ are produced simultaneously when signals $\overline{T10}$ and $\overline{B2}$ are coincident. These signals enable the reset drivers, thereby clearing the addressed memory location prior to writing in data. The reset strobe flip-flop, consisting of gates 52314 and 52315, is reset by signals $\overline{T02}$, $\overline{B2}$ and Q2. Write strobes $\overline{WEX}$ and $\overline{WEY}$ are generated from time 11 to time 1 by flip-flop gates 52308 and 52309. Signal $\overline{T01}$ is inverted and supplied to fixed memory cycle timing. The flip-flops which produce the inhibit, reset, and write strobes are reset by signal TIMR. Signal TIMR is generated as the result of stop signals STPA and STPB, which occur at time 12. Timing signals P01 through P03, and P05 control the generation of TIMR to ensure the signal is not generated until after the completion of the strobes.

4-8.6.2.3 Address Decoder. A storage location in erasable memory is addressed by X and Y coordinates. There are 32 X coordinates and 32 Y coordinates (figure 4-154). The X coordinate is controlled by signals XT0 through XT3 and XB0 through XB7; the Y coordinate is controlled by signals YT0 through YT3 and YB0 through YB7. Signals XT, XB, YT, and YB are generated as a function of bits ST01 through ST10 from register S (figure 4-155). The three lowest-order bits, ST01 through ST03, produce signals XB0 through XB7 (see table 4-XIII); bits ST04 and ST05 produce XT0 through XT3 bits; bits ST06 through ST08 produce YB0 through YB7; and bits ST09 and ST10 produce XT0 through XT3.

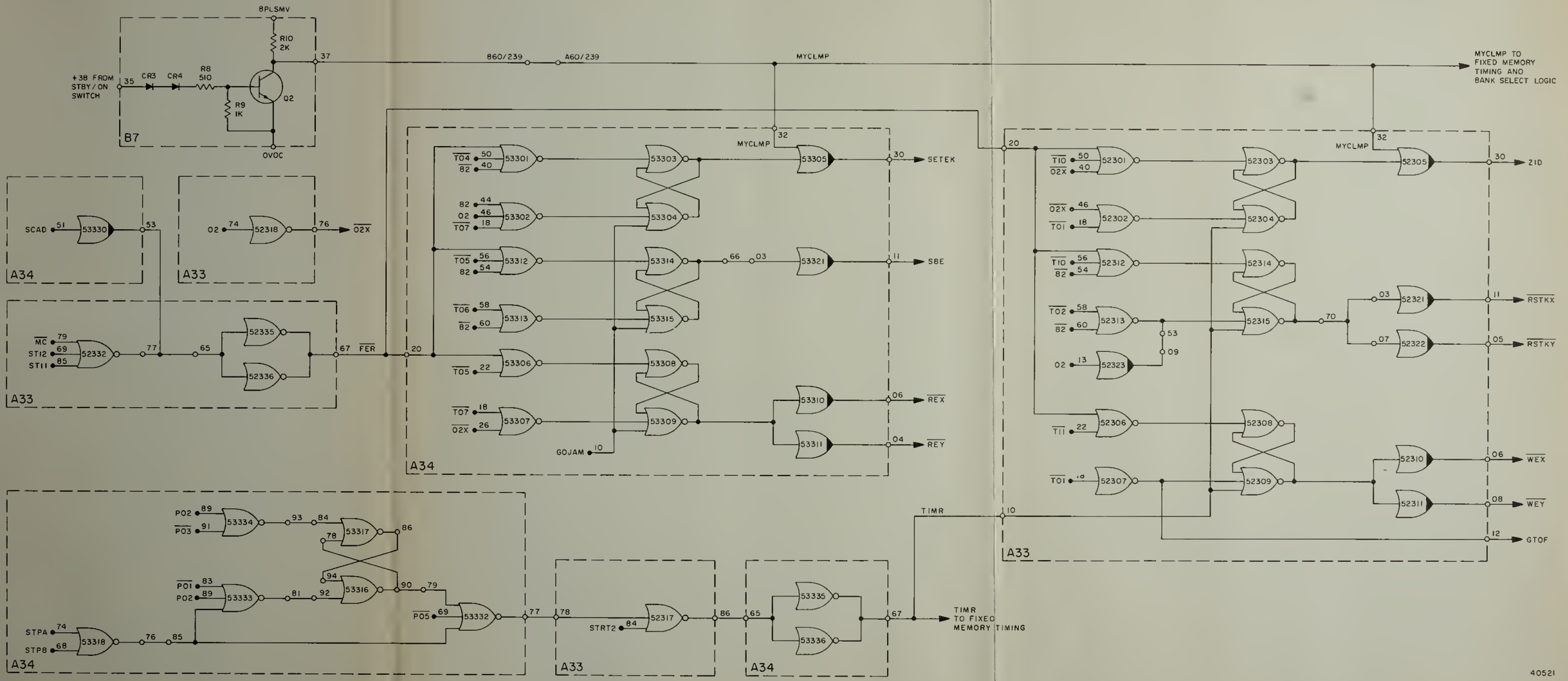


Figure 4-153. Memory Cycle Timing - Erasable

Combinations of control signals XT, XB, YT, and YB, produced as a result of octal addresses 0000 through 1777, set the proper selection switches which are associated with each control pulse. Addresses 0000 through 0017 are reserved for the addressable flip-flop registers, 0020 through 0027 for special registers, 0034 through 0057 for the various counters, and 0060 through 1777 for general storage.

4-8.6.2.4 Selection Circuits. As previoulsy stated, information is written into and read out of a storage location by means of core selection. This selection is performed by selection switches and associated driver circuits (figure 4-156). Since X and Y operations function the same, only one set of selection switches (X bottom and X top) and their associated drivers (X bottom, X top, X read, X write, and X reset) is discussed. Signal names and pin numbers for other circuits than those discussed may be found on figure 4-156.

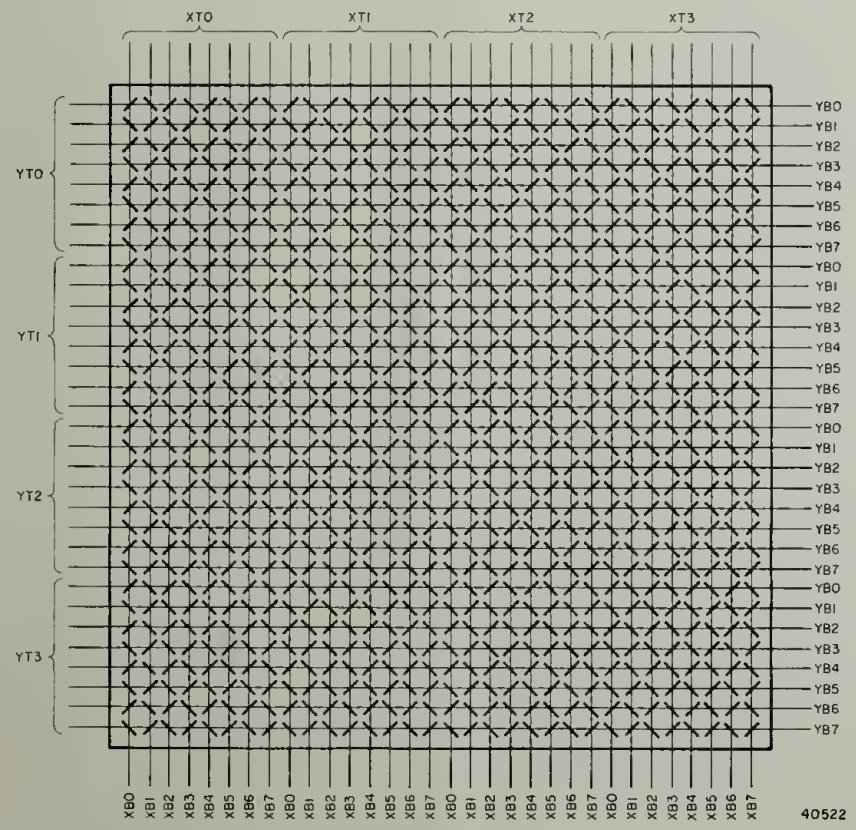


Figure 4-154. X and Y Coordinates

Table 4-XIII. Register S Bit Assignments

Signal	Bit		Signal	Bit			Signal	Bit		Signal	Bit		
	10	9		8	7	6		5	4		3	2	1
YT0	0	0	YB0	0	0	0	XT0	0	0	XB0	0	0	0
YT1	0	1	YB1	0	0	1	XT1	0	1	XB1	0	0	1
YT2	1	0	YB2	0	1	0	XT2	1	0	XB2	0	1	0
YT3	1	1	YB3	0	1	1	XT3	1	1	XB3	0	1	1
			YB4	1	0	0				XB4	1	0	0
			YB5	1	0	1				XB5	1	0	1
			YB6	1	1	0				XB6	1	1	0
			YB7	1	1	1				XB7	1	1	1

The set strobe driver acts as a power switch for the bottom and top select drivers by suppling +13 vdc to the drivers. Signal SETEK forces transistor Q4 to conduct, which causes transistors Q5, Q6, and Q7 to conduct. When Q6 and Q7 conduct, B+ is supplied to the collectors of transistors Q13 and Q14, which causes both to conduct.

The read and write drivers operate in the same manner; therefore, only the write driver is discussed. Input signal $\overline{\text{WEX}}$ is inverted by transistor Q10. Diodes CR9 and CR10, emitter follower Q11, and resistor R17 stabilize transistor Q12 base current and the current through diodes CR11 and CR12. Transistor Q12 collector current rise time is controlled by inductor L2 and is independent of collector voltage.

The reset driver supplies a path for current through winding D of the selection switches to reset the cores. Signal $\overline{\text{RSTKX}}$ is inverted by transistor Q8. Diodes CR6, CR7, and CR8 maintain a constant voltage on the base of Q9, which provides a constant output current.

Each selection switch contains a ferrite selection core with four windings, two of which are connected to power transistors. Transistor Q1 of the X bottom selection switch and transistor Q17 of the X top selection switch form a path for read current. Transistors Q2 and Q18 form a path for write current. In order to generate a current on the X selection line, the selection switches and drivers must be energized.

Transistor Q1 in the bottom select driver conducts, via winding A of core K1, only if control signal XB0E is present and signal SETEK is supplied to the set strobe driver. Current then flows through winding A and through Q14 which changes the state of K1. When this occurs, a current is induced in winding B, which causes transistor Q1 of the bottom selection switch to conduct and transistor Q2 to be cut off. In a similar manner another control signal, XT0E, causes Q1 of the top select driver to conduct, and tran-

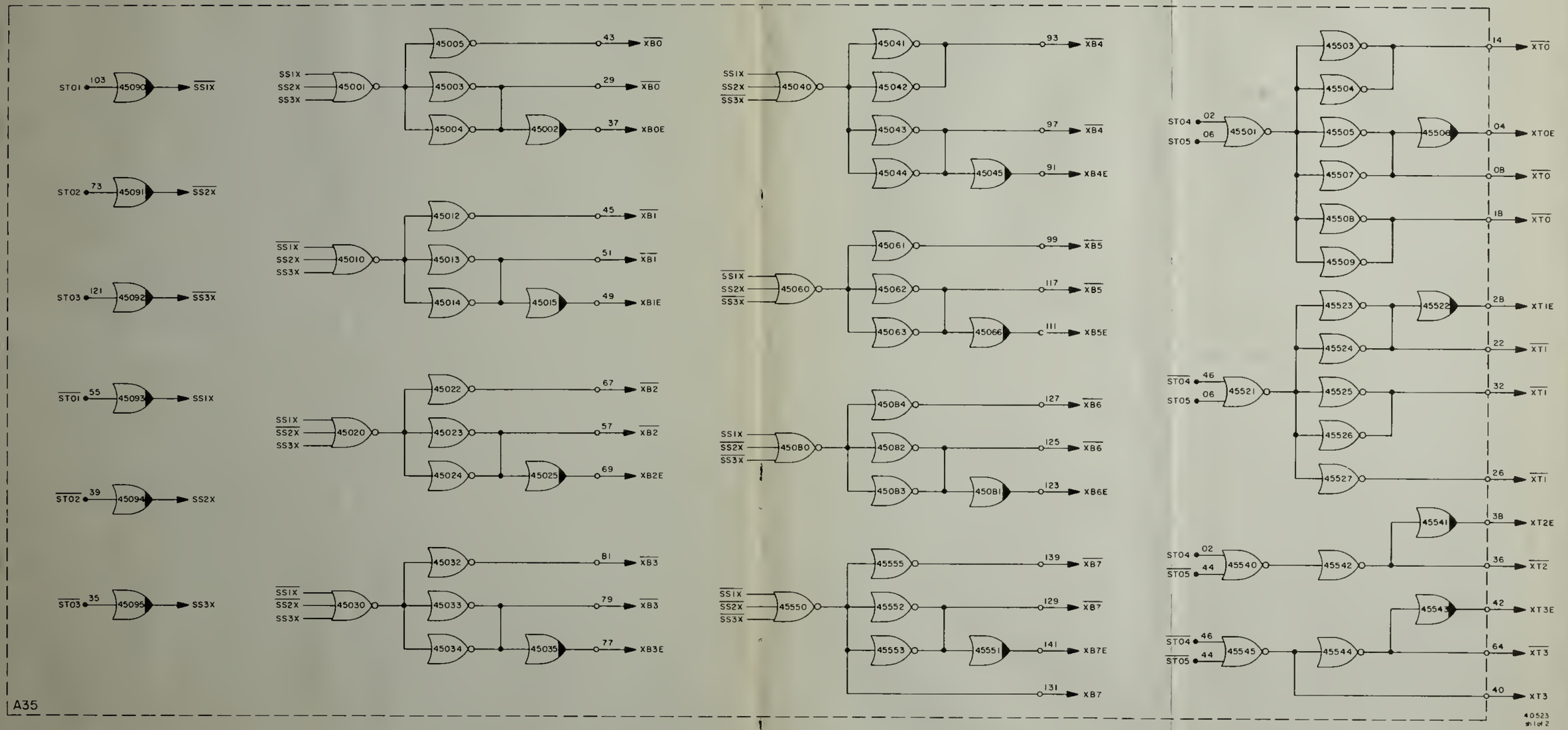


Figure 4-155. Address Decoder (Sheet 1 of 2)

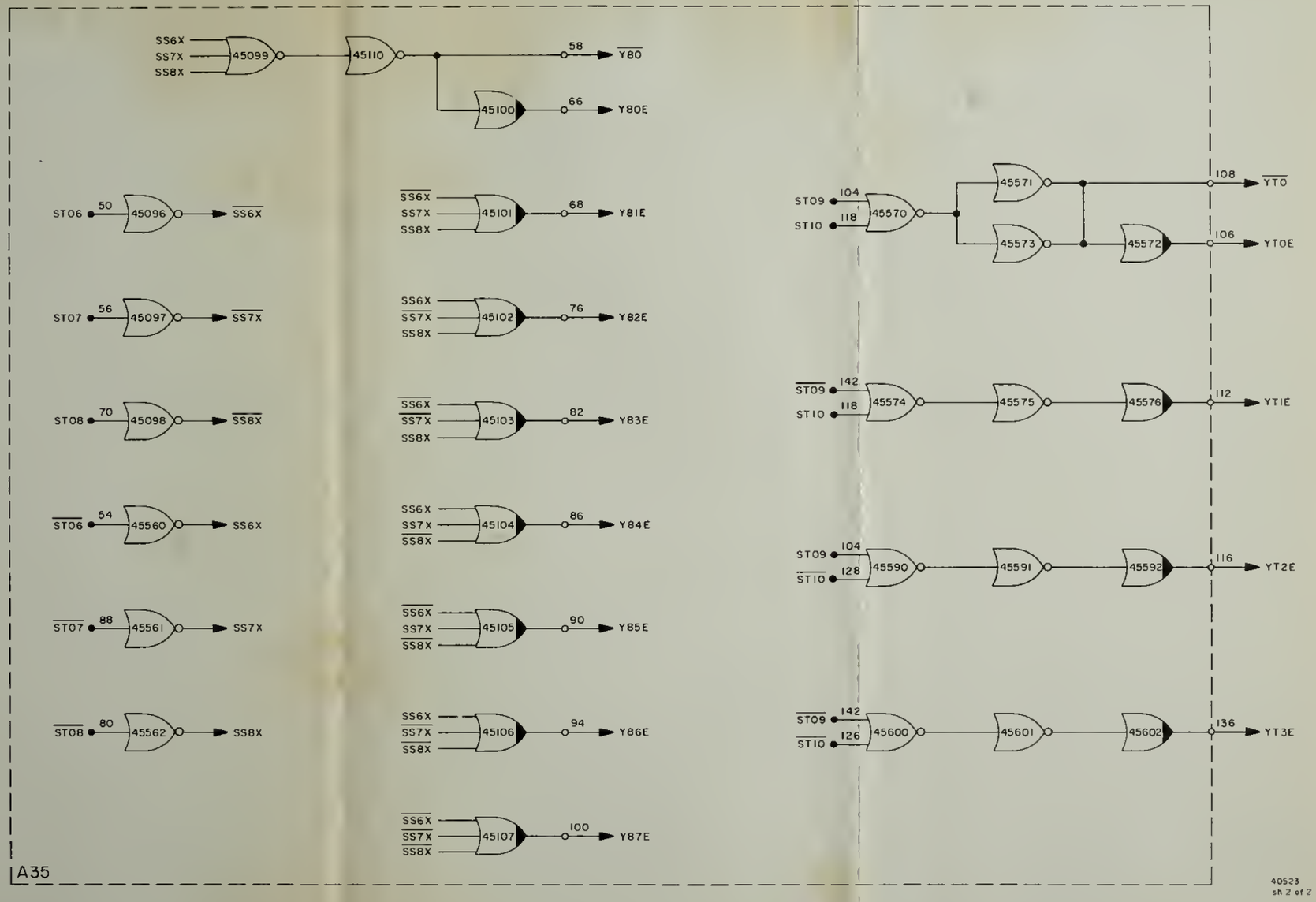
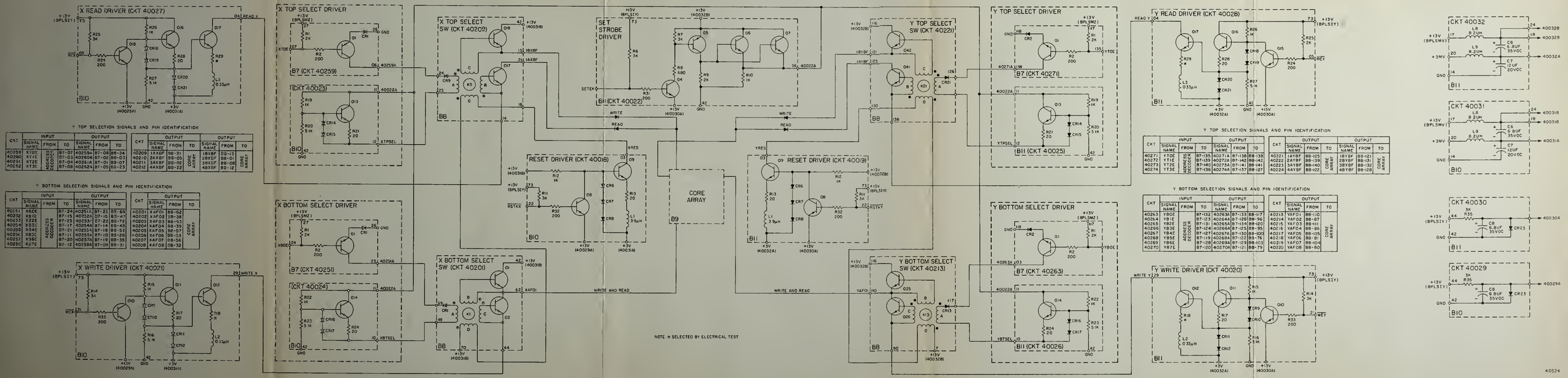


Figure 4-155. Address Decoder (Sheet 2 of 2)



Y TOP SELECTION SIGNALS AND PIN IDENTIFICATION

CKT	INPUT SIGNAL NAME	INPUT FROM	INPUT TO	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40259	XTOE	ADDRESS DECODER	B7-07	40259A	B7-08	B8-24
40260	XTIE		B7-03	40260A	B7-02	B8-03
40261	XT2E		B7-04	40261A	B7-01	B8-07
40262	XT3E		B7-06	40262A	B7-05	B8-23

CKT	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40209	1AXDF	B8-21	CORE ARRAY	1BXDF	B8-13	CORE ARRAY
40210	2AXDF	B8-09		2BXDF	B8-01	
40211	3AXDF	B8-02		3BXDF	B8-06	
40212	4AXDF	B7-05		4BXDF	B8-12	

Y BOTTOM SELECTION SIGNALS AND PIN IDENTIFICATION

CKT	INPUT SIGNAL NAME	INPUT FROM	INPUT TO	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40251	XBOE	ADDRESS DECODER	B7-24	40251A	B7-23	B5-69
40252	XB1E		B7-15	40252A	B7-16	B5-67
40253	XB2E		B7-23	40253A	B7-22	B5-72
40254	XB3E		B7-17	40254A	B7-14	B5-65
40255	XB4E		B7-21	40255A	B7-18	B8-52
40256	XB5E		B7-11	40255A	B7-10	B5-28
40257	XB6E		B7-20	40257A	B7-19	B8-55
40258	XB7E		B7-12	40258A	B7-09	B8-31

CKT	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40201	XAFOI	B8-62	CORE ARRAY
40202	XAFO2	B8-38	
40203	XAFO3	B8-93	
40204	XAFO4	B8-39	
40205	XAFO5	B8-57	
40206	XAFO6	B8-33	
40207	XAFO7	B8-56	
40208	XAFO8	B8-32	

Y TOP SELECTION SIGNALS AND PIN IDENTIFICATION

CKT	INPUT SIGNAL NAME	INPUT FROM	INPUT TO	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40271	YTOE	ADDRESS DECODER	B7-135	40271A	B7-138	B8-13B
40272	YT1E		B7-139	40272A	B7-142	B8-14D
40273	YT2E		B7-140	40273A	B7-141	B8-14B
40274	YT3E		B7-136	40274A	B7-137	B8-12F

CKT	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40221	1AYBF	B8-125	CORE ARRAY
40222	2AYBF	B8-139	
40223	3AYBF	B8-140	
40224	4AYBF	B8-122	

CKT	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40213	YAFOI	B8-110	CORE ARRAY
40214	YAFO2	B8-87	
40215	YAFO3	B8-111	
40216	YAFO4	B8-86	
40217	YAFO5	B8-105	
40218	YAFO6	B8-81	
40219	YAFO7	B8-104	
40220	YAFO8	B8-80	

Y BOTTOM SELECTION SIGNALS AND PIN IDENTIFICATION

CKT	INPUT SIGNAL NAME	INPUT FROM	INPUT TO	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40263	YBOE	ADDRESS DECODER	B7-132	40263A	B7-133	B8-117
40264	YB1E		B7-123	40264A	B7-126	B8-96
40265	YB2E		B7-131	40265A	B7-134	B8-120
40266	YB3E		B7-124	40266A	B7-125	B8-95
40267	YB4E		B7-127	40267A	B7-130	B8-100
40268	YB5E		B7-119	40268A	B7-122	B8-76
40269	YB6E		B7-128	40269A	B7-129	B8-103
40270	YB7E		B7-120	40270A	B7-121	B8-79

CKT	OUTPUT SIGNAL NAME	OUTPUT FROM	OUTPUT TO
40231	1BYBF	B8-125	CORE ARRAY
40232	2BYBF	B8-131	
40233	3BYBF	B8-132	
40234	4BYBF	B8-128	

40524

Figure 4-156. Selection Switches and Drivers

sistor Q13 changes the state of K9. As K9 switches, transistor Q17 is forced to conduct and transistor Q18 is cut off. At the time that transistor Q1 and Q17 are conducting and signal $\overline{REX}$ is applied to the X read driver, read current flow from B+ to B- (+3V) through transistor Q1 in the bottom selection switch, the core array, transistor Q17 in the top selection switch, and transistor Q13 in the read driver.

Generating a write current is similar to generating a read current. Signal $\overline{RSTKX}$ enables the reset driver, which allows current to flow through winding D of both selection switches. Current through winding D resets cores K1 and K9, which in turn induces current into both C windings causing transistors Q2 and Q18 to conduct and transistors Q1 and Q17 to cut off. At the same time signal $\overline{WEX}$ enables the write driver. A current path is provided from B+ to B- through transistor Q18, the core array, transistor Q2, and transistor Q12 in the write driver.

The inhibit line drivers prevent the setting of a core in erasable memory when a ZERO is to be written into a bit location. In order to address a storage location, 16 inhibit line drivers are required, one per bit plane. Each driver (figure 4-157) receives +13 vdc signal (40017A) when inhibit strobe ZID occurs from memory cycle timing, and one bit (GEM01 through 16) from register G. During the write operation, ZID initiates a power switching action similar to that of the set strobe driver and B+ is applied to the collectors of transistors Q1 and Q2. If the input from register G is a logic ONE, Q1 conducts and inhibits Q2 and Q3. This prevents current from flowing through the inhibit line and the addressed core can be switched to the ONE state. When the input is a logic ZERO, the signal is inverted by Q1, which enables Q2 and Q3. When transistor Q3 is enabled, a path is provided for the inhibit current, which prevents the switching of the addressed core.

4-8.6.2.5 Sense Amplifiers. Sixteen sense amplifiers (one per bit plane) are associated with erasable memory. Each sense amplifier (figure 4-158) accepts bipolar signals (SAF01 through 16 and SBF01 through 16) from the core array sense lines. When a core switches from a ONE state to a ZERO state, a current is induced in the sense line and applied to transformer T1. The output of T1 is applied to a differential amplifier consisting of transistors Q1 and Q2. Base bias voltage V_Z is applied to the bases of Q1 and Q2 via resistors R1 and R2. Transistor Q3 is constant-current source for the differential amplifier and establishes the dc operating point. Voltage V_X establishes the bias for transistor Q3. The output from the differential amplifier is OR'ed at the bases of a threshold detector consisting of Q5 and Q6. The collector of Q2 supplies the base input of Q5, and the collector of Q1 supplies the base input of Q6. This produces a single-polarity output, even though the input waveform is bipolar. The threshold for Q5 and Q6 is set by voltage V_y, which is connected to the emitters of Q5 and Q6. Transistors Q5 and Q6 cannot be switched on unless the base drive exceeds a predetermined level established by V_y. The sense amplifier outputs (SA01 through SA16) are fed through transistor Q1 to register G by strobing Q4 with signal STBE from the strobe driver. Data from fixed memory (40410A through 40417A and 40420A through 40427A) is fed also through Q1 to register G.

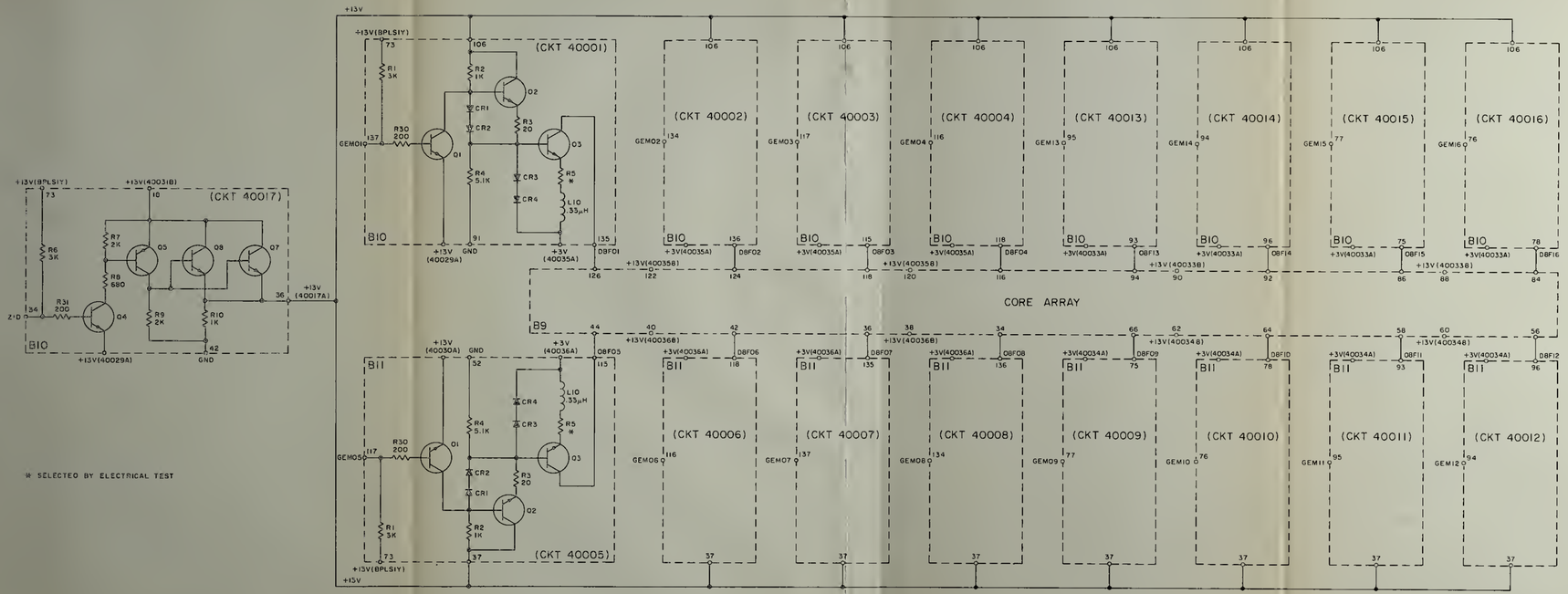
Voltages V_X, V_Y, and V_Z, which are required for sense amplifier operation, are provided by a constant-voltage source. Base bias voltage V_Z is maintained at a constant value by diodes CR1 and CR7 through CR10. Diodes CR2 through CR5 set the operating point for transistors Q3 and Q4. Zener diode CR6 compensates for any changes in B+ to maintain the values of V_X and V_Y relatively constant.

The strobe driver (figure 4-159) receives erasable memory strobe signal SBE and fixed memory strobe signal SBF from their respective memory cycle timing circuits. The strobe signals are amplified and supplied to the appropriate sense amplifiers as signal STBE and STBF. These signals enable data to be transferred from the sense amplifiers to register G.

4-8.6.3 Fixed Memory Functional Description. Fixed memory (figure 4-160) consists of the fixed memory cycle timing circuits, bank register, selection logic, core ropes and drivers, and the sense amplifiers. Memory cycle timing generates the timing signals necessary for fixed memory operation. A location in fixed memory is addressed according to the contents of register S in the central processor and the bank register (register BNK) in fixed memory. The selection logic converts the contents of registers BNK and S into the various signals necessary to select the addressed storage location. The three core ropes which are the storage medium for storing data in fixed memory are designated ropes R, S, and T. A rope consists of two modules, each of which contains four planes. Each plane in a module (figure 4-161) contains 128 cores arranged in a 4-by-32 matrix. The sense amplifiers detect the content of the addressed storage location and supply this data through the sense amplifiers in erasable memory to the central processor.

4-8.6.3.1 Magnetic Core. The characteristics of the magnetic cores used in fixed memory are similar to those of the ferrite cores used in erasable memory. However, the rope core differs from the ferrite core in that it is fabricated from 1/8 mil Mo-perm ribbon wound on a steel bobbin. Use of the Mo-perm ribbon allows the size of the fixed memory core to be large (core diameter is approximately 0.25 inch compared with 0.05 inch of the erasable memory core) without requiring large drive currents, as would be the case if ferrite were used. The larger size is needed to accommodate the number of wires required to thread the rope core (a maximum of 146 wires compared with 4 wires in the ferrite core).

4-8.6.3.2 Fixed Memory Cycle Timing Circuits. Fixed memory cycle timing (figure 4-162) consists of timing control and timing flip-flops. The timing control regulates the generation of timing signals, used for fixed memory operation, by means of signal ROP. Signal ROP is generated when either bit 11 or bit 12 or both are logic ONE's and signal MC is present. Signal ROP occurs for memory addresses above 1777. The timing flip-flops generate the timing signals (figure 4-162) necessary to sequence the operation of fixed memory subject to signals B2 and Q2 from the timer. The timing signals generated are RGENVX (conditions the set and reset circuits), IHENV (inhibit),



* SELECTED BY ELECTRICAL TEST

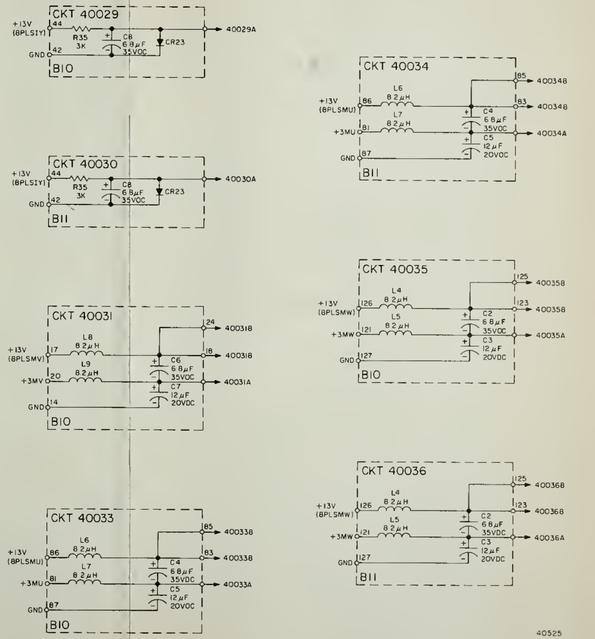


Figure 4-157. Inhibit Line Drivers

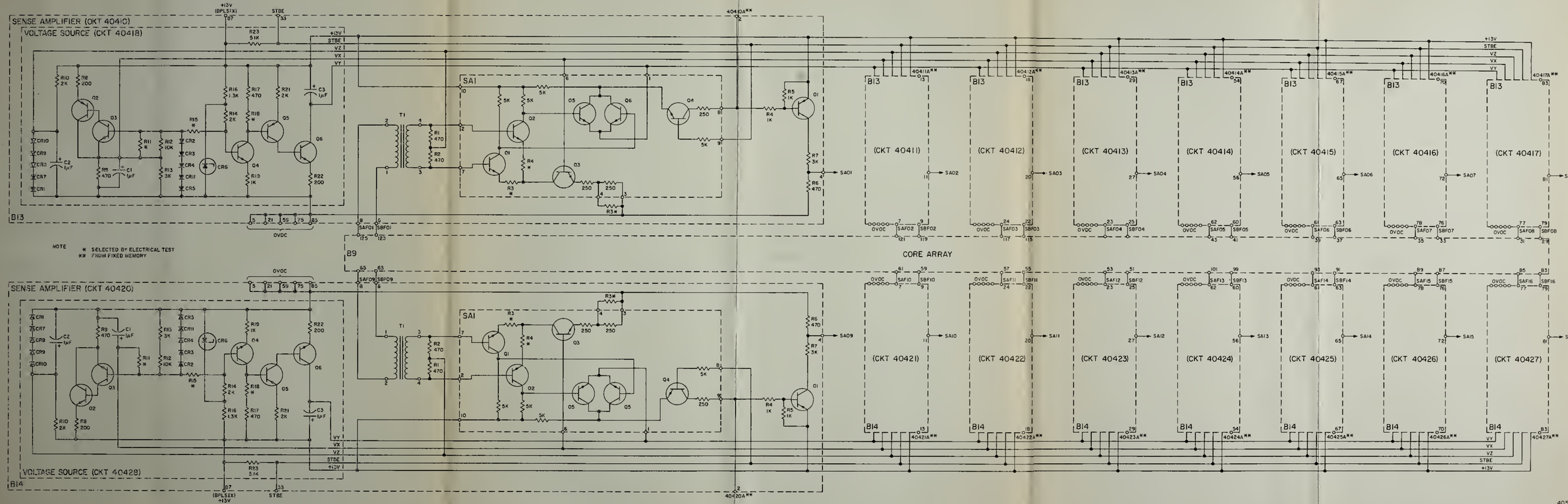


Figure 4-158. Sense Amplifier and Voltage Source

set 2 (set), SBF (enables sense amplifiers), and $\overline{\text{RSTRP}}$ (reset). Signal RGENV is used for enabling the bank selector gates. The generation of the set and inhibit signals is inhibited by signal GOJAM from the timer and the remaining timing signals are inhibited by signal TIMR from the erasable memory cycle timing circuits whenever a monitor stop or alarm condition exists.

4-8.6.3.3 Bank Register. The bank register (figure 4-160) receives its contents on write lines 11 through 14 and 16 from the central processor. When the bank register is addressed (address 0015) and signal $\overline{\text{WSC12}}$ is present, the flip-flop register is cleared by signal CBKG from the clear gates. The contents on the write lines are then entered into the flip-flop register by signal $\overline{\text{WBKG}}$, via signal WSC234 to the write gates. The output from the bank register (R0 through R4, $\overline{\text{R0}}$, $\overline{\text{R1}}$, and $\overline{\text{R2}}$) is supplied to the selection logic where, along with other signals, it selects the proper rope and strand signals. The output from the register is supplied also to the central processor through the read gates, subject to signal $\overline{\text{RSC234}}$.

4-8.6.3.4 Selection Logic. The selection logic (figure 4-160) generates the rope, strand, set, and inhibit signals necessary to select an addressed storage location in fixed memory. The bank selector gates produce the following signals:

(1) One of six rope control signals (RPG1 through RPG6)

(2) $\overline{\text{IL09A}}$ (used for set selection)

(3) IL10A and $\overline{\text{IL10A}}$ (used for strand selection)

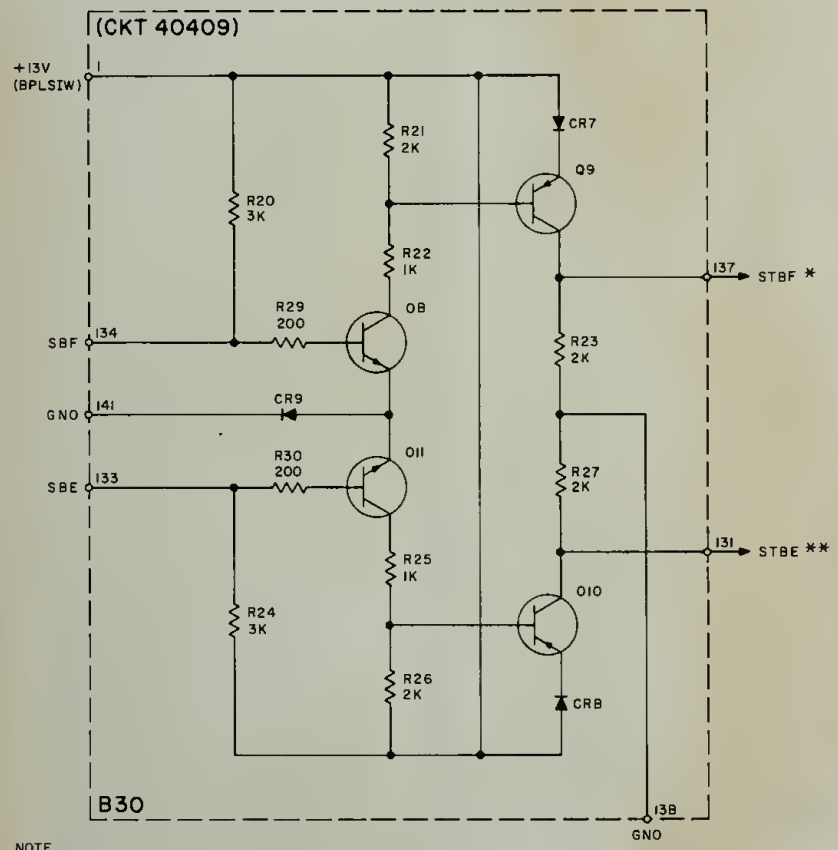
The above signals are produced as a result of signals $\overline{\text{ST11}}$ and $\overline{\text{ST12}}$ from register S, and output signals of the bank register, subject to timing signal RGENV.

A rope is selected by enabling one of three rope return circuits with signals GATER, GATES, and GATET. These signals are produced by the rope selector, subject to the rope control signals.

A sense strand is selected by gating signals GTRS through GTWS from the rope selector with strand gate signals SD00 through SD07 from the strand gates. The strand gate signals are generated by gating signals $\overline{\text{YT0}}$ through $\overline{\text{YT3}}$ from erasable memory with IL10 and $\overline{\text{IL10A}}$. This 6-by-8 combination selects 1 of 48 sense strands.

Set selection is accomplished by gating signals ST08 and $\overline{\text{ST08}}$ with signal $\overline{\text{IL09A}}$ from the bank select gates. The gating actions produce one of four set signals, SET A through SET D, subject to timing signal SET 2.

Inhibit selection is divided into two parts. Bits 1 through 7 of register S and their complements determine which of the 14 inhibit lines is activated, and the remaining two lines are activated by gating bit 9 of register S with signal PARTY 9 from the parity logic in the central processor.



NOTE
* TO ROPE MEMORY SENSE AMPLIFIER CIRCUITS (FIGURE 4-131)
** TO ERASABLE MEMORY SENSE AMPLIFIER CIRCUITS (FIGURE 4-120)

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Figure 4-159. Strobe Driver

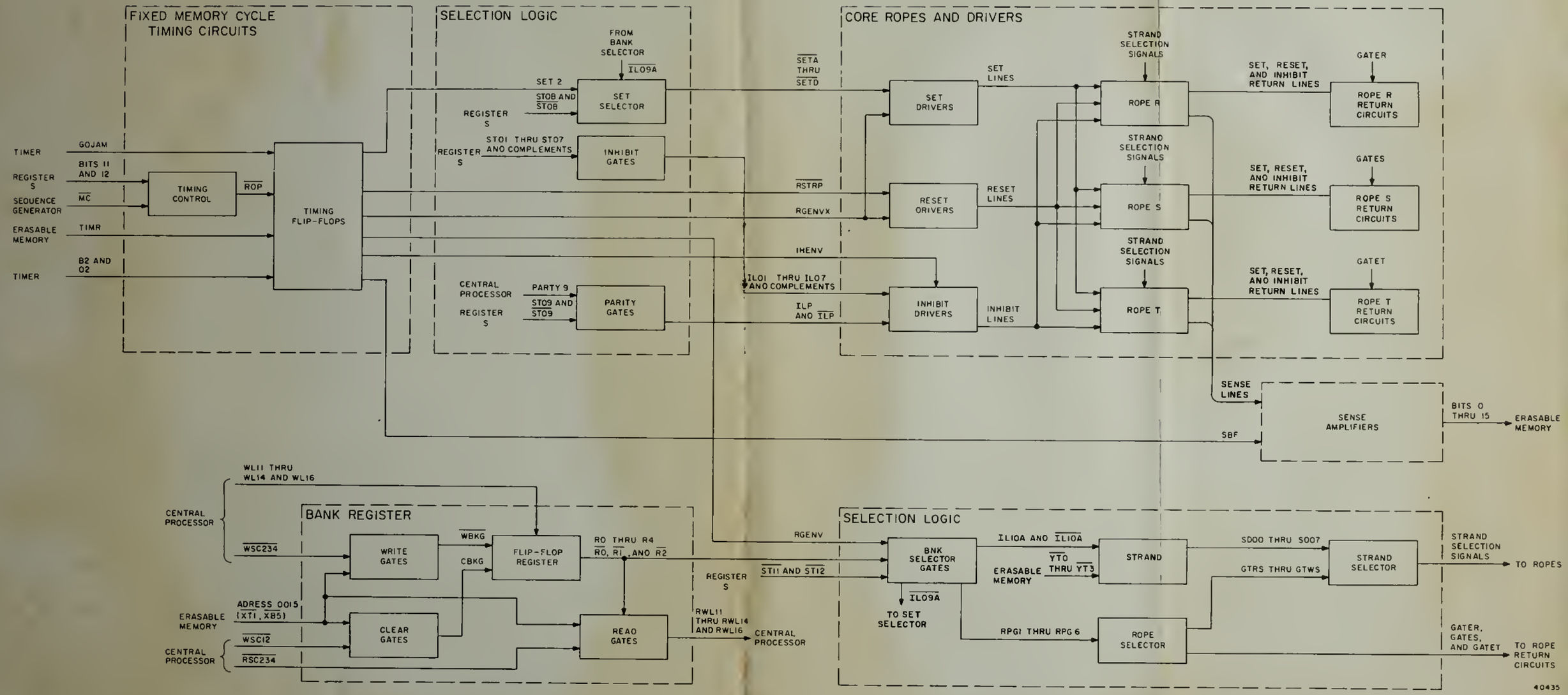


Figure 4-160. Fixed Memory, Functional Diagram

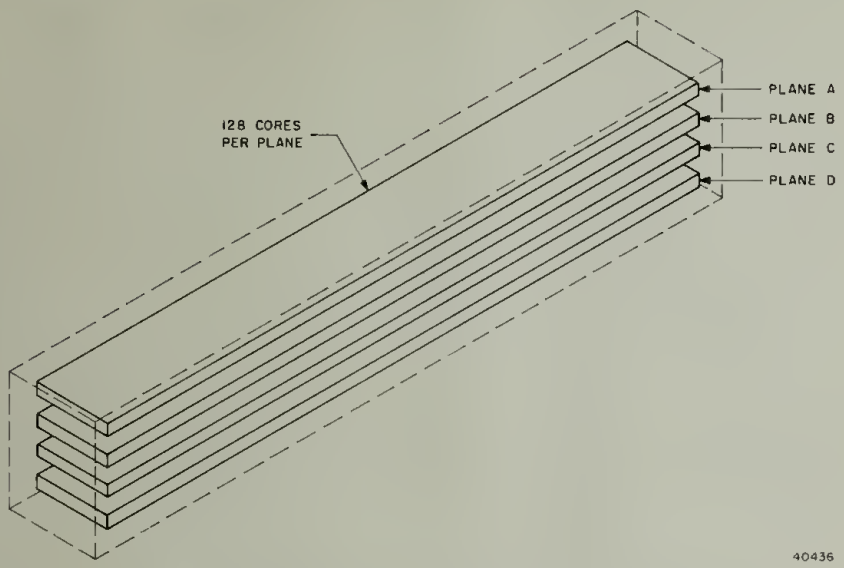


Figure 4-161. Rope Module

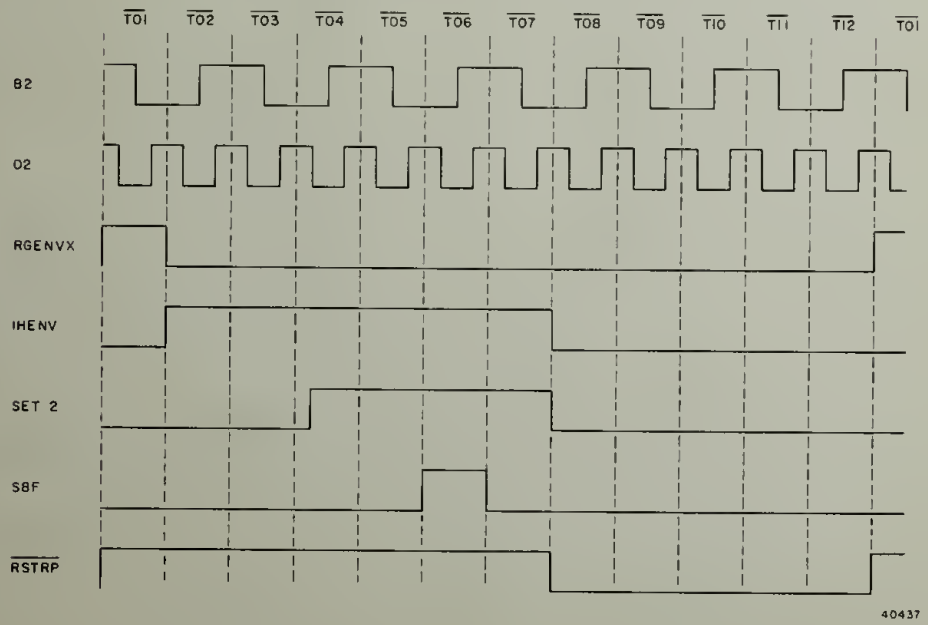


Figure 4-162. Fixed Memory Cycle, Timing Diagram

4-8.6.3.5 Cores, Ropes, and Drivers. As previously stated there are three core ropes in fixed memory designated ropes R, S and T, and each rope (figure 4-163) consists of two modules.

There are 4 set drivers, 2 reset drivers, and 16 inhibit drivers. The set drivers are enabled subject to timing signals RGENVX. The reset drivers are enabled subject to timing signals RGENVX and $\overline{\text{RSTRP}}$. The inhibit drivers are enabled subject to timing signal IHENV. The drive lines (4 set, 2 reset, and 16 inhibit) threading the three ropes are connected in parallel, but return to three separate rope return circuits. Thus a particular rope is selected by enabling the appropriate rope return circuit. This enabling occurs when one of three signals (GATER, GATES, or GATET) from the rope selector is received.

The sense lines threading or bypassing each core are grouped together into strands. A strand consists of 16 sense lines (one per bit), and there are 16 strands per rope for a total of 48 strands in fixed memory. However, only one strand select signal is present at a time. The strands are threaded through a rope such that eight strands thread or bypass all cores in a module (half a rope). Therefore, when any one strand select signal is present, one word (one of eight) of each core in a module is conditioned.

The fourteen inhibit lines, which thread or bypass all cores in a rope, inhibit 127 cores in each plane leaving eight cores (one per plane) available for selection. All cores are threaded by an additional inhibit signal (parity inhibit) or its complement, which is used for noise reduction in the sense lines.

Four set lines thread through each rope (each set line threads all cores in one plane of each module). By enabling one of the four set lines, two of the eight planes in a selected rope are enabled by the set line. The selected strand signal however, threads only one module. Thus, only one of the eight planes is actually selected by a set signal.

The selected word is detected and amplified by 16 sense amplifiers, which are enabled by signal SBF. The reset signal (there are two reset signals, each threads 512 cores) resets the core switched during set time.

The above mentioned selection process occurs as follows:

(1) Rope select, selects 1 of the 3 core ropes R, S, and T when one of three rope return signals (GATER, GATES, or GATET) is received.

(2) Strand select, combination of one strand gate signal and one rope select signal will condition 512 words in a rope module (one word per core).

(3) Inhibit, combination of fourteen signals which will inhibit 508 cores in a rope module leaving one core per plane to be selected.

(4) Set, one of four signals which will set one of the cores not inhibited previously.

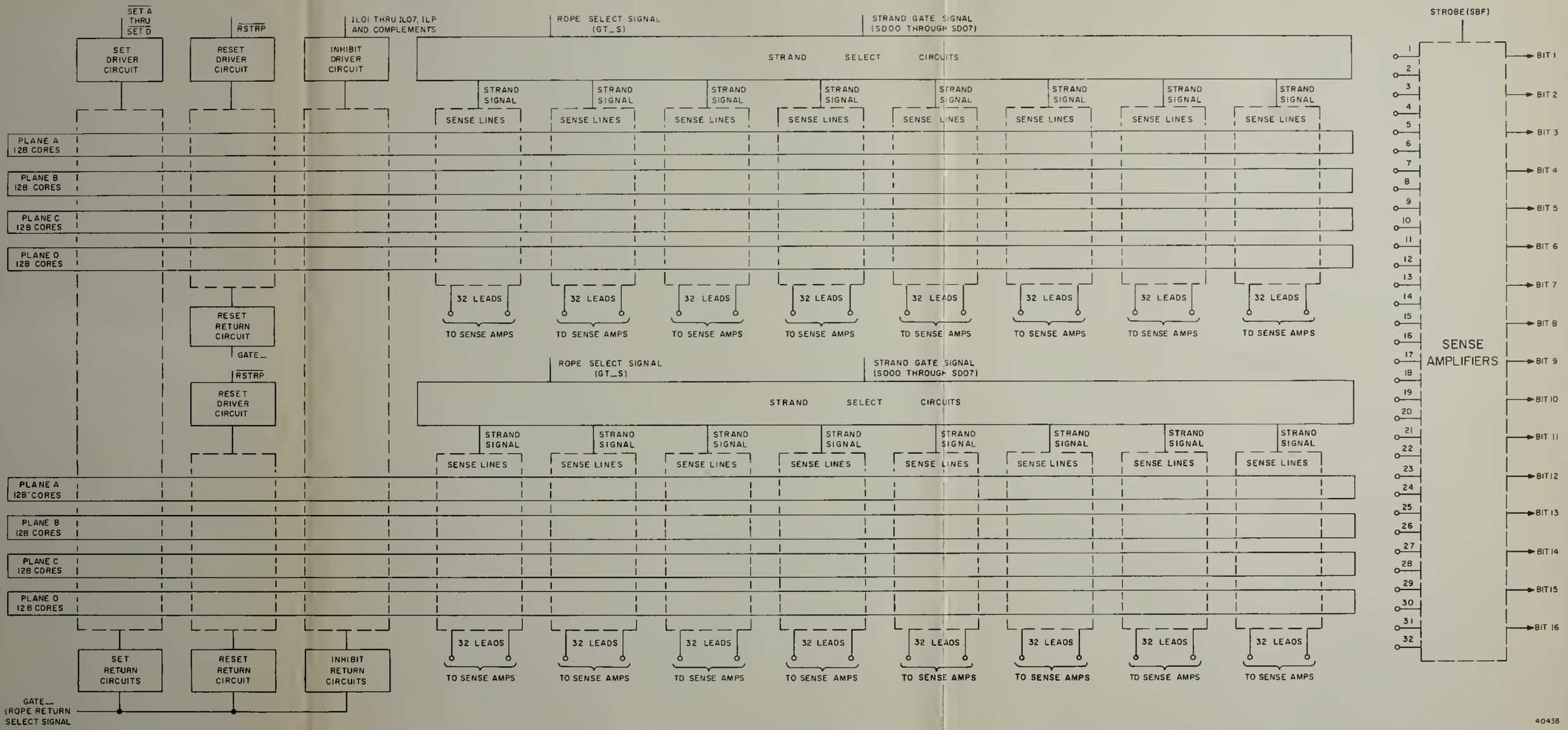


Figure 4-163. Rope Organization

(5) Sense strobe, enabling signal from timing circuits used for the detection of the selected word.

(6) Reset, signal that resets the core, selected during set time, to its normal state.

4-8.6.3.6 Sense Amplifiers. As in erasable memory, there are 16 sense amplifiers in fixed memory. Each amplifier amplifies the data on the selected sense line and forwards the data to erasable memory, when enabled by timing signal SBF.

4-8.6.4 Fixed Memory Detailed Description. Fixed memory is a nondestructive, random-access storage device. Data is wired into fixed memory; therefore, it cannot be altered electrically. Fixed memory consists of core ropes, memory cycle timing, bank register, selection logic, driver and return circuits, and sense amplifiers.

4-8.6.4.1 Core Ropes. A core rope is a storage device in which information is stored by wiring the cores in a unique manner. There are three core ropes in fixed memory: R, S, and T (modules B28 and B29, B21 and B22, B23 and B24 respectively). Each core rope module (figure 4-164) contains four 128-core planes for a total of 512 cores in a rope module.

Each core in a rope module stores eight 16-bit words. A total storage capacity of 24,576 sixteen-bit words is provided by fixed memory. A core is threaded or bypassed by set, reset, inhibit, and sense lines (one per bit). The effect of currents passing through a core via the set, reset, and inhibit lines is additive. The currents in the set lines and the inhibit lines are of opposite polarity; therefore, the set current is cancelled by the inhibit current when the currents are time-coincident. Thus, a core changes state at set time if none of the inhibit lines threading the core is carrying current. When a core changes state, current is induced into all the sense lines threading the core. The sense lines bypassing the core receive no curent. In this manner the sense lines associated with each core receive the same words each time the core is set. A core is reset when current flows through the reset line.

Inhibit signals IL01 through IL07 and their complements are sufficient to select one core in each plane. A core is selected by inhibiting all but one core in each plane. Inhibit signals ILP and $\overline{\text{ILP}}$ ensure that all but the selected core are inhibited by at least two signals and thus the noise in the sense lines is reduced. Four set lines thread each core rope, and each set line threads all cores of one plane in each rope module. Only one set signal is present at set time, and that signal is selected by address. The sense lines threading or bypassing each core are grouped into strands. A strand consists of the sense lines necessary to detect one 16-bit word. There are 8 strands per rope module, for a total of 48 strands in fixed memory. With the application of a rope select signal (one of six) and a strand select signal (one of eight), a particular strand (one of forty eight) is selected. The matched diodes shown on the sense lines (figure 4-164) are used for bipolar operation.

4-8.6.4.2 Fixed Memory Cycle Timing. Fixed memory cycle timing (figure 4-165) consists of several flip-flops and gates on modules A33 and A34 which produce the timing signals necessary to perform the set, reset, inhibit, and sensing functions in fixed memory. As In erasable memory all the timing pulses are generated in one memory cycle time (11.97 microsecond). A logic ONE in either bit position 11 or 12, or both, indicates that fixed memory is addressed. This condition, coincident with signal $\overline{MC}$, produces rope condition signal $\overline{ROP}$. Signal $\overline{ROP}$ must be present to generate the fixed memory timing signals.

The waveforms for fixed memory cycle timing are illustrated in figure 4-162. At time 2, FF52325-52326 Is set by signal GTON and generates output RGENV and RGENVX. These outputs are present until time 1 of the next memory cycle. Signal RGENV enables the bank selector gates in the selection logic. Signal RGENVX is the condltioning signal for the set and reset driver clrcults. Also at time 2 as a function of GTON, inhlbit signal IHENV is generated. This slgnal is present until time 8 and enables the inhibit drivers in the driver and return circuits to allow inhibit current to flow through the selected inhibit line.

At time 4 (coincident with $\overline{Q2X}$ from the timer) signal SET 2 is generated (FF53328-53329) and enables the set selector circuits. At time 6, strobe signal SBF (approxlmately 1 microsecond in duratlon) is generated and enables the sense amplifiers. At tlme 8 the inhibit signal IHENV and the SET 2 signal are reset. Coincident with this actlon, reset signal $\overline{RSTRP}$ is generated which enables the reset drivers and allows current to flow in the reset lines.

4-8.6.4.3 Bank Register. A location In fixed memory is addressed according to the contents of register S and the bank register (BNK). Register BNK (figure 4-166) is a 5-bit addressable fllp-flop register. Clear (CBKG), write ($\overline{WBKG}$), and read ($\overline{RBKG}$) pulses are generated when slgnals XT1 and XB5 (address 0015) are coincident with control pulses $\overline{WSC12}$, $\overline{WSC234}$, and $\overline{RSC234}$, respectlvely. Signal CBKG clears register BNK before bits 16 and 14 through 11 enter the register on write lines WL16 and WL14 through WL11, subject to signal $\overline{WBKG}$. If the data on the write lines is a ZERO, the associated bit position in register BNK remains cleared. The contents of the register are supplied to the bank selector (subject to signal $\overline{RBKG}$) as signals R0 through R4, $\overline{R0}$, $\overline{R1}$, and $\overline{R2}$ and to the central processor as signals RWL16 and RWL14 through RWL11.

4-8.6.4.4 Selection Logic. The selection logic converts the contents of registers S and BNK into the various signals necessary to select the addressed storage location. Fixed memory has the capability of addressing 32 banks; however, there are only 24 banks physically available for use. The flrst two banks (table 4-XIV) are designated fixed-fixed (FF) memory and the remaining 22 banks are designated fixed-switchable (FS) memory. Whenever a location in FF memory is addressed, a ONE in either bit position 11 or 12, is present in register S. A location in FS memory Is addressed when both bit positions 11 and 12 contain a ONE. Locations in FF memory and bank 03 of FS memory are addressed by the content of blt positlons 12 through 1 of reglster S.

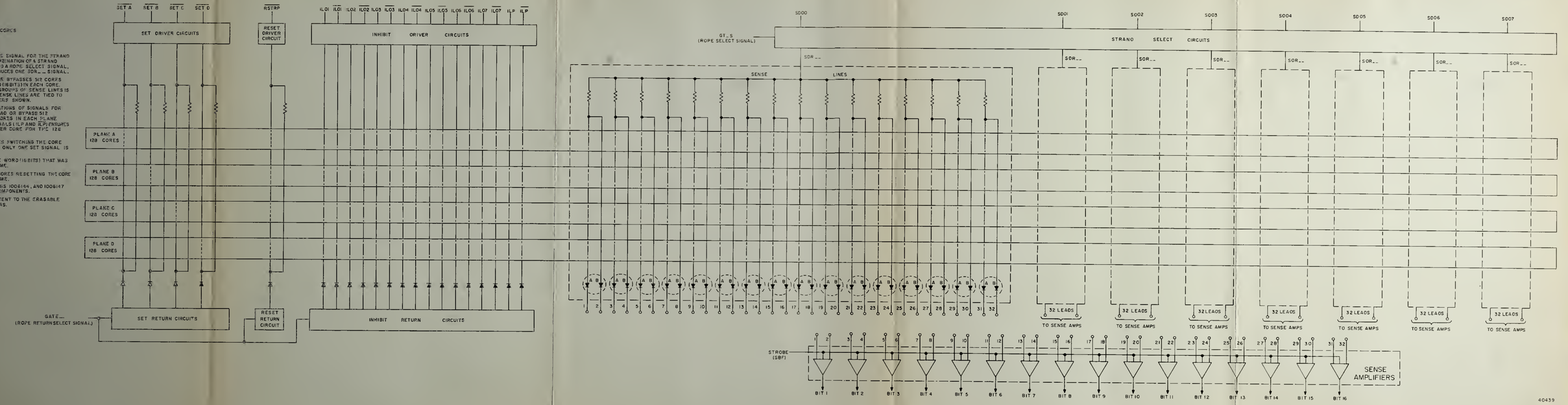


Figure 4-164. Rope Module Organization

Table 4-XIV. Addressing

				Octal Address		Pseudo Address (Decimal)	Contents of BNK*					Contents of S*											
				Real	Pseudo		15	14	13	12	11	12	11	10	9	8	7	6	5	4	3	2	1
F	F_1	FF	BANK 01	3600 3777	Same	1024 2047	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X
			02	4000 5777	Same	2048 3071	X	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X	X
			03	6000 7777	6000 7777	3072 4095	0	0	0	X	X	1	1	X	X	X	X	X	X	X	X	X	X
			04	6000 7777	10000 11777	4096 5119	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			05	6000 7777	12000 13777	5120 6143	0	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			06	6000 7777	14000 15777	6144 7167	0	0	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			07	6000 7777	16000 17777	7168 8191	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			10	6000 7777	20000 21777	8192 9215	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			11	6000 7777	22000 23777	9216 10239	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			12	6000 7777	24000 25777	10240 11263	0	1	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			13	6000 7777	26000 27777	11264 12287	0	1	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			14	6000 7777	30000 31777	12288 13311	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X
	F_2		21	6000 7777	42000 43777	17408 18431	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			22	6000 7777	44000 45777	18432 19455	1	0	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			23	6000 7777	46000 47777	19456 20479	1	0	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			24	6000 7777	50000 51777	20480 21503	1	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			25	6000 7777	52000 53777	21504 22527	1	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			26	6000 7777	54000 55777	22528 23551	1	0	1	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			27	6000 7777	56000 57777	23552 24575	1	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X
	F_3		30	6000 7777	60000 61777	24576 25599	1	1	0	0	0	1	1	X	X	X	X	X	X	X	X	X	X
			31	6000 7777	62000 63777	25600 26623	1	1	0	0	1	1	1	X	X	X	X	X	X	X	X	X	X
			32	6000 7777	64000 65777	26624 27647	1	1	0	1	0	1	1	X	X	X	X	X	X	X	X	X	X
			33	6000 7777	66000 67777	27648 29671	1	1	0	1	1	1	1	X	X	X	X	X	X	X	X	X	X
			34	6000 7777	70000 71777	29672 30695	1	1	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X

*X means 0 or 1

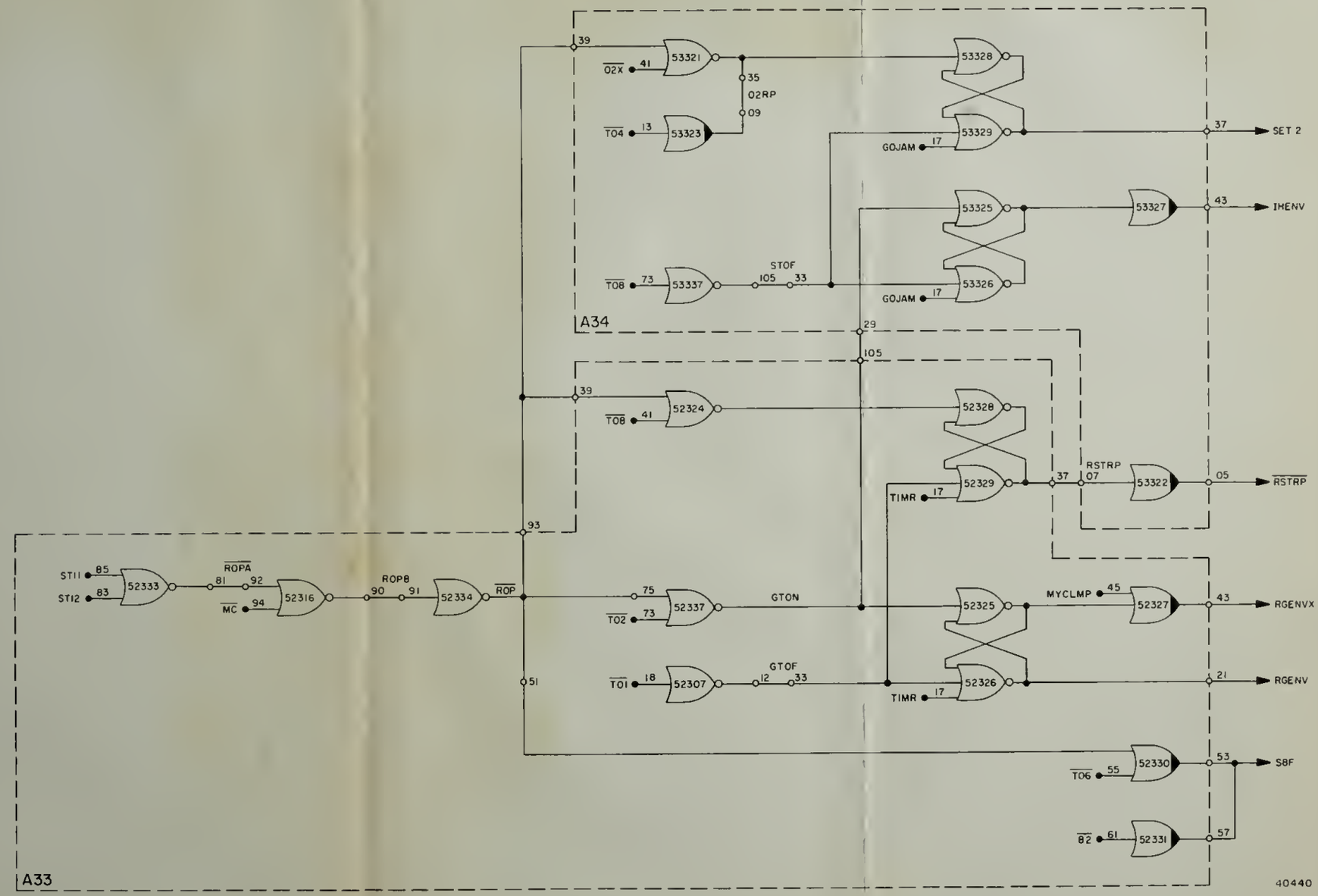
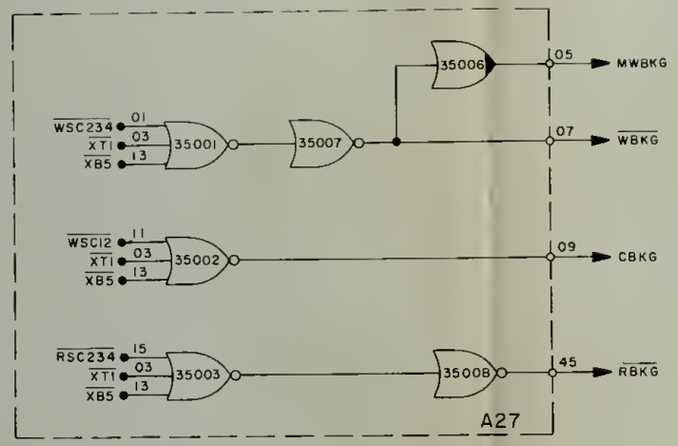


Figure 4-165. Memory Cycle Timing, Fixed



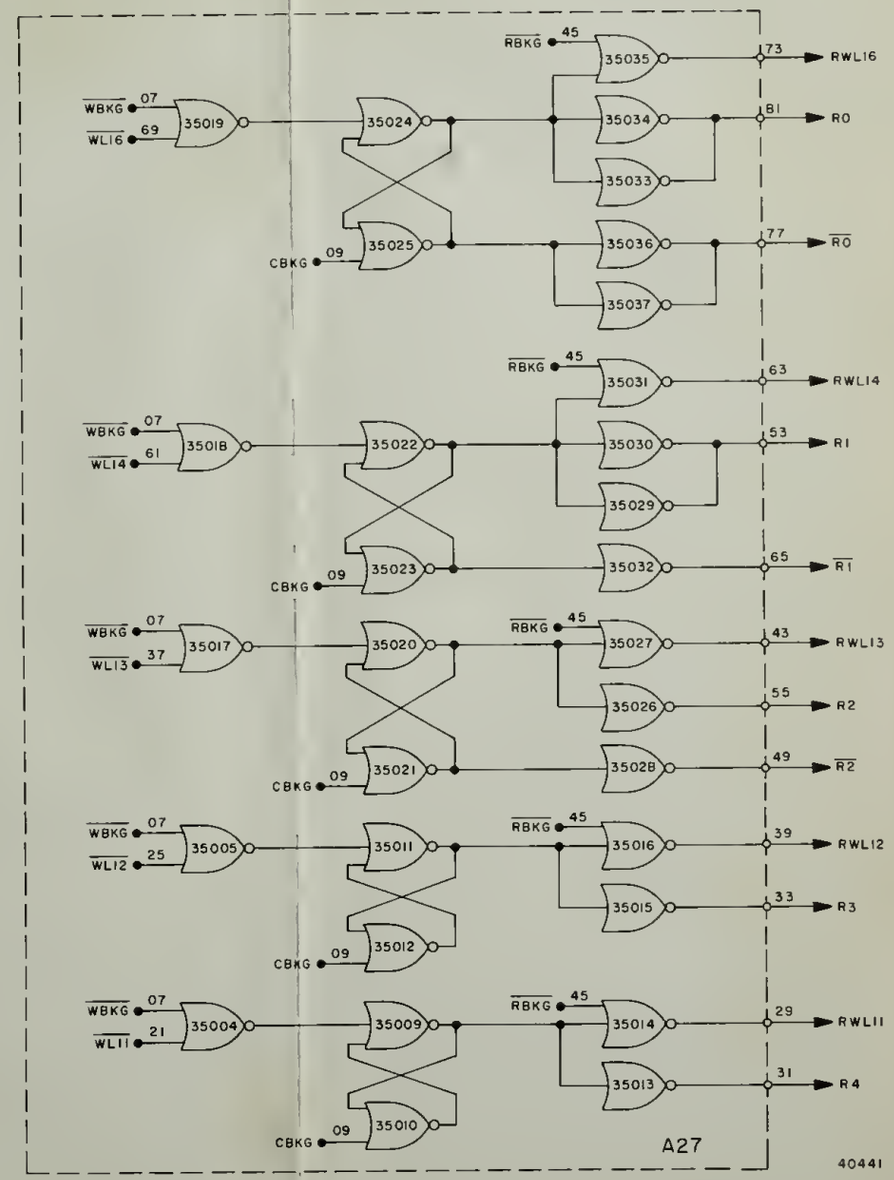


Figure 4-166. Bank Register

The remaining locations in FS memory are addressed by the content of both registers BNK and S. The content of bit positions R4 through R0 of register BNK determines which bank (octal 04 through 34 with some exceptions) in FS memory is being addressed and the content of bit positions 10 through 1 of register S determines which location within the bank is being addressed.

Table 4-XV lists all the pseudo octal addresses for fixed memory. Although the addresses are pseudo to computer operation they are real for manual addressing via the DSKY's. Included in the table are the sets, strands, and banks associated with each of the locations. The inhibit combinations are too numerous for inclusion in the table.

The bank selector gates (figure 4-167) sense the state of signals R0 through R4, $\overline{R0}$, $\overline{R1}$, and $\overline{R2}$ of register BNK and signals $\overline{ST11}$ and $\overline{ST12}$ from register S. This sensing operations results in the generation of one of six rope control signals (RPG1 through RPG6). The bank selector gates also generate set enabling signal $\overline{IL09A}$ and strand enabling signals IL10A and $\overline{IL10A}$, as a result of the inputs from register BNK and S. The above signals select one of 24 banks in fixed memory subject to timing signal RGENV. Each bank consists of 1024 word locations. Table 4-XVI illustrates the relationship between the inputs and outputs of the bank selector gates and the associated bank.

The generation of an RPG signal is inhibited if signal MYCLMP is a logic ONE. Signal MYCLMP is a logic ONE only when the dc voltages supplied to memory are not within tolerance. If input signals R0 through R4, $\overline{R0}$, $\overline{R1}$ and $\overline{R2}$ do not represent a valid address, signal BAL1 (bank alarm one) or BAL2 is produced. These two signals are inverted and supplied to the CTS as signal $\overline{MBAL}$.

The set selector (figure 4-168) gates signals ST08 and $\overline{ST08}$ from register S with signal $\overline{IL09A}$ from the bank selector gates. By combining these inputs, one of four set signals ($\overline{SET\ A}$, $\overline{SET\ B}$, $\overline{SET\ C}$, or $\overline{SET\ D}$) will be generated subject to timing signal SET 2. The selected set signal is supplied to the set lines through driver circuits.

The seven low-order bits (ST07 through ST01) of register S and their complements are inverted by the inhibit gates (figure 4-169) and are applied to the inhibit lines through driver circuits. Signal ST09 of register S is gated by signal PARTY 9 from the parity tree in the parity gates (figure 4-169) to produce the parity inhibit signal (ILP) and its complement. The parity inhibit lines thread the cores, through driver circuits, to reduce noise in the sense lines. The PARTY 9 signal represents an even number of ONE's in bits 9 through 1 of the address sent to the parity block.

The strand gates (figure 4-170) receive signals ST09, ST10 and their complements from register S and signals IL10 and $\overline{IL10A}$ from the bank selector gates. Combinations of these signals will produce one of eight strand gate signals designated SD00 through SD07. Table 4-XVII illustrates the manner in which the input signals are combined to produce the strand gate signals.

Table 4-XV. Bank Addressing

Pseudo Octal Address	Rope R			Pseudo Octal Address	Rope S		
	Set	Strand	Bank		Set	Strand	Bank
02000-02177	C	00	01	12000-12177	C	08	05
02200-02377	D	00	01	12200-12377	D	08	05
02400-02577	C	01	01	12400-12577	C	09	05
02600-02700	D	01	01	12600-12777 (3)	D	09	05
03000-03177 (1)	C	02	01	13000-13177	C	10	05
03200-03377	D	02	01	13200-13377	D	10	05
03400-03577	C	03	01	13400-13577	C	11	05
03600-03777	D	03	01	13600-13777	D	11	05
04000-04177	A	04	02	14000-14177	A	12	06
04200-04377	B	04	02	14200-14377	B	12	06
04400-04577	A	05	02	14400-14577	A	13	06
04600-04777	B	05	02	14600-14777	B	13	06
05000-05177	A	06	02	15000-15177	A	14	06
05200-05377	B	06	02	15200-15377	B	14	06
05400-05577	A	07	02	15400-15577	A	15	06
05600-05777 (2)	B	07	02	15600-15777 (4)	B	15	06
06000-06177	C	04	03	16000-16177	C	12	07
06200-06377	D	04	03	16200-16377	D	12	07
06400-06577	C	05	03	16400-16577	C	13	07
06600-06777	D	05	03	16600-16777	D	13	07
07000-07177	C	06	03	17000-17177	C	14	07
07200-07377	D	06	03	17200-17377	D	14	07
07400-07577	C	07	03	17400-17577	C	15	07
07600-07777	D	07	03	17600-17777	D	15	07
10000-10177	A	00	04	20000-20177	A	08	10
10200-10377	B	00	04	20200-20377	B	08	10
10400-10577	A	01	04	20400-20577	A	09	10
10600-10777 (1)	B	01	04	20600-20677 (3)	B	09	10
11000-11177	A	02	04	21000-21177	A	10	10
11200-11377	B	02	04	21200-21377	B	10	10
11400-11577	A	03	04	21400-21577	A	11	10
11600-11777	B	03	04	21600-21777	B	11	10

(1) B28, (2) B29, (3) B21, and (4) B22

(Sheet 1 of 3)

Table 4-XV. Bank Addressing (cont)

Pseudo Octal Address	Rope T			Pseudo Octal Address	Rope R		
	Set	Strand	Bank		Set	Strand	Bank
22000-22177	C	16	11	42000-42177	C	24	21
22200-22377	D	16	11	42200-42377	D	24	21
22400-22577	C	17	11	42400-42577	C	25	21
22600-22777 (5)	D	17	11	42600-42777 (1)	D	25	21
23000-23177	C	18	11	43000-43177	C	26	21
23200-23377	D	18	11	43200-43377	D	26	21
23400-23577	C	19	11	43400-43577	C	27	21
23600-23777	D	19	11	43600-43777	D	27	21
24000-24177	A	20	12	44000-44177	A	28	22
24200-24377	B	20	12	44200-44377	B	28	22
24400-24577	A	21	12	44400-44577	A	29	22
24600-24777	B	21	12	44600-44777	B	29	22
25000-25177	A	22	12	45000-45177	A	30	22
25200-25377	B	22	12	45200-45377	B	30	22
25400-25577	A	23	12	45400-45577	A	31	22
25600-25777 (6)	B	23	12	45600-45777 (2)	B	31	22
26000-26177	C	20	13	46000-46177	C	28	23
26200-26377	D	20	13	46200-46377	D	28	23
26400-26577	C	21	13	46400-46577	C	29	23
26600-26777	D	21	13	46600-46777	D	29	23
27000-27177	C	22	13	47000-47177	C	30	23
27200-27377	D	22	13	47200-47377	D	30	23
27400-27577	C	23	13	47400-47577	C	31	23
27600-27777	D	23	13	47600-47777	D	31	23
30000-30177	A	16	14	50000-50177	A	24	24
30200-30377	B	16	14	50200-50377	B	24	24
30400-30577	A	17	14	50400-50577	A	25	24
30600-30777 (5)	B	17	14	50600-50777 (1)	B	25	24
31000-31177	A	18	14	51000-51177	A	26	24
31200-31377	B	18	14	51200-51377	B	26	24
31400-31577	A	19	14	51400-51577	A	27	24
31600-31777	B	19	14	51600-51777	B	27	24

(1) B28, (2) B29, (5) B23, and (6) B24

Table 4-XV. Bank Addressing (cont)

Pseudo Octal Address	Rope S			Pseudo Octal Address	Rope T		
	Set	Strand	Bank		Set	Strand	Bank
52000-52177	C	32	25	62000-62177	C	40	31
52200-52377	D	32	25	62200-62377	D	40	31
52400-52577	C	33	25	62400-62577	C	41	31
52600-52777	D	33	25	62600-62777	D	41	31
53000-53177	C	34	25	63000-63177	C	42	31
53200-53377	D	34	25	63200-63377	D	42	31
53400-53577	C	35	25	63400-63577	C	43	31
53600-53777	D	35	25	63600-63777	D	43	31
54000-54177	A	36	26	64000-64177	A	44	32
54200-54377	B	36	26	64200-64377	B	44	32
54000-54577	A	37	26	64400-64577	A	45	32
54600-54777	B	37	26	64600-64777	B	45	32
55000-55177	A	38	26	65000-65177	A	46	32
55200-55377	B	38	26	65200-65377	B	46	32
55400-55577	A	39	26	65400-65577	A	47	32
55600-55777	B	39	26	65600-65777	B	47	32
56000-56177	C	36	27	66000-66177	C	44	33
56200-56377	D	36	27	66200-66377	D	44	33
56400-56577	C	37	27	66400-66577	C	45	33
56600-56777	D	37	27	66600-66777	D	45	33
57000-57177	C	38	27	67000-67177	C	46	33
57200-57377	D	38	27	67200-67377	D	46	33
57400-57577	C	39	27	67400-67577	C	47	33
57600-57777	D	39	27	67600-67777	D	47	33
60000-60177	A	32	30	70000-70177	A	40	34
60200-60377	B	32	30	70200-70377	B	40	34
60400-60577	A	33	30	70400-70577	A	41	34
60600-60777	B	33	30	70600-70777	B	41	34
61000-61177	A	34	30	71000-71177	A	42	34
61200-61377	B	34	30	71200-71377	B	42	34
61400-61577	A	35	30	71400-71577	A	43	34
61600-61777	B	35	30	71600-71777	B	43	34

△3 B21, △4 B22, △5 B23, and △6 B24

(Sheet 3 of 3)

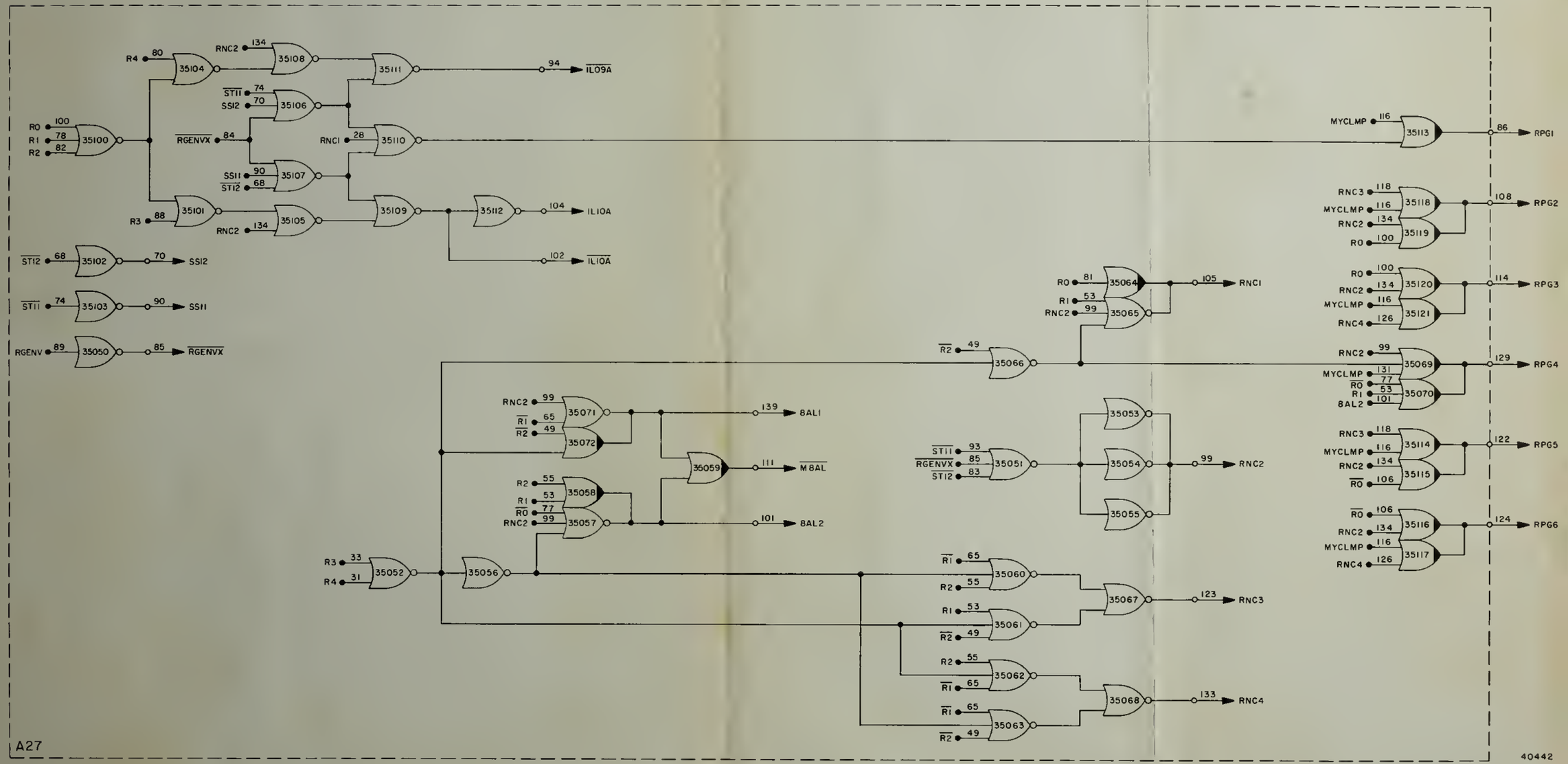


Figure 4-167. Bank Selector Gates

Table 4-XVI. Selector Gates - Inputs and Outputs

Register BNK					Register S		Set Enable Signal	Strand Enable Signal	Rope Control Signal	Bank
Input Bit										
16	14	13	12	11						
Output Signal*					Bit					
R0	R1	R2	R3	R4	12	11	$\overline{IL09A}$	IL10A		
x	x	x	x	x	0	1	1	0	RPG1	01
x	x	x	x	x	1	0	0	1	RPG1	02
0	0	0	x	x	1	1	1	1	RPG1	03
0	0	1	0	0	1	1	0	0	RPG1	04
0	0	1	0	1	1	1	1	0	RPG2	05
0	0	1	1	0	1	1	0	1	RPG2	06
0	0	1	1	1	1	1	1	1	RPG2	07
0	1	0	0	0	1	1	0	0	RPG2	10
0	1	0	0	1	1	1	1	0	RPG3	11
0	1	0	1	0	1	1	0	1	RPG3	12
0	1	0	1	1	1	1	1	1	RPG3	13
0	1	1	0	0	1	1	0	0	RPG3	14
1	0	0	0	1	1	1	1	0	RPG4	21
1	0	0	1	0	1	1	0	1	RPG4	22
1	0	0	1	1	1	1	1	1	RPG4	23
1	0	1	0	0	1	1	0	0	RPG4	24
1	0	1	0	1	1	1	1	0	RPG5	25
1	0	1	1	0	1	1	0	1	RPG5	26
1	0	1	1	1	1	1	1	1	RPG5	27
1	1	0	0	0	1	1	0	0	RPG5	30
1	1	0	0	1	1	1	1	0	RPG6	31
1	1	0	1	0	1	1	0	1	RPG6	32
1	1	0	1	1	1	1	1	1	RPG6	33
1	1	1	0	0	1	1	0	0	RPG6	34

* x means 0 or 1

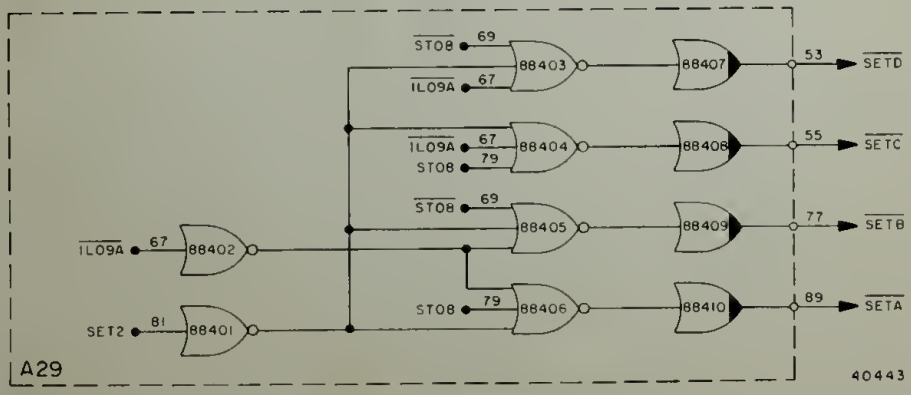


Figure 4-168. Set Selector Gates

Table 4-XVII. Strand Gate Input and Output Signals

ST10	ST09	IL10	SD
0	0	0	00
0	1	0	01
1	0	0	02
1	1	0	03
0	0	1	04
0	1	1	05
1	0	1	06
1	1	1	07

Since there are a total of 48 sense strands in fixed memory and 8 strands thread each rope module, a selection system is required to select the proper rope module and strand to read out data. This selection process is performed by the rope and strand selectors (figure 4-171). There are three identical rope selector circuits, and each circuit receives two RPG signals. However, only one signal is present at a time. In addition, there are eight strand selector circuits, each consisting of six gates. Each strand selector gate receives one of eight SD signals from the strand gates and one of six GTS signals from the rope selectors. This 6-by-8 combination selects the proper sense strand from among 48 possibilities. For simpliciation only one rope selector circuit (40501) and one strand selector circuit (40401) are discussed.

Assuming RPG1 (circuit 40501) to be a logic ONE, transistors Q1 and Q3 conduct, which results in signal GTRS (+13 vdc) being applied to CR1 in the eight strand selectors. In addition, diode CR1 in the rope selector is forward-biased, which enables the rope R return circuits with signal GATER. Thus, one rope return circuit is enabled, and eight gates (one per strand selector) are conditioned to be enabled. The application of a strand gate signal determines which of the eight gates is enabled. Assuming signal SD00 (circuit 40401) to be a logic ONE, transistors Q1 and Q2 conduct and sense strand SDR00 is selected. Table 4-XVIII illustrates the manner in which the 48 strand-select signals are produced as a result of combining the RPG and SD signals.

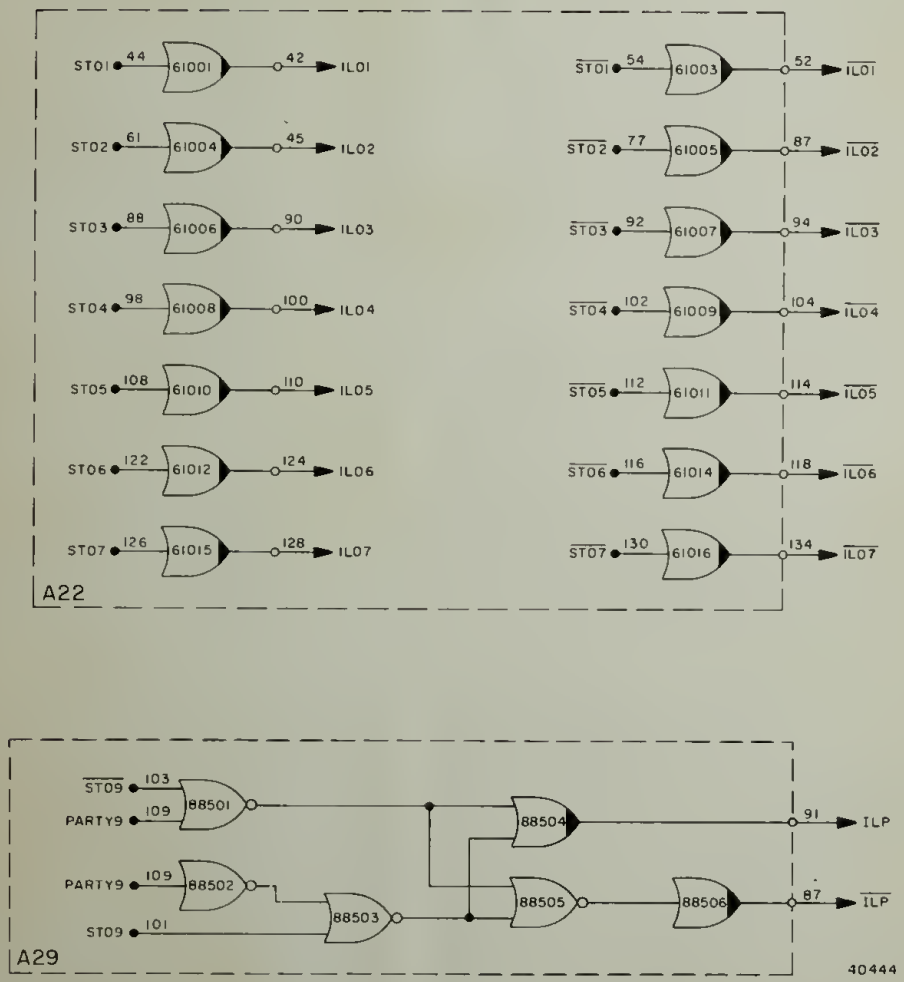


Figure 4-169. Inhibit Gates

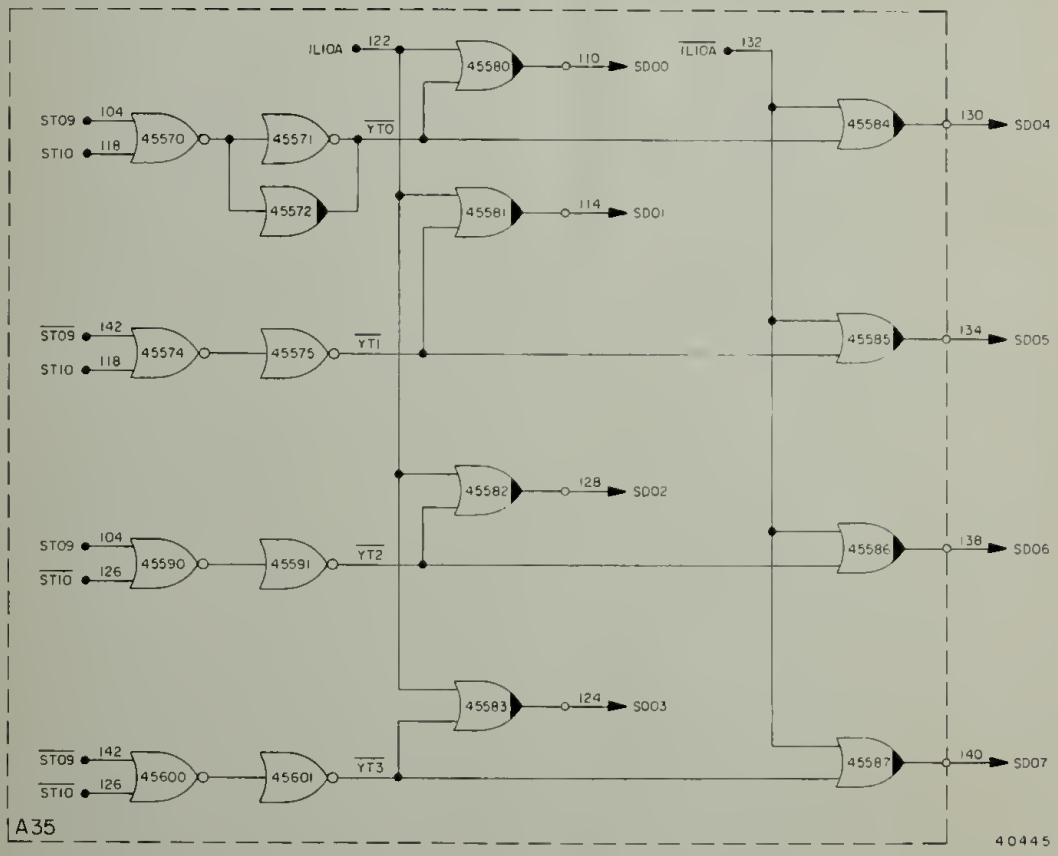


Figure 4-170. Strand Gates

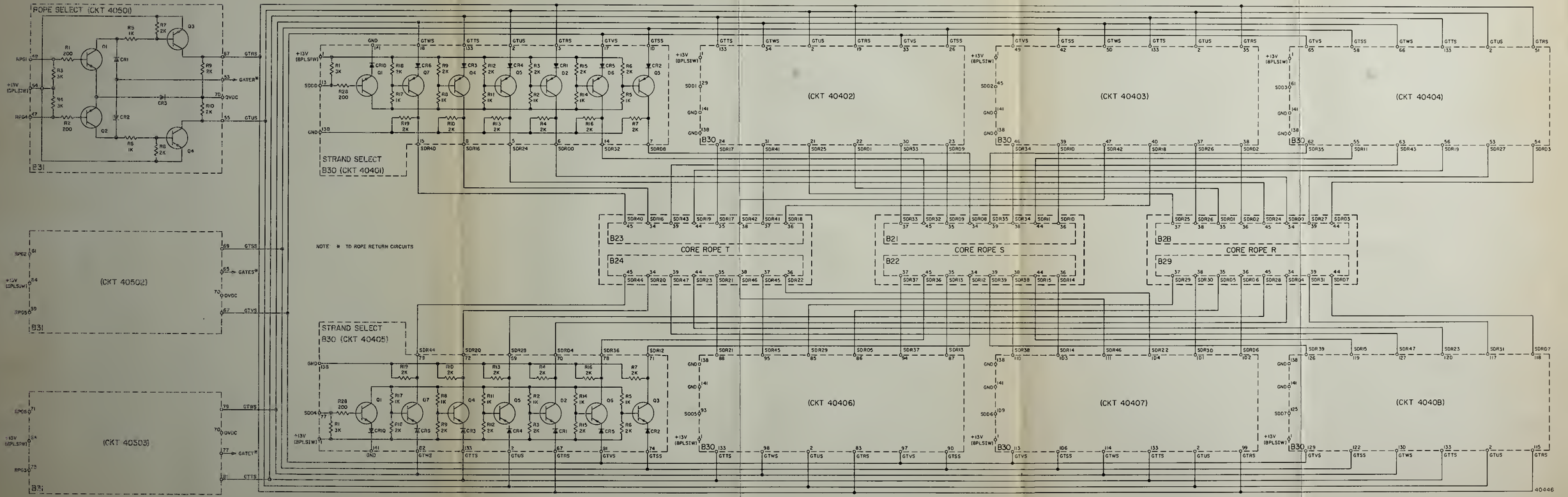


Figure 4-171. Rope and Strand Selectors

4-8.6.4.5 Driver and Return Circuits. The set, reset, and inhibit lines threading or by-passing the three ropes are connected in parallel, but return to three separate rope return circuits (figure 4-160). Each line is driven by a separate driver circuit, and all lines which are common to a particular rope are treutnred to an associated circuit. There are 16 inhibit drivers, 4 set drivers, and 2 reset drivers.

The 16 inhibit drivers (figure 4-172) are enabled subject to signals IL01 through 1L07 and their complements, and signal 40331A (+13 vdc). Signal 40331A (circuit 40331) is generated subject to timing signal 1HENV. Input signal IHENV turns on transistor Q15 which in turn will cause transistor Q16 to conduct and supply +13 vdc to the base of emitter follower Q17. The output of Q17 (40331A) is supplied to all sixteen inhibit drivers. For simplication only one inhibit driver (circuit 40311) and one inhibit return (circuit 40353) are discussed.

Assuming signal IL01 (circuit 40311) to be a logic ZERO and signal 40331A to be present, transistor Q1 is cut off by signal IL01 and transistor Q2 is turned on by signal 40331A. Simultaneously, signal GATET (circuit 40353) is a logic ZERO, transistor Q18 is turned on, which will then turn on emitter follower transistors Q19 and Q20 and supply +13 vdc to diodes CR29 through CR36. Thus, the above operation provides a current path from +13 vdc (B+) through transistor Q19, diode CR29, core rope T, transistor Q2, resistor R4, and inductor L1 to +3 vdc (B-).

The 4 set drivers (figure 4-173) are enabled subject to signals SET A, SET B, SET C, and SET D and signal 40332A (+13 vdc). Signal 40332A (circuit 40332) is generated subject to timing signal RGENVX. The operation of circuit 40332 is identical to circuit 40331 (inhibit) previously discussed. The output of Q17 (40332A) is supplied to all four set drivers. For simplification only set driver (circuit 40361) and one set return (circuit 40351) are discussed.

Assuming signal SET A (circuit 40361) to be a logic ZERO and signal 40332A to be present, transistor Q3 is cut off by signal SET A and emitter follower transistor Q4 is turned on by signal 40332A. Transistor Q4 then turns on transistors Q5 and Q6 which connect signal XSETAD to the three core ropes and to three of the six return circuits. Signal XSETAD is connected to the return circuits for reduction of noise on the set lines. Simultaneously, signal GATER (circuit 40351) is a logic ZERO and transistor Q7 is turned on which will then turn on emitter follower transistor Q10 and supply +13 vdc to diodes CR16 and CR17. This operation provides a current path from +13 vdc (B+) through transistors Q7 and Q10, diode CR16, core rope R, transistors Q5 and Q6, resistors R10 and R11 and inductors L2 and L3 to +3 vdc (B-).

The two reset drivers (figure 4-174) are enabled by timing signal RSTRP. The operation of the reset circuits and the set circuits is similar. Reset circuits 40332, 40367, and 40352 function the same as set circuits 40332, 40361, and 40351, respectively. However a difference exists in current path operation. When signal RSTRP is received and signal 40332A is present both circuits 40367 and 40368 are activated. This connects XRST1N and XRST2N to two separate rope return circuits. If signal GATES (circuits 40352 and 40355) is a logic ZERO, it will provide two current paths for reset operation.

Table 4-XVIII. Rope and Strand Selection Signals

Rope Control	Rope Return	Strand Gate	Sense Strand
RPG1	GATER	SD00 through SD07	SDR00 through SDR07
RPG2	GATES	SD00 through SD07	SDR08 through SDR15
RPG3	GATET	SD00 through SD07	SDR16 through SDR23
RPG4	GATER	SD00 through SD07	SDR24 through SDR31
RPG5	GATES	SD00 through SD07	SDR32 through SDR39
RPG6	GATET	SD00 through SD07	SDR40 through SDR47

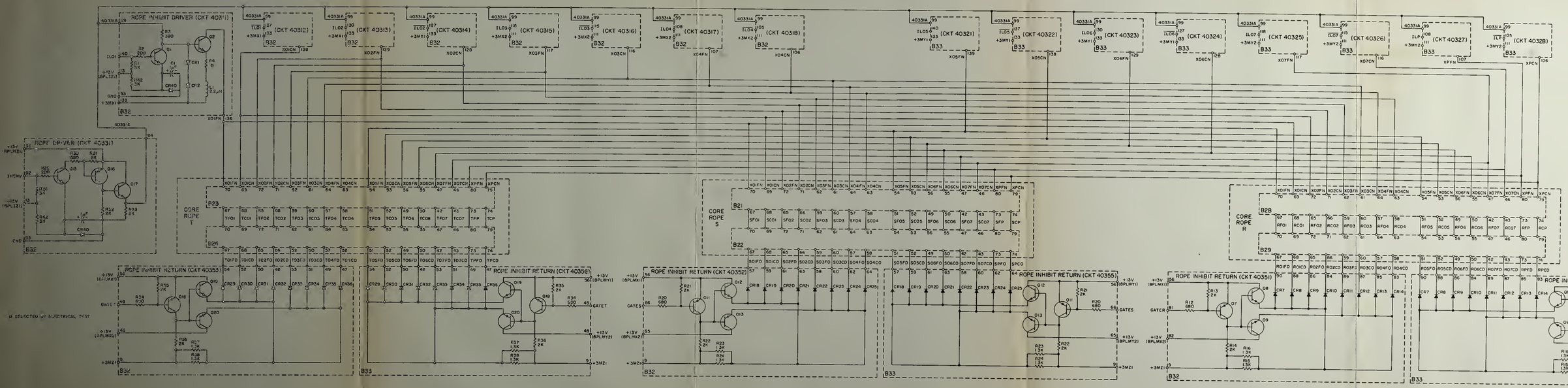


Figure 4-172. Fixed Memory Inhibit Drivers and Return Circuits

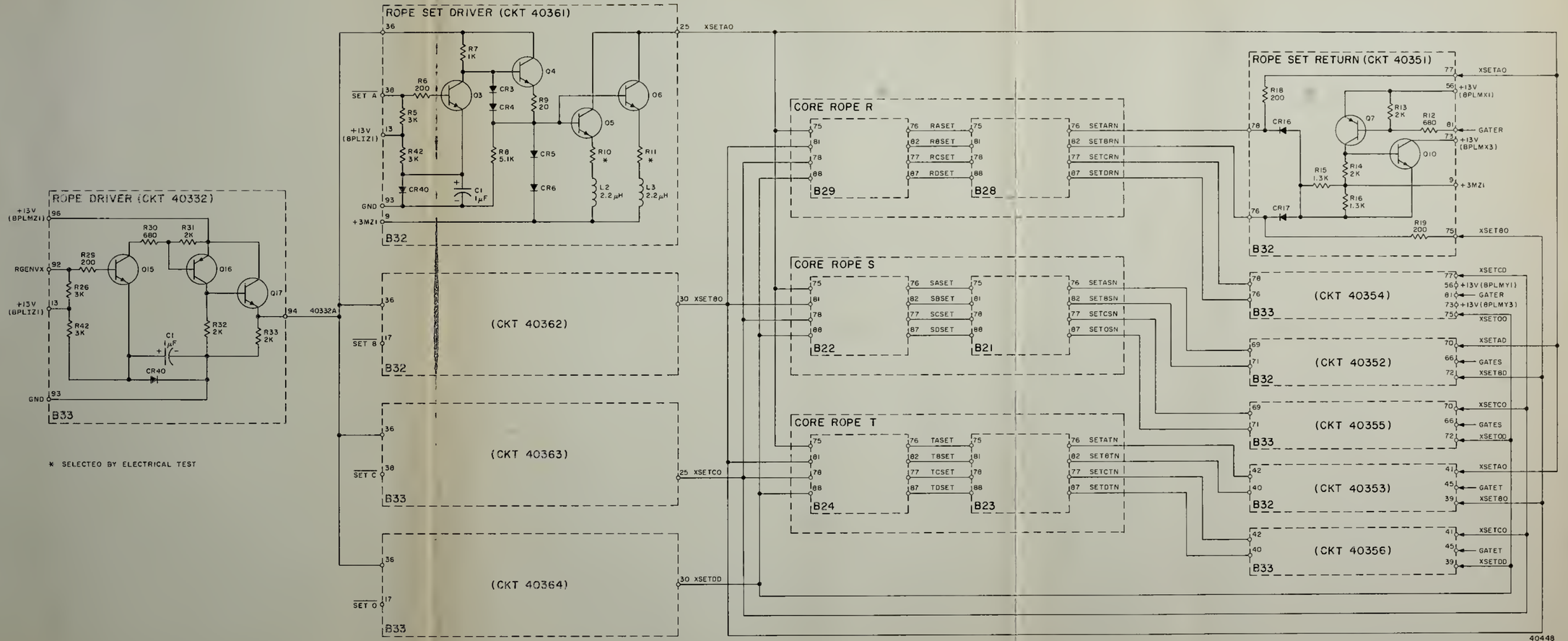


Figure 4-173. Fixed Memory Set Drivers and Return Circuits

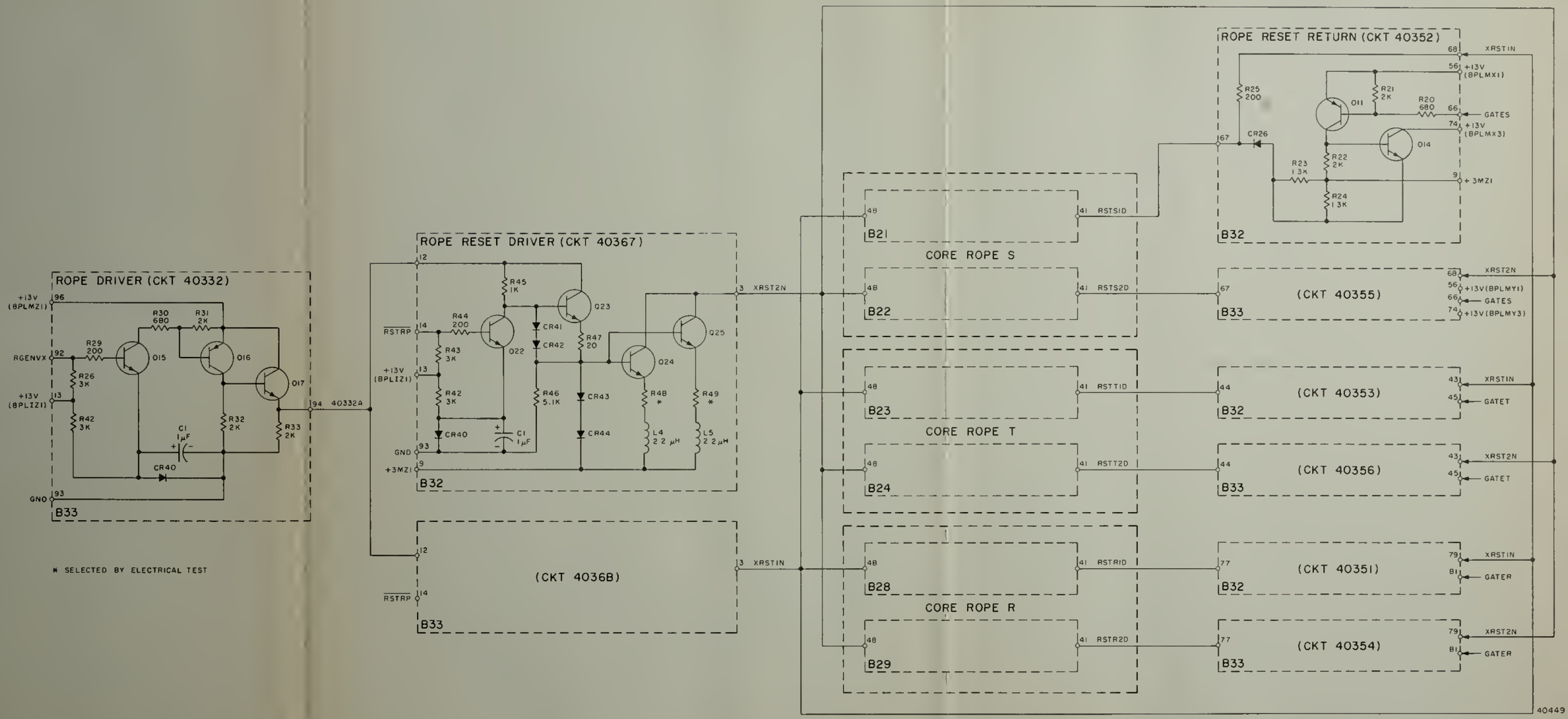


Figure 4-174. Fixed Memory Reset Drivers and Return Circuits

4-8.6.4.6 Sense Amplifiers. Sixteen sense amplifiers are associated with fixed memory. These amplifiers operate similarly to those in erasable memory. The difference occurs in the input circuit (figure 4-175). The inputs to transformer T1 are returned to +3 vdc through resistors R1 and R2 to provide a return path for the sense lines. Output signals (40410A through 40417A and 40420A through 40427A) are fed to register G through the sense amplifiers in erasable memory.

4-8.7 POWER SUPPLY. Power required for operation of the AGC is provided by two switching regulator circuits. The power supply functional block diagram is shown in figure 4-176, and consists of a +3 volt switching regulator, +13 volt switching regulator, filter circuits, and failure detection circuits.

4-8.7.1 +3 Volt and +13 Volt Regulators Functional Description. The power switches and control circuits of the +3 volt and +13 volt regulators are identical. The voltage outputs are determined by minor circuit changes and the input from the control circuits. The primary power input from the spacecraft is applied on two lines (A and B) through the primary power filter to the power switches of the +3 volt regulator. The outputs of both switches are tied together to produce an output designated +3A. The +3A output feeds some of the logic modules on tray A, the filter circuits, and the standby switch. Operation in the standby mode is described below. The dc level of +3 volts from the power switches is determined by the control circuits. A 51.2 kpps sync signal from the timer (PRSYNC) triggers a multivibrator in the control circuit, the output of which is of sufficient duration to produce 3 volts out of the power switch. The 3 volt output is regulated by feed-back of the +3A output into the control circuit.

The +28A and +28B inputs to the power switches of the +3 volt regulator are combined to produce a +28 COM output, which energizes the +13 volt power switch. This circuit and its associated control circuit function in a manner identical to the +3 volt switching regulator. The output from this one power switch is designated B PLUS A. This output is applied to the oscillator, to the control circuit, to logic tray A, and to the standby switch. Inputs CNTRL 1 and CNTRL 2 to the +3 volt and +13 volt switching regulators, respectively, allow simulated failure of the power supply under control of the CTS during subsystem tests.

Rather extensive filtering occurs on the +3 and +13 volt outputs to the memory modules. The filters act essentially as isolation devices and are necessary to prevent the spurious signals that are generated in memory from being reflected into the power supply.

4-8.7.2 Failure Detection Circuits Functional Description. The failure detection circuit monitors the +3A and B PLUS A outputs and generates a power fail indication for an out-of-limits condition or complete failure of either output from the power supply. The low primary power detector generates signal STRT 1 which, when applied to the timer, causes a GOJAM condition if the +28 volt input falls below a predetermined level. The oscillator activity detector generates signal STRT 2 and assures an initial

start sequence (GOJAM) until the oscillator starts running during a power-up condition.

4-8.7.3 +3 Volt Power Supply Detailed Description. The +3 volt power supply consists of control circuit A1 in module B12 and power switch modules B3 and B4. Primary power (28 vdc) from the spacecraft is supplied on two lines (28 AUF, 28BUF) to the primary power filter circuit (figure 4-177). The filter outputs, +28A and +28B, are applied to power switches B4 and B3 respectively (figure 4-178). Two lines are used so that in the event that one line opens, primary power will still be supplied to the AGC. The two +28 volt inputs are combined in the power switch modules to form a +28 COM output which is used to power the control circuits (A1 and A2), the power failure detection circuits, and the oscillator.

Transistors Q2 and Q3 in control circuit A1 form a free running multivibrator, the output of which is applied to the power switches through output stage Q4. The dc level supplied by the power switches is determined by the duty cycle of the signal from the multivibrator. The 51.2 kpps signal (PRSYNC), coupled to the base of Q2 through capacitor C5, fixes the frequency of the output pulses from the multivibrator. This input establishes the pulse width of the output (+3 PLS to the power switches) at 2.5 microsecond.

Transistor Q1 in the control circuit is a differential amplifier which acts as a regulating device on the multivibrator. Zener diode CR2 establishes a constant reference voltage at the base of Q1A. The +3 volt output is fed back to the base of Q1B through the combination of C6 and R7. Any difference between the reference voltage applied to the base of Q1A and the feedback voltage applied to the base of Q1B affects the pulse width output of the multivibrator and opposes any change in the +3 volt output.

The control circuits for both the +3 volt and +13 volt regulators are identical. The level of the regulator output, either +3 or +13 volts, is established by resistor R2 and resistor R8. In the +3 volt regulator, R8 is connected in series with R9. In the +13 volt regulator, R8 is shunted out of the circuit.

The multivibrator output pulses are applied to transistor Q1 in power switch modules B3 and B4. The output of Q1, applied through emitter follower Q2, charges the filter network (C1, C2, C8, and L2) to a +3 volt level. The +28 volt primary input is filtered (C3-C6, L1) and applied to transistors Q1 and Q2. The filter network prevents any ripple generated by the input pulses of the multivibrator from affecting the primary voltage supply.

Temperature sensing device R7 monitors the temperature of power transistors Q1 and Q2, and provides temperature monitor signals (RD172, 173) to the spacecraft.

4-8.7.4 +13 Volt Power Supply Detailed Description. The +13 volt power supply, figure 4-179, consists of control circuit A2 in module B12 and power switch module B2.

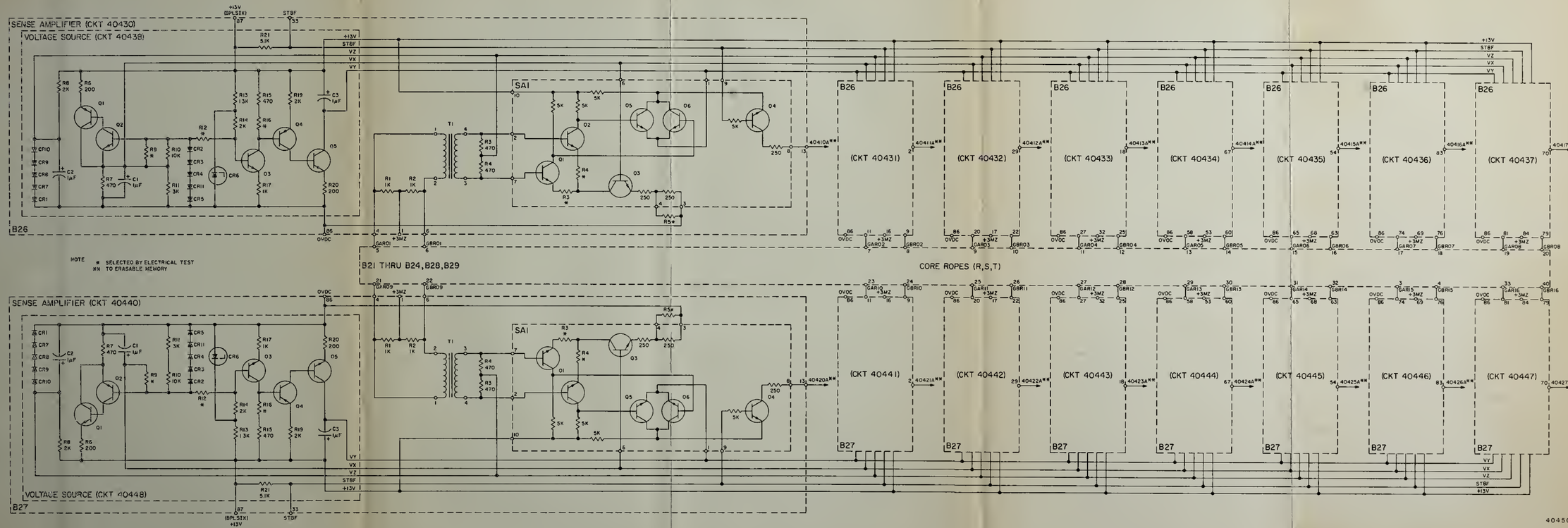


Figure 4-175. Sense Amplifier and Voltage Source

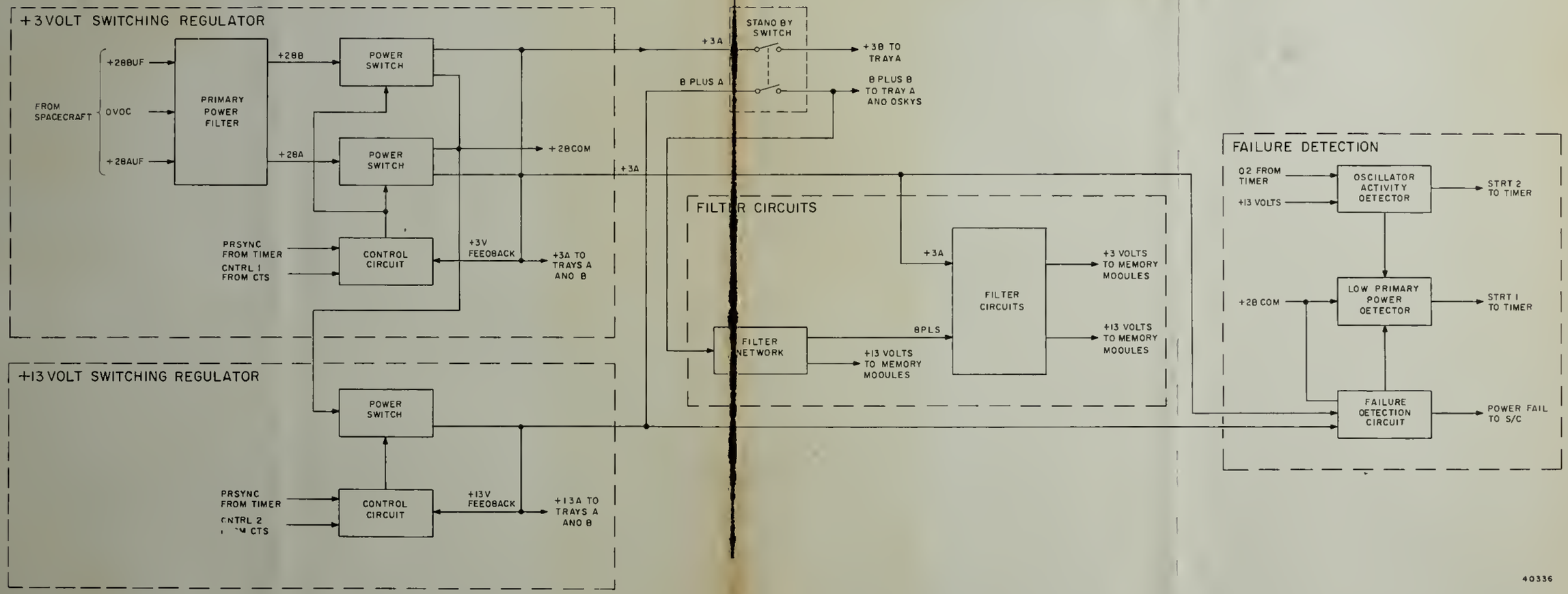


Figure 4-176. Power Supply, Functional Block Diagram

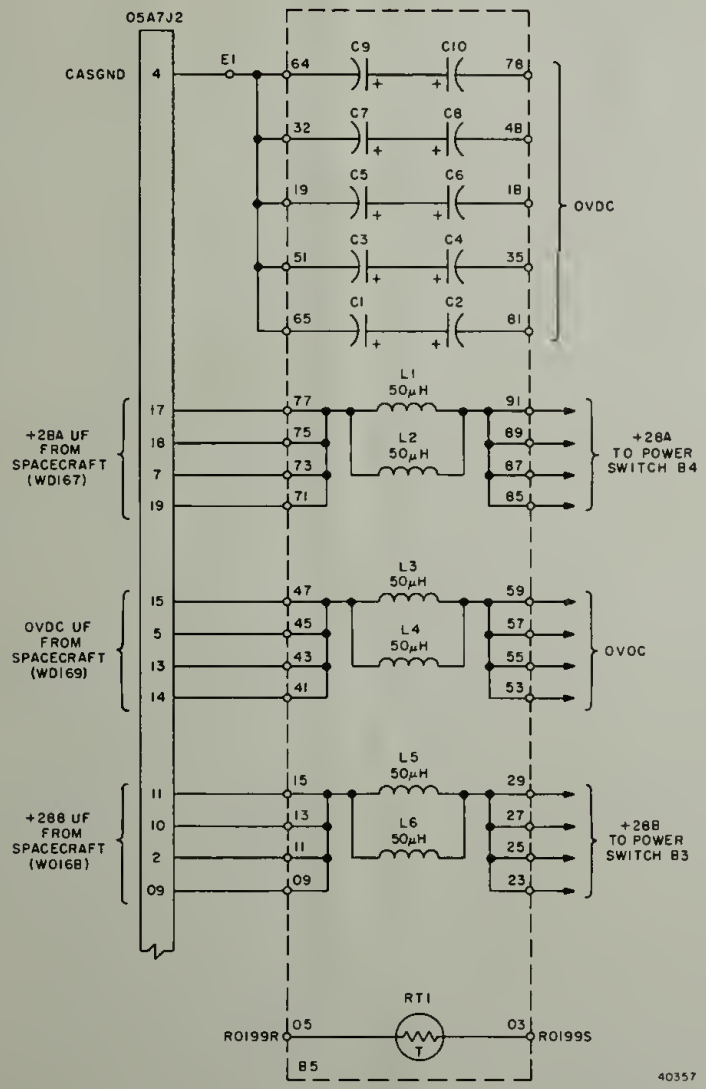


Figure 4-177. Primary Power Filter

The +28 COM line from power switch modules B3 and B4 is applied to the control circuit and the power switch.

Operation of control circuit A2 is identical to circuit A1 in the +3 volt power supply. The level of the multivibrator output, +13 PLS, is established by resistor R2 and by shunting resistor R8 out of the circuit.

Power switch module B2 is identical to modules B3 and B4 of the +3 volt supply and supplies an output of +13 volts (B PLUS A). The temperature of the power transistors is monitored by R7, and sent to the spacecraft as signal RD171.

4-8.7.5 Standby Mode. The standby mode of operation is controlled by the STBY/ON switch mounted at the front of the AGC. When placed in the STBY position, the +3A and B PLUS A voltages applied to the switch contacts are interrupted, thus deenergizing most of the AGC. As shown in figure 4-180, the +3A and B PLUS A voltages become +3B and B PLUS B respectively with the switch in the ON position. The +3B output powers all of the logic modules on tray A with the exception of the timer. This latter functional area is powered by the +3A output. Thus, during standby all the logic modules except the timer (A28, A33, and A34) are disabled. The B PLUS B output powers three of the interface modules on tray A (A19, A20, and A39) and is applied to the filter circuits for use in the memory modules on tray B. Consequently, during standby there is no access to memory. However, the oscillator and power supply as well as interface module A40 are operative.

4-8.7.6 Filter-Circuits. The power supply filter circuits, figure 4-181, consist of several filters for power supplied to tray B, and capacitor filters for power supplied to most of the modules on tray A. Filtering circuits for the +3A output supplied to tray A are contained on the logic modules. The +3A output is applied to the circuitry for scalers A and B and the clock divider logic only. All other modules are powered by the +3B output with the exception of the interface modules (A19, A39; A20, A40).

4-8.7.7 Failure Detection Circuits Detailed Description. The failure detection circuits, figure 4-182, detect failures of the +3 volt and +13 volt power supply outputs. This includes an out-of-limits condition (either high or low) or complete failure of either power supply. In addition, a detector circuit monitors the primary input of +28 vdc in the event that this input is too low. The oscillator activity detector, is included in this funtional area sincc it is a function of the presence of outputs from the power supplies. The operation of this circuit is discussed below.

The power supply fail detection circuits include transistors Q5 through Q12 and associated circuitry. The +28 COM input from the power switch modules is dropped across the series combination of R19 and CR13, CR14 and CR15, and is applied as a reference voltage to differential amplifiers Q5 through Q8. Transistors Q5 and Q6 are the high and low limit detectors respectively for the +13 volt power supply. Transistor Q5 conducts when the +13 volt output decreases to approximately +9 volts; transistor Q6 conducts when the +13 volt output increases. Transistors Q7 and Q8

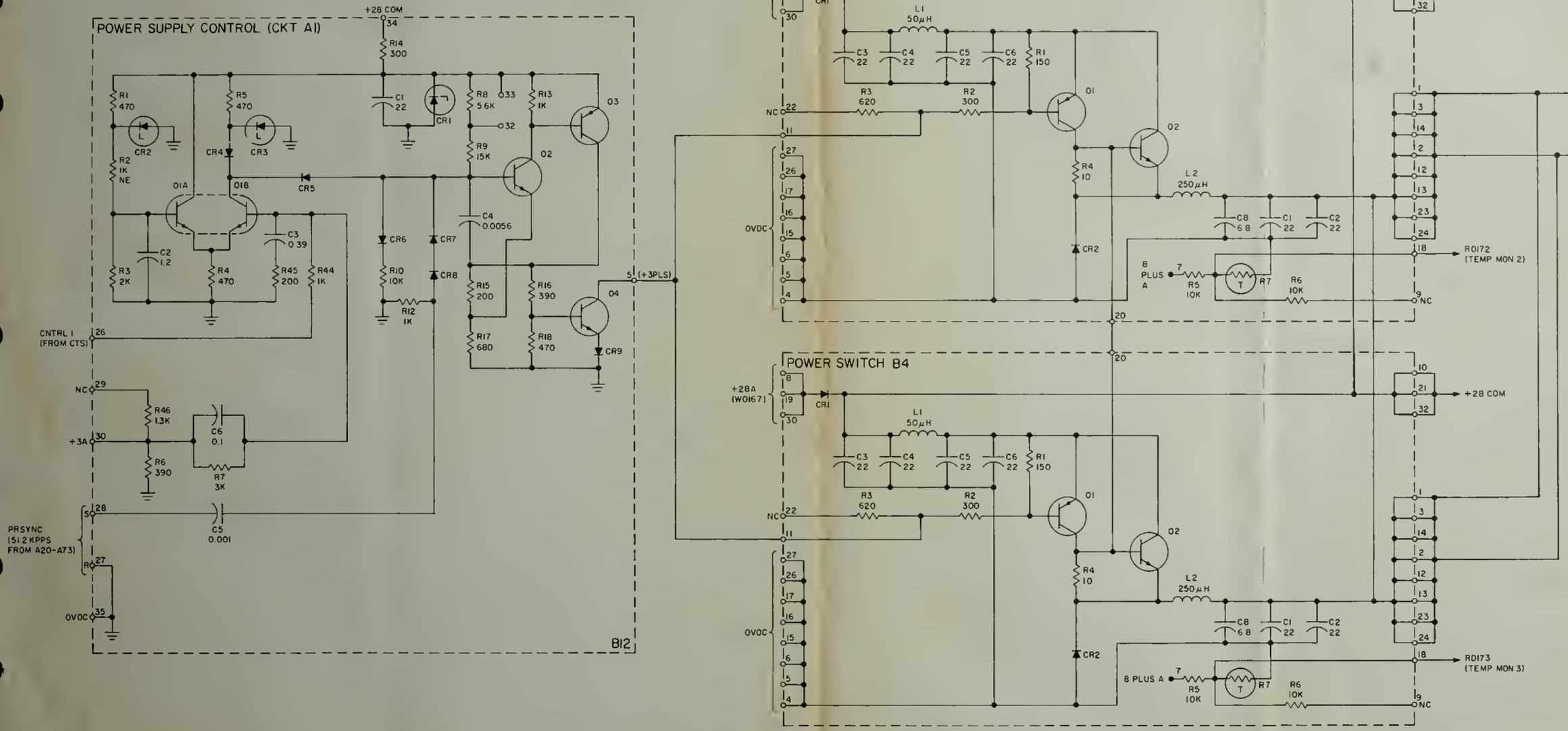


Figure 4-178. +3 Volt Power Supply

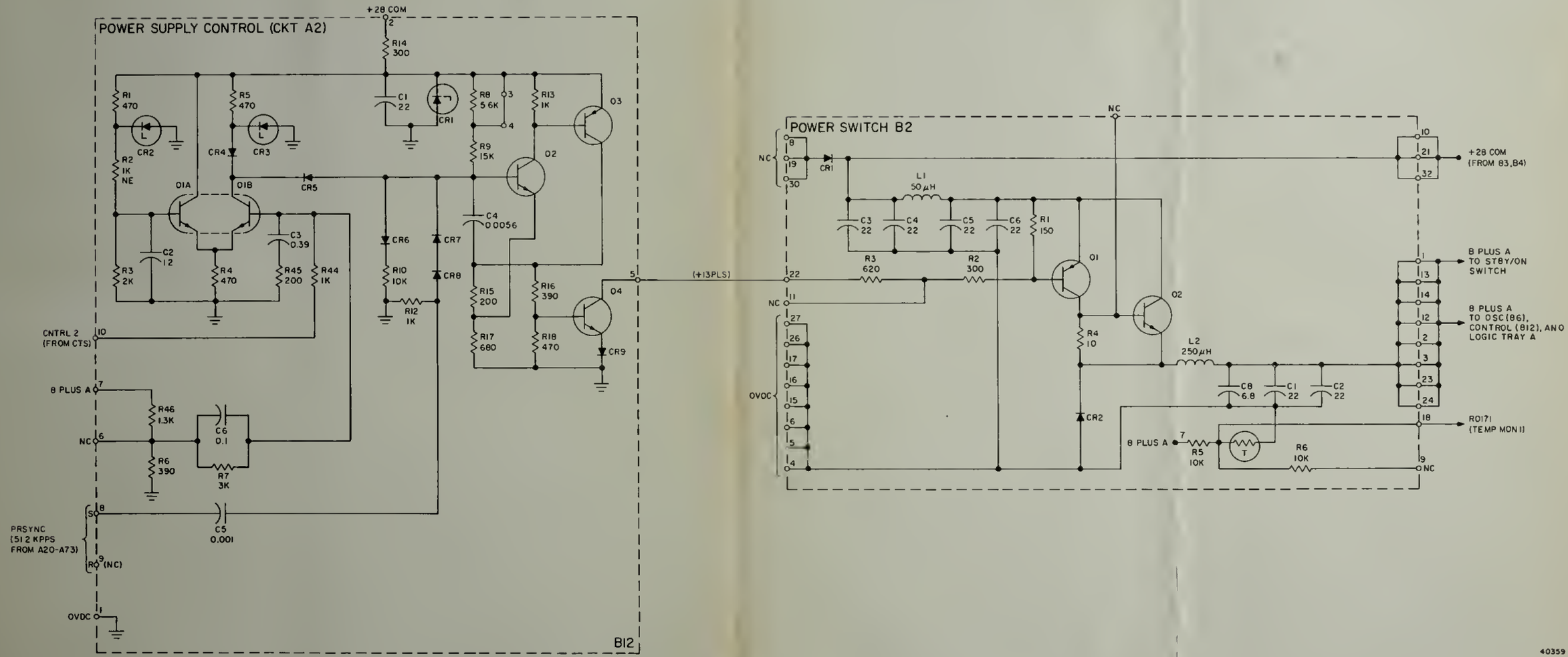


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Figure 4-179. +13 Volt Power Supply

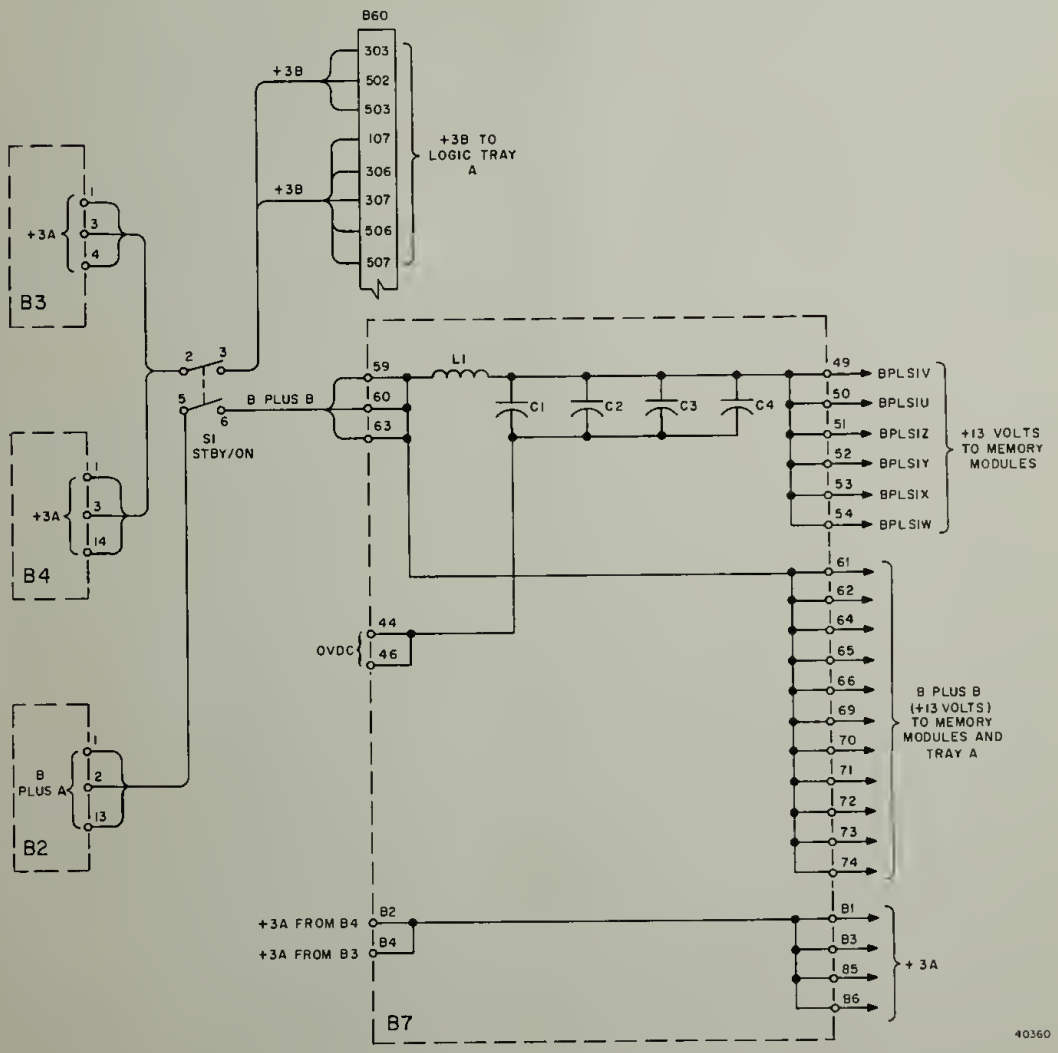


Figure 4-180. Standby Circuit

are the high and low limit detectors respectively for the +3 volt power supply. Transistor Q7 conducts when the +3 volt output increases to approximately +3.5 volts; Q8 conducts when the output decreases to approximately +2.5 volts.

Normally, transistors Q9 and Q10 are on, Q11 is off and Q12 is on. The current flowing through Q12 energizes relay K1. With K1 energized, the return circuit for the power fail indicators is open, and the indicators are not illuminated. When the output from either supply goes out of tolerance, one of the differential amplifiers turns on causing either Q9 or Q10 to cut off. This action causes Q11 to turn on causing Q12 to cut off. Relay K1 deenergizes closing the power fail indication circuit to the DSKY's. In addition, signal STRT1 is generated and is applied to the timer. This causes signal GOJAM to be generated.

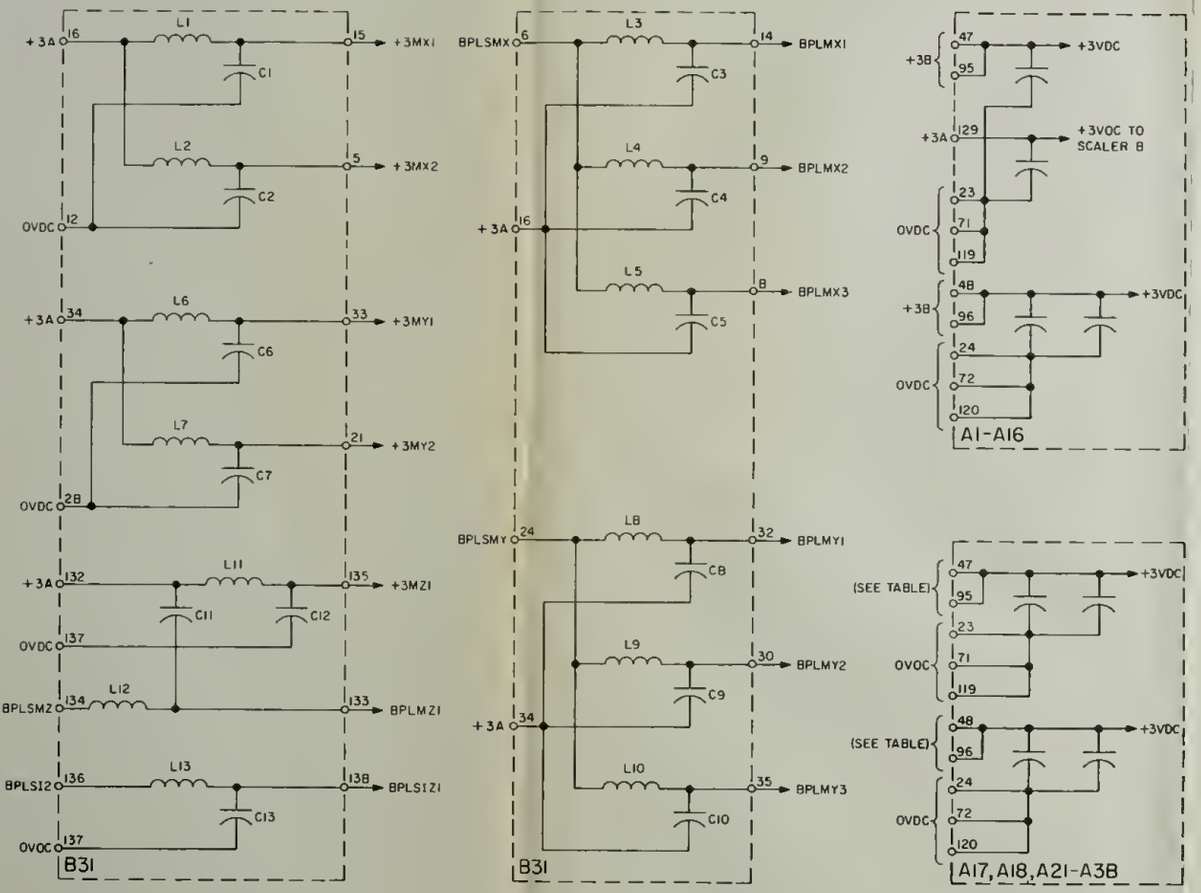
The low primary power detector circuit monitors the +28 volt input. If this input drops too low, signal STRT1 is generated and causes signal GOJAM to fresh-start the AGC.

The oscillator activity detector (transistors Q5-Q7) assures the presence of signal GOJAM during a power-up sequence or if the oscillator fails. After power turn-on, the oscillator output experiences some inherent delay. Consequently, the time counter does not start running until after the supply voltages reach their nominal values. Signal STRT2 is generated and is applied to the timer, and causes signal GOJAM. This condition exists until the clock starts running as indicated by signal Q2A from the clock divider section. Similarly, if the clock fails (assuming +13 volts is still present), Q2A is absent from the input to Q5. Signal STRT2 is generated and causes signal GOJAM.

4-8.8 MACHINE INSTRUCTIONS. Twenty-one different logical operations called machine instructions are performed on data within the AGC. Each instruction is a distinct operation such as add, increment the addressed counter, or multiply as defined by order codes or command signals in the sequence generator. Order codes are supplied from the central processor or generated with the sequence generator. The machine instruction is executed by sets of control pulses from the sequence generator which regulate the flow of data through all functional areas except the DSKY's. A set of control pulses is called an action; actions are generated at the rate of 1.024 megacycles, or every 0.977 microsecond. Twelve actions make one subinstruction and require one memory cycle time (MCT) for execution. An MCT is defined by timing pulses T01 through T12.

Machine instructions require from 1 to 16 MCT's for execution and contain as many subinstructions as there are distinct operations in the instruction. For example, the multiply instruction requires 8 MCT's to be executed but contains only three distinct operations. The first and last operations are executed once; the second operation is executed six times.

There are three functional divisions of machine instructions listed in table 4-XIX: regular, involuntary, and miscellaneous. Table 4-XX lists and defines those control pulses which are directly involved with the execution of a machine instruction. The



PIN / MODULE	47,95	48,96
A17, A18	+3B	+3B
A21-A27	↓	↓
A29-A32	+3B	+3B
A35-A38	+3B	+3B
A28	+3A	+3A
A33, A34	+3A	+3A

NOTE ALL CAPACTORS ARE 6.8 μF
ALL CHOKES ARE 82 μH

40361

Figure 4-181. Power Supply Filter Circuits

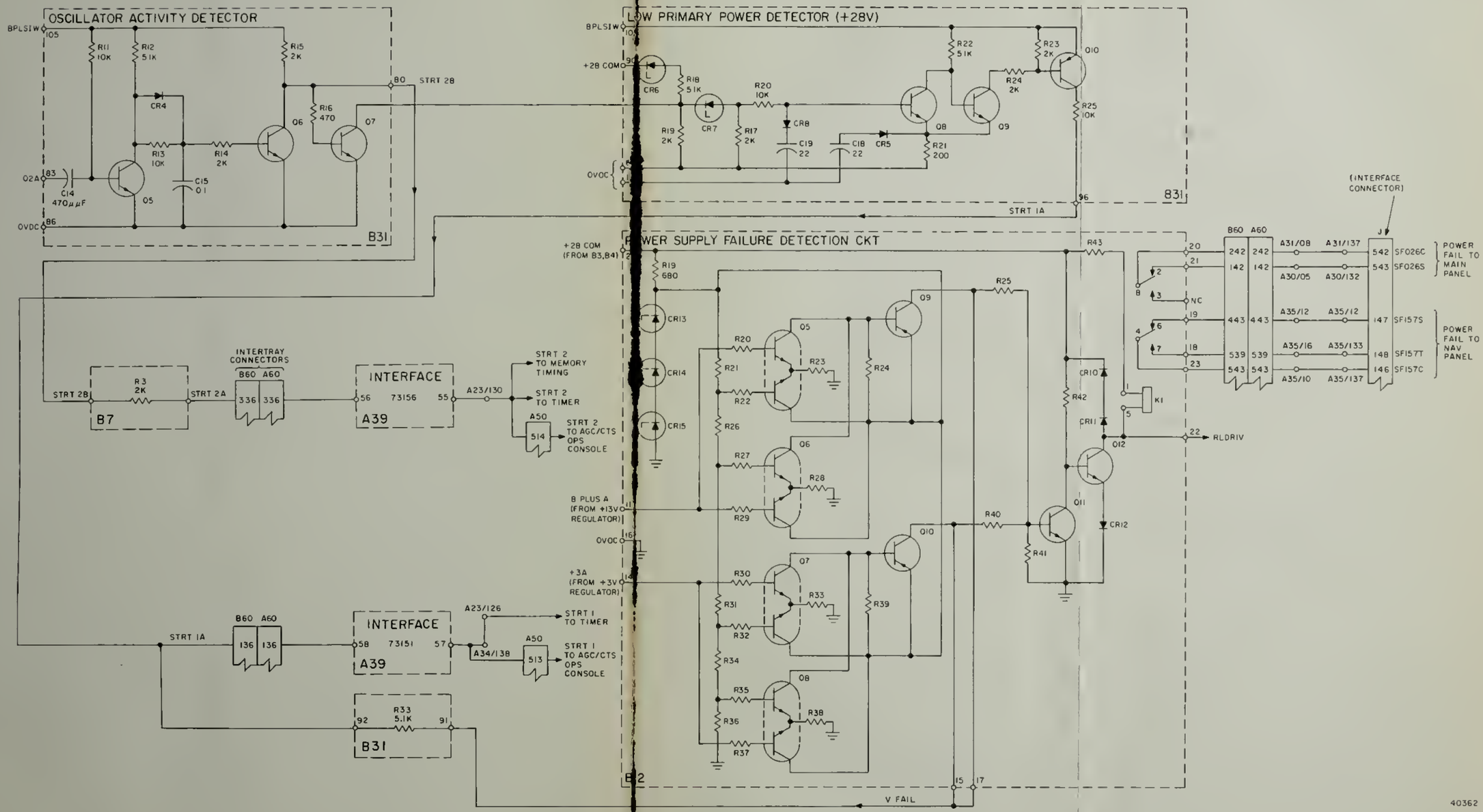


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Figure 4-182. Power Supply Failure Detection Circuits

Table 4-XIX. Machine Instructions

Initials	Purpose	Order Code Entered Into Register SQ	Subinstruction	Execution Time in MCT's
	REGULAR INSTRUCTIONS			
	Basic Instructions			
TC K	Transfer control to K	00	TC0	1
XCH K	Exchange data with location K	03	XCH0, STD2	2
CS K	Clear A and subtract data in K	14	CS0, STD2	2
TS K	Transfer data to K	15	TS0, STD2	2
MSK K	Mask (AND) with data from K	17	MSK0, STD2	2
AD K	Add data from K and count on overflow or underflow	16	AD0, STD2	2
	In case of overflow		Also PINC	3
	In case of underflow		Also MINC	3
NDX K	Index (modify) next instruction	02	NDX0, NDX1	2
CCS K	Count, compare, and skip with data at K	01	CCS0, CCS1	2
	Extra Code Instructions			
SU K	Subtract data from K and count on overflow or underflow	13	SU0, STD2	4
	In case of overflow		Also PINC	5
	In case of underflow		Also MINC	5
MP K	Multiply with data at K	11	MP0, MP1, MP3	10
DV K	Divide by data at K	12	DV0, DV1, STD2	18

(Sheet 1 of 2)

Table 4-XIX. Machine Instructions (cont)

Initials	Purpose	Order Code Entered Into Register SQ	Subinstruction	Execution Time in MCT's
INVOLUNTARY INSTRUCTIONS				
Priority Program Instructions				
RUPT	Interrupt program		RPT1, RPT3, STD2	3
RSM	Resume program		NDX0, RSM	2
Counter Instructions				
PINC	Increment content of addressed counter		PINC	1
MINC	Decrement content of addressed counter		MINC	1
SHINC	Shift content of addressed counter		SHINC	1
SHANC	Shift content of addressed counter and add one		SHANC	1
MISCELLANEOUS INSTRUCTIONS				
Start Instructions				
GO	Computer GO		GO	1
TCSA	Start at specified address		TCSA	1
Display and Load Instructions				
OINC	Display content of address location		OINC	1
LINC	Load addressed location		LINC	1

(Sheet 2 of 2)

Table 4-XX. Control Pulses

Pulse	Purpose
CI	Forced-carry into bit position 1 of adder.
CLG*	Clear (reset) bit positions 16 and 14 through 1 of register G.
CTR	Decrements the multiply counter and sets stage 2 of state counter at action 12 when the content of the multiply counter goes to zero.
GP	Reset bit position 15 of register G and enter the new parity bit generated by the parity pyramid into it. If c(S) = 0014, reset bit position 15 of register OUT 4 and enter the generated parity bit there.
KRPT	Clears the request flip-flop (in interrupt priority control) that initiated program interrupt.
NISQ	Transfer the content of register B, bits 16 through 13, to register SQ at action 12.
RA	Read the content of register A into the write amplifiers.
RB	Read the content of register B into the write amplifiers.
RB1	Read 0 00001 (octal) into the write amplifiers.
RB2	Read 0 00002 (octal) into the write amplifiers.
RC	Read C output of register B into the write amplifiers.
RB14	Read 0 20000 (octal) into the write amplifiers (a logic ONE in bit position 14).
RG, RG*	Read the content of register G into the write amplifiers.
RLP	Read the content of register LP into the write amplifiers.
RP2	Reset bit position 15 of register G and enter c(P2) into it.

*The read (or write) signal generated is 1 microsecond long rather than 0.75 microsecond.

(Sheet 1 of 4)

Table 4-XX. Control Pulses (cont)

Pulse	Purpose
RRPA	Read the address provided by program interrupt priority control into the write amplifiers.
RS	Read the content of register S into the write amplifiers.
RSB	Read 1 00000 into the write amplifiers (minus zero is a logic ONE in write amplifier 16 only).
RSC	Read the content of the addressed flip-flop register onto the write amplifiers.
RSCT	Read the address provided by counter priority control into the write amplifiers.
RSTRT	Read STRT address into the write amplifiers.
RU, RU*	Read the content of adder output gates into the write amplifiers (1-15).
RUAC	Read bit position 16 of adder.
RZ	Read the content of register Z into the write amplifiers.
R1C	Read 1 77776 (octal) into the write amplifiers.
R22	Read 0 00022 (octal) into the write amplifiers.
R24	Read 0 00024 (octal) into the write amplifiers.
ST1	Set stage 1 of the state counter at action 12.
ST2	Set stage 2 of the state counter at action 12.
TMZ	Test for minus zero. Transfer the contents of the write amplifiers to the sequence generator and set BR2 if all bits are logic ONE's. Reset BR2 if all bits are logic ZERO's.

*The read (or write) signal generated is 1 microsecond long rather than 0.75 microsecond.

(Sheet 2 of 4)

Table 4-XX. Control Pulses (cont)

Pulse	Purpose
TOV	Test for overflow or underflow. Transfer the contents of write amplifiers 16 and 15 to the sequence generator and set BR2 in case of overflow or set BR1 in case of underflow. Reset BR1 and BR2 for other conditions.
TP	Test for correct parity.
TRSM	Test for resume. Transfer c(S) to the sequence generator and set stage 2 of state counter at action 12 if c(S) = 0025.
TSGN	Test sign. Transfer the content of write amplifier 16 to the sequence generator and set BR1 if bit 16 is a logic ONE. Reset BR1 if bit 16 is a logic ZERO.
TSGN2	Test sign. Transfer the content of write amplifier 16 to the sequence generator and set BR2 if bit 16 is a logic ONE. Reset BR2 if bit 16 is a logic ZERO.
TSGN3	Test sign. Transfer the content of write amplifier 16 to the sequence generator and send signal to program interrupt priority control if bit 16 is a logic ONE.
WA	Clear register A and write the contents of the write amplifiers into register A.
WALP	Clear register A and bit position 14 of register LP.
WB	Clear register B and write the contents of the write amplifiers into register B.
WG	Clear bit positions 15 through 1 of register G and write the contents of the write amplifiers into register G.
WG*	Write contents of write amplifiers directly into bit positions 16 and 14 through 1 of register G and the parity bit into bit position 15.
WLP	Clear register LP and write the contents of the write amplifiers into register LP.

*The read (or write) signal generated is 1 microsecond long rather than 0.75 microsecond.

(Sheet 3 of 4)

Table 4-XX. Control Pulses (cont)

Pulse	Purpose
WP, WP*	Enter the content in the write amplifiers into the parity logic.
WP2	Clear P2 in parity logic and enter the generated parity bit. If c(S) = 0014, reset bit position 15 of register OUT 4 and enter c(P2).
WS	Clear register S and write the contents of write amplifiers 12 through 1 into register S.
WSC	Clear the addressed flip-flop register and write the contents of the write amplifiers into it.
WX, WX*	Write the contents of the write amplifiers into register X.
WY, WY*	Clear registers X and Y and write the contents of the write amplifiers into register Y.
WZ	Clear register Z and write the contents of the write amplifiers into register Z.
WOVI	Inhibit program interruption at end of current instruction in case of overflow or underflow.
WOVC	Increment or decrement OVCTR by executing PINC or MINC.
WOVR	Deliver counter overflow or underflow to the appropriate priority input selected by the content of register S.

*The read (or write) signal generated is 1 microsecond long rather than 0.75 microsecond.

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following paragraphs define each instruction in detail with the aid of instruction flow charts such as that shown in figure 4-183.

The fixed (F) and erasable (E) memories are shown combined on the charts. The central processor flip-flop registers are shown individually. Buffer-register B is shown with its direct (B) and its complement (C) side. The row marked "+1" symbolizes that circuitry of the adder which, on command, adds the quantity plus one to an operand entered into input register X or Y. The basic principle of operation of the adder is described as part of the central processor. The write amplifiers (WA's) are symbolized by triangles placed into the flow lines. Registers are always signified by

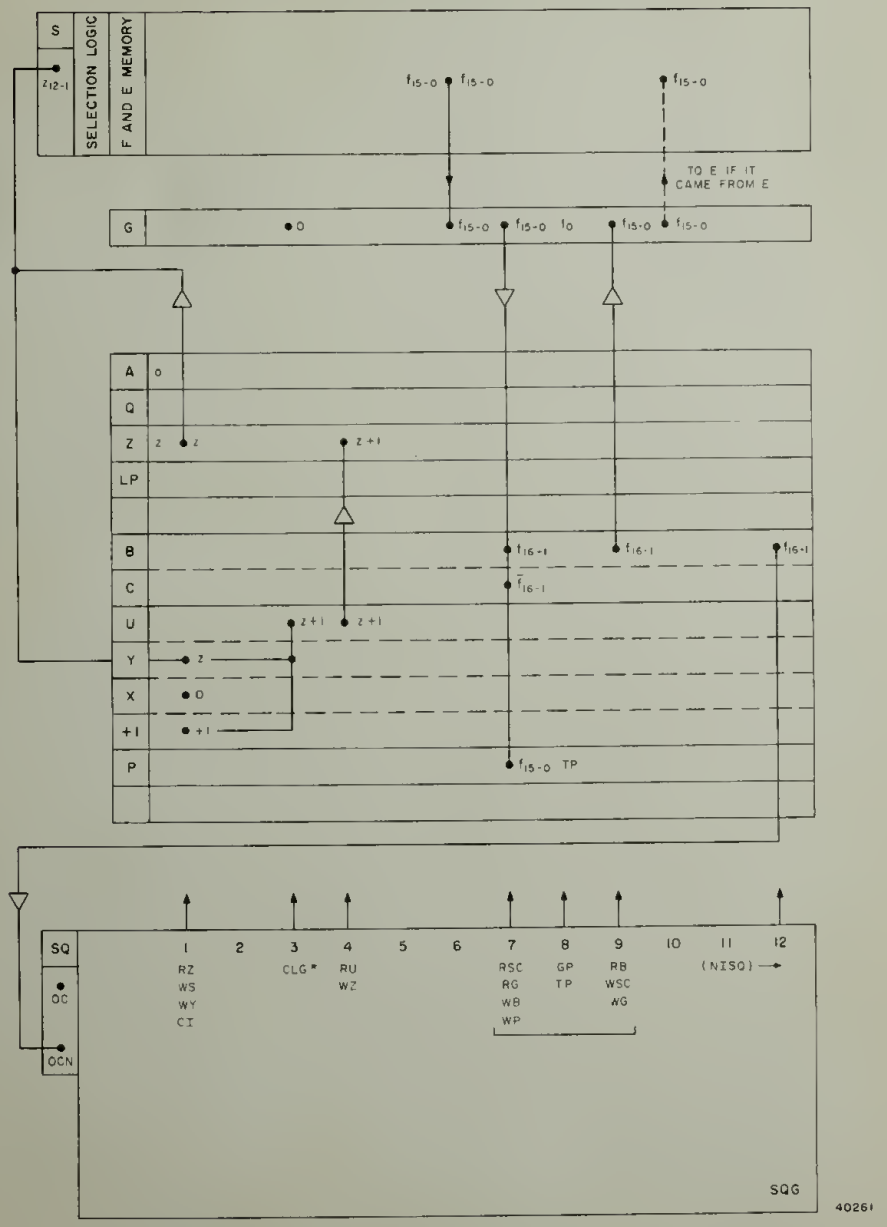

Figure 4-183. Subinstruction STD2 (Example for z $\geq$ 0020)

capital letters, their contents by small letters. Further, $\bar{a}$ means the complement of a. Control pulse symbols in parentheses indicate signals internal to the sequence generator (SQG). In the text, c(A) means the content of A, b(A) means the previous (before) content of (A). $\bar{c}$(A) indicates the complemented c(A), and c^e(A) indicates the edited c(A). In the box representing the sequence generator, action times are listed form 1 to 12. Each action time lists the control pulses generated by the sequence generator. Directly above each action time listing, the flow of information between the registers is shown. The AGC is performing no action when no control pulses are shown at an action time. Table 4-XXI lists all the machine instructions and the control pulses generated at each action.

4-8.8.1 Regular Instructions. Regular instructions identify distinct operations during program execution and consist of basic instructions and extra code instructions. Each basic instruction word in memory contains a three bit order code which identifies a basic instruction. This three bit order code is converted to a four bit order code within the central processor and then is supplied to the SQG. The three bit order code identifies eight basic instructions. Three additional regular machine instructions, the extra code instructions, are identified by order codes obtained within the central processor by indexing. Indexing adds selected quantities to quantities specified by the three bit order code. Therefore, the four bit order code sent to the sequence generator is not limited to identifying eight instructions. Eleven regular machine instructions, consisting of eight basic instructions and three extra code instructions, are identified.

A program consists of a series of basic instructions; extra code instructions are derived by modifying basic instructions. The relevant address of each basic instruction is normally used to specify the location of the data to be worked with. The instructions are stored at locations in numerical order to specify their sequence of execution. Therefore, the address of the instruction to be executed next (the next address) is defined by incrementing by one the address of the instruction presently being executed and storing it in register Z, the program counter. This is accomplished during the execution of the basic instruction. If the normal sequence of execution is interrupted, the next address is stored in register Q for later use. Another duty of a basic instruction is to enter the entire code of the instruction to be executed next (the subsequent instruction) into register B. Finally, each regular instruction must enter the order code of the subsequent instruction into register SQ in order to initiate its execution.

4-8.8.1.1 Basic Instructions. There are eight basic instructions (table 4-XIX), each of which consists of one or more subinstructions that are represented by order codes. The eight basic instructions are:

(1) Transfer control

(2) Count, compare, and skip

(3) Index

(4) Exchange

Table 4-XXI. Control Pulse Timing for all Machine Instructions

Subinstruction	Action 1	Action 2	Action 3	Action 4	Action 5	Action 6	Action 7	Action 8	Action 9	Action 10	Action 11	Action 12
INSTRUCTION TS K (ORDER CODE 15)												
TS	RB WS	RA WB WP TOV	CLG	NO ACTION RZ WY CI	NO ACTION RBI, RIC WA or WA	NO ACTION	NO ACTION RU WZ	GP	RB WSC WG	RA WOVI	STZ	
STD2	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	
INSTRUCTION AD K (ORDER CODE 16)												
AD	RB WS	RA WY	CLG	NO ACTION	NO ACTION	NO ACTION	RSC RG WB WP	GP TP RB WX	RB WSC WG	NO ACTION	RU WA WOVI WOVC STZ	
STD2	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	
PINC (in case of overflow)	RSCT WS	NO ACTION	CLG	RBI WY	NO ACTION	RG WX WP	TP	WP	RU CLG WP	RU WG WOVR	NO ACTION	
MINC (in case of underflow)	RSCT WS	NO ACTION	CLG	RIC WY	NO ACTION	RG WX WP	TP	WP	RU CLG WP	RU WG WOVR	NO ACTION	
INSTRUCTION MSK K (ORDER CODE 17)												
MSK	RB WS	RA WB	CLG	RC WY	NO ACTION	NO ACTION	RSC RG WB WP	RU RC WA GP TP	NO ACTION	RA WB	RC WA WOVI STZ	
STD2	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	
INSTRUCTION RUPT												
RUPT1	RZ4 WY WS CI	NO ACTION	CLG	NO ACTION	NO ACTION	NO ACTION	NO ACTION	NO ACTION	RZ WG	RU WZ	ST1 ST2	
RUPT3	RZ WS	RRPA WZ	RZ KRPT	NO ACTION	NO ACTION	NO ACTION	NO ACTION	NO ACTION	RB WSC WG	NO ACTION	ST2	
STD2	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	

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Table 4-XXI. Control Pulse Timing for all Machine Instructions (cont)

Subinstruction	Action 1	Action 2	Action 3	Action 4	Action 5	Action 6	Action 7	Action 8	Action 9	Action 10	Action 11	Action 12
INSTRUCTION PINC												
PINC	RSCT WS	NO ACTION	CLG	RBI WY	NO ACTION	RG WX WP	TP	WP	RU CLG WP	RU* WG WOVR	NO ACTION	
INSTRUCTION MINC												
MINC	RSCT WS	NO ACTION	CLG	RIC WY	NO ACTION	RG WX WP	TP	WP	RU CLG WP	RU* WG WOVR	NO ACTION	
INSTRUCTION SHINC												
SHINC	RSCT WS	NO ACTION	CLG	WY	NO ACTION	RG WY WX WP TSGN1	TP	WP	RU CLG WP	RU WG WOVR	NO ACTION	
INSTRUCTION SHANC												
SHANC	RSCT WS	NO ACTION	CLG	WY	NO ACTION	RG WY WX WP TSGN1	TP CI	WP	RU CLG WP*	RU* WG? WOVR	NO ACTION	
INSTRUCTION OINC												
OINC	WS	NO ACTION	CLG	NO ACTION	NO ACTION	NO ACTION	RSC RG	NO ACTION	NO ACTION	NO ACTION	NO ACTION	
INSTRUCTION LINC												
LINC	WS	NO ACTION	CLG	NO ACTION	NO ACTION	NO ACTION	WSC WG WP	GP	NO ACTION	NO ACTION	NO ACTION	
INSTRUCTION GO												
GO	RSTRT WS WY CI	NO ACTION	CLG	RA WOVI	NO ACTION	NO ACTION	RG RSC WB WP	GP TP RZ WQ	RB WSC WG	RU WZ	NISQ →	
INSTRUCTION TCSA												
TCSA	WS WY CI	NO ACTION	CLG	RA WOVI	NO ACTION	NO ACTION	RG RSC WB WP	GP TP RZ WQ	RB WSC WG	RU WZ	NISQ →	

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Table 4-XXI. Control Pulse Timing for all Machine Instructions (cont)

Subinstruction	Action 1	Action 2	Action 3	Action 4	Action 5	Action 6	Action 7	Action 8	Action 9	Action 10	Action 11	Action 12
INSTRUCTION TC K (ORDER CODE 0)												
TC	RB WS WY CI	NO ACTION	CLG	RA WOV1	NO ACTION	NO ACTION	RG RSC WB WP	GP TP RZ WC	RB WSC WG	RU WZ	NISQ →	
INSTRUCTION CCS K (ORDER CODE 1)												
CCS0	RB WS	RZ WY	CLG	NO ACTION	NO ACTION	RSC RG WB WP TSGN	RC TMZ RB TMZ	GP TP R2 WX GP TP	R1 WX GP TP R1 R2 WX GP TP	RB WSC WG	RC WA RB WA RIC WA RIC WA	RU ST1 WZ	
CCS1	RZ WS WY CI	NO ACTION	CLG	RU WZ	RA WY CI	NO ACTION	RSC RG WB WP	RU WB GP TP	NO ACTION	RC WA WOV1	RG RSC WB NISQ →	
INSTRUCTION NDX K (ORDER CODE 2)												
NDX0	RB WS	NO ACTION	CLG	RA WOV1	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	TRSM	ST1	
NDX1	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	RB WY	RSC RG WB WP	GP TP RB WX	RB WSC WG	NO ACTION	RU WB WOV1 NISQ →	
RSM	R24 WS	NO ACTION	CLG	NO ACTION	NO ACTION	NO ACTION	RG WZ	NO ACTION	NO ACTION	NO ACTION	NISQ →	
INSTRUCTION XCH K (ORDER CODE 3)												
XCH	RB WS	RA WP	CLG	WP2	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RA WSC WG RP2	RB WA WOV1	ST2	
STD2	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO	
INSTRUCTION MP K (ORDER CODE 11)												
MP0	RB WS	RA WB CLG TSGN	RSC WG	RB WLP RC WLP	RLP WA	NO ACTION	RG WY WP RG WB WP	GP TP RC WY GP TP	RU WB TSGN2	RA WLP TSGN RA RB 14 WLP TSGN	WALP (ST1) RU WALP (ST1) R1 RIC WALP (ST1) RU WALP (ST1)	

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Table 4-XXI. Control Pulse Timing for all Machine Instructions (cont)

Subin-struction	Action 1	Action 2	Action 3	Action 4	Action 5	Action 6	Action 7	Action 8	Action 9	Action 10	Action 11	Action 12
INSTRUCTION MP K (ORDER CODE 11) cont												
MP1	RA WY	RLP WA TSGN	NO ACTION RB WX	RA WLP	RLP TSGN	RU WALP	RA WY	NO ACTION RB WX	RLP WA	RA WLP CTR	RU WALP STI	
MP1	RZ WS WY CI	RLP TSGN	CLG*	RU WZ	RA WY	NO ACTION RB WX	RG RSC WB WP	RLP WA GP TP	RB WSC WG	RA WLP	RU WALP NISO →	
INSTRUCTION DV K (ORDER CODE 12)												
DV0	RB WS	RA WB CLG* TSGN	RSC WG	RC WA NO ACTION	R1 WLP R2 WLP	RA WQ	RG WB WP (TSGN)	RB WA GP TP	RLP R2 WB | NO ACTION	RB WLP | RC WA	R1 WB ST1	
DV1	RZZ WS CLG-	RQ WG	RG RSB WO WY	RA WX	RLP (TSGN2)	NO ACTION	RU (TSGN)	NO ACTION RU WQ	RB RSB WG RB WG	RG WB (TSGN)	ST1 | RB WA (ST2) RC WA (ST2)	
STD2	RZ WS WY CI	NO ACTION	CLG	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	
INSTRUCTION SU K (ORDER CODE 13)												
SU	RB WS	RA WY	CLG*	NO ACTION	NO ACTION	NO ACTION	RSC RG WB WP	GP TP RC WX	RB WSC WG	NO ACTION	RU WA WOVI WOVG ST2	
STD2	RZ WS WY CI	NO ACTION	CLG*	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	
PINC (in case of overflow)	RSGT WS	NO ACTION	CLG*	R1 WY	NO AGTION	RG* WX* WP	TP	WP	RU* CLG* WP	RU* WG* WOVR	NO AGTIO.4	
MINC (in case of underflow)	RSGT WS	NO ACTION	CLG*	R1G WY	NO ACTION	RG* WX* WP	TP	WP	RU* CLG* WP*	RU* WG* WOVR	NO ACTION	
INSTRUCTION CS K (ORDER CODE 14)												
CS	RB WS	NO ACTION	CLG*	NO ACTION	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	RC WA WOVI	ST2	
STD2	RZ WS WY CI	NO ACTION	CLG*	RU WZ	NO ACTION	NO ACTION	RSC RG WB WP	GP TP	RB WSC WG	NO ACTION	NISO →	

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(5) Clear and subtract

(6) Transfer to storage

(7) Add

(8) Mask

The transfer control instruction changes AGC control to an instruction word in a given location. The address of the instruction word that was to be executed next is stored, and a transfer control instruction can later be used to return AGC control to this stored instruction word.

The count, compare, and skip instruction selects one of four new instruction words, depending on the magnitude and sign of a quantity at a given location. This branching control allows program options depending on the results of selected computations.

The index instruction modifies basic instruction words to obtain order codes of extra code instructions and to obtain other basic instruction words. If a basic-instruction-word result is desired, either the order code or the order code and relevant address can be changed. The relevant address can not be changed when an order code of an extra code instruction is obtained.

The exchange instruction exchanges the contents of the central processor accumulator with the contents at a given location. If a location in fixed memory is given, its contents are copied into the accumulator after the former accumulator contents are cleared.

The clear and subtract instruction enters the complement of the contents at a given location into the accumulator. If the given location is the accumulator, the accumulator contents are complemented.

The transfer to storage instruction copies the accumulator quantity into a memory location or into another flip-flop register. If one memory location is not sufficient to store the quantity, other instructions which copy part of the quantity into a second location may be initiated.

The add instruction copies the contents of a given location into the accumulator if the accumulator was initially cleared. If the accumulator contained a number, the add instruction adds the contents of the given location to the number in the accumulator. If the given location is the accumulator, the accumulator contents are doubled.

The mask instruction detects individual-bit conditions of the binary word contained in the accumulator. The results are used to determine program execution options.

When an order code is entered into the sequence generator, control pulses are generated for the execution of the subinstruction defined by the order code. Most basic instructions consist of two subinstructions. Normally the first subinstruction

carries out the specific task of the instruction, such as adding data, transferring information et cetera. The second subinstruction performs the common duties required of the instruction. Usually the second subinstruction is STD2 (standard subinstruction two). Subinstruction STD2 and the transfer control instruction are described in detail to illustrate the use of the instruction flow charts.

Standard subinstruction STD2 execution is illustrated on figure 4-183 for c(Z) $\geq$ 0020. Octal addresses below 0020 indicate the address of an addressable flip-flop register. Four control pulses (RZ, WS, WY, and CI) are generated at action 1. Pulse RZ reads the contents of register Z (the next address) into the write amplifiers. Note that if L is the location of the instruction being executed, then z = c(Z) = L +1. Pulse WS resets (clears) register S, then writes the next address into it. Pulse WY clears input registers X and Y of the adder and writes c(Z) into Y. Control pulse CI forces a carry into the adder; that is, a one is added to z. The sum z + 1, the address after the next or the second-next address, appears in the output gates (U) of the adder within 3 microseconds. Now, z + 1 = L + 2. Control pulse CLG*, at action 3, clears register G as symbolized by the 0 on the diagram. At action 4, pulse RU reads quantity z + 1 to the write amplifiers, and pulse WZ clears Z and writes z + 1 into it.

The content of register S (bits 12 through 1 of z, entered at action 1) causes the selection logic to gate the proper location for readout and write-in. The corresponding location in the F or E memory will deposit its content (f or e) into register G during action 6. If the address refers to a location in the E memory, the z drivers of the E memory are energized during actions 10 through 12 and any content of register G is written into the addressed location in the E memory. If the address stored in register S is equal to or smaller than 0017, a flip-flop register is addressed for readout or write-in, as shown in figure 4-184 for the case of z = 0001.

Actions 7, 8, and 9, as shown in figures 4-183 and 4-184 are common to most subinstructions. This group of control pulses is referred to as the standard memory inquiry cycle (STM1C) and is symbolized by the bracket underneath. Control pulses RG, WB, and WP transfer data to be worked with, or the subsequent instruction f, from G to B and P. The complement of f appears at the C side of buffer-register B. Control pulse RSC has no effect unless a flip-flop register is addressed. Pulse GP gates the new parity bit (generated by the parity pyramid) for the word stored at register P into bit position 0 of G, as symbolized by f_0 in G. Pulse TP (test parity) causes an alarm to be generated in case the parity of the word in register P is incorrect. The parity test is symbolized by TP in register P. (The operation of the parity circuits is described as part of the central processor.) For the purposes of the description, it is always assumed that the parity is correct and no consequences of incorrect parity are discussed. Control pulses RB and WG transfer the content of B through the write amplifiers into bit positions 1 through 15 of G. Pulse WSC has no effect since a flip-flop register has not been addressed.

Control pulse NISQ, generated at action 11, causes the SQG to transfer (at action 12, as indicated by an arrow) the order code OCN of the instruction to be executed

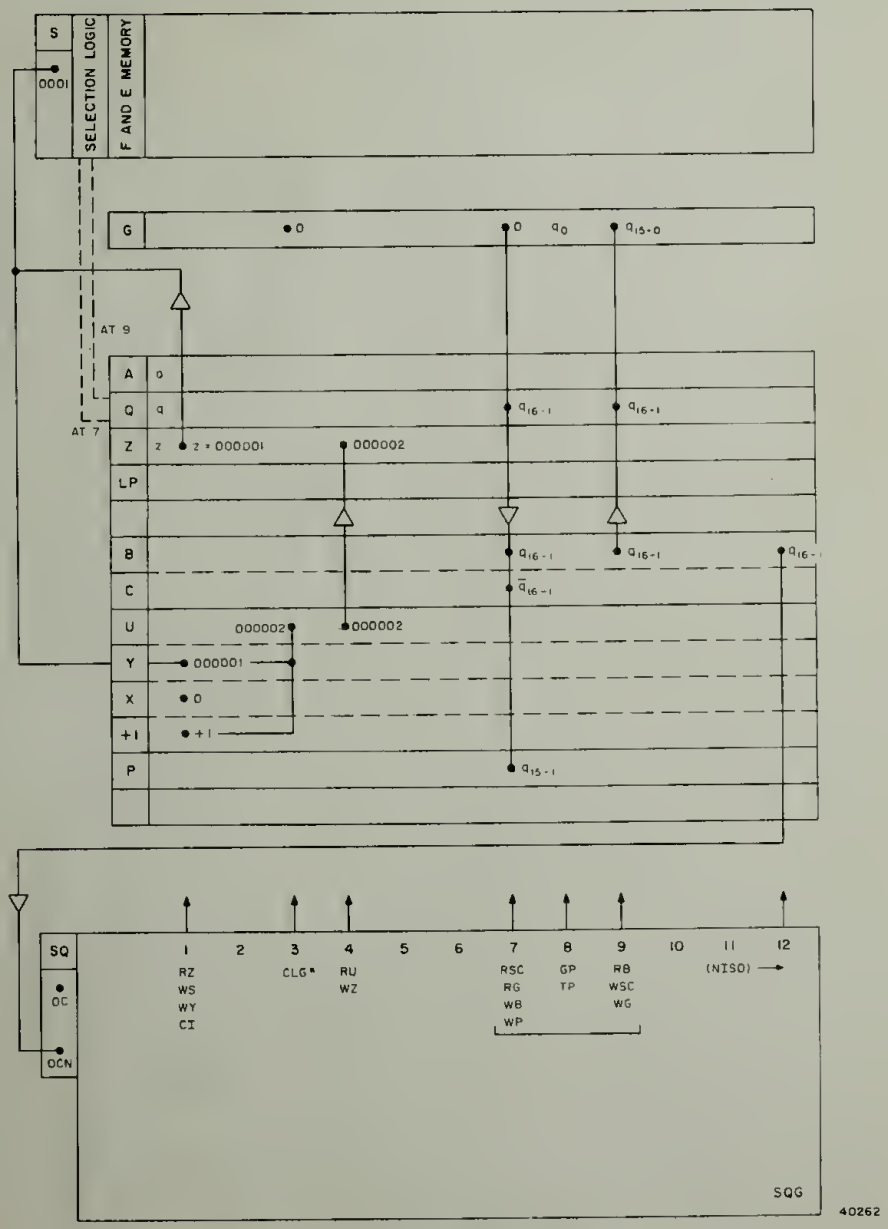

Figure 4-184. Subinstruction STD2 (Example for z = 0001)

next from bit positions 16 through 13 of B to register SQ. If the transfer of data or of the subsequent instruction is not established by means of STD2 (i.e., if STD2 is not the second subinstruction), control pulse NISQ must be contained in another concluding subinstruction.

Figure 4-183 is very similar to figure 4-184 except that the addressed register is Q, a flip-flop register, instead of a location in the F or E memory. Control pulse RG at action 7 has no real effect since register G is cleared at action 3 and not loaded from the F or E memory thereafter. Since the address stored in S (0001) is lower than 0020, the selection logic signals the SQG to gate the proper flip-flop register for readout and write-in during actions 7 and 9. This is indicated by dotted lines leading from the selection logic to register Q. Pulse RSC goes to all addressable flip-flop registers, but is only able to read out the one which is addressed simultaneously. Control pulse WSC also goes to all addressable flip-flop registers, but only that register which is addressed at the same time is enabled to accept data. Since $c(S) \leq 0027$, control pulse TP is prevented from causing an alarm.

Instruction TC K (Transfer Control to K, Order Code 00) means: Transfer program control to the instruction stored at location K. When K is greater than address 0024 but less than address 1777, the location of K is in erasable memory. To perform the TC K operation, register Z is set to equal the before contents of register B plus one. The basic instruction that was to be executed next [b(Z)] is skipped by instruction TC K and stored in register Q. It can be returned to by instruction TC Q. If K is in E memory, the information is restored by setting the contents of K to the before contents of K. When K is greater than 0020 but less than 0023, the location of K is in a special editing location of erasable memory, in which case the information is restored by setting the contents of K to the before edited contents of K. The entire operation of TC K (for $0020 \leq K$) can be formulated as follows:

(1) Execute next the instruction located at K instead of at $z = L + 1$.

(2) Set $c(Z) = (TC\ K) + 1 = b(B) + 1$.

(3) Set $c(Q) = z = b(Z)$, $z = L + 1$.

(4) Restore $c(K) = b(K)$, if $0024 \leq K \leq 1777$.
If $0020 \leq K \leq 0023$, then $c(K) = b^e(K)$.

The TC K instruction consists of only one subinstruction, TC0. Figure 4-185 illustrates the execution of TC 6145 as an example. Assume that the present instruction is located at address 2670 of the F memory. The command TC 6145 means that the instruction f located at 6145 shall be executed next instead of the instruction located at z = 2671, the next instruction of the present sequence of instructions. Instruction f might be the first instruction of another program, of a subroutine, etc. The address (z) of the next instruction is transferred from register Z to Q in order to be available in case a return to the origianl sequence of instructions is requested.

The entire code of instruction TC 6145 (06145) was entered into register B during the execution of the previous instruction, and B now contains b = 006145. The order

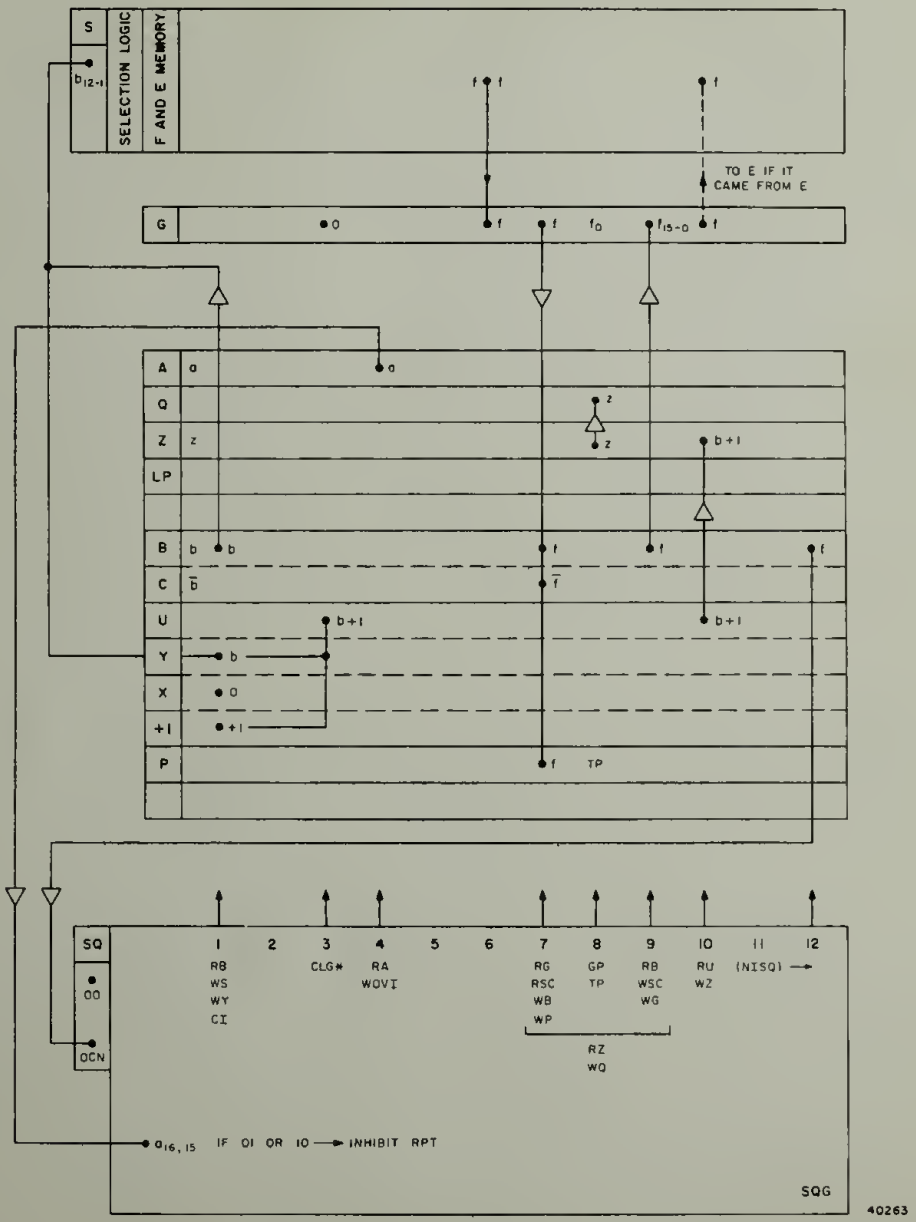

Figure 4-185. Subinstruction TC0

code 00 was entered into register SQ at action 12 of previous instruction by control pulse NISQ. In so doing, the SQG was set to execute a TC instruction. At action 1, the relevant address 6145, contained in bit positions 12 through 1 of B, is transferred to register S and the selection logic gates a location with address 6145 for readout and write-in. The content of register BNK determines which location with address 6145 is selected. At the same time, the entire content of register B is fed into Y, and X is cleared. Control pulse CI forces a one into the adder; thus a one is added to b. The sum b + 1 = 006146 is available at the output of the adder (U) within 3 microsecond. At action 3, register G is cleared. At action 4, bits 16 and 15 contained in register A are transferred to the SQG for test of overflow or underflow. If both bits are ZERO's or both bits are ONE's, no overflow or underflow occurred and control pulse WOVI has no consequence. In case the two bits are not equal, interrupt at the end of the current instruction is inhibited in order to save the overflow bit. The overflow bit would be lost in the process of transferring the content of register A to location 0024 as requested by a program interruption. Actions 7, 8, and 9 of instruction TC K are very similar to the STMIC in STD 2 with the exception that control pulses RZ and WQ are added to transfer next address z = 2671 from register Z to Q. Instruction f located at address 6145 is transferred from the F memory into register G at action 6, and from G into B and P at action 7. At action 8 the parity of word f is tested, an alarm is caused in case of incorrect parity, and a new parity bit (f_o) for quantity f is generated and entered into G. At action 9 instruction f is returned to register G. At action 10, b + 1 = 006146 is entered into register Z and becomes the next address 6146. At action 12 order code OCN of instruction f is entered into register SQ to initiate the execution of instruction f. (If K refers to a flip-flop register, the STMIC has an effect similar to that shown on figure 4-184.)

Instruction XCH K (Exchange Data with Location K, Order Code 03) means: exchange data contained in the accumulator (A) with data stored at location K. If K represents a location in F memory, then XCH transfers data from K to A but data in K remains undisturbed. Therefore the optional code CAF (clear and add F) may be used. The entire operation XCH K can be formulated as follows:

(1) Set c(A) = b(K) and c(K) = b(A) if $0024 \leq K \leq 1777$.
If $2000 \leq K$, set c(A) = b(K) only.
If $0020 \leq K \leq 0023$, then $c(K) = b^e(A)$.
Remember that bit 15 (overflow bit) of A gets lost and that bit 16 (sign bit) of A moves into bit position 15 of K. Bit 16 of K moves into positions 16 and 15 of A.

(2) Execute the instructions located at z = L + 1 next.

The XCH K instruction consists of two subinstructions, XCH0 and STD2. The entire code of instruction XCH K was entered into register B and the order code (03) into register SQ during the execution of the previous instruction. Figure 4-186 illustrates the execution of subinstruction XCH0.

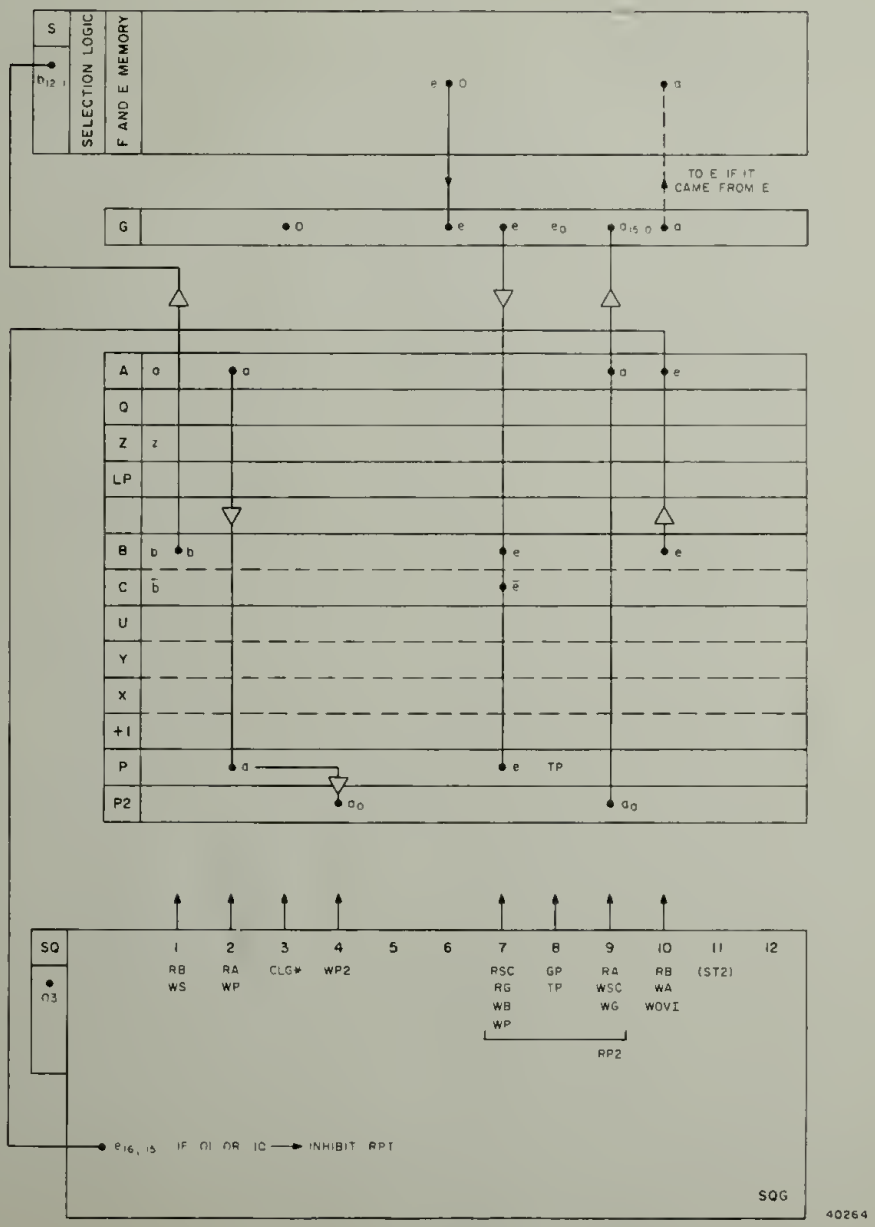

Figure 4-186. Subinstruction XCH0

Instruction CS K (Clear A and Subtract Data in K, Order Code 14) means: clear the accumulator (A) and enter into it the complemented value of the quantity stored at location K. The entire operation CS K (for $0020 \leq K$) can be formulated as follows:

(1) Set $c(A) = \bar{b}(K)$.

(2) Restore $c(K) = b(K)$ if $0024 \leq K \leq 1777$.
If $0020 \leq K \leq 0023$, then $c(K) = b^e(K)$.

(3) Execute next the instruction located at $z = L + 1$.

The CS K instruction consists of two subinstructions: CS0 and STD2. Figure 4-187 illustrates the execution of CS 1021. Quantity e located at 1021 is complemented and entered into A. During the execution of the previous instruction, the entire code of CS 1021 (41021) was entered into B (B now contains b = 141021 because bit 15 of G is written into bit positions 15 and 16 of B) and order code 14 was entered into register SQ.

Instruction TS K (Transfer Data to K, Order Code 15) means: transfer the content of the accumulator (A) to location K. If K represents a location in the F memory, then TS K is equivalent to NOOP (No Operation). If A contains no overflow or underflow, execute next the instruction at $z = L + 1$. If A contains overflow or underflow, execute next the instruction at $L + 2$, and enter the value plus one or minus one, respectively, into A. The "skip on overflow" feature is used chiefly in multiprecision operations. The entire operation TS K (for $0020 \leq K$) can be formulated as follows:

(1) Set $c(K) = b(A)$ for $0024 \leq K \leq 1777$.
If $0020 \leq K \leq 0023$, then $c(K) = b^e(A)$.
Remember that bit 15 of b(A) gets lost, and that bit 16 of b(A) moves into position 15 of c(K).

(2) If $000000 \leq b(A) \leq 037777$, or
if $177777 \geq b(A) \geq 140000$, then
keep $c(A) = b(A)$ and execute next the instruction located at $z = L + 1$.

If $040000 \leq b(A) \leq 077777$, then
set $c(A) = 000001$ and execute next the instruction located at $L + 2$.
Set $c(Z) = b(Z) + 1$.

If $137777 \geq b(A) \geq 100000$, then
set $c(A) = 177776$ and execute next the instruction located at $L + 2$.
Set $c(Z) = b(Z) + 1$.

The TS K instruction consists of two subinstructions: TS0 and STD2. Figures 4-188 and 4-189 illustrate the execution of TS 0611; figure 4-188 shows the execution without overflow, and figure 4-189 shows the execution with overflow. The quantity a stored in A is to be transferred to location 0611 in the E memory where the quantity e is presently located. During the execution of the previous instruction, the entire code of instruction TS 0611 (50611) was entered into register B (B now contains b = 150611), and order code 15 was entered into register SQ.

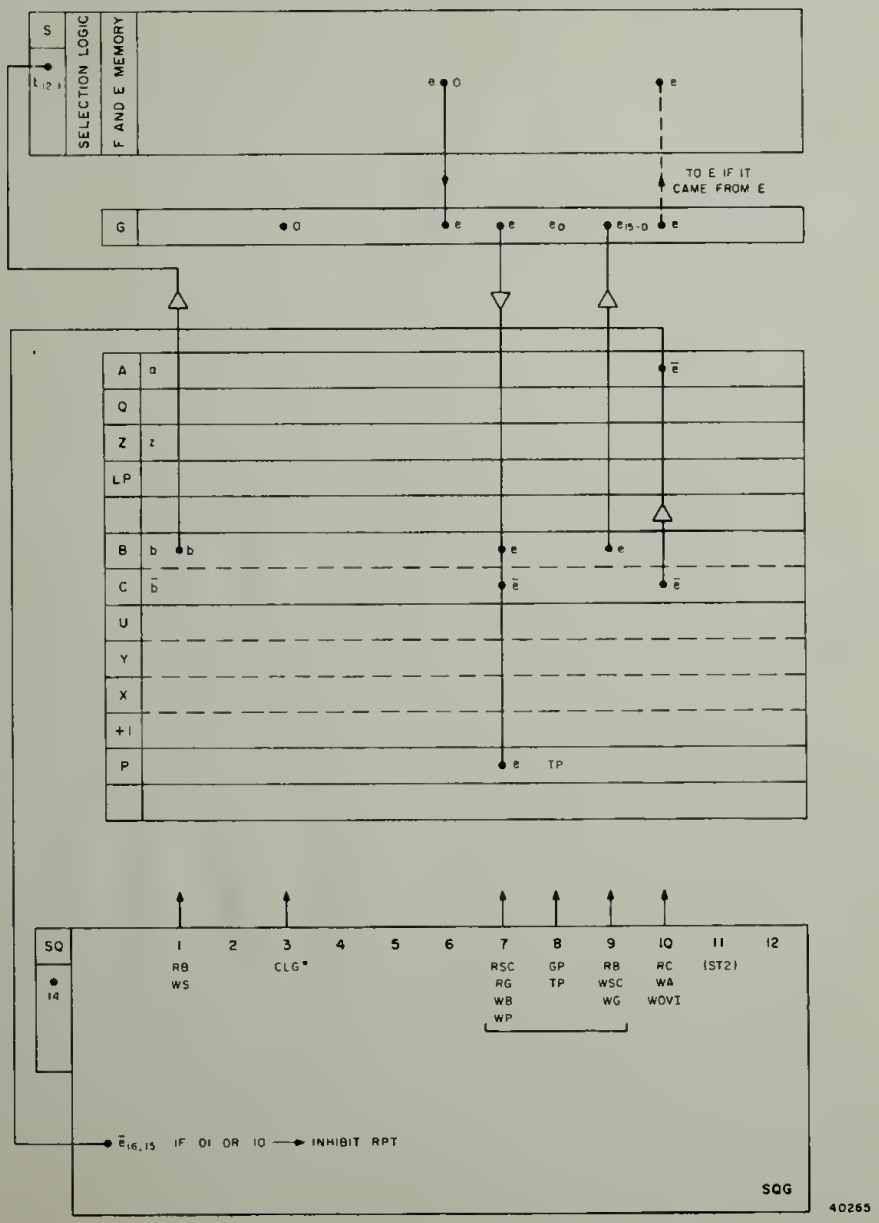

Figure 4-187. Subinstruction CS0

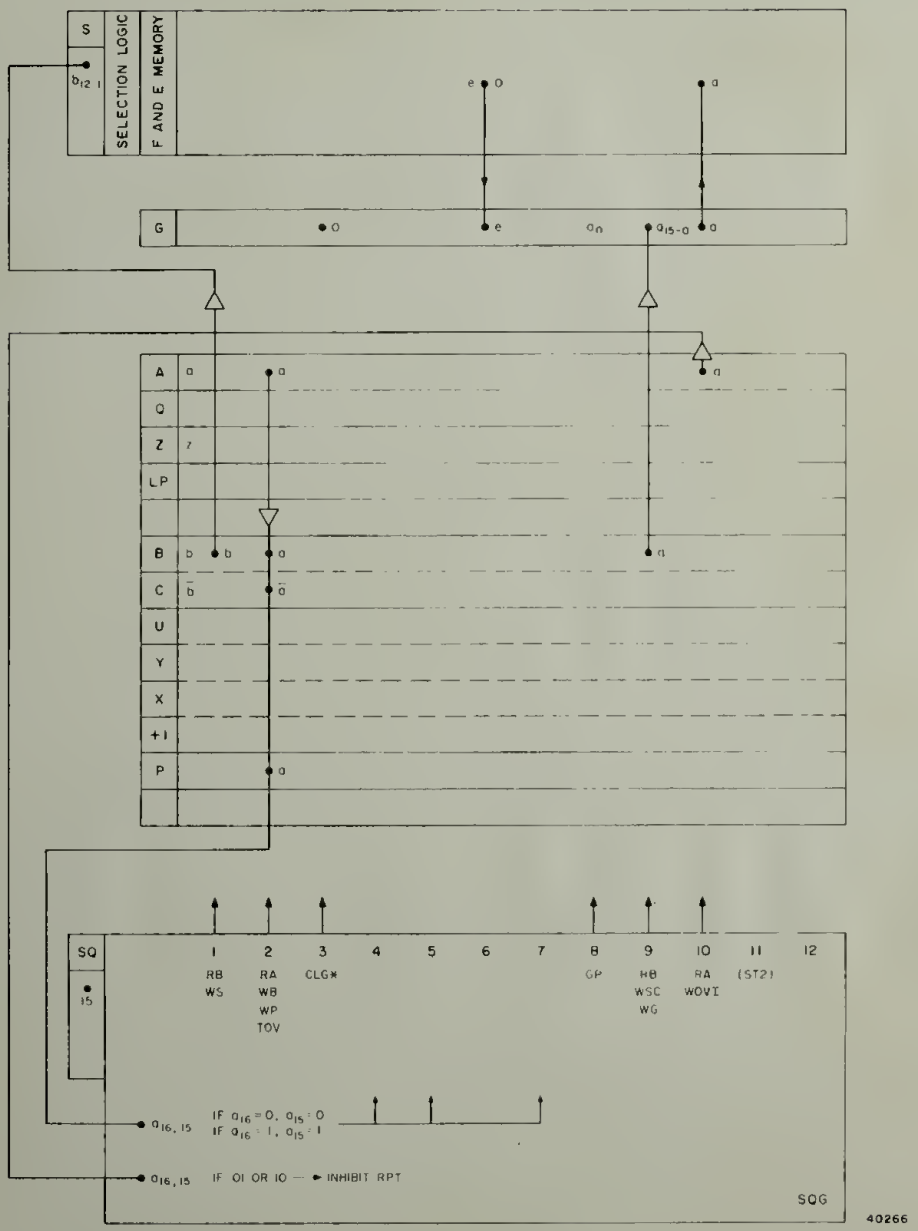

Figure 4-188. Subinstruction TS0 (without Overflow or Underflow in A)

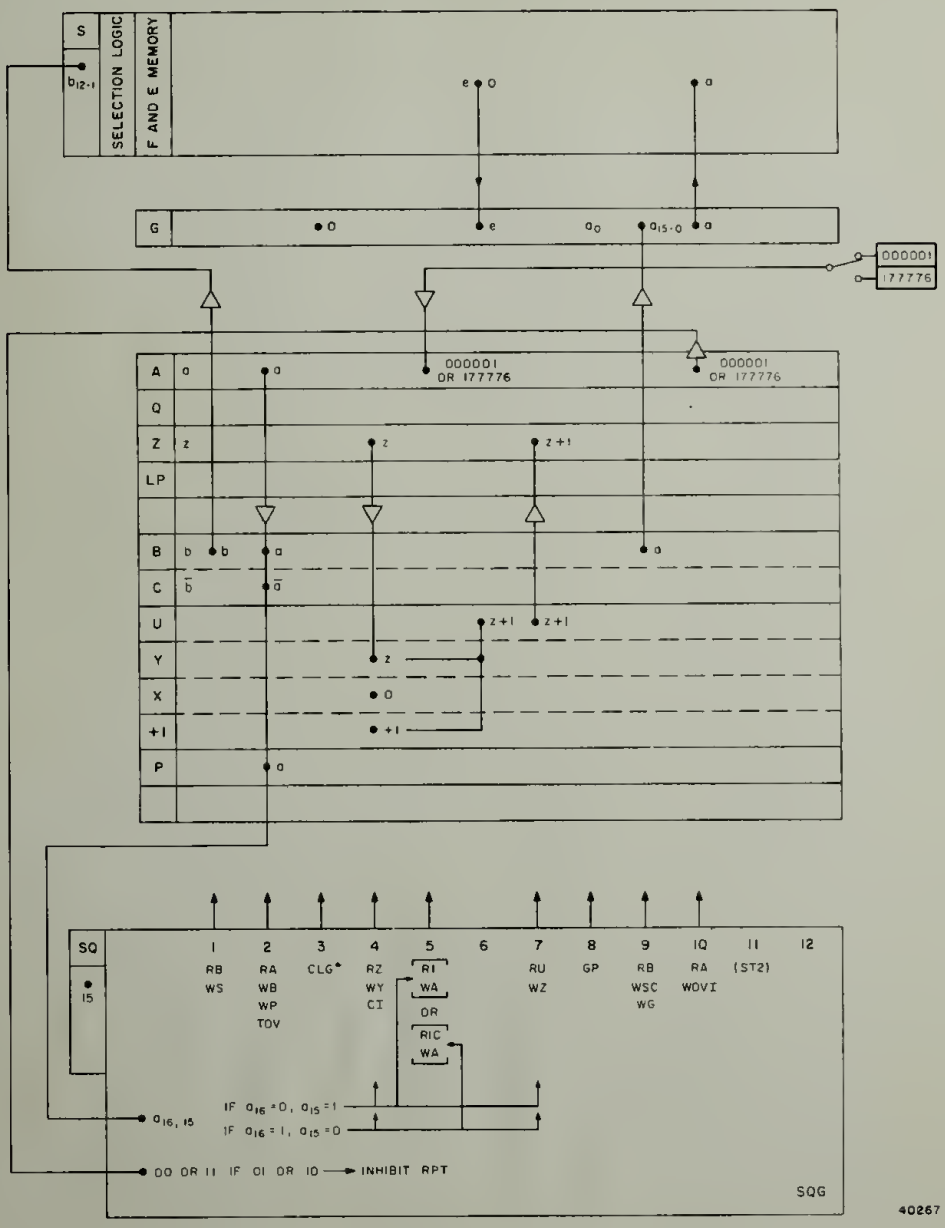

Figure 4-189. Subinstruction TS0 (with Overflow or Underflow in A)

Instruction MSK K (Mask with Data from K, Order Code 7) means: mask the content of location K with the content of the accumulator (A); AND operation for each bit position of locations A and K. This is accomplished by applying $\bar{c}(A)$ OR $\bar{c}(K)$ instead of c(A) AND c(K) for each bit position. The entire operation MSK K (for $0020 \leq K$) can be formulated as follows:

(1) Set c(A) = b(A) AND c(K).

(2) Restore c(K) = b(K) if $0020 \leq K \leq 1777$.

(3) Execute the instruction located at z = L + 1 next.

The MSK K instruction consists of two subinstructions: MSK0 and STD2. Figure 4-190 illustrates the execution of MSK 0700. The quantity e = 36000, located at K, is to be masked with the quantity a = 024252, contained in A. During the execution of the previous instruction, the entire code of instruction MSK 0700 (70700) was entered into B (B now contains b = 170700), and order code 17 was entered into register SQ.

Instruction AD K (Add Data from K and Count on Overflow or Underflow, Order Code 6) means add the quantity located at K to the quantity contained in the accumulator (A). In case of overflow or underflow, increment or decrement the overflow counter (OVCTR). The entire operation AD K (for $0020 \leq K$) can be formulated as follows:

(1) Set c(A) = b(A) + c(K).

(2) In case of overflow, set c(OVCTR) = b(OVCTR) + 1 by executing PINC. In case of underflow, set c(OVCTR) = b(OVCTR) - 1 by executing MINC.

(3) Restore c(K) = b(K) if $0024 \leq K \leq 1777$.
If $0020 \leq K \leq 0023$, then $c(K) = b^e(K)$.

(4) Execute the instruction located at z = L + 1 next.

The AD K instruction consists of two subinstructions: AD0 and STD2. In case of overflow or underflow, it takes 3 MCT's to perform an addition.

Figure 4-191 illustrates the execution of AD 1043. Quantity e located at 1043 is to be added to the quantity a in A. During the execution of the previous instruction, the entire code of instruction AD 1043 (61043) was entered into B (B now contains b = 161043), and order code 16 was entered into register SQ. In case of overflow or underflow a program interruption at the end of the current instruction is inhibited. If overflow occurs, a control pulse is sent to the counter priority control. About 10 microseconds later the counter priority control causes the SQG to initiate instruction PINC in order to increment the OVCTR by one. Incrementing the OVCTR is executed at the end of STD2. If underflow occurred, WOVC causes decrementing (MINC) the OVCTR by one.

Instruction NDX K (Index Next Instruction, Order Code 2) means: use as the next instruction the arithmetic sum of the instruction located at the next address z = L + 1

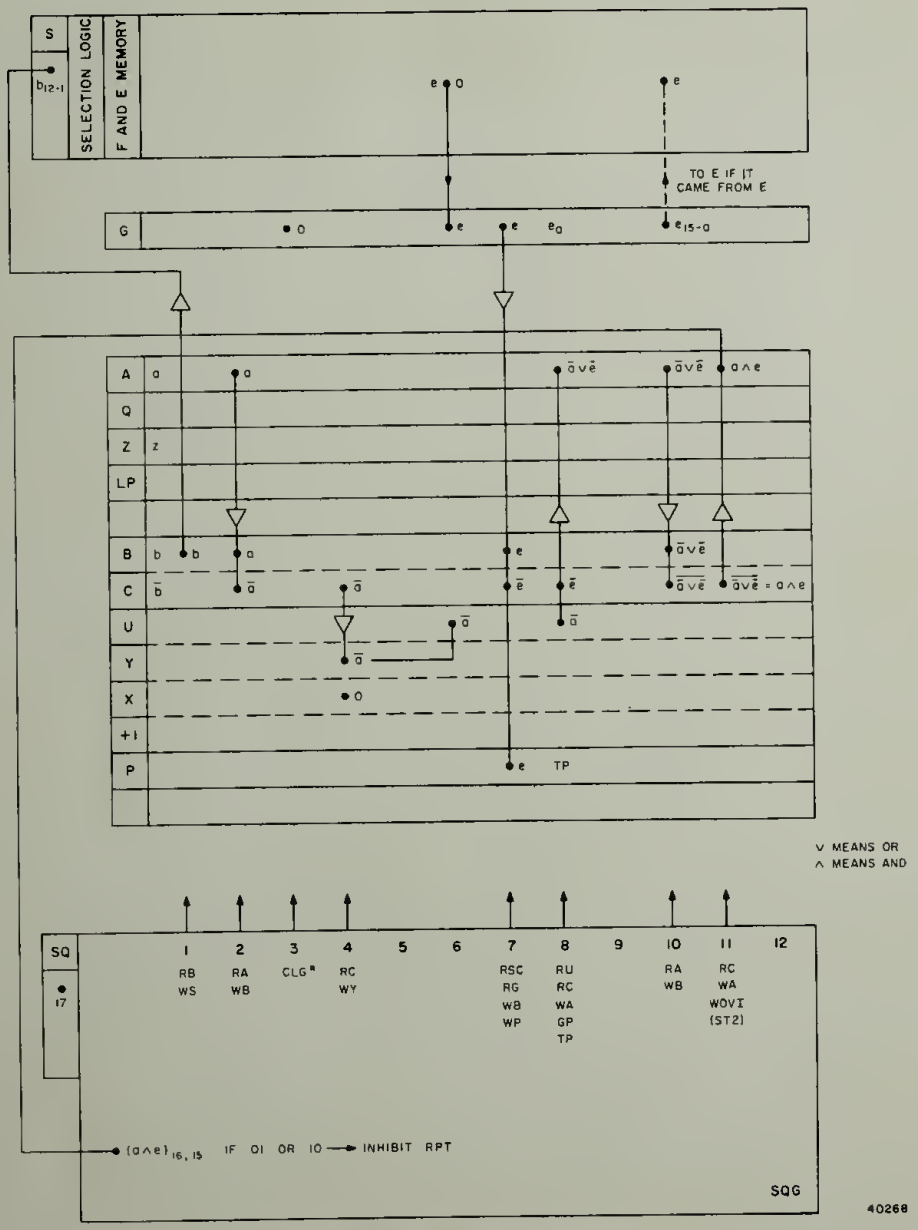

Figure 4-190. Subinstruction MSK0

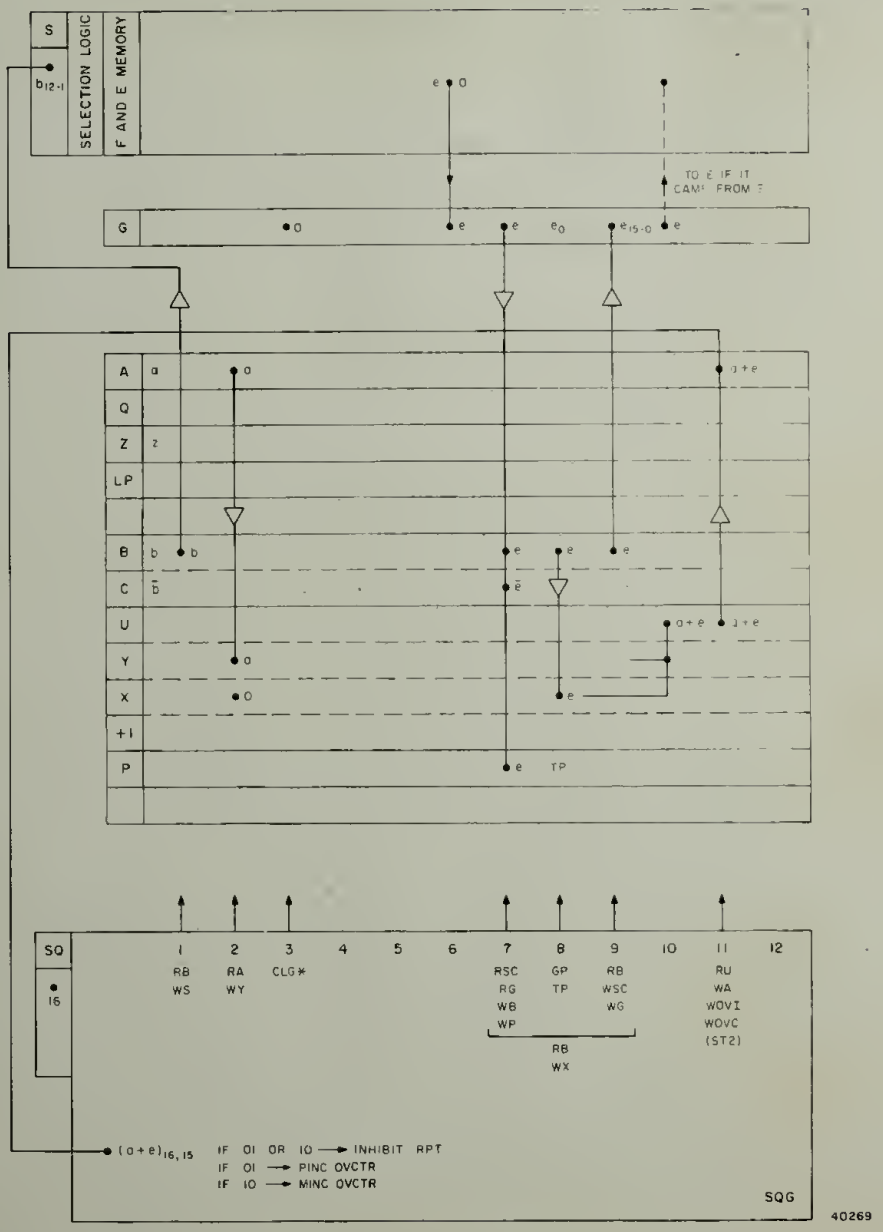

Figure 4-191. Subinstruction AD0

plus the quantity located at K. Address K may be any address except 0025. If K = 0025, this is instruction RESUME. When no overflow or underflow of the 4 bit order code occurs during addition, the new instruction remains a basic instruction. When underflow occurs, the new instruction is an extra code instruction. The entire operation NDX X (for 0020 $\leq$ K, except K = 0025) can be formulated as follows:

(1) Set c(B) = c(Z) + c(K), z = L + 1.

(2) Restore c(K) = b(K) if 0024 $\leq$ K $\leq$ 1777.
If 0020 $\leq$ K $\leq$ 0023, then c(K) = b^e(K).

(3) After the execution of the instruction put into B, execute next the instruction located at L + 2, L being the location of the NDX instruction. If the instructions at L + 1 and K are TC instructions (and if no overflow or underflow occurs during addition), the instruction to be executed next is not located at L + 2 but at address c(L + 1) + c(K).

The NDX K instruction consists of two subinstructions: NDX0 and NDX1. Figures 4-192 and 4-193 illustrate the execution of NDX 1174, this instruction being located at address 6534. Instruction AD 2103 is located at address z = 6535. Location K = 1174 contains the quantity e = 00011. The instruction AD 2103 is to be indexed to AD 2114. During the execution of the previous instruction, the entire code of instruction NDX 1174 (21174) was entered into register B (B now contains b = 021174) and order code 02 was entered into register SQ.

Instruction CCS K (Count, Compare, and Skip with Data at K, Order Code 1) means examine the data located at K. If c(K) > +0, take as the subsequent instruction the one located at z = L + 1. If c(K) = +0, take the subsequent instruction from L + 2. If c(K) < -0, take from L + 3. If c(K) = -0, take from L + 4. K may be any address, but an instruction referring to an address in fixed memory has no purpose. The entire operation CCS K (for 0020 $\leq$ K) can be formulated as follows:

(1) If 00000 < c(K) < 37777, set c(A) = c(K) - 00001 and execute the instruction located at z = L + 1 next.

If c(K) = 00000, set c(A) = 000000 and execute the instruction located at L + 2 next.

If 40000 < c(K) < 77777, set c(A) = $\overline{c}$(K) - 00001 = $\lceil$c(K)$\rceil$ - 00001 and execute the instruction located at L + 3 next.

If c(K) = 77777, set c(A) = 000000 and execute the instruction located at L + 4 next.

(2) Restore c(K) = b(K) if 0024 $\leq$ K $\leq$ 1777.
If 0020 $\leq$ K $\leq$ 0023, then c(K) = b^e(K).

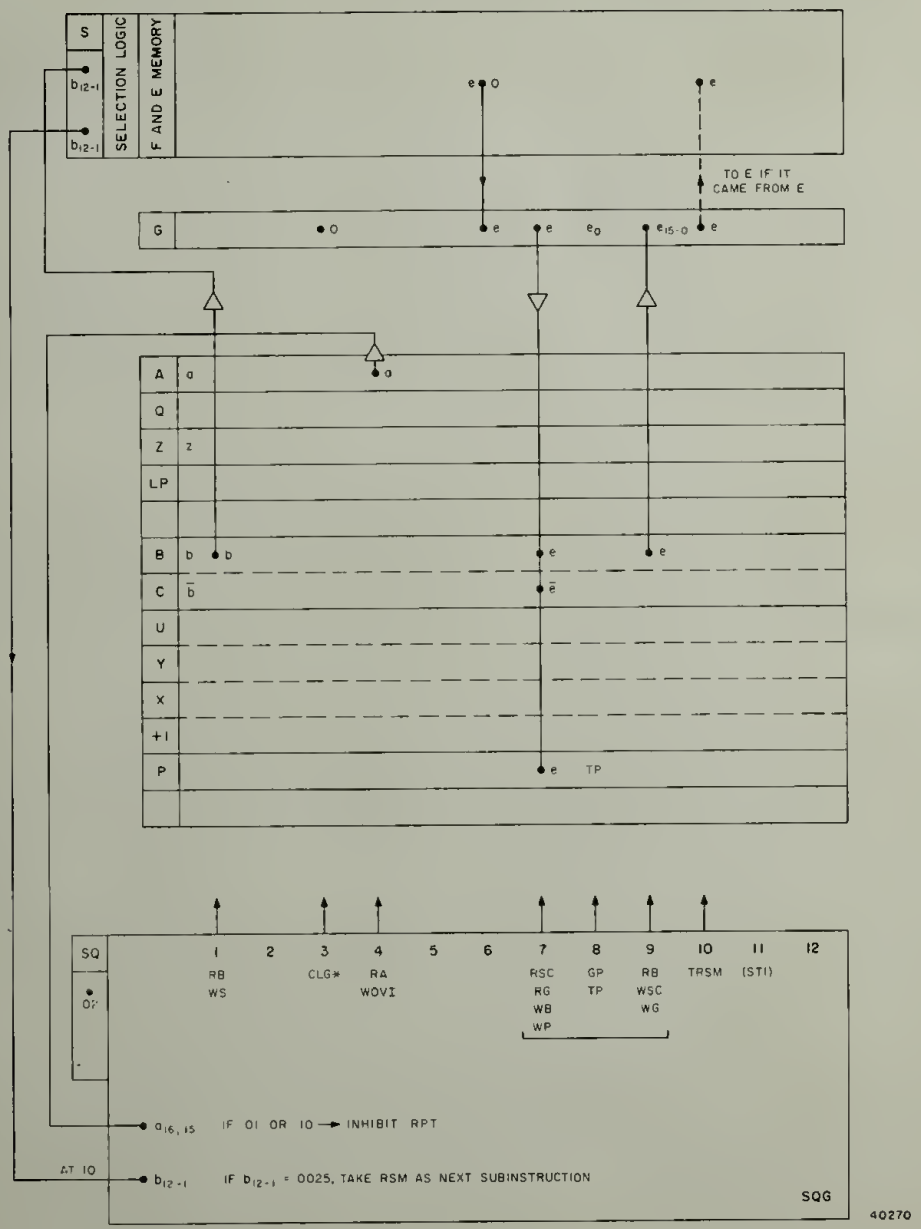

Figure 4-192. Subinstruction NDX0

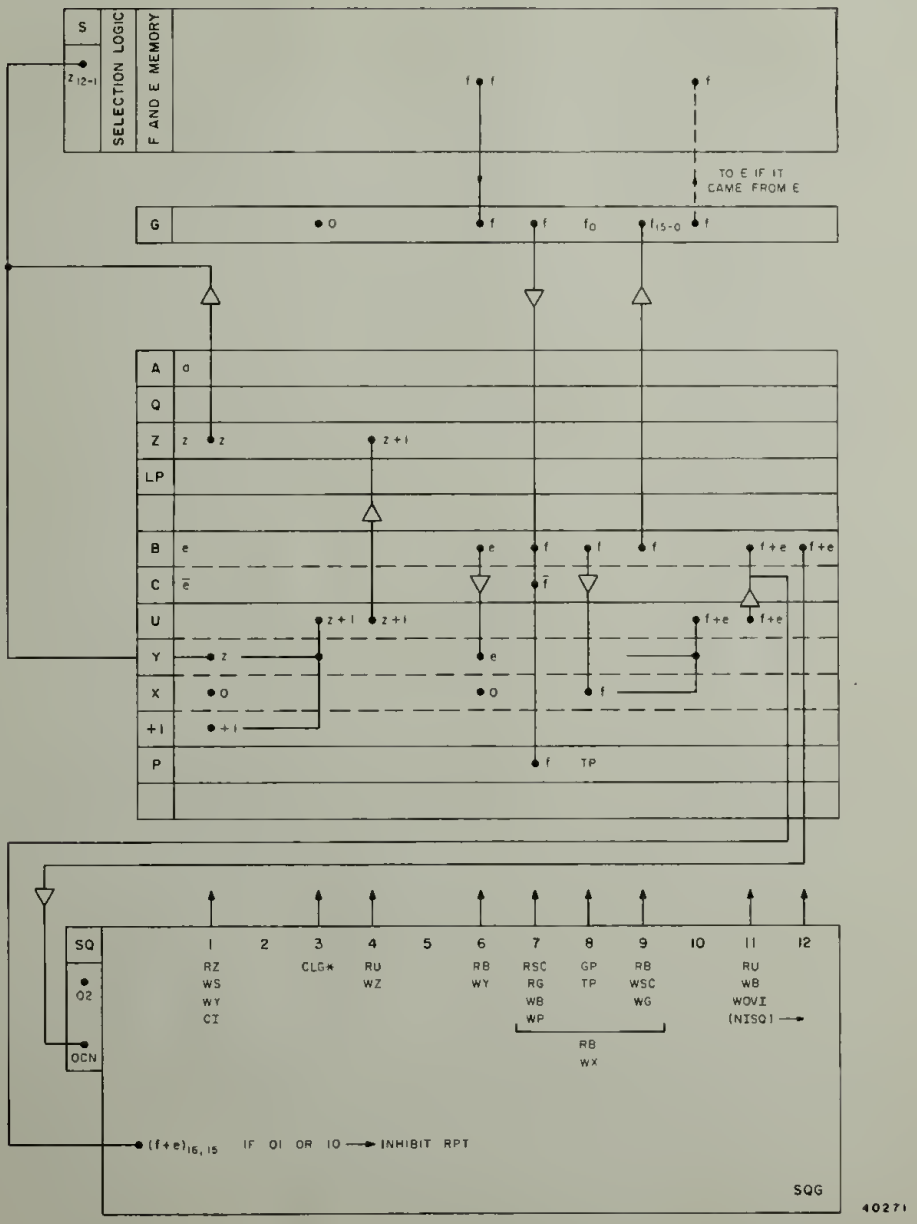

Figure 4-193. Subinstruction NDXI

The CCS K instruction consists of two subinstructions: CCS0 and CCS1. Figures 4-194 through 4-198 and table 4-XXII illustrate the execution of CCS 1051 being located at 6040. Content e of location 1051 is to be examined and, dependent on the result, the instruction to be executed next is to be taken from location 6041, 6042, 6043, or 6044. During the execution of the previous instruction, the entire code of instruction CCS 1051 (21051) was entered into register B (B now contains b = 021051) and order code 02 was entered into register SQ.

Table 4-XXII. Contents of A and Z at End of CCS0 and CCS1

Initial Condition c(K) = e	α (Content of A At End of CCS0)	δ (Content of Z At End of CCS0)	$\delta + 1$ (Content of Z At End of CCS1)	$\overline{\alpha + 1}$ (Content of A At End of CCS1)
e > +0	$\bar{e}$	z	z + 1	e - 1
e = +0	177776	z + 1	z + 2	+0
e < -0	e	z + 2	z + 3	$\bar{e}$ - 1
e = -0	177776	z + 3	z + 4	+0

4-8.8.1.2 Extra Code Instructions. There are three code instructions: multiply, divide, and subtract. The multiply instruction multiplies the accumulator contents by the contents of a given location. The result, because of its length, is stored in the accumulator and another register. The contents of the accumulator are squared if the given location is the accumulator.

The divide instruction divides the contents of a given location into the accumulator contents. The quotient is stored in the accumulator; any remainder is stored separately.

The subtract instruction subtracts the contents of a given location from the accumulator contents. The result is stored in the accumulator. If the accumulator was initially cleared, the subtract instruction copies the complement of the contents of a given location into the accumulator. If the given location is the accumulator, the result is a minus zero.

Extra code instructions are derived by indexing (modifying) basic instructions and are executed as the modified order codes are entered into the SQG. If modification of only the order code is desired (no modification of the relevant address), instruction NDX 5777 is executed. This is the mnemonic code for EXTEND. The location 5777

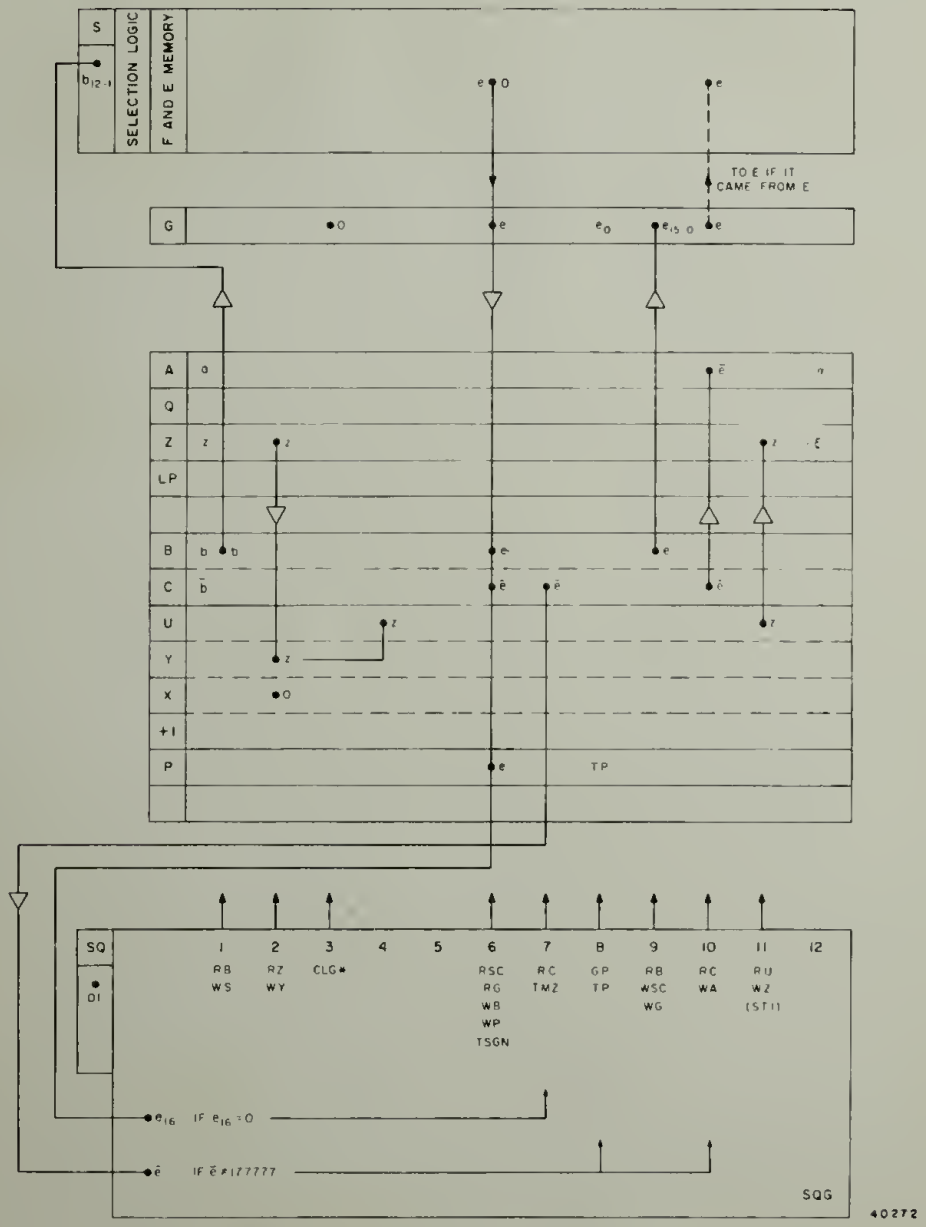

Figure 4-194. Subinstruction CCS0 (Example e > +0)

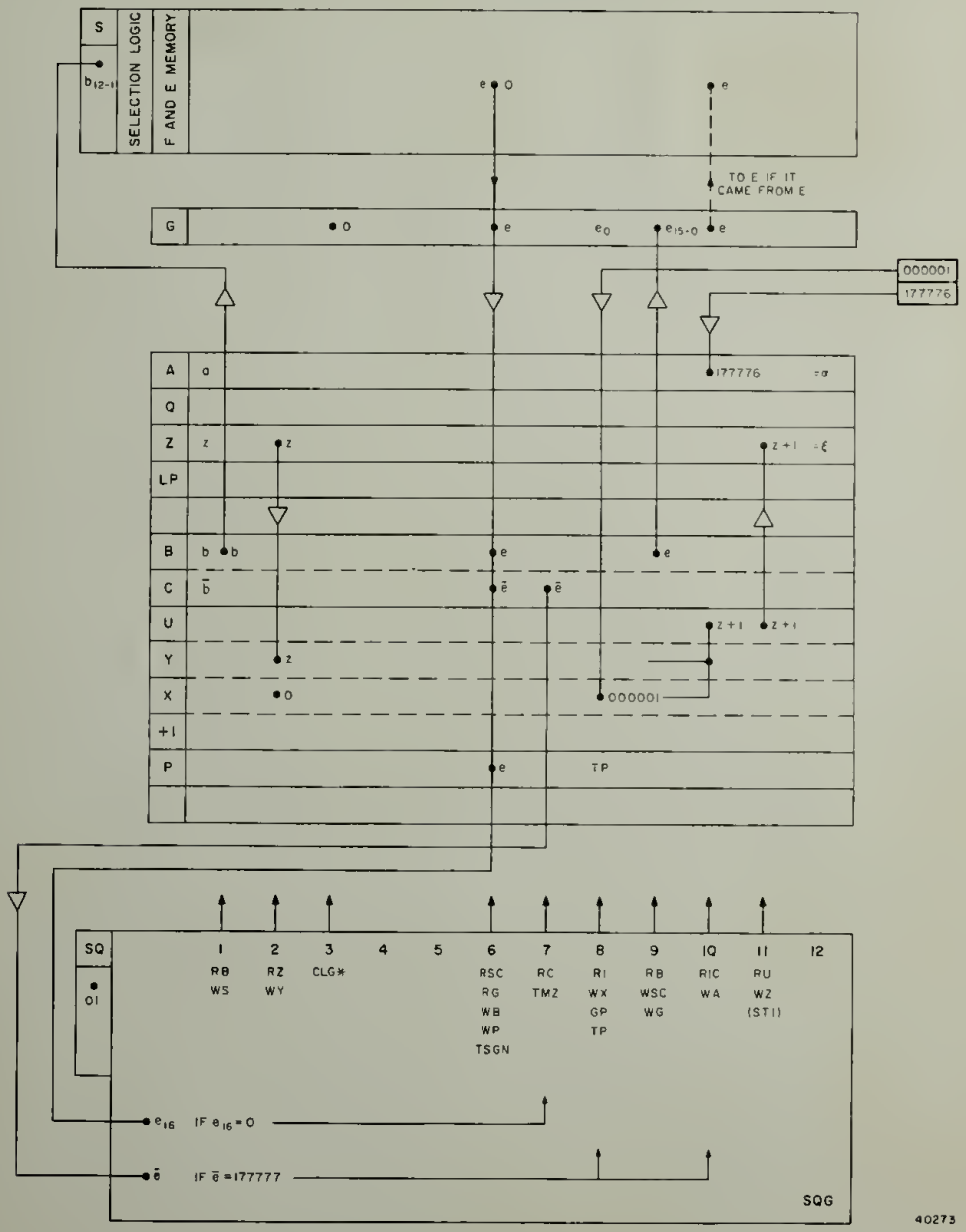

Figure 4-195. Subinstruction CCS0 (Example e = +0)

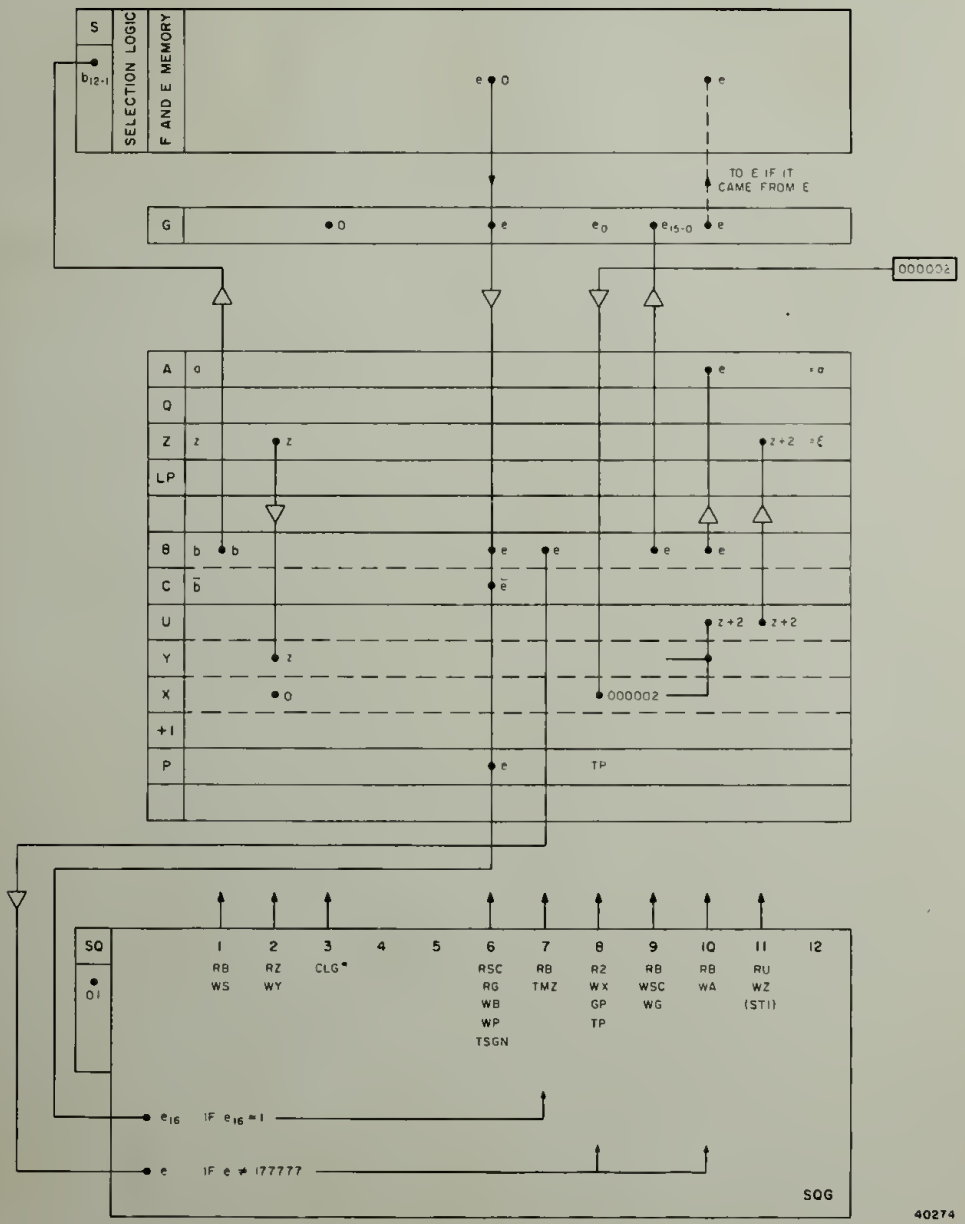

Figure 4-196. Subinstruction CCS0 (Example e < +0)

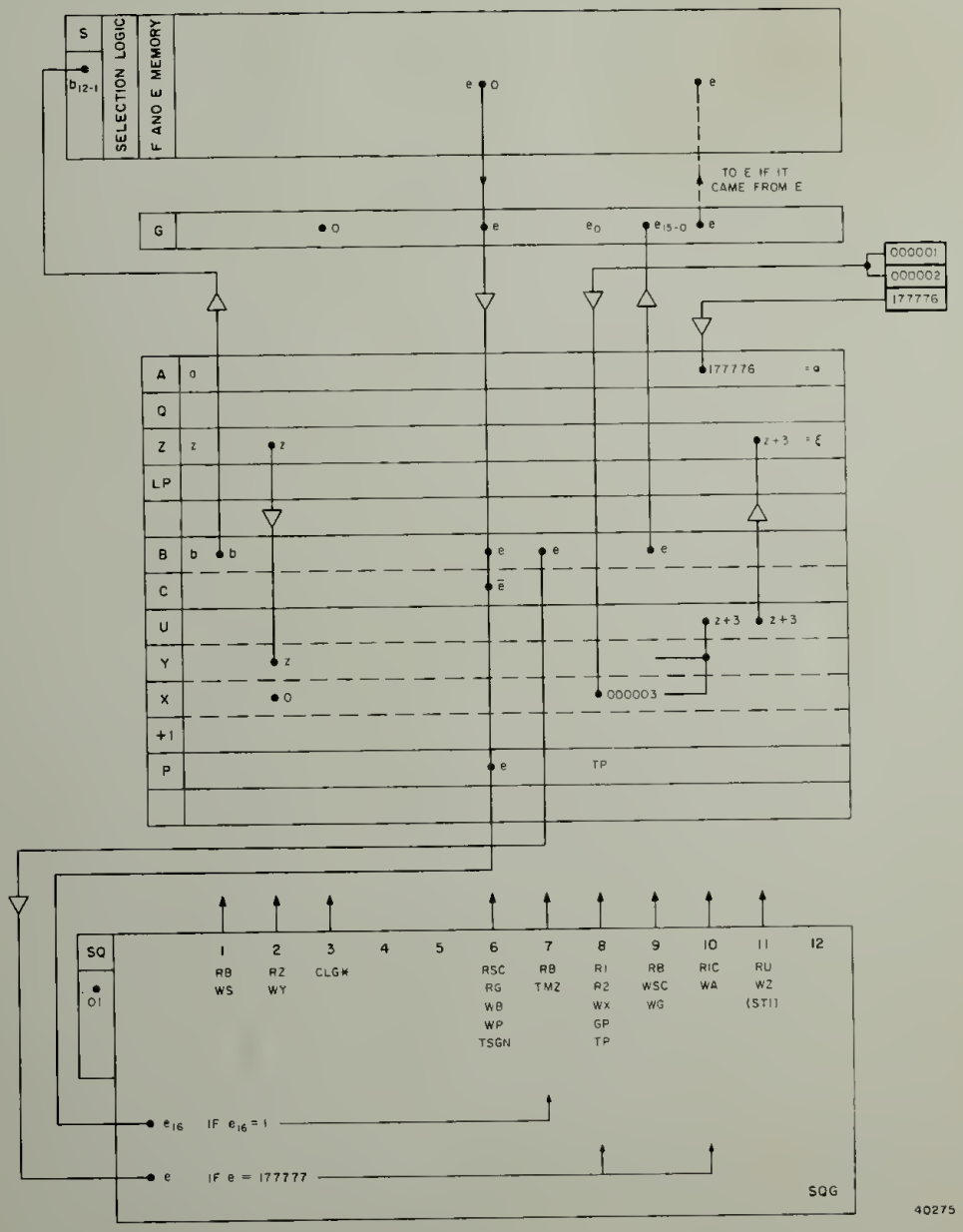

Figure 4-197. Subinstruction CCS0 (Example e = -0)

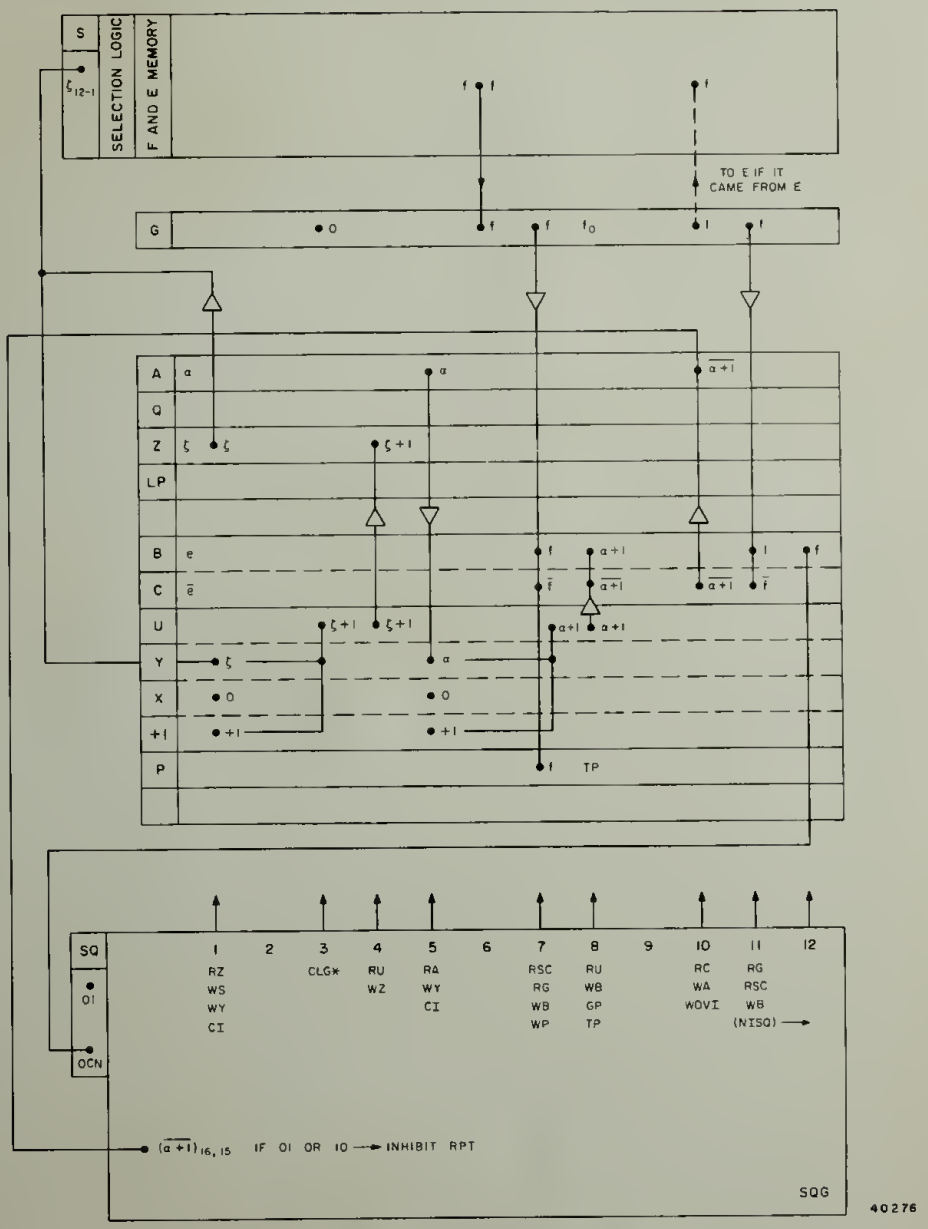

Figure 4-198. Subinstruction CCS1

contains the quantity 47777; for example, if NDX 5777 is followed by AD 1043, then the derived extra code instruction is 161043 + 147777 = 131043. The new order code entered into register SQ is 13.

Instruction SU K (Subtract Data from K and Count on Overflow or Underflow, Order Code 6 with EXTEND Preceding) means: subtract the quantity located at K from the quantity contained in the accumulator (A). In case of overflow or underflow, increment or decrement the overflow counter (OVCTR). Instruction SU K is very similar to AD K, except that the subtraction is established by adding the complemented value located at K rather than the original value to the quantity in A. The entire operation SU K (for $0020 \leq K$) can be formulated as follows:

(1) Set $c(A) = b(A) + \bar{c}(K)$.

(2) In case of overflow, set $c(OVCTR) = b(OVCTR) + 1$ by executing PINC. In case of underflow, set $c(OVCTR) = b(OVCTR) - 1$ by executing MINC.

(3) Restore $c(K) = b(K)$ if $0024 \leq K \leq 1777$.
If $0020 \leq K \leq 0023$, then $c(K) = b^e(K)$.

(4) Execute the instruction located at $z = L + 1$ next.

The SU K instruction consists of two subinstructions: SU0 and STD2. Since an NDX and an SU instruction have to be executed to perform a subtraction, the time needed for a subtraction is 4 or 5 MCT's.

Figure 4-199 illustrates the execution of SU 1043. Quantity e, located at 1031, is to be subtracted from the quantity a in register A. The entire code of the instruction was entered into register B during the execution of the preceding NDX instruction (B now contains b = 131043) and order code 13 was entered into register SQ. Figure 4-199 is very similar to figure 4-195 except that quantity e is taken from register C instead of e from register B.

Before the execution of instruction MP K (Multiply with Data at K, Order Code 4 with EXTEND Preceding) is discussed, the principle of multiplication applied should be explained. Figure 4-200 demonstrates the multiplication of binary number e = +1110 with a = +1011. First it is shown how the multiplication can be carried out manually, and then by a computer similar to the AGC. The procedure is basically the same for both approaches but with two differences. With manual operation the quantity e is shifted left each time it is multiplied by a digit of a, and the partial products are then all added at once. With the machine, only two numbers may be added at a time; therefore, it is necessary to compute subtotals of the partial products. In the example, registers Y, X, U, A, and LP each consist of six bit positions. At instant 4 quantity e is entered into register Y (the four value bits into positions 4 through 1, the sign into positions 5 and 6) because the lowest bit of multiplier is a ONE. The quantity zero is fed into X at instant 5. At instant 6 the content of register U (the sum of Y and X) is equal to e. At instant 8 the content of register U is transferred to A and shifted one place to the right. Bit 1 of U is moved into position 4 of LP at the same time. The quantity in A and LP_4 (bit position 4 of LP) represents the first subtotal. Positions 3, 2, and 1 of LP may contain any information used for other purposes. Positions 5 and 6 of LP contain the

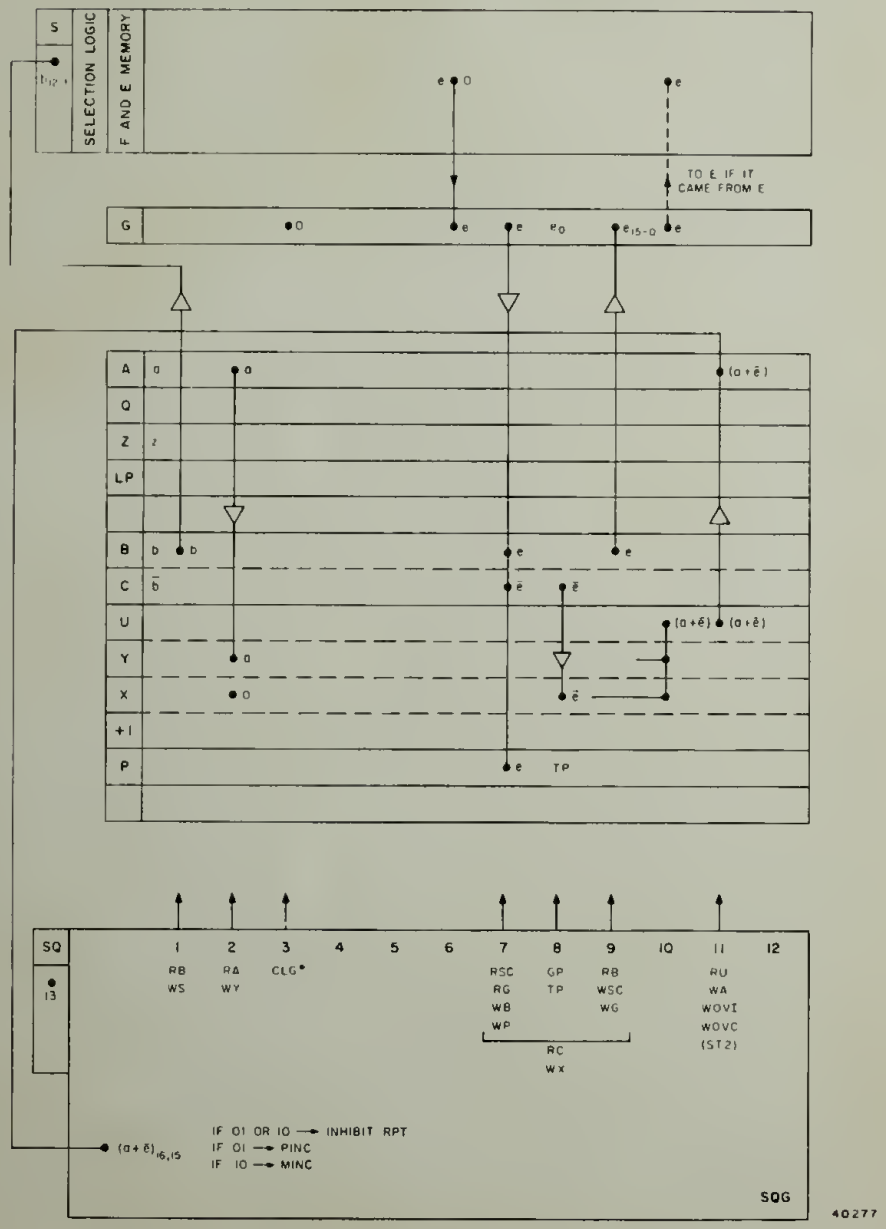

Figure 4-199. Subinstruction SU0

MANUAL OPERATION

$a = +1011$	$e \cdot a = \underline{1110 \cdot 1011}$
$e = +1110$	1110
	1110
	0000
	1110
	10011010

MACHINE OPERATION

INSTANT	FUNCTION	REGISTERS Y,X,U,A						REGISTER LP				
		6	5	4	3	2	1	4	3	2	1	
4	$e \rightarrow Y$	0	0	1	1	1	0	X	X	X	X	
5	$o \rightarrow X$	0	0	0	0	0	0					
6	U	0	0	1	1	1	0					
8	$U \rightarrow A, LP_4$	0	0	0	1	1	1	0	X	X	X	1st SUBTOTAL
9	$A \rightarrow Y$	0	0	0	1	1	1					
10	$e \rightarrow X$	0	0	1	1	1	0					
11	U	0	1	0	1	0	1					
13,14	$U \rightarrow A, LP_4; \overrightarrow{LP_3}$	0	0	1	0	1	0	1	0	X	X	2nd SUBTOTAL
15	$A \rightarrow Y$	0	0	1	0	1	0					
16	$o \rightarrow X$	0	0	0	0	0	0					
17	U	0	0	1	0	1	0					
19,20	$U \rightarrow A, LP_4; \overrightarrow{LP_{3,2}}$	0	0	0	1	0	1	0	1	0	X	3rd SUBTOTAL
21	$A \rightarrow Y$	0	0	0	1	0	1					
22	$e \rightarrow X$	0	0	1	1	1	0					
23	U	0	1	0	0	1	1					
25,26	$U \rightarrow A, LP_4, \overrightarrow{LP_{3,2,1}}$	0	0	1	0	0	1	1	0	1	0	PRODUCT

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Figure 4-200. Multiplication of Two Binary Numbers, Principle of Operation

same information as positions 5 and 6 of A and are not shown. At instant 9 the content of A is transferred to Y. Quantity e is entered into X at instant 10, becuase the second last bit of quantity a is a ONE. At instant 11 the sum is available in U. At instant 13 the content of LP_4 is moved to LP_3 (by shifting the whole content of LP one position to the right). The quantity in U is shifted and entered into A and LP_4 at instant 14. The quantity in A and $LP_{4,3}$ represents the second subtotal. During instants 15 through 20 no quantity e is added, because bit 3 of multiplier a is a ZERO. The third subtotal is contained in A and three bit positions of LP. During instants 21 through 26, quantity e is again added to the content of A because bit 4 of multiplier a is a ONE. The final product is contained in A and positions 4 through 1 of LP.

Figure 4-201 illustrates the method of multiplication in more detail, in particular how quantity a = +1011 is shifted in LP and used to decide whether or not quantity e = +1110 is to be added. At instant 1 the accumulator (A) contains quantity a, which is transferred to LP and cycled one position to the right at instant 2. Note that bits 5 and 6 of quantity a are lost, that bit 1 of a is entered into bit positions 5 and 6 of LP, and that nothing is entered into bit position 4 of LP. At instant 3 the content of LP is transferred to A. Bit 6 contained in A is now used for decision-making as symbolized by an underline. Since bit 6 is a ONE, quantity e is entered into Y at instant 4. Instants 4, 5, and 6 are the same as those described for the principles of multiplication. At instant 7 the content of A is again transferred to LP and cycled, as described for instant 2. Since bit position 6 of LP contains a ONE, the quantity e is entered into Y again at instant 10. Instants 8 through 11 are the same as described for the principles of multiplication. At instants 12 and 13 the content of LP is cycled once more. Since a ZERO is now in position 6, the quantity zero is entered into X at instant 16. At instant 22 quantity e is entered into X, because bit position 6 of LP contains a ONE at instant 19. At instants 24 and 25, the content of LP is cycled the last time. After instant 26, the final product is contained in registers A and LP. Note that sign bits 6 and 5 contained in A and LP are identical. The value bits are contained in bit positions 4 through 1 of A and LP. The instruction MP K is now described.

Instruction MP K means: multiply the content of the accumulator (A) by the quantity located at K. The entire operation MP K (for $0020 \leq K$) can be formulated as follows:

(1) Set $c(A, LP) = b(A) \cdot c(K)$. To prevent erroneous results, no overflow or underflow should exist for b(A). Register A holds the high order product, LP the low order product. Fourteen value bits are stored in bit positions 14 through 1 of A, and fourteen in bit positions 14 through 1 of LP. The sign bits stored in positions 16 and 15 are identical for both registers.

(2) Restore $c(K) = b(K)$ if $0020 \leq K \leq 1777$.

(3) Execute the instruction located at $z = L + 1$ next.

Performing a multiplication requires the execution of instruction NDX, subinstruction MP0 once, MP1 six times, and MP3 once. Figures 4-202 through 4-207 illustrate the execution of MP 1032. Quantity a, contained in the accumulator (A), is to be multiplied by quantity e, located at K = 1032. The entire code of the instruction was entered into B during the execution of the preceding NDX instruction (B now contains

INSTANT	FUNCTION	REGISTERS Y,X,U,A						REGISTERS A,LP					
		6	5	4	3	2	1	6	5	4	3	2	1
1	c(A) = a							0	0	1	0	1	1
2	A → LP							1	1	–	1	0	1
3	LP → A							1	1	0	1	0	1
4	e → Y	0	0	1	1	1	0						
5	o → X	0	0	0	0	0	0						
6	U	0	0	1	1	1	0						
7	→ LP							1	1	–	0	1	0
8	U → A, LP_4	0	0	0	1	1	1			0			
9	A → Y	0	0	0	1	1	1						
10	e → X	0	0	1	1	1	0						
11	U	0	1	0	1	0	1						
12	LP → A							1	1	0	0	1	0
13	→ LP							0	0	–	0	0	1
14	U → A, LP_4	0	0	1	0	1	0			1			
15	A → Y	0	0	1	0	1	0						
16	o → X	0	0	0	0	0	0						
17	U	0	0	1	0	1	0						
18	LP → A							0	0	1	0	0	1
19	→ LP							1	1	–	1	0	0
20	U → A, LP_4	0	0	0	1	0	1			0			
21	A → Y	0	0	0	1	0	1						
22	e → X	0	0	1	1	1	0						
23	U	0	1	0	0	1	1						
24	LP → A							1	1	0	1	0	0
25	→ LP							0	0	–	0	1	0
26	U → A, LP_4	0	0	1	0	0	1			1			
	A, LP	0	0	1	0	0	1	0	0	1	0	1	0

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Figure 4-201. Multiplication of Two Binary Numbers, Method of Operation

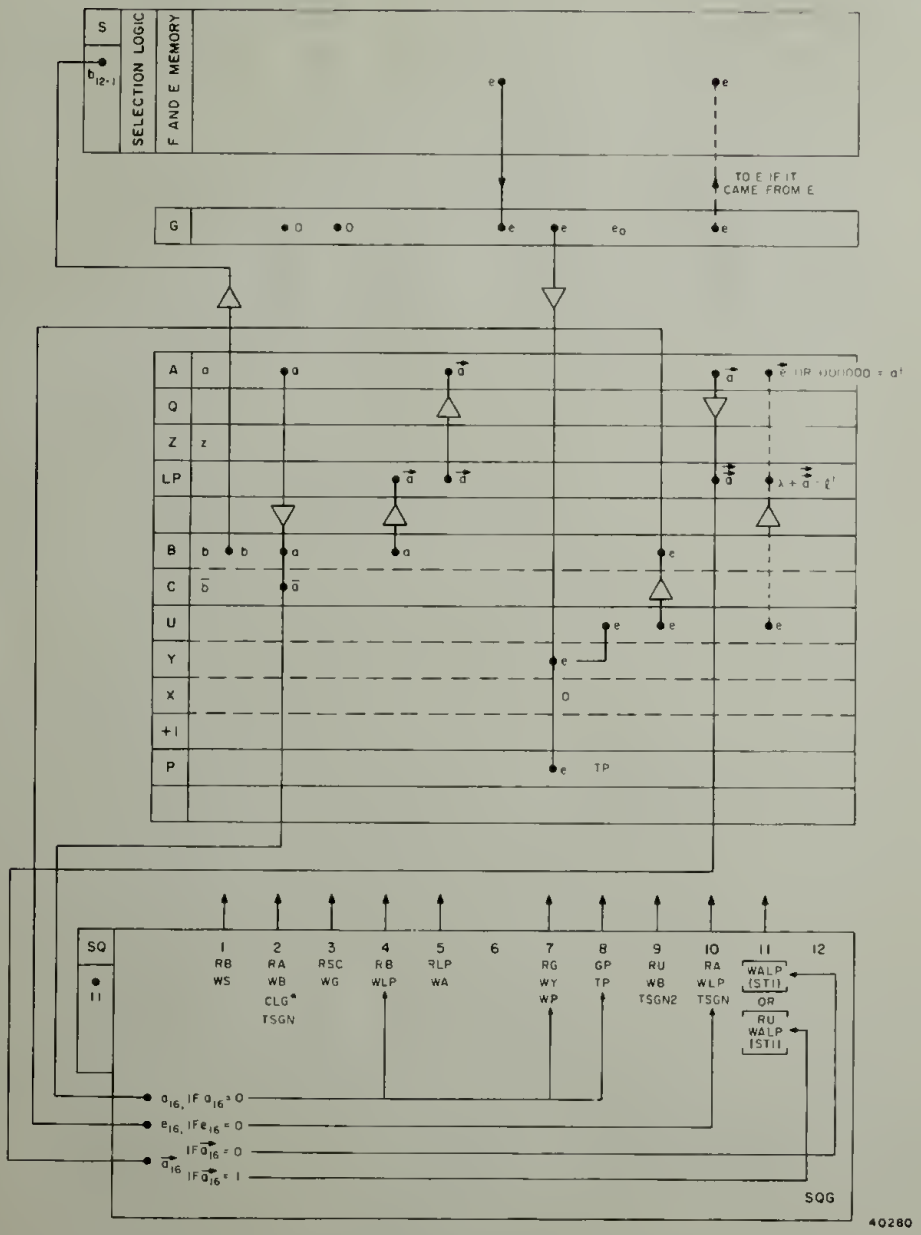

Figure 4-202. Subinstruction MP0 (a and e Positive)

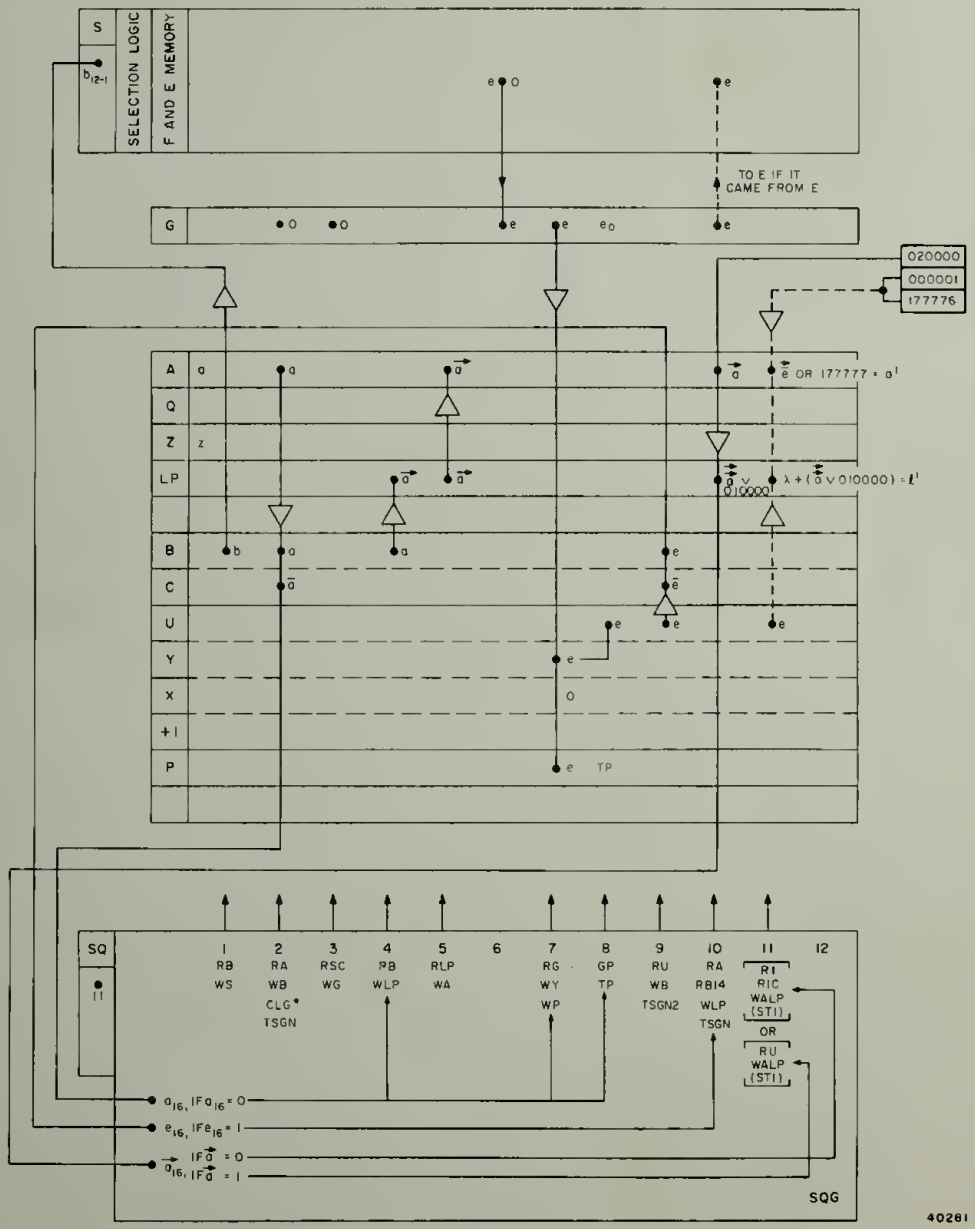

Figure 4-203. Subinstruction MP0 (a Positive and e Negative)

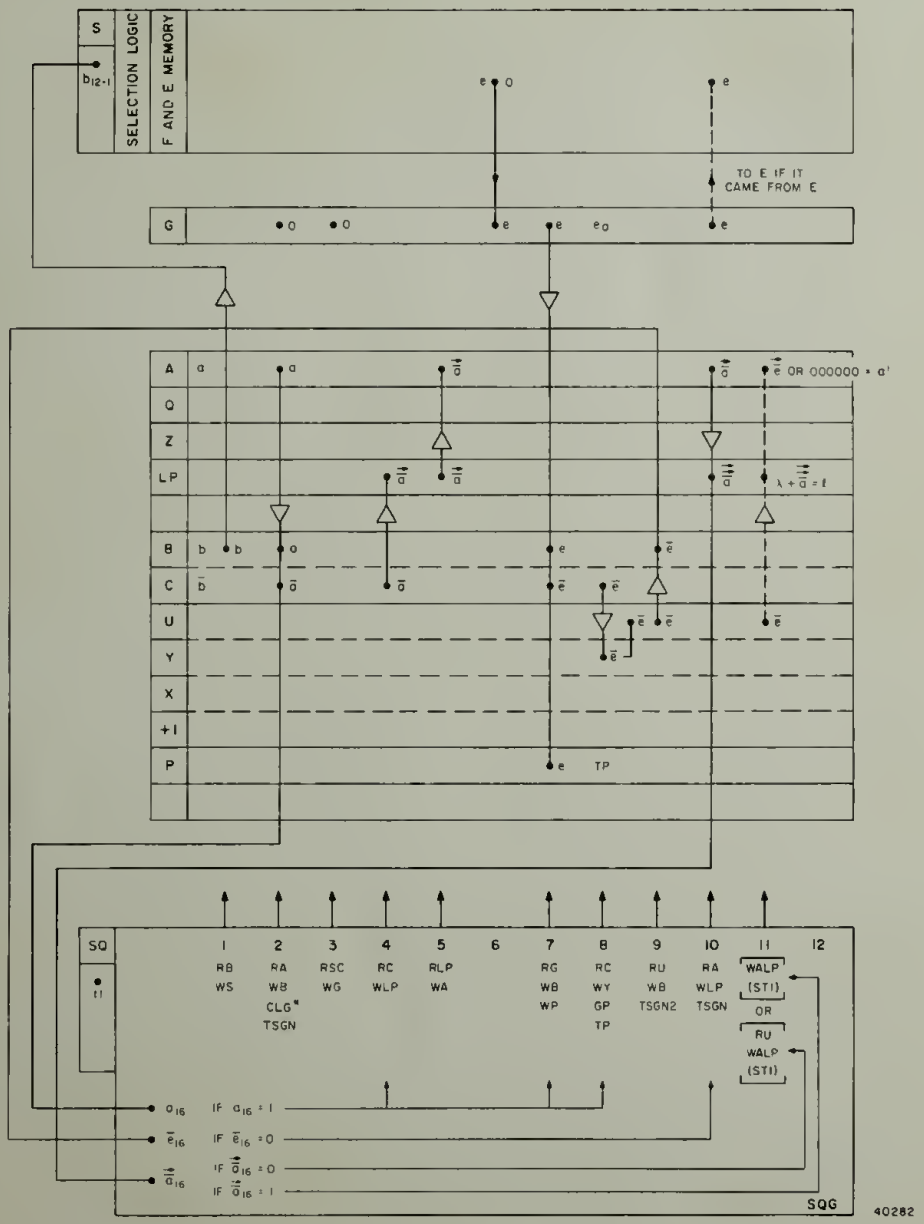

Figure 4-204. Subinstruction MP0 (a and e Negative)

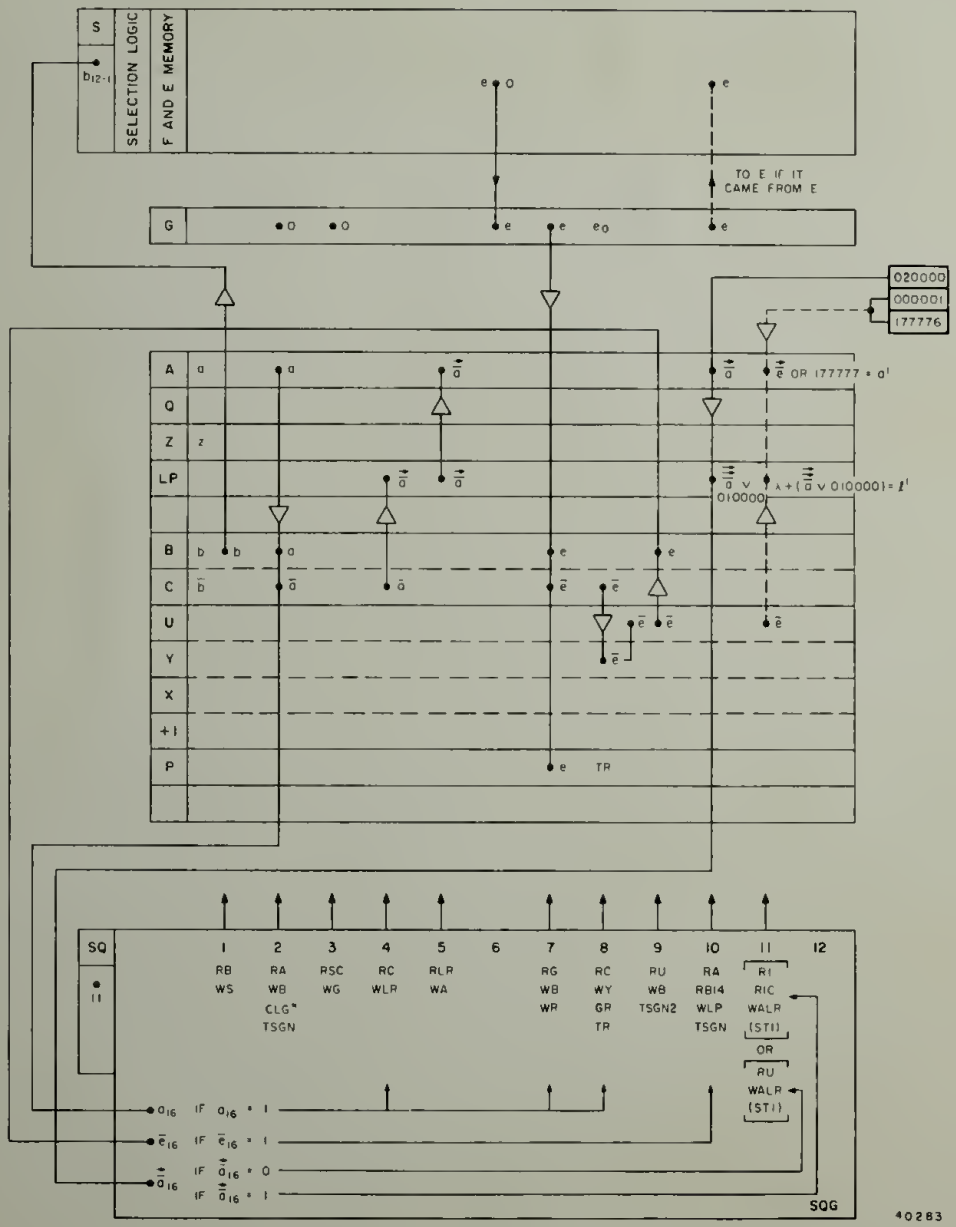

Figure 4-205. Subinstruction MP0 (a Negative and e Positive)

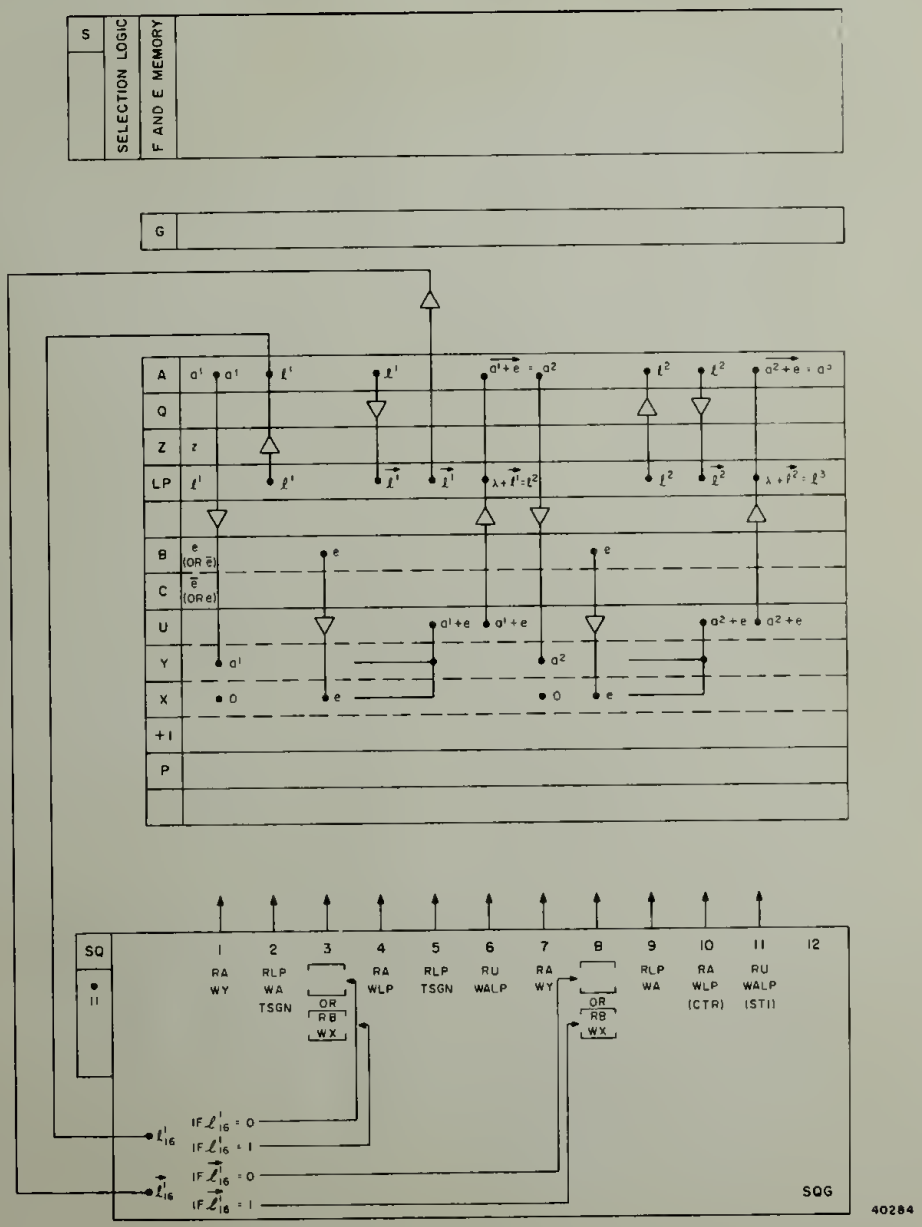

Figure 4-206. Subinstruction MP1

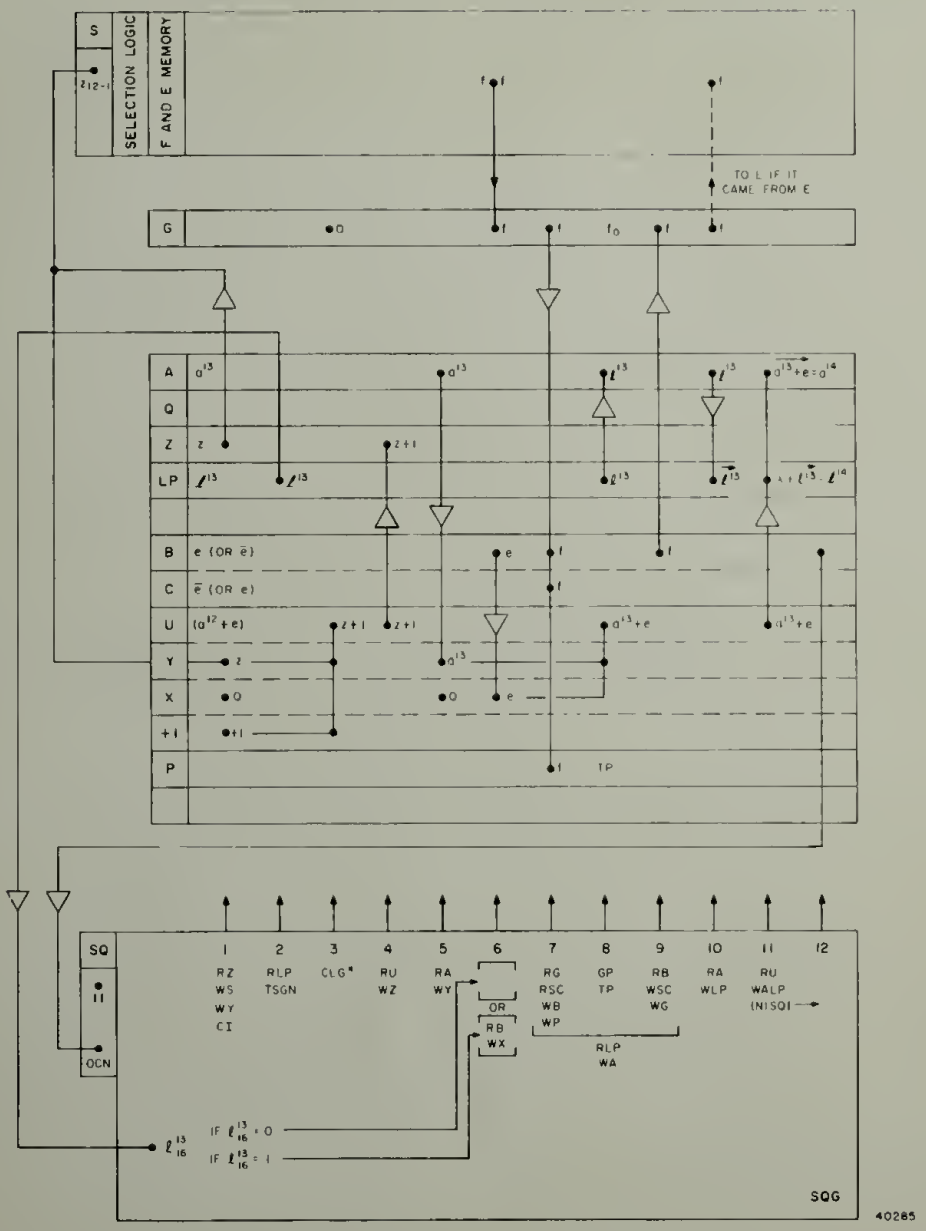

Figure 4-207. Subinstruction MP3

b - 111032), and order code 11 was entered into register SQ. At action 1 of subinstruction MP0 (figures 4-202 through 4-207) the address contained in B is transferred to S, and the selection logic gates location 1032 for readout and write-in. At action 2 register G is cleared, quantity a (the multiplier) is transferred to B, and the sign bit of a is entered into the SQG by means of TSGN. At action 3 no transfer of data occurs unless the address in register S is smaller than 0020. If c(S) $\leq$ 0017, control pulse RSC reads the selected flip-flop register into G. This arrangement makes it possible to transfer quantity a to register G and to spare quantity a.

If the sign of quantity a was found (at action 2) to be positive (figures 4-202 and 4-203), a is written into LP (and cycled one position to the right, as symbolized by $\hat{a}$) at action 4. At action 5 quantity $\hat{a}$ is transferred to A. At action 7 quantity c is entered into Y and P. A new parity bit (c_0) is entered into G, and an alarm is caused in case of incorrect parity at action 8. At action 9 quantity e is transferred to B and the sign bit of e is entered into the SQG by means of TSGN2. If the sign of e is positive (figure 4-202), quantity a contained in A is transferred to LP (and cycled another position to the right as symbolized by a) at action 10. Also at action 10, bit 16 contained in A is entered into the SQG by means of another TSGN control pulse.

If the sign of e is negative at action 9 (figure 4-203), quantity a contained in A is transferred to LP (and cycled a second time) at action 10, and a ONE is entered into bit position 13 of LP at the same time. (This is equivalent to OR'ing a ONE into bit position 3 of LP at instant 7 of figure 4-201.) Also at action 10, bit 16 contained in A is entered into the SQG. The ONE entered into bit position 13 of LP will be moved later several times to the right and, finally, will appear in bit positions 16 and 15 of LP. Since e is negative, bit positions 16 and 15 of A will also contain ONE's at the end of the multiplication.

If the sign of quantity a was found (at action 2) to be negative (figures 4-204 and 4-205), quantity $\bar{a}$ is written into LP (and cycled) at action 4. At action 5 quantity a is transferred to A. At action 7 quantity e is entered into B and P. A new parity bit (e_0) is entered into G and an alarm is caused in case of incorrect parity at action 8. Furthermore, the quantity $\bar{e}$ is entered into Y and becomes available at U. At action 9 quantity $\bar{e}$ is transferred to B and the sign bit of $\bar{e}$ is entered into the SQG by means of TSGN2. If the sign of $\bar{e}$ is positive (figure 4-204), i.e., if e is negative, quantity a contained in A is transferred to LP (and cycled) at action 10. Also at action 10, bit 16 contained in A is entered into the SQG. The operations during actions 4 through 10 replace negative quantity a by a positive quantity and negative quantity e by a positive quantity, after which the example in figure 4-204 is similar to the example in figure 4-202. The final product is positive.

If the sign of $\bar{e}$ is negative at action 9 (figure 4-205), i.e., if e is positive, quantity $\hat{a}$ contained in A is transferred to LP (and cycled) and a ONE is entered into bit position 13 of LP at action 10. Also at action 10, bit 16 contained in A is entered into the SQG. This operation replaces negative quantity a by a positive quantity, and positive quantity e by a negative quantity, after which the example in figure 4-205 is similar to the example in figure 4-203, and the final product is negative.

At action 11 of figure 4-202 the accumulator (A) is cleared if bit 16 of $\vec{a}$ is a ZERO. If bit 16 is a ONE, quantity e is shifted and entered into A and bit position 14 of LP. (Compare with instant 8 of figure 4-201.) The λ in figure 4-202 indicates that bit position 14 of LP has been filled. At action 11 of figure 4-203 the quantity minus zero (177777) is entered into A if bit 16 of $\vec{a}$ is a ZERO. If bit 16 is a ONE, quantity $\bar{e}$ is shifted and entered into A and bit position 14 of LP. Action 11 of figure 4-204 is similar to action 11 of figure 4-203, and action 11 of figure 4-205 is similar to action 11 of figure 4-203. In all four figures the content of A at action 12 is renamed a^1, and the content of LP is called l^1. The upper index 1 means containing parts of first subtotal. The first subtotal is contained in A and bit position 14 of LP and is symbolized as (a^1, l^1_{14}). Control pulse ST1 causes the SQG to execute subinstruction MP1 next. Table 4-XXIII shows the conditions of registers A, L, B, P, and Z after the execution of MP0.

Table 4-XXIII. Contents of Registers at End of MP0

INITIAL CONDITIONS	c(A)	c(LP)	c(B)	c(Z)
a POSITIVE e POSITIVE	000000 OR $\vec{e}$	$\lambda + \vec{a}$	e	z
a POSITIVE e NEGATIVE	177777 OR $\vec{e}$	$\lambda \vee 10000 + \vec{a}$	e	z
a NEGATIVE e NEGATIVE	000000 OR $\bar{\vec{e}}$	$\lambda + \vec{a}$	$\bar{e}$	z
a NEGATIVE e POSITIVE	177777 OR $\bar{\vec{e}}$	$\lambda \vee 100000 + \vec{a}$	$\bar{e}$	z

0694

Figure 4-206 illustrates the first execution of subinstruction MP1. Registers A and LP contain parts of the first subtotal before action 1. The next address (z) is still contained in Z. When MP1 is executed after MP0 of the example in figure 4-202 or 4-204, the buffer (B) contains the quantity e before action 1, as shown in table 4-XXIII and figure 4-206. When MP1 follows MP0 of the example in figure 4-203 or 4-205, B contains $\bar{e}$ instead of e. At action 1 of MP1, quantity a^1 is entered into Y. At action 2, quantity ℓ^1 is transferred to A, and bit 16 of ℓ is entered into the SQG. If bit 16 is a ZERO, no operation takes place at action 3. If bit 16 is a ONE, quantity e is entered into X (as at instant 10 of figure 4-201) and added to a^1. The quantity a^1 or the sum $a^1 + e$ is transferred to A and bit position 14 of LP at action 6. (Compare with instant 14 of figure 4-201.) After action 6 the second subtotal (a^2, ℓ^2_{14-13}) is contained in A and bit positions 14 and 13 of LP. At action 7 quantity a^2 is entered into Y. At action 4 the quantity ℓ^1 is transferred to LP (and cycled), and bit 16 of quantity ℓ^1 is entered into the SQG at action 5. If bit 16 is a ZERO, no operation takes place at action 8. (At instant 16 of figure 4-201 the quantity zero was entered into X.) If bit 16 is a ONE, quantity e is entered into X and added to a^2. At actions 9 and 10 quantity ℓ^2 is cycled and the content of the MPCTR (multiply counter, located in the SQG) is decremented from six to five by means of control pulse CTR. The quantity a^2 or the sum $a^2 + e$ is transferred to A and bit position 14 of LP at action 11. (Compare with instant 20 of figure 4-201.) After action 11 the third subtotal (a^3, ℓ^3_{14-12}) is contained in A and bit positions 14 through 12 of LP.

Control pulse ST1 (action 11 of figure 4-206) causes the SQG to execute subinstruction MP1 again if the multiply counter (MPCTR) contains a five, four, three, two, or one. Therefore, MP1 is executed six times. The fifth subtotal (a^5, ℓ^5_{14-10}) is established after the second MP1. The seventh subtotal (a^7, ℓ^7_{14-8}) is established after the third MP1. The ninth subtotal (a^9, ℓ^9_{14-6}) is established after the fourth MP1. The eleventh subtotal $(a^{11}, \ell^{11}_{14-4})$ is established after the fifth MP1, and the thirteenth subtotal $(a^{13}, \ell^{13}_{14-2})$ is established after the sixth MP1. If the MPCTR contains the number zero, control pulse ST1 causes the SQG to execute subinstruction MP3 next.

Figure 4-207 illustrates the execution of subinstruction MP3. Before action 1, register A contains quantity a^{13}, LP contains ℓ^{13}, B still contains e (or $\bar{e}$), U contains $a^{12} + 3$ (or $a^{12} + 0$), Z still contains next address z, and order code 11 is still contained in register SQ. At action 1 of MP3 next address z is entered into S and Y and is incremented by one in the adder. The selection logic gates the location of next instruction f for readout and write-in. At action 2 bit 16 of ℓ^{13} is entered into the SQG. At action 3 register G is cleared, as usual. At action 4 quantity z + 1 is transferred to Z. At action 5 quantity a^{13} is entered into Y. If bit 16 of ℓ^{13} at action 2 is a ZERO, no operation takes place at action 6. If bit 16 is a ONE, quantity e is added to a^{13}. Actions 7 through 9 are very similar to the STMIC: entering, testing, and

restoring f. The additional control pulses, RLP and WA, transfer $\mathcal{f}^{13}$ to A. At action 10 quantity $\mathcal{f}^{13}$ is transferred to LP (and cycled). At action 11 quantity a^{13} or $a^{13} + e$ is shifted and entered into A and bit position 14 of LP as described previously. The final product ($a^{14}, \mathcal{f}^{14}_{14-1}$) is now established. Control pulse NISQ enters the order code (OCN) of the instruction to be executed next into the SQG at action 12.

Before the execution of instruction DV K (Divide by Data at K, Order Code 5 with EXTEND Preceding) is discussed, the principle of division applied should be explained. Figure 4-208 demonstrates the division of binary quantity a = +1011 by e = +1110. Approach 1 shows how the division can be carried out manually in a way commonly used. Since a < e, a binary point has to be set into the quotient first. Then the divided (a) is rewritten, and a ZERO is added as a new lowest order bit. If the new number (absolute value, not quantity) formed (10110) is larger than the number e, e is subtracted from the new number (thereby establishing the first remainder, 100.0) and a ONE is set into the quotient. A ZERO is added as a new lower order bit position of the first remainder to again form a new number (10000). Since the new number is larger than e, e is subtracted again and a second ONE is set into the quotient. Quantity 00.10 is the second remainder. Adding a ZERO to the second remainder leaves a new number (00100) still smaller than e. For this reason a ZERO is set into the quotient, and quantity 0.100 becomes the third remainder. A ZERO is added to the third remainder, but again the new number (01000) is smaller than e. Therefore, a second ZERO is entered into the quotient, and quantity 0.1000 becomes the final remainder. Expressed in decimal numbers, the resulting quotient is 3/4 and the remainder is 1/2.

Approach 2 of figure 4-208 illustrates an operation which can be performed more easily by a computer than by the mental process of comparing the divisor with the various remainders. Sign bit ZERO has been added as bit 5 for dividend a and divisor e. Starting with the divide operation (a ÷ e), the dividend is cycled one position to the left, which is the same as adding a ZERO as a new lowest order bit. The complement of the divisor ($\bar{e}$) is added to the new number to obtain the first remainder (r^1). The cross-out numbers indicate the end around carry operation. If bit 5 of r^1 is a ZERO (indicating that r^1 is still positive), as in the example, a ONE is entered into the quotient. Then r^1 is cycled, $\bar{e}$ is added again, and another ONE is entered into the quotient because the second remainder (r^2) also contains a ZERO in bit position 5. At the next instant, r^2 is cycled, and $\bar{e}$ is added again. The third remainder (r^3) contains a ONE in bit position 5, which indicates that the last remainder was too small for a correct subtraction. Consequently, a ZERO is entered into the quotient, and r^2 (the last correct remainder) is cycled again. Number $\bar{e}$ is added once more, and remainder r^4 is also incorrect. A second ONE is set into the quotient and r^2 shifted twice ($\overrightarrow{\overrightarrow{r^2}}$) is taken as the final remainder (R). Setting a ONE into the quotient, if bit 5 of the last remainder contains a ZERO, or setting a ZERO, if bit 5 contains a ONE, leads to an error whenever a remainder happens to be a minus zero (11111). This is demonstrated by the example 01001 ÷ 01100, where the second remainder is minus zero, but a ONE has to be entered into the quotient since the remainder is not smaller than zero. A remainder is incorrect only if it is smaller than zero (either plus zero or minus zero).

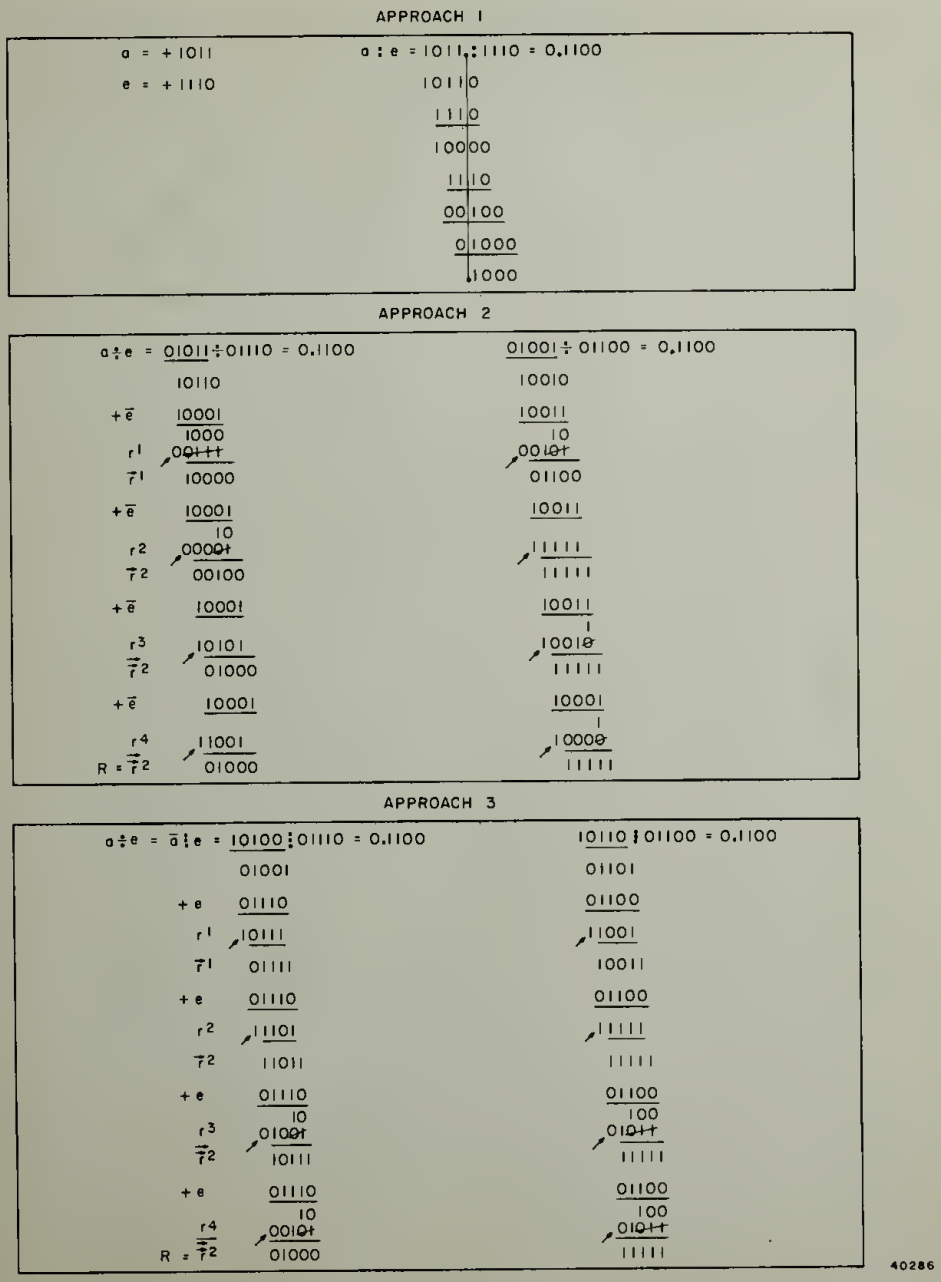

Figure 4-208. Division of Binary Numbers, Principle of Operation

Approach 3 of figure 4-208 is free of the possibility for errors described in approach 2. Instead of dividing a by e, the complement of a is used for cycling, and e is added to the various remainders. This operation is indicated by three points (⋮). Starting with the operation $\bar{a}$ ⋮ e, quantity $\bar{a}$ is cycled and e is added. Because remainder r^1 contains a ONE, a ONE has to be entered into the quotient. Whenever a remainder contains a ZERO (as for r^3 and r^4), a ZERO is to be set into the quotient. The second example of approach 3 proves that this approach is also correct if a remainder becomes minus zero. Approach 3 needs only the highest order bit of a remainder to decide a bit of the quotient and is relatively simple to instrument. Approach 3 is instrumented for the AGC. Although the AGC uses two sign bits (SG and US) instead of one, this does not matter, as can be proved by performing 110100 ⋮ 001110.

Figure 4-209 illustrates the method of operation for the divide instruction and is similar to figures 4-200 and 4-201. At instant 1 the complement of dividend a is entered into Q. After instant 2 a positive quantity is stored in LP for later use if the quotient is to be positive, or a negative quantity is stored in LP if the quotient is to be negative. At instant 3 a ONE is entered in bit position 1 of B. The content of B will be cycled to the left several times during the operation. When the ONE entered at instant 3 moves into the highest bit position, this indicates that the divide operation has been completed. At instants 4 and 5 the quantity contained in Q is cycled one position to the left, returned to Q, and entered into Y. At the same time, a ONE (minus sign) is entered into bit position 6 of Q and Y to correct the cycle operation. (The CYL operation of the computer transfers the ZERO contained in bit position 4 to positions 5 and 6. The ONE entered into position 6 by a special control pulse has the same effect as transferring the ONE at position 5 to position 6.) At instant 6 divisor e is entered into X and added to the quantity which was entered into Y. The sum is available at U at instant 7. Bit position 6 of U contains a ONE; therefore, as described for approach 3, the first remainder is correct, and the actions taken next are as shown for instants 8 and 9. The first remainder is transferred from U to Q for later use. The content of B is cycled to the left one place, and a ZERO is written into the quotient, which is stored in complemented form in the bit positions following the ONE set into B at instant 3. Instants 10 through 15 are repetitions of instants 4 through 9. Bit position 6 of U contained a ONE at instant 13 which indicates that the second remainder is also correct. Instants 16 through 19 are identical in their actions to instants 10 through 13 and 4 through 7, but bit 16 of U now contains a ZERO. The ZERO indicates that the third remainder is incorrect. For this reason the content of Q (the last remainder cycled) is not replaced by the new remainder and a ONE is entered into B as its content is cycled. Instants 21 through 25 are a repetition of instants 16 through 20 because bit 6 of the fourth remainder is also a ZERO. As the content of B is cycled the fourth time, the ONE set at instant 3 now moves into bit positions 5 and 6, and this indicates that the divide operation is complete. At instant 26 the content of B is complemented to become the final quotient and is transferred to A. Q contains the complemented quantity of the absolute value of the final remainder. For the given example the final remainder contained in Q is 1000 but becomes 0.1000 when the binary point is set. The instruction DV K is now described.

INSTANT	FUNCTION	REGISTERS O,Y,X,U						REGISTERS LP,B						
		6	5	4	3	2	1	6	5	4	3	2	1	
1	$\overline{a} \rightarrow$ O	1	1	0	1	0	0							
2	00010 → LP							0	0	0	0	0	1	
3	00001 → B							0	0	0	0	0	1	
4	100000 V O → O	1	0	1	0	0	1							
5	→ Y	1	0	1	0	0	1							
6	e → X	0	0	1	1	1	0							
7	U	$\underline{1}$	1	0	1	1	1							r^1
8	U → O	1	1	0	1	1	1							
9	$\overleftarrow{B} \rightarrow$ B							$\underline{0}$	0	0	0	1	0	
10	100000 V O → O	1	0	1	1	1	1							
11	→ Y	1	0	1	1	1	1							
12	e → X	0	0	1	1	1	0							
13	U	$\underline{1}$	1	1	1	0	1							r^2
14	U → O	1	1	1	1	0	1							
15	$\overleftarrow{B} \rightarrow$ B							$\underline{0}$	0	0	1	0	0	
16	100000 V O → O	1	1	1	0	1	1							
17	→ Y	1	1	1	0	1	1							
18	e → X	0	0	1	1	1	0							
19	U	$\underline{0}$	0	1	0	1	0							r^3
20	$\overleftarrow{100000 \text{ V } B} \rightarrow$ B							$\underline{0}$	0	1	0	0	1	
21	100000 V O → O	1	1	0	1	1	1							
22	→ Y	1	1	0	1	1	1							
23	e → X	0	0	1	1	1	0							
24	U	$\underline{0}$	0	0	1	1	0							r^4
25	$\overleftarrow{100000 \text{ V } B} \rightarrow$ B							$\underline{1}$	1	0	0	1	1	$\overline{\text{QUOTIENT}}$
26	$\overline{B} \rightarrow$ A							0	0	1	1	0	0	QUOTIENT

ALL NUMBERS ARE WRITTEN IN BINARY FORM
V MEANS OR _ MEANS USED FOR TEST

40287

Figure 4-209. Division of Binary Numbers, Method of Operation

DV K means: divide the content of the accumulator (A) by the quantity located at K. K may be any legal address. The entire operation DV K (for $0020 \leq K$) can be formulated as follows:

(1) Set $c(A) = b(A) \div c(K)$ for $|b(A)| < |c(K)|$ No overflow or underflow is allowed for b(A).
Set $c(Q) = |\overline{R}|$ (complemented quantity of the absolute value of the remainder).
Set $c(LP) > 0$, if quotient is positive.
Set $c(LP) < 0$, if quotient is negative.
If $|b(A)| = |c(K)|$, then $|c(A)| = 37777$ and $c(Q) = -|c(K)|$.
If $|b(A)| > |c(K)|$, then $|c(A)| = 37777$ and c(Q) is meaningless.

(2) Restore c(K) - b(K), if $K \leq 1777$, except for K = 0000, 0001, or 0003.

(3) Execute the instruction located at $z = L + 1$ next.

Dividing requires the execution of instruction NDX, subinstruction DV0 once, DV1 fourteen times, and STD2 once. Instruction DV K is the only regular instruction (except TC) which uses register Q. Therefore, any program portion following a TC instruction and including a DV instruction must preserve the return address (normally contained in Q) somewhere else.

Figures 4-210 through 4-215 illustrate the execution of DV 1125. Quantity a, contained in the accumulator (A), is to be divided by quantity e, located at 1125. The entire code of the instruction was entered into B during the execution of the preceding NDX instruction (B now contains b - 121125), and order code 12 was entered into SQ. At action 1 of subinstruction DV0 (figures 4-210 through 4-213) the address contained in B is transferred to S and the selection logic gates location 1125 for readout and write-in. At action 2 register G is cleared, dividend a is transferred to B, and the sign bit of a is entered into the SQG by means of pulse TSGN. At action 3 no transfer takes place unless the address in S is smaller than 0020. If $c(S) \leq 0017$, control pulse RSC reads the selected flip-flop register into G.

If the sign of dividend a was found (at action 2) to be positive (figures 4-210 and 4-211), quantity $\bar{a}$ is written from C into A at action 4 and transferred to Q at action 6. At action 5 the quantity 000001 is transferred (and cycled) into LP and becomes 140000. At action 7 divisor e is entered into B and P, and bit 16 of e is entered into the SQG. At action 8 the divisor is transferred to A, an alarm is caused in case of incorrect parity, and a new parity bit of e is entered into G. If the sign of divisor e was found (at action 7) to be positive (figure 4-212), the quantity located at LP and the quantity 00002 are written simultaneously (OR'ed) into B, which contains 140002 after action 9. The quantity 140002 is transferred to LP at action 10 and becomes 000001, an indication that the quotient has to be positive. (Compare with instant 2 of figure 4-209.) At action 11 a ONE is entered into bit position 1 of B (as in figure 4-209) and used for shift counting. Control pulse ST1 causes the SQG to execute subinstruction DV1 next.

If the sign of divisor e was found (at action 7) to be negative (figure 4-211), no operation is performed at action 9, and at action 10 quantity $\bar{e}$ is transferred from C

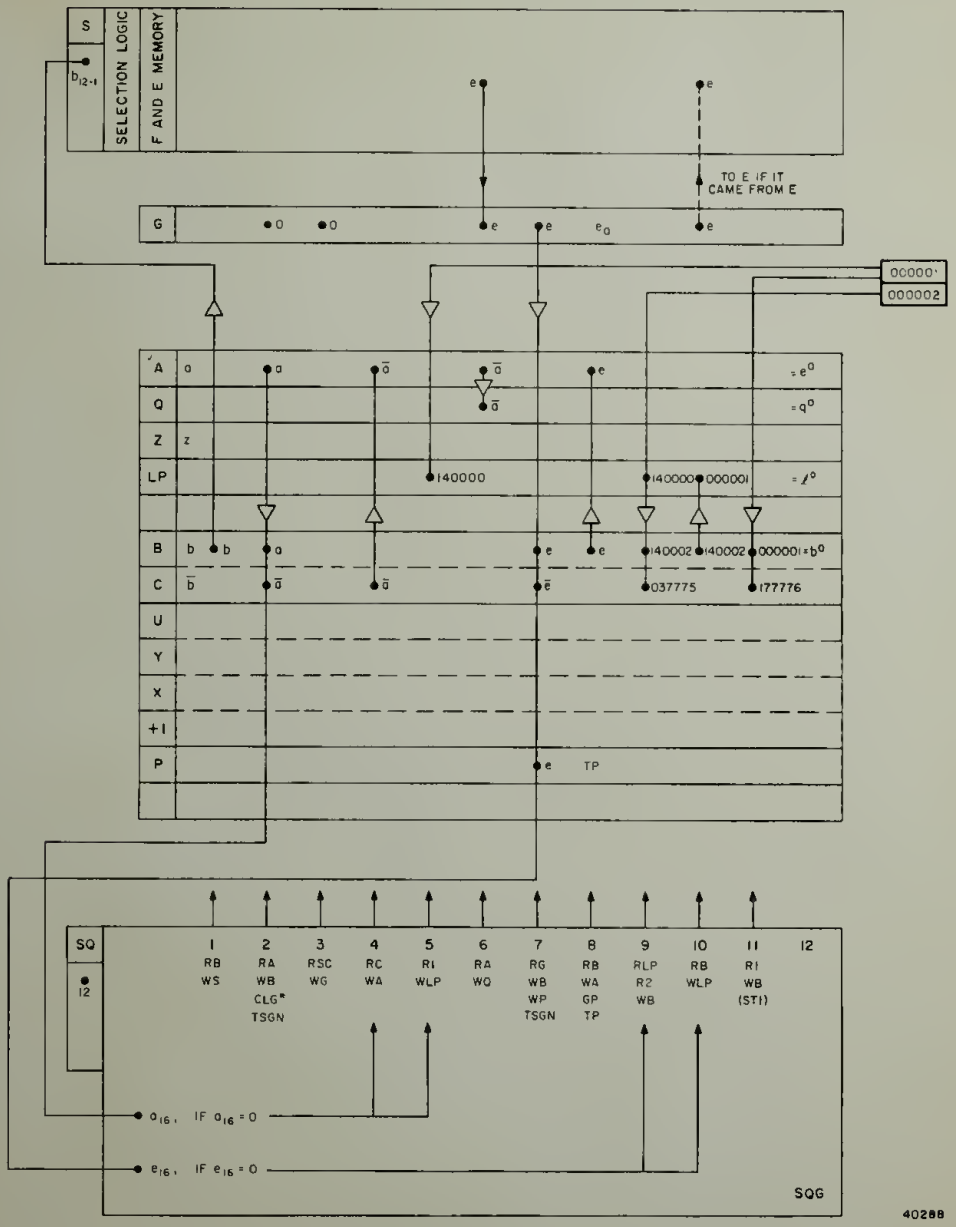

Figure 4-210. Subinstruction DV0 (a and e Positive)

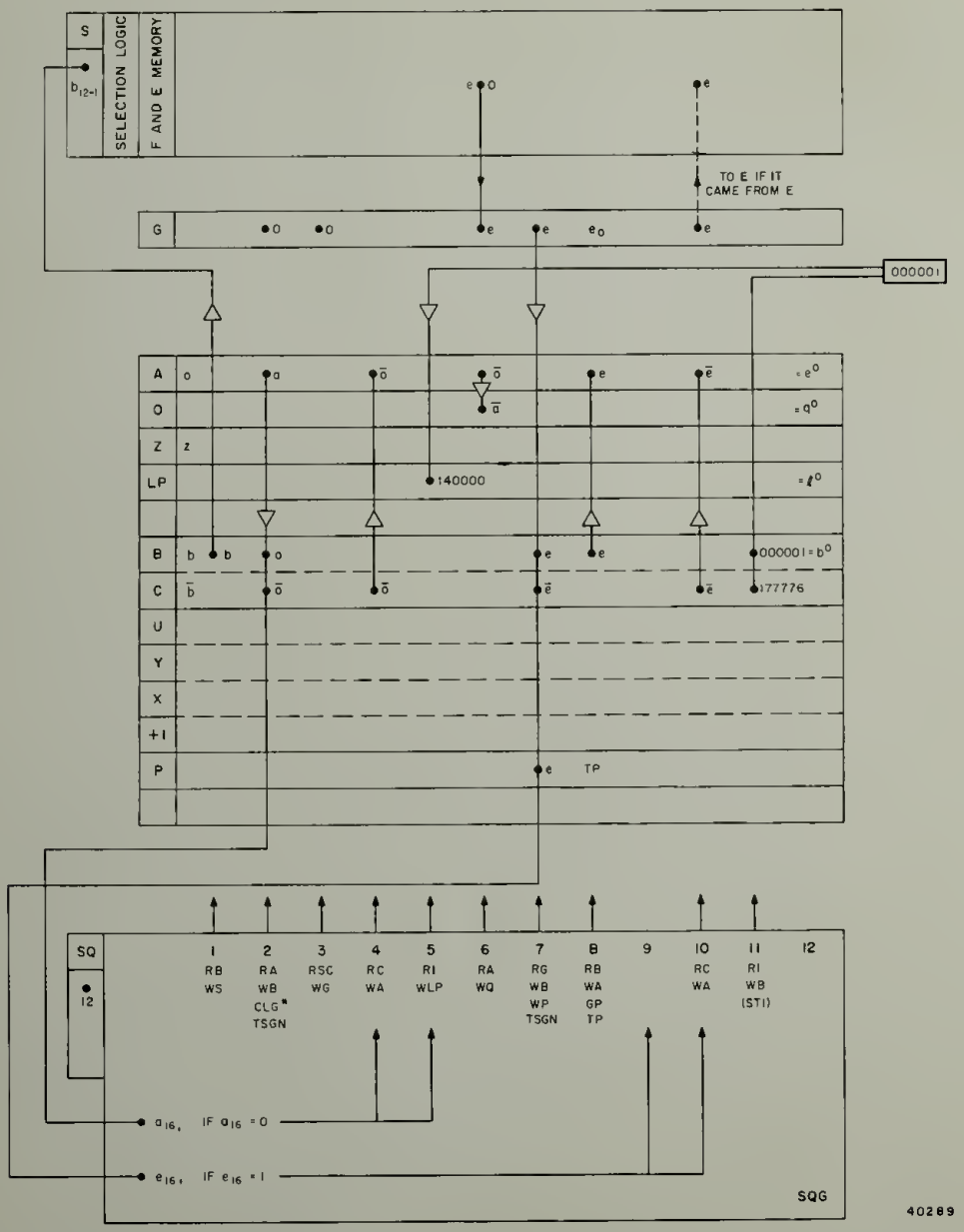

Figure 4-211. Subinstruction DV0 (a Positive and e Negative)

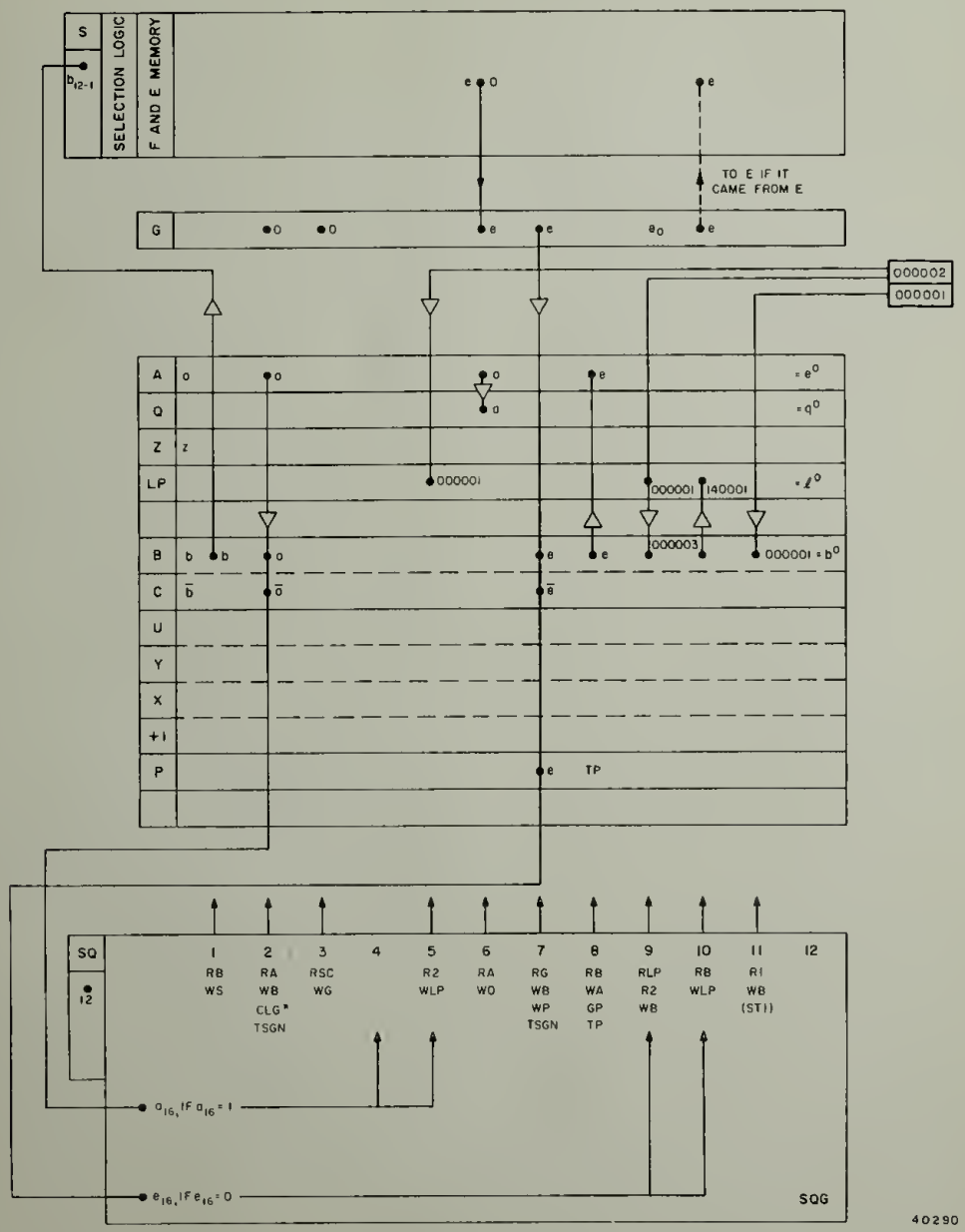

Figure 4-212. Subinstruction DV0 (a Negative and e Positive)

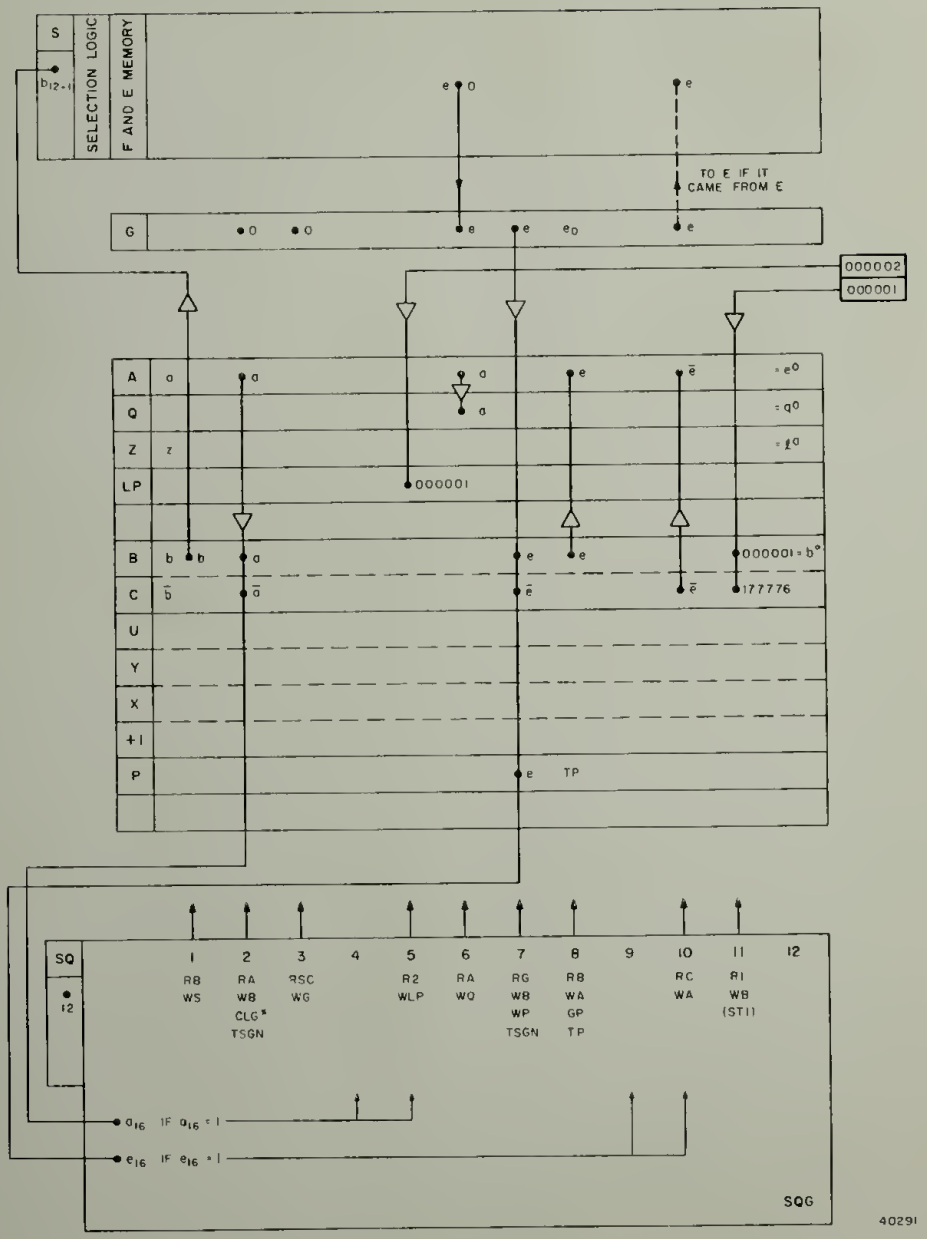

Figure 4-213. Subinstruction DV0 (a and e Negative)

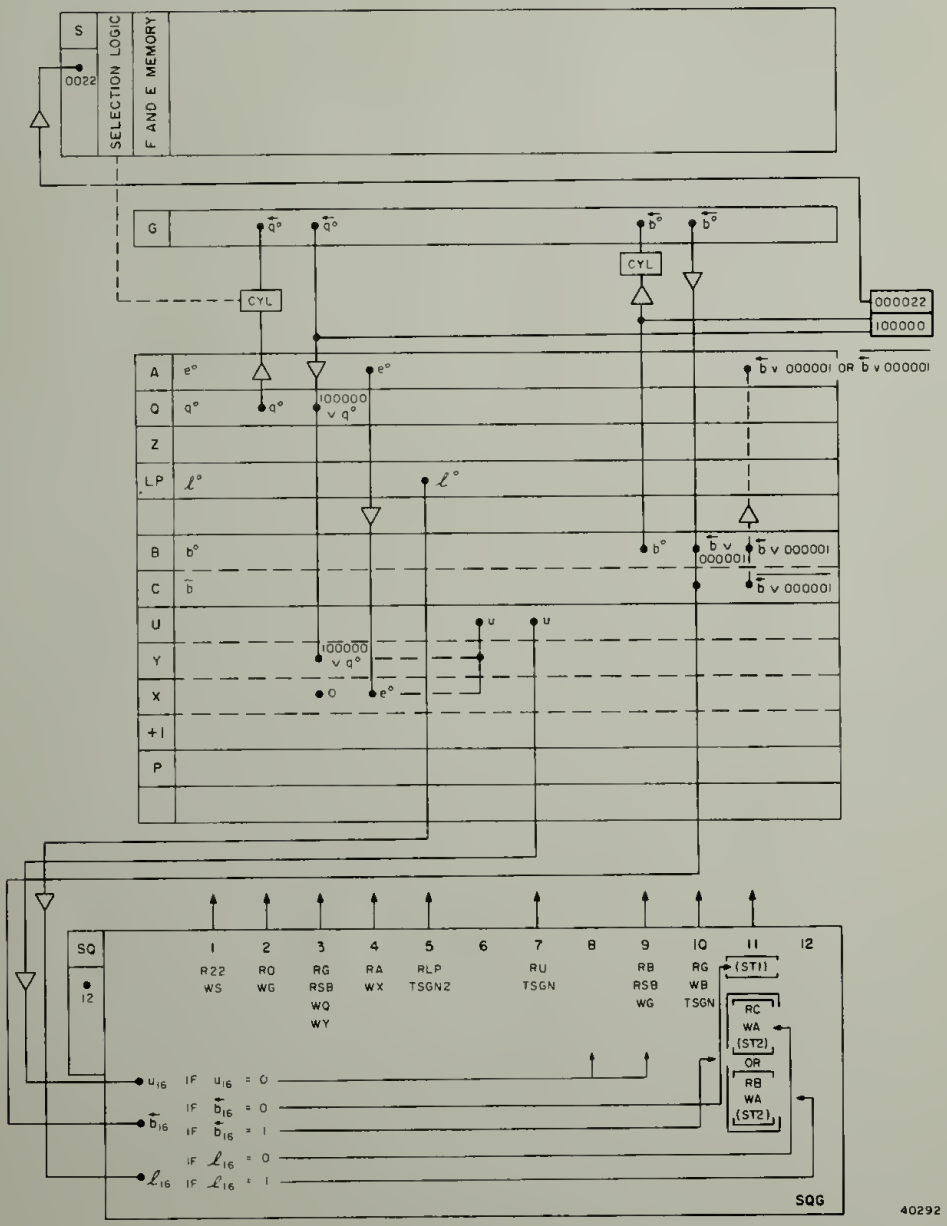

Figure 4-214. Subinstruction DV1 (Incorrect Remainder)

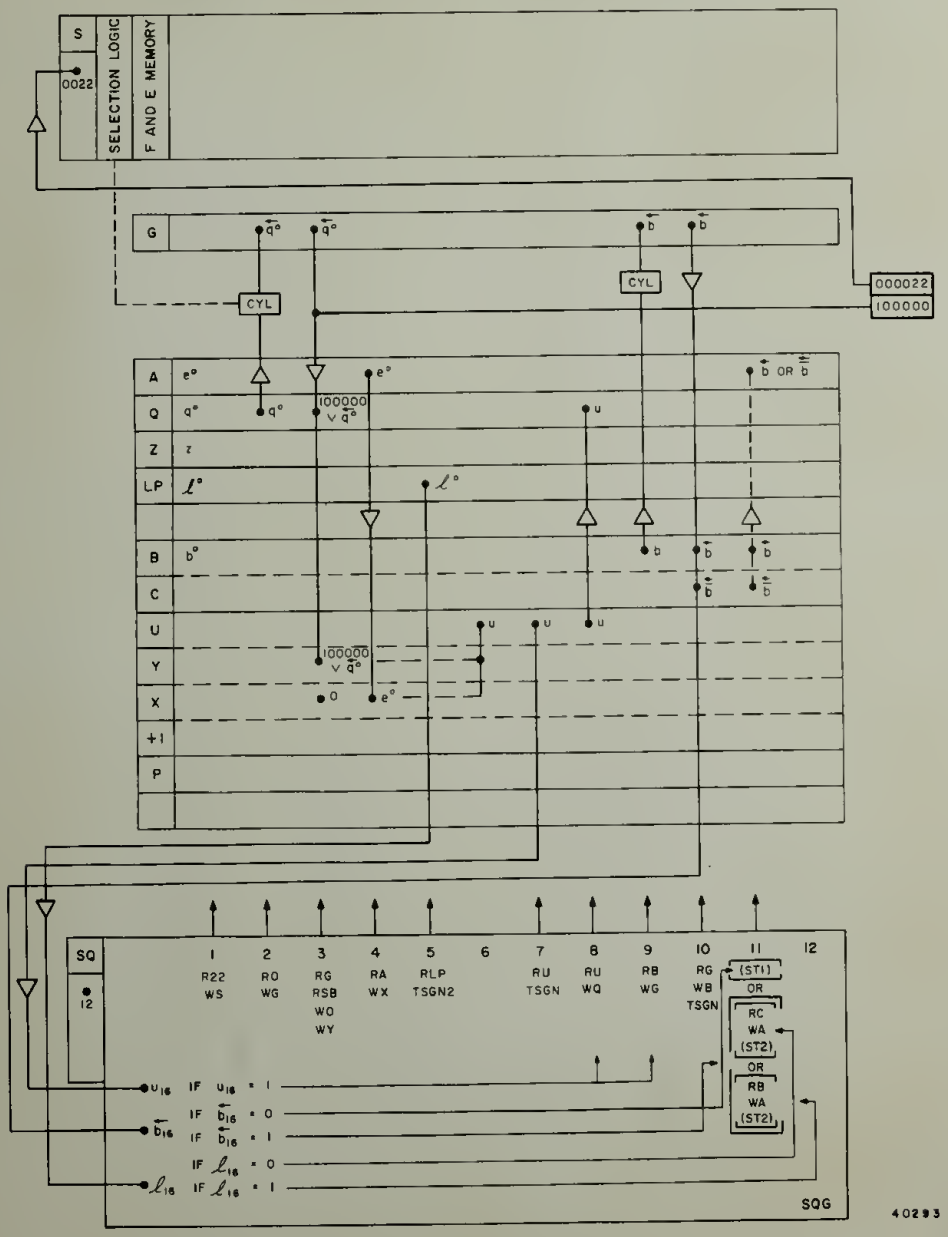

Figure 4-215. Subinstruction DV1 (Correct Remainder)

to A. Register LP still contains 140000, an indication that the quotient is to be negative. Action 11 of figure 4-211 is identical to action 11 of figure 4-210.

If the sign of dividend a was found (at action 2) to be negative (figures 4-212 and 4-213), a is still in A at action 4, and the quantity 000001 is written into LP at action 5. At action 6 dividend a is transferred to Q. The effects of actions 7 and 8 in figures 4-210 through 4-213 are identical. If the sign of the divisor was found (at action 7) to be positive (figure 4-213), the quantity located at LP and the quantity 000002 are written simultaneously into B which contains 000003 after action 9. The quantity 000003 is transferred to LP at action 10 and becomes 140001, an indication that the quotient has to be negative. The effect of action 11 is identical for figures 4-210 through 4-213.

If the sign of divisor e was found (at action 7) to be negative (figure 4-213), the effect of actions 9 and 10 is identical to that indicated in figure 4-211. Register LP still contains 000001, an indication that the quotient has to be positive. The contents of registers A, Q, LP, and B after the execution of DV0 are renamed as listed in table 4-XXIV.

Figures 4-214 and 4-215 illustrate the first execution of subinstruction DV1. At action 1 address 0022 is entered into register S and the selection logic sets the switch in front of register G so that any word transferred from the write amplifiers to register G is cycled one position to the left, as indicated by CYL and the dotted line. At action 2 quantity q^0 is cycled one position to the left and entered into G. At action 3 the content of G is transferred to Q and Y simultaneously with a ONE which is entered (OR'ed) into position 16 of Q and Y (similar to instants 4 and 5 of figure 4-209). At action 4 quantity e^0 is entered into X (as at instant 6 of figure 4-209) and the sum $u = (100000 \vee q^0) + e^0$ becomes available at U. At action 5, bit 16 of quantity 1 is entered into the SQG for later use. At action 7, bit 16 of quantity u is entered into the SQG. If bit 16 of u is a ZERO (figure 4-214), no operation is performed at action 8. At actions 9 and 10 quantities b^0 and 100000 are cycled simultaneously (OR'ed) and entered into B (as at instants 20 and 25 of figure 4-209), and the new bit 16 ($\overleftarrow{b_{16}}$) is also entered into the SQG. If bit 16 of u is a ONE (figure 4-215), quantity u is transferred to Q (as at instants 8 and 14 of figure 4-209). At actions 9 and 10 only quantity b^0 is cycled and its new bit 16 entered into the SQG. Action 11 depends on bit 16 of b (entered into the SQG at action 10) and on bit 16 of 1 (entered at action 5). If $\overleftarrow{b_{16}} = 0$, which indicates that the division operation has not been completed yet (as at instants 9, 15, and 20 of figure 4-209), control pulse TS1 is generated in order to execute subinstruction DV1 again. The contents of registers Q and B after the first execution of DV1 may be called q^1 and b^1; after the second execution, q^2 and b^2; etc. After fourteen executions of DV1, quantity b^{14} will contain a ONE in bit position 16 (indicating that the division operation has been completed at instant 25) and control pulse ST2 causes the SQG to execute subinstruction STD2 next. When DV1 is executed the final time, the quotient has to be transferred from C to A if $l_{16}^{14} = 0$ or from B to A if $l_{16}^{14} = 1$. Subinstruction STD2, executed right after the final DV1 subinstruction, increments next address z by one and initiates the execution of the subsequent instruction.

Table 4-XXIV. Contents of Registers At End of DV0

INITIAL CONDITIONS	c(A) = e°	c(Q) = q°	c(LP) = ℓ°	c(B) = b°	c(Z)
a POSITIVE e POSITIVE	e	$\bar{a}$	000001	000001	z
a POSITIVE e NEGATIVE	$\bar{e}$	$\bar{a}$	140000	000001	z
a NEGATIVE e POSITIVE	e	a	140001	000001	z
a NEGATIVE e NEGATIVE	$\bar{e}$	a	000001	000001	z

0695

4-8.8.1.3 Special Cases of Regular Instructions. The preceding paragraphs deal with normal cases; i.e., instructions in which relevant address K refers to a location in the F or E memory. Instructions in which address K refers to flip-flop registers A, Q, Z, or LP, together with other special cases of NDX K instructions, are discussed in the following paragraphs. For selection of the addressed flip-flop register and the operation of subinstruction STD2, see figure 4-184.

The special cases of instruction TC K are:

(1) TC A = XAQ, which means: execute the instruction contained in A using Q.

If c(A) = 000000, this is a program trap.

If A contains a TC K instruction, the transfer of control will be executed.

If A contains an instruction other than TC K, the instruction contained in Q will be executed after the instruction contained in A.

(2) TC Q = RETURN, which means: return program control to the instruction entered into Q at the time the last TC K instruction was executed. Normally, Q contains a TC K instruction. (After the execution of this TC K instruction, Q contains TC Z.) If Q contains an instruction other than TC K, then TC Q is not a useful operation.

(3) TC Z, which is not a useful operation.

(4) TC LP, which transfers control to LP, $c(LP) = b^e(LP)$.

The special cases of instruction XCH K are:

(1) XCH A = NOOP; the instruction to be executed next is taken from L + 1, but c(Q) is preserved. TC L + 1 is faster but changes c(Q).

(2) XCH Z, which transfers program control to the instruction which is located at the address contained in A, similar to TS Z = TCAA.

(3) XCH Q, which replaces the return address.

(4) XCH LP, which results in $c(LP) = b^e(A)$.

The special cases of instruction CS K are:

(1) CS A = COM, which means: complement contents of A, $c(A) = \bar{b}(A)$.

(2) CS Q, which results in $c(A) = \bar{b}(Q)$ and $c(Q) = b(Q)$.

(3) CS Z, which results in $c(A) = \bar{b}(Z)$ and $c(Z) = b(Z) + 1$.

(4) CS LP, which results in $c(A) = \bar{b}(LP)$ and $c(LP) = b^e(LP)$.

The special cases of instruction TS K are:

(1) TS A = OVSK, which means: overflow skip. If A contains no overflow or underflow, the instruction at z = L + 1 is executed next. If A contains overflow or underflow, the instruction at L + 2 is executed next. TS A is very useful when used before an XCH instruction is executed, in order to prevent loss of an overflow bit.

(2) TS Q, which enters new return address.

(3) TS Z = TCAA, which means: transfer program control to the instruction which is located at the address stored in A. Q does not contain the same return address which would be entered by a TC K instruction. The first TC K instruction following a TCAA must not be a subroutine call, unless Z contains a TC K instruction. In this case, XAQ (TC A) is as fast and preferred, unless it is desired to save c(Q).

(4) TS LP, which results in $c(LP) = b^e(A)$.

The special cases of instruction MSK K are:

(1) MSK A = NOOP (no operation).

(2) MSK Q, which results in c(Q) = b(A) AND c(Q) and c(Q) = b(Q).

(3) MSK Z, which results in c(A) = b(A) AND b(Z) and c(Z) = b(Z) + 1. This is is not a useful operation.

(4) MSK LP, which results in c(A) = b(A) AND b(LP) and c(LP) = b(LP). (No editing of b(LP) occurs.)

The special cases of instruction AD K are:

(1) AD A = DOUBLE, which results in c(A) = 2b(A). In case of overflow or underflow, OVCTR is incremented or decremented.

(2) AD Q, which results in c(A) = b(A) + c(Q) and c(A) = b(Q).

(3) AD Z, which results in c(A) = b(A) + b(Z) and c(Z) = b(Z) + 1.

(4) AD LP, which results in c(A) = b(A) + b(LP) and $c(LP) = b^e(LP)$.

The special cases of instruction NDX K are:

(1) NDX A, which results in c(B) = c(z) + c(A) with z = L + 1; c(A) = b(A). Register B contains the instruction executed next.

(2) NDX Q, which results in c(B) = c(z) + c(Q) with z = L + 1; C(Q) = b(Q).

(3) NDX Z, which results in c(B) = 2b(Z) + 1 with z = L + 1; c(Z) = b(Z) + 1.

(4) NDX LP, which results in c(B) = c(z) + b(LP) with z = L + 1; c(LP) = b^e(LP).

(5) NDX 5777 - EXTEND, which was explained previously.

(6) NDX 0025 - RESUME, which is an involuntary instruction.

(7) NDX 0017 - INHINT, which was explained previously.

(8) NDX 0016 - RELINT, which was explained previously.

The special cases of instruction CCS K are:

(1) CCS A, which is very useful and very similar to CCS K.

(2) CCS Q and CCS LP, which might be useful; CCS Z is not a useful operation.

The special cases of instruction SU K are:

(1) SU A, which puts 177777 into A; to do this requires 4 MCT's.

(2) SU Q, SU Z, and SU LP, which are similar to AD Q, and AD LP except that complemented quantities are added.

The special cases of instruction MP K are:

(1) MP A - SQUARE, which results in c(A, LP) = $|b(A)|^2$.

(2) MP Q, which results in c(A, LP) = b(A) · c(Q) and c(Q) = b(Q).

(3) MP Z, which results in c(A, LP) = b(A) · b(Z) and c(Z) = b(Z) + 1. This is not a useful operation.

(4) MP LP, which results in c(A, LP) = b(A) · c(LP) = b(LP).

The special cases of instruction DV K are:

(1) DV A, which puts 037777 into A; to do this requires 18 MCT's. This is a useful test loop.

(2) DV Q, which results in c(A) = b(A) ÷ b(Q) and c(Q) = $|\overline{R1}|$.

(3) DV Z, which results in c(A) = b(A) ÷ b(Z), c(Z) = b(Z) + 1. This is not a useful operation.

(4) DV LP, which results in c(A) = b(A) ÷ c(LP) and c(Q) = $|\overline{R1}|$.

4-8.8.2 Involuntary Instructions. Involuntary instructions are divided into interrupt instructions and counter instructions. Involuntary instructions do not obtain order codes from the central processor; they are initiated by program interrupt and resume condition signals and by counter instruction commands generated by priority control. Resume conditions are detected by the SQG when an interrupting program is finished. Order and subinstruction codes for the two interrupt involuntary instructions are generated within the SQG. These are the interrupt and resume instructions that allow an interrupting program to be executed. The counter instruction commands from priority control inhibit program executions and initiate the counter instructions. There are four counter instructions: increment, decrement, shift, and shift and add one. The counter instruction commands control the sequence generator outputs and also prevent the stored order and subinstruction codes from affecting sequence generator outputs. Therefore, the counter instructions do not require order and subinstruction codes.

The interrupt instruction accomplishes transfer operations necessary to initiate an interrupt program. Instruction information and computation results of the current program are stored so that later the current program can be resumed at the point of interruption. Also, the address of the first instruction word of the interrupt program is brought into the central processor.

The resume instruction occurs at the end of an interrupting program. This instruction restores the instruction information and computation results. Execution of the interrupted program is then resumed.

The counter instructions are initiated in the counter priority control circuits which also supply the address of the applicable counter to the central processor. A counter word is then brought into the central processor, and the counter operation is performed. The increment instruction adds one to the counter word; the decrement instruction subtracts one from the counter word; the shift instruction shifts the contents one place to the left; and the shift and add one instruction shifts the contents one place to the left and adds one. The shift instructions accomplish serial-to-parallel conversions of inputs to the AGC.

Certain inputs to the AGC are connected both to the IN registers and to the priority control circuits. At the time a signal arrives at one of these inputs (and no input signal of higher priority is present), priority control signals the SQG to execute instruction RUPT next and provides 2000, 2010, 2014, 2020, or 2024 (called RUPT Transfer Routines, table 4-XXV) for initiating the requested interrupting program. Execution of instruction RUPT causes the last contents of registers Z and B to be transferred to locations 0024 and 0025 in E memory and program control to be transferred to one of five routines. No matter to which of the five routines control is transferred, the contents of A and Q are first transferred to locations 0026 and 0027 in E memory. Thereafter program control is transferred (by a TC instruction) to one of the six interrupt programs, T3RUPT, T4RUPT, KEYRUPT, UPRUPT, or DOWNRUPT. Each interrupting program has the responsibility of returning the contents of locations 0026 and 0027 to registers A and Q and of initiating instruction RSM. Execution of instruction RSM causes the contents of locations 0024 and 0025 to be transferred to Z and B and causes the execution of the interrupted program to continue.

A program interruption (execution of RUPT) may occur at the end of any instruction (not subinstruction) except when:

(1) An interrupting program is in progress.

(2) A program interruption has been inhibited by the execution of instruction INHINT (NDX 0017) and the inhibition has not been released by the execution of instruction RELINT (NDX 0016). By executing INHINT and RELINT, the selection logic gates interrupt priority control to prevent it or allow it to send a command to the SQG.

(3) The next instruction to be executed is an extra code instruction. In this case, register B contains a quantity with underflow, and control pulse WOVI at action 11 of subinstruction NDX1 prevents an interruption.

Table 4-XXV. RUPT Transfer Routines

Location	Content	Routine	Order Code	Relevant Address
2000	5 0026 0	WAITLIST	TS	ARUPT
2001	3 0001 0		XCH	Q
2002	3 0027 1		XCH	QRUPT
2003	0 4071 0		TC	T3RUPT
2010	5 0026 0	DISPLAY	TS	ARUPT
2011	3 0001 0		XCH	Q
2012	3 0027 1		XCH	QRUPT
2013	0 2427 1		TC	T4RUPT
2014	5 0026 0	KEYRUPT	TS	ARUPT
2015	3 0001 0		XCH	Q
2016	3 0027 1		XCH	QRUPT
2017	0 2467 0		TC	KEYRUPT
2020	5 0026 0	UPLINK	TS	ARUPT
2021	3 0001 0		XCH	Q
2022	3 0027 1		XCH	QRUPT
2023	0 2300 0		TC	UPRUPT
2024	5 0026 0	DKEND	TS	ARUPT
2025	3 0001 0		XCH	Q
2026	3 0027 1		XCH	QRUPT
2027	0 2301 1		TC	DOWNRUPT

(4) The accumulator (A) contains a quantity with overflow or underflow. In this case, control pulse WOVI is normally provided at action 4, 10, or 11 to prevent program interruption.

All incremental input signals of the AGC are first stored in the counter priority control circuits. At the time the incremental data arrive (and if no incremental data of higher priority are present), counter priority control provides the address of the proper counter and sends a signal to the SQG to execute instruction PINC, MINC, SHINC, or SHANC next. Dependent on the counter address provided, the increment or decrement is carried out with or without correction in case of overflow or underflow. Instructions PINC, MINC, SHINC, and SHANC can be executed after any action 12.

4-8.8.2.1 Instruction RUPT (Interrupt Program). Instruction RUPT means: transfer control to the interrupting program and store enough information of the interrupted program in order to continue it later. The entire operation RUPT can be formulated as follows:

(1) Set c(ZRUPT) = b(Z)
(2) Set c(BRUPT) = b(B)

} Remember that bit 15 of b(Z) and b(B) is lost, and bit 16 is moved into position 15 of ZRUPT AND BRUPT, respectively.

(3) Execute next the instruction located at the address provided by interrupt priority control.

(4) Inhibit interrupt until further notice. (This is established by setting the interrupt-in-progress flip-flop in the SQG.)

(5) Reset interrupt priority control.

Instruction RUPT consists of three subinstructions: RUPT1, RUPT3, and STD2. Figures 4-216 and 4-217 illustrate the execution of RUPT. The current program is to be interrupted and program ERRUPT is to be executed immediately. At action 1 of RUPT1, address 0024 is entered into S and the selection logic gates location 0024 for write-in. At the same time, address 0024 is also entered into Y and a one is added to it. At action 3, register G is cleared as usual. At action 9, the next address (z) of the program being interrupted is entered into G and transferred to location 0024 (ZRUPT). At action 10, quantity 0025 is entered into Z. Control pulses ST1 and ST2 at action 11 cause the SQG to execute subinstruction RUPT3 next. At action 1 of RUPT3, address 0025 (BRUPT) is entered into S and the selection logic gates location 0025 for write-in. At action 2, the address provided by the priority control circuits (2004) is entered into Z. At action 3, address 2004 is transferred to G and control pulse KRPT clears the request flip-flop (in priority control) that initiated the program interrupt. At action 9, the content of B is entered into G and transferred to location 0025 at action 10. Control pulse ST2 causes the SQG to execute subinstruction STD2 next, in order to increment address 2004, which is now the next address, and to initiate instruction TS ARUPT.

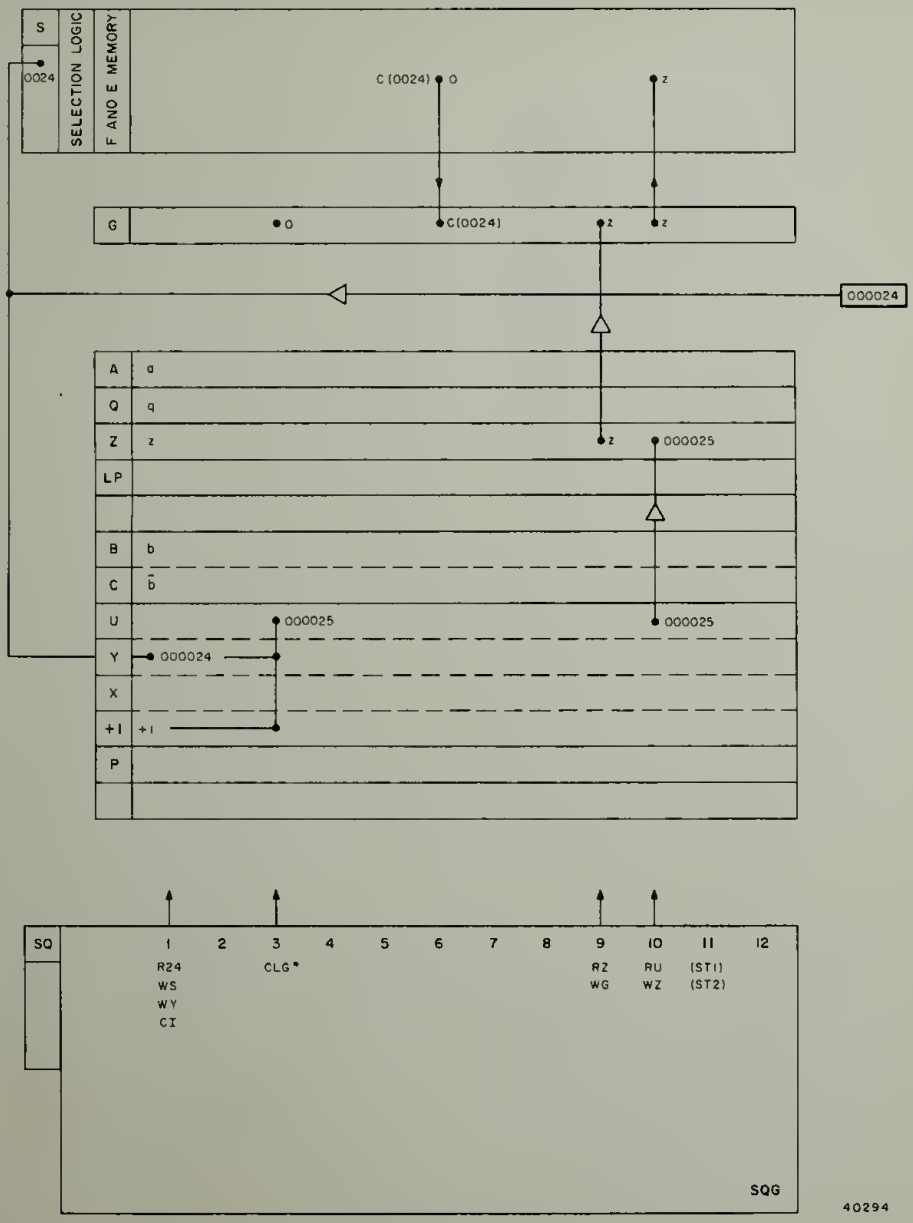

Figure 4-216. Subinstruction RPT1

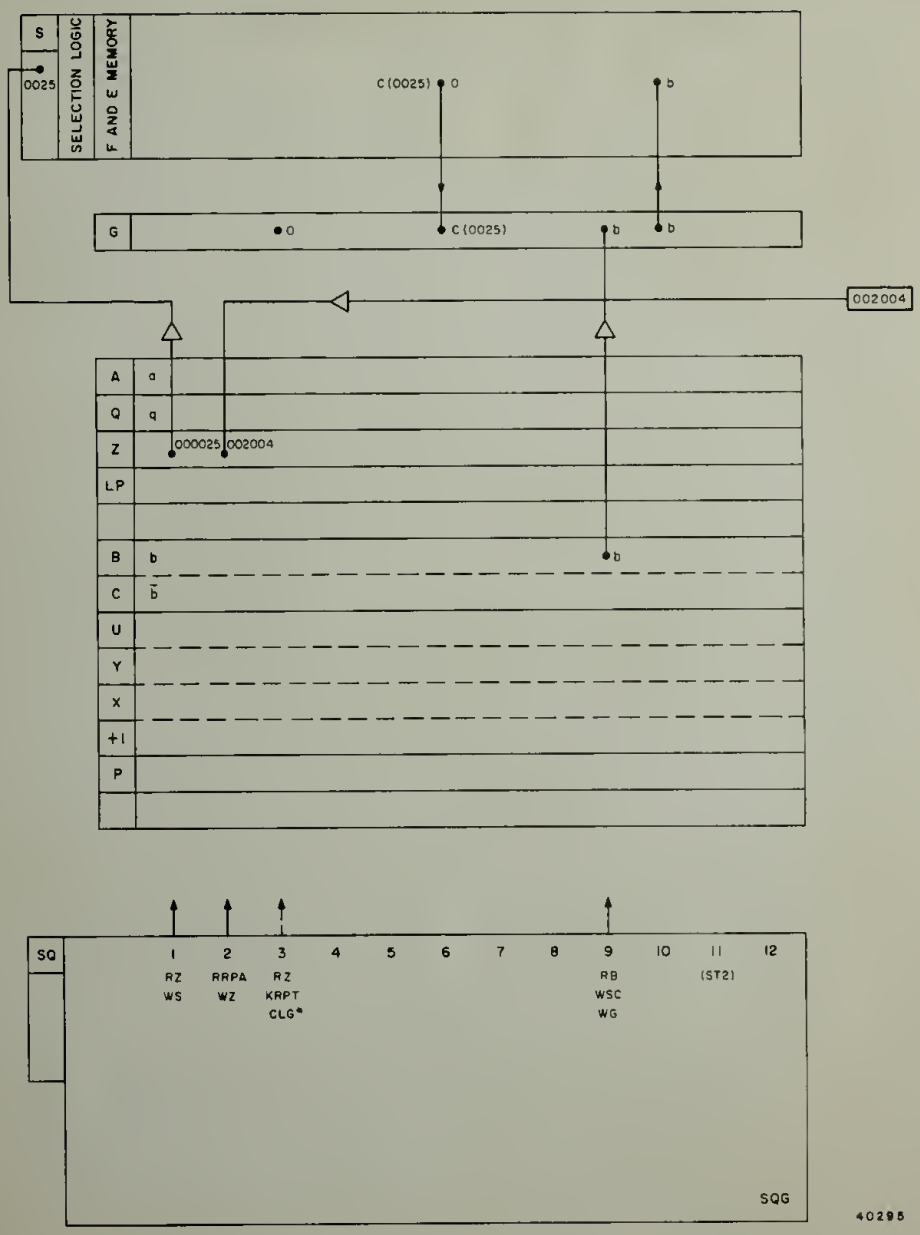

Figure 4-217. Subinstruction RPT3

4-8.8.2.2 Instruction RSM (Resume Program, Order Code 2, K = 0025). Instruction RSM means: resume the interrupted program by entering into B and Z what was contained in B and Z at time of interruption. The entire operation RSM can be formulated as follows:

(1) Set c(B) = c(BRUPT).

(2) Set c(A) = c(ZRUPT).

(3) Execute the instruction now contained in B next.

(4) Release inhibition of program interruption. This is established by the interrupt priority circuit.

Instruction RSM consists of two subinstructions: NDX0 and RSM. Figure 4-218 illustrates the execution of instruction RSM = NDX 0025. As subinstruction NDX0 is executed, the content of location 0025 (the instruction stored away by instruction RUPT) is returned to B. At action 10 control pulse TRSM causes the SQG to execute subinstruction RSM next because c(S) = 0025. At action 1 of RSM, address 0024 is entered into S and the selection logic gates location 0024, containing the next address (z) of the interrupted program, for readout. At action 3 register G is cleared as usual. At action 7 address z is returned to Z. At action 12 the order code (OC) is entered into register SQ and the execution of the instruction contained in B is initiated.

4-8.8.2.3 Instruction PINC (Increment Content of Addressed Counter). Instruction PINC means: increment by one the quantity contained in that counter the address of which is provided by counter priority control. The entire operation of PINC can be formulated as follows:

(1) Enter into S the address provided by counter priority control.

(2) Set c(CTR) = b(CTR) + 000001.

(3) In case of overflow, send the signal to priority control or reverse the sign if CTR = 0047, 0050, 0051, 0052, 0053.

(4) Reset counter priority control.

Instruction PINC consists of only one subinstruction, PINC. Figure 4-219 illustrates the execution of PINC which increments the content of counter 0044. At action 1, address 0044, provided by counter priority control, is entered into register S and the selection logic gates location 0044 for readout and write-in. At action 3 register G is cleared as usual. At action 4 quantity 000001 is entered into Y. At action 6 quantity e of the addressed counter is transferred to X and P. At action 7 an alarm is caused in case of incorrect parity. At action 8 register P is cleared. At action 9 register G is cleared again and the sum e + 1 is written into P. At action 10 control pulse RU* reads the incremented quantity e + 1 into the WA's and control pulse WG* writes the contents of the WA's and the parity bit generated for quantity e + 1 into register G. The complete word $(e + 1)_{15-0}$ is returned to location 0044 at

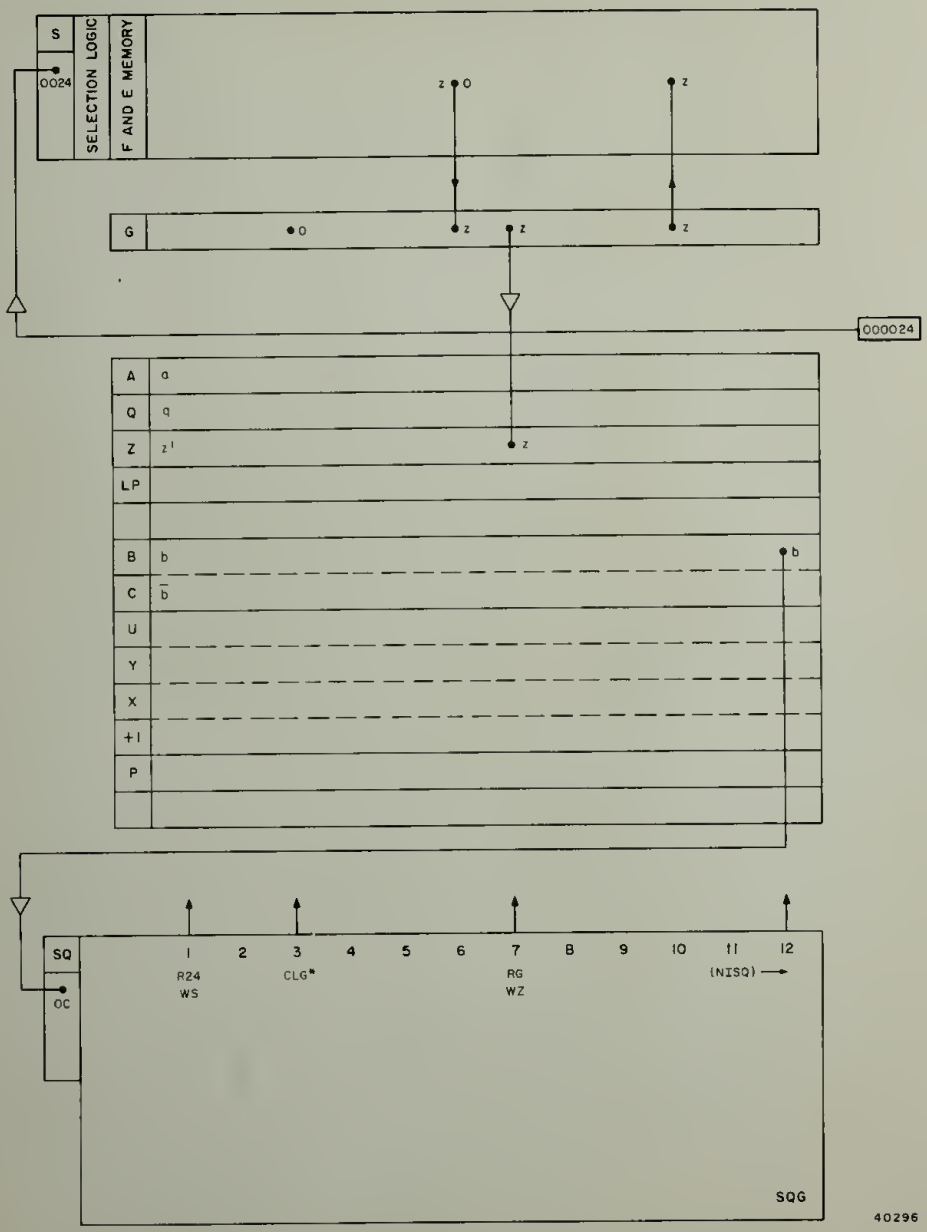

Figure 4-218. Subinstruction RSM

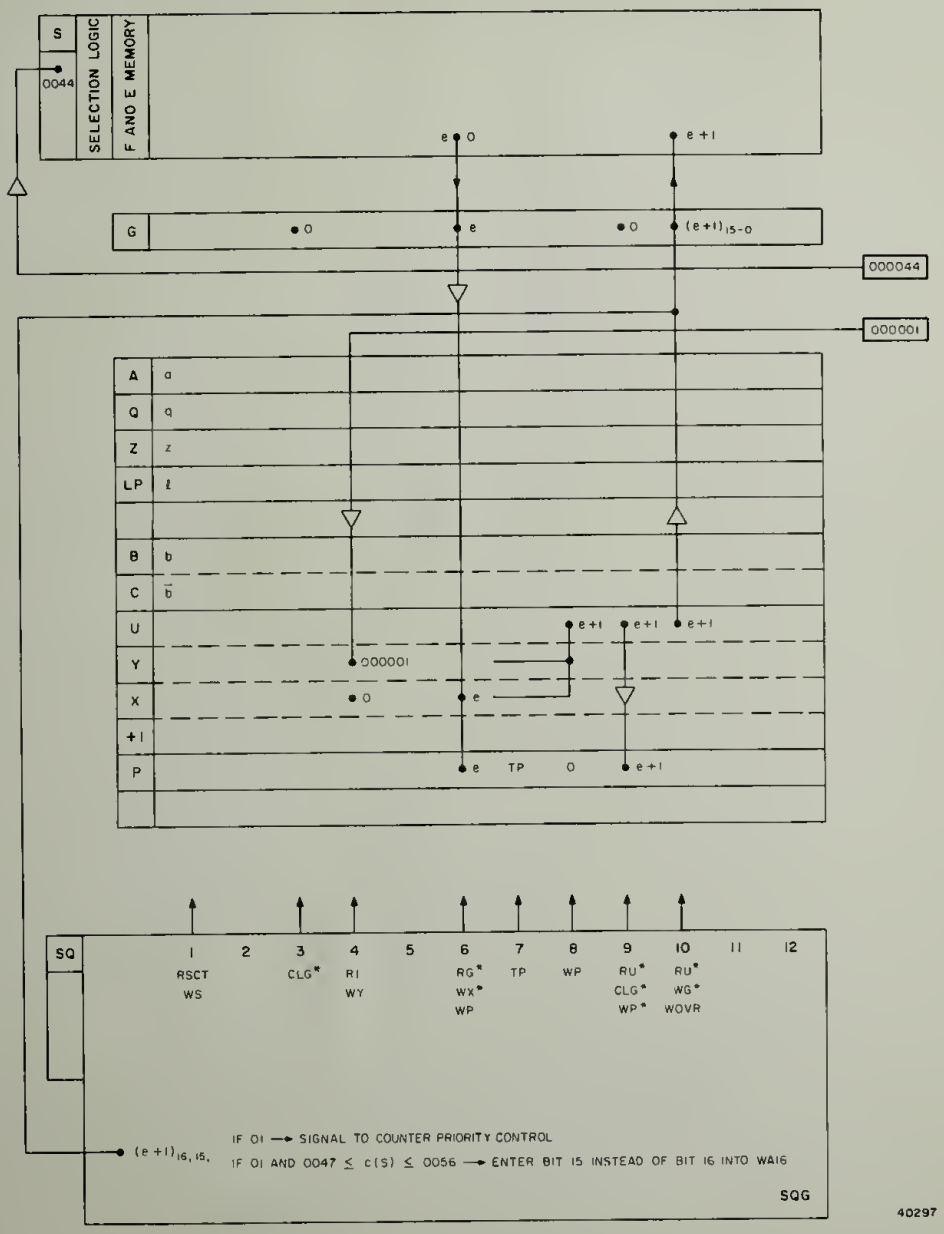

Figure 4-219. Subinstruction PINC

action 10. Control pulse WOVR transfers bits 16 and 15 of e + 1 into the SQG for test of overflow or underflow and resets counter priority control. In case of overflow, a signal is sent to the priority inputs.

4-8.8.2.4 Instruction MINC (Decrement Content of Addressed Counter). Instruction MINC means: decrement by one the quantity contained in that counter of which the address is provided by counter priority control. The entire operation MINC can be formulated as follows:

(1) Enter into S the address provided by counter priority control.

(2) Set c(CTR) = b(CTR) + 177776.

(3) In case of underflow, send the signal to priority control or the reverse sign if CTR - 0047, 0050, 0051, 0052, 0053.

(4) Reset counter priority control.

Instruction MINC consists of only one subinstruction, MINC. Figure 4-220 illustrates the execution of MINC which decrements the content of counter 0044. Figure 4-220 is the same as figure 4-219 except that control pulse RB1 at action 4 is replaced by control pulse R1C which reads quantity 177776 into Y. The decremented quantity is e - 1. In case of underflow of quantity e - 1, a signal is sent to counter priority control.

4-8.8.2.5 Instruction SHINC (Shift Content of Addressed Counter). Instruction SHINC means: shift one position to the left the quantity contained in that counter the address of which is provided by counter priority control. Instructions SHINC and SHANC are used to convert serial uplink data to parallel data. The entire operation SH1NC can be formulated as follows:

(1) Enter into S the address provided by counter priority control.

(2) Set c(CTR) = 2b(CTR) = $\overleftarrow{b(CTR)}$.

(3) If bit 15 of the quantity located at 0041 is a ONE, send a signal to interrupt priority control at the time the quantity is transferred into the adder to initiate the UPRUPT program.

(4) Reset counter priority control.

Instruction SHINC consists of only one subinstruction, SHINC. Figure 4-221 illustrates the execution of SHINC which shifts the content of location 0041 one position to the left. At action 1, address 0041, provided by counter priority control, is entered into S and the selection logic gates location 0041 for readout and write-in. At action 3 register G is cleared as usual. At action 4 registers X and Y are cleared. At action 6 quantity e of the addressed counter is transferred to Y, X, and P and the sign bit is entered into the SQG. If bit position 16 of Y or X (i.e., bit position 15 of location 0041) contains a ONE, a signal is sent to interrupt priority control to initiate

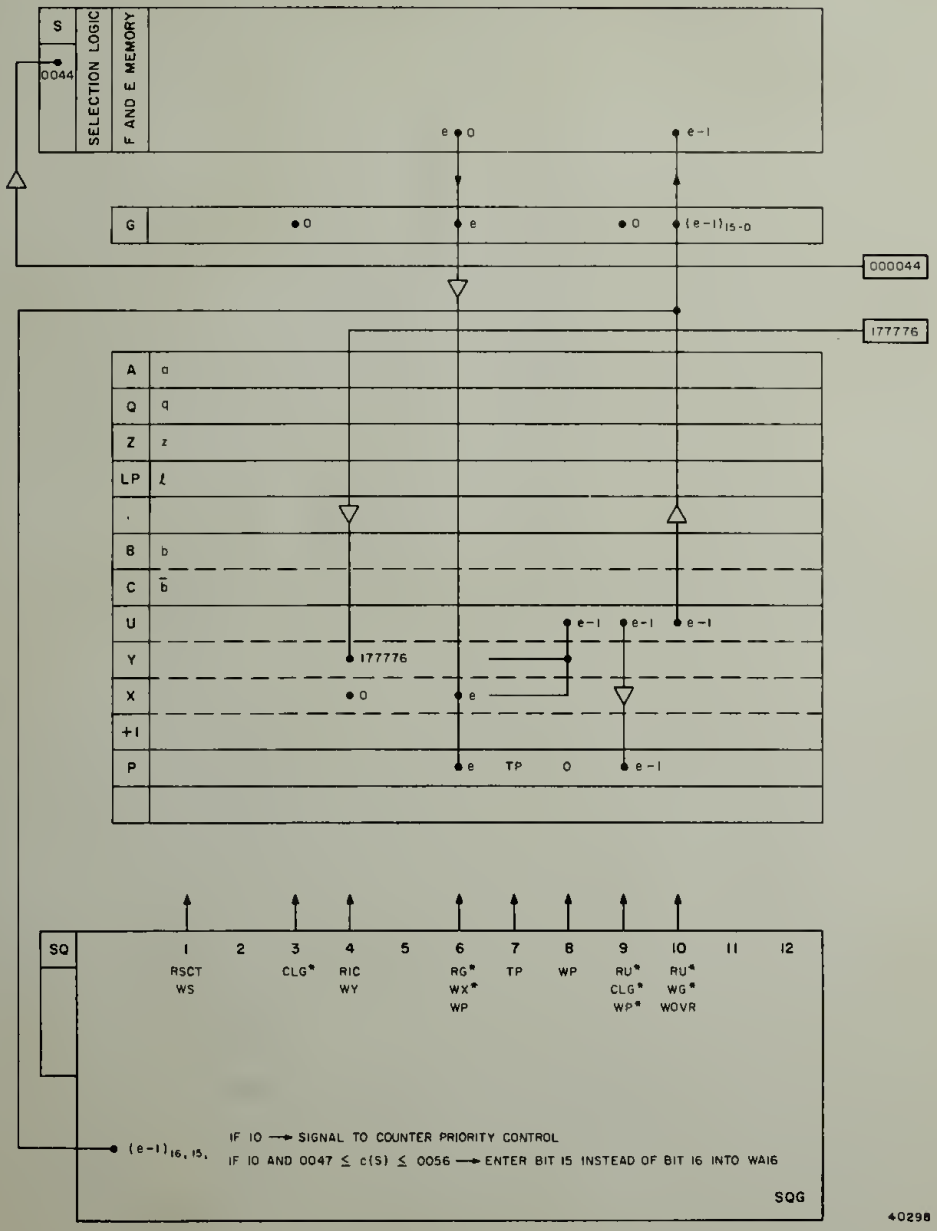

Figure 4-220. Subinstruction MINC

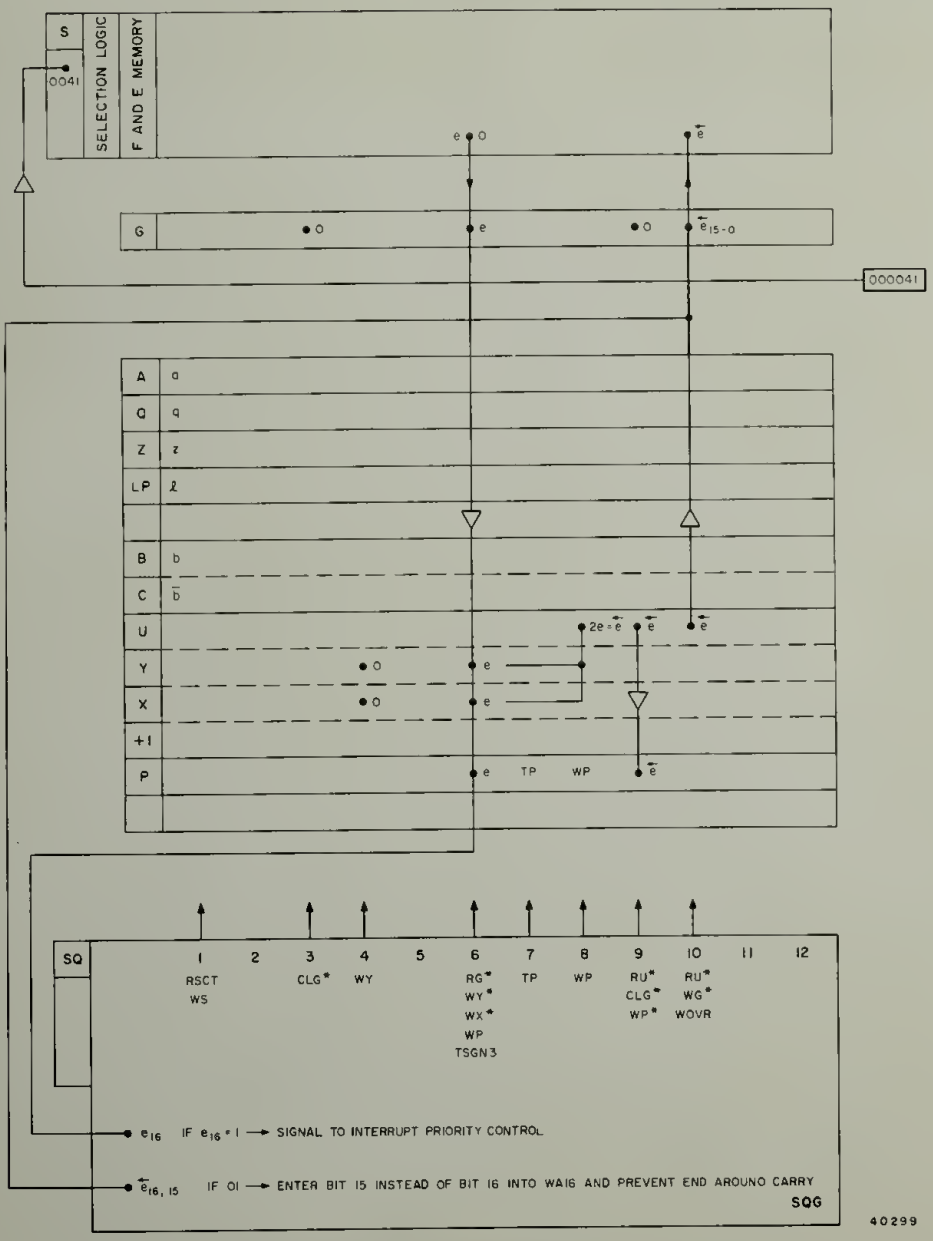

Figure 4-221. Subinstruction SHINC

the UPRUPT program. At action 7 an alarm is caused in case of incorrect parity. At action 8 register P is cleared. At action 9 register G is cleared again and the sum e + e = 2e = $\overleftarrow{e}$ is written into P. At action 10 control pulse RU* reads the shifted quantity ($\overleftarrow{e}$) into the WA's and control pulse WG* writes the contents of the WA's and the parity bit generated for quantity $\overleftarrow{e}$ into register G. Also at action 10, the complete word e_{15-0} is returned to location 0041.

Figure 4-222 demonstrates how the completion of an uplink word is signalled. In the example shown, several bits of the uplink word have already been received and the flag bit (the first bit of a word received via uplink) has moved into bit position 14 of location 0041. The flag bit is used to indicate the completion of the uplink word. At instant 1 the flag bit (1) is located at bit position 14 and bit position 13 through 1 contain data. At instant $\overline{2}$ the quantity located at 0041 is entered into both Y and X. At instant 4 the shifted quantity is transferred from U to location 0041 and the flag bit is now contained in position 15. By shifting the content of location 0041 once more at instants 5, 6, and 7, the data moves into bit position 15 through 3 and the flag bit gets lost.

4-8.8.2.6 Instruction SHANC (Shift Content of Addressed Counter and Add One). Instruction SHANC means shift one position to the left quantity contained in that counter the address of which is provided by counter priority control and add one to it. Instructions SHINC and SHANC are used to transform serial uplink and radar range data into

INSTANT	FUNCTION	LOCATION 0041															
		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	0041		0	$\underline{1}$	1	0	1	1	0	1	1	1	0	1	1	1	1
2	0041 → Y,X	0	0	1	1	0	1	1	0	1	1	1	0	1	1	1	1
	NORMAL SUM	0	1	1	0	1	1	0	1	1	1	0	1	1	1	1	0
3	U	1	1	1	0	1	1	0	1	1	1	0	1	1	1	1	0
4	0041		$\underline{1}$	1	0	1	1	0	1	1	1	0	1	1	1	1	0
5	0041 → Y,X	$\underline{1}$	$\underline{1}$	1	0	1	1	0	1	1	1	0	1	1	1	1	0
	NORMAL SUM	1	1	0	1	1	0	1	1	1	0	1	1	1	1	0	1
6	U	1	1	0	1	1	0	1	1	1	0	1	1	1	1	0	0
7	0041		1	0	1	1	0	1	1	1	0	1	1	1	1	0	0

40300

Figure 4-222. Completion of an Uplink Word

parallel data for use by the computer. The entire operation SHANC can be formulated as follows:

(1) Enter into S the address provided by the counter priority control.

(2) Set c(CTR) = 2b(CTR) + = $\overleftarrow{b}$(CTR) + 1.

(3) If bit position 15 of location 0041 or 0056 contains a ONE, send a signal to interrupt priority control to initiate the UPRUPT program.

Instruction SHANC consists of only one subinstruction, SHANC. Figure 4-223 illustrates the execution of SHANC which shifts the content of location 0041 one position to the left and enters a ONE into the new bit position 1. Figure 4-223 is the same as figure 4-221 except that control pulse CI is added to action 7 to add a one to the shifted quantity.

> NOTE: Although the CTS is outside the scope of this document, some of its functions are described in the following paragraphs.

4-8.8.3 Miscellaneous Instructions. The miscellaneous instructions consist of the start instructions (go and start at specified address), display, and load instructions (OINC and LINC). The sequence generator generates order and subinstruction codes for the go and start at specified address instructions. The timer supplies the start signal which initiates the start instructions. The CTS supplies the start at specified address instruction. The display and load initiation signals are instruction commands received from priority control circuits and are initiated by the CTS. As with the counter instructions, the display and load instructions have no order or subinstruction code.

The go instruction occurs in conjunction with the start signal. This instruction transfers AGC control to an instruction word that begins a program operation which places the AGC in an idle mode. The program being performed when the start signal occurs is displayed on the DSKY's. Through DSKY operation, the AGC can be returned to the original program or any other selected program. Other programs might be selected to perform tests if the start signal was generated as the result of an alarm. (The start signal can also be generated by the CTS.)

The start at specified address instruction enables the CTS to transfer AGC control to selected instruction words. An address is received from the CTS and copied into the central processor when the instruction is performed.

The display and load instructions are initiated by the CTS. The display instruction obtains a word from memory that is addressed by the CTS and provides this word to the CTS for display and other uses. The load instruction loads data from the CTS into memory locations that are addressed by the CTS.

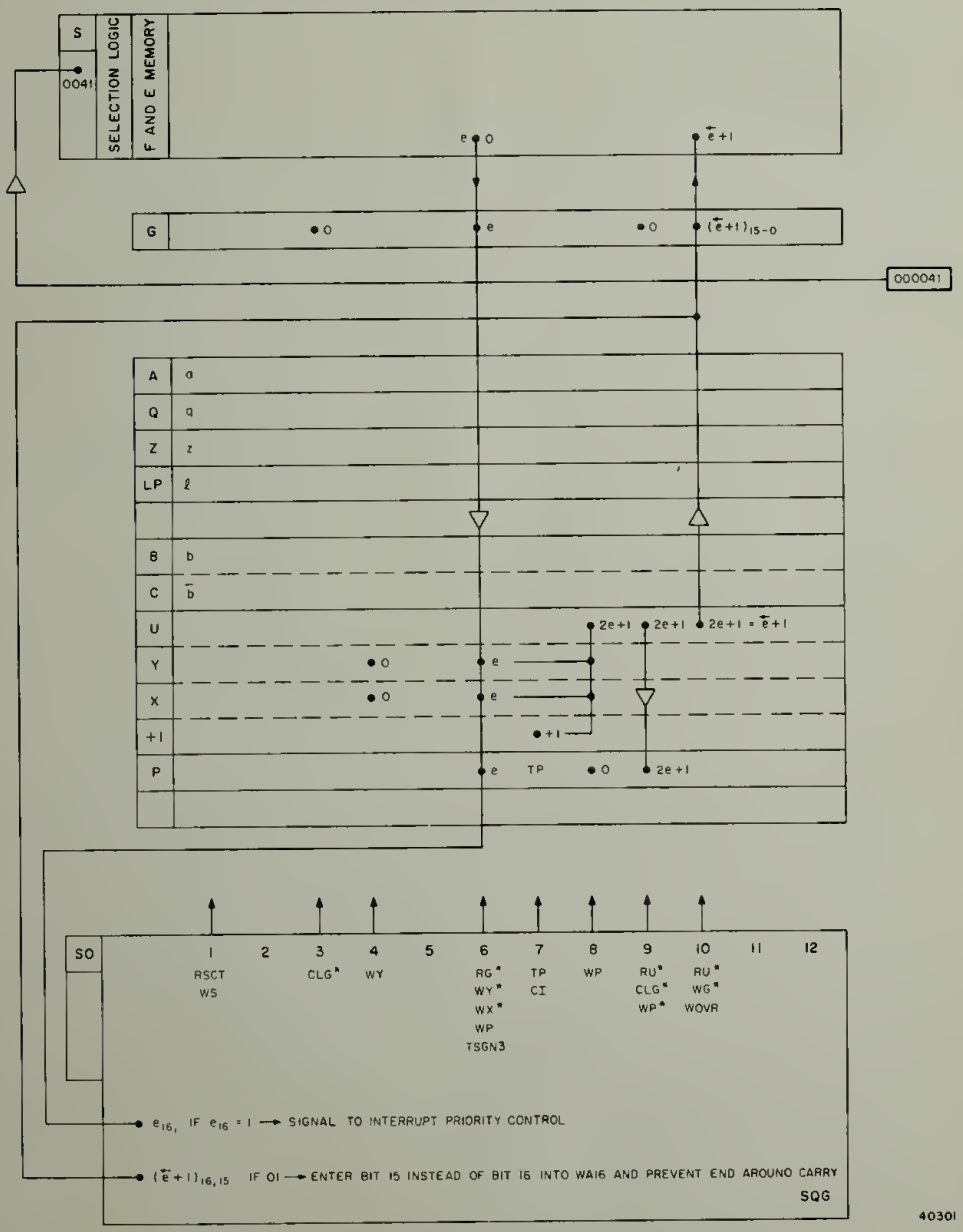

Figure 4-223. Subinstruction SHANC

4-8.8.3.1 Instruction GO (Computer GO). Instruction GO means: get AGC operating by executing the instruction located at START first, where START is a fixed address stored in the AGC. Instruction GO is identical to instruction TC except that control pulse RB at action 1 is replaced by RSTRT (Read STRT). Pulse RSTRT transfers the START address into register S, and the selection logic gates location START for readout. After the execution of GO, the instruction stored at location START is contained in B and its order code is in register SQ.

4-8.8.3.2 Instruction TCSA (Start at Specified Address). Instruction TCSA means: start the execution of a program by executing the instruction located at SA first, where SA might be any specified address entered into the AGC by the CTS. Instruction TCSA is identical to GO except that at action 1 RSA replaces RB instead of RSTRT.

4-8.8.3.3 Instruction OINC (Display Content of Addressed Location). Instruction OINC stands for zero increment and means: read and display the content of the addressed location. Instruction OINC is used in conjunction with the CTS. The content of the addressed location is displayed by punching an address into the keyboard and pressing a READ button. Figure 4-224 illustrates the execution of OINC for display of data e located at address 1.

4-8.8.3.4 Instruction LINC (Load Addressed Location). Instruction LINC stands for load increment and means: write into the addressed location the data punched into the keyboard. Instruction LINC is also used in conjunction with the CTS. By punching both an address and data into the keyboard, then pressing a LOAD button, the data will be entered into the location selected. Figure 4-225 illustrates the execution of LINC for data d to be written into location 1.

4-8.9 PROGRAMS. An AGC program performs such functions as solving guidance and navigation problems, testing the operation of the G and N system, and monitoring the operation of the spacecraft. Such a program consists of a group of program sections that are classified according to the function they perform. These classifications are mission functions, auxiliary functions, and utility functions.

Mission functions are performed by program sections that implement operations directly concerned with the major functions of the G and N system. These operations include erecting the IMU stable member and aligning it to a desired azimuth while the spacecraft is situated on the ground. The mission functions also include realignment of the stable member each time the ISS is energized during a flight. Other mission functions include the computation of spacecraft position and velocity during coasting periods of the flight by solution of second-order differential equations which describe the motions of a body subject to the forces of gravity. In addition, the mission functions test other elements of the G and N system.

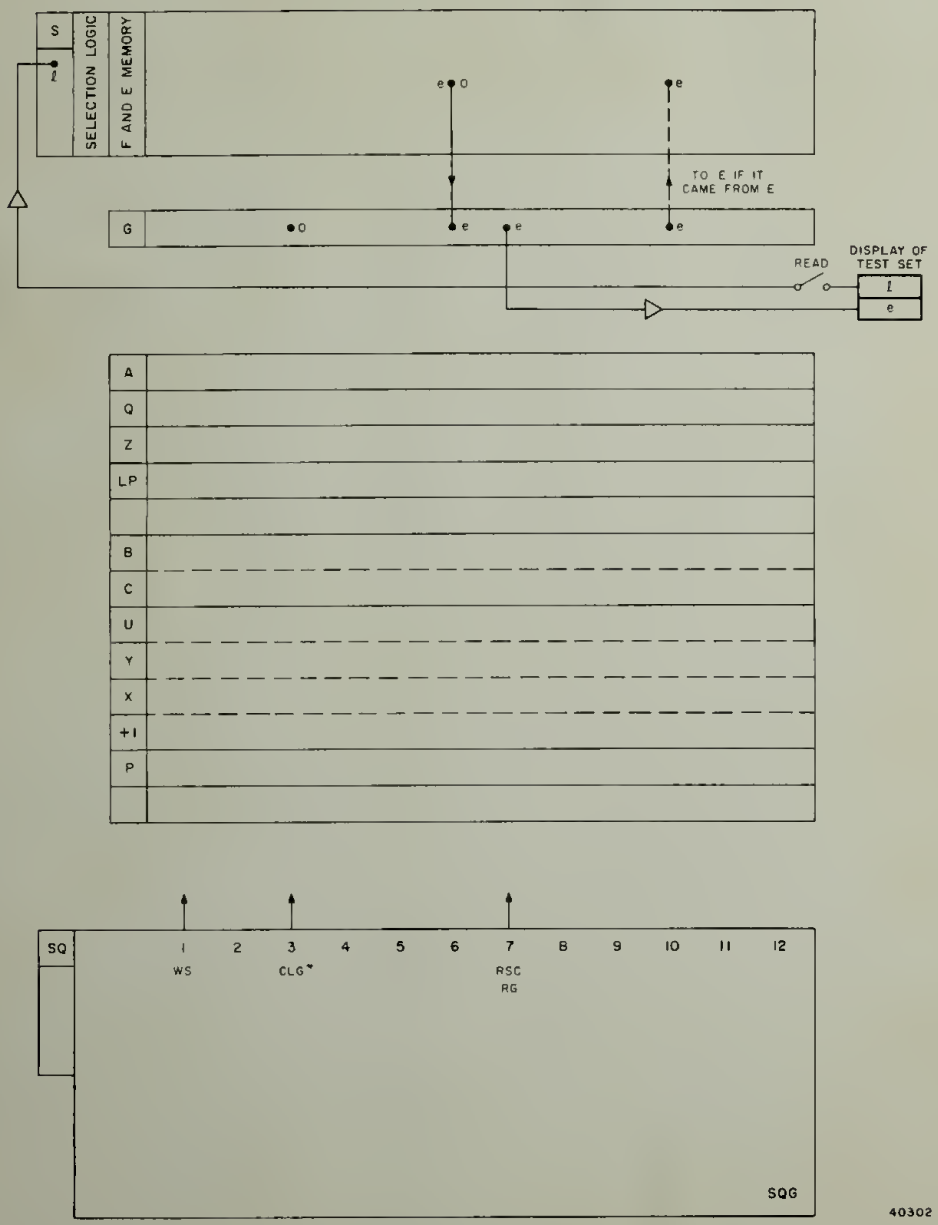

Figure 4-224. Subinstruction OINC

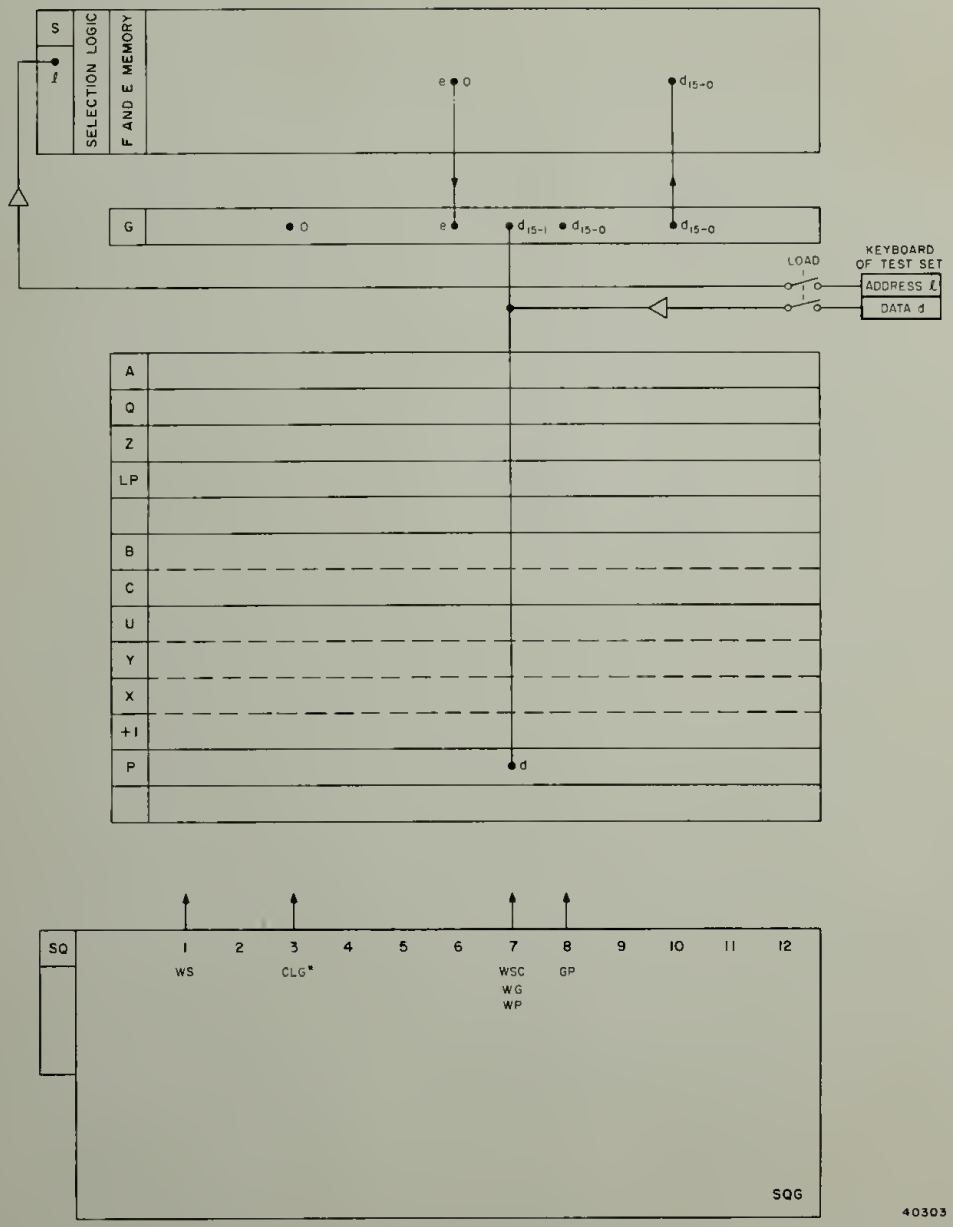

Figure 4-225. Subinstruction LINC

Auxiliary functions are executed at the occurrence of certain events, requests, or commands to implement many and varied operations in support of the mission functions. These operations include:

(1) Starting and restarting most program sections in response to a keyboard entry via the DSKY's or as the result of a hardware failure.

(2) Accepting and processing keyboard and uplink information.

(3) Supplying data to the telemetry system.

(4) Servicing devices outside the CSS which require high-frequency attention.

(5) Selecting the various modes of the IMU and OSS, and controlling the use of these units.

(6) Providing the means for aligning the IMU in flight.

(7) Testing the CSS.

(8) Displaying alarm messages on the DSKY's to notify the operator of failure conditions within the G and N system.

Utility functions are performed by program sections that coordinate and synchronize AGC activity to guarantee orderly and timely execution of required operations. These functions control the operation of the mission functions and the auxiliary functions by scheduling AGC operations on either a priority or a real-time basis. The utility functions also translate interpretive language to basic machine language which allows complex mathematical operations such as matrix multiplication and vector and multiprecision computations to be performed within the framework of compact routines at the expense of computing time. In addition, the utility functions supervise interrupt conditions and enable data retrieval and control transfer between isolated banks in the fixed-switchable portion of fixed memory.

The programs which have been wired into rope memory modules for field use with the AGC form a family of programs called the Sunrise programs. The current AGC program is Sunrise 45 which consists of 20 program sections as listed in table 4-XXVI. The table identifies the program sections as to the function they perform: M for mission function, A for auxiliary function, and U for utility function. The table also indicates where the program sections are located in fixed memory.

The following paragraphs contain descriptions of each program section organized by functional group. However, before describing the program sections, several terms must be introduced and defined so that they may be used to describe the program sections. These terms are phase, routine, job, and task.

Table 4-XXVI. Program Sunrise 45 -- Program Sections

Program Section		Memory Locations Used	
Name	Class	FF	FS
Interrupt (RPT and GO) Transfer Routines	U	2000 - 2036 3200 - 3203	
Interpreter	U	4000 - 5652 2130	03,6000 - 03,7435
Executive (Job Control)	U	2037 - 2123	04,6000 - 04,6351
Waitlister (Task Control)	U	2124 - 2127 2131 - 2216	04,6352 - 04,6501
Progress Control (Master Control)	U	2217 - 2300	04,6502 - 04,6743
Fresh Start And Restart	A		04,6744 - 04,7264
Telemetry (DOWNRUPT) Processor	A	2301 - 2426	
T4RUPT Output Control	A	2427 - 2466	10,6000 - 10,7053
Mode Switching and Mark	A	2467 - 2515	05,6000 - 05,6675 05,7345 - 05,7416 05,7740 - 05,7777 10,7054 - 10,7732 10,7740 - 10,7765
AGC Selfcheck	A		05,6676 - 05,7344
Interbank Communication	U	2516 - 2604	
Alarm And Display Processor	A	2605 - 2667	05,7634 - 05,7642
Initialization And Test (Orbital Integration)			22,6000 - 22,6304
Orbital Integration Initialization (Orbital Integration)	M		22,6305 - 22,7743 23,6000 - 23,6107
Prelaunch Alignment	M		23,6110 - 23,7020
RTB Op Codes	U		23,7021 - 23,7165
System Test	M		30,6000 - 30,7357 30,7400 - 30,7402
In-Flight (IMU) Alignment Routines	A		25,6000 - 25,6626
KEYRUPT And UPRUPT Processor	A		04,7265 - 04,7375
Pinball (Keyboard And Display)	A	2670 - 3117	21,6000 - 21,7621 24,6000 - 24,7630

A phase is an identifiable portion of a mission function that serves as a milestone at which a mission function may be reentered following the occurrence of an error during the execution of the mission function. This it is not necessary to restart at the beginning of the mission function.

A routine is a sequence of machine instructions which requires a request from a source outside of itself to set it into operation.

A job is a routine which is executed according to an assigned priority based on the relative importance of the job to the overall accomplishment of the Apollo mission.

A task is a routine which is to be executed at an assigned future time counting ahead from the present time.

4-8.9.1 Mission Functions. Three program sections are classified as mission functions: prelaunch alignment, oribital integration, and system test. Program section system test differs from the other two mission functions, in that it has no phases. This difference exists because system test is utilized only during CSS checkout and not during an actual flight. If an error occurs during the execution of system test, the program section is terminated and corrective action is initiated. If an error occurs during any other mission function, a fresh start or a restart is initiated depending upon the nature of the error.

4-8.9.1.1 Prelaunch Alignment. Prelaunch alignment aligns the IMU gimbals so that the X axis points along the local vertical and the Z axis points along a specified azimuth in the plane of the desired vehicle trajectory. During vertical erection both the Y and Z PIPA input channels are handled identically; during gyrocompassing the Z channel is maintained as in erection and the Y channel performs the azimuth alignment and holds the vertical orientation of the X axis.

4-8.9.1.2 Orbital Integration. Orbital integration computes position and velocity of the spacecraft during coasting periods of the Apollo mission. Position and velocity are maintained in the AGC in non-rotating rectangular coordinates and referenced to the earth. An earth-centered coordinate system is used.

4-8.9.1.3 System Test. System test measures various parameters of the G & N system and presents the results of these measurements for verification that system performance criteria are within given specifications.

4-8.9.2 Auxiliary Functions. Nine program sections are termed auxiliary functions. These are as follows:

(1) Fresh Start and Restart

(2) T4RUPT Output Control

(3) Telemetry Processor

(4) KEYRUPT and UPRUPT Processor

(5) Pinball

(6) Mode Switching and Mark

(7) AGC Self-Check

(8) Alarm and Display Processor

(9) In-Flight Alignment

These program sections perform various operations in support of the mission functions to facilitate accomplishment of the overall mission.

4-8.9.2.1 Fresh Start and Restart. A fresh start initiates most program sections in response to a keyboard entry from the DSKY's, when the AGC is turned on, when a serious error condition exists, or after a GO sequence if there is a disagreement between the phase tables. A restart initiates most program sections after a GO sequence when the phase tables agree. A restart returns program control to the beginning of the appropriate phase of that mission function which was interrupted by the error.

4-8.9.2.2 T4RUPT Output Control. The T4RUPT Output Control is activated when the TIME 4 counter overflows, and serves as a connection between the mission functions and devices external to the AGC. The operations performed by this program section include:

(1) Driving the IMU CDU's and the optics CDU's

(2) Updating the DSKY displays and discrete relay outputs

(3) Monitoring the IMU and optics

(4) Monitoring the downlink transmission rate to ensure that it is not too slow

(5) Checking for IMU, PIPA, and CDU failures.

4-8.9.2.3 Telemetry Processor. The telemetry processor is initiated on receipt of an end pulse from the NAA programmer, and provides data for downlink transmission and checks the transmission rate to ensure that it is not too fast. The transmitted data may represent a DSKY or UPLINK keycode, a DSKY relay word, a display character word, an identification word, or a data word.

4-8.9.2.4 KEYRUPT and UPRUPT Processor. Program section KEYRUPT or UPRUPT processor accepts data from the DSKY's, the optics, and uplink. Auxiliary function KEYRUPT is initiated each time a DSKY key is pressed or when the optics MARK button is pressed. Auxiliary function UPRUPT is initiated whenever data is received via uplink. After the data has been accepted, KEYRUPT and UPRUPT processor requests the execution of program section pinball which processes the data.

4-8.9.2.5 Pinball. Program section pinball processes information exchanged between the AGC and the astronaut. These exchanges are initiated primarily by keycode action; however, exchanges can also be initiated under internal AGC program control. Various functions are performed in response to requests from the keyboard; information resulting from these keyboard requests or internal requests from other program sections is displayed on the DSKY's.

4-8.9.2.6 Mode Switching and Mark. Mode switching and mark selects the ISS and the OSS modes of operation and controls the use of these subsystems. The selection and control is requested automatically by the mission functions or manually via keyboard entries. Mode switching and mark also supervises the input-output operations performed by T4RUPT output control which relate to ISS and OSS moding.

4-8.9.2.7 AGC Self-Check. The AGC self-check exercises most of the control pulses in the AGC to check performance of the AGC. This is accomplished by initiating various program instructions. Most of the control pulses in an instruction are used every time that particular instruction is executed; however, the functions that some of these pulses perform are not utilized until some time later. Therefore, a systematic method is used to exercise those pulses not used immediately. Program section AGC self-check is requested via the DSKY's and executed only when the AGC is idle, that is, when there is no job waiting to be performed. The AGC self-check also has the duty of maintaining the computer ACTIVITY indicator on the DSKY's. These indicators are illuminated only when a genuine job is being processed by the AGC.

4-8.9.2.8 Alarm And Display Processor. The alarm and display processor causes the display of certain failure messages on the DSKY's. These failures are defined as being either an alarm or an abort. Except for repeated alarms, an alarm is a failure which does not require an AGC fresh start or restart. In the case of repeated alarms, the astronaut may initiate a manual fresh start via a keyboard entry. An abort is a failure which requires an AGC fresh start. Both failure conditions are displayed on the DSKY's in a five-character code of the form AAANN where AAA identifies the program section or routine in which the failure occurred and NN identifies the specific error which has occurred.

4-8.9.2.9 In-Flight Alignment. Program section in-flight alignment provides the framework for aligning the IMU. The program section consists of a set of routines written in interpretive language which are used for geometric transformation of the many coordinate axes needed in the in-flight alignment process.

4-8.9.3 Utility Functions. Utility functions perform the housekeeping activities for the AGC. These activities include recording the progress of mission functions, supervising the execution of jobs, scheduling tasks, decoding and executing interpretive instructions, servicing interrupts, and transferring control between banks in fixed memory. The program sections classified as utility functions are as follows:

(1) Progress Control

(2) Executive

(3) Waitlist

(4) Interrupt Transfer Routines

(5) Interbank Communications

(6) Interpreter

(7) RTB Op Codes

4-8.9.3.1 Progress Control. Progress control consists of routines which initiate, terminate, change, and supervise the restart of all mission functions except system test. In addition, progress control maintains the PROGRAM indicators on the DSKY's.

The capability to start, stop, and change the mission functions manually is provided by progress control in conjunction with pinball via a keyboard entry. A restart is initiated following the detection of a hardware failure or an abort both of which cause a GO sequence. To implement restart, progress control maintains a phase table which indicates the status of all the mission functions. The phases stored in the table provide a point at which an interrupted mission function may be restarted. The phase table is stored in triplicate and the mission functions are restarted only if all three copies agree. If the copies do not agree, a fresh start is executed with no restart of the mission functions.

4-8.9.3.2 Executive. The executive supervises the execution of all requested jobs according to an assigned priority scheme. The job having the highest priority is allowed to operate until displaced by another job of higher priority. (As many as eight jobs may be in various stages of completion within the program at any given time.) Each job is assigned a job area which is a group of locations in erasable memory into which information relating to the job can be stored. When the job having the highest priority is completed, the executive initiates the execution of that job having the next highest priority. If no job is awaiting execution, a dummy job is executed which keeps the AGC idling until the next job request. While the AGC is idling, program section AGC self-check may be executed in response to a manual request from the DSKY's.

In addition, the executive places jobs into a dormant state when they require the occurrence of certain external events before proceeding. The executive then must reactivate these jobs when the external events have been completed.

4-8.9.3.3 Waitlist. Program section waitlist schedules the execution of tasks which must be executed at a specific time. Waitlist derives its timing from the TIME 3 counter and whenever this counter overflows, program control is transferred to that task which must be executed next. Waitlist maintains a list of tasks to be performed (up to six tasks may be simultaneously under its control). If there are less than six tasks awaiting execution, dummy tasks are used to fill the list. The dummy tasks are scheduled to be executed 81.93 seconds apart. A dummy task performs the same function for waitlist as the dummy job performs for the executive.

4-8.9.3.4 Interrupt Transfer Routines. The interrupt transfer routines save the contents of registers A (accumulator) and Q (return address) and transfer program control to the routines that must be executed when an interrupt transfer request is recognized. The interrupt transfer routines transfer program control to routines T3RUPT, T4RUPT, KEYRUPT, UPRUPT, and DOWNRUPT. The contents of the registers mentioned are saved so that program control can return to the instruction following that instruction which was being executed when the interrupt occurred and so that the data in the accumulator is not destroyed.

4-8.9.3.5 Interbank Communication. Interbank communication allows the transfer of information and/or control between banks in the fixed-switchable portion of fixed memory. This transfer is accomplished by transferring program control to fixed-fixed memory where the bank address can conveniently be changed. Then register S is set to address the desired location within the proper bank. Program control is then transferred to the correct location in fixed-switchable memory.

4-8.9.3.6 Interpreter. The interpreter translates into basic machine language and executes that part of the AGC program written in interpretive language. This allows for complex operations to be prepared in a compact form at the sacrifice of AGC operational speed. Routines written in interpretive language contain explicit double precision, vector, and matrix operations.

4-8.9.3.7 RTB Op Codes. The RTB Op Codes serve as an appendage to the interpreter to increase its effectiveness. The RTB Op Codes provide a convenient link between basic and interpretive language and make possible the execution of subroutines in basic language while operating in the interpretive mode.

4-8.9.4 Program Operation. The interaction between the various program sections during the operation of an AGC program is quite complex. Therefore, to facilitate the explanation of an AGC program, program operation is discussed in terms of interrupt, idle, normal, and abnormal conditions.

4-8.9.4.1 Interrupt Conditions. During program operation, five possible interrupts can occur; some occur at specific intervals, others at random. These interrupts enable the execution of tasks and the processing of input-output data. All interrupts suspend the execution of the current program section, save the contents of registers A and Q (the contents of registers B and Z are saved also by hardware action), and return program control to the intrrupted program section when the required interrupt operations have been completed. The interrupts initiate the execution of corresponding routines in program section interrupt transfer routines (figure 4-226). The five interrupt transfer routines transfer program control to routines T3RUPT, T4RUPT, KEYRUPT, UPRUPT, and DOWNRUPT.

Tasks are executed at specific times subject to the overflow of the TIME 3 counter. This counter is preset within routine T3RUPT to some value less than 163.84 seconds (overflow condition) and incremented every 10 msec until overflow occurs. When the counter overflows, the interrupt transfer routine associated with routine T3RUPT is initiated, interrupting the current program section, saving the contents of registers A and Q, and transferring program control to routine T3RUPT of program section waitlist. Routine T3RUPT initiates the execution of the task due and sets the TIME 3 counter so it will overflow when the next task is due. Upon completion of the initiated task, program control is returned to the interrupted program section with the content of registers A and Q restored to the values present at the time the interrupt occurred.

Various input-output operations must be performed periodically during the operation of an AGC program. These operations are initiated subject to the overflow of the TIME 4 counter which is preset in routine T4RUPT to overflow every 60 msec to perpetuate its execution.

When the TIME 4 counter overflows, the interrupt transfer routine associated with routine T4RUPT is initiated, interrupting the current program section, saving the contents of registers A and Q, and transferring program control to routine T4RUPT of program section T4RUPT output control. The execution of T4RUPT output control must be initiated periodically to perform the following operations:

(1) Transfer new information to DSKY's (one relay bank may be switched each 120 msec)

(2) Drive the IMU CDU's and the optics CDU's (the IMU CDU's may be driven every 60 msec and the optics CDU's every 480 msec)

(3) Sample the ISS mode and OSS mode settings (both may be sampled every 120 120 msec)

(4) Check the downlink rate to ensure that it is not too slow (the rate is checked every 120 msec)

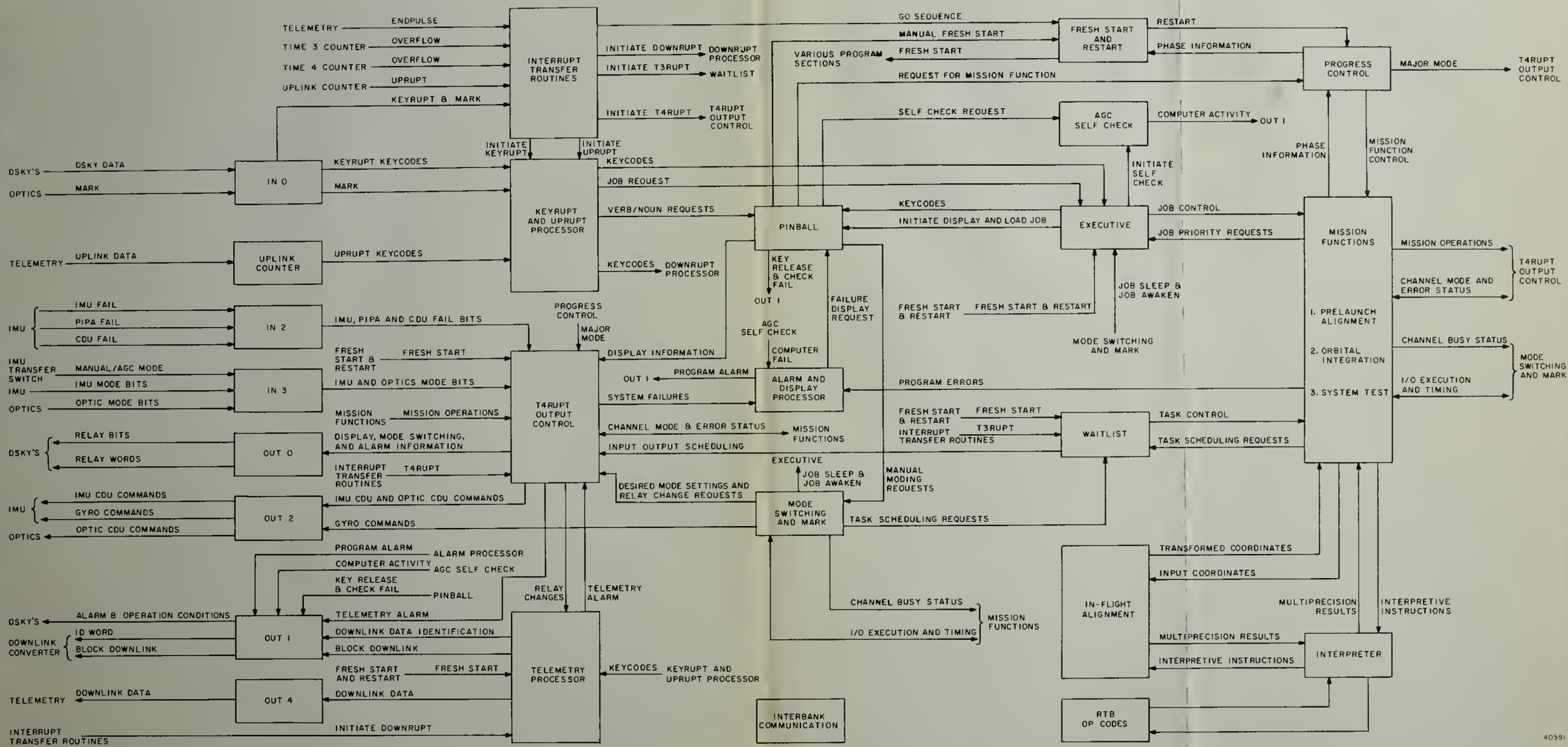

Figure 4-226. Program Sunrise 45

(5) Test for IMU, CDU, and PIPA failures (the test is made every 480 msec).

Upon completion of the required input-output operation, T4RUPT output control returns program control to the interrupted program section.

Whenever DSKY or MARK data is entered into the AGC, the current program section must be interrupted so the data can be accepted and processed. Therefore, each time a DSKY key (except key TEST ALARM) or the MARK button on the G & N indicator control panel is pressed, the interrupt transfer routine associated with routine KEYRUPT is initiated, interrupting the current program section, saving the contents of registers A and Q, and transferring program control to KEYRUPT and UPRUPT processor.

The KEYRUPT and UPRUPT processor accepts the input data and requests the executive to initiate the execution of pinball which decodes the data. After completing these operations, program control is returned to the interrupted program section.

The AGC will accept uplink data from the ground only when the UPTL switch on the AGC main panel DSKY is in the ACCEPT position. When uplink data is received, the current program section must be interrupted so the uplink data can be accepted and processed by the AGC. Therefore, upon the reception of each uplink word, the interrupt transfer routine associated with routine UPRUPT is initiated, interrupting the current program section, saving the contents of registers A and Q, and transferring program control to KEYRUPT and UPRUPT processor. Since uplink data is in a coded form similar to the DSKY keycodes except that the code is transmitted three times for verification, KEYRUPT and UPRUPT processor performs the same operations described for routine KEYRUPT.

The AGC provides data for transmission downlink at a rate of one to seven times in each 120 msec time period. At the end of each transmission, the current program section must be interrupted to allow the AGC to prepare for the next transmission. Therefore, each time a transmission has been completed, the telemetry system sends an END pulse to the AGC which initiates the interrupt transfer routine associated with routine DOWNRUPT in program section telemetry processor. This routine interrupts the current program section, saves the contents of registers A and Q, and transfers program control to the telemetry processor. The telemetry processor checks to insure the downlink rate is not too fast and, if the rate is not too fast, loads register OUT 4 with the data to be sent downlink during the next transmission. Then the telemetry processor returns program control to the interrupted program. If the downlink rate is too fast, a telemetry alarm is generated and displayed on the AGC navigation panel DSKY and the downlink transmission is blocked.

There are occasions during program operation when it is inconvenient to recognize and process an interrupt. Thus, an interrupt inhibit (INHINT) instruction is programmed into various program sections which inhibits the processing of interrupts while an operation is being performed which should not be interrupted (e.g., displaying information on the DSKY's). Upon the completion of the operation, an interrupt release (RELINT) instruction is used to release the INHINT instruction and allow interrupts to be processed when they occur. Interrupt requests received between the execution of instructions INHINT and RELINT are not lost, but are stored for processing after RELINT is executed.

4-8.9.4.2 Idle Conditions. When power is first applied to the CSS, the hardware automatically initiates the GO sequence (GOJAM) and program control is transferred to program section fresh start and restart. Fresh start and restart initializes certain locations (registers) in erasable memory which results in the following:

(1) The executive has no jobs awaiting execution except the dummy job

(2) The waitlist has no tasks scheduled to be executed except the dummy task

(3) The three phase tables in progress control are set to agree

(4) All relays under AGC control are deenergized which clears the displays on both DSKY's and places the G & N system in the attitude control mode. (In this mode power is removed from the IMU.)

(5) The TIME 3 and TIME 4 counters are preset to overflow in 10 msec.

Program control is then transferred to program section AGC self-check where the dummy job is executed.

The dummy job continually searches for a genuine job of higher priority. However, since power has just been applied, no jobs have been requested and the dummy job is continually executed to keep the AGC idling until the execution of a genuine job is requested via a keyboard entry or uplink. Until a genuine job is requested, the AGC continues operating in a loop and can only be interrupted by an interrupt transfer routine.

While the AGC is idling awaiting a KEYRUPT or UPRUPT, only those interrupt transfer routines associated with T3RUPT, T4RUPT, and DOWNRUPT are intermittently active. Every 81.93 seconds the TIME 3 counter overflows, the dummy job is interrupted and suspended, and program control is transferred to the waitlist at routine T3RUPT, Routine T3RUPT initiates the execution of the dummy task since no genuine tasks are scheduled. When the dummy task has been completed, program control is returned to the interrupted job which is in this instance the dummy job. The dummy task continues to be executed every 81.93 seconds until the idling condition is terminated.

Within the 81.93 second intervals the TIME 4 counter overflows every 60 msec, interrupting the execution of the dummy job and causing program control to be transferred to program section T4RUPT output control. There are no operations to be performed by this program section while the AGC is idling; therefore, program control returns to the dummy job.

Routine DOWNRUPT in the telemetry processor is also intermittently active at this time because END pulses are received one to seven times every 120 msec. When an END pulse is received, the execution of the dummy job is interrupted, program control is transferred to the telemetry processor which loads register OUT 4, and program control is returned to the dummy job.

Routines UPRUPT and KEYRUPT are inactive because the AGC receives no inputs from uplink or the DSKY's during the idling condition. Thus, in the idle condition, the program executes only the dummy job in program section AGC self-check, routine T3RUPT in program section waitlist, the T4RUPT output control, and the telemetry processor. The dummy job is executed most of the time with brief moments taken by program sections waitlist, T4RUPT output control, and telemetry processor.

4-8.9.4.3 Normal Conditions. The following discussion of the AGC program in normal operation assumes the AGC has been turned on recently, is presently idling, and has received no job requests. It is further assumed that the TRANSFER switch on the IMU control panel is in the COMPUTER position. Several of the initial operations performed during mission function prelaunch alignment are described to illustrate the interplay among program sections to accomplish these operations. However, before discussing the AGC program in normal operation, the overall purpose of prelaunch alignment is discussed.

Mission function prelaunch alignment is used to align the IMU prior to launch. This is necessary to ensure that the thrust acceleration will be in the plane of trajectory, to prevent gimbal lock during launch, and to monitor the boost phase for failures. Prelaunch alignment is performed in four steps: initialization, ISS moding, vertical erection, and gyrocompassing. The discussion of the AGC program in normal operation is confined to only the initialization and the zero encoder portion of the ISS moding. This is sufficient for adequate understanding of the interplay among program sections.

Mission function prelaunch alignment is initiated through either DSKY keyboard by pressing keys VERB, 3, 7, ENTER, D_1, D_2, and ENTER where D_1 is key 0 and D_2 can be any of the digit keys between 0 and 7. VERB 37 is a request to change the major mode (mission function) to that specified by digits D_1 and D_2. In this discussion, D_1 is key 0 designating mission function prelaunch alignment and D2 is key 1 designating manual phase 1. The manual phases should not be confused with the internal phases described previously. A manual phase is a keyed-in code used at the keyboard to gain access to an internal phase (or combination of internal phases) of the mission function.

When the VERB key is pressed, the AGC generates a KEYRUPT which interrupts the dummy job and initiates the appropriate interrupt transfer routine. Program control is then transferred to KEYRUPT and UPRUPT processor which accepts the five-bit keycode representing key VERB and requests the executive to schedule the job CHARIN in pinball. When the request has been processed by the executive, KEYRUPT and UPRUPT processor stores the keycode in a register of the job area assigned to the requested job CHARIN. Program control returns to the dummy job which checks for a genuine job and finds there is one, job CHARIN. Program control is then transferred via the executive to pinball where job CHARIN decodes the keycode. When the decoding is complete, program control returns to the executive which terminates job CHARIN and reinitiates the dummy job. The dummy job remains active until another keyboard entry is received.

The sequence of operations is repeated for each keyboard entry; however, the specific action taken by job CHARIN is dependent upon the particular keycode received. When key VERB is pressed, job CHARIN requests that the VERB indicators be blanked and conditions the AGC to accept the next two entries (digits 3 and 7) as a Verb code. As keys 3 and 7 are pressed, job CHARIN, which is executed twice, once per key, requests the display of digits 3 and 7 in the VERB indicators, and preserves the Verb code for later use. When key ENTER is pressed, job CHARIN requests that the VERB indicators flash to alert the astronaut that additional information must be keyed in. Then the astronaut keys in digits 0 and 1 and job CHARIN (again executed twice) requests the display of the digits in the NOUN indicators as they are entered. Upon pressing key ENTER the second time, job CHARIN blanks the NOUN indicators and decodes the two digits 0 and 1. Program control is then transferred to program section progress control.

Each time job CHARIN makes a display request, program section T4RUPT output control honors the request within 120 msec during a T4RUPT. The requested display information is supplied to the DSKY's via register OUT 0. In addition, the keycodes (from job CHARIN) and the resulting relay changes (from T4RUPT output control) are sent downlink by program section telemetry processor subject to DOWNRUPT's.

When the last entry has been processed and program control has been transferred to progress control, the mission function code 0 is used to determine the proper place (cell) in the phase table. The phase presently contained in the cell is replaced with the manual phase (1) just keyed in. Program control is then transferred to the executive to request the execution of prelaunch alignment. Program control returns to progress control and is passed on to pinball to update the PROGRAM indicators on the DSKY's which will display digits 0 and 1. (The digits 0 and 1 which are displayed on the DSKY's are not the same digits that were keyed in but rather a two-digit code representing prelaunch alignment.) The executive then assumes program control, terminates job CHARIN, and searches for the job having the highest priority.

At this time, prelaunch alignment, which is now considered a job, has the highest priority; therefore, program control is transferred to it. Prelaunch alignment immediately utilizes progress control to change the content of the phase table cell from the manual phase to the internal phase. Program control is returned to prelaunch alignment and its execution is continued.

As a result of keying in manual phase 1, prelaunch alignment sets the IMU azimuth gimbal angle to a desired value, zeros the initial gimbal angles, zeros the gyro drift rates, and sets the latitude angle. Program control is then transferred to mode switching and mark to initiate the zero encoding sequence. This initiation includes requesting the zero encode mode and the scheduling of a task by the waitlist which is executed after a 40 second delay. (The 40 second delay is required to allow the CDU shafts to reach the zero position.) This is the first of five tasks required to complete the zero encoding sequence which equates the reading of the CDU dials with the actual gimbal angles. (The

five tasks are scheduled to be executed by transferring program control to the waitlist where each task, when executed, requests the scheduling of the following task. Thus, the first task schedules the second, the second the third, et cetera.)

Program control is transferred from the waitlist back to mode switching and mark and on to prelaunch alignment where further initialization is performed. This transfer consists of setting up a five minute period for vertical erection, setting the nominal gain for driving the CDU's, and clearing the gyro command registers. This initialization requires only a very small part of the 40 second delay prior to execution of the first task. Thus program control is transferred to mode switching and mark which requests the executive to put prelaunch alignment into a dormant state (made active) until all five tasks have been completed. Between each task the executive then searches for the job having the next highest priority which is the dummy job. Program control is transferred to AGC self-check where the dummy job keeps the AGC operating in a loop while checking for the existence of a genuine job.

This operation continues until the 40 second delay has elapsed; then a T3RUPT occurs which transfers control to the waitlist and the task is executed. However, during the waiting period, T4RUPT output control is initiated between 600 and 700 times. The first and second (or second and third) times that T4RUPT output control is executed, the mode switching that was requested is accomplished and register IN 3 is tested to verify that the mode switching has in fact been accomplished. In addition, the TIME 3 counter might overflow before the 40 second delay elapses due to a request for the dummy task which occurs every 81.93 seconds.

When the 40 second delay is over, program control is transferred from AGC self-check to the waitlist by means of a T3RUPT. Program control is then transferred to mode switching and mark where the scheduled task is executed. During the execution of the task, a request is made to the waitlist for the scheduling of the next task and program control goes to the dummy job until the task comes due. (The dummy job is interrupted by T3RUPT's, T4RUPT's, and DOWNRUPT's and the mode switching is verified during the initial T4RUPT's.) This sequence of operation is repeated until all five tasks have been requested and successfully completed. During the execution of the last task, mode switching and mark requests the executive to make prelaunch alignment active once again. When prelaunch alignment is again executed, it completes the remaining IMU moding and further initialization before entering the vertical erection portion of its operation.

4-8.9.4.4 Abnormal Conditions. During program operation, several abnormal conditions may occur. These conditions are classified as hardware failures, aborts, or alarms. A hardware failure occurs as the result of such conditions as incorrect parity, a counter failure, an interrupt lock or a transfer control (TC) trap. An abort occurs when a serious program failure exists such as an excessive number of jobs or tasks. An alarm occurs when a program failure exists which is not too serious, such as the reception of unrequested mark information. Hardware failures and aborts result in AGC restart while alarms may (or may not) result in an AGC fresh start subject to the discretion of the astronaut. It is assumed in the following paragraphs that mission function prelaunch alignment is operating when the abnormal conditions occur.

When a hardware failure occurs, the appropriate failure indicator is illuminated on the AGC navigation panel DSKY, the COMP FAIL indicator is illuminated on the AGC main panel DSKY, and a GO sequence is initiated automatically, transferring program control to program section fresh start and restart. A restart is initiated and the phase tables are checked for agreement. Assuming the phase tables agree, program control is transferred to program section progress control which determines the phase of mission function orbital integration and examines this phase to determine if orbital integration is active. Since (by definition) no mission function is active except prelaunch alignment at this time the code for orbital integration is not displayed on the DSKY's and the executive does not request its execution. Next, the phase of prelaunch alignment is determined and examined to ascertain if prelaunch alignment is active. Prelaunch alignment being active, program control is transferred to fresh start and restart where the mission function code is made available for display. Program control is then transferred to prelaunch alignment where a request is made to the executive to execute prelaunch alignment (prelaunch alignment requests the execution of itself). Program control is transferred from the executive to fresh start and restart via prelaunch alignment. Since there are no other mission functions to examine at this time, program control is transferred to the executive to request the execution of job DOALARM in the alarm and display processor. Pinball then assumes program control via fresh start and restart and requests the display of the current (active) mission function code, 01 for prelaunch alignment. Program control is transferred to AGC self-check where the dummy job is initiated.

During the routine check for a genuine job, job DOALARM is found to have the highest priority and program control is transferred to it via the executive. Since a hardware failure does not have a display code and no aborts or alarms have occurred previously, job DOALARM has no failure code to display. However, since pinball has requested a display, five zeros are prepared for display in display register R1; digits 0 and 1 are displayed in the VERB indicators; and digits 3 and 1 are displayed in the NOUN indicators on both DSKY's. These displays are performed subject to T4RUPT output control within 120 msec.

Program control passes from job DOALARM to the executive which terminates job DOALARM, searches for the next highest priority job which is prelaunch alignment, and transfers program control to prelaunch alignment. Program control is transferred to progress control to obtain the phase that prelaunch alignment was in when the hardware failure occurred. Program control returns to prelaunch alignment, examines the phase just obtained to determine if a manual phase was recently keyed in and, assuming no manual phase, it commences execution at the beginning of the internal phase. Thus the hardware failure operation is completed.

When an abort occurs, program control goes to the alarm and display processor which causes the PROG ALM (program alarm) indicator on the AGC navigation panel DSKY to light via an entry into register OUT 1. The alarm and display processor then sets up a display code indicating where the abort occurred and the type of abort that exists. Then the alarm and display processor enters a loop that results in a TC trap which causes a GOJAM. The sequence of operation from this point on is similar to that of a hardware faulure except that job DOALARM displays a failure code via program sections pinball and T4RUPT output control.

When an alarm occurs, program control goes to the alarm and display processor which causes the PROG ALM indicator on the AGC navigation panel DSKY to light, re-

quests the execution of job DOALARM, and returns program control to location L + 2 (where location L is the location at which the alarm occurred and L + 1 is the location at which the failure code is stored). At the next break point (place where a current job can be superseded by a higher priority job), the executive executes job DOALARM to display the failure code. If the alarm condition repeats, the astronaut has the option of manually initiating a fresh start by a keyboard entry. A fresh start results in the AGC entering an idle state similar to that previously discussed.

4-9 DISPLAY AND KEYBOARDS (DSKY's)

The CSS has two DSKY's associated with it. One is mounted on the main display and control panel in the lower equipment bay of the command module. It is designated the AGC main panel DSKY. The other DSKY is on the navigation display and control panel. It is designated the navigation panel DSKY. Both DSKY's provide a means of communicating with the AGC. They enable the astronauts to load information into the AGC, request information from the AGC, initiate various programs stored in memory, and perform tests on the AGC and other subsystems of the G and N system. The DSKY's also provide an indication of failure and operational changes which may occur within the AGC or G and N system. Except for a few differences in the number of controls and alarm indicators, the two DSKY's are electrically identical.

4-9.1 AGC MAIN PANEL DSKY FUNCTIONAL DESCRIPTION. The AGC main panel DSKY consists of a keyboard, power supply, decoder, relay matrix, alarm circuits, and displays.

The keyboard (figure 4-227) contains the key controls with which the astronaut operates the DSKY. Inputs to the AGC initiated via the keyboard are processed by the program. The resulsts are supplied to the decoder and relay matrix for display. The key controls on the AGC main panel DSKY initiate keycode, key reset, and error reset signals which are routed to the AGC. Each key when pressed will produce a 5 bit code. The keycode is entered into the AGC and initiates an interrupt to allow the data to be accepted. The key reset signal is generated each time a key is released, and conditions the AGC to accept another keycode. The error reset signal extinguishes the failure indicators on both DSKY's. In addition, the AGC main panel DSKY supplies a check uplink signal (voltage level) to the spacecraft and to the input-output section which inhibits the reception of data via uplink.

The power supply utilizes +28 volts dc and +13 volts dc from the AGC power supply and an 800 cps sync signal from the timer to generate a 275 volt, 800 cps display voltage. The display voltage is applied to the displays via the relay matrix and alarm circuits.

The decoder receives a four bit relay word (RLYWD) from register OUT 0 in the AGC. The relay word in conjunction with relay bits 1 through 11 (RLYBIT) from register OUT 0 energizes specific relays in the matrix. The relays are energized by the coincidence of a selection signal from the diode matrix in the decoder which produces a row select signal, and relay bits which produce column select signals. Relay selection allows the display voltage (275 volts, 800 cps) from the power supply to be routed to the proper sign and digit indicators.

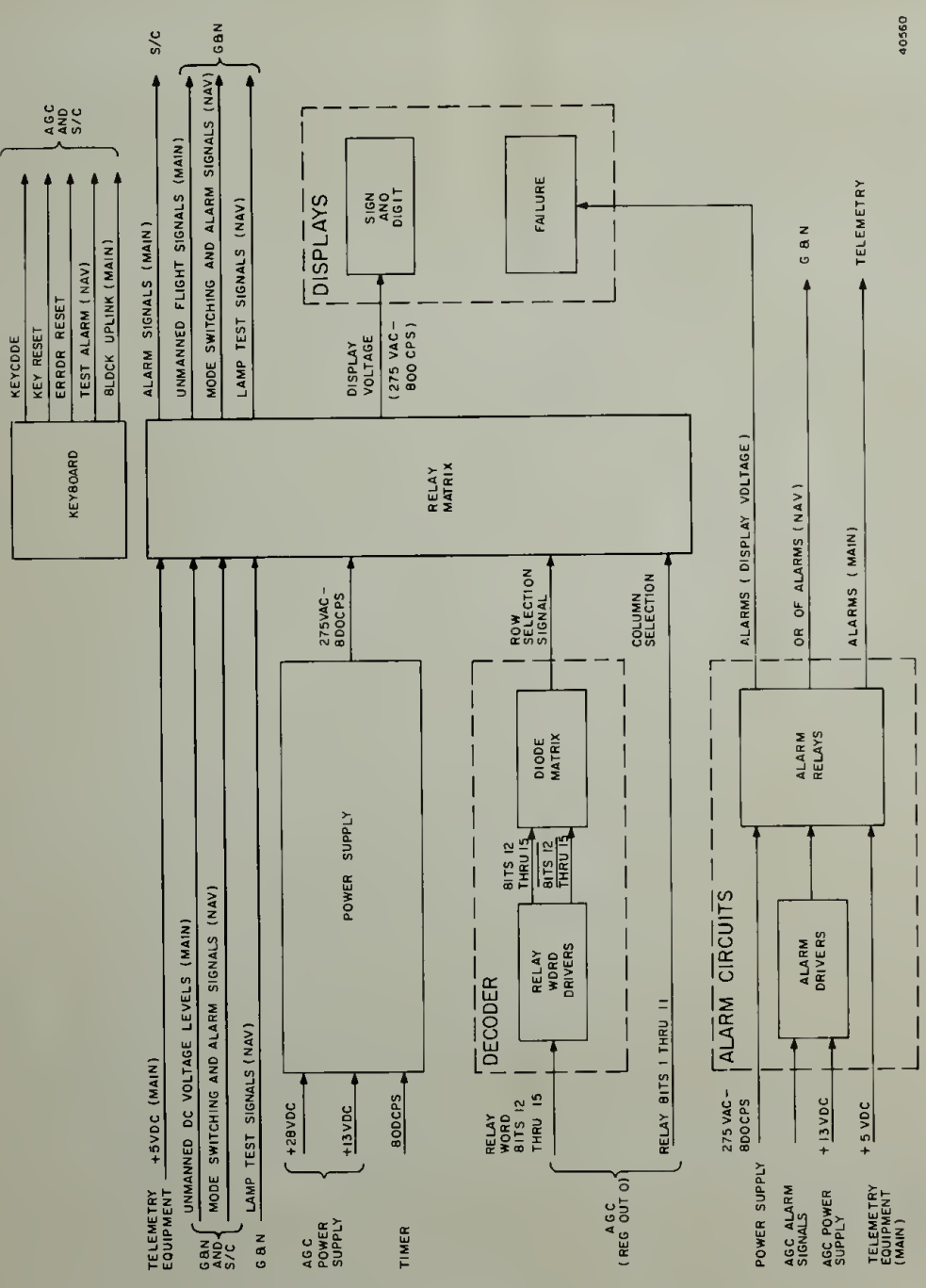

Figure 4-227. DSKY's, Functional Diagram

The relay matrix provides unmanned flight signals to the G and N system and alarm signals to the spacecraft. The unmanned flight signals (voltage levels) specify +X TRANSLATION, COMM MOD-SERVICE MOD SEPARATE, G/N ENTRY SELECT, G/N DV SELECT, G/N ATT CONTROL SELECT, TELECOM SWITCH, FDAI ALIGN, GIMBAL MOTOR POWER CENTRAL, AUTO .05G IND, G/N FAIL, ENCODER ZEROING, and C33 conditions. The alarm signals (telemetry voltage levels) specify CDU, PIPA, and IMU fail indications.

The alarm circuits receive all AGC alarm signals. Each alarm signal is applied to a driver circuit and associated relay. When a relay is energized, it allows the voltage from the power supply or telemetry equipment to be routed to the proper equipments. The voltage from the power supply to the AGC main panel DSKY is applied to the COMP FAIL indicator. When this indicator is illuminated, it indicates one of seven alarms: TC TRAP, RUPT LOCK, COUNTER, PARITY, SCALER, PROGRAM, or CHECK FAIL indication. The voltage from telemetry through the AGC main panel DSKY alarm circuits is used to indicate KEY RLSE, COMPUTER ACTIVITY, and TEL FAIL, in addition to the seven alarms described above.

The displays consist of sign and digital (operational and data display) and failure indicators. The sign and digital indicators allow the astronaut to observe the data entered or requested via the keyboard. The failure indicators present an indication of any hardware failures.

4-9.2 AGC MAIN PANEL DSKY DETAILED DESCRIPTION. The AGC main panel DSKY consists of a keyboard and display, decoder, relay matrix, alarm circuits, displays and indicators, and power supply.

4-9.2.1 Keyboard and Display. The AGC main panel DSKY (figure 4-228) contains 10 digit keys (0 through 9) and 8 operational keys (ERROR RESET, KEY RLSE, ENTER, NOUN, VERB, CLEAR, +, and -). Each of these 18 keys, when pressed, generates a different five-bit binary keycode which is applied to register IN 0 of the input-output section and to the keycode trap circuit of priority control.

The key contacts (figure 4-229) are connected in series to insure that only one keycode will be produced at one time. The binary keycode is produced by applying +13 vdc through the key contacts to a diode network. Table 4-XXVII illustrates the relationship between the keys and their keycodes. The keycode initiates a program interruption (KEYRUPT) in priority control. At the same time transistor Q1 (figure 4-229) is turned off. When the key is released, transistor Q1 is turned on, producing a key reset signal (KYRST 1) which resets the keycode trap circuit of priority control. A key must be released before another key is pressed in order to have information processed by the AGC.

The AGC main panel DSKY display (figure 4-228) contains 24 digit displays (21 for numerical and 3 for sign) and 4 indicators. The 24 digit displays are arranged in three data display registers (REG 1, REG 2, and REG 3), a VERB-NOUN register (REG 4),

RELAY MATRIX CODES

Row Select	REGISTER OUT0 BITS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	RLY WD				RLY BITS											
1	0	0	0	1	R3 -	Reg 3			Pos 2		Reg 3			Pos 1		
2	0	0	1	0	R3 +	Reg 3			Pos 4		Reg 3			Pos 3		
3	0	0	1	1		Reg 2			Pos 1		Reg 3			Pos 5		
4	0	1	0	0	R2 -	Reg 2			Pos 3		Reg 2			Pos 2		
5	0	1	0	1	R2 +	Reg 2			Pos 5		Reg 2			Pos 4		
6	0	1	1	0	R1 -	Reg 1			Pos 2		Reg 1			Pos 1		
7	1	1	0	0				IMU FAIL	PIPA FAIL	CDU FAIL	ENCODER ZEROING					
8	0	1	1	1	R1 +	Reg 1			Pos 4		Reg 1			Pos 3		
9	1	0	0	0	UPLINK	SPARES					Reg 1			Pos 5		
10	1	0	0	1		Noun			Pos 2		Noun			Pos 1		
11	1	0	1	0	FLASH	Verb			Pos 2		Verb			Pos 1		
12	1	0	1	1		Program			Pos 2		Program			Pos 1		
13	1	1	1	0	C33	C32	C31	C30	C29	C28	C27	C26	C25	C24	C23	

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Figure 4-228. AGC Main Panel DSKY

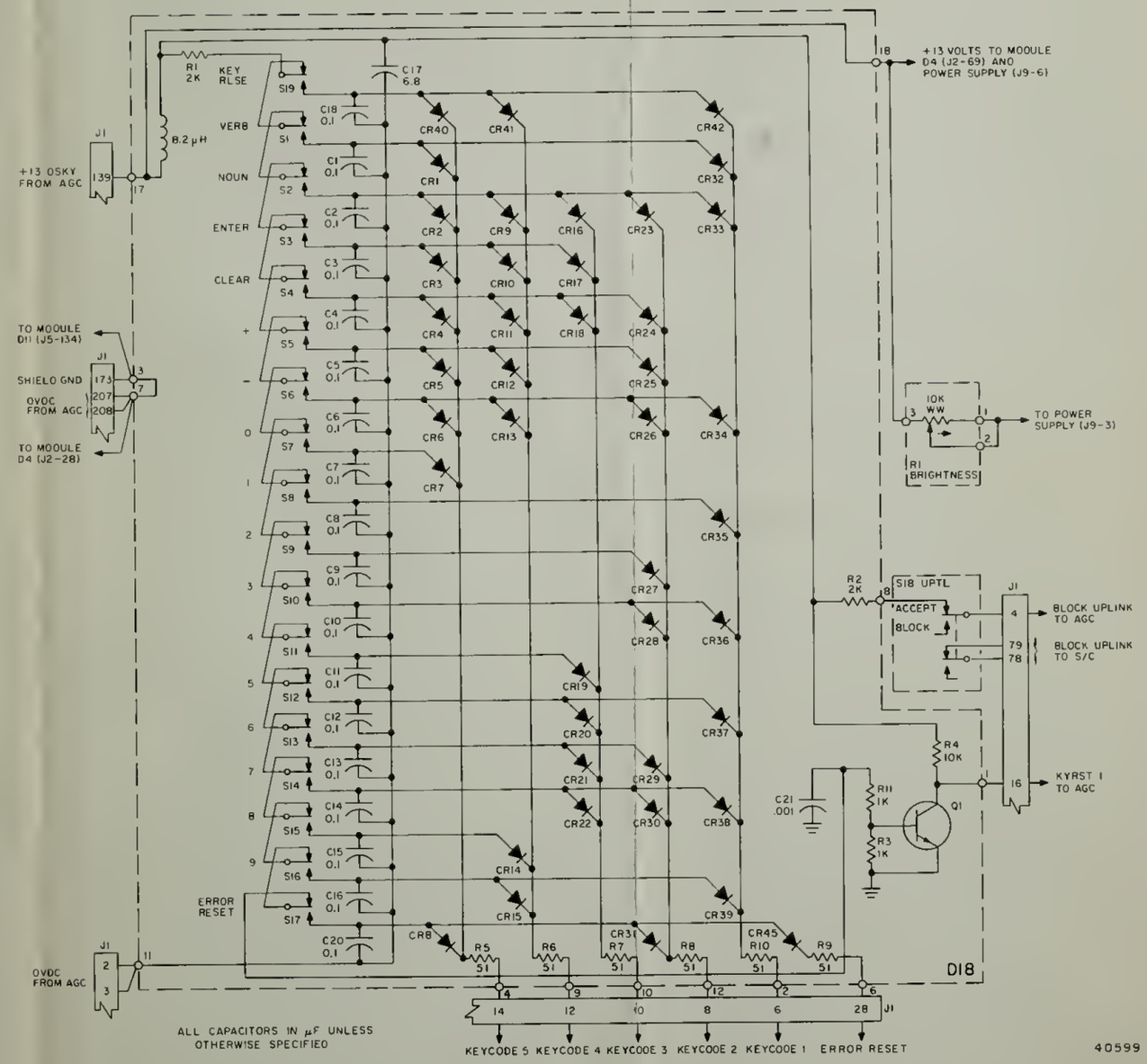


Figure 4-229. AGC Main Panel DSKY, Schematic Diagram

Table 4-XXVII. Keys and Keycode

Digit Key	Keycode	Operational Key	Keycode
1	00001	VERB	10001
2	00010	ERROR RESET	10010
3	00011	KEY RLSE	11001
4	00100	+	11010
5	00101	-	11011
6	00110	ENTER	11100
7	00111	CLEAR	11110
8	01000	NOUN	11111
9	01001		
0	10000		

and a PROGRAM register (REG 5). The four indicators are arranged as follows: UPTL (uplink) and COMP activity (REG 5), and KEY RLSE and COMP FAIL (REG 6). The standard procedure for communicating with the AGC is to press seven keys in the following sequence: VERB-DIGIT-DIGIT, NOUN-DIGIT-DIGIT, ENTER.

Pressing the VERB key on the keyboard clears the VERB displays on the display and indicators (REG 4). The next two digits punched in are interpreted as a VERB code and displayed in the VERB section of (REG 4). This same operation occurs using the NOUN and two digits. The operation of the VERB-NOUN code is not initiated in the AGC until key ENTER is pressed. If an error is noticed in either the VERB or CODE before ENTER is pressed, it may be corrected by repunching either the VERB or NOUN key and the correct code.

If the VERB-NOUN combination punched in requires additional data to be furnished by the astronaut, the VERB and NOUN displays flash approximately once every second after the ENTER key has been pressed. The flashing indicates to the astronaut that he should punch in the required data on the keyboard. The data word is displayed in one of the three display registers (REG 1, REG 2, or REG 3). After punching in the required data and pressing the ENTER key, the flashing ceases.

Two types of data words can be punched in, octal data words and decimal data words. The AGC assumes that an octal data word will be entered if a sign key (+ or -) is not pressed. If digit key 8 or 9 is pressed while loading an octal data word, an alarm is actuated and indicator COMP FAIL (REG 6) is turned on. Whenever key (+) or key (-) is pressed, the corresponding sign is displayed and the AGC assumes that a decimal word is to be entered. If an error is noticed while punching in either octal or decimal data, the CLEAR key can be pressed, and the correct entry can be made provided the ENTER key has not been pressed. All data words entered must be either octal or decimal; combinations of octal and decimal are not permitted.

The ERROR RESET key is pressed whenever the COMP FAIL indicator is on. It may be used to test for the presence of a continuous alarm rather than a transient alarm. In addition to a keycode, the ERROR RESET key initiates a light reset signal (LTRST) in the AGC. Signal LTRST resets the alarm flip-flops in the alarm control section of input-output. The keycode, through AGC operation, will disable the alarm signals associated with register OUT 1. When the above is accomplished it will extinguish the COMP FAIL indicator on the AGC main panel DSKY.

When the AGC wants to display information while it is under astronaut control, the KEY RLSE indicator (REG 6) is turned on. By pressing the KEY RLSE key the astronaut can make the AGC main panel DSKY available for AGC use.

The computer activity indicator (REG 5) is on while the AGC is in operation.

The PROGRAM display (REG 5) is a two digit function or functions of the program being executed in the AGC.

The up-telemetry (UPTL) switch controls the reception of UPLINK information to the AGC. The UPTL indicator (REG 5) is only on when the UPTL switch is in the accept position and UPLINK information is present.

The BRIGHTNESS control adjusts the brightness of all displays and indicators.

4-9.2.2 Decoder. The decoder (figure 4-230) contains four relay word drivers, a diode matrix, and thirteen row select drivers. The relay word drivers receive bits 15 through 12 of register OUT 0. Combinations of these four bits will select one of thirteen rows of relays in the relay matrix. The thirteen code combinations from register OUT 0 are shown beside their particular row selection number on figure 4-230. For simplification, only the selection of row 1 will be discussed. The code for row 1 selection (0001) is inverted in the interface circuits and applied to circuits 90624 through 90627. Thus, circuits 90624 through 90626 will receive a logic ONE and circuit 90627 will receive a logic ZERO. A logic ONE shuts off transistor Q1, which holds transistor Q2 off and allows transistor Q3 to conduct. Therefore, signals RLYWD4, RLYWD3, RLYWD2, and RLYWD1 are logic ONE's and signals $\overline{\text{RLYWD4}}$, $\overline{\text{RLYWD3}}$, $\overline{\text{RLYWD2}}$, and $\overline{\text{RLYWD1}}$ are logic ZERO's.

The diode matrix receives the 8 bit output from the four relay word drivers. The matrix is wired in such a manner that each 8 bit input produces a logic ONE on only one output line (J3 pins). For the selection of row 1, diodes CR1, CR2, CR23, and CR24 must be reverse biased. When these diodes are not conducting, row select driver circuit (90642) will be activated. A current path is provided from +13 vdc through R1, CR1, and R2 to 0 vdc. Thus, parallel transistors Q1 and Q2 will conduct and supply 0 vdc (representing row 1 selection) to the relay matrix.

4-9.2.3 Relay Matrix. The relay matrix (figure 4-231) consists of 11 relay bit drivers and 13 rows of 11 relays. Each relay bit driver accepts 1 of 11 bits (11 through 1) of register OUT 0. For simplification, only bit 11 (circuit 90612) will be discussed. When bit 11 of register OUT 0 is a ONE, it is inverted in the interface circuits and applied to

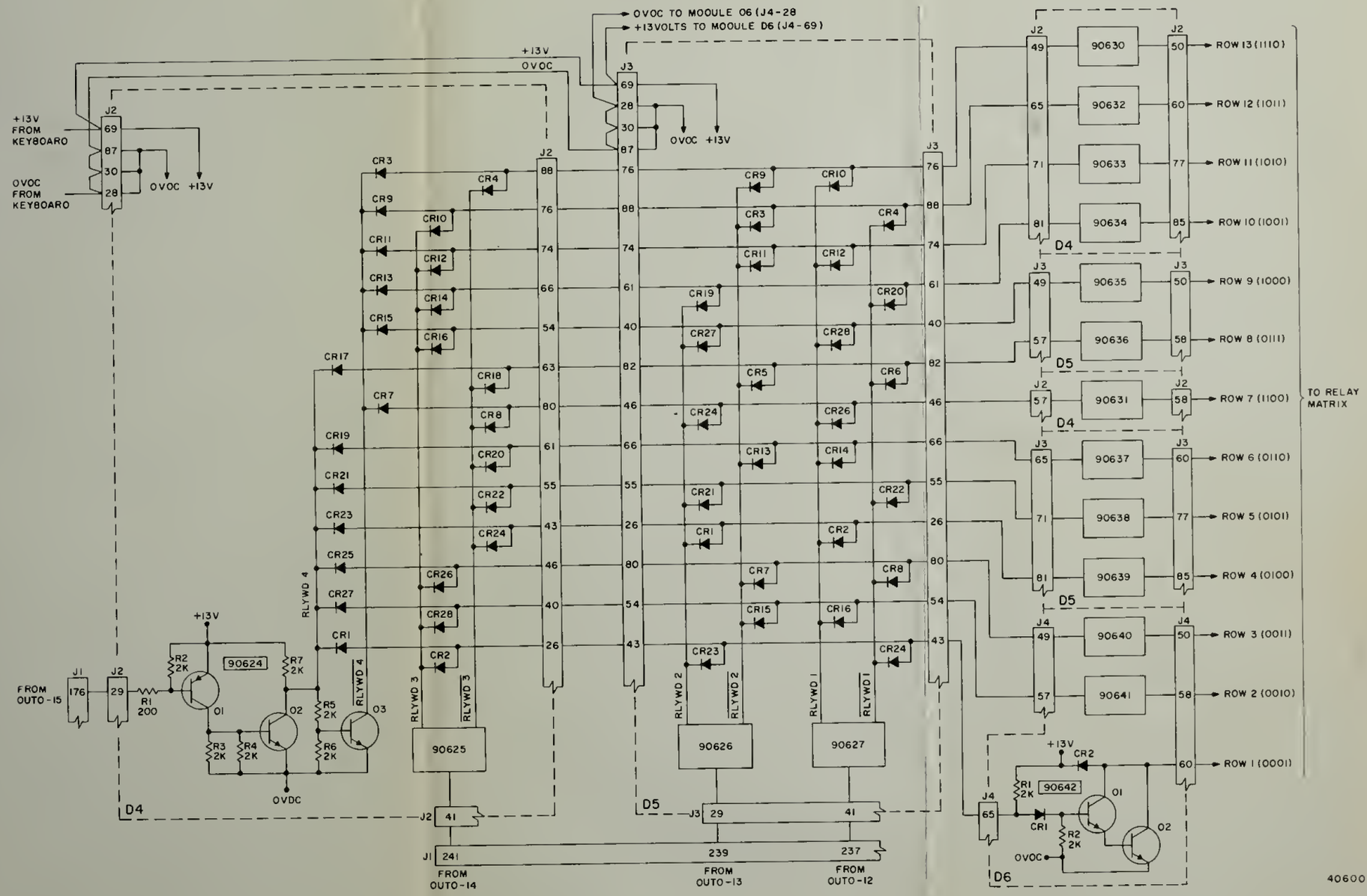


Figure 4-230. Decoder, AGC Main Panel DSKY

MODULE	CONNECTOR
D4	J2
D5	J3
D6	J4
D11	J5
D12	J6
D13	J7
D14	J8

"C" RELAYS - C23 THRU C33

* SIGNALS TO TELEMETRY

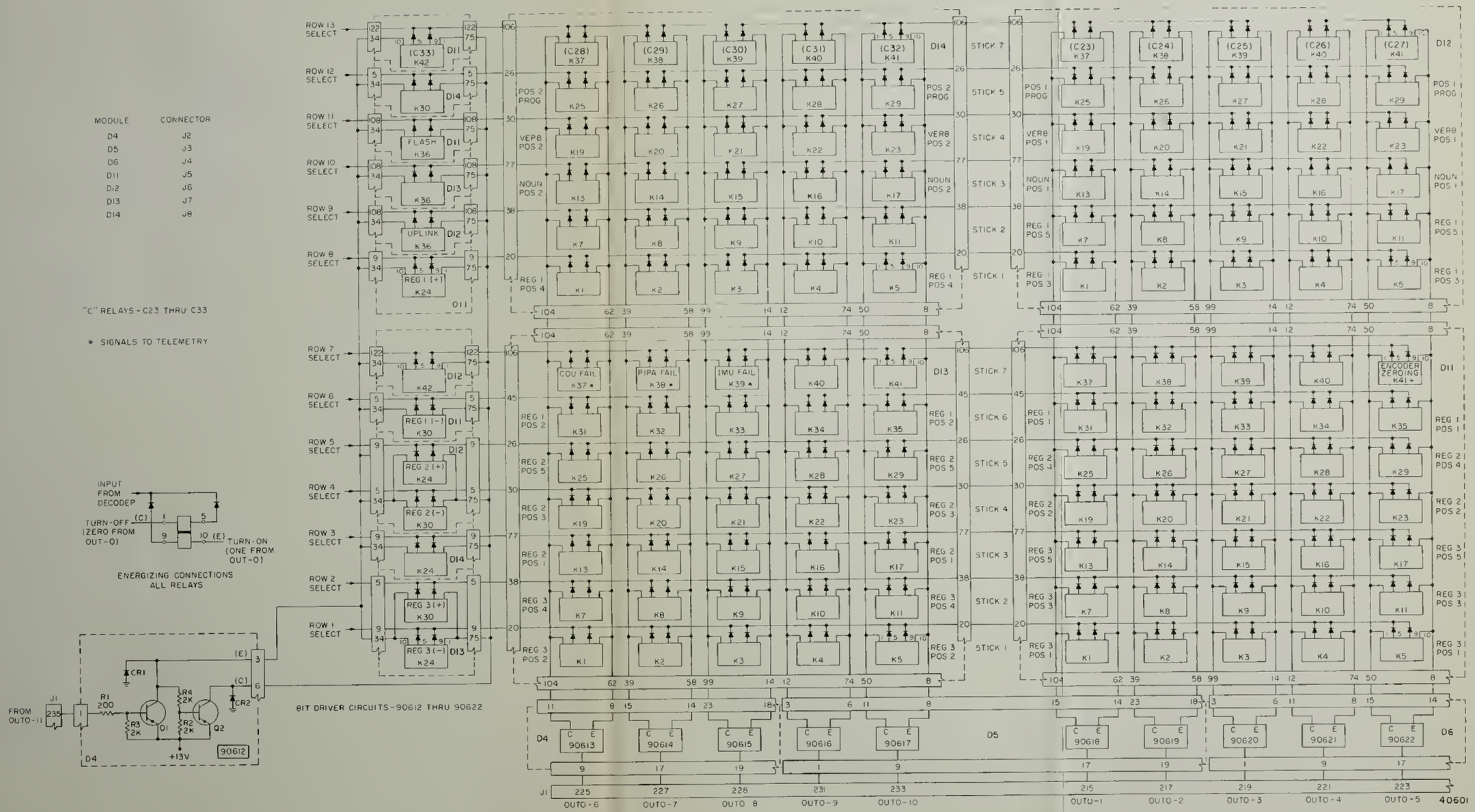


Figure 4-231. Relay Matrix, AGC Main Panel DSKY

transistor Q1. This input turns on transistor Q1 which will then switch transistor Q2 off. Thus, +13 vdc is present at output E (TURN-ON) of circuit 90612, and is applied to a column of 13 relays. Therefore, with a row selection signal from the diode matrix and a column select signal from a relay bit driver a single relay within the relay matrix is controlled.

Eleven of the 13 rows of relays control the DSKY displays, and the other two (rows 7 and 13) supply signals to the G and N system and the spacecraft. All the relays in the relay matrix are of the latching type. Table 4-XXVIII relates the content of register OUT 0 to the selected relay bank and to the digit display controlled by relays within the bank. Five relays are required to display one digit. Relay bit drivers 10 through 6 control the display of one digit and relay bit drivers 5 through 1 control the display of a second digit. Relay bit driver 11 causes the display of a plus or minus sign, the lighting of the UPTL activity indicator (UPLINK), or the flashing of the NOUN and VERB indicators, depending on which row has been selected. The five bit code necessary to display digits 0 through 9 in any display location is listed in table 4-XXIX. The relays of row 1 are used as an example. For identification of display locations, refer to figure 4-232.

Energizing the proper relays within the relay matrix (rows 1 through 6 and 8 through 12) allows approximately 250 vac (display voltage) from the DSKY power supply to be routed through the relay contacts to the various segments of the electroluminescent digit and sign indicators. Figure 4-233 illustrates the relays, their codes, and a display coding key. Timing signal ACTREQ (action request), which is approximately 1 cps, initiates the VERB-NOUN flash. Signal ACTREQ is applied through a driver circuit and relay K36 (when energized) to the VERB-NOUN relays. For simplification, figure 4-233 is used to illustrate both main and navigation DSKY relay matrix display operation.

The two relay rows associated with the G and N system and the spacecraft (rows 13 and 7 respectively) are unlike the display relays in that each relay has a separate function as illustrated on figure 4-234. The 11 relays (one spare), associated with the G and N system are termed the C relays (C23 through C33) and are also referred to as unmanned flight signals. If any of the C relays is energized, the associated signal is sent to the G and N system and an OR signal (+13 vdc) is generated and supplied to bit 15 of register IN 3 of input-output in the AGC. The 11 relays (7 spares) associated with the spacecraft supply three failure indications (IMU, PIPA, and CDU) and signal ENCODER ZEROING to the spacecraft telemetry. The three failure indications are also supplied to the condition annunciator on the G and N indicator control panel.

4-9.2.4 Alarm Circuits. The alarm circuits (figure 4-235) consist of alarm drivers and associated relays. All relays in the alarm circuits are nonlatching.

The alarm circuits accept alarm signals from register OUT1 and the alarm control section of input-output, and operational signals from register OUT 1. The alarm signals from register OUT 1 are CHECK FAIL, TL FAIL, and PROG ALM. The alarm signals

Table 4-XXVIII. Display Codes

Row Select	REGISTER OUT 0 BITS														
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	RLY WD				RLY BITS										
1	0	0	0	1	R3 −	Reg 3		Pos 2			Reg 3		Pos 1		
2	0	0	1	0	R3 +	Reg 3		Pos 4			Reg 3		Pos 3		
3	0	0	1	1		Reg 2		Pos 1			Reg 3		Pos 5		
4	0	1	0	0	R2 −	Reg 2		Pos 3			Reg 2		Pos 2		
5	0	1	0	1	R2 +	Reg 2		Pos 5			Reg 2		Pos 4		
6	0	1	1	0	R1 −	Reg 1		Pos 2			Reg 1		Pos 1		
7	1	1	0	0				IMU FAIL	PIPA FAIL	CDU FAIL	ENCODER ZEROING				
8	0	1	1	1	R1 +	Reg 1		Pos 4			Reg 1		Pos 3		
9	1	0	0	0	UPLINK	SPARES					Reg 1		Pos 5		
10	1	0	0	1		Noun		Pos 2			Noun		Pos 1		
11	1	0	1	0	FLASH	Verb		Pos 2			Verb		Pos 1		
12	1	0	1	1		Program		Pos 2			Program		Pos 1		
13	1	1	1	0	C33	C32	C31	C30	C29	C28	C27	C26	C25	C24	C23

Table 4-XXIX. Digit Code

Relays					Digit Displayed
K5	K4	K3	K2	K1	
K10	K9	K8	K7	K6	
0	0	0	0	0	Blank
1	0	1	0	1	0
0	0	0	1	1	1
1	1	0	0	1	2
1	1	0	1	1	3
0	1	1	1	1	4
1	1	1	1	0	5
1	1	1	0	0	6
1	0	0	1	1	7
1	1	1	0	1	8
1	1	1	1	1	9

from the alarm control are TC TRAP, RUPT LOCK, COUNTER FAIL, PARITY FAIL, and SCALER FAIL. The operational signals from register OUT 1, are KEY RELEASE and COMPUTER ACTIVITY. Although the KEY RELEASE signal lights an indicator grouped with the failure indicators, it does not indicate a failure. The signal indicates a request by the AGC to the astronaut that it wishes to display information. Signal COMPUTER ACTIVITY indicates that the AGC is operating. If a dummy job is being executed (AGC is idle) the COMP activity indicator is off.

All of the alarm and operational signals illustrated on figure 4-235 are forwarded to spacecraft telemetry via J1. These signals are +5 vdc levels sent to the alarm circuits from telemetry. The alarm signals, except TL FAIL, are also OR'ed to light the COMP FAIL indicator.

4-9.2.5 Displays and Indicators. The displays and indicators (figure 4-228) are luminescent coated glass assemblies which glow when a voltage is applied to the coating. The displays (digit and sign) are segmented and the display voltage (approximately 250 vac) is applied to each segment. The indicators are made in one piece and the display voltage is applied to each indicator. The brightness of the displays and indicators varies as a function of the voltage and frequency applied to the coating. The voltage can be varied using the BRIGHTNESS control on the front panel of the AGC main panel DSKY (figure 4-228).

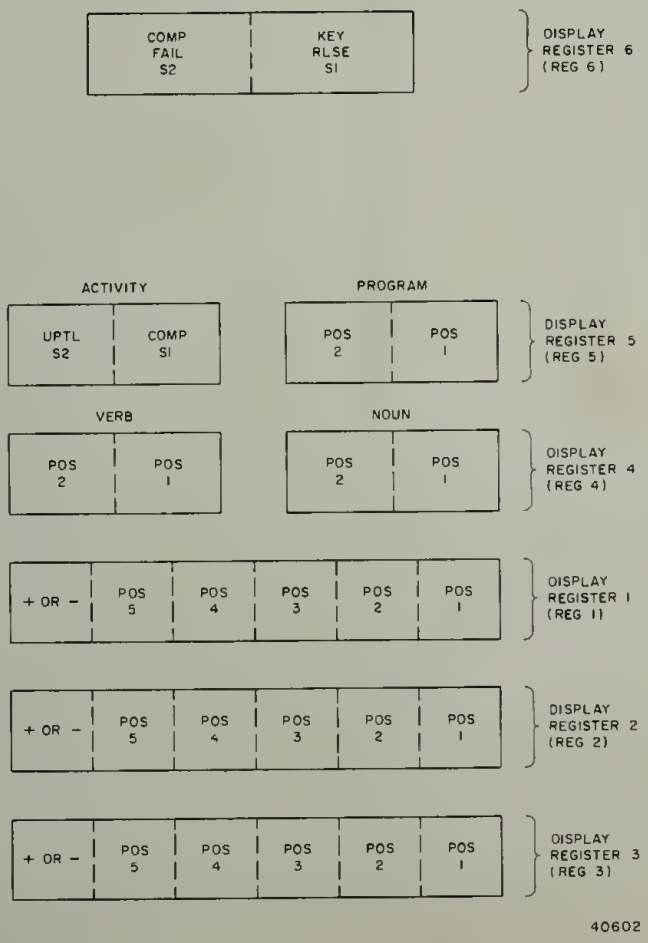
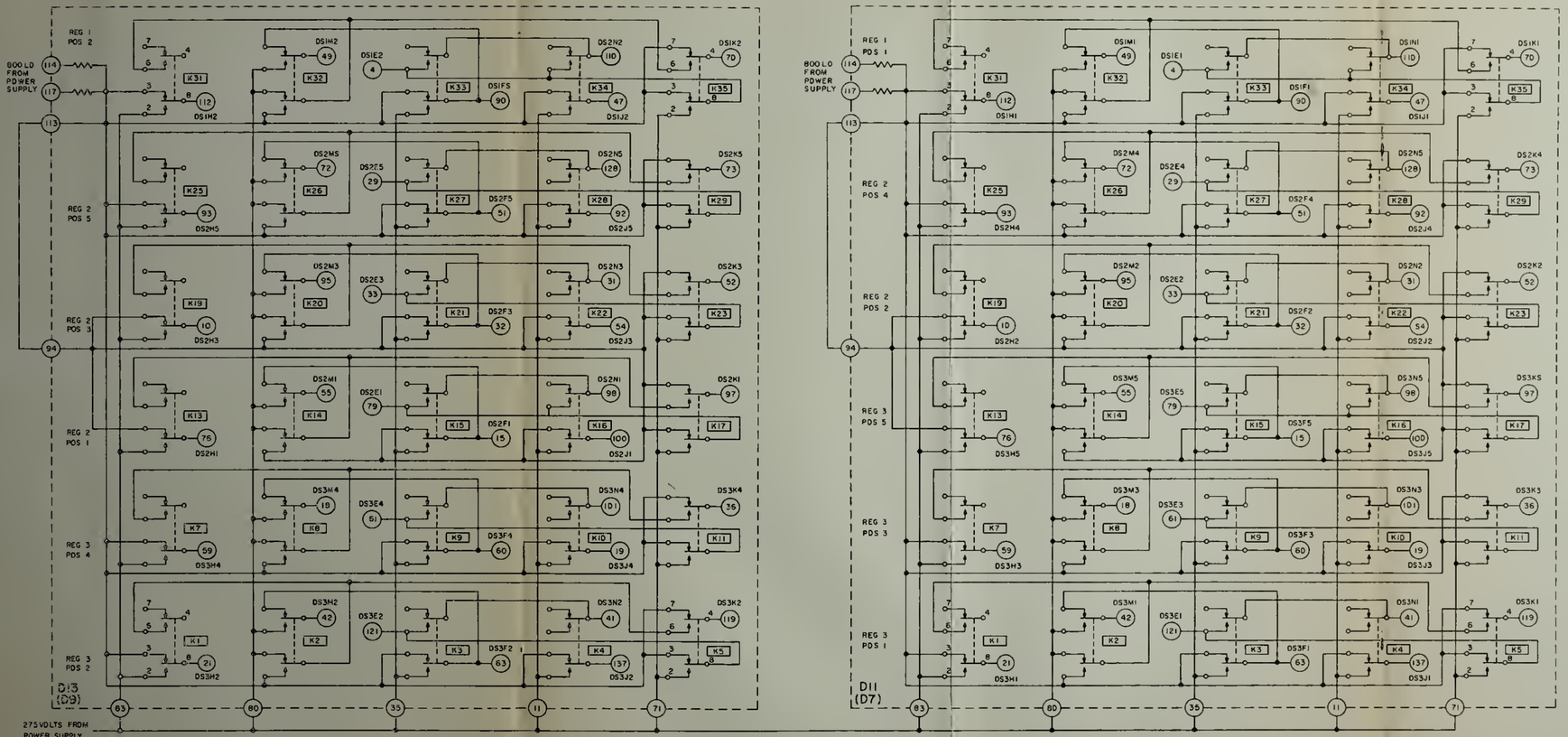
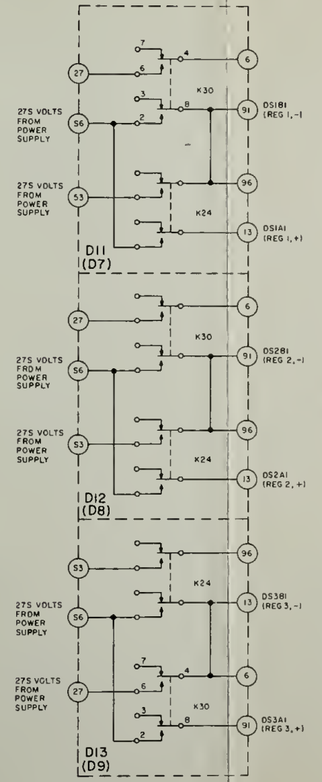
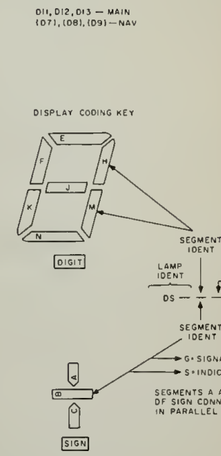


Figure 4-232. Display Locations, AGC Main Panel DSKY

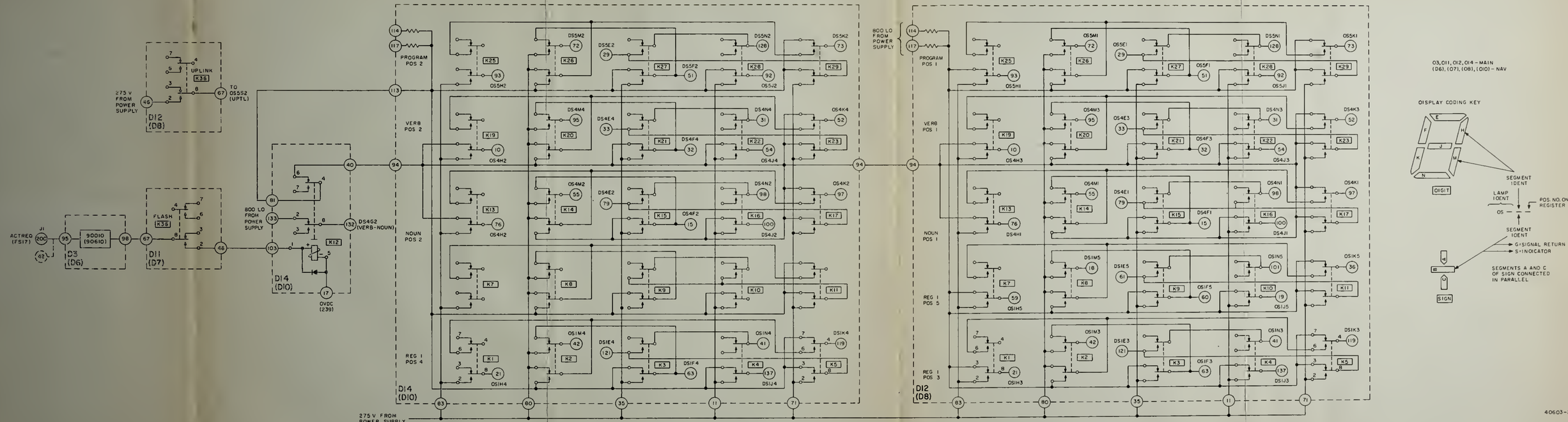






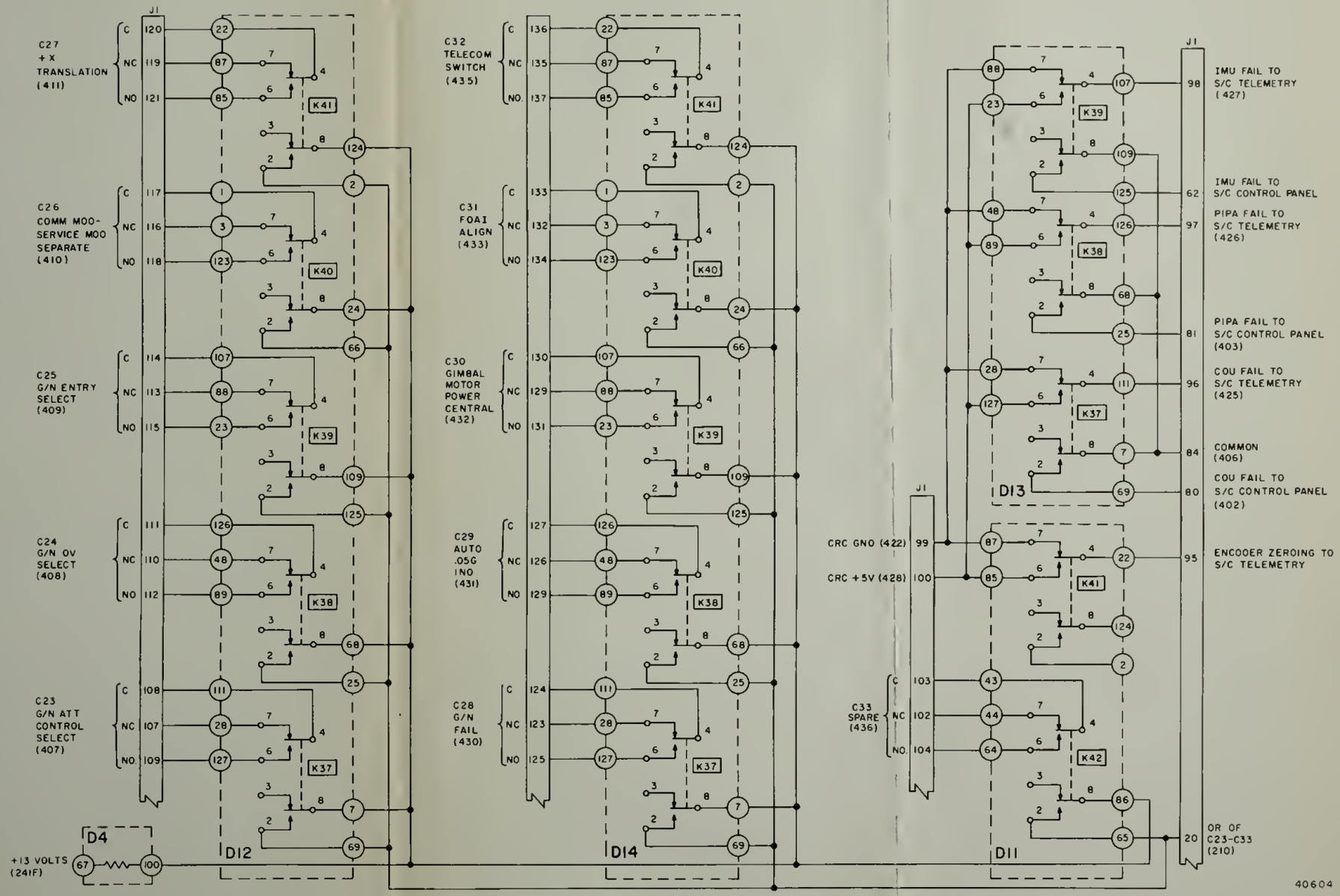
40603-1

Figure 4-233. Relay Matrix Display Connections (Sheet 1 of 2)



40603-2

Figure 4-233. Relay Matrix Display Connections (Sheet 2 of 2)



40604

Figure 4-234. G and N System and Spacecraft Relay Functions, AGC Main Panel DSKY

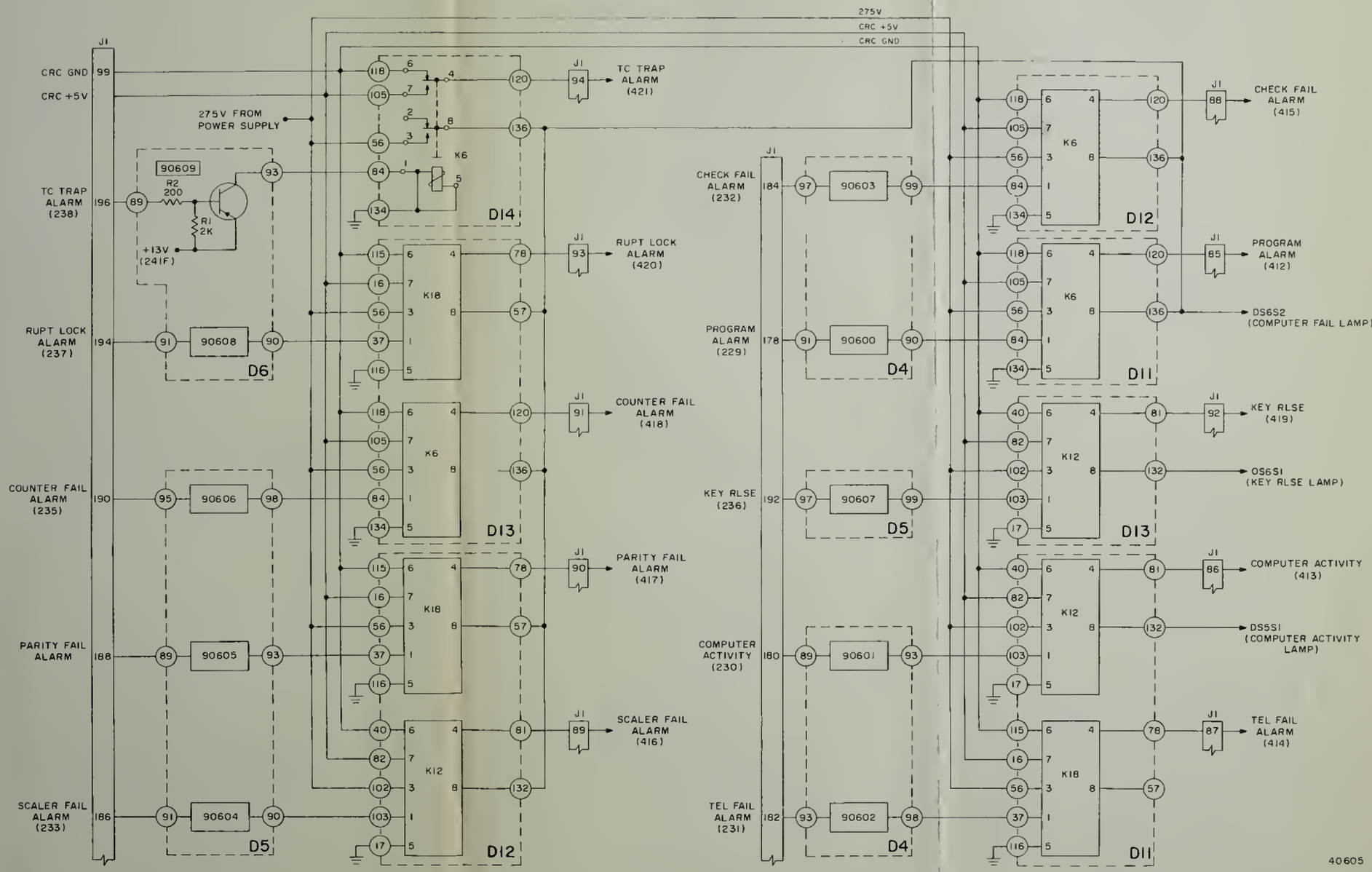


Figure 4-235. Alarm Circuits, AGC Main Panel DSKY

4-9.2.6 Power Supply. The AGC main panel DSKY power supply (figure 4-236) utilizes +13 vdc from the AGC power supply, +28 vdc from the spacecraft electrical power system, and an 800 cps sync signal from the timer to generate an approximate 250 vac 800 cps display voltage. The power supply contains two transformer-coupled, push-pull amplifiers. The input to the first stage is an 800 cps square wave varying about a +13-vdc level. The dc level is controlled by the BRIGHTNESS control on the keyboard. Transformers T1 and T2 step up the voltage applied to their primary windings. The output from the second push-pull stage is applied to the primary of transformer T3.

Transformer T3 is a saturable reactor which regulates the current applied to the displays. The displays act as a variable capacitive load that varies as a function of the number of indicators that are illuminated. Changes in the load are reflected back to the control winding via the full-wave bridge rectifier, CR1 through CR4. As the number of illuminated indicators increases, the reactance of the load decreases, which in turn increases the current applied to the control winding. An increase in current through the control winding drives transformer T3 further into saturation, reducing the current in the secondary and keeping the output relatively constant. If the load decreases, the capacitive reactance increases, the current through the control winding decreases, T3 is less saturated, and the secondary current increases.

4-9.3 AGC NAVIGATION PANEL DSKY FUNCTIONAL DESCRIPTION. The functional description of the AGC navigation panel DSKY is similar to the functional description of the AGC main panel DSKY. The differences, as outlined in the DSKY functional diagram (figure 4-227), are TEST ALARM, OR OF ALARMS, and outputs from the relay matrix. TEST ALARM from the keyboard is sent to the AGC where it generates PARITY, RUPT, TC, and COUNTER FAIL alarms. These alarms will illuminate the appropriate failure indicators on the navigation panel. The OR OF ALARMS to the G and N system from the AGC navigation panel DSKY alarm circuits indicate TC TRAP, RUPT LOCK, COUNTER, PARITY, SCALER, TEL, or CHECK FAIL.

The relay matrix provides mode switching, alarm, and lamp test signals to the G and N system. The mode switching signals specify STAR TRACKER ON, ZERO OPT, ROLL RE-ENTRY, ATTITUDE CONTROL, ZERO ENCODE, COARSE ALIGN, LOCK CDU, FINE ALIGN, and ENCODER ZEROING conditions. The alarm signals which are not determined within the AGC, specify CDU, PIPA, and IMU fail indications, and are not displayed on the DSKY panel. Mode switching and alarm signals to the G and N system are both direct inputs from the G and N system and spacecraft, and row select and column select signals from the AGC. Lamp test signals to the G and N system are direct inputs from the G and N system.

4-9.4 AGC NAVIGATION PANEL DSKY DETAILED DESCRIPTION. The detailed description of the AGC navigation panel DSKY is similar to the detailed description of the AGC main panel DSKY. The differences are outlined in the following paragraphs.

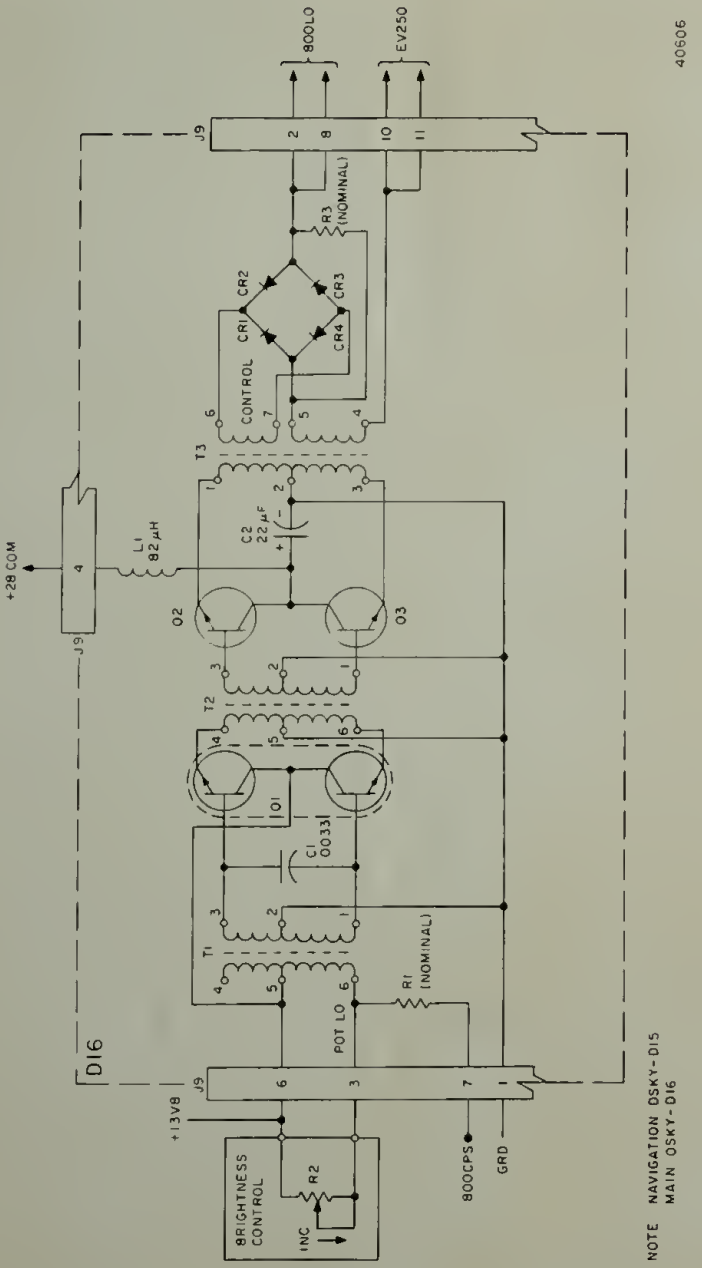


Figure 4-236. Power Supply, AGC Main Panel DSKY

4-9.4.1 Keyboard and Display. The AGC navigation panel DSKY display (figure 4-237) contains the following failure indicators: PROG ALM, COUNTER FAIL, RUPT LOCK, TC TRAP, SCALER FAIL, PARITY FAIL, TL FAIL, and CHECK FAIL. In the AGC main panel DSKY these signals were OR'ed to produce a COMP FAIL indication. However, in the AGC navigation panel DSKY, there is no COMP FAIL indication; the failures are indicated separately.

The AGC navigation panel DSKY (figure 4-237) does not contain an UPTL switch, but it does have an additional key called TEST ALARM. When the TEST ALARM key is pressed, signal TEST ALARMS (figure 4-238) is sent to the AGC and causes the alarm control circuits of input-output to turn on display indicators COUNTER FAIL, RUPT LOCK, TC TRAP, and PARITY FAIL. These indications may be removed by pressing the ERROR RESET key.

4-9.4.2 Decoder. The decoder (figure 4-239) in the AGC navigation panel DSKY contains a difference code for the selection of the relays in row 13 of the relay matrix. The code for row 13 selection is 1101.

4-9.4.3 Relay Matrix. The AGC navigation panel DSKY relay matrix (figure 4-240) contains 11 more C relays than does the AGC main panel DSKY. Each of the 22 relays (C1 through C22) which are also referred to as mode switching and alarm signals, has a separate function as illustrated on figure 4-241. The C relays, when energized, supply a signal to the G and N system and also produce an OR signal (+13 vdc) which is supplied to input-output in the AGC. Table 4-XXX relates the content of register OUT 0 to the selected relay bank and the digit display controlled by relays within the bank. For identification of display locations, refer to figure 4-242.

4-9.4.4 Alarm Circuits. The alarm circuits (figure 4-243) supply the display voltage to the appropriate indicators and an OR OF ALARMS signal to the G and N system.

RELAY MATRIX CODES

Row Select	REGISTER OUTPUT BITS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	RLY WD				RLY BITS											
1	0	0	0	1	R3 -	Reg 3		Pos 2			Reg 3		Pos 1			
2	0	0	1	0	R3 +	Reg 3		Pos 4			Reg 3		Pos 3			
3	0	0	1	1		Reg 2		Pos 1			Reg 1		Pos 5			
4	0	1	0	0	R2 -	Reg 2		Pos 4			Reg 2		Pos 3			
5	0	1	0	1	R2 +	Reg 2		Pos 5			Reg 2		Pos 4			
6	0	1	1	0	R1 -	Reg 1		Pos 2			Reg 1		Pos 1			
7	1	1	0	0	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	
8	0	1	1	1	R1 +	Reg 1		Pos 4			Reg 1		Pos 3			
9	1	0	0	0	UPLINK	SPARES					Reg 1		Pos 5			
10	1	0	0	1		Noun		Pos 2			Noun		Pos 1			
11	1	0	1	0	FLASH	Verb		Pos 2			Verb		Pos 1			
12	1	0	1	1		Program		Pos 2			Program		Pos 1			
13	1	1	0	1	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	

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Figure 4-237. AGC Navigation Panel DSKY

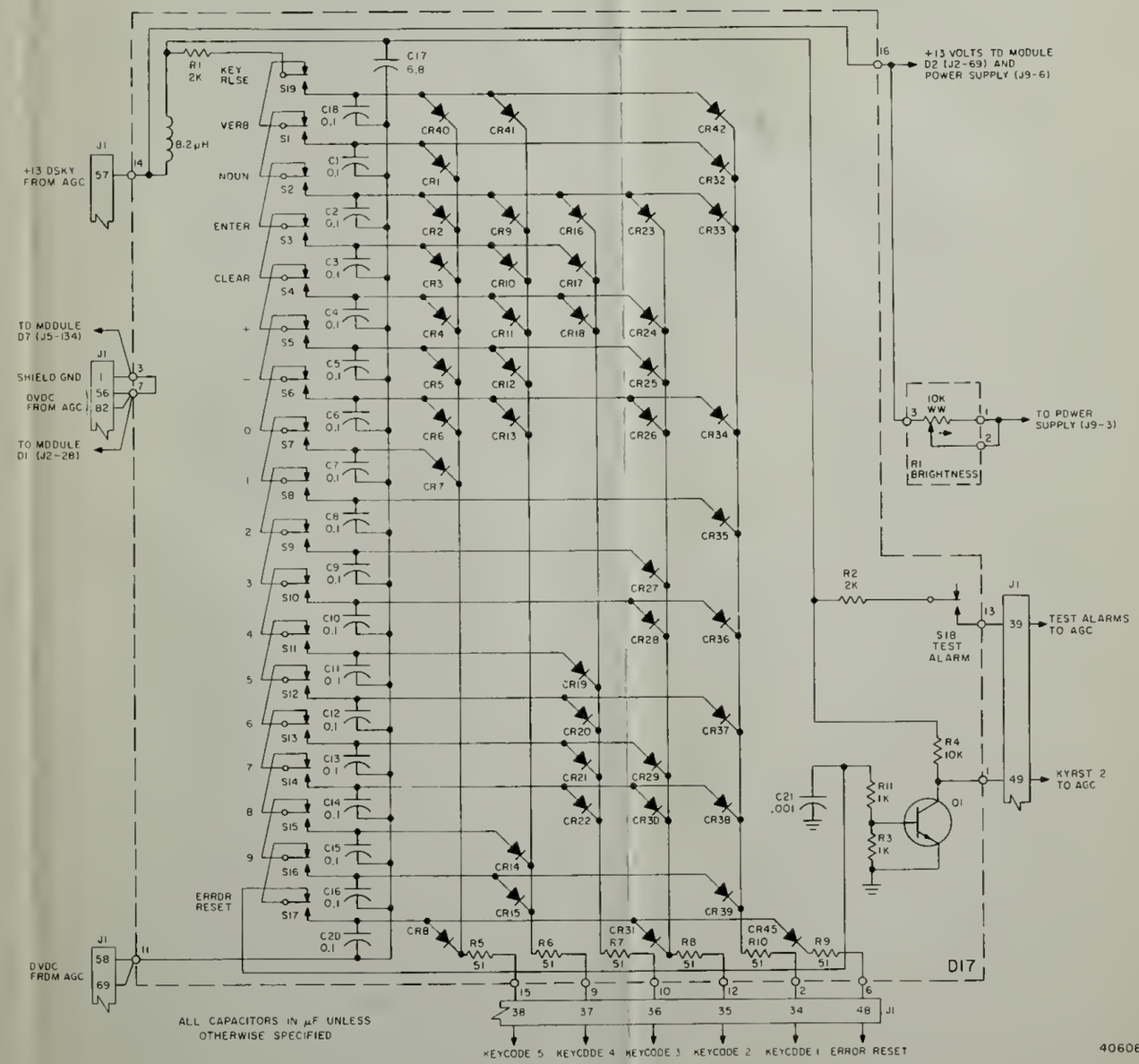

Figure 4-238. AGC Navigation Panel DSKY, Schematic Diagram

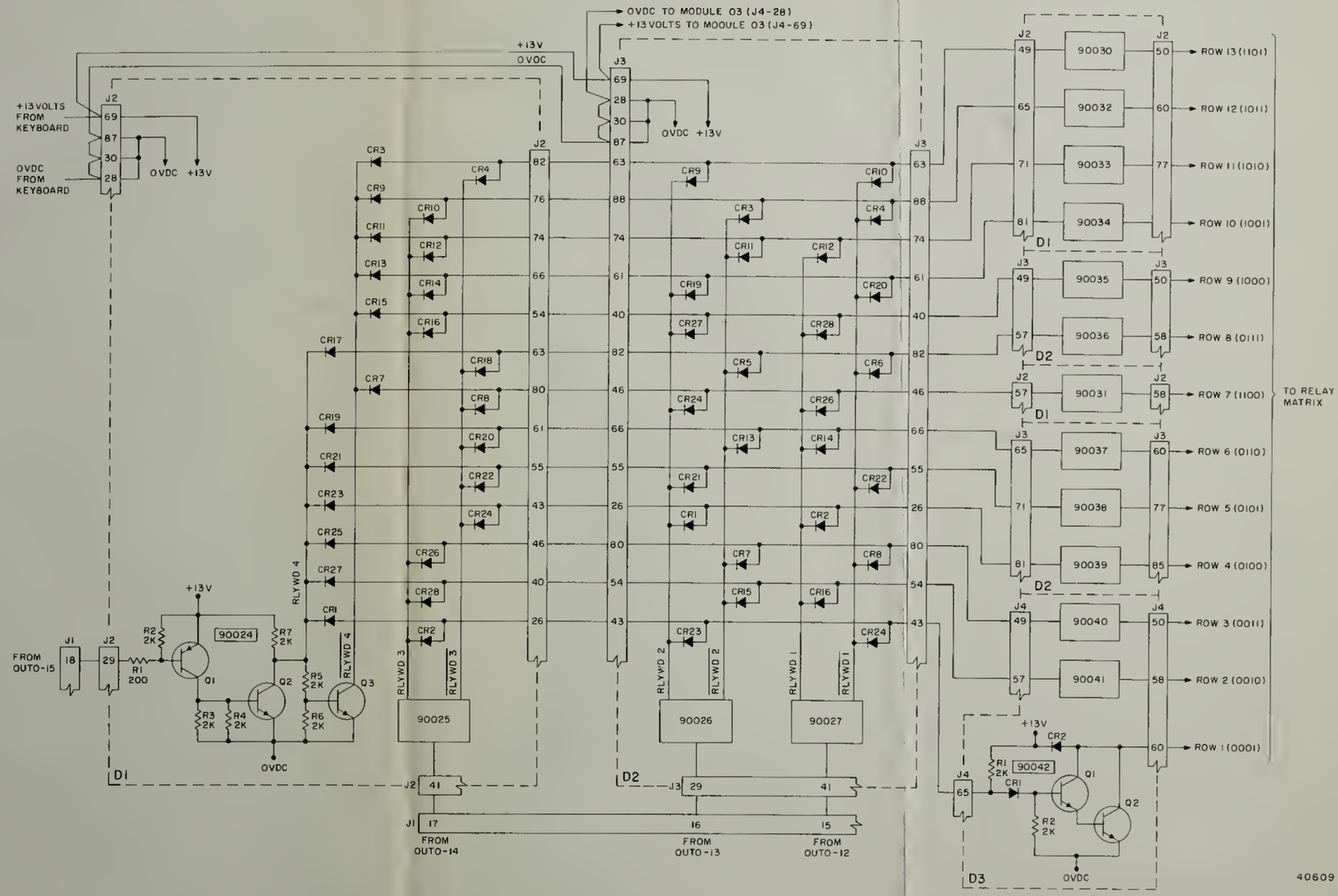

Figure 4-239. Decoder, AGC Navigation Panel DSKY

MDOULE	CONNECTOR
D1	J2
D2	J3
D3	J4
D7	J5
D8	J6
D9	J7
D10	J8

"C" RELAYS - C1 THRU C22

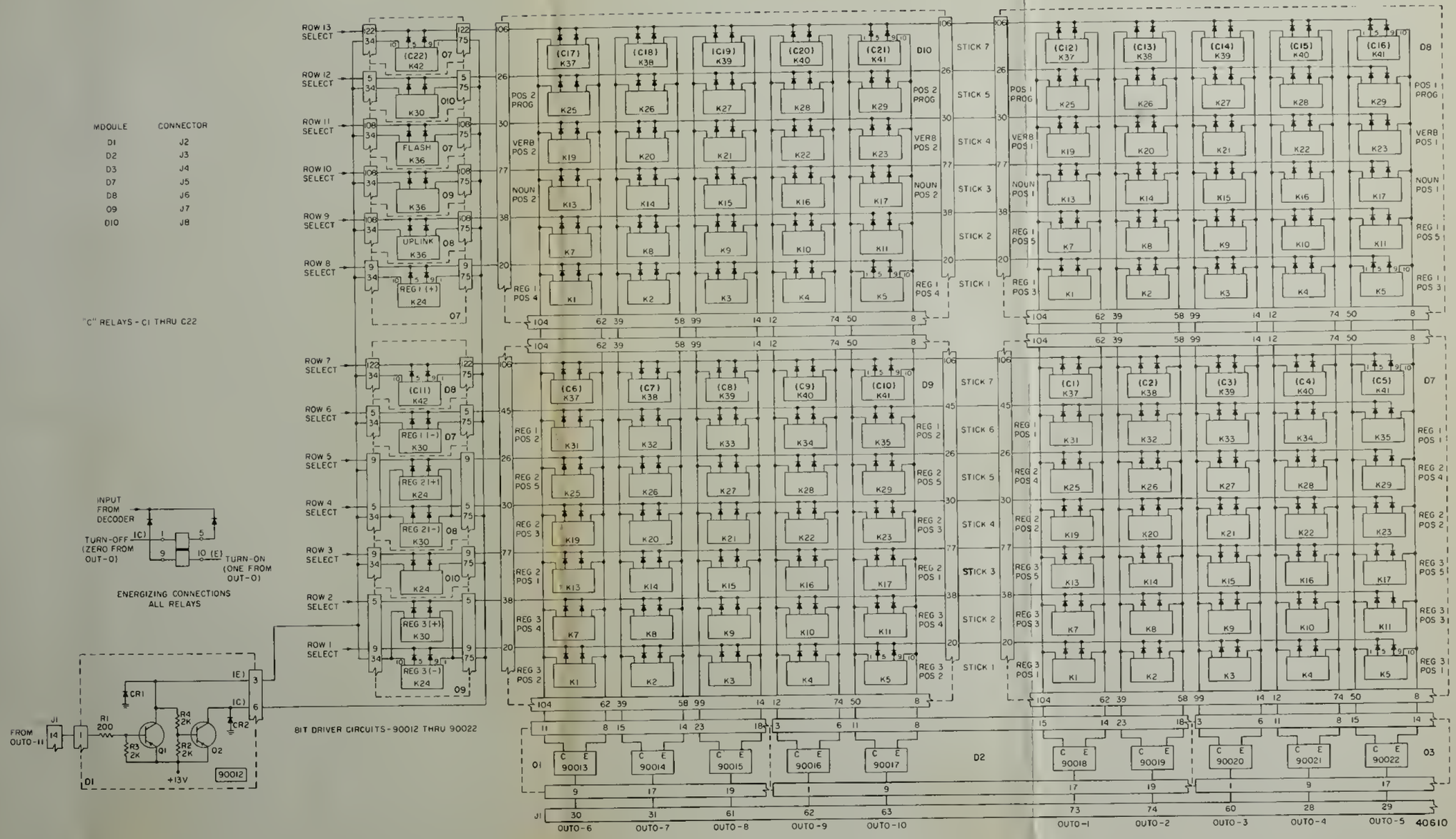

Figure 4-240. Relay Matrix, AGC Navigation Panel DSKY

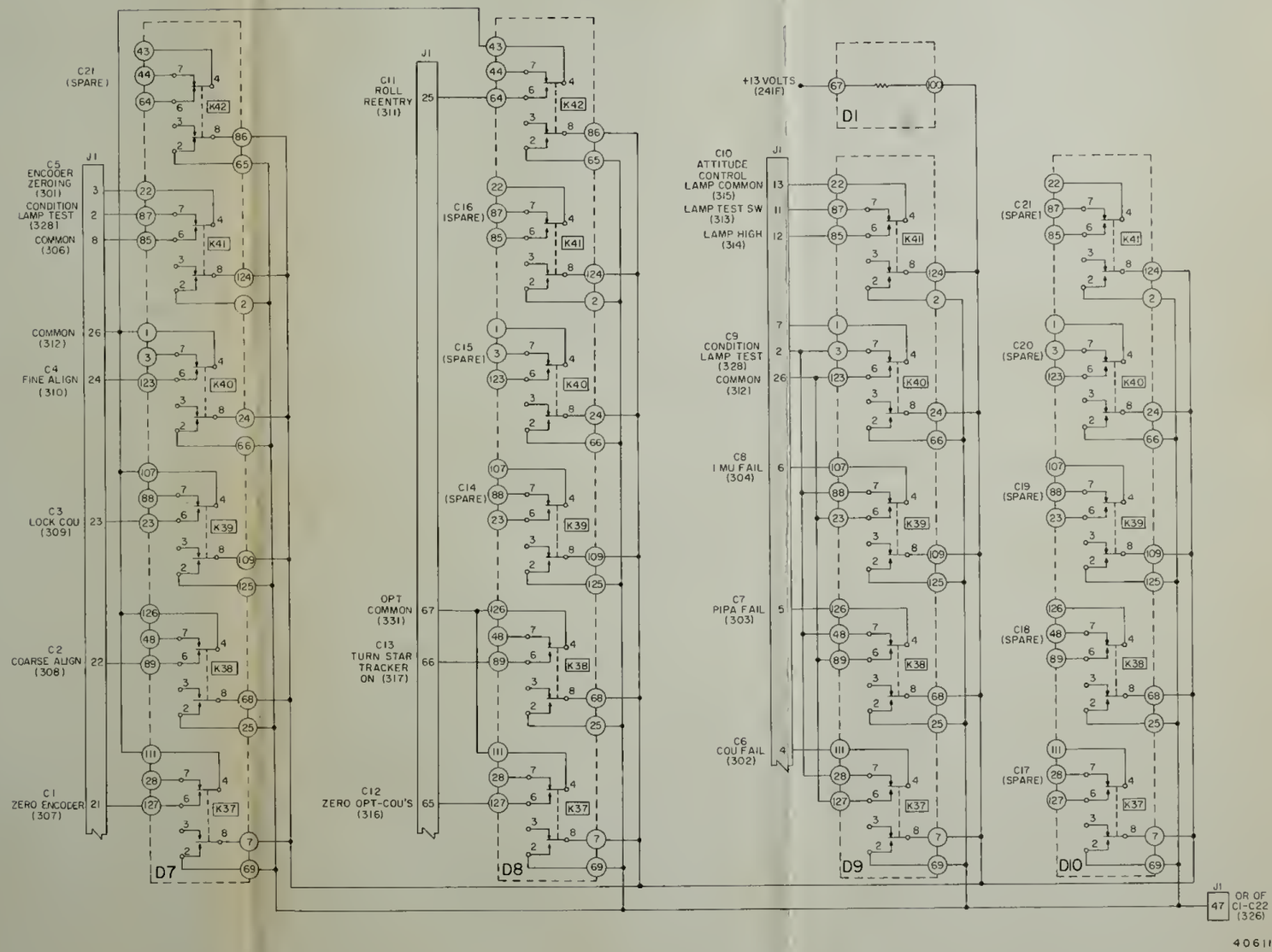

Figure 4-241. G & N System Relay Functions, AGC Navigation Panel DSKY

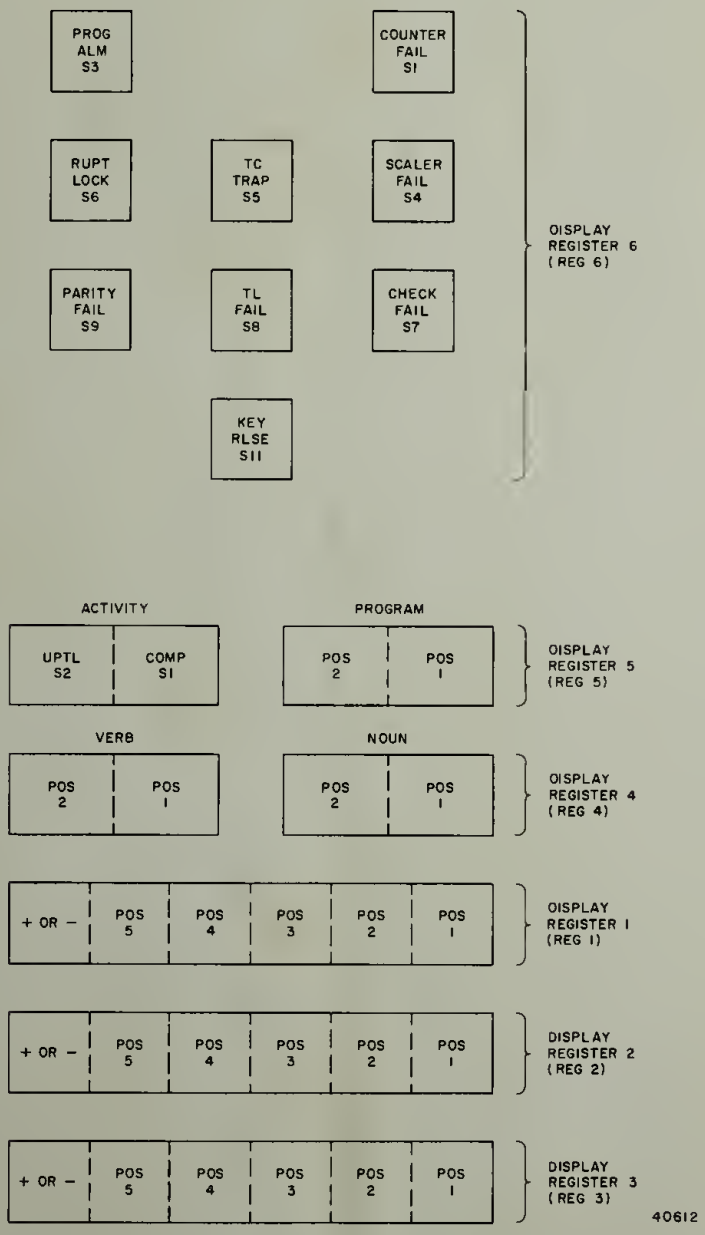

Figure 4-242. Display Locations, AGC Navigation Panel DSKY

Table 4-XXX. Relay Matrix Codes

Row Select	Register OUT 0 Bits														
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	RLY WD				RLY BITS										
1	0	0	0	1	R3 −	Reg 3		Pos 2			Reg 3		Pos 1		
2	0	0	1	0	R3 +	Reg 3		Pos 4			Reg 3		Pos 3		
3	0	0	1	1		Reg 2		Pos 1			Reg 3		Pos 5		
4	0	1	0	0	R2 −	Reg 2		Pos 3			Reg 2		Pos 2		
5	0	1	0	1	R2 +	Reg 2		Pos 5			Reg 2		Pos 4		
6	0	1	1	0	R1 −	Reg 1		Pos 2			Reg 1		Pos 1		
7	1	1	0	0	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
8	0	1	1	1	R1 +	Reg 1		Pos 4			Reg 1		Pos 3		
9	1	0	0	0	UPLINK	SPARES					Reg 1		Pos 5		
10	1	0	0	1		Noun		Pos 2			Noun		Pos 1		
11	1	0	1	0	FLASH	Verb		Pos 2			Verb		Pos 1		
12	1	0	1	1		Program		Pos 2			Program		Pos 1		
13	1	1	0	1	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12

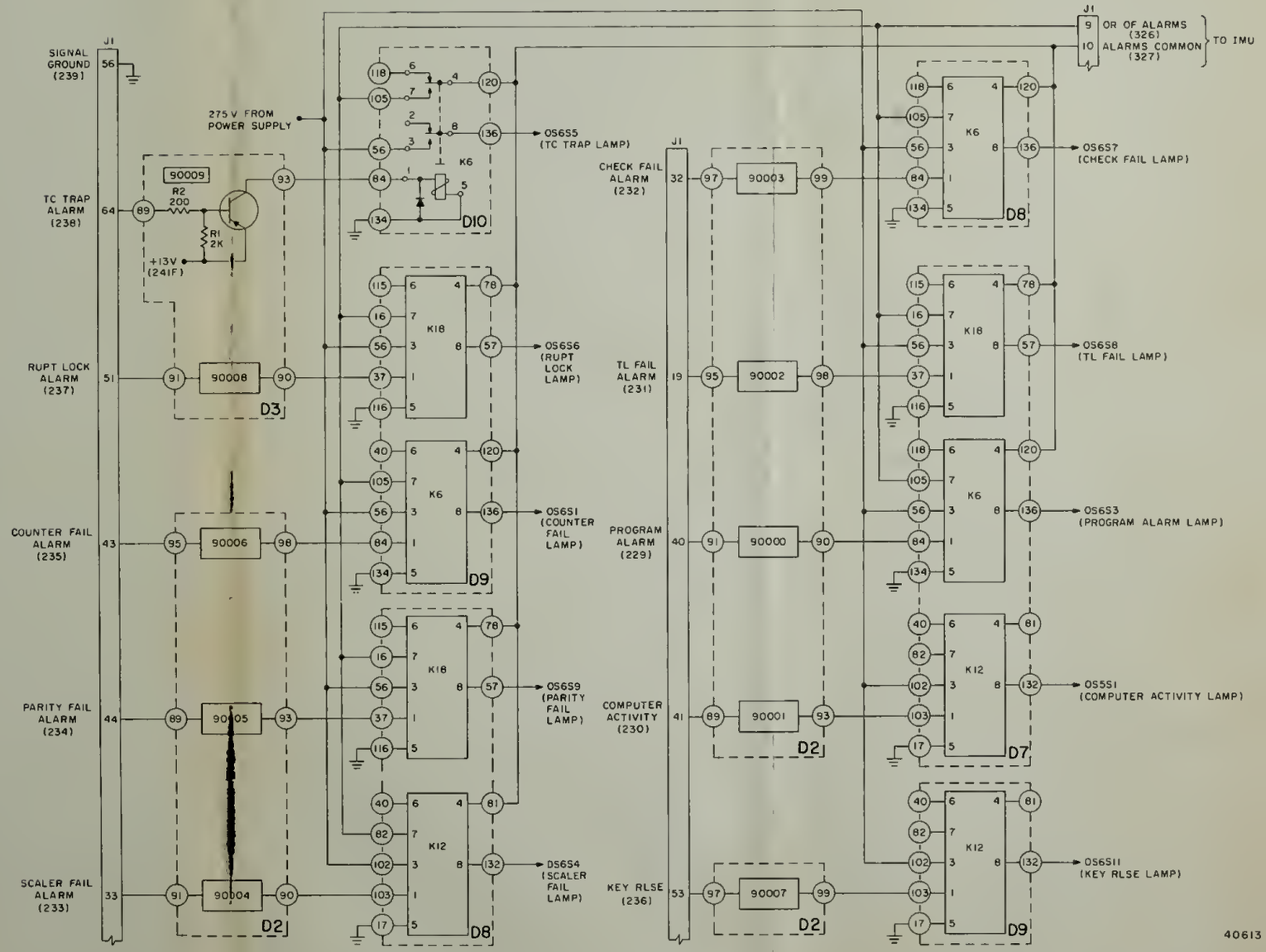

Figure 4-243. Alarm Circuits, AGC Navigation Panel DSKY

Chapter 5

PRELAUNCH AND IN-FLIGHT OPERATIONS

5-1 SCOPE

This chapter describes the functions of the G and N system during an earth orbiting mission, from preparation of the spacecraft for launch to command module touchdown. G and N system operation and crew procedures have been correlated for major phases of the flight profile as follows: prelaunch, launch, boost, injection into earth orbit, earth orbit, entry, and landing. (See figure 5-1.)

5-2 PREPARATION FOR LAUNCH

Preparation for launch begins when the backup crew enters the spacecraft and begins checkout 14 hours before liftoff. After control circuits linking the space vehicle to the launch pad have been verified as operational, the G and N subsystems are energized and a G and N operational test is performed. Data on trajectory and launch coordinates is then entered into the computer in preparation for prelaunch alignment of the IMU.

5-2.1 PRELAUNCH IMU ALIGNMENT. Initial alignment of the IMU establishes reference conditions from which spacecraft velocity and position are later calculated by the G and N system. The G and N system monitors the S-4B guidance during the boost phase and provides prime guidance during translunar (phase II and III) injection if more than two earth orbits are required before injection.

Alignment is accomplished at the launch site by erecting the stable member to local vertical and aligning the IMU in azimuth by means of a known geographical reference. Vertical erection is performed by positioning the X accelerometer input axis to sense local gravity, while maintaining the Y and Z accelerometer input axes in the horizontal plane. If the stable member drifts from this orientation, so that the outputs of the Y and Z accelerometers indicate a portion of local gravity, the AGC repositions the stable member through the stabilization loops.

The desired azimuth can vary from 72^{o} to 108^{o}, depending on the launch constraints. (See figure 5-2.) The desired azimuth of the stable member is maintained by gyro compassing, a self-alignment process which utilizes the east 25 IRIG to sense a component of the earth's rotation rate when the stable member is misaligned in azimuth. The resultant signal is used by the computer to reposition the stable member, thus compensating for earth rate and bias drift until launch. The initial optics sighting to align the G and N system for gyro compassing is taken approximately 11 hours before launch; the final verification sighting is taken 1-1/2 hours later.

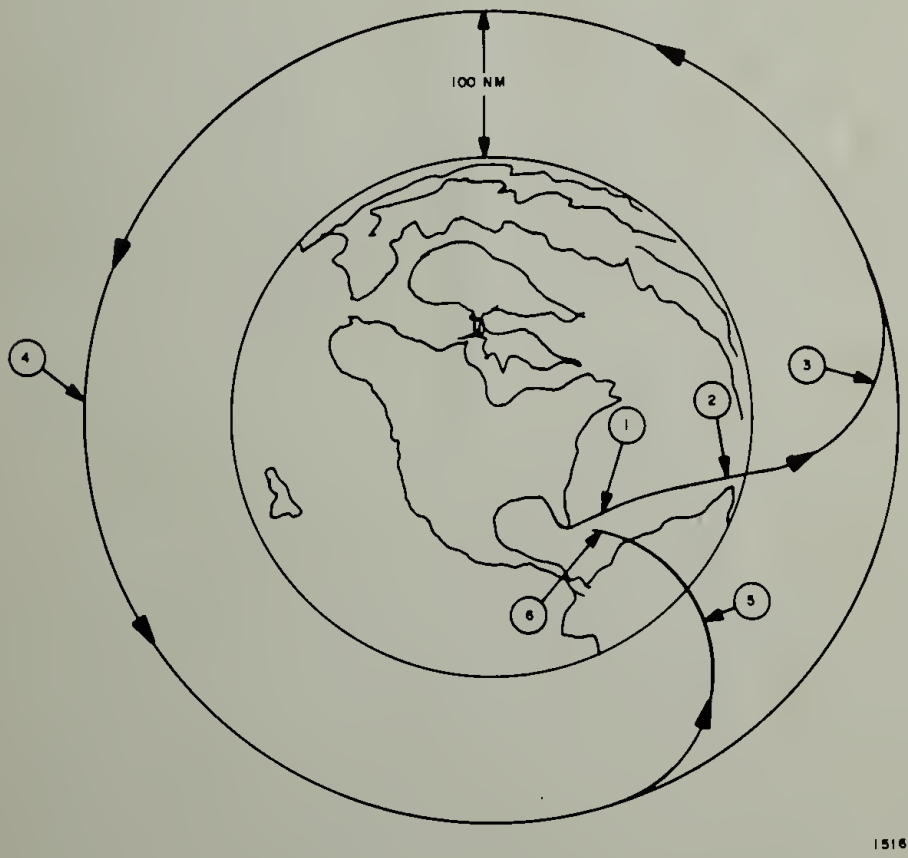

Figure 5-1. Flight Profile for Earth Orbiting Mission

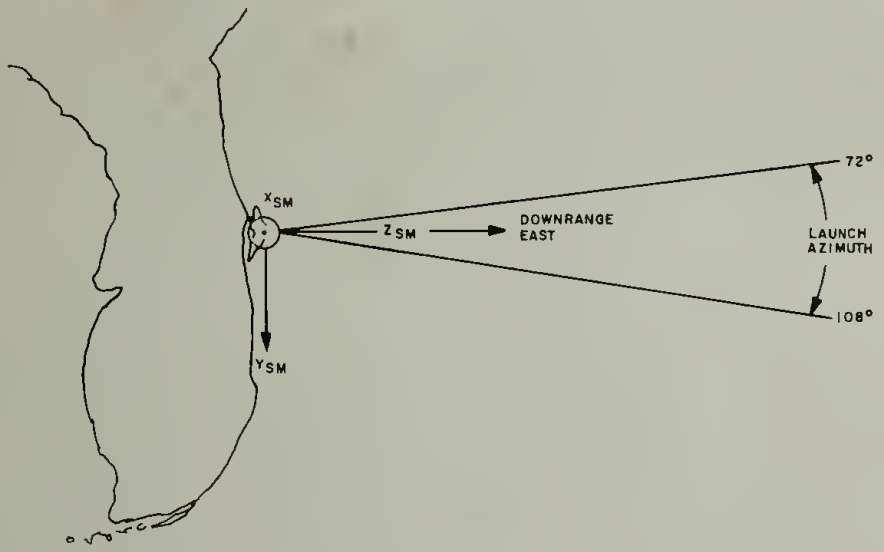

Figure 5-2. Prelaunch IMU Alignment

The backup crew leaves the spacecraft after disconnecting the GSE and securing the navigation station by folding up the work table, installing the hand controller on the center couch, and checking G and N indicator lamps and controls. The flight crew enters the spacecraft to program the computer for launch about 2-3/4 hours before lift-off.

5-3 BOOST PHASE

During earth ascent, the computer subsystem monitors changes in spacecraft position and velocity to compute the boost trajectory. Trajectory data is compared with data for a preprogramed trajectory by the computer and the difference is displayed to the astronaut. The AGC also computes and updates an abort re-entry program which can be utilized at the command of the astronaut.

Gimbal angles are fed to the flight director attitude indicator (FDAI) and velocity increments and gimbal angles are fed to the computer from the inertially referenced IMU. The booster provides discretes, such as guidance release and liftoff, to the computer.

5-4 ORBITAL NAVIGATION

When the spacecraft is in orbit about the earth, navigational measurements are taken to update values of velocity and position. Sightings are normally taken using the earth's limb (blueline) and a prominent star as reference targets for the horizon photometer and star tracker. This procedure is semi-automatic. An alternate manual procedure makes use of predetermined earth landmarks.

5-4.1 STAR-HORIZON NAVIGATIONAL MEASUREMENT. The star tracker and the horizon sensor are used to measure the angle between the earth's limb and a target star. (See figure 5-3.) The star tracker automatically locks the star line-of-sight (SLOS) to the target star after it has been acquired in the sextant (SXT) field of view. The horizon photometer fixes on the earth's limb when the SXT landmark line-of-sight (LLOS) is directed toward the earth, and automatically provides a mark signal to the AGC when on target.

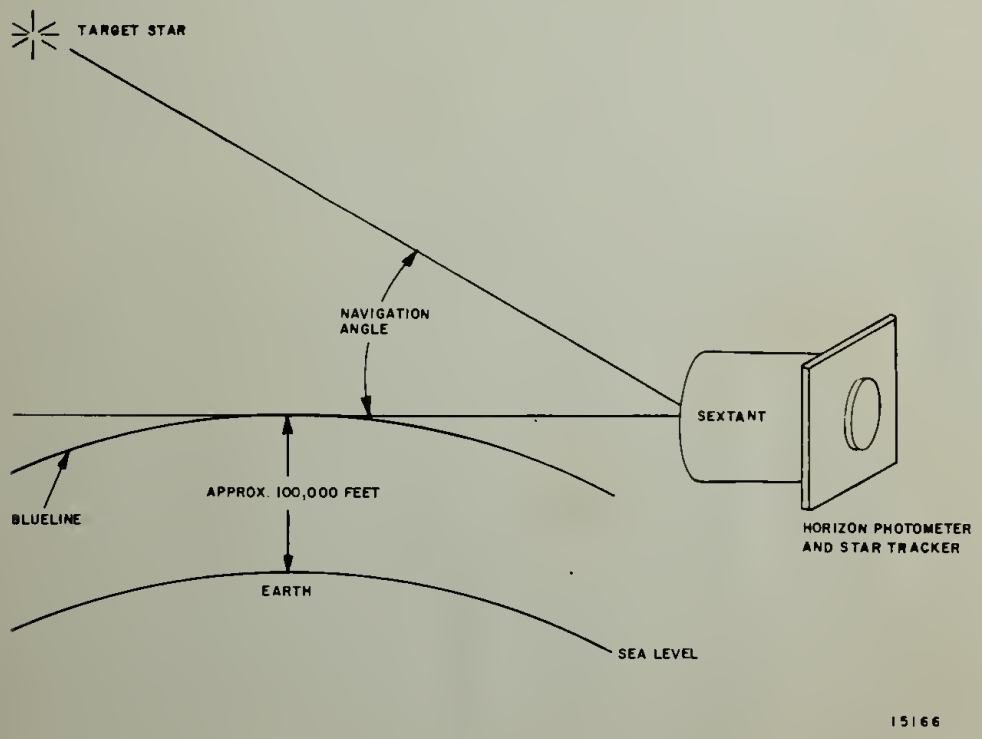

Figure 5-3. Star-Horizon Navigational Measurement

To perform a star-horizon navigational measurement, the navigator prepares his station for use, selects a computer program, zeros the optics CDU's, and selects a target star. The target must be a rising star on a bright horizon with less than 57° azimuth relative to the orbital plane of the spacecraft. After the slave telescope mode has been entered and the star acquired in the scanning telescope (SCT), the astronaut verifies that the star tracker has locked the SLOS to the target star by observing the calibrated shaft axis crosshair.

The command module is rolled approximately 75° to point the LLOS toward a bright portion of the earth's limb. A second roll maneuver, used to raise the LLOS through the earth's limb, is initiated when the trunnion axis crosshair of the SXT becomes perpendicular to the earth's limb. When the horizon photometer measures the required brightness level, an automatic mark signal occurs.

5-4.2 LANDMARK NAVIGATIONAL MEASUREMENT. Navigational measurements may be taken on predetermined landmarks on the horizon to update position and velocity data. The landmarks chosen as optical targets are close to the orbital ground path so that a target image acquired near the horizon is tracked along a path which passes directly beneath the spacecraft. (See figure 5-4.) The SCT is used for taking optical measurements because of its wide field of view.

The navigator's initial preparation for landmark navigational measurements consists of mounting the optical eyepiece and adjusting instrument panel and spacecraft interior lighting. To insure maximum accuracy in measurement, a check is made to ascertain that IMU alignment has been updated within the past 15 minutes.

The navigator first applies power to the optics subsystem; he then selects the zero optics mode and verifies that the optics CDU's read zero. After referring to the procedures check list to obtain the code number for orbital landmark measurement, the navigator enters the data into the display and keyboard (DSKY).

When a landmark appears in the SCT field of view, the navigator centers it by manipulating the optics hand controller. As the landmark is centered in the reticle, the navigator presses the MARK pushbutton, conditioning the computer to accept the information presented. If possible, three suitably spaced marks are taken for each landmark. The specific code number for the landmark sighted is then entered into the computer and the optics shaft and trunnion CDU's are driven to the required values. Resultant position and velocity data is sent to the Manned Spacecraft Flight Center (MSFC) by downlink telemetry and is checked for accuracy by comparison with ground calculations.

5-5 IN-FLIGHT IMU ALIGNMENTS

The process of IMU alignment consists of using optical sightings to align the stable member. The IMU requires alignment each time the inertial subsystem is energized or after a prolonged operation during which gyro drift could cause an error in stable member alignment. During the alignment process, the navigator is located at the lower display and control panel.

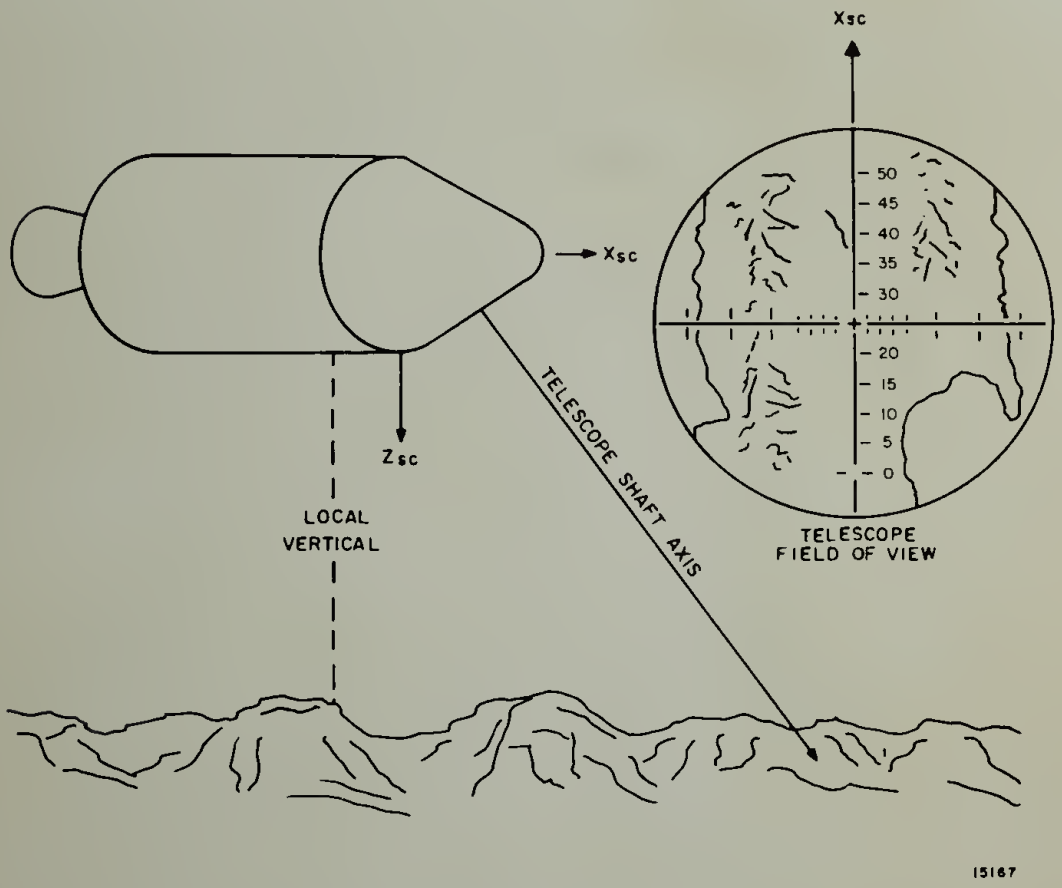

Figure 5-4. Orbital Navigation Sighting

Either an in-flight initial alignment or an update alignment may be required. If the inertial subsystem is in the standby mode, an initial alignment is performed and the system is cycled through the coarse align and fine align modes. If the IMU has been aligned but has not been realigned recently, an update alignment may be required. The update alignment requires only the precise orientation of the fine align mode.

To accomplish a fine alignment of the IMU, the astronaut selects the required computer program and targets for sighting on two stars. Each of the stars is acquired in the SCT and centered in the SXT (figure 5-5); data is recorded when the sighting is marked.

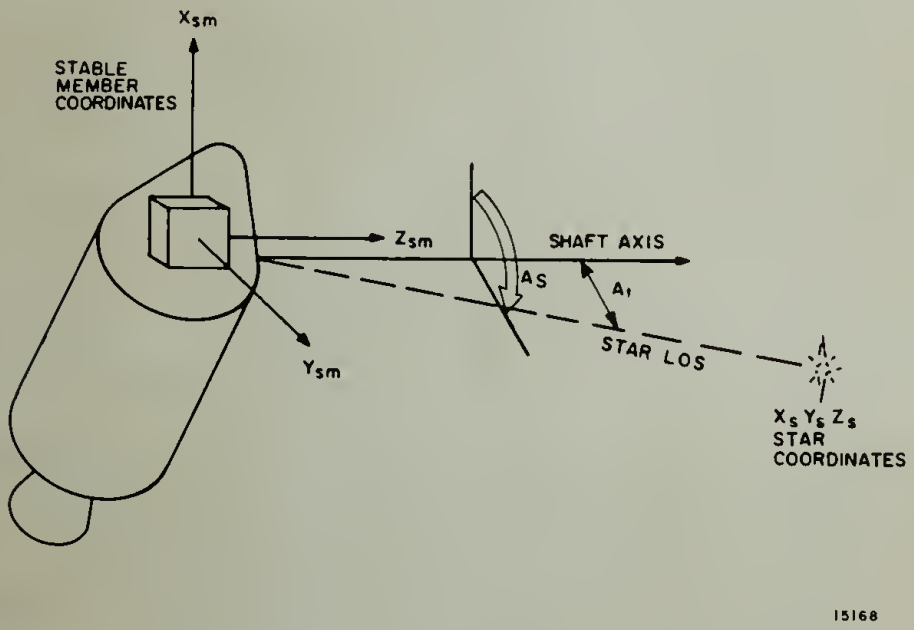

Figure 5-5. In-flight IMU Alignment

After each sighting, a star code number is entered into the computer. The computer then records all inertial and optical CDU settings. After axis transformation, the star components of the existing stable member position are compared to the components of a properly aligned stable member, as determined from the sighting. The astronaut checks the alignment by observing that the CDU's follow the gimbal angles as the gimbals are torqued into position.

5-6 THRUST MANEUVERS

Thrust maneuvers are used during an earth orbiting (phase I) mission for orbital plane and path changes. Thrust maneuvers will also be used during later missions for midcourse corrections and lunar injection.

The purpose of a thrust maneuver is to change the velocity and position of the spacecraft so that the free-fall trajectory of the vehicle will carry it to a predetermined aim point. The decision to perform a thrust maneuver is made by the crew and confirmed through communication with MSFN.

After preparation of the navigator's station and the computer for use, the navigator selects a procedures checklist and performs an in-flight initial or update IMU alignment, as required. He also aligns the FDAI, which displays steering and gimbal errors. The navigator then returns to the center couch and requests that the pilot initiate the thrust maneuver. The maneuver is monitored at the DSKY and the new spacecraft position and velocity are checked with MSFN.

Thrust maneuvers are also used during orbit of the earth while practicing docking and rendezvous techniques. Rendezvous radar is used to give range, range rate, and LOS information during these movements.

5-7 ENTRY

Entry of the command module into the earth's atmosphere is controlled by G and N roll commands which vary the aerodynamic forces on the spacecraft.

Just prior to entry, the service module is jettisoned and the command module is rotated 115 degrees to the proper entry attitude with the heat shield forward. (See figure 5-6.) The computer recieves precalculated lift and drag ratios from ground control and provides a signal representing desired roll angles to the outer gimbal CDU. This signal is compared with the actual roll angle signal from the IMU, and the difference error signal is applied to the roll jets on the command module. The module rolls about the entry roll axis, varying the lift-drag ratio and thereby maintaining the module on the proper trajectory. The stabilization loop senses spacecraft rotation and cancels the difference error signal when the proper angle is reached.

A high degree of control sensitivity is required to prevent undershoot (excessive g force) or overshoot (skip-out) of the command module. This is attained by connection of the IMU 1X resolver to the CDU 16X resolver and the application of the 16X output to the reaction jets.

Selection of the entry mode is accomplished by either the computer or the astronaut. Entry parameters are received from ground control and entered into the DSKY by the astronaut. The computer program initiates alignment of the IMU to the entry axis. The CDU and FDAI are aligned by the astronaut. Approximately 15 minutes prior to entry, the astronaut initiates separation of the service module and observes for proper firing of the pyrotechnic charges and illumination of the CM-SM Separation Light. He also observes for proper operation of the command module reaction control jets and maneuvering of the command module to the entry attitude.

Upon entry into the atmosphere (.05 g indication on main display and control (D and C) panel), the astronaut starts the elapsed time event time clock. During the entry phase the astronaut monitors the attitude indicator, entry monitor display, Δ V display, and DSKY to assure proper attitude, velocity, and roll control. This procedure is followed until the Earth Landing System parachutes are deployed.

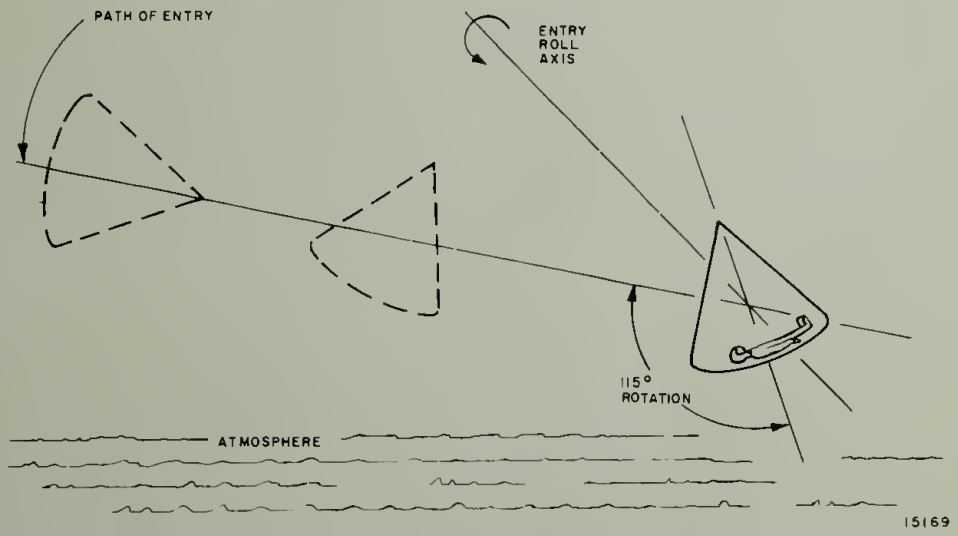

Figure 5-6. Command Module Entry Attitude

Chapter 6

CHECKOUT AND MAINTENANCE EQUIPMENT

6-1 SCOPE

This chapter contains a list of test equipment and tools necessary to complete guidance and navigation (G and N) system, inertial subsystem (ISS), optical subsystem (OSS), and computer subsystem (CSS) checkout. The test equipment is listed in alphabetical order in table 6-I. The tools are listed in alphabetical order in table 6-II. Operation and front-panel calibration procedures for the GSE are contained in the job description cards (JDC's) listed in table 6-III. The layout of equipment in a universal test station is shown in figure 6-1. The universal test station is environmentally controlled and provides for precision checkout of the G and N system and all subsystems. All components of the G and N system are mounted on the G and N mounting fixture during G and N system, ISS, OSS, and CSS checkout, except as follows:

(1) The Apollo guidance computer (AGC) main panel display and keyboard (DSKY) is mounted on the pedestal mount during G and N system checkout.

(2) The inertial measuring unit (IMU) and power and servo assembly (PSA) are mounted on the rotary table during ISS checkout.

(3) The navigation (nav) base and optical unit assembly is mounted on the rotary table during OSS checkout.

(4) The AGC, AGC navigation panel DSKY, and AGC main panel DSKY are mounted on the Apollo guidance computer test set operation console (AGC-OC) during CSS checkout.

Tahle 6-I. Checkout and Maintenance Test Equipment

Nomenclature and Part Numher	Short Nomenclature	Description and Use
Adjustahle mirror and pedestal assemhly, 1019759	adjustahle mirror	Serves as alignment reference device when aligning autocollimator assemblies during G and N system checkout.
AGC calihration system, 1020344	AGC/CS	Checks calibration of the AGC clock oscillator
AGC/computer test set operation console, 1020342	AGC-OC	Provides mounting and cooling for the CSS.
AGC handling fixture, 1020001	AGC handling fixture	Provides mounting and protection for the AGC prior to installation and during handling.
Alignment mirror assemhly, 1016951	alignment mirror	Checks alignment of nav hase and optical unit during OSS checkout.
Apollo computer simulator drawer assemhly, 1014061	AGC simulator	Simulates AGC signals, loads, and outputs for ISS and OSS checkout.
Autocollimator assemhly, 0°, 1017380	0° auto-collimator assemhly	Checks optical alignment and accuracy during G and N system and OSS checkout.
Autocollimator assemhly, 45°, 1017381	45° auto-collimator assembly	Checks optical alignment and accuracy during G and N system checkout.
Computer test set, 1020341	CTS	Checks operation of the CSS.
Coolant hose sets, a) 1901876 1901663-031 1900866-031 1900866-041 1900866-051 1900866-061 1900867-031	coolant hose	Connect G and N coolant and power console to G and N system, ISS, and OSS components.

(Sheet 1 of 5)

Table 6-I. Checkout and Maintenance Test Equipment (cont)

Nomenclature and Part Number	Short Nomenclature	Description and Use
b) 1901875 1900867-041 1900866-081 1900866-071 1901663-041		
Degausser assembly, 1900299-011	degausser	Demagnetizes 16 PIP's and 25 IRIG's during ISS checkout.
Digital ohmmeter: 0.01% and not more than 4 milliwatt output (wheatstone bridge or equivalent)	digital ohmmeter	Measures thermistor resistances in AGC.
Digital voltmeter: EI model 4000-3083, Digitec Z-204 (1), or equivalent	digital voltmeter	Mcasures 28 volt output of AGC-OC.
Filling and purging fixture, 1902371-011	filling and purging fixture	Purges and fills all components requiring coolant.
G and N coolant and power console, 1902134-011	G and N coolant and power console	Part of OITS. Provides cooling, power, and precision voltage monitoring during G and N system, ISS, or OSS checkout.
G and N mounting fixture, 1902204-011	G and N mounting fixture	Serves as mounting fixture for selected G and N components for G and N system, ISS, and OSS checkout.
G and N test interconnection kit, 1020313	G and N test interconnection kit	Provides cables and buffer circuit assembly for G & N system tests.
G and N transportation cart assembly, 1900009-031	G and N transportation cart	Used for local transportation of G and N system components.
GSE junction box assembly, 1901959-011	OJB	Part of OITS. Provides test interconnection for use during G and N system, ISS, or OSS checkout.

Table 6-I. Checkout and Maintenance Test Equipment (cont)

Nomenclature and Part Number	Short Nomenclature	Description and Use
GSE-PSA junction box assembly, 1902195-011	SJB	Provides test interconnection between PSA and GSE during ISS or OSS checkout.
IMU mounting fixture alignment bar set, 1900800-011	IMU mounting fixture alignment set	Align rotary table and IMU mounting fixture to horizontal reference during ISS checkout.
IMU mounting fixture assembly, 1900012-011	IMU mounting fixture	Mounts IMU to rotary table for ISS checkout.
IMU pressure seal tester, 1900804-011	IMU pressure seal tester	Checks for leakage of pressure seals in IMU case during G and N system checkout.
IMU snap on bellows, 1900802-011	IMU snap-on bellows	Allows for expansion of coolant in IMU during storage.
Inertial components temperature controller assembly, 1900342-011	ICTC	Provides IMU temperature control during local transportation and storage.
Interconnect cable, 1901520	interconnect cable	Used with ICTC to provide heater power to the IMU during transport.
Interconnect cables (GSE to G and N and GSE to GSE), 1902299	interconnect cables	Part of OITS. Interconnects GSE and G and N components during G and N system, ISS, and OSS checkout.
Load and signal simulator set, 1900797-021	load and signal simulator	Checks ISS and OSS phasing and fault isolation.
Optics-inertial analyzer, 1901976-011	OIA	Part of OITS. Provides control signals and monitoring and measurement facilities for use during G and N system, ISS, and OSS checkout.
Optics-inertial test set, 1902300-011	OITS	Provides control signals and monitoring and measurement facilities for use during G and N system, ISS, and OSS checkout.

Table 6-I. Checkout and Maintenance Test Equipment (cont)

Nomenclature and Part Number	Short Nomenclature	Description and Use
Optics/navigation base handling fixture, 1901426-011	optics/nav base handling fixture	Provides mounting, positioning, and protection for the nav base and optical unit assembly during installation on the G and N mounting fixture.
Optics/navigation base mounting fixture, 1902303-011	optics/nav base mounting fixture	Mounts nav base and optical unit on rotary table for OSS checkout.
Oscillograph console assembly, 1900000-011	oscillograph	Part of OITS. Monitors and records signals from OIA.
Pedestal mount (main panel DSKY), 1020195	pedestal mount	Provides mounting for the Main Panel DSKY during G and N system checkout.
Portable light assembly, 1019837	portable light assembly	Illuminates SXT reticle during OSS checkout.
PSA test point adapter assembly, 1901981-011	PSA test point adapter	Part of OITS. Provides test interconnections for use with the OIA.
PSA mounting fixture assembly, 1900606-021	PSA mounting fixture	Serves as mounting fixture for PSA during ISS checkout.
PSA tray extender set, 1900805-011	PSA tray extender	Part of OITS. Provides additional test interconnections for use during G and N system, ISS, and OSS checkout.
Remote optics controller assembly, 1902046-011	remote optics controller	Positions optical unit during OSS checkout.
Retro-reflecting prism, 1019840	retro-reflecting prism	Used in aligning OSS targets and checking SCT shaft accuracy.
Rotary table calibration set, 1900810-011	rotary table calibration set	Contains all equipment necessary to perform rotary table calibration.
Shaft accuracy tester, 1019769	shaft accuracy tester	Checks accuracy of SCT shaft during OSS checkout. The tester is also used to support the star and horizon simulator during OSS checkout.

(Sheet 4 of 5)

Table 6-I. Checkout and Maintenance Test Equipment (cont)

Nomenclature and Part Number	Short Nomenclature	Description and Use
Star and horizon simulator, 1019900	star and horizon simulator	Optically simulates star and earth horizon during OSS checkout.
Subsystem test interconnection kit, 1020312	subsystem test interconnection kit	Provides cables and mounting bracket assembly for subsystem tests. Requires part of G & N test interconnection kit.
Theodolite and support assembly, 1017447	theodolite	Aligns 0^{o} autocollimator assembly and 45^{o} autocollimator assembly.
Ultra precision rotary table, 1900926-011	rotary table	Serves as mounting and test platform for selected G and N system components during ISS or OSS checkout.
Variable deviation optical wedge assembly, 1017376	variable deviation wedge	Checks optical alignment and accuracy during G and N system checkout.
Vertical leveling mirror assembly, 1017445	vertical leveling mirror	Checks optical target alignment during G and N system and OSS checkout.
Volt-ohm-milliammeter; Simpson 270, or equivalent	multimeter	Provides voltage and continuity checks in AGC.

(Sheet 5 of 5)

Table 6-II. Checkout and Maintenance Tools

Nomenclature and Part Number	Short Nomenclature	Description and Use
AGC sling: MY-4, Abbot Jordan Hoist Co., Brighton, Mass.	AGC sling	Connects lifting hoists to AGC when transporting the AGC outside of the AGC shipping container.
Allen adapter: 5/32 inch, JO Line, or equivalent	allen adapter	Adapts the torque wrench to the AGC module inserts.
Torque wrench: 17 inch-pound, JO Line, or equivalent	torque wrench	Torque AGC modules onto AGC trays.
IMU sling	IMU sling	Connects lifting hoist to the IMU to position and remove IMU from rotary table during ISS checkout or from G and N mounting fixture during G and N system checkout.
Tool kit	tool kit	Contains tools required to support maintenance activities in G and N laboratory and stockroom.

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Coaxial distribution panel	18004	Operating the primary signal selector panel, coaxial distribution panel, and PSA test point adapter to apply auxiliary signals to the dual beam oscilloscope.
Computer test set	04690 thru 04694	Check operation of the CTS.

(Sheet 1 of 5)

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Counter	18017	Operating the counter as a forward or reverse counter.
Counter	18018	Operating the counter to count the number of input events that occur during any preselected time interval.
Counter	18019	Operating the counter to count the number of input events that occur during interval determined by "D" input events.
Counter	18020	Operating the counter to count the clock frequency pulses that occur during interval determined by "D" input events.
Counter	18021	Test to determine correct operation of N_1 switches, time base circuitry, and count-chain circuitry (counter operation).
Counter	18022	Test to determine correct operation of N_2 switch (counter operation).
Digital recorder	18043	Operating and interpreting the digital recorder.
Digital voltmeter	18035	Operating the digital voltmeter to measure a dc voltage.

(Sheet 2 of 5)

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Digital voltmeter	18036	Operating the digital voltmeter to measure an ac voltage.
Digital voltmeter	18037	Operating the digital voltmeter to automatically measure an ac or dc voltage.
Dual beam oscilloscope	18005	Operating the dual beam oscilloseope, scope "A", upper beam differential amplifier, and primary signal selector panel to measure voltages.
Dual beam oscilloscope	18006	Operating the dual beam oscilloscope upper beam differential amplifier to measure phase shift.
Dual beam oscilloscope	18007	Operating the dual beam oscilloscope to make time measurements.
Dual beam oscilloscope	18008	Operating the dual beam oscilloscope to make frequency measurements.
Dual beam oscilloscope	18009	Operating the dual beam oscilloscope, scope "B". channel 1 to monitor pulses.
Dual beam oscilloscope	18010	Instructions for applying two signals simultaneously to the dual beam oscilloscope, scope "B".
Dual beam oscilloscope	18011	Instructions for applying an oscillograph signal to the dual beam oscilloscope, scope "B", channel 2.
Galvanometer and current source monitor	18016	Operating the galvanometer and current source monitor panel to measure voltages.
G and N coolant and power console	18046	Operating and interconnecting the G and N coolant and power console for G and N system, ISS, and OSS testing.
Gimbal position control panel	18044	Operating the gimbal position control panel.
IMU CDU load and signal simulator	18048	Operation of the IMU CDU load and signal simulator.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Optics CDU load and signal simulator	18147	Operation of the optics CDU load and signal simulator.
Oscillograph console	18023	Operating the oscillograph (electric writing).
Oscillograph console	18024	Operating the oscillograph (ink writing).
Oscillograph console	18025	Adjustment of oscillograph console dc amplifiers.
Oscillograph console	18026	Operating the oscillograph console dc amplifiers.
Oscillograph console	18027	Adjustment of oscillograph console phase sensitive demodulators (800 cps reference) (normal operation).
Oscillograph console	18028	Adjustment of oscillograph console phase sensitive demodulators (3200 cps reference) (normal operation).
Oscillograph console	18029	Adjustment of oscillograph console phase sensitive demodulators (800 cps reference) (periodic phase shift check and operation).
Oscillograph console	18031	Operating the oscillograph console phase sensitive demodulators.
Oscillograph console	18032	Installation of new ink cartridge in oscillograph console.
Oscillograph console	18033	Installation of new ink pen in oscillograph console.
Oscillograph console	18034	Installation of new paper in oscillograph console.

Table 6-III. List of Operating Procedure JDC's for GSE (cont)

Equipment	JDC Number	JDC Description
Phase angle voltmeter	18038	Operating the phase angle voltmeter to measure total rms voltage.
Phase angle voltmeter	18039	Operating the phase angle voltmeter to measure a fundamental rms voltage.
Phase angle voltmeter	18040	Operating the phase angle voltmeter to measure a phase angle.
Phase angle voltmeter	18041	Operating the phase angle voltmeter to measure in-phase and quadrature components.
Phase angle voltmeter	18042	Operating the phase angle voltmeter to indicate a phasc sensitive null.
Primary signal selector panel	18000	Operating the primary signal selector pancl to apply internal signals to the digital voltmeter, phase angle voltmeter and dual beam oscilloscope.
Primary signal selector panel	18001	Operating the primary signal selector panel to apply reference signals to the dual beam oscilloscope.
Primary signal selector panel	18002	Operating the primary signal selector panel to apply PSA test point adapter test point signals to the digital voltmeter, phase angle voltmeter, and dual beam oscilloscope.
Primary signal selector panel	18003	Operating the primary signal selector panel to apply auxiliary signals to the digital voltmeter, phase angle voltmeter, and dual beam oscilloscope.
Filling and purging fixture	18045	Operating the filling and purging fixture to purge and fill G and N system components.
Star and horizon simulator	03092	Photometer setup and operation.
Signal generator	18012	Adjustment of the signal gencrator.
Signal generator	18013	Operating the signal generator.

(Sheet 5 of 5)

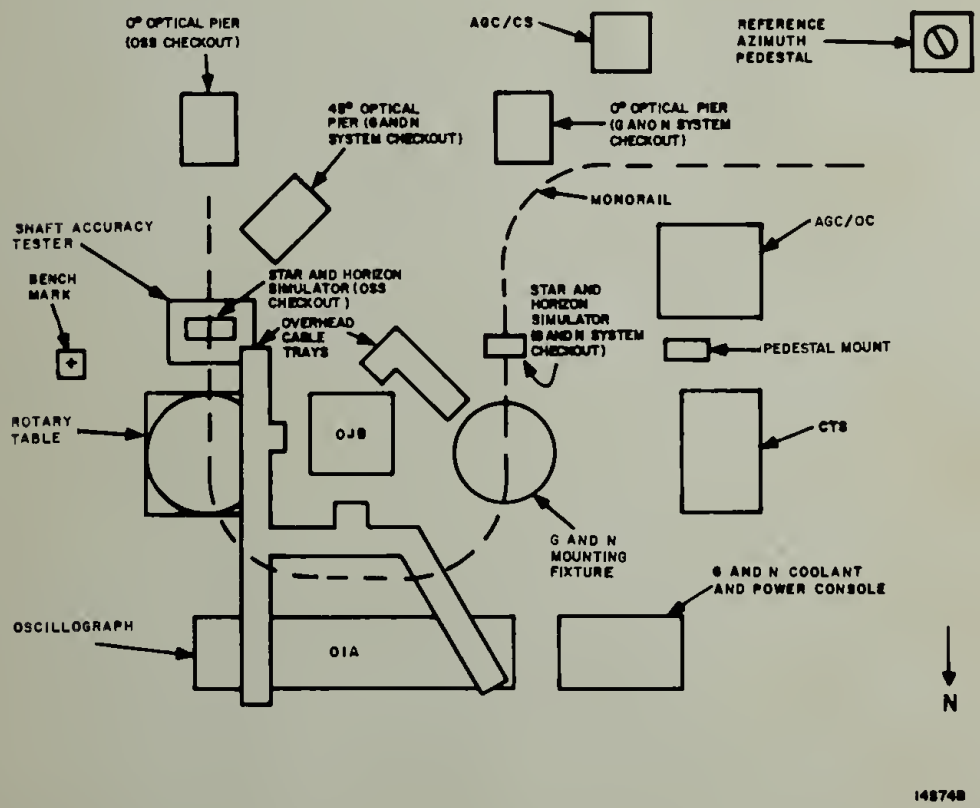

Figure 6-1. Universal Test Station Layout

Chapter 7

CHECKOUT

7-1 SCOPE

This chapter contains flowgrams which outline checkout procedures for the guidance and navigation (G and N) system, inertial subsystem (ISS), optical subsystem (OSS), and computer subsystem (CSS). Checkout is performed at the G and N laboratories of North American Aviation (NAA) and Merritt Island Launch Area (MILA). A master flowgram for the G and N system and one for each of the three subsystems precedes more detailed preparation and checkout flowgrams. Each master flowgram references the detailed flowgrams which in turn reference the Job Description Cards (JDC's) required to fulfill the checkout function. The detailed flowgrams also refer to JDC's which describe setup and operation of ground support equipment (GSE).

Information regarding packing, shipping, and handling of any component of the G and N system will be found in Packing, Shipping, and Handling Manual ND-1021038.

7-2 G AND N SYSTEM

7-2.1 PREPARATION. Table 7-I lists G and N system components and GSE required for system and subsystem checkout. Table 7-II lists required system and GSE interconnect cabling.

7-2.2 CHECKOUT. The G and N system master flowgram (figure 7-1) specifies the conditions leading to a G and N system checkout and displays the mandatory sequence to be followed. Detailed flowgrams (figures 7-2 and 7-3) give sequential listings of JDC's to be performed. The following paragraphs describe the tests performed using these JDC's.

7-2.2.1 Standby Power-On Test. During this test, 28 volt dc and 3200 cps voltages are checked. Temperature control and indicating circuits are checked for proper response to imbalances, and inertial measuring unit (IMU) temperatures are checked in the proportional and backup modes.

During the standby mode, the ability of the Apollo guidance computer (AGC) to supply the master clock signal and the 3200 cps sync pulses for the power supplies is checked, deenergization of the AGC logic is checked, and operation of the display and keyboard (DSKY) C-relay and AGC self-check are checked.

To allow use of airborne heater power in the standby mode, ground support equipment (GSE) cable W18 is replaced with a shorting plug. The IMU TEMP MODE selector on the G and N indicator control panel is set to PROPORTIONAL to activate the temperature control and indicating circuits. The PROCEED/ISS STANDBY pushbutton on the test control panel is pressed to close the 28 volt dc standby power circuit. After proper lamp indications are observed, the 28 volt dc GSE power is checked using the primary signal selector panel and digital voltmeter. Before proceeding with further tests, a period of one hour is allowed for stabilization of the IMU temperature.

After the waiting period, heater current is checked on the temperature monitor control panel. The IMU TEMP MODE selector is set to AUTO OVERRIDE to allow measurement of IRIG and PIP temperatures and automatic switchover to the emergency mode. To check nominal temperature on the IRIG TEMP meter and ACCEL TEMP meter, the IMU TEMP MODE ZERO button is pressed to establish a null condition in the indicating bridge. To check low temperature operation on the IRIG TEMP meter, the IMU TEMP MODE IRIG GAIN button is pressed to simulate a low temperature (-5 degrees) in the indicating bridge. The HEATER CURRENT indication is also checked to assure switchover to the emergency mode. To check high temperature operation on the ACCEL TEMP meter, the IMU TEMP MODE PIPA GAIN button is pressed to simulate a high temperature (+5 degrees) in the indicating bridge. Heater current is also checked under this condition to assure switchover to the emergency mode. After both low and high temperature checks, the IMU TEMP MODE selector is set to PROPORTIONAL to allow the circuit to return to normal.

To permit measurement of temperature indicating bridge outputs using the MONITOR meter, the shorting plug is removed, cable W18 reconnected, and the power servo assembly (PSA) test point adapter connected. With the IMU TEMP MODE selector set to PROPORTIONAL, bridge outputs are measured with the MONITOR METER SELECT switch in both IRIG TEMP and ACCEL TEMP positions. To test backup mode operations, these measurements are repeated with the IMU TEMP MODE selector set to BACKUP.

The frequency output of the 3200 cps, 2 volt power supply is measured by applying this signal through the primary signal selector panel to the "D" input of the counter. A counter indication of 100000 (±32) pulses indicates a frequency of 3200 (±1) cycles.

7-2.2.2 Operate Power-On Test. This test checks proper IMU time delay circuit operation, proper turn-on mode sequencing, coupling display unit (CDU) servo functional operation, and system power availability with the IMU operate and AGC power applied during initial power-on phases. The test is performed after the system has been in standby mode for a minimum of two hours to allow stabilization of the magnetic suspension circuits.

With the CDU's set to zero, IMU power is applied by pressing the ISS OPERATE pushbutton on the test control panel. Automatic sequencing from the initial coarse align mode directly to the attitude control or entry mode is checked by observing the mode lamps on the IMU control panel. Using the oscillograph, the IMU time delay required for gyros to attain their operating speed is measured. The CDU 1 speed (1X) resolver outputs for the inner, middle, and outer gimbals are displayed on the oscillograph. The amplitudes of the CDU 1X resolver outputs just prior to the end of the time delay are measured to verify that the gimbals are following properly as evidenced by the specified minimum error.

With the OSS in the zero optics mode, the OPTICS POWER ON pushbutton on the test control panel is pressed. Proper CDU servo action is checked by observing that the CDU counters drive to zero.

To insure that 27.5 volts dc is being supplied from the GSE to the AGC, this voltage is adjusted using the VOLTAGE ADJUST control on the test control panel and measuring the voltage on the digital voltmeter.

7.2.2.3 Failure Indicating Circuitry Tests. This test checks the operation of failure indicating devices in the monitor panel, condition annunciator, DSKY, and computer test set (CTS). The presence of error detecting signals on PSA test points is also checked. The failure indicator tester is used in conjunction with the PSA tray extender set to simulate failures in the system. These indications are noted on panel displays, oscillograph, and digital voltmeter.

The initial test checks the presence of CDU fail signals on PSA test points which are accessible to the astronaut. The system is initially placed in the zero encoder mode to drive the CDU's to zero. The system is advanced to the CDU manual mode and the CDU's are manually positioned to 355 degrees to generate CDU fail signals. The signals are routed to the oscillograph for measurement.

Tests involving the failure indicator tester consist primarily of setting various switches on the failure indicator tester to TEST and observing resultant failure indications. Such tests are performed in the fine align mode.

To generate a G and N error voltage at PSA test points, the MICROSYN EXCITATION switch on the failure indicator tester is set to TEST. The voltage is measured using the primary signal selector panel and digital voltmeter.

A test is included to check the operation of AGC alarm circuits. These tests are performed with the system in the standby mode and power to the AGC removed.

Telemetry CDU fail signals are checked in the fine align mode. The signal conditioner input is routed through the primary signal selector panel to the oscilloscope. The CDU is manually rotated until the CDU FAIL lamp on the condition annunciator lights. The voltage is then measured on the oscilloscope.

7-2.2.4 Temperature Control Test. During this test, temperature control operation is demonstrated in the proportional, backup, and emergency modes. Temperature stability is checked by periodic measurement of heater and blower currents. System interfaces are checked by monitoring signals present at PSA test points.

After initial turn-on, the system is placed in the coarse align mode and the temperature control circuit is placed in the proportional mode. Excitation to the temperature control bridge is measured using the primary signal selector panel and digital voltmeter. The inherent bias in the pulsed integrating pendulum (PIP) and inertial reference integrating gyro (IRIG) temperature control bridge circuits is measured by pressing the TEMP MODE ZERO pushbutton on the G and N indicator control panel and observing the MONITOR meter on the temperature monitor control panel. After 30 minutes, the actual PIP and IRIG temperature signals are measured and recorded. To assure stability, the temperatures are rechecked during and after a 90 minute period using the oscillograph and MONITOR meter. Heater current and blower current are measured to check proper operation in the proportional mode. System interfaces are checked using the primary signal selector panel and digital voltmeter.

In the backup mode, the PIP and IRIG temperature signals are measured on the MONITOR meter and recorded on the oscillograph. Heater current is observed on the oscillograph for computation of the duty cycle. Blower current is also observed on the oscillograph to insure that its cycling is inversely proportional to the heater current.

In the emergency mode, tests performed in the backup mode are repeated.

Because of temperature control circuitry identical to that in the proportional mode, functional tests are not performed in the auto override mode. The circuit is placed in the auto override mode at the completion of this test and succeeding tests for performance of system interface checks.

7-2.2.5 G and N System Power Supplies Test. The power supplies test consists primarily of voltage and frequency measurements of power supply outputs. Input timing pulses, telemetry output signals, and phase shift of critical signals are also checked. Measurements are made with prime power supplied through bus A and through bus B.

The AGC calibration system is used to measure the oscillator frequency of the AGC master clock signal that provides sync pulses to each power supply. The signal is monitored every 100 milliseconds for 15 minutes to check frequency stability. The CTS oscilloscope is used to observe the waveform of the master clock signal.

Using the digital voltmeter and primary signal selector panel, power supply output voltages are measured at PSA test points. The signals are also measured at the signal conditioner connectors to verify proper system interface. Frequencies of power supply outputs are measured by means of the counter.

Amplitudes of SET and RESET pulses applied from the AGC to multivibrators in the ac power supplies are measured using an oscilloscope. To determine the phase shift in the 3200 cps, 2 volt supply, input and output waveforms are compared on the dual-trace oscilloscope.

After completion of bus A voltage and frequency tests, the AGE POWER A BUS/AGE POWER B BUS pushbutton on the test control panel is pressed and measurements are repeated for bus B.

7-2.2.6 Panel Brightness and Lamp Test. This test checks operation of various lamps on the G and N indicator control panel, IMU control panel, condition annunciator, and DSKY. Proper operation of the ATTITUDE IMPULSE ENABLE switch on the G and N indicator control panel is also checked.

Panel brightness of the G and N indicator control panel is checked by rotating the PANEL BRIGHTNESS thumbwheel and observing panel illumination.

Mode lamps are checked by pressing the CHECK MODE LAMPS pushbutton on the G and N indicator control panel and observing the mode lamps on the IMU control panel.

Failure and condition lamps are checked by pressing the CHECK CONDITION LAMPS pushbutton on the G and N indicator control panel and observing indications on the condition annunciator.

The AGC failure lamps are checked by pressing the TEST ALARM pushbutton on the DSKY and observing DSKY lamp indications.

The coolant lamp is checked by pressing the CHECK COOLANT LAMP pushbutton on the G and N indicator control panel and observing that coolant connectors are visible.

The ATTITUDE IMPULSE ENABLE switch is checked by operating the switch and observing the PROCEED/CONTINUITY lamp on the test selector panel.

7-2.2.7 Zero Optics Test. This test measures the time required to zero the optics and checks the zeroing accuracy of the CDU's.

Before the optics zeroing time is measured, the motor drive amplifier outputs and the tachometer feedback voltages are checked, on the oscillograph and the digital voltmeter, while using the control stick to slew the 2X TRUNNION CDU and SHAFT ANGLE CDU in a maximum increasing direction. The CDU encoder outputs are also checked, on the oscillograph, by using the thumbwheels to drive the 2X TRUNNION CDU and SHAFT ANGLE CDU in an increasing and decreasing direction. The CDU's and optics are then zeroed and, using the control stick, the 2X TRUNNION CDU is driven to 180 degrees and the SHAFT ANGLE CDU is driven to 270 degrees. The OPTICS MODE switch

is set to ZERO OPTICS and the elasped time between the steady state maximum voltage and the steady state minimum voltage is checked on the oscillograph to determine the time required for the optics to zero. The CDU dial indications are checked and the CDU 16X resolver error voltage is measured. The AGC is programmed to indicate the optics angles and thus check the DSKY indications to a known CDU angle of zero.

7-2.2.8 Optics Slew Rate Test. This test checks the slewing operation of the optics servo loops.

Using the control stick, the optics servo loops are slewed with the CONTROLLER SPEED switch set to high, medium, and low. Measurements are obtained on the oscillograph and the digital voltmeter for the following signals during slewing of the optics servo loops:

Sextant (SXT) shaft and trunnion motor drive amplifier inputs

SXT shaft and trunnion tachometer feedback

Scanning telescope (SCT) shaft and trunnion 1X resolver error

SCT shaft and trunnion tachometer feedback

shaft and trunnion CDU 16X resolver error

trunnion CDU tachometer feedback

shaft CDU tachometer feedback

SCT trunnion tachometer output.

7-2.2.9 Optics Coordinate Transformation Control Test. This test checks the operation of the cosecant circuit, resolution of the control stick, and slewing of the optics in the resolved mode. The cosecant circuit is used to provide an image angular velocity independent of the magnitude of trunnion angle by decreasing the shaft speed as the trunnion angle increases. The resolved mode of operation provides an up-down motion of the image with an up-down movement of the control stick independent of shaft angle. Likewise, a right-left movement of the control stick provides a right-left motion of the image.

To check the cosecant circuit, the resolved mode of operation, and the resolved mode slew rate, an object is centered in the SCT field-of-view with the SCT set to a shaft angle of 225 degrees and a trunnion angle of 10 degrees. The control stick is displaced 45 degrees in the upper right hand quadrant and the image motion is viewed through the SCT. The image motion in the SCT will be 45 degrees toward the upper right

quadrant of the SCT field-of-view. Effectively, the control stick is providing a pure trunnion movement of the optics. When the image leaves the SCT upper right field-of-view, the control stick is released, the SHAFT ANGLE CDU is stopped, and the EVENT MARKER pushbutton on the oscillograph is pressed. The SHAFT ANGLE CDU indication is recorded and compared with the original 225 degree setting. During this test, the SHAFT ANGLE CDU should not have moved from the original 225 degree setting. The slew rate (time required for the image to leave the SCT field-of-view) is recorded on the oscillograph and is dependent upon the CONTROLLER SPEED switch setting.

To terminate this test, the manual direct mode is selected and the optics are zeroed.

7-2.2.10 Optics Positional Accuracy Test. This test checks the SXT landmark line-of-sight (LLOS) and star line-of-sight (S_tLOS) parallelism, the SXT LLOS and SCT LOS parallelism, SXT S_tLOS positional accuracy, and SCT and SXT slew characteristics in the computer mode. A comparison is also made with corresponding data from other tests. This test requires that the G and N mounting fixture be set to 0 degree and the optics be set to a shaft angle of 270 degrees and a trunnion angle of 0 degree (for parallelism checks) or 45 degrees (for positional accuracy checks).

Before performing the parallelism checks, the optics are set to a shaft angle of 270 degrees and a trunnion angle of 0 degree. The 2X TRUNNION CDU dial indication is then recorded as (a). The variable deviation wedge (VDW) is placed in front of target number 1 and the VDW dial is adjusted to zero. The G and N mounting fixture is then adjusted while sighting through the SXT LLOS until the horizontal reticle line of the SXT is coincident with the dot and horizontal reticle line of target number 1. The VDW is then moved laterally and the VDW dial is adjusted while sighting through the SXT LLOS until the central vertical reticle line of the SXT is coincident with dot and vertical reticle line of target number 1. This VDW dial setting is then recorded as (c). The VDW dial is then adjusted while sighting through the SXT S_tLOS until the central vertical reticle line of the SXT is coincident with dot and vertical reticle line of target number 1. This VDW dial setting is then recorded as (e). The VDW dial setting (e) is subtracted from VDW dial setting (c) and the result is the degree of parallelism between the SXT S_tLOS and LLOS. The control stick is then manipulated while sighting through the SCT until the central dot on the reticle of target number 2 is aligned between crosshairs on the SCT reticle. The 2X TRUNNION CDU dial indication is then recorded as (h). The CDU dial indication (h) is subtracted from CDU dial indication (a) and the result is the degree of parallelism between the SCT LOS and the SXT LLOS.

Before the positional accuracy checks of the SXT S_tLOS are performed, the optics are set to a shaft angle of 270 degrees and a trunnion angle of 0 degree. The VDW is placed in front of target number 3 and the VDW dial is set to a calculated position. The VDW dial calculated setting is obtained by subtracting the target calibration angle for target number 3, obtained from tests performed prior to this test, from 45 degrees and

then adding the VDW dial setting (c) recorded previously. The control stick is then manipulated vertically while sighting through the SXT StLOS until the central dot on the reticle of target number 3 is coincident with the vertical crosshair of the SXT reticle. At the instant of coincidence the MARK pushbutton is pressed and the 2X TRUNNION CDU dials are stopped. Pressing the MARK pushbutton allows the AGC to record and display the optical CDU angles and the time. The AGC display of the 2X TRUNNION CDU angle and the 2X TRUNNION CDU dial indication are then recorded as (s). The control stick is manipulated two more times and at the instant of coincidence the MARK pushbutton is pressed. The AGC display of the 2X TRUNNION CDU angle and the 2X TRUNNION CDU dial indication are recorded for each mark as (s). The AGC displays of the 2X TRUNNION CDU angle are converted to bit counts by multiplying the indication by 364.09. One of the three bit counts is then selected and recorded as (t). A similar bit count is then obtained from tests performed prior to this test and is recorded as (v). The bit count recorded as (t) is subtracted from the bit count recorded as (v) and a comparison is made with the data of previous tests to determine the positional accuracy of the SXT StLOS. This same procedure is repeated six times, using the following sequence: for the first three tests, first 90 seconds, then 30 seconds, and then 60 seconds are added to the previously calculated VDW setting; for the last three tests, first 30 seconds, then 90 seconds, and then 60 seconds are subtracted from the previously calculated VDW setting.

Before performing computer control checks of the optics, the optics are slewed to a shaft angle of 270 degrees and a trunnion angle of 45 degrees. While sighting through the SXT StLOS, the control stick is manipulated until the SXT reticle pattern is coincident with the target number 3 reticle pattern. At the instant of coincidence the MARK pushbutton is pressed. The SHAFT ANGLE CDU and 2X TRUNNION CDU angles are displayed on the DSKY and these angles are then recorded as R1 and R2, respectively. VERB 41 NOUN 55 (coarse align optical CDU's) is entered into the DSKY. Optics angles of 0 degree for the shaft and trunnion are entered into the DSKY and the optics are slewed to 0 degree. The time required for the optics to slew to 0 degree is recorded on the digital recorder. VERB 41 NOUN 55 is again entered into the DSKY and then the angles R1 and R2 recorded previously are entered. The time required for the optics to slew to these angles is recorded on the digital recorder. VERB 16 NOUN 55 (monitor all components of optical CDU's) is entered into the DSKY and the CDU angles are displayed. These angles are again recorded as R1 and R2 and are subtracted from R1 and R2 recorded previously to check positional accuracy of the SXT when using the AGC.

7-2.2.11 Tracker Response and Accuracy Test.. This test checks the tracker dynamics, accuracy, tracker LOS and SXT StLOS parallelism, and the computer mode indications. This test requires that the star and horizon simulator be set to produce a +1.0 magnitude star at the 15 degree position, that the G and N mounting fixture be set to -90 degrees, that the optics shroud be installed between the SXT and the star and horizon simulator, and that the optics be set to a shaft angle of 337 degrees and a trunnion angle of 15 degrees.

After initial setup, the star and horizon simulator micrometer dials are adjusted while sighting through the SXT eyepiece until the 6 arc-second star is centered on the SXT reticle. The 6 arc-second star is then offset 1 arc-minute and the tracker drive voltages and output voltages are measured at system test points to check proper test point connections. The TRACK pushbutton is pressed and the SXT will track the 6 arc-second star. The SHAFT ANGLE CDU and 2X TRUNNION CDU dial indications are recorded; the tracker circuit is inhibited by pressing the TRACK pushbutton. The control stick is then manipulated while sighting through the SXT eyepiece until the 6 arc-second star is coincident with the SXT reticle. The MARK pushbutton is pressed at the instant of coincidence and the SHAFT ANGLE CDU and 2X TRUNNION CDU dial indications are recorded and compared with the dial indications recorded previously to check parallelism between the tracker LOS and SXT StLOS. The TRACK pushbutton is pressed and the time required for the tracker to acquire the 6 arc-second star is measured on the oscillograph. The X and Y tracker in-phase null output voltages are also recorded. The optics are zeroed and then set to a shaft angle of 337 degrees and a trunnion angle of 15 degrees. The star and horizon simulator micrometer dials are adjusted while sighting through the SXT eyepiece until the 6 arc-second star is centered on the SXT reticle. The star and horizon simulator micrometer dial settings are then recorded. Micrometer dial A is adjusted in a counterclockwise direction until the STAR PRESENCE indicator goes out and then adjusted in the clockwise direction until the STAR PRESENCE indicator lights. The micrometer dial A setting is then recorded and compared with the micrometer dial A setting recorded previously to check operation of the star and horizon simulator. The TRACK pushbutton is pressed and the time required for the tracker circuit to acquire the 6 arc-second star is recorded. The star and horizon simulator is set for a star magnitude of +2.0, and the optics are zeroed and then set to a shaft angle of 337 degrees and a trunnion angle of 15 degrees. The star and horizon simulator micrometer dials are adjusted while sighting through the SXT eyepiece until the 6 arc-second star is centered on the SXT reticle. The star and horizon simulator micrometer dials are then offset 0.006 (one arc-minute). The TRACK pushbutton is pressed and the time required for the tracker to acquire the 6 arc-second star is measured on the oscillograph. The AGC is then programmed to indicate the tracker mode by entering VERB 15 NOUN 01 into the DSKY and then entering address 00007_8 of the first mode register. The tracker mode is indicated on the DSKY by the display of $-3---_8$ in register 3 of row 1. The star and horizon simulator micrometer dial A is adjusted in a counterclockwise direction until the STAR PRESENCE indicator goes out. The DSKY will indicate the absence of the star by the display of $-1---_8$ in row 1 of the DSKY.

To terminate this test, the optics are zeroed, the optics shroud between the SXT and star and horizon simulator is removed, and the G and N mounting fixture is set to the 0 degree position.

7-2.2.12 Photometer Response and Accuracy Test. This test checks the horizon photometer response, accuracy, horizon photometer LOS and SXT LLOS parallelism, and the computer mode indications. This test requires that the G and N mounting fixture be set to the 90 degree position, that the optics shroud be installed between the star and horizon simulator and the SXT, and that the optics be set to a shaft angle of 0 degree and a trunnion angle of 60 degrees.

After initial setup, the star and horizon simulator micrometer A and B dials are adjusted while sighting through the SXT eyepiece until the 30 arc-second star is centered on the SXT reticle. The micrometer A and B dial settings are then recorded. The horizon photometer output voltages are measured at system test points to check proper test point connections. The star and horizon simulator micrometer A and B dials are adjusted again while sighting through the SXT eyepiece to insure that the 30 arc-second star is centered on the SXT LLOS. The micrometer A and B dial settings are recorded as X_S and Y_S, respectively. The horizon photometer output voltage is connected to the digital voltmeter and the micrometer A and B dials are adjusted until maximum voltage is indicated on the digital voltmeter. This voltage is recorded. Micrometer B dial is adjusted in a counterclockwise direction until the digital voltmeter indicates one-half of the maximum voltage recorded previously and then adjusted in a clockwise direction until the digital voltmeter indicates one-half of the maximum voltage recorded previously. Micrometer B dial settings for both the counterclockwise and clockwise directions are recorded and the average of these settings is calculated and recorded as Y_H. Micrometer B dial is set to Y_H. Micrometer A dial is adjusted in the counterclockwise direction and in the clockwise direction until the digital voltmeter indicates one-half of the maximum voltage recorded previously. Micrometer A dial setting for both the counterclockwise and clockwise directions are recorded and the average of these settings is calculated and recorded as X_H. Micrometer A dial is set to X_H. The coordinates of the horizon photometer LOS relative to the SXT LLOS is calculated by subtracting the micrometer A dial setting recorded as X_S from the micrometer A dial setting recorded as X_H. The result is the horizon photometer LOS to the SXT LLOS parallelism about the nav base Y axis. The micrometer B dial setting recorded as Y_S is subtracted from the micrometer B dial setting recorded as Y_H to calculate the horizon photometer LOS to the SXT LLOS parallelism about the nav base X axis.

The computer mode indication is checked by adjusting the intensity of a reference horizon photometer to produce an intensity of 2.4×10^{-4} watts/cm^2/steradian and obtaining a full scale deflection on the light intensity meter. VERB 15 NOUN 01 is entered into the DSKY and then address 00004_8 is entered. The DSKY will display 0----$_8$ in row 1 of mode register 0. The horizon photometer automatic mark command to the AGC is checked by noting the value of intensity of the reference horizon photometer, as indicated on the digital recorder, and then decreasing the intensity of the reference photometer until a mark command appears. The two intensity values are used to calculate the percent of the maximum intensity at which the mark command appeared. The DSKY will display 4----$_8$ in row 1 as an indication of the mark command.

To terminate this test, the optics are zeroed, the G and N mounting fixture is set to the 0 degree position, and the optics shroud is removed from between the SXT and the star and horizon simulator.

7-2.2.13 AGC Mode Control Test. This test checks the ability of the AGC to sequence the G and N system through its operating modes by entering information into the DSKY. Mode changes are indicated by the mode lamps on the IMU control panel and by displays on the DSKY. This test also checks the attitude signals sent to the spacecraft and checks the gimbal resolvers, the pitch-yaw resolver, and the fixed resolution transformer for proper operation.

The G and N mounting fixture is tilted to 32.5 degrees to simulate the G and N system in the spacecraft configuration. The zero encoder mode is initiated by entering data into the DSKY. The zero encoder mode drives the CDU's to zero. The CDU dial indications and the displays on the DSKY verify that the CDU's have been zeroed. The coarse align mode is then initiated and the IMU gimbals are driven to zero.

The inner gimbal digital to analog converter positive torquing rate is checked on the digital recorder by commanding the inner gimbal, middle gimbal, and outer gimbal angles to 60 degrees. The middle gimbal digital to analog converter negative torquing rate is checked on the digital recorder by commanding the inner gimbal, middle gimbal, and outer gimbal angles to 0 degree. The outer gimbal digital to analog converter positive torquing rate is checked on the digital recorder by commanding the inner gimbal, middle gimbal, and outer gimbal angles to 60 degrees. All three gimbals are torqued simultaneously to provide normal time sharing of the AGC in conjunction with the drive loops.

The CDU 1X resolver error signals are measured to verify that the IMU gimbals are at the angles indicated on the CDU's. The inner gimbal, middle gimbal, and outer gimbal 1X resolver sine and cosine voltage outputs are also measured to determine that the IMU gimbals are at 60 degrees. The phase angle of the inner gimbal, middle gimbal, and outer gimbal 1X resolver sine and cosine voltage outputs are also checked with respect to an 800 cps demodulator reference signal. The IMU CDU's and gimbals are driven to zero and the CDU 16X resolver in-phase nulls are measured to verify IMU and CDU angle coincidence.

The yaw body offset error scale factor also is checked. Error due to earth rate drift is minimized by adding 1 degree to the outer gimbal. The CDU manual mode is entered and the pitch error signal is nulled using the inner gimbal CDU thumbwheel. The polarity and phase angle of the yaw body offset error signal is checked to insure that an increasing angle results in positive voltage indications. The earth rate drift of the yaw body offset error is timed and then the magnitude and phase angle of the yaw body offset error signal is measured with a 5 degree offset of the middle gimbal. The yaw body error, roll body offset error, roll body error, and pitch error scale factors are checked by a similar method.

7-2.2.14 Gimbal Friction Test. During this test, gimbal torque motor voltages are monitored under dynamic conditions to detect frictional restraints of the inner, middle, and outer gimbals. The IRIG torquing signals are supplied by the AGC to rotate the gimbals in each direction. The resulting voltages are observed on the oscillograph.

The G and N mounting fixture is set to 32.5 degrees to simulate installation in the spacecraft. The system is placed in the CDU manual mode for zeroing of the CDU's. Outputs of the gimbal servo amplifiers and torque drive amplifiers are checked to verify null positions. The constant current supply to the ternary current switch is checked by measuring the precision voltage reference.

The oscillograph is set up to monitor gimbal torque motor voltages and gimbal servo error voltages. Gyro torquing signals are initiated through commands made using the DSKY and the outer and inner gimbals are rotated 360 degrees and the middle gimbal is rotated 120 degrees. To detect friction in the opposite direction, DSKY commands to the AGC are initiated to reverse torquing currents. The torque motor voltage indications on the oscillograph are observed to insure that amplitude is within specified limits.

7-2.2.15 Frequency and Step Response Test. This test checks proper response of the stabilization loop. Frequency response and bandwidth are measured by applying a range of signal generator frequencies to the input of the torque drive amplifier and monitoring the error signal at the preamplifier output. Stability of the loop is measured by alternately closing and opening a 12 volt dc test circuit to the input of the torque drive amplifier and observing the error signal.

The system is advanced to the fine align mode to allow normal functioning of the stabilization loop. Using the oscillograph signal selector panel, gimbal error signals are routed to the oscillograph. By means of the GIMBAL SERVO TEST switch on the test selector panel, signal generator outputs are applied to the inner, middle, and outer gimbal servo loops. Amplitude of error signals displayed on the oscillograph at various frequencies indicate frequency response of the loop. Bandwidth is indicated by noting the frequency at which the signal is attenuated 50 percent from a relative value at 0.1 cps.

A test circuit for generating a step input is formed by connecting a voltage dropping resistor across the 12 volt pulse torque supply and applying this voltage to the torque drive amplifier. The time required for the servo error to reach a constant value is measured as an indication of loop response. The number of overshoots after the test signal is removed are counted as a measure of loop stability.

7-2.2.16 IRIG Scale Factor Test. This test checks IMU gimbal rotation in response to the application of IRIG torquing pulses. A predetermined number of pulses is applied to the torque motors to cause a rotation of 360 degrees. The actual rotation is measured and used to determine scale factor.

The TRANSFER switch on the IMU control panel is set to COMPUTER to allow AGC control of the system through the DSKY. VERB 40 NOUN 20 is entered to initiate zero encoder mode. After 72 seconds are allowed for CDU zeroing, the system is advanced to the coarse align mode by entering VERB 41 NOUN 20. Using the DSKY, the outer gimbal angle and middle gimbal angle are set to zero, and the inner gimbal angle is set to position the X and Z IRIG's in the latitude plane (to minimize earth rate effects). The fine align mode is initiated by entering VERB 42 in the DSKY. A +00000 is entered to indicate no change in gimbal angles for fine align mode. The final preparatory step is adjustment of the G and N mounting fixture for a zero reading on the inner gimbal CDU.

The scale factor test is initiated by a sequence ended with +00001 entered into the DSKY. The AGC applies 4,096 bursts of torquing pulses to the torquing loop to rotate the inner gimbal 360 degrees. (Pulses are supplied in bursts to prevent overheating of the gyro.) After the rotation is complete, the AGC calculates the difference between the nominal scale factor and the actual scale factor and displays the error in parts per million on the DSKY display register. The scale factor in the opposite direction is measured in a similar manner by entering -00001 into the DSKY.

The procedure is repeated for measuring the scale factor of the X AND Z IRIG's using the outer and middle gimbals.

7-2.2.17 PIPA Scale Factor and Bias Test. During this test, the G and N mounting fixture is tilted to the 32.5 degree position to simulate a spacecraft position, an AGC program is used to control test sequence, and local gravity and latitude are used as known inputs.

The zero encoder mode is initiated to zero the CDU's by entering VERB 40 NOUN 20 into the DSKY. The zero encoder mode is completed in 72 seconds and, during this time, no other IMU operations or mode changes should be initiated. The coarse align mode is initiated after 72 seconds by entering VERB 41 NOUN 20 into the DSKY. The DSKY VERB-NOUN display will flash and indicate 21-22. This indication informs the operator that the AGC will accept the angles to which the IMU gimbals are to be positioned. Gimbal angles of 0 degree for the outer gimbal, -12.5 degrees for the inner gimbal, and +38.25 degrees for the middle gimbal are entered into the DSKY. This orientation of the IMU gimbals positions the PIP's so that each one will sense a portion of the local gravity vector and provide outputs resulting in + ΔV pulses. Internal PIPA loop signals are measured to indicate the PIPA loops positive velocity performance. VERB 25 NOUN 22 is then entered into the DSKY which programs the AGC to accept new angles for the IMU gimbals. The IMU gimbals are set to 0 degree for the outer gimbal, +167.5 degrees for the inner gimbal, and -38.25 degrees for the middle gimbal. This orientation of the IMU gimbals positions the PIP's so each PIP will sense a portion of the negative or minus local gravity vector. Loop parameters are measured to test the negative velocity performance.

The AGC is programmed for a test by entering VERB 21 NOUN 26 into the DSKY and then entering the priority of 4 to start the test. The internal priority of the test, which is 24, insures that lower priority programs such as a self-check cannot interrupt the test. (However, higher priority programs or DSKY keyboard commands could be used to override the test.) By entering VERB 20 NOUN 01 into the DSKY and then entering the address of the first register, the AGC is programmed to start the test. The test requires that local latitude information be entered or verified in the AGC. The AGC then sequences through the test and displays the test results on the DSKY registers. Register 1 contains the whole number of the measured gravity in centimeters per second squared, register 2 contains the fraction of the test results, and register 3 contains the PIPA test being performed (+00001 indicates +X PIPA test, +00002 indicates -X PIPA test, +00003 indicates +Z PIPA test, +00004 indicates -Z PIPA test, +00005 indicates +Y PIPA test, and +00006 indicates -Y PIPA test). The PIP temperature is measured at the end of the test to determine if the temperature is in tolerance and the test is valid.

To terminate this test, the AGC is programmed for a "fresh start" which clears the AGC registers, the control of the IMU is transferred to manual control, and the coarse align mode is selected. Calculations are performed using the measurements and test results obtained to determine the scale factor and bias deviation for each PIPA.

7-2.2.18 G and N Fine Alignment Test. This test checks the misalignment between the SXT S_tLOS and LLOS to each PIP input axis. This test is an automatic AGC program test. Local latitude and initial SXT alignment are required inputs to the AGC prior to performing this test.

The G and N mounting fixture is tilted to 32.5 degrees to simulate the G and N system in the spacecraft configuration. A low priority of 04 and the address of the first register are entered into the DSKY. Local latitude is then entered into the DSKY. The test is begun by entering VERB 33 (proceed without data) and then entering 00001 into the DSKY. Entering 00001 into the DSKY programs the AGC to align the IMU with two PIP's horizontal using the following SXT angles as references. The SXT shaft is set to approximately 180 degrees and the SXT trunnion is set to approximately 33 degrees. The SXT horizontal reticle line is then aligned to the horizontal reticle line and dot of target number 1. At the instant of coincidence the MARK pushbutton is pressed to enter the SXT angles into the AGC. The SXT shaft is then set to approximately 241 degrees and the SXT trunnion is set to approximately 53 degrees. The SXT central reticle line is then aligned with the central dot of target number 4 and at the instant of coincidence the MARK pushbutton is pressed to enter the SXT angles into the AGC. The AGC will use the two sets of SXT angles to align the IMU and then the apparent misalignment is displayed on the DSKY. Misalignment is determined by the amount of gravity sensed by the horizontal PIP's. This procedure is repeated two more times to determine the misalignment between the SXT S_tLOS and the LLOS and each set of horizontal PIP's (X and Y PIP's, X and Z PIP's, and the Y and Z PIP's).

7-2.2.19 IRIG Coefficient Determination Test. This test is an AGC-controlled measurement of gyro drift. The PIP outputs and CDU encoder outputs are used to measure gyro drift. which is displayed on the DSKY. Displays of registers R1, R2, and R3 are noted in each of 15 different test measurements. Registers R1 and R2 display test results in double precession form. Register R3 identifies the test position. Through JDC data sheet calculations, values for each of the three characteristic drifts are determined: normal bias drift (NBD), drift due to acceleration along the spin reference axis (ADSRA), and drift due to acceleration along the input axis (ADIA).

In test position +00001, bias drift of the Y IRIG is measured. The G and N mounting fixture is set to 32.5 degrees to simulate the IMU position in the spacecraft. After the program is initiated through the DSKY, latitude values for the site location are entered. Upon entering VERB 33 and pressing the ENTER pushbutton, register R1 displays the nav base position in degrees, register R2 identifies the type of sensing device (+00000 for PIP and +00001 for CDU), and register R3 displays the IMU test position. Repeating the VERB 33 entry initiates the test. The stable member is oriented to place the output axis of the Y IRIG vertical (to eliminate mass unbalance effects) and the input axis south. The IRIG develops a signal proportional to sensed earth rate and bias drift, and torques the inner gimbal at this rate. The Z PIP is rotated from its initial horizontal position in earth space and develops a signal, due to the sensed gravity, representing Y IRIG bias drift and components of earth rate. Four readings of the PIP pulses are made by the AGC at intervals of 90 seconds. The AGC displays on the DSKY a value of earth rate and bias drift. Through calculations on the JDC data sheet, bias drift is isolated from earth rate. The bias drift is compared to ISS test results to determine if required tolerances are met. In test positions +00002 and +00003, the bias drift of the Z and X IRIG's is measured in a similar manner using the output of the Y PIP.

In test position +00004, the ADSRA coefficient of the Y IRIG is measured. The input axis of the Y IRIG is positioned south and its output axis is positioned east. The gyro torques the inner gimbal at a rate proportional to earth rate, bias drift, and ADSRA. The Z PIP senses a component of gravity due to the rotation and transmits a signal to the AGC. The AGC displays on the DSKY a value representing earth rate, bias drift, and ADSRA. Using the JDC data sheet, the known values of earth rate and values of bias drift obtained in the previous test are subtracted from the reading to determine ADSRA. The ADSRA's of the Z and X IRIG's are found based on outputs of the X and Z PIP's from test positions +00005 and +00006, respectively.

In test position +00007, ADIA difference measurements of the Y and Z IRIG's similar to those made in the spacecraft are performed. The input axis of the Y IRIG is positioned at an angle 45 degrees upward from north. The Z input axis is positioned at an angle 45 degrees upward from south. The Y and Z IRIG outputs cause the X PIP to rotate at a rate proportional to the horizontal component of earth rate, the PIP bias drifts, ADSRA's, and ADIA's. The rotation is sensed by the X PIP which initiates a digital signal for display on the DSKY. The results are recorded for reference use during spacecraft tests.

In test position +00008, ADIA measurements of the X and Y IRIG's are made using the output of the Z PIP. In test position +00009, measurements of the X and Z IRIG's are made using outputs of the Y PIP.

After completion of the nine bias drift, ADSRA, and ADIA reference tests, six ADIA measurements are made to insure that the ADIA is within specified tolerances. In test position +00001, the G and N mounting fixture is set at 0 degree using the SXT. The X IRIG then senses earth rate, bias drift, and ADIA. Beginning with the outer gimbal, the resulting outer gimbal angle rotoation is sensed by the CDU, transmitted to the AGC in the form of encoder pulses, and, after processing, the rotation rate is displayed on the DSKY. In test position +00002, the step is repeated with the inner gimbal rotated 180 degrees to obtain opposing results. New readings displayed on the DSKY are subtracted from the initial readings. The bias drift cancels out in the subtraction process, leaving only earth rate and ADIA. The known value of earth rate is then subtracted, leaving only ADIA. To measure Z ADIA, measurements are taken with the inner gimbal set to 90 degrees and 270 degrees. To measure Y ADIA, the G and N mounting fixture is set to -90 degrees and the outer gimbal is set to 90 degrees and 270 degrees.

After completion of the test, VERB 34 is entered into the DSKY to terminate the program.

7-2.2.20 IMU Operational Check. The IMU operational check consists of a gravity measurement to check PIP operation and an earth rate measurement to check IRIG operation.

The G and N mounting fixture is set to 32.5 degrees to simulate spacecraft installation. The TRANSFER switch on the IMU control panel is set to COMPUTER to allow AGC control of the test. The AGC program is selected by entering VERB 20 NOUN 01 and address 55711 in the DSKY. Through AGC action the system advances to the fine align mode. The gimbals align to a position at which gravity is sensed equally by all PIP's and the horizontal component of earth rate is sensed equally by all IRIG's. After a 5-1/2 minute measurement period, the AGC displays gravity in centimeters per second squared on the DSKY. Entering VERB 33 causes the AGC to display the horizontal component of earth rate as sensed by the IRIG's and measured by the PIP's. Entering VERB 34 terminates the test.

7-2.2.21 Gyro Compassing Test. This test checks the ability of the stable platform to maintain a local vertical erection with the Z_{SM} axis at an easterly azimuth. The effects of high and low prime power on power supply outputs are also checked during this test. The erection on the stable platform is maintained by the AGC prelaunch alignment program, which utilizes the local gravity output of the Y and Z PIP's to provide an earth reference. Gyro coefficients and local latitude are inserted into the AGC program and the IMU gimbal angles are checked against angles obtained from the AGC, based on optical sightings, to determine if the stable platform is maintained at local vertical.

The optics CDU's are first zeroed then driven to an optics reference of 270 degrees for the shaft angle and 0 degree for the trunnion angle. The G and N mounting fixture is tilted, while sighting through the SXT eyepiece, until the horizontal reticle line of the SXT is coincident with dot and horizontal reticle line of target number 1. The control stick is manipulated, while sighting through the SXT S_tLOS, until the vertical reticle line of the SXT is coincident with dot and vertical reticle line of target number 1. At the instant of coincidence, the MARK pushbutton is pressed to enter the optics angles into the AGC. The SXT S_tLOS is then aligned to an azimuth of 135 degrees with a shaft angle of 270 degrees and a trunnion angle of 45 degrees. The control stick is manipulated, while sighting through the SXT eyepiece, until the center of the SXT reticle is coincident with the reticle dot of target number 3. At the instant of coincidence, the MARK pushbutton is pressed to enter the optics angles into the AGC. The AGC program then zeros the IMU CDU's.

Local latitude is inserted into the AGC program and then the AGC computes the desired IMU CDU angles and displays these angles on the G and N AGC DSKY. The desired angles are recorded and these angles are used as a reference during the test. The stable platform is then erected to local vertical with Z_{SM} axis at an easterly azimuth by torquing the middle gimbal to 270 degrees and the outer and inner gimbals to 0 degree. Gyro coefficients are then inserted into the AGC program. The IMU CDU angles, as displayed on the G and N AGC DSKY, are then recorded every 15 minutes for 7 hours. After two hours, the IMU CDU angles displayed on the G and N AGC DSKY are recorded and subtracted from the previously recorded desired angles and then, every 15 minutes for the remaining 5 hours, the angles displayed on the G and N AGC DSKY are recorded and subtracted from the angles recorded at the end of the 2 hour period. This procedure checks the gyro compassing capability of the stable platform.

The effect of high and low power inputs to the power supplies is checked by setting the power supply input power above and below the nominal 27.5 volt dc input. The power supply input power is set to 25.8 volts dc by adjusting the AGE VOLTAGE ADJUST control on the test control panel. The outputs of various power supplies are then checked. The input power is then set to 30.8 volts dc and again the outputs of the same power supplies are checked.

To terminate this test, the power supply input power is set to the nominal 27.5 volts dc, the AGC is programmed for "Not In Use" operation, and the IMU gimbal angles are set to 0 degree while in the coarse align mode.

7-2.2.22 AGC Operational Test. During this test, the main panel and G and N AGC DSKY's alarm displays and alarm circuitry are checked by commands entered into both DSKY's. The AGC instruction words and control pulses are checked as well as AGC to spacecraft and telemetry interface. All DSKY functions are verified and the ability of the AGC to accept data loaded through the DSKY's is checked.

The IMU is moded to the manual coarse align mode. The brightness control of each DSKY is checked by loading +88888 into the DSKY's and varying the brightness controls from full on to full off. The ability to clear information from the display registers is checked. Data is loaded into the AGC and read out again to verify proper DSKY operation.

A program to light certain DSKY lamps is then entered into the AGC. The following lamps are lighted: ACTIVITY COMP lamp on the G and N AGC DSKY and on the main panel DSKY, and the telemetry lamp on the CTS. The UPTEL, PROGRAM ALARM, COMP FAIL, CHECK FAIL, KEY RELEASE, RUPT LOCK, PARITY FAIL, TC TRAP, and COUNTER FAIL lamps are checked for both DSKY's. The AGC instruction words and control pulses are then checked by programming the AGC for an AGC self-check program. The T3 RUPT, PARITY FAIL, TC TRAP, and RUPT LOCK signals are generated by the AGC program to check the failure detection circuitry in the AGC. The ENGINE ON signal generated by the AGC program is routed to the oscilloscope to monitor signal characteristics. A checkerboard pattern (25252) is entered in the DSKY's to check all locations in erasable memory which are the telemetry monitor locations. The telemetry output is routed to the oscilloscope to monitor signal characteristics.

The UPLINK circuitry is then checked by the following operations. An UPLINK tape is prepared on the CTS and then used to feed data into the AGC via the CTS. The DSKY's are checked to verify that the information from the UPLINK tape is received correctly by the AGC. The AGC discretes to the spacecraft and the inputs from the spacecraft are checked with signals generated by the CTS. Power failure circuitry is checked by varying the +13 volt and +3 volt dc voltages of the AGC to low and high limits and observing failure indicating lamps.

7-3 INERTIAL SUBSYSTEM (ISS)

7-3.1 PREPARATION. Refer to tables 7-I and 7-III for setup and cabling instructions for checkout of the ISS.

7-3.2 CHECKOUT. The ISS master flowgram (figure 7-4) specifies the conditions leading to an ISS checkout. Detailed flowgrams (figures 7-5 and 7-6) give sequential listings of JDC's to be performed.

7-4 OPTICAL SUBSYSTEM (OSS)

7-4.1 PREPARATION. Refer to tables 7-I and 7-IV for setup and cabling instructions for checkout of the OSS.

7-4.2 CHECKOUT. The OSS master flowgram (figure 7-7) specifies the conditions leading to an OSS checkout. Detailed flowgrams (figures 7-8 and 7-9) give sequential listings of JDC's to be performed.

7-5 COMPUTER SUBSYSTEM (CSS)

7-5.1 PREPARATION. Refer to tables 7-I and 7-V for setup and cabling instructions for checkout of the CSS.

7-5.2 CHECKOUT. The CSS master flowgram (figure 7-10) specifies the conditions leading to a CSS checkout. Detailed flowgrams (figures 7-11, 7-12, and 7-13) give sequential listings of JDC's to be performed.

Table 7-1. Equipment Required for Checkout

Equipment	Part Number	Used in			
		G and N System	ISS	OSS	CSS
G AND N SYSTEM COMPONENTS					
AGC	1003770	X			X
AGC main panel DSKY	1003707	X			X
AGC navigation panel DSKY	1003706	X			X
CDU	1015500-021 1015500-031	X(3) X(2)	X(3)	X(2)	
CDU frame	1016885-021	X	X	X	
CDU panel	1017538-021	X	X	X	
Condition annunciator assembly	1023014-011	X			
Control electronics	1015064-021	X	X	X	
D and C electronics	1015065-041	X	X	X	
G and N harness	1015086-000	X			
G and N indicator control panel	1014664-011	X		X	
IMU	1001500-021, -031	X	X		
IMU control panel	1014628-011	X	X		
Navigation base and optical unit assembly	1899950-041	X		X	
Optics cover	1014532	X			

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Table 7-1. Equipment Required for Checkout (cont)

Equipment	Part Number	Used in			
		G and N System	ISS	OSS	CSS
Optics shroud	1014502	X			
PSA toe cap	1008135	X			
PSA tray 1	1007571-011	X	X		
PSA tray 2	1007572-011	X	X	X	
PSA tray 3	1007573-011	X	X		
PSA tray 4	1007574-011	X	X		
PSA tray 5	1007575-011	X	X		
PSA tray 6	1007576-011	X	X	X	
PSA tray 7	1007577-011	X	X	X	
PSA tray 8	1007578-011	X	X	X	
PSA tray 9	1007579-011	X	X	X	
PSA tray 10	1007580-011	X	X	X	
Tracker X and Y assembly	1007585	X			
GSE					
Adjustable mirror	1019759	X			
Alignment certification fixture	1017387			X	
Alignment mirror	1016951			X	
AGC/CS	1020344				X

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Table 7-1. Equipment Required for Checkout (cont)

Equipment	Part Number	Used in			
		G and N System	ISS	OSS	CSS
AGC-OC	1020342	X			X
AGC handling fixture	1020001				X
AGC simulator	1014061-011		X	X	
AGC sling	N/A	X			X
Coolant hose	1900866-011	X(6)	X(2)	X(4)	
Coolant hose	1900866-021		X(2)		
Coolant hose	1900867-011	X			
Coolant hose	1900867-021		X	X	
Coolant hose	1901663-011	X			
Coolant hose	1901663-021		X	X	
CTS	1020341	X			X
Degausser	1900299-011	X	X		
Electronic level	1901328			X	
G and N mounting fixture	1902204-011	X	X	X	
G and N test interconnection kit	1020313	X			
G and N transportation cart	1900009-021	X	X	X	X
ICTC	1900342-011	X	X		
IMU mounting fixture	1900012-011		X		

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Table 7-1. Equipment Required for Checkout (cont)

Equipment	Part Number	Used in			
		G and N System	ISS	OSS	CSS
IMU mounting fixture alignment set	1900800-011		X		
IMU pressure seal tester	1900804-011		X		
IMU sling	N/A	X	X		
Interconnect cables	1902299	X	X	X	
OITS	1902300-011	X	X	X	
Optics/nav. base handling fixture	1901426-011	X			
Optics/nav. base mounting fixture	1902301-011			X	
Pedestal mount	1020195	X			
Portable light assembly	1019837			X	
PSA mounting fixture	1900606-021		X		
PSA test point adapter	1901981-011	X	X	X	
PSA tray extender set	1900805-011	X	X		
Remote optics controller	1902046-011			X	
Retro-reflecting prism	1019840			X	
Rotary table	1900926-011		X	X	
Rotary table calibration set	1900810-011		X		
Shaft accuracy tester	1019769			X	

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Table 7-1. Equipment Required for Checkout (cont)

Equipment	Part Number	Used in			
		G and N System	ISS	OSS	CSS
SJB	1902195-011		X	X	
Star and horizon simulator	1019900	X		X	
Subsystem test interconnection kit	1020312				X
Theodolite	1017447	X		X	
Tool kit	N/A	X	X	X	X
Variable deviation wedge	1017376	X			
Vertical leveling mirror	1017445	X		X	
0^{o} autocollimator assembly	1017380	X		X	
45^{o} autocollimator assembly	1017381	X			

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Table 7-II. G and N System Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W1	1900886	P1/J1 P2/J1	OIA Oscillograph
W2	1900669	P1/J2 P2/J2	OIA Oscillograph
W3	1900670	P1/J3 P2/J3	OIA Oscillograph
W4	1900671	P1/J4 P2/J4	OIA Oscillograph
W10	1900976	P1/J10 P2/J12	OIA PSA test point adapter
W11	1900975	P1/J11 P2/J13 P3/P3	OIA PSA test point adapter W31
W18	1900974	P1/J19 P2/J2	OIA PSA tray 7
W19	1900873	P1/J20 P2/J3	OIA G and N coolant and power console
W22	1900959	P1/J23 P2/J5	OIA CTS
W25	1900918	P1/J26 P2/J7	OIA OJB
W26	1900921	P1/A30J1 P2/facility	OIA Wall power
W27	1900871	P1/A30J2 P2/J1	OIA G and N coolant and power console
W28	1900872	P1/J2 P2/facility	G and N coolant and power console Wall power
W29	1900879	P1/J4 P2/J6	G and N coolant and power console OJB

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Table 7-II. G and N System Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W31	1901302	P1/J16 P2/J2 P3/P3	OIA AGC/PSA/SC adapter assembly W11
W33	1901404	P1/E1 P2/E4	OIA Oscillograph
W34	1901614	P1/E1 P2/E300	G and N coolant and power console Rotary table
W35	1901660	P1/E1 P2/E300	OIA Rotary table
W37	1901662	P1/facility P2/E300	Facility ground Rotary table
W55	1902374	P1/J40 P2/56P11 P3/E2	OJB G and N harness G and N mounting fixture cradle
W59	1902366	P1/J46 P2/56P12 P3/E2	OJB G and N harness G and N mounting fixture cradle
W64	1901676	P1/E1 P2/E300	G and N mounting fixture base Rotary table
W65	1900739	P1/J4 P2/J15	Current source monitor panel PSA test point adapter
W66	1901677	P1/E2 P2/E1	G and N mounting fixture cradle G and N mounting fixture base
W69	1901680	P1/E80 P2/E1	OIA G and N mounting fixture base
W83	1901879	P1/P4 P2/56P9 P3/J1	W96 G and N harness Signal conditioner
W85	1901960	P1/A30J5 P2/facility	OIA Aux wall power
W86	1902095	P1/E1 P2/E1	CTS G and N mounting fixture base

Table 7-II. G and N System Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W96	1902347	P1/J6	OIA
		P2/J7	OIA
		P3/J12	OIA
		P4/P1	W83
		P5/J1	Star and horizon simulator
W98	1902369	P1/E1	OJB
		P2/E1	G and N mounting fixture base
W200	1020241	P1/J1	Buffer assembly
		P2/E1	CTS
W201	1020242-1	P1/J2	Buffer assembly
		P2/J9	CTS
W202	1020242-2	P1/J3	Buffer assembly
		P2/J13	CTS
W203	1020244	P1/J9	Buffer assembly
		P2/J14	CTS
W207	1020253	P1/	AGC/CS
		P2/	AGC/CS
		P3/	AGC/CS
		P4/J7	Buffer assembly
		P5/J8	Buffer assembly
		P6/J2	W209
		P7/	AGC/CS
		P8/	AGC/CS
W209	1020284	P1/J1	AGC/PSA/SC adapter assembly
		P2/J8	CTS
		P3/J2	CTS
		P4/J7	CTS
		P5/J11	CTS
		J1/P2	W211
		J2/P6	W207
W211	1020330	P1/J1	Main panel DSKY
		P2/J1	W209

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Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W1	1900886	P1/J1 P2/J1	OIA Oscillograph
W2	1900669	P1/J2 P2/J2	OIA Oscillograph
W3	1900670	P1/J3 P2/J3	OIA Oscillograph
W4	1900671	P1/J4 P2/J4	OIA Oscillograph
W5	1900916	P1/J5 P2/J10	OIA OJB
W6	1900907	P1/J6 P2/J5	OIA OJB
W7	1900908	P1/J7 P2/J11	OIA OJB
W8	1900983	P1/J8 P2/J9	OIA SJB
W9	1900982	P1/J9 P2/J10	OIA SJB
W10	1900976	P1/J10 P2/J12	OIA PSA test point adapter
W11	1900975	P1/J11 P2/J13 P3/P3	OIA PSA test point adapter W38
W12	1900981	P1/J13 P2/J8	OIA SJB

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Table 7-III. Inertial Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W13	1900984	P1/J14 P2/J6	OIA SJB
W14	1900985	P1/J15 P2/J7	OIA SJB
W15	1900906	P1/J16 P2/J4	OIA OJB
W16	1900876	P1/J17 P2/J3	OIA OJB
W17	1900875	P1/J18 P2/J9	OIA OJB
W18	1900974	P1/J19 P2/J2	OIA PSA tray 7
W19	1900873	P1/J20 P2/J3	OIA G and N coolant and power console
W20	1900878	P1/J21 P2/J8	OIA OJB
W21	1900977	P1/J22 P2/J5	OIA SJB
W23	1900877	P1/J24 P2/J2	OIA OJB
W25	1900918	P1/J26 P2/J7	OIA OJB
W26	1900921	P1/A30J1 P2/facility	OIA Wall power
W27	1900871	P1/A30J2 P2/J1	OIA G and N coolant and power console

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Table 7-III. Inertial Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W28	1900872	P1/J2 P2/facility	G and N coolant and power console Wall power
W29	1900879	P1/J4 P2/J6	G and N coolant and power console OJB
W30	1901403	P1/E80 P2/E300	OIA Rotary table
W33	1901404	P1/E1 P2/E4	OIA Oscillograph
W34	1901614	P1/E1 P2/E300	G and N coolant and power console Rotary table
W35	1901660	P1/E1 P2/E300	OIA Rotary table
W36	1901661	P1/E319 P2/E300	SJB Rotary table
W37	1901662	P1/facility P2/E300	Facility ground Rotary table
W38	1900930	P1/J22 P2/J11 P3/P3	OJB SJB W11
W39	1900928	P1/J25 P2/J12	OJB SJB
W40	1900927	P1/J26 P2/J13	OJB SJB
W41	1900961	P1/J21 P2/J15	OJB SJB
W42	1900992	P1/J27 P2/J14	OJB SJB
W47	1900990	P1/J32 P2/P1 P3/E2	OJB Outer gimbal CDU G and N mounting fixture cradle

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Table 7-III. Inertial Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W48	1900993	P1/J33 P2/P1 P3/E2	OJB Middle gimbal CDU G and N mounting fixture cradle
W53	1900980	P1/J38 P2/P1 P3/E2	OJB Inner gimbal CDU G and N mounting fixture cradle
W60	1900989	P1/J1 P2/J1	SJB IMU
W61	1900991	P1/J2 P2/J2	SJB IMU
W62	1900987	P1/J3 P2/J3	SJB IMU
W63	1902330	P1/J4 P2/J4	SJB IMU
W64	1901676	P1/E1 P2/E300	G and N mounting fixture base Rotary table
W65	1900739	P1/J4 P2/J15	Current source monitor panel PSA test point adapter
W66	1901677	P1/E2 P2/E1	G and N mounting fixture cradle G and N mounting fixture base
W85	1901960	P1/A30J5 P2/facility	OIA Aux wall power
W87	1902309	P1/J43 P2/J44 P3/J47 P4/J9 or P4/P4 P5/P10 P7/J17 E9/E2	OJB OJB OJB G and N indicator control panel or W93 W88 SJB G and N mounting fixture cradle

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Table 7-III. Inertial Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W88	1902308	P1/J34	OJB
		P2/J39	OJB
		P3/J45	OJB
		P4/P1	IMU control panel
		P5/J1	D and C electronics
		P6/J1	Control electronics
		P10/P5	W87
		E11/E2	G and N mounting fixture cradle
		E12/E2	G and N mounting fixture cradle
		E13/E2	G and N mounting fixture cradle
W93	1902349	P1/P4	W87
		P2/J2	Remote optics controller
W98	1902369	P1/E1	OJB
		P2/E1	G and N mounting fixture base

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Table 7-IV. Optical Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W1	1900886	P1/J1 P2/J1	OIA Oscillograph
W2	1900669	P1/J2 P2/J2	OIA Oscillograph
W3	1900670	P1/J3 P2/J3	OIA Oscillograph
W4	1900671	P1/J4 P2/J4	OIA Oscillograph
W5	1900916	P1/J5 P2/J10	OIA OJB
W10	1900976	P1/J10 P2/J12	OIA PSA test point adapter
W11	1900975	P1/J11 P2/J13	OIA PSA test point adapter
W12	1900981	P1/J13 P2/J8	OIA SJB
W13	1900984	P1/J14 P2/J6	OIA SJB
W14	1900985	P1/J15 P2/J7	OIA SJB
W17	1900875	P1/J18 P2/J9	OIA OJB
W19	1900873	P1/J20 P2/J3	OIA G and N coolant and power console
W20	1900878	P1/J21 P2/J8	OIA OJB
W24	1900917	P1/J25 P2/J1	OIA OJB

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Table 7-IV. Optical Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W25	1900918	P1/J26 P2/J7	OIA OJB
W26	1900921	P1/A30J1 P2/facility	OIA Wall power
W27	1900871	P1/A30J2 P2/J1	OIA G and N coolant and power console
W28	1900872	P1/J2 P2/facility	G and N coolant and power console Wall power
W29	1900879	P1/J4 P2/J6	G and N coolant and power console OJB
W33	1901404	P1/E1 P2/E4	OIA Oscillograph
W34	1901614	P1/E1 P2/E300	G and N coolant and power console Rotary table
W35	1901660	P1/E1 P2/E300	OIA Rotary table
W37	1901662	P1/facility P2/E300	Facility ground Rotary table
W45	1900960	P1/J30 P2/J20	OJB SJB
W64	1901676	P1/E1 P2/E300	G and N mounting fixture base Rotary table
W66	1901677	P1/E2 P2/E1	G and N mounting fixture cradle G and N mounting fixture base
W67	1901678	P1/E219 P2/E2	GSE-PSA junction box G and N mounting fixture cradle
W68	1901679	P1/E300 P2/E100	Rotary table TJB
W69	1901680	P1/E80 P2/E1	OIA G and N mounting fixture base

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Table 7-IV. Optical Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W85	1901960	P1/A30J5	OIA
		P2/facility	Aux wall power
W87	1902309	P1/J43	OJB
		P2/J44	OJB
		P2/J47	OJB
		P4/J1 or	W93 or
		P4/J9	G and N indicator control panel
		P5/P10	W88
		P7/J17	SJB
		E9/E2	G and N mounting fixture cradle
W88	1902308	P1/J34	OJB
		P2/J39	OJB
		P3/J45	OJB
		P4/	Not used
		P5/J1	D and C electronics
		P6/J1	Control electronics
		P10/P5	W87
		E11/E2	G and N mounting fixture cradle
		E12/E2	G and N mounting fixture cradle
		E13/E2	G and N mounting fixture cradle
W89	1902346	P1/J6	OIA
		P2/J7	OIA
		P3/J12	OIA
		P4/J16	SJB
W90	1902365	P1/P8	Telescope
		P2/P4	Sextant
		P3/P5	Sextant
		P4/J3	TJB
		P5/J4	TJB
		P6/P13	Tracker X and Y assembly
W91	1902338	P1/J19	SJB
		P2/J5	Trunnion CDU
		E7/E2	G and N mounting fixture cradle

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Table 7-IV. Optical Subsystem Interconnect Cables (cont)

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W92	1902339	P1/J18 P2/J4 E6/E2	SJB Shaft CDU G and N mounting fixture cradle
W93	1902349	P1/P4 P2/J2	W87 Remote optics controller
W94	1902337	P1/J31 P2/J1	SJB TJB
W95	1902340	P1/J32 P2/J5	SJB TJB
W97	1902381	P1/J1 P2/J5	Star and horizon simulator TJB
W98	1902369	P1/E1 P2/E1	OJB G and N mounting fixture base

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Table 7-V. Computer Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
All interconnect cables for the CSS are contained in Subsystem Test Interconnection Kit, Part Number 1020312, and G and N Test Interconnection Kit, Part Number 1020313.			

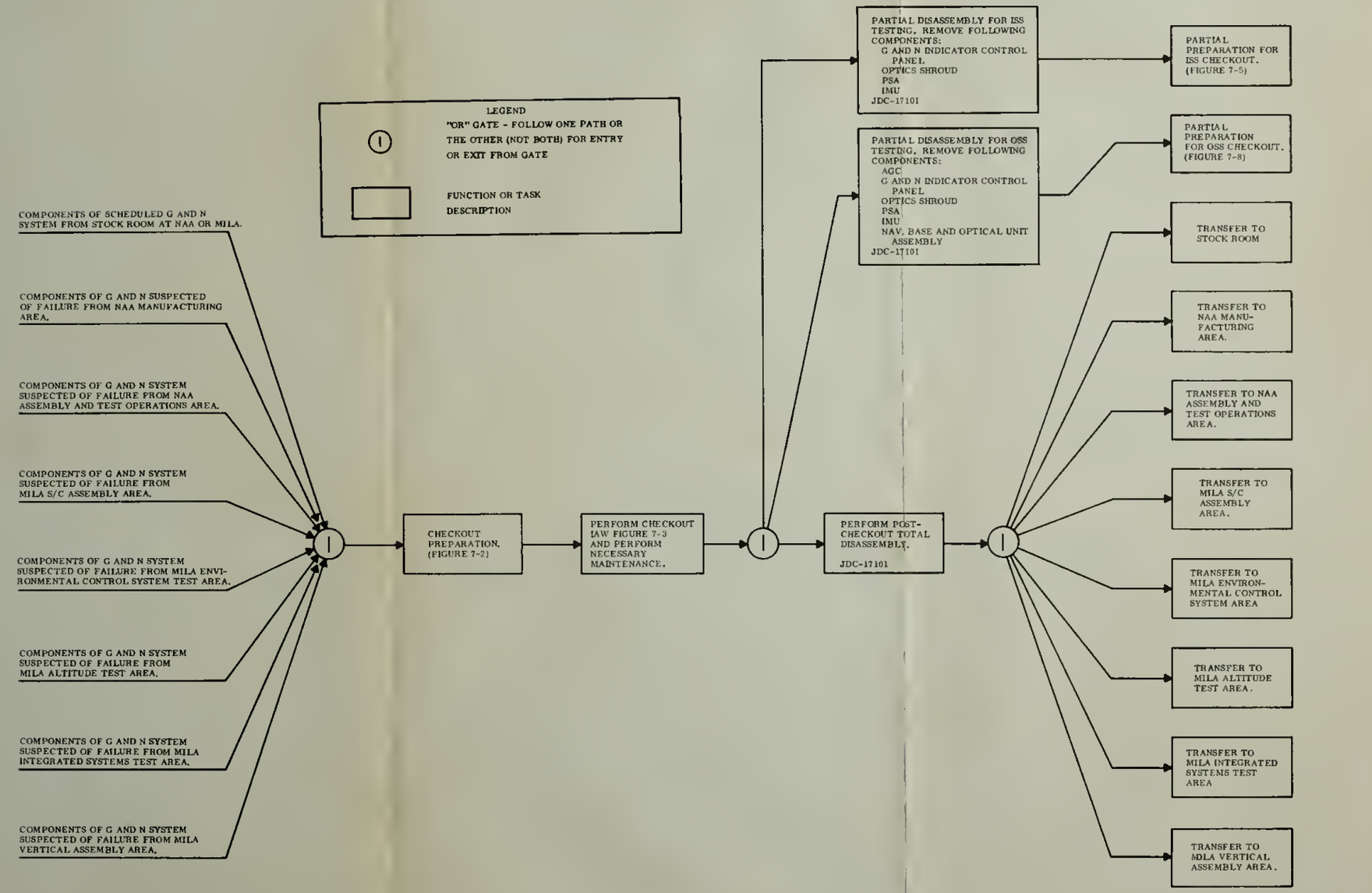

Figure 7-1. G and N System Checkout Master Flowgram

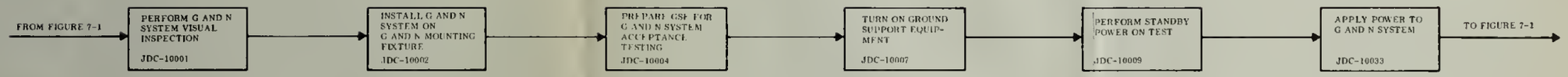

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Figure 7-2. G and N System Checkout Preparation Flowgram

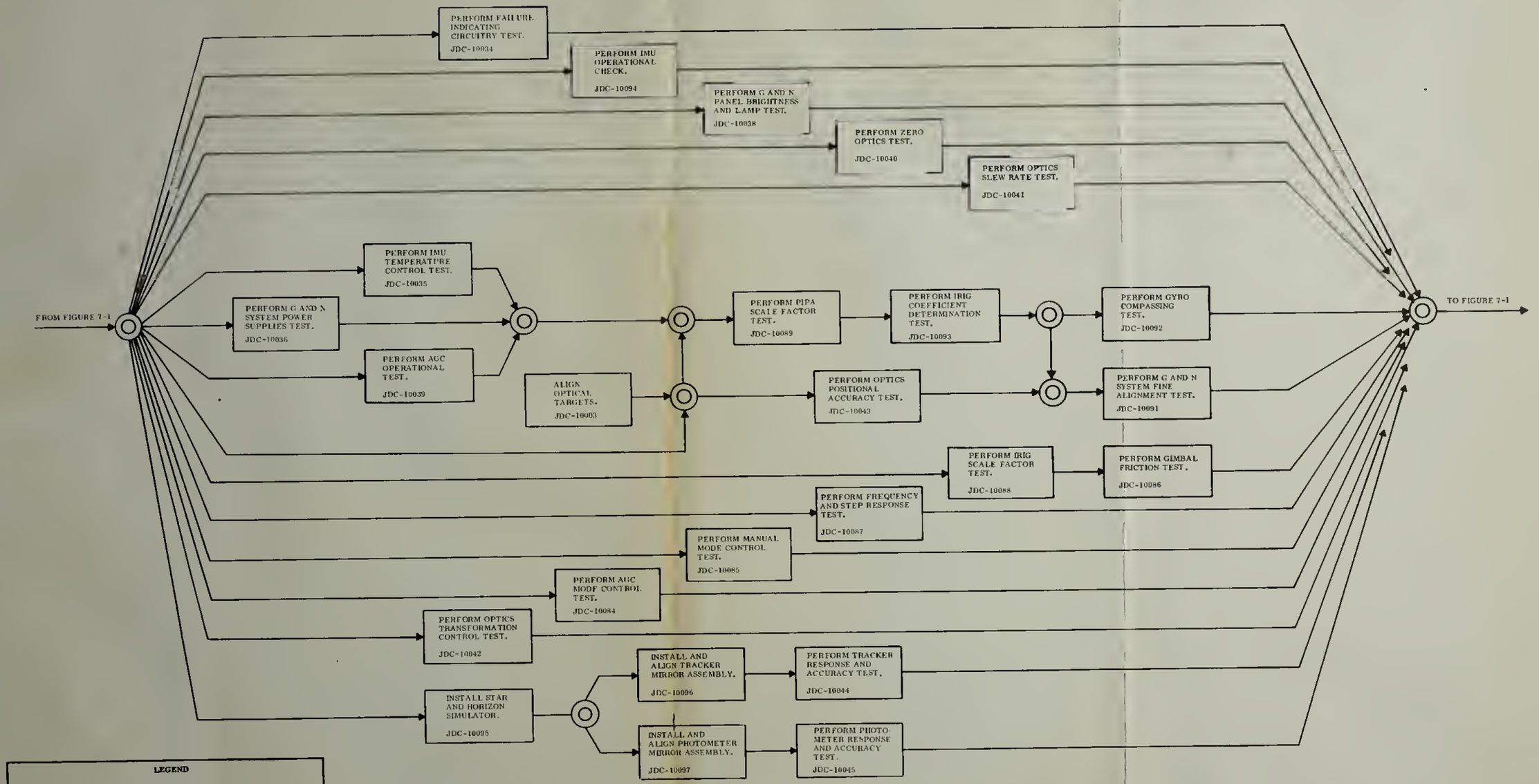


Figure 7-3. G and N System Checkout Flowgram

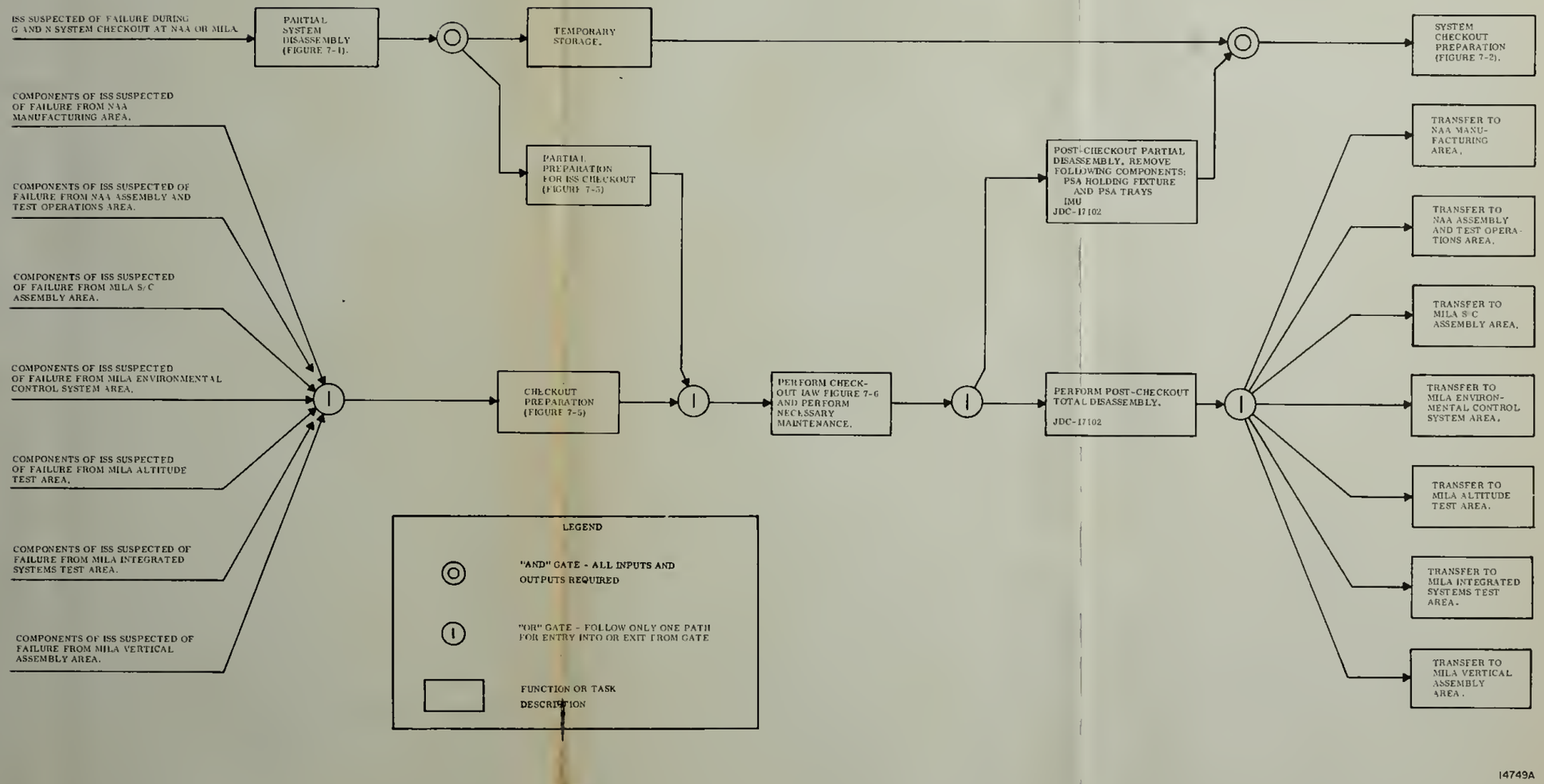
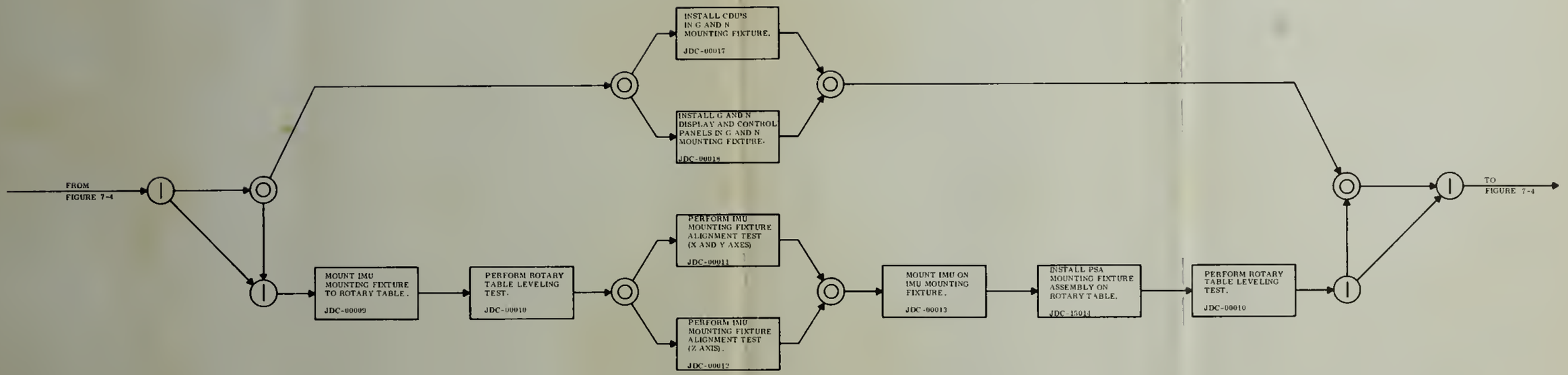


Figure 7-4. ISS Checkout Master Flowgram



14750-A

Figure 7-5. ISS Checkout Preparation Flowgram

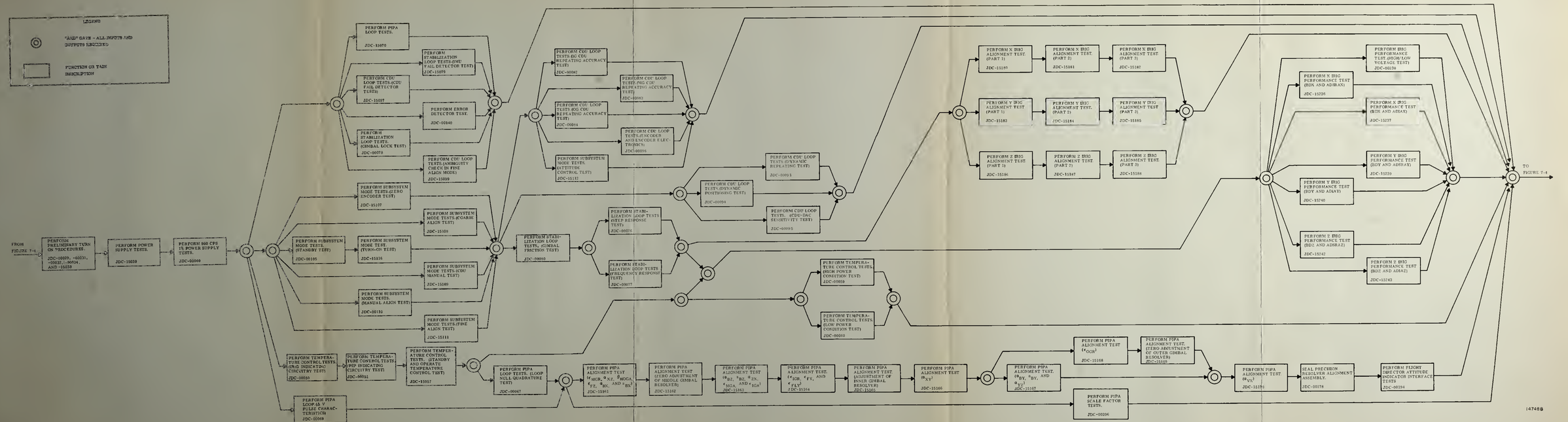


Figure 7-6. ISS Checkout Flowgram

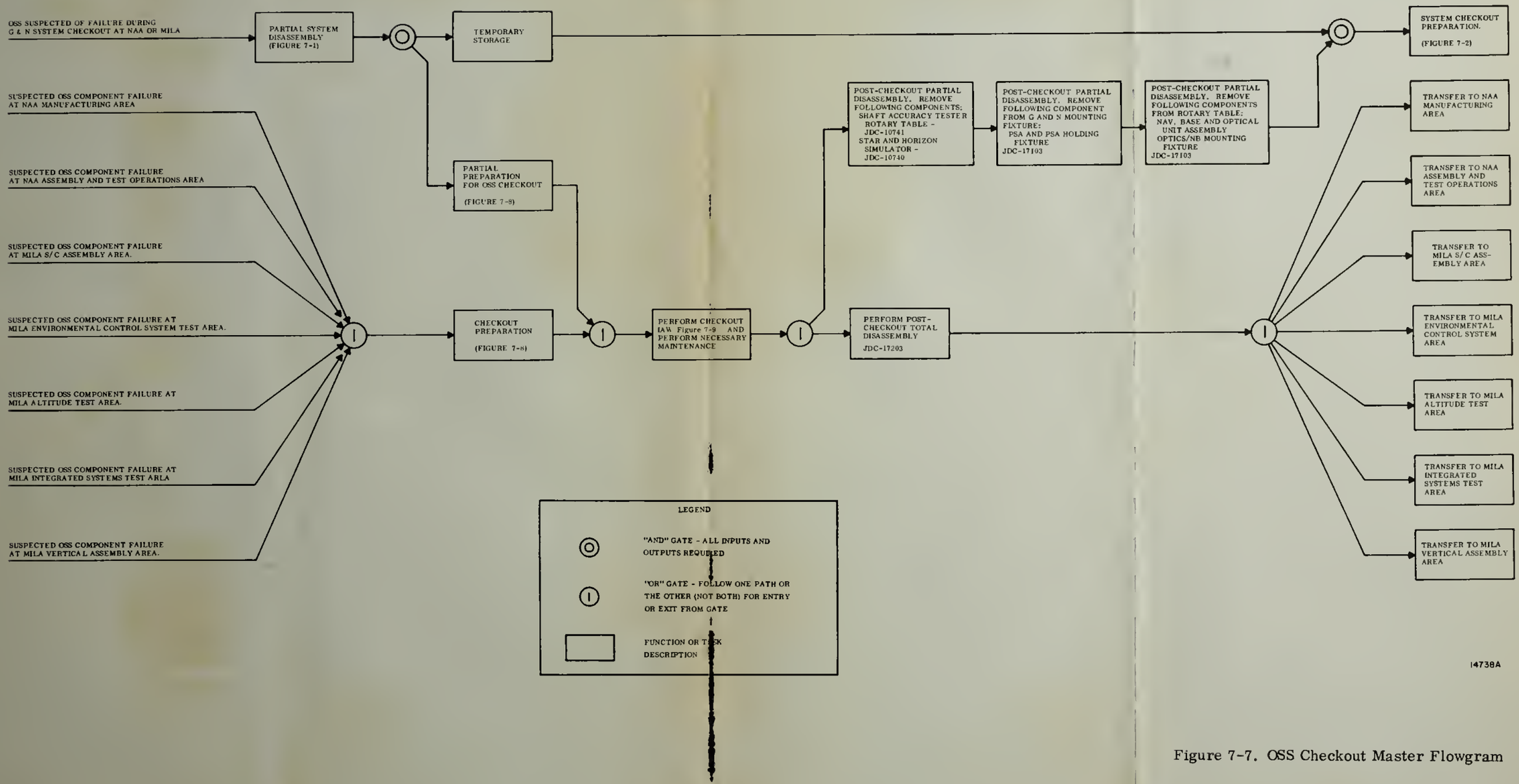


Figure 7-7. OSS Checkout Master Flowgram

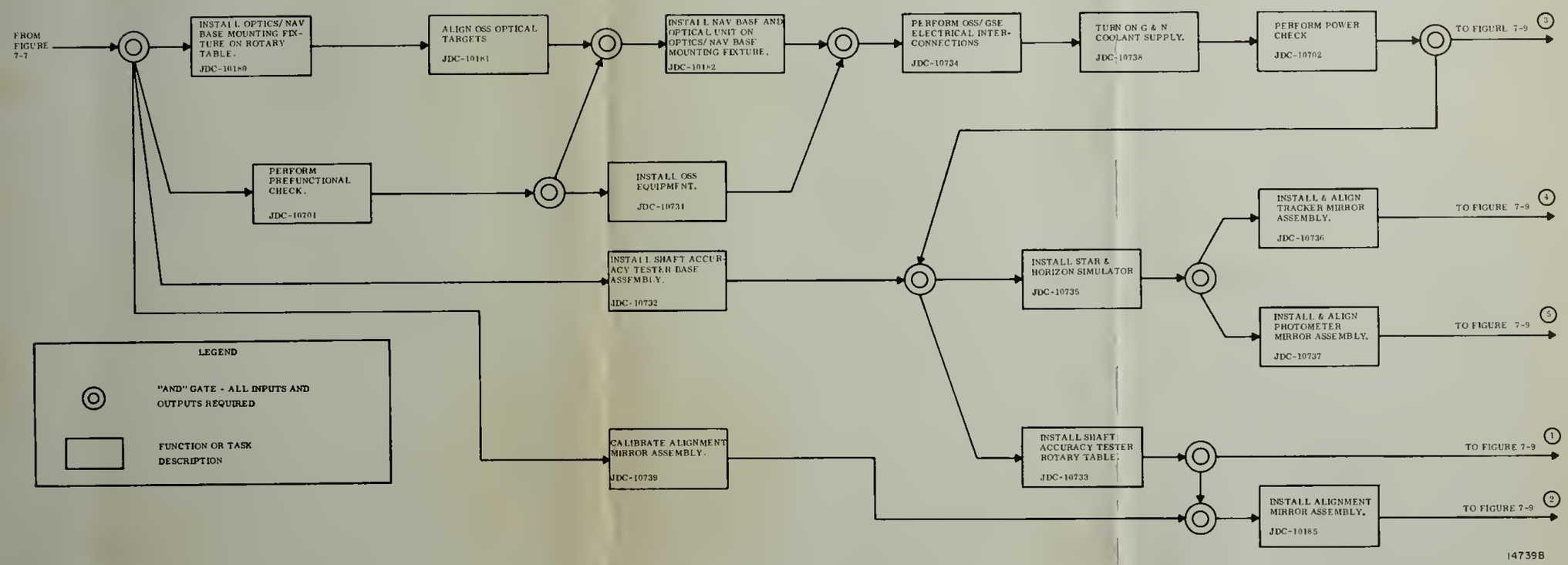


Figure 7-8. OSS Checkout Preparation Flowgram

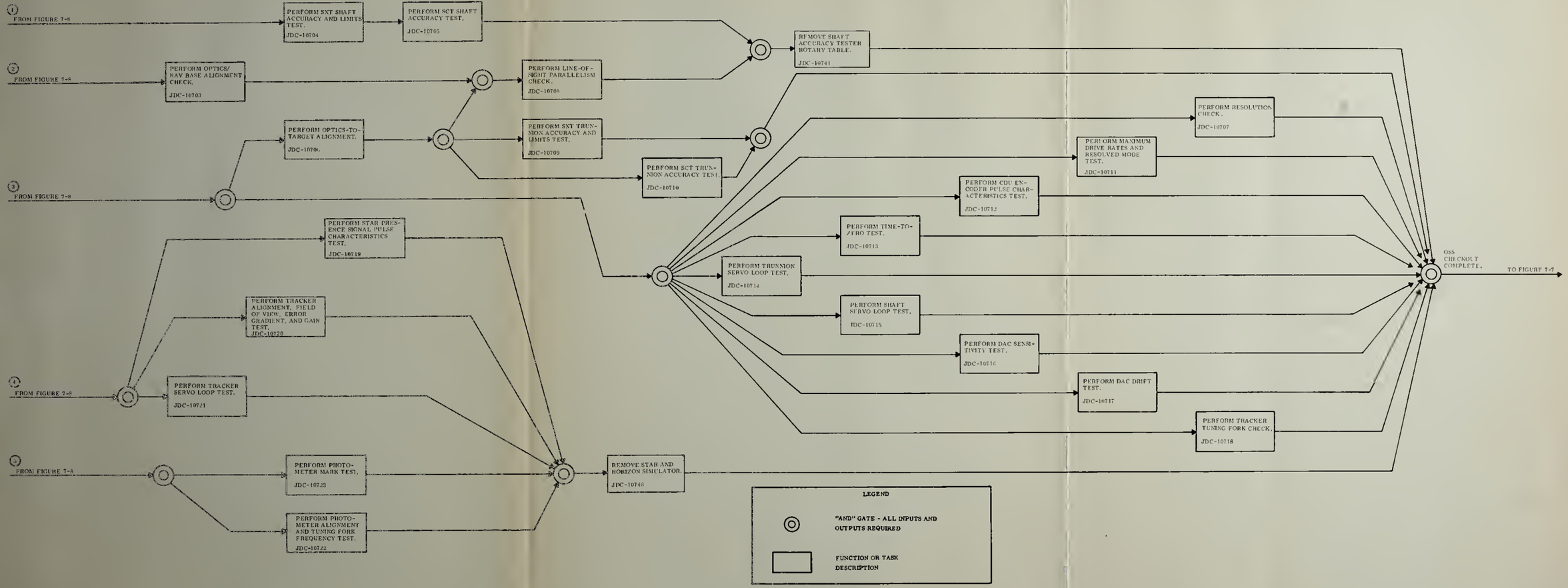


Figure 7-9. OSS Checkout Flowgram

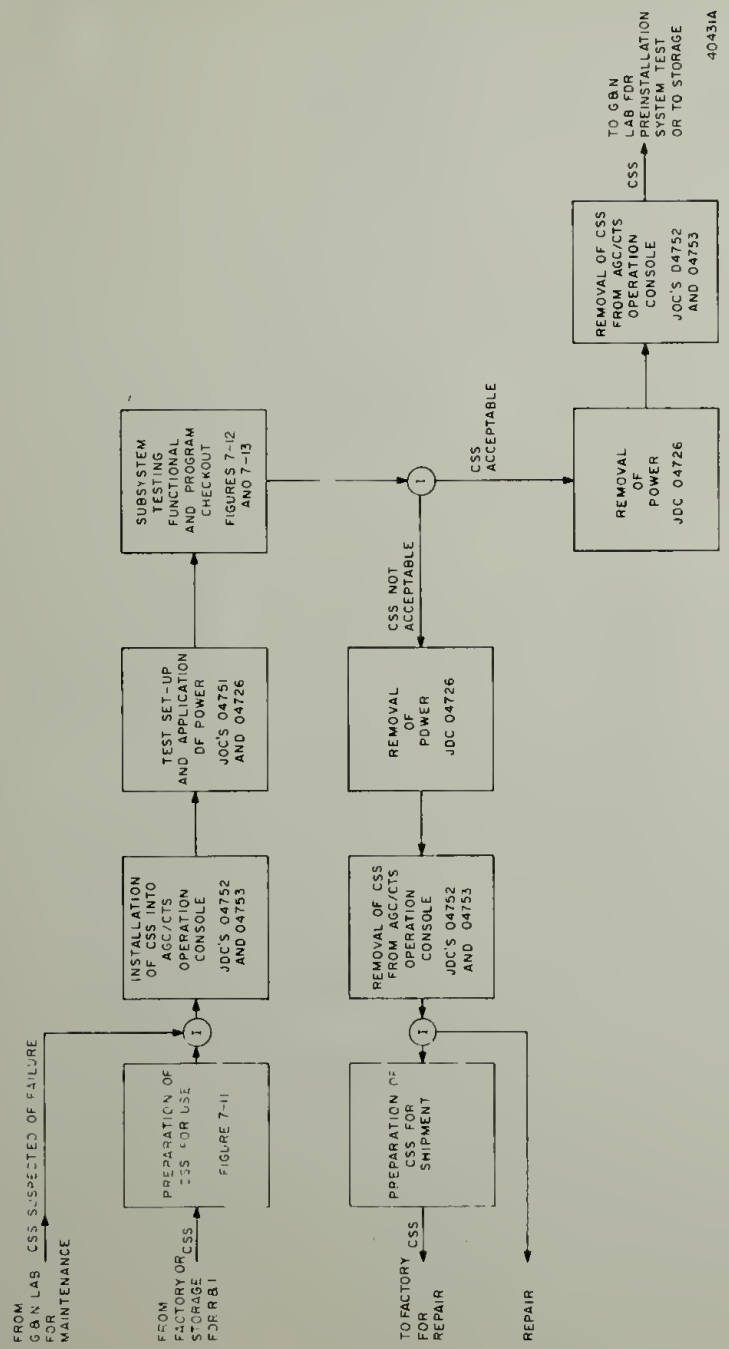


Figure 7-10. CSS Checkout Master Flowgram

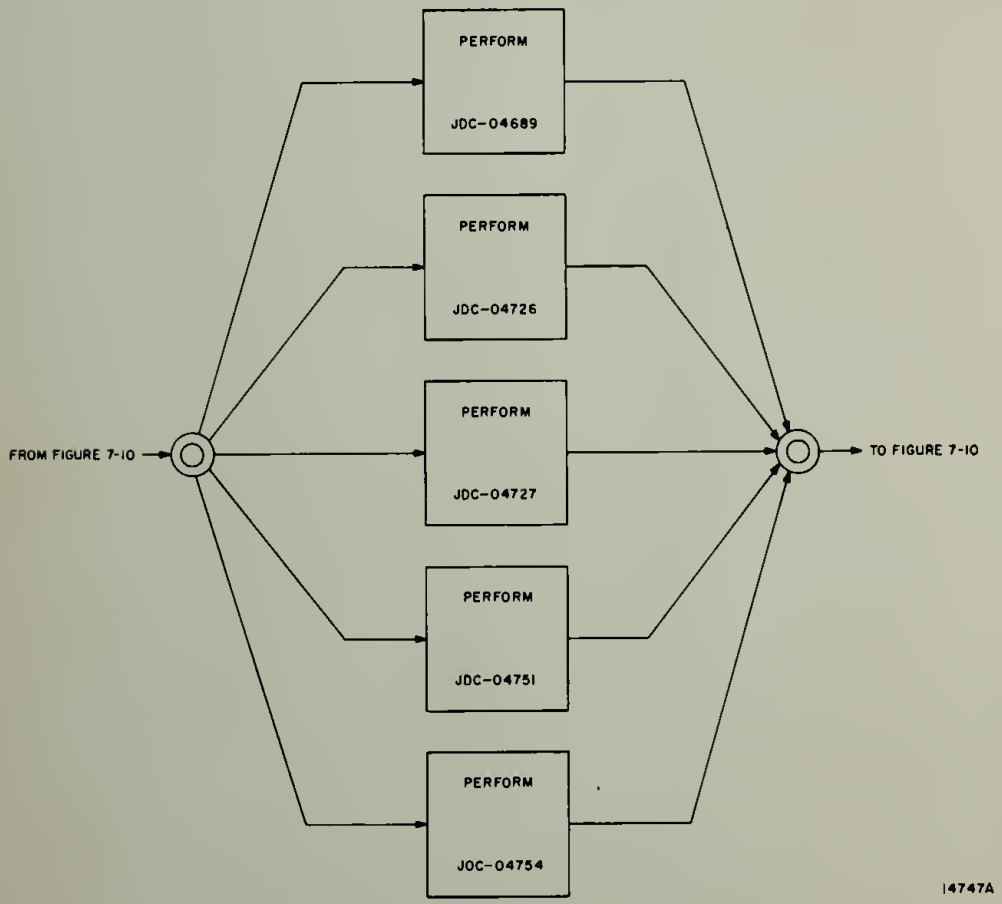


Figure 7-11. CSS Checkout Preparation Flowgram

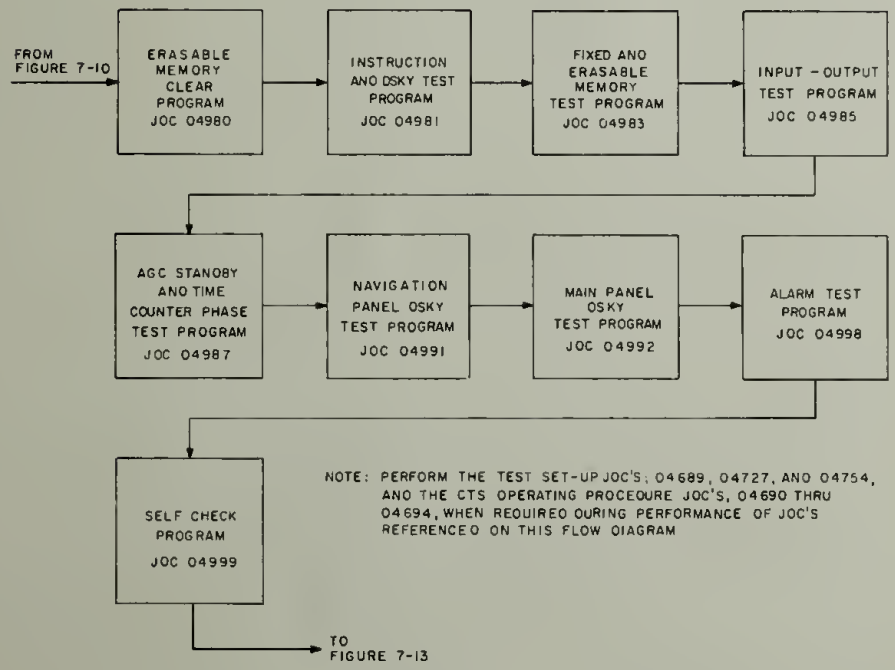


Figure 7-12. CSS Program Checkout Flowgram

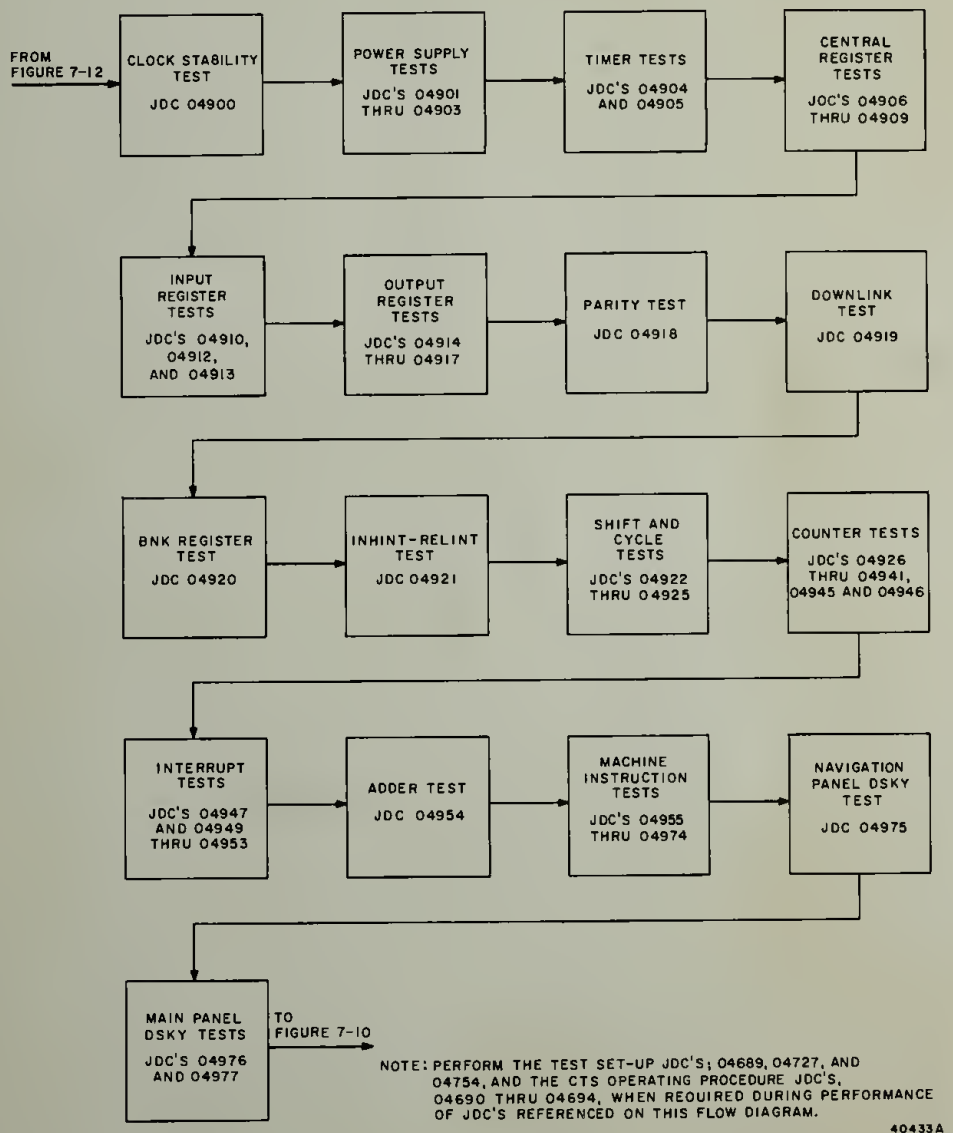


Figure 7-13. CSS Functional Checkout Flowgram

Chapter 8

MAINTENANCE

8-1 SCOPE

This chapter contains maintenance procedures for the guidance and navigation (G and N) system and the three subsystems. Malfunction diagrams contained in this chapter provide procedures to isolate malfunctions, references to job description cards (JDC's) required to repair the malfunction, and provide test requirements after repair. In addition, chapter 8 contains maintenance schedules for the G and N system, inertial subsystem (ISS), optical subsystem (OSS), and computer subsystem (CSS).

8-2 G AND N SYSTEM

8-2.1 MAINTENANCE CONCEPT. When a malfunction occurs in the G and N system at the Merritt Island Launch Area (MILA) or North American Aviation (NAA), the system is repaired by replacement of a black box. The malfunction will be isolated to one of the following black boxes:

Each coupling display unit (CDU).

Inertial measuring unit (IMU) with 7 matched power and servo assembly (PSA) modules: 3 inertial reference integrating gyro (IRIG) calibration modules, 3 pulsed integrating pendulum (PIP) calibration modules, and an IMU/CDU load compensation module.

Navigation (nav) base and optical unit assembly.

G and N indicator control panel.

IMU control panel.

Display and control (D and C) electronics.

Control electronics.

Signal conditioner.

G and N interconnect harness.

Apollo guidance computer (AGC).

Condition annunciator.

Each display and keyboard (DSKY).

AGC flight ropes (MILA only).

AGC test ropes.

Each PSA tray minus the 7 matched IMU modules in trays 2, 3, and 4.

The information in this chapter provides basic maintenance procedures for isolating a G and N system malfunction to one of the black boxes. The operator is assumed to be an engineer who has a thorough knowledge of G and N system operation and has system schematics available. The procedures assume that one malfunction exists in the G and N system and that the ground support equipment (GSE) is trouble free.

A major consideration in presenting G and N system maintenance procedures is that the operator is capable of applying his initiative and experience in malfunction isolation. The procedures provide a general diagnostic approach to the maintenance problem, but allow the operator latitude in carrying out the isolation.

In the event that the malfunction cannot be isolated to a black box in system configuration, it may be necessary to perform malfunction isolation on a subsystem level in accordance with paragraphs 8-3.2, 8-4.2, and 8-5.2.

Figure 8-1 presents, in flow diagram format, the maintenance concept for the G and N system and subsystems. Paragraph references in figure 8-1 show the proper sequence for using chapter 8 paragraphs in performing system or subsystem maintenance.

8-2.2 MALFUNCTION ISOLATION. Malfunction isolation for the G and N system is contained in malfunction diagrams (MD's). A table will contain a cross reference between malfunctions that can occur during system checkout and the MD's which isolate the malfunction.

The MD's are diagnostic flow diagrams for use in malfunction isolation. Each MD is entered through a set of initial conditions that include the malfunction indication and moding, voltage, and switch configurations. The MD proceeds from the initial conditions to the tests required for determining the malfunction.

The following checks shall be made before proceeding to an MD:

(1) Check for open interlock switches and loose connectors.

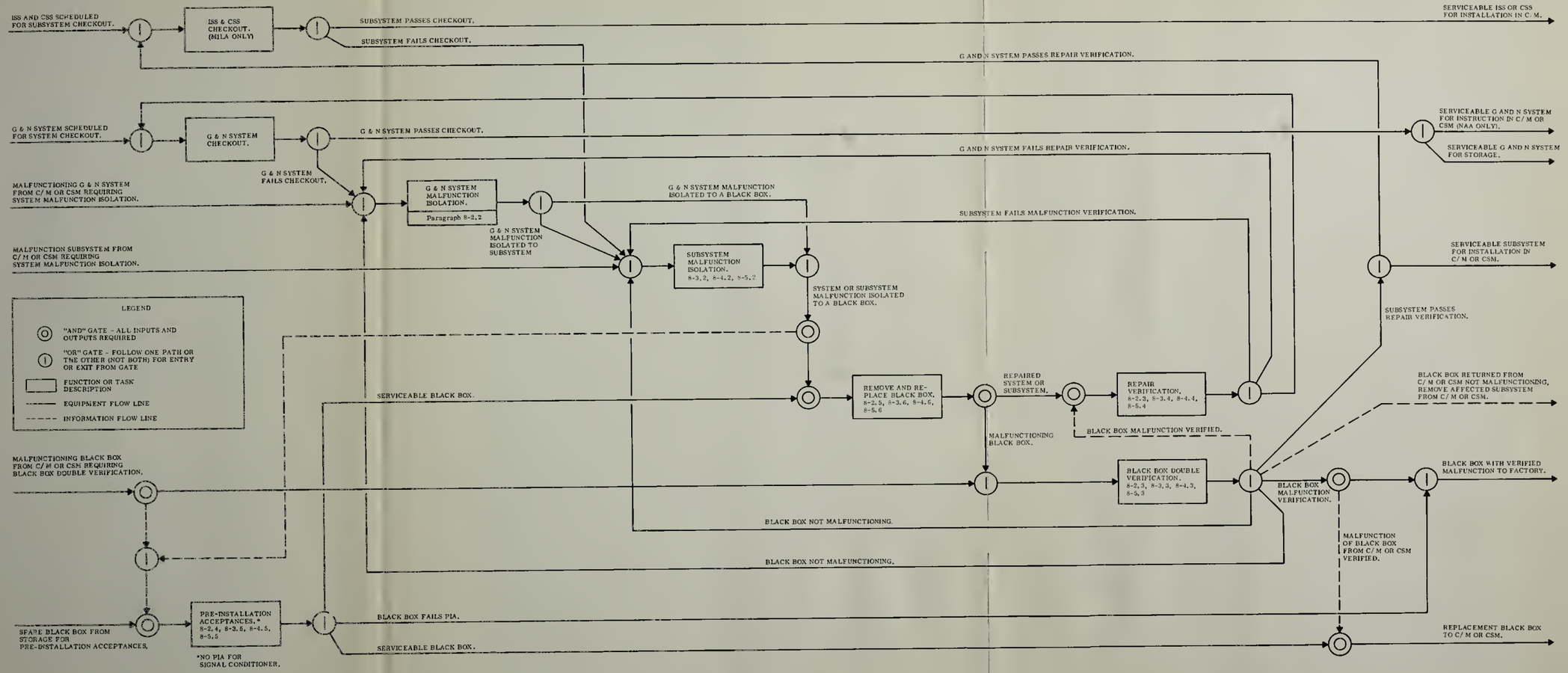


Figure 8-1. G and N System and Subsystem Maintenance Concept Flowgram

(2) Insure that switches are set to positions called out in the procedure.

(3) Check power supplies and insure that they are within tolerances specified in the power supplies check, JDC 10036.

If a G and N system malfunction is isolated to a black box, the suspected black box is removed and double verification is performed. In the event a malfunction cannot be isolated to a black box during system checkout, the suspected subsystem will be removed from the system and transferred to subsystem checkout. The malfunctioning black box is then isolated during subsystem checkout, and black box double verification is performed in accordance with paragraphs 8-3.3, 8-4.3, or 8-5.3 as required. Flowgrams in chapter 7 provide the sequence of functions required for system and subsystem checkout. The MD's for chapter 8 will be completed when information is available.

8-2.3 BLACK BOX DOUBLE VERIFICATION. Double verification of black boxes consists of:

(1) Verification of the malfunction of the black box in a system or subsystem other than that in which the malfunction was originally indicated.

(2) Recertification of the G and N system or subsystem in which the malfunction originally occurred using a replacement black box.

To verify that a malfunction is isolated to the correct black box, the suspected black box is transferred from system checkout to a system or subsystem consisting of the suspected black box along with test article black boxes. The test articles are those qualified black boxes required to complete the verification set-up. Identification of these test articles will be provided in a table. When the malfunction which occurred during system checkout occurs again in the test article configuration, the suspected black box is assumed to be malfunctioned. If no malfunction occurs during the verification, the wrong black box was isolated during malfunction isolation and malfunction isolation must be performed again.

When the malfunction is verified in the test article configuration, the specified repair verification procedures are performed.

After installation of a spare black box, the G and N system is checked out to insure that the malfunction has been corrected. A table will list verification JDC's required to check out each replaced black box. If the repaired G and N system passes repair verification, resume system checkout at the start of the JDC which was being performed when the malfunction occurred, or return the repaired G and N system to the command module (C/M) or command service module (CSM).

8-2.4 PRE-INSTALLATION ACCEPTANCE TEST (PIA). Before a black box is qualified for system operation, it must meet the requirements of certain JDC's as specified in a table which will be supplied when information is defined. In the event such tests have not been performed on the item to be installed, a combined test including all applicable JDC's can be performed to qualify the spare and recheck system operation.

8-2.5 REMOVAL AND REPLACEMENT. JDC 17101 provides instructions for removing and replacing G and N system black boxes. Black box replacement is performed after a satisfactory PIA of the spare black box.

8-3 INERTIAL SUBSYSTEM

8-3.1 MAINTENANCE CONCEPT. When a malfunction occurs in the ISS at MILA or NAA, the subsystem is repaired by replacement of a black box. The malfunction will be isolated to one of the following black boxes:

IMU with 7 matched PSA modules: 3 IRIG calibration modules, 3 PIP calibration modules, and an IMU/CDU load compensation module.

Each ISS CDU.

IMU control panel.

D and C electronics.

Control electronics.

Each ISS PSA tray minus the 7 matched IMU modules in trays 2, 3 and 4.

The operator is assumed to be an engineer who has a thorough knowledge of ISS operation and has ISS schematics available. The procedures assume that one malfunction exists in the ISS and that the GSE is trouble free.

A major consideration in presenting ISS maintenance procedures is that the operator is capable of applying his initiative and experience in malfunction isolation. The procedures provide a general diagnostic approach to the maintenance problem, but allow the operator latitude in carrying out the isolation.

Figure 8-1 presents, in flow diagram format, the maintenance concept for the ISS. Paragraph references in figure 8-1 show the proper sequence for using chapter 8 paragraphs in performing ISS maintenance.

8-3.2 MALFUNCTION ISOLATION. ISS malfunction isolation consists of using ISS indications, GSE indications, and ISS schematics to isolate the malfunction to a black box. Table 8-I contains a list of ISS schematics required to perform malfunction isolation. After the malfunction is isolated to a black box, black box double verification is performed.

Table 8-I. ISS Schematics

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
CDU, part number 1015500-021	1017544 (electrical schematic) 1015550 (mechanical schematic)		
Control Electronics, part number 1015064-021	1021738	Relay and Diode Module, part number 1015097-011	1021739
D and C Electronics, part number 1015065-041	1023024	Attitude Error Demodulator, part number 1014638-011	1014637
		Time Delay, part number 1015038-021	1023022
		Relay and Diode Module, part number 1015036-011	1014623
		Base Assembly, part number 1015076-011	none
IMU, part number 1001500-031, with matched PSA modules	1021414 (IMU wiring diagram)	IMU - CDU Load Compensation (in tray 2), part number 1007550	1010042
		PIPA Calibrate (X and Y in tray 3, Z in tray 4), part number 1007509-021	1009541
		Pulse Torque Gyro Calibration (X in tray 3, Y and Z in tray 4), part number 1007521-021	1009542

(Sheet 1 of 5)

Table 8-I. ISS Schematics (cont)

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
PSA Tray 1, part number 1007571-011	1009561	Gimbal Servo Amplifier, part number 1007540-021	1009534
		Gimbal Coarse Alignment Amplifier, part number 1007541-021	1009524
		-28 VDC Power Supply, part number 1007542-011	1010025
		3200 CPS AAC, Filter and Multivibrator, part number 1007543-011	1010047
		3200 CPS 1% Power Amplifier, part number 1007544-011	1009529
		Temperature Controller Power Supply, part number 1007545-021	1009544
PSA Tray 2, part number 1007572-011	1009562	800 CPS AAC, Filter and Miltivibrator, part number 1007546-011	1010044
		800 CPS 1% Power Amplifier, part number 1007547-011	1009525
		800 CPS 5% Power Amplifier, part number 1007548-011	1009526
		25.6 Encoder Excitation Power Supply, part number 1007549-021	1009527
		Failure Indicator, part number 1007551-011	1009528
		Pulse Torquing Power Supply, part number 1007552-011	1009532

(Sheet 2 of 5)

Table 8-I. ISS Schematics (cont)

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
PSA Tray 3, part number 1007573-011	1009563	DC Differential Amplifier and Precision Voltage Reference, part number 1007507-011	1010008
		AC Differential Amplifier, part number 1007517-011	1010032
		Interrogator, part number 1007519-011	1009522
		Binary Current Switch, part number 1007527-011	1009523
PSA Tray 4, part number 1007574-011	1009564	DC Differential Amplifier and Precision Voltage Reference, part number 1007507-011	1010008
		Ternary Current Switch, part number 1007516-011	1009531
		AC Differential Amplifier, part number 1007517-011	1010032
PSA Tray 5, part number 1007575-011	1009565	Encoder, part number 1007554-011	1010034
		CDU Digital to Analog Converter, part number 1007555-011	1010041
		Forward - Backward Counter and Computer Output, part number 1007558-011	1010050
		CDU Zeroing and Lock Relays, part number 1007561-011	1010056

(Sheet 3 of 5)

Table 8-I. ISS Schematics (cont)

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
PSA Tray 6, part number 1007576-011	1009566	800 CPS AAC, Filter and Multivibrator, part number 1007546-011	1010044
		800 CPS 1% Power Amplifier, part number 1007547-011	1009525
		800 CPS 5% Power Amplifier, part number 1007547-011	1009526
		Motor Drive Amplifier and Selector Circuit, part number 1007557-011	1009543
		CDU Resolver Loads, part number 1007510-011	1009501
		CDU Zeroing Transformer, Relays, and Entry Relays, part number 1007564-011	1010056
PSA Tray 7, part number 1007577-011	1009567	Pulse Torquing Power Supply, part number 1007552-011	1009532
		Encoder, part number 1007554-011	1010034
		IMU Temperature Controller, part number 1007556-011	1009530
		CDU Fixed Resolution Transformation and Entry Mode, part number 1007563-011	1010057

(Sheet 4 of 5)

Table 8-I. ISS Schematics (cont)

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
PSA Tray 7, part number 1007577-011 (cont)	1009567	IMU Temperature Indicating Alarm and Backup Controller, part number 1007518-011	1010140
		PVR Delay Module, part number 1007218-011	1010143
PSA Tray 10, part number 1007580-011	1009570	800 CPS 5% Power Amplifier, part number 1007548-011	1009526
		G and N Subsystem Supply Filter, part number 1007590-011	1010104
		800 CPS Compensation, part number 1007591-011	1010104
		Signal Conditioner Power Supply, part number 1007525-011	1010120
IMU Control Panel, part number 1014628-011	1021737		

(Sheet 5 of 5)

8-3.3 BLACK BOX DOUBLE VERIFICATION. To verify that a malfunction is isolated to the correct black box, the suspected black box is transferred from ISS checkout to a system or subsystem black box double verification configuration. This verification is performed using the suspected black box along with test article black boxes. The test articles are those qualified black boxes required to complete the verification set-up. When the malfunction which occurred during ISS checkout occurs again during black box double verification, the suspected black box is proven to be malfunctioned. If no malfunction occurs during the verification, the wrong black box was isolated during malfunction isolation and malfunction isolation must be performed again.

When the malfunction is verified by black box double verification, the specified repair verification procedures are performed. The test articles which are required for double verification of each black box suspected of failure will be listed in a table.

8-3.4 REPAIR VERIFICATION. After black box double verification is accomplished, the repaired ISS is checked out to insure that the malfunction has been corrected. A table will list verification JDC's required to check out each replaced black box. If the repaired ISS passes repair verification, resume system or ISS checkout at the start of the JDC which was being performed when the malfunction occurred, or return the repaired ISS to the C/M or CSM.

8-3.5 PRE-INSTALLATION ACCEPTANCE TEST. Before a black box is considered to be a qualified replacement item, it must pass the JDC's which will be specified for that black box in a table. These JDC's will be performed using the spare black box to be checked along with test article black boxes which will be listed in a table.

8-3.6 REMOVAL AND REPLACEMENT. JDC 17102 provides instructions for removing and replacing G and N system black boxes. Black box replacement is performed after a satisfactory PIA of the black box.

8-4 OPTICAL SUBSYSTEM

8-4.1 MAINTENANCE CONCEPT. When a malfunction occurs in the OSS at MILA or NAA, the subsystem is repaired by replacement of a black box. The malfunction will be isolated to one of the following black boxes:

Each OSS CDU.

Nav base and optical unit assembly.

G and N indicator control panel.

D and C electronics.

Control electronics.

Each OSS PSA tray.

The operator is assumed to be an engineer who has a thorough knowledge of OSS operation and has OSS schematics available. The procedures assume that one malfunction exists in the OSS and that the GSE is trouble free.

A major consideration in presenting OSS maintenance procedures is that the operator is capable of applying his initiative and experience in malfunction isolation. The procedures provide a general diagnostic approach to the maintenance problem, but allow the operator latitude in carrying out the isolation.

Figure 8-1 presents, in flow diagram format, the maintenance concept for the OSS. Paragraph references in figure 8-1 show the proper sequence for using chapter 8 paragraphs in performing OSS maintenance.

8-4.2 MALFUNCTION ISOLATION. OSS malfunction isolation consists of an experienced operator using OSS indications, GSE indications, and OSS schematics to isolate the malfunction to a black box. Table 8-II contains a list of OSS schematics required to perform malfunction isolation. After the malfunction is isolated to a black box, black box double verification is performed.

8-4.3 BLACK BOX DOUBLE VERIFICATION. To verify that a malfunction is isolated to the correct black box, the suspected black box is transferred from OSS checkout to a system or subsystem black box double verification configuration. This verification is performed using the suspected black box along with test article black boxes. The test articles are those qualified black boxes required to complete the verification set-up. When the malfunction which occurred during OSS checkout occurs again during black box double verification, the suspected black box is proven to be malfunctioned. If no malfunction occurs during the verification, the wrong black box was isolated during malfunction isolation and malfunction isolation must be performed again.

When the malfunction is verified by black box double verification, the specified repair verification procedures are performed. The test articles which are required for double verification of each black box suspected of failure will be listed in a table.

8-4.4 REPAIR VERIFICATION. After black box double verification is accomplished, the repaired OSS is checked out to insure that the malfunction has been corrected. A table will list verification JDC's required to check out each replaced black box. If the repaired OSS passes repair verification, resume system or ISS checkout at the start of the JDC which was being performed when the malfunction occurred, or return the repaired OSS to the C/M or CSM.

8-4.5 PRE-INSTALLATION ACCEPTANCE TEST. Before a black box is considered to be a qualified replacment item, it must pass the JDC's which will be specified for that black box in a table. These JDC's will be performed using the spare black box to be checked along with test article black boxes which will be listed in a table.

8-4.6 REMOVAL AND REPLACEMENT. JDC 17103 provides instructions for removing and replacing OSS black boxes. Black box replacement is performed after a satisfactory PIA of the spare black box.

8-4.7 OPTICAL CLEANING. Cleaning of the optics shall be performed only when necessary, with the approval of the cognizant engineer. Detailed instructions for cleaning are in JDC 03029.

Table 8-II. OSS Loop Diagrams and Schematics

Subsystem		Loop Diagram	
Optical		1009502	
Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
CDU, part number 1015500-031	1017559 (electrical schematic) 1015550 (mechanical schematic)		
Control Electronics, part number 1015064-021	1021738	Relay and Diode Module, part number 1015097-011	1021739
D and C Electronics, part number 1015065-041	1023024	Attitude Error Demodulator, part number 1014638-011	1014637
		Time Delay, part number 1015038-021	1023022
		Relay and Diode Module, part number 1015036-011	1014623
		Base Assembly, part number 1015076-011	none
G and N Indicator Control Panel, part number 1014664-011	1014662		

(Sheet 1 of 3)

Table 8-II. OSS Loop Diagrams and Schematics (cont)

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
PSA Tray 8, part number 1007578-011	1009568	CDU Digital to Analog Converter, part number 1007555-011	1010041
		Two Speed Switch, part number 1007522-011	1009505
		Motor Drive Amplifier, part number 1007581-011	1009503
		Buffer Circuit, part number 1007526-011	1009507
		Relay Module, part number 1007567-011	1009506
		SCT Moding, part number 1007528-011	1009504
PSA Tray 9, part number 1007579-011	1009569	Two Speed Switch, part number 1007522-011	1009505
		Motor Drive Amplifier, part number 1007581-011	1009503
		Buffer Circuit, part number 1007526-011	1009507
		Relay Module, part number 1007567-011	1009506
		Cosecant Generator, part number 1007524-011	1009509
		Resolver Drive Amplifier, part number 1007651-011	1009545

(Sheet 2 of 3)

Table 8-II. OSS Loop Diagrams and Schematics (cont)

Black Box	Black Box Schematic or Wiring Diagram	Module or Subassembly	Module or Subassembly Schematic
PSA Tray 10, part number 1007580-011	1009570	G and N Subsystem Supply Filter, part number 1007590-011	1010104
		Modulator and Loop Compensation, part number 1007511-011	1009521
		Photometer Electronics, part number 1007559-011	1009508
Tracker X and Y Assembly, part number 1007585-011		Tracker X Channel Module Assembly, part number 1007566	1009520
		Tracker Y Channel Module Assembly, part number 1007512	1009511

(Sheet 3 of 3)

8-5 COMPUTER SUBSYSTEM

8-5.1 MAINTENANCE CONCEPT. When a malfunction occurs in the CSS at MILA or NAA, the CSS is repaired by replacement of a black box. The malfunction will be isolated to one of the following replaceable black boxes:

AGC.

Either DSKY.

AGC test ropes.

AGC flight ropes (MILA only).

The operator is assumed to be an engineer who has a thorough knowledge of CSS operation and has CSS schematics available. The procedures assume that one malfunction exists in the CSS and that the GSE is trouble free.

A major consideration in presenting CSS maintenance procedures is that the operator is capable of applying his initiative and experience in malfunction isolation. The procedures provide a general diagnostic approach to the maintenance problem, but allow the operator latitude in carrying out the isolation.

Figure 8-1 presents, in flow diagram format, the maintenance concept for the CSS. Paragraph references in figure 8-1 show the proper sequence for using chapter 8 paragraphs in performing CSS maintenance.

8-5.2 MALFUNCTION ISOLATION. A CSS malfunction isolation consists of an experienced operator using CSS indications, GSE indication, and CSS schematics to isolate the malfunction to a black box. Table 8-III contains a list of CSS schematics required to perform malfunction isolation. After the malfunction is isolated to a black box, black box double verification is performed.

8-5.3 BLACK BOX DOUBLE VERIFICATION. To verify that a malfunction is isolated to the correct black box, the suspected black box is transferred from CSS checkout to a system or subsystem black box double verification configuration. This verification is performed using the suspected black box along with test article black boxes. The test articles are those qualified black boxes required to complete the verification set-up. When the malfunction which occurred during CSS checkout occurs again during black box double verification, the suspected black box is proven to be malfunctioned. If no malfunction occurs during the verification, the wrong black box was isolated during malfunction isolation and malfunction isolation must be performed again.

When the malfunction is verified by black box double verification, the specified repair verification procedures are performed. The test articles which are required for double verification of each black box suspected of failure will be listed in a table.

8-5.4 REPAIR VERIFICATION. After black box double verification is accomplished, the repaired CSS is checked out to insure that the malfunction has been corrected. A table will list verification JDC's required to check out each replaced black box. If the repaired CSS passes repair verification, resume system or CSS checkout at the start of the JDC which was being performed when the malfunction occurred, or return the repaired CSS to the C/M or CSM.

8-5.5 PRE-INSTALLATION ACCEPTANCE TEST. Before a black box is considered to be a qualified replacement item it must pass the JDC's which will be listed in a table.

8-5.6 REMOVAL AND REPLACEMENT. Procedures for removing and replacing OSS components are in the following JDC's: AGC, JDC 04752; either DSKY, JDC 04753; Tray A modules, JDC 04682; Tray B modules, JDC 04683. Black box replacement is performed after a satisfactory PIA of the spare black box.

8-5.7 MAINTENANCE SCHEDULE. The only scheduled maintenance for the CSS is the clock stability test that must be performed every three hours of G and N system laboratory operating time. This test is specified in JDC 04900, Clock Stability Test - Block I (100 Series), and must be performed during CSS tests and PIA. Connection to the AGC calibration system is required.

Table 8-III. CSS Logic Diagrams and Schematics

Title	NASA Drawing
TRAY A SUBASSEMBLY	
Modules A1-A16	1006540
Interface A19, A39	1005701
Interface A20, A40	1005702
Module A17	1006543
Module A18	1006542
Module A21	1006556
Module A22	1006553
Module A23	1006545
Module A24	1006555
Module A25	1006554
Module A26	1006549
Module A27	1006544
Module A28	1006552
Module A29	1006559
Module A30, A31	1006548
Module A32	1006546
Module A33, A34	1006547
Module A35	1006541
Module A36	1006557
Module A37	1006550
Module A38	1006551
TRAY B SUBASSEMBLY	
Power Switch B2, B3, B4	1006097
Filter Module B5	1005700
Oscillator B6	1006140
Driver Service B7	1006082

(Sheet 1 of 2)

Table 8-III. CSS Logic Diagrams and Schematics (cont)

Title	NASA Drawing
TRAY B SUBASSEMBLY (cont)	
Current Switch B8	1006074
Erasable Memory B9	1006061
Erasable Driver B10, B11	1006086
Power Supply Cont. B12	1006098
Erasable Sense Ampl. B13, B14	1006118
Rope Memory B21, B22, B23, B24, B28, B29	1006144
Rope Sense Ampl B26, B27	1006119
Rope Strand Select B30	1006099
Strand Gate B31	1006199
Rope Driver B32, B33	1006147
MAIN PANEL DSKY	
Keyboard Module	1006150
Decoding Module	1006162
Relay Module	1006161
Power Supply	1006163
NAVIGATION PANEL DSKY	
Keyboard Module	1006160
Decoding Module	1006162
Relay Module	1006161
Power Supply	1006163

(Sheet 2 of 2)

Appendix A

List of Technical Terms and Abbreviations

Term	Definition
A_{IG}	Inner gimbal angle
A_{MG}	Middle gimbal angle
A_{OG}	Outer gimbal angle
A_S	Shaft angle
A_t	Trunnion angle
ABP	Auxiliary battery pack
ACC	Accepted
ACCL or ACCEL	Accelerometer
ACSP	AC Electronics, Division of General Motors
ACTREQ	Action request
AD	Add
ADA	Angular differentiating accelerometer
ADC	Analog to digital converter
ADIA	Gyro drift due to acceleration along the input axis caused by an unbalance on the spin reference axis
ADSRA	Gyro drift due to acceleration along the spin reference axis caused by an unbalance on the input axis
AGC	Apollo guidance computer
AGC/CS	AGC calibration system
AGC-OC	Apollo guidance computer test set operation console
AGCU	Attitude Gyro Coupling Unit

Appendix A (cont)

Term	Definition
A-GSE	Auxiliary ground support equipment
AIICR	Apollo Integrated Inventory and Consumption Report
αB	Hypothetical rotation of the PIP case about its output axis equivalent to bias. Subscripts (X, Y, or Z) may be added to denote a specific PIP case rotation.
αX, αY. or αZ	Misalignment of PIP case about stable member axis. Subscripts (X, Y, or Z) may be added to denote a specific PIP case alignment.
ATP	Assembly test procedure
ATT	Attitude
BAL	Bank alarm
BD	Bias drift of IRIG. Subscripts (X. Y, or Z) may be added to denote a specific IRIG bias drift.
BKTF	Block transfer
BLKUPL	Block uplink
BM-GSE	Bench Maintenance ground support equipment
BNK	Bank
BPP	Battery power pack
CAGEN	Counter address generate
CCB	Change control board
CCS	Count, compare and skip
CDU	Coupling display unit
COMP	Computer
COMP FAIL	Computer fail
CM or C/M	Command module

Appendix A (cont)

Term	Definition
CS	Clear and subtract
C/S	Computer simulator
CSM	Command and Service Module
CSS	Computer subsystem
CTRAL	Counter fail alarm
CTROR	Request to increment counter
CTS	Computer test set
CYL	Cycle left
CYR	Cycle right
D and C	Display and control
DAC	Digital to analog converter
DEC	Decrease
DEMOD	Demodulator
DKEND	Downlink end
DLKHN	Downlink inhibit
DLNK	Downlink
DRB	Design review board
DSKY	Display and keyboard
DV	Divide
DVM	Digital voltmeter
ECS	Environmental control system
E_{ig}	Inner gimbal error signal

Appendix A (cont)

Term	Definition
E memory	Erasable memory
ENC	Encoder
$E\phi_{NB}$	Roll body offset error
$E\phi_{SC}$	Roll body error signal
EPS	Electrical power system
$E\Psi_{NB}$	Yaw body offset error signal
$E\Psi_{SC}$	Yaw body error signal
$E\theta$	Pitch body offset error signal
ϵ_{in}	In-phase component of voltage
ϵ_{q}	Quadrature component voltage
ϵ_{t}	Total voltage
ϵF_{Y}	Misalignment between rotary table fixed axes and gimbal case fixed axes
ϵIGA	Inner gimbal axis error
ϵIGR	Inner gimbal resolver error
ϵMGA	Middle gimbal axis error
ϵMGR	Middle gimbal resolver error
ENOFF	Engine off
ENON	Engine on
ENRST	Engine reset
ϵOGR	Outer gimbal resolver error
EPS	Electrical power system
EXC or EXCIT	Excitation

Appendix A (cont)

Term	Definition
$E(X_g)$	X gyro error signal
$E(Y_g)$	Y gyro error signal
$E(Z_g)$	Z gyro error signal
FDAI	Flight director attitude indicator
FINDVAC	Find vector accumulated data
F memory	Fixed memory
FF	Flip-flop or fixed-fixed
FS	Fixed-switchable
GAEC	Grumman Aircraft Engineering Corporation
γX, γY, or γZ	Misalignment of IRIG case about stable member corresponding axis. (First subscript denotes a specific gyro, second subscript is added to denote a specific stable member axis about which the gyro input axis is misaligned.)
G and N	Guidance and navigation
GSE	Ground support equipment
GYRST	Gyro reset
HICOSLAM	High cosine of lambda
HISINLAM	High sine of lambda
HND PPS	Hundred pulses per second
HLOS	Horizon line of sight
IAW	In accordance with
ICTC	Inertial components temperature controller
IG	Inner gimbal

Appendix A (cont)

Term	Definition
IIP	Interrupt in progress
ILP	Parity inhibit
IMU	Inertial measuring unit
INC	Increase
INHINT	Inhibit interrupt
INKL	Counter increment request
IP	Interrogate pulse
IRIG	Intertial reference integrating gyro
ISS	Inertial subsystem
JDC	Job description card
JDC-DS	Job description card data sheet
K	Address or location
KEY RLSE	Key release
KRST	Key reset
LEM	Lunar excursion module
LINC	Load location
LLOS	Landmark line of sight
LOCOSLAM	Low consine of lambda
LOS	Line of sight
LOSINLAM	Low sine of lambda
LSD	Least significant digit
LTRST	Light reset

Appendix A (cont)

Term	Definition
MC	Memory cycle or memory control
MCT	Memory cycle time
MD	Malfunction diagram
MDA	Motor drive amplifier
Meru	Milliearth rate unit(s)
MG	Middle gimbal
MG	Tachometer-generator
MILA	Merritt Island Launch Area
MINC	Minus increment
MIT/IL	Massachusetts Institute of Technology Instrumentation Laboratory
MKTRP	Mark trap
MNHRPT	Monitor inhibit interrupt
MP	Multiply
MSC	Manned Spacecraft Center
MSD	Most significant digit
MSFC	Manned Spacecraft Flight Center
MSFN	Manned Space Flight Network
MSK	Mask
MSK K	Mask with data from K
MSTRT	Monitor start
N	Negative
N	Noun

Appendix A (cont)

Term	Definition
N_1	Sample time
N_2	Display time
NAA	North American Aviation
Nav	Navigation
NBO	Navigation base and optics
NBD	Normal bias drift
ND	NASA document
NDX	Index
NHSYNC	Inhibit upsync
NISQ	Next instruction sequence
NLT	Not less than
NMT	Not more than
NOOP	No operation
NOVAC	No vector accumulated data
NRPTAL	Interrupt has not occurred during an 80 millisecond period
OA	Output axis
OG	Outer gimbal
OIA	Optics-inertial analyzer
OINC	Display location
OITS	Optics-inertial test set
OJB	GSE junction box
OSS	Optical subsystem

Appendix A (cont)

Term	Definition
OUA	Optical unit assembly
OUTCR	Out counter
OVCTR	Overflow counter
OVF	Overflow
P	Positive
PA	Pendulum axis
PAL	Parity fail alarm
PAVM	Phase angle voltmeter
ΦH_{MGA}	Corrected reading taken from the tilt axis optigon screen with rotary axis at θH_{OGA}, outer gimbal at precision zero, and middle gimbal axis in horizontal plane
ΦH_{RA}	Corrected reading taken from the tilt axis optigon screen with rotary axis in horizontal plane
PIA	Pre-installation acceptance
PINC	Plus increment
PIP	Pulsed integrating pendulum
PROG ALM	Program alarm
PSA	Power and servo assembly
PSA-EC	Power and servo assembly end connector
PTC	Portable temperature controller
PTE	Pulse torque electronics
PVR	Precision voltage reference

Appendix A (cont)

Term	Definition
RCS	Reaction control system
RDA	Resolver drive amplifier
RDRST	Radar reset
REJ	Rejected
RELINT	Release inhibit interrupt
RL	Read line
RLSE	Release
RLYBIT	Relay bit
RLYWD	Relay word
RPTAL	Interrupt lock alarm
RPTLDS	Interrupt in progress longer than 10 milliseconds
RSM	Resume
RSTRT	Read start
RUPT	Interrupt
S	Total gain from rotation about an IRIG input axis to voltage output of the preamplifier, (millivolts per milliradians). Subscripts (X, Y, or Z) may be added to denote a specific IRIG total gain voltage.
SAT	System assembly and test
S/C or SC	Spacecraft
SCAFAL	Scaler fail alarm
SCS	Stabilization and control system
SCT	Scanning telescope
SC_x	Spacecraft roll axis

Appendix A (cont)

Term	Definition
SETEK	Set strobe
SF(A)	Scale factor of PIP. Subscripts (X, Y, or Z) may be added to denote a specific PIP scale factor.
SFTG	Scale factor of torque generator, (milliradians per pulse). Subscripts (X, Y, or Z) may be added to denote a specific IRIG torque generator scale factor.
SHANC	Shift and add increment
SHINC	Shift increment
SIDL	System Identification Data List
SJB	GSE-PSA junction box assembly
SL	Shift left
SM	Stable member or service module
SP	Switch pulse
SPS	Service propulsion system
SQG	Sequence generator
SR	Shift right
SRA	Spin reference axis
ST	State
STD2	Standard subinstruction two
S, LOS	Star line of sight
STMIC	Standard memory inquiry cycle
SU	Subtract
SXT	Sextant

Appendix A (cont)

Term	Definition
TC	Transfer control
TCAL	Transfer control trap alarm
TCSA	Start at specified address
TDA	Torque drive amplifier
TDCR	Technical data change request
TDCR-RB	Technical data change review board
TDRR	Technical data release or revision
TG	Tachometer-generator
THRCOM	Thrust command
θH_{IGA}	Rotary axis optigon screen with outer and middle gimbals at precision zero, and inner gimbal axis at local vertical
θH_{OGA}	Rotary axis optigon screen with rotary axis horizontal and outer gimbal axis horizontal and east
$\theta + lg$	True table rotary axis angle which places PIP input axis opposite local vertical vector. Subscripts (X, Y, or Z) may be added to denote a specific PIP input axis.
$\theta - lg$	True table rotary axis angle which places PIP input axis along local vertical vector. Subscripts (X, Y, or Z) may be added to denote a specific PIP input axis.
TLEND	Telemetry end
TLOS	Tracker line of sight
TLSTRT	Telemetry start
TM	Torque command pulse
TP	Test point or test parity
TS	Transfer to storage

Appendix A (cont)

Term	Definition
ULNK	Uplink
UNF	Underflow
UPTEL	Up telemetry
V	Verb
VDW	Variable deviation wedge
VTVOM	Vacuum tube voltohmmeter
WA	Write amplifier
WL	Write line
wrt	With respect to
XCH	Exchange
XFMR	Transformer
ZID	Inhibit strobe

Appendix B

RELATED DOCUMENTATION

This appendix explains the function and relationship of the System Identification Data List (SIDL), the Apollo Integrated Inventory and Consumption Report (AIICR), and the Aperture Card System to Apollo guidance and navigation (G and N) system publications.

SIDL is an official release record for documents issued to implement NASA contracts. SIDL identifies drawings, specifications, manuals and job description cards (JDC's), and other documents released to support the G and N system.

Manuals and JDC's are based upon the latest information available as of the publication freeze date. Manuals and JDC's are distributed after formal CCB approval. SIDL shall be consulted to determine which is the currently effective information. AC Electronics, Field Service Publications Department, will periodically revise the manuals and JDC's to the latest technical information releases.

The AIICR is a listing of all approved spare parts for the G and N system equipment and its associated ground support equipment (GSE).

The aperture card system is a compilation of documents in the Apollo program. Each aperture card consists of a mounted 35 MM microfilm copy of a complete document, with the exception that for manuals, only the title page, signature page, record of revisions page and list of effective pages are included to identify the revision letter, change pages, and TDRR number.

Aperture card sets are maintained at all field sites and are used with the G and N system manuals to refer to schematics, wiring diagrams, and other drawings which are not included in the manuals.

Appendix C

LOGIC SYMBOLS

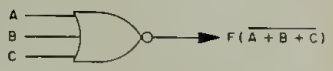
The Apollo Guidance Computer contains NOR gates, extended NOR gates, and NOR gate flip-flops. For a better understanding of the logic used in the AGC, the logic symbols, terminology, and conventions used in logic descriptions in this chapter are discussed in detail in the following paragraphs.

The NOR gate (figure C-1) is a 3-input OR element with internal negation or inversion. This gate performs the logic function of $F = \overline{A + B + C}$, which is expressed as "neither A nor B nor C". From this the term NOR gate is derived.

The two more commonly used configurations of the NOR gate in the AGC are the AND and OR functions, also illustrated on figure C-1. The AND function ($\overline{A} \cdot \overline{B} \cdot \overline{C}$) is expressed as "not A and not B and not C". Another way of expressing this function is to state that an output is present when not A and B and C are coincident. An actual application of the AND function will demonstrate still another way of describing this configuration. The gate shown has as inputs the negations $\overline{T09}$ and $\overline{XCH0}$. The output function is described as: signal RP2 is generated at time 9 during an Exchange instruction. This means of describing the AND function will appear more frequently in text than the others. An OR function is simply the inverted result of a NOR function. The output function F is present if either A or B is present. If neither A nor B is present, the function F is not present.

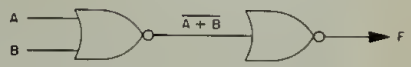
The extended NOR gate assumes the configuration shown on figure C-1. This is simply a method of increasing the number of inputs (fan-in) to produce a given function. On figure C-1 both gates are shown tangent to one another. They are drawn in this manner on many of the detailed logic drawings of this section since both gates follow in numerical sequence. However, both gates need not be, and on many drawings are not shown tangent to each other to produce the given function. The shaded portion of the lower gate indicates that it is an extension of the NOR gates shown above it through a common connection, which will be described in detail.

The NOR gate consists of three NPN transistors with resistive inputs, as shown in figure C-2. The collector of each transistor is connected to a common load resistor, the other end of which is connected to the +3 vdc supply. All three emitters are common

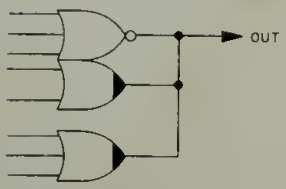


NOR GATE

AND FUNCTION



OR FUNCTION



EXTENDED NOR GATE

40622

Figure C-1. NOR Gate Symbols

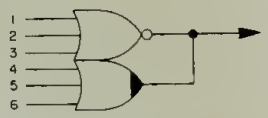
and are connected to ground. As a result of these connections, the logic levels for the AGC can be defined (+3 vdc represents a logic ONE; approximately ground level represents a logic ZERO). Since an NPN transistor requires a positive transition for turn-on, a logic ONE at any one input or at all three inputs results in a logic ZERO at the output. To correlate this to the NOR gate symbol of figure C-1, consider that inputs A, B, and C are each a logic ONE. The output is logic ZERO or the inverted form of the input.

When all three inputs to the NOR gate are each logic ZERO, the transistors are cutoff. The output assumes the collector supply voltage (+3 vdc) or logic ONE. This latter condition can be correlated to the AND function of the NOR gate in figure C-1. When the two inputs ($\overline{T09} \cdot \overline{XCH0}$) are each logic ZERO, the output (RP2) is a logic ONE. In the detailed discussions which follow, a logic ZERO level is often referred to as enabling an associated input gate leg. For example, the negation input $\overline{T09}$ enables the gate coincident with $\overline{XCH0}$ (both inputs logic ZERO). An input gate leg is considered to be a logic ZERO if there is no connection to that particular leg. Each NOR gate has a capacity of three inputs. If connections are made to only two inputs, the third is considered to be logic ZERO, or the leg is enabled.

The fan-in capacity is increased to produce a given function, as shown by the dotted connection on figure C-2. The extended gate has no connection through the common collector resistor to +3 vdc. Instead, the output from the extended gate is connected to the output line from the other gate. The collector resistor of this gate is now common to the transistors in both gates. This configuration does not change the logic ability of the gates. A logic ONE at any one or all of the six inputs results in a logic ZERO out. A logic ZERO at all six inputs results in a logic ONE out.

A NOR gate flip-flop consists of two NOR gates interconnected, as shown on figure C-3. The flip-flop is set by a logic ONE applied to the set input and is reset by a logic ONE applied to the reset input. The set pulse actually is applied to the reset side of the flip-flop; likewise the reset pulse is applied to the set side. This condition exists because of the characteristics of the NOR gate (a logic ONE at any input results in a logic ZERO out). The logic ZERO is applied to the input of the opposite side and holds that side off, which results in a logic ONE out. Thus, a set pulse applied to gate A of figure C-3 turns the gate on. The output of gate A (or the reset side) is a logic ZERO, which is applied to gate B and holds this gate off. The output of gate B (the set side) is a logic ONE.

The format used for each of the logic diagrams contained in the discussions in this manual is illustrated and explained on figure C-4.



EXTENDED NOR GATE SYMBOL

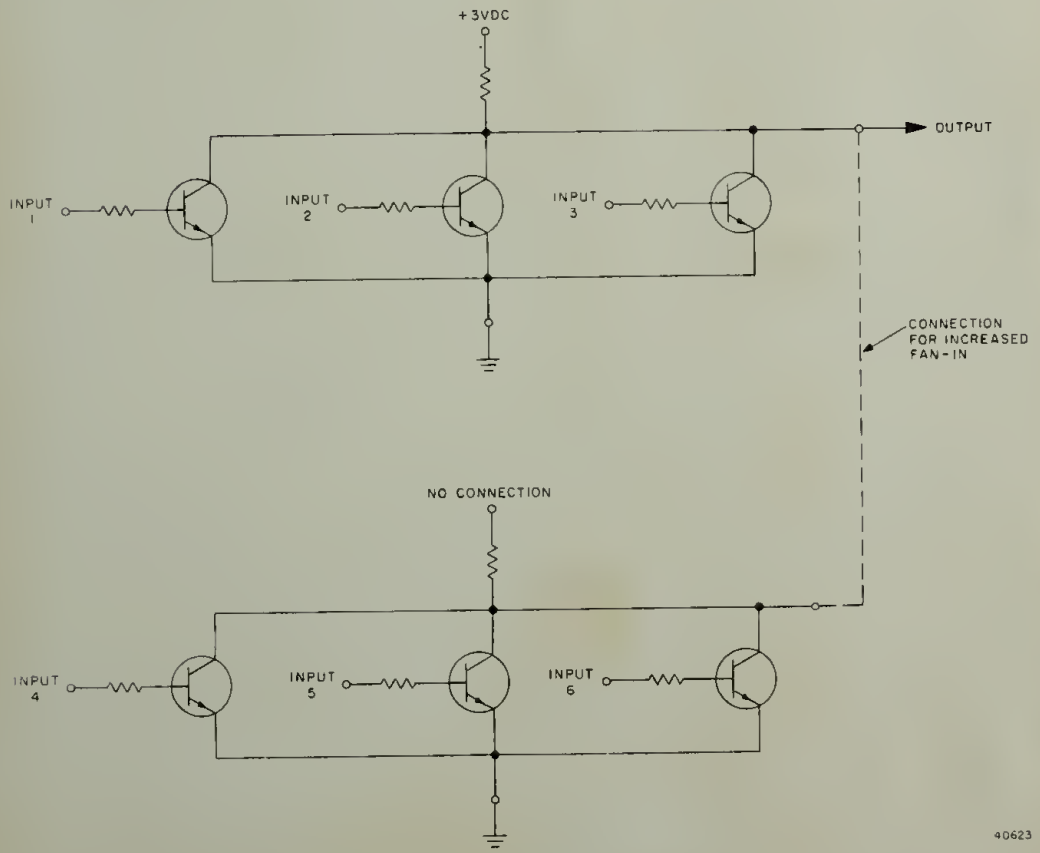


Figure C-2. NOR Gate Schematic

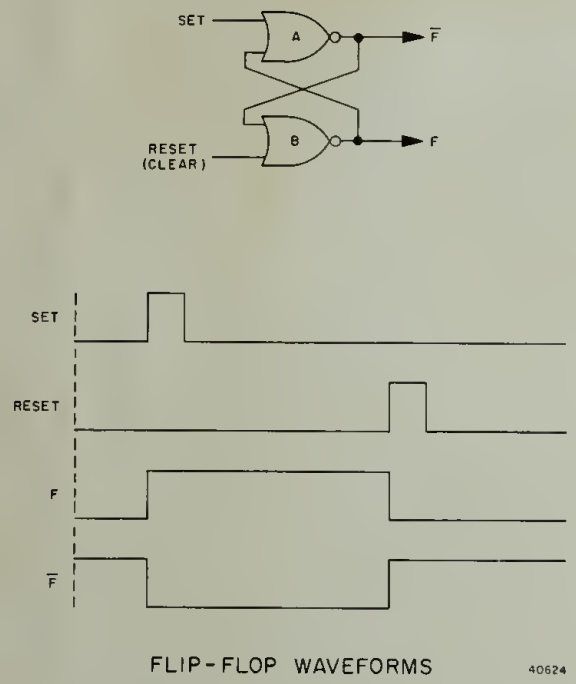
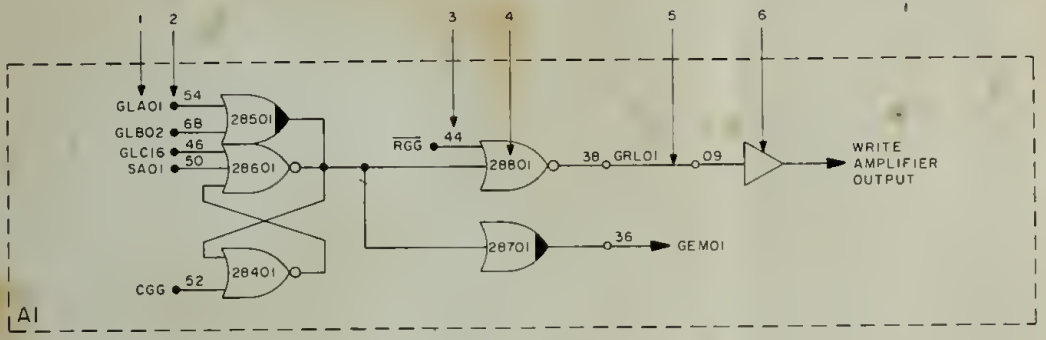
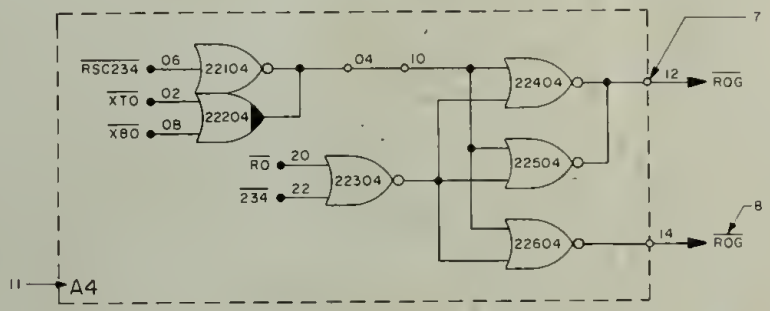


Figure C-3. NOR Gate Flip-Flop





KEY	
INDEX NUMBER	FUNCTION
1	INPUT SIGNAL
2	MODULE INPUT TERMINAL
3	MODULE INPUT TERMINAL NUMBER
4	CIRCUIT NUMBER
5	CONNECTION BETWEEN TERMINALS
6	WRITE AMPLIFIER
7	MODULE OUTPUT TERMINAL
8	OUTPUT SIGNAL
9	OUTPUT INTERFACE CIRCUIT
10	INPUT INTERFACE CIRCUIT
11	TRAY-MODULE DESIGNATION (LETTER DESIGNATES TRAY, NUMERAL DESIGNATES MODULE LOCATION)

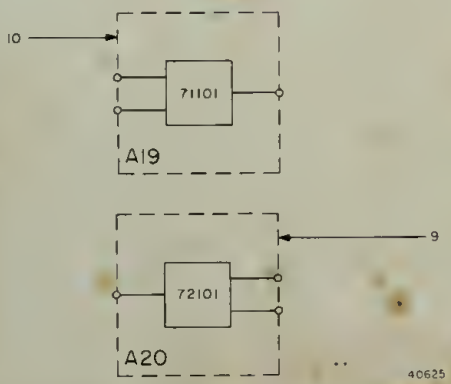


Figure C-4. Logic Diagram Symbols