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Digital Development Memo #193

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Subj: AGC Block II Instructions
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An expanded instruction set for adoption into the Block II computer is proposed. All of the Block I instructions are retained with a few minor changes.

Both computers have eight basic operation codes. The Block I AGC uses the uncorrected sign bit as an extension mechanism, control of this bit being exercised by the index instruction. In addition to such "extracodes," the Block II AGC will extend its operation code set by using address bits 11 and 12 in operations whose address field is limited to 1024 words. For example, the use of the CCS instruction with operands in fixed memory is prohibited in Block I; therefore address bits 11 and 12 must be zero. In Block II, these two bits will be examined by the sequence generator, and if they are in a configuration other than 00, a different instruction sequence will be invoked. This other instruction is, of course, restricted to a small memory field just as CCS is. The other instruction which basically pertains only to erasable memory is TS. Because of this, six so-called quarter codes can be provided in the basic operation field over and above the old set.

A number of useful quarter code instructions have been devised. They are: Clear and add Erasable, Double add to storage, Modular subtract, Double transfer to storage, Double exchange, and Transfer control within bank. All but the last reference erasable memory only. The last references octal addresses 6000-7777.

The double precision instructions treat the A and LP registers as a double length accumulator. Double add to storage forms the double precision sum of two consecutive erasable registers and the double accumulator and stores the result in the same two erasable registers. Modular subtract forms the difference between two angles. The result is expressed as that one of the two possible answers which has the lowest magnitude. Transfer control within bank is like TC except that Q is not altered.

Three new extracode instructions are being added. They are Double clear and add, Double clear and subtract, and Edit. The first two are made extracode rather than quarter code in order to be able to reach all of memory. The Edit instruction uses bits 10 through 7 to specify the number of shifts or cycles desired, and the remainder of the address word to select an editing register (SR, SL, CYR, or CYL).

The TC instruction will be modified such that TCA and TCQ receive special treatment. The former will operate without altering Q or Z; the latter will be reduced to a single memory cycle which effects a TC to the contents of Q.

The design of the new instruction is nearly complete. The new sequence generator will use an estimated 520 nor-gates where the Block I sequence generator now uses about 450. More nor-gates will be needed to implement the new control pulses necessary for these instructions. This number is estimated to be about 50, making an estimated excess over Block I of 120 gates. This would seem to be a low estimate; however, it should be pointed out that many economies are realized in the new set from the similarities between many of the instructions and the faster than expected add time which has been realized in the AGC.

Instruction Sets

Block I	Block II
TC	TC
CCS*	CCS*
INDEX	XCH*
XCH	DAS* (double add to storage)
CS	MSU* (modular subtract)
TS	INDEX
AD	CA (clear and add)
MSK	CS
------	TS*
MP	DTS* (double TS)
DV	DXCH* (double XCH)
SU	TCB** (TC within bank)
	AD
	MSK

	MP
	DV
	SU
	DCA (double CA)
	DCS (double CS)
	ED X (edit x times)

* Erasable only

** 6000-7777 only