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Digital Development Memo #194

To: Eldon Hall
From: Albert Hopkins
Subj: Erasable Memory for Block II Computer
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It has been concluded that the erasable memory for AGC Block II can be augmented to double its Block I capacity, without any increase in volume. This is made possible by repackaging the stack and drivers. Such an increase in capacity would be desirable from the point of view of mission capability and flexibility. Block II design therefore incorporates the necessary logic and driving circuitry for a 2048 word erasable memory.

The field of addresses assigned to erasable memory will remain the same i.e., up through octal 1777. The extra memory cells will be accessible through a bank substitution arrangement like that of fixed memory. The first half of the erasable address field, through octal 777, will always refer to the same memory cells. The second half will be ambiguous, and refer to one of three groups of cells. A separate erasable memory bank register will govern which of the three groups is accessible.

The new erasable bank register may be loaded and read via octal addresses 16 and 17 in bit positions one and two. Address 17 will simultaneously access the fixed memory bank register, normally accessed via address 15. The two new addresses 16 and 17 are borrowed from the relint and inhint operations: The instruction words TC 16 and TC 17 will operate as INDEX 16 and 17 did in Block I to control

interrupt inhibits. Any other instruction referencing 16 and 17 will operate on the bank registers as described.

Double sized memory stacks are presently on order for evaluation.