Instrumentation Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Digital Development Memo #219

To: Eldon C. Hall
From: Albert L. Hopkins
Subj: Core Rope Memory Selection, Block II
Date: 3 November 1964

To provide for compatibility between the core rope memory and its potential successor, the braid memory, a common point of departure has been established, called the Fixed Memory Address. This is a sixteen bit total address generated as a function of the contents of S, FBANK, and the three Fixed Extension bits. It provides up to 65,536 words of fixed memory. The core rope memory contains only 36,864 words; it is not yet known how many words a braid memory might contain.

1. Conversion to Fixed Memory Address

The Fixed Memory Address depends on the bank number if the contents of S are between 2000 and 3777. It depends on the Extension bits if the Bank number is 30 or greater. A seventeenth bit not explicitly listed is the bit which distinguishes the number in S as a fixed memory address rather than erasable.

The rule for conversion is based on the fact that the 11th through 15th FMA bits are the same as the corresponding FBANK bits if $2000 \leq S \leq 3777$ and $0 \leq \text{FBANK} \leq 27$. If $0 \leq S \leq 1777$, the erasable memory is actuated and the FMA is unspecified. If $4000 \leq S \leq 7777$, the address is in fixed-fixed memory, whose FMA is the same as the contents of S.

For bank numbers between 30 and 37, the FMA depends on the Fixed extension bits. The relationship is shown in the following table.

| Fixed Extension Channel ($E_7$, $E_6$, $E_5$) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| Banks accessed by Bank Numbers 30-37 | 30-37 | 30-37 | 30-37 | 30-37 | 40-47 | 50-57 | 60-67 | 70-77 |
| FMA Bit 14 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| FMA Bit 15 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| FMA Bit 16 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

This allocation is somewhat arbitrary, and the available freedom has been used to simplify the conversion logic.

Conversion Functions:

a) Definitions:

$S_k$ contents of kth bit of S (bits 1 - 12)

$B_k$ contents of kth bit of FBANK (bits 11, 12, 13, 14, 16)

$E_k$ contents of kth bit of Fixed Extension Channel (also called Super-bank: see AGC 4 Memo #8). (bits 5, 6, 7)

$F_k$ kth bit of FMA (bits 1 - 16)

b) Descriptions:

$F_1 - F_{10} = S_1 - S_{10}$

$F_{11} = S_{11}$ for fixed-fixed
$B_{11}$ otherwise

$F_{12} = S_{12}$ for fixed-fixed
$B_{12}$ otherwise

$F_{13} = 0$ for fixed-fixed
$B_{13}$ otherwise

$F_{14} = 0$ for fixed-fixed
$B_{14}$ for Banks 0 - 27
1 for Banks 30 -37 $E_7 = 0$
$E_5$ for Banks 30 - 37 $E_7 = 1$

b) Descriptions: (cont.)

$F_{15}$ = 0 for fixed-fixed
$B_{16}$ for Banks 0 - 27
1 for Banks 30 -37 $E_7$ = 0
$E_6$ for Banks 30 - 37 $E_7$ = 1

$F_{16}$ = 0 for fixed-fixed
0 for Banks 0 - 27
$E_7$ for Banks 30 - 37

c) Functions: (Note: $S_{12}$ = 1 implies fixed-fixed. $S_{12}$ = 0 implies bank or erasable, but since the selection between fixed and erasable occurs elsewhere we can assume that $S_{12}$ = 0 implies bank. $B_{16} \cdot B_{14} \cdot S_{12}$ = 1 implies banks 30 - 37).

$F_1$ through $F_{10}$ = $S_1$ through $S_{10}$ respectively

$$F_{11} = S_{12}\, S_{11} + \overline{S_{12}}\, B_{11}$$

$$F_{12} = S_{12}\, S_{12} + \overline{S_{12}}\, B_{12} = S_{12} + B_{12}$$

$$F_{13} = \overline{S_{12}}\, B_{13}$$

$$F_{14} = \overline{S_{12}}\, [(\overline{B_{16}} + \overline{B_{14}})\, B_{14} + B_{16}\, B_{14}\, (\overline{E_7} + E_5)] = \overline{S_{12}}\, B_{14}\, (\overline{B_{16}} + \overline{E_7} + E_5)$$

$$F_{15} = \overline{S_{12}}\, [(\overline{B_{16}} + \overline{B_{14}})\, B_{16} + B_{16}\, B_{14}\, (\overline{E_7} + E_6)] = \overline{S_{12}}\, B_{16}\, (\overline{B_{14}} + \overline{E_7} + E_6)$$

$$F_{16} = \overline{S_{12}}\, B_{16}\, B_{14}\, E_7$$

2. Core Rope Addressing

Addresses in core ropes are ordered by strand number, bank number, and module number. The meaning of the preceding statement may be clarified somewhat by the following statements:

a) The first module contains the first six banks, 0 - 5.

b) The first bank contains the first two strands, 101 and 102.

c) The first strand contains two substrands: the first ones on each side of the module, 1A01 and 1B01.

d) The first substrand on side A contains the first 256 addresses of Bank 0.

The selection among the 512 cores in two substrands is effected by seven inhibit pairs plus parity and four set lines. All further selection is effected by strand selection and by rope gating, which is logically, but not electrically, redundant with strand selection.

A. Strand Selections

The number of strands in Block II is 72, rather than the 48 in Block I. In order to minimize the size of the circuitry, a coincident strand selection scheme is being implemented in Block II. In this scheme each module has one of its twelve strands selected, but only one of the six modules can communicate with the sense amplifiers.

To derive the conversion from the FMA to the twelve strand functions and the six module functions we start with a tabulation of the top seven bits of the FMA. The module functions are denoted R1, R2, S1, S2, T1, T2; the strand functions P01, P02, ... P12. The top seven bits of the FMA form a three digit octal number 000 to 107, equivalent to the decimal range zero to 71. This tabulation is given in Table 1.

| | Strand Function | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Module Function | P01 | P02 | P03 | P04 | P05 | P06 | P07 | P08 | P09 | P10 | P11 | P12 |
| R1 | 000 | 001 | 002 | 003 | 004 | 005 | 006 | 007 | 010 | 011 | 012 | 013 |
| R2 | 014 | 015 | 016 | 017 | 020 | 021 | 022 | 023 | 024 | 025 | 026 | 027 |
| S1 | 030 | 031 | 032 | 033 | 034 | 035 | 036 | 037 | 040 | 041 | 042 | 043 |
| S2 | 044 | 045 | 046 | 047 | 050 | 051 | 052 | 053 | 054 | 055 | 056 | 057 |
| T1 | 060 | 061 | 062 | 063 | 064 | 065 | 066 | 067 | 070 | 071 | 072 | 073 |
| T2 | 074 | 075 | 076 | 077 | 100 | 101 | 102 | 103 | 104 | 105 | 106 | 107 |

Table 1

Table of N as a function of module and strand, where N is composed of the top seven bits of the Fixed Memory Address.

B. Strand Functions

The inverse of the relationship expressed in this table yields the Strand and Module functions. The strand functions are decomposable into functions of $F_{10}$ and $F_{11}$ and of $F_{12}$ through $F_{16}$. Table 2 expresses the strand functions in terms of the three auxiliary functions $\phi A1$, $\phi A2$, and $\phi A3$, where:

$$\phi A1 = \overline{F_{16}} \left\{ \overline{F_{15}} \left[ \overline{F_{14}} \left( \overline{F_{13}}\ \overline{F_{12}} + F_{13}\ F_{12} \right) + F_{14}\ F_{13}\ \overline{F_{12}} \right] + F_{15} \left[ \overline{F_{14}}\ \overline{F_{13}}\ F_{12} + F_{14} \left( \overline{F_{13}}\ \overline{F_{12}} + F_{13}\ F_{12} \right) \right] \right\}$$

$$\phi A2 = \overline{F_{16}} \left\{ \overline{F_{15}} \left[ \overline{F_{14}}\ \overline{F_{13}}\ F_{12} + F_{14} \left( \overline{F_{13}}\ \overline{F_{12}} + F_{13}\ F_{12} \right) \right] + F_{15} \left[ \overline{F_{14}}\ F_{13}\ F_{12} + F_{14}\ \overline{F_{13}}\ F_{12} \right] \right\} + F_{16}\ \overline{F_{15}}\ \overline{F_{14}}\ \overline{F_{13}}\ \overline{F_{12}}$$

$$\phi A3 = \overline{F_{16}} \left\{ \overline{F_{15}} \left[ \overline{F_{14}}\ F_{13}\ \overline{F_{12}} + F_{14}\ \overline{F_{13}}\ F_{12} \right] + F_{15} \left[ \overline{F_{14}} \left( \overline{F_{13}}\ \overline{F_{12}} + F_{13}\ F_{12} \right) + F_{14}\ F_{13}\ \overline{F_{12}} \right] \right\} + F_{16}\ \overline{F_{15}}\ \overline{F_{14}}\ \overline{F_{13}}\ \overline{F_{12}}.$$

| | $\phi A1$ | $\phi A2$ | $\phi A3$ |
|---|---|---|---|
| $\overline{F_{10}}\ \overline{F_{11}}$ | P01 | P05 | P09 |
| $F_{10}\ \overline{F_{11}}$ | P02 | P06 | P10 |
| $\overline{F_{10}}\ F_{11}$ | P03 | P07 | P11 |
| $F_{10}\ F_{11}$ | P04 | P08 | P12 |

Table 2

The strand functions P01 - P12 are the logical products of the row and column heads in which they are placed in the preceding table. Thus, for instance, P07 = $\phi$A2 $\cdot$ $\overline{F_{10}}$ $F_{11}$.

The derivation of the three $\phi$A functions is probably obscure to the casual reader and perhaps equally so to the engineers concerned, so it is worth laboring the point. The number N in Table 1 is a shorthand form for a bit configuration of $F_{10}$ - $F_{16}$. The Table says, for example, that N = 0000 implies both P01 and R1. This means that $\overline{F_{16}}\ \overline{F_{15}}\ \overline{F_{14}}\ \overline{F_{13}}\ \overline{F_{12}}\ \overline{F_{11}}\ \overline{F_{10}} = 1$ implies P01 = 1 and R01 = 1 and all other P's and R's, S's and T's are <u>zero</u>. It is further true that the logical sum of all N terms which imply P01 forms an expression which not only implies P01 but is implied by P01. Thus N = 000, 014, 030, 044, 060, or 074 $\Longleftrightarrow$ P01 = 1. This is short for:

$$
\begin{aligned}
\text{P01} = \quad & \overline{F_{16}}\ \overline{F_{15}}\ \overline{F_{14}}\ \overline{F_{13}}\ \overline{F_{12}}\ \overline{F_{11}}\ \overline{F_{10}} \\
& + \overline{F_{16}}\ \overline{F_{15}}\ \overline{F_{14}}\ F_{13}\ F_{12}\ \overline{F_{11}}\ \overline{F_{10}} \\
& + \overline{F_{16}}\ \overline{F_{15}}\ F_{14}\ F_{13}\ \overline{F_{12}}\ \overline{F_{11}}\ \overline{F_{10}} \\
& + \overline{F_{16}}\ F_{15}\ \overline{F_{14}}\ \overline{F_{13}}\ F_{12}\ \overline{F_{11}}\ \overline{F_{10}} \\
& + \overline{F_{16}}\ F_{15}\ F_{14}\ \overline{F_{13}}\ \overline{F_{12}}\ \overline{F_{11}}\ \overline{F_{10}} \\
& + \overline{F_{16}}\ F_{15}\ F_{14}\ F_{13}\ F_{12}\ \overline{F_{11}}\ \overline{F_{10}}.
\end{aligned}
$$

This expression for P01 is the canonical form of the one given in Table 2, i.e., $\phi$A1 $\overline{F_{10}}\ \overline{F_{11}}$. Actually it is possible to reduce the $\phi$A functions even further, but the AGC circuits are not so constructed.

C. Module Functions

These functions are also decomposable. Five auxiliary functions are used to generate them. These are denoted $\phi B1$, $\phi B2$, $\phi B3$, $\phi C1$, and $\phi C2$, where:

$$\phi B1 = \overline{F_{16}}\ \overline{F_{15}}\ (\overline{F_{14}} + \overline{F_{13}})$$

$$\phi B2 = \overline{F_{16}}\ (\overline{F_{15}}\ F_{14}\ F_{13} + F_{15}\ \overline{F_{14}})$$

$$\phi B3 = \overline{F_{16}}\ F_{15}\ F_{14} + F_{16}\ \overline{F_{15}}\ \overline{F_{14}}\ \overline{F_{13}}$$

$$\phi C1 = \overline{F_{16}}\left\{\overline{F_{15}}\ [\overline{F_{14}}\ (\overline{F_{13}} + \overline{F_{12}}) + F_{14}\ F_{13}]\right.$$
$$\left. + F_{15}\ [\overline{F_{14}}\ \overline{F_{13}}\ \overline{F_{12}} + F_{14}\ (\overline{F_{13}} + \overline{F_{12}})]\right\}$$

$$\phi C2 = \overline{F_{16}}\left\{\overline{F_{15}}\ [\overline{F_{14}}\ F_{13}\ F_{12} + F_{14}\ \overline{F_{13}}]\right.$$
$$\left. + F_{15}\ [\overline{F_{14}}\ (F_{13} + F_{12}) + F_{14}\ F_{13}\ F_{12}]\right\}$$
$$+ F_{16}\ \overline{F_{15}}\ \overline{F_{14}}\ \overline{F_{13}}.$$

Table 3 describes the module functions,

| | $\phi B1$ | $\phi B2$ | $\phi B3$ |
|---|---|---|---|
| $\phi C1$ | R1 | S1 | T1 |
| $\phi C2$ | R2 | S2 | T2 |

Table 3

where, for example, $R2 = \phi B1 \cdot \phi C2$.

3. Implementation

A. Logic

The following is a list of functions generated in NOR logic:

1. $F15A16 = \overline{\overline{F15} \cdot \overline{F16}}$
2. $F15B16 = \overline{\overline{F15} \cdot \overline{F16}}$

3. NE00 = $\overline{F15A16} \cdot \overline{F14} \cdot \overline{F13}$
4. NE01 = $\overline{F15A16} \cdot \overline{F14} \cdot F13$
5. NE02 = $\overline{F15A16} \cdot F14 \cdot \overline{F13}$
6. NE03 = $\overline{F15A16} \cdot F14 \cdot F13$
7. NE04 = $\overline{F15B16} \cdot \overline{F14} \cdot \overline{F13}$
8. NE05 = $\overline{F15B16} \cdot \overline{F14} \cdot F13$
9. NE06 = $\overline{F15B16} \cdot F14 \cdot \overline{F13}$
10. NE07 = $\overline{F15B16} \cdot F14 \cdot F13$
11. NE10 = $F16 \cdot \overline{F15} \cdot \overline{F14} \cdot \overline{F13}$
12. NE036/ = $\overline{NE00 + NE03 + NE06}$
13. NE147/ = $\overline{NE01 + NE04 + NE07}$
14. NE2510/ = $\overline{NE02 + NE05 + NE10}$
15. ROPER = NE00 + NE011 + NE02 (= ΦB1) *
16. ROPES = NE03 + NE04 + NE05 (= ΦB2) *
17. ROPET = NE06 + NE07 + NE10 (= ΦB3) *
18. STR14 = NE036 · $\overline{F12}$ + NE147 · F12 (= ΦA1) *
19. STR58 = NE2510 · $\overline{F12}$ + NE036 · F12 (= ΦA2) *
20. STR912 = NE147 · $\overline{F12}$ + NE2510 · F12 (= ΦA3) *
21. LOMOD = NE036 · $\overline{F12}$ + NE036 · F12 + NE147 · $\overline{F12}$ (= ΦC1) *
22. HIMOD = NE147 · F12 + NE2510 · $\overline{F12}$ + NE2510 · F12 (= ΦC2) *
23. STR412 = F10 · F11 *
24. STR311 = $\overline{F10}$ · F11 *
25. STR210 = F10 · $\overline{F11}$ *
26. STR19 = $\overline{F10}$ · $\overline{F11}$ *

NOTE: * Denotes a memory interface signal.

Note that items 15 through 26 in the preceding list are identical to the row and column head functions in Tables 2 and 3. Therefore it follows that the functions P01 through P12 and the R's, S's, and T's are AND functions of items 15 through 26. These AND operations are effected in the Strand Select module using stacked transistors, as will be described shortly.

To sum up the discussion of strand and module function logic, the problem of generating 72 strand select voltages has been recast into the problem of generating twelve strand functions and six module functions. This, in turn, is solved by generating the NOR logic for the twelve functions just listed. The reason for this particular partitioning of the problem is that it uses fewer transistors and gates and fewer memory interfaces than the more straightforward approach of generating the strand and module functions entirely in NOR logic.

B. Transistor AND Functions

The strand select module contains transistor circuitry for connecting the selected Strand function line to B Plus through two PNP transistor switches, and for connecting the selected module function line to ground through a constant current source. The reason for having a current regulator is that the attenuation of the strand selection diode networks is current-dependent, and hence, in the absence of a regulator of some sort, it is dependent on supply voltage.

Figure 1 illustrates the way in which strand 000 is selected, given that the four memory interface voltages STR14, STR19, ROPER, and LOMOD are high. $Q_1$, $Q_3$, $Q_5$, and $Q_7$ are interface amplifiers. $Q_2$, $Q_4$, $Q_6$, and $Q_8$ are gating transistors, and $Q_9$ is the current limiter. The dashed lines indicate connections to other selection transistors whose roles are similar to those of $Q_4$ and $Q_8$; but because of the nature of coincident selection, $Q_4$ is the only transistor depending for its selection on both $Q_2$ and $Q_3$. A similar statement holds for $Q_8$ with $Q_6$ and $Q_7$.

C. Strand Selection Diode Networks

The coincident strand-selection method employs a thirteenth set of matched diodes in every module along with the twelve sets associated with the twelve strands. The scheme is depicted in Figure 2. The selected strand function

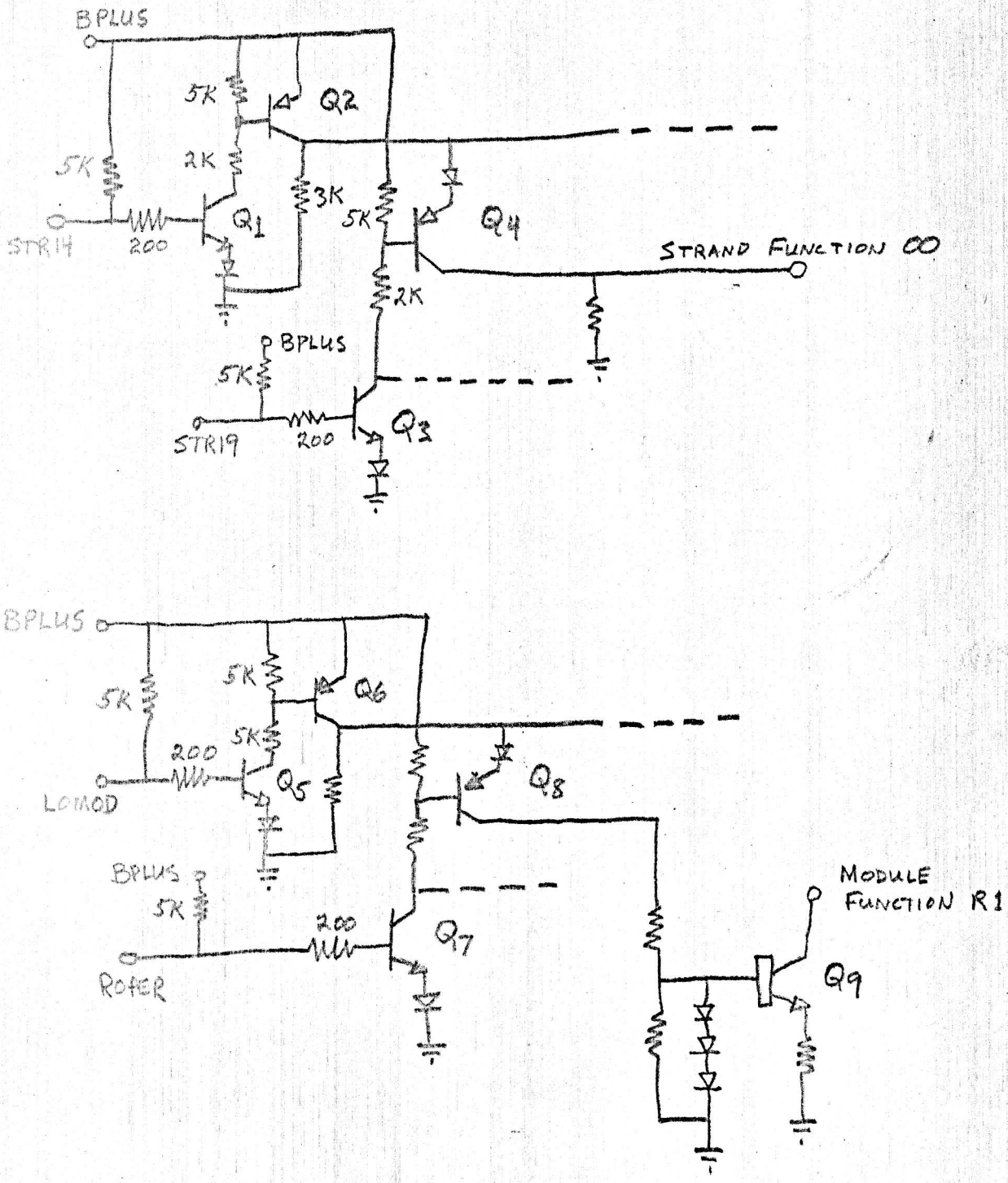


Figure 1

Transistor AND Circuits AND Current Regulator in Strand Select Module

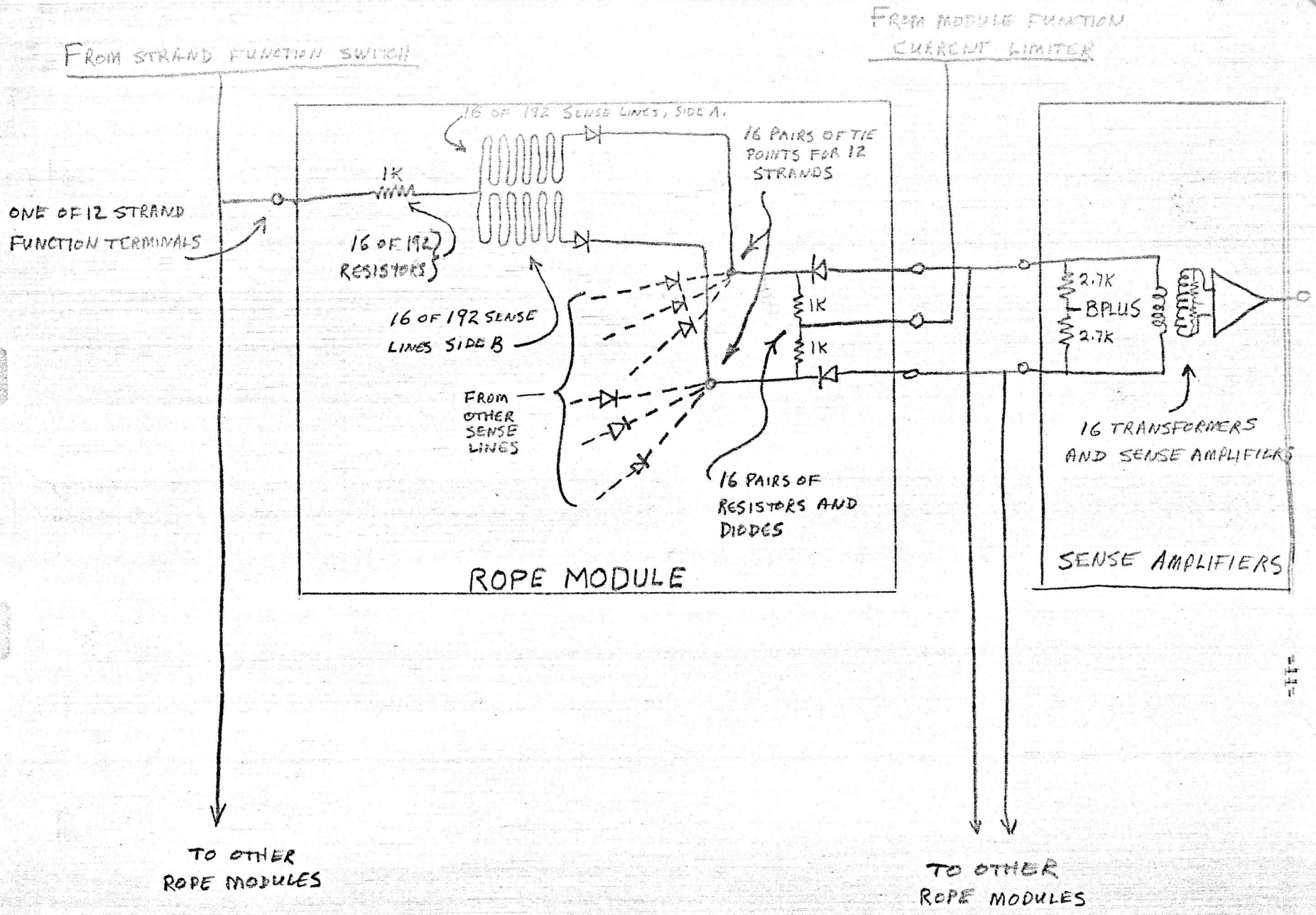


Figure 2
Rope Strand Selection

produces no current in the strand diodes unless the module function current limiter is turned on, in which case a simultaneous A.C. connection is made from the sense amplifier transformer to the module.