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Digital Development Memo #239

To: Eldon Hall
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Subj: Block II Rope Memory Circuits and Timing
Date: 26 February 1965

Rope memory operation in Block II is more sophisticated than in Block I. Rope addresses are generally known by time Eight of the memory cycle preceding every rope cycle; this allows sensing (strobing) the fixed memory on reset, rather than set time, with an attendant improvement in the signal to noise ratio. This is possible only, however, at a penalty of having rope cycles begin and then be aborted at time One whenever counter increment cycles, program interrupts, or certain quarter codes occur.

Increments and interrupts are enabled after time Eight and cause the S register's contents to change at time One whereupon an erasable memory cycle is started. Quarter codes are instructions which refer only to erasable memory. The rope memory address circuits regard any address between octal 2000 and 7777 as a rope address and begin operation if such an address is in the S register at time Eight. At time One, when the next instruction begins, the contents of the S register will be altered if the instruction is any of the following:

LXCH	ROR
INCR	WOR
ADS	RXOR
DXCH	QXCH
TS	AUG
XCH	DIM
RAND	
WAND	

Since two cores are set on any aborted rope cycle (or normal rope cycle), some means must be provided to reset these cores; this is accomplished by the addition of a CLEAR drive line for each rope. After each aborted rope cycle, all three CLEAR lines are pulsed which ensures that all cores have been reset. The pulsing of all three CLEAR lines simplifies the rope address logic since buffer address storage would have to be provided if this were not done.

RESET and SET lines have been interchanged in the Block II rope; that is, Block II ropes will have four RESET lines and two SET lines per rope. In addition to this change, the Block II SET line will thread the cores in a different manner; these changes are delineated in Figure 1.

Figure 2 shows the time relationship for the various signals required to operate the rope memory. All functions are performed when the signals are high; however, this may not be the proper polarity to operate the various drivers and memory gates.

Inhibit drivers corresponding to the selected address are turned on when signal IHENV is present. Since the rise times of the inhibit currents are slow (2.0 to 2.5 μsec.), the set current is not turned on until 1.75 μsec. after signal IHENV is present; this is done to ensure that all inhibit currents are of sufficient amplitude to inhibit all unselected cores. Inhibit current rise times are slow due to the high inductance of the drive lines (38 to 73 microhenries for Block I ropes). Assuming a normal rope cycle, the reset current will be turned on at time Five and will reset the two previously set cores. If, however, an aborted rope cycle occurs, the clear fixed current drivers will be turned on at time Two, and these clear currents will reset the two previously set cores. Signal SBF (strobe fixed memory) and STRGAT (strand gate) will be present only during a normal rope cycle.

In the Block II rope, the nominal value of the set and reset Current will be 450 milliamperes. This value of current results in a larger amplitude signal and faster core switching. It is particularly advantageous to have large signals since strobing will be done at reset time where cores are being switched into their normal state and there is no danger of overdriving the cores. Also the transmission path for the sense line signals will have four diodes in it; the forward diode resistance will attenuate the sense line signals more than the Block I system which only had two diodes; however, the Block II strand selection system was designed on the premise that strobing would be done during reset time where a large amplitude signal would be present.

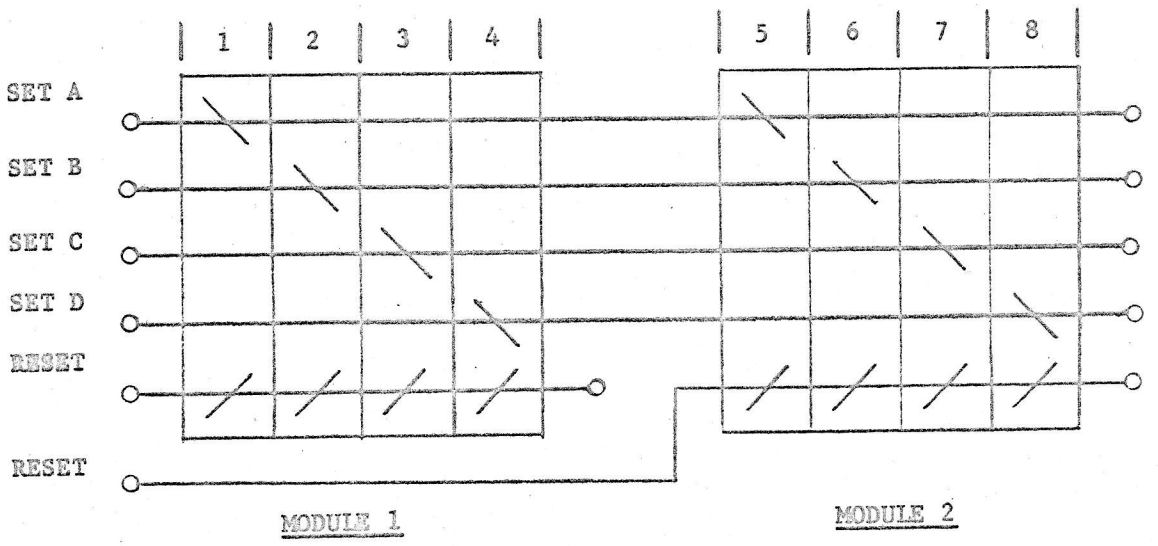
Since IHENV signal time duration is restricted to 4.5 μsec. the amplitude of the set current will be 450 milliamperes to ensure that all selected cores are completely set in 2.75 microseconds and no partial setting occurs.

To offset this increase in set current, the parity inhibit currents will be increased to 300 milliamperes to prevent setting of a core in an adjacent section of the rope. To illustrate (see Figure 1), assume the SET AB current driver is turned on and that the desired core corresponding to a selected address is located in section one. Under this condition all cores in

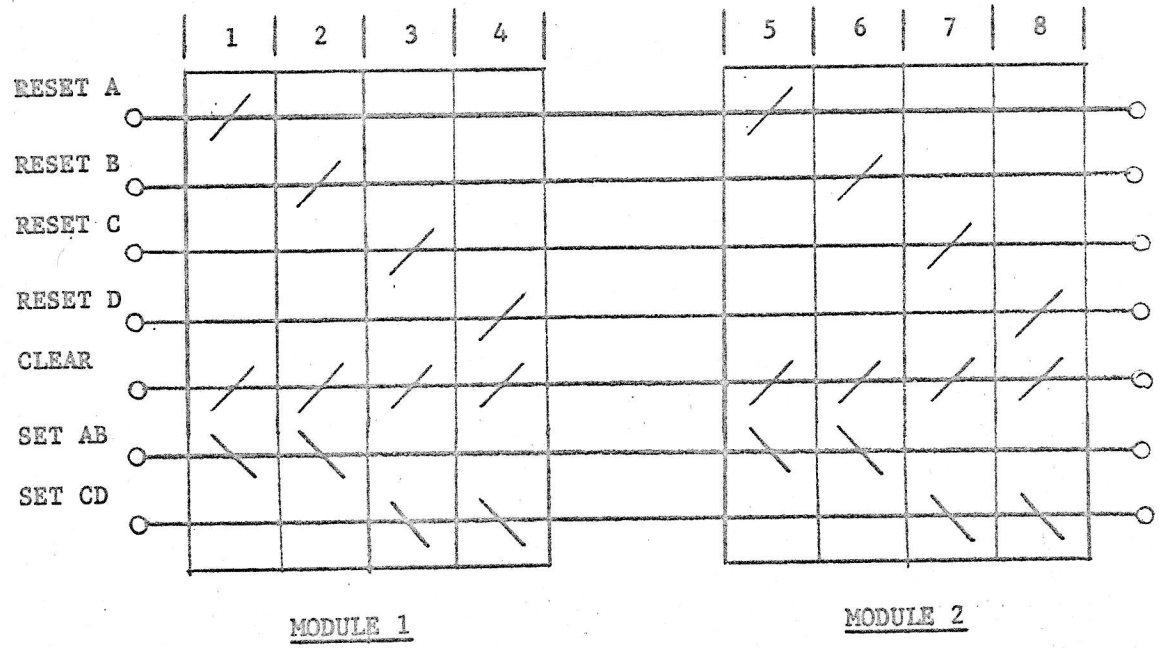
sections 1 and 5 except the desired core will be at least doubly inhibited. One core in sections 2 and 6 will have only the parity inhibit current flowing. With a parity inhibit current of 300 milliamperes the net excess current in the direction which sets the core will be only 150 milliamperes; therefore cores in sections 2 and 6 will not be set. Because of this only two cores will be set at SET time and the desired core is communicated with by the strand select circuitry. It should be remembered that an 8-bit parity logic circuit (bits 1 to 8 of the S register) is used to control the parity inhibit drivers. To illustrate its operation, assume again that the desired core is located in section 1 and that the SET AB current driver had been turned on. Under this condition (assuming a normal rope cycle), the Reset A current driver will be turned on and will reset the cores in sections 1 and 5. Bits 8 and 9 of the S register are in the logical "0" state under this condition. In order to turn on the RESET B current driver bit 8 will be a logical "1" and bit 9 a logical "0." Since the parity inhibit drive lines thread the cores in the even and odd numbered sections of the rope in a complementing manner it can be seen that if a selected core in an odd numbered section (say section one) has the PARITY drive line threading it, the adjacent core in the even numbered section (say section two) will have the $\overline{\text{PARITY}}$ drive line threading it. Thus it can be seen that the parity inhibit currents prevent the setting of four cores at SET time and only two cores are set and reset during a rope cycle.

The remaining inhibit drivers (controlled by bits 1 to 7 of the S register) will have a nominal current value of 225 milliamperes. Clear drive currents, which have a time duration of 4 microseconds, will have a nominal current value of 300 milliamperes.

Because of the high resistance and inductance associated with the various drive lines, the reset, set, and clear drivers have been redesigned and the output transistors are being returned to ground rather that 4 volts d-c. A circuit diagram for the new driver is shown in Figure 3. The operation of the circuit is similar to the Block I rope driver; the major difference being the pre-driver where the NPN transistor has been replaced by a PNP. This is desirable since a noisy ground on the driver output stage will not turn on the pre-driver which is controlled by the input NPN transistor whose emitter will be returned to a quiet ground.



BLOCK I ROPE



BLOCK II ROPE

FIGURE 1. BLOCK I AND BLOCK II ROPE ORGANIZATION DIAGRAM

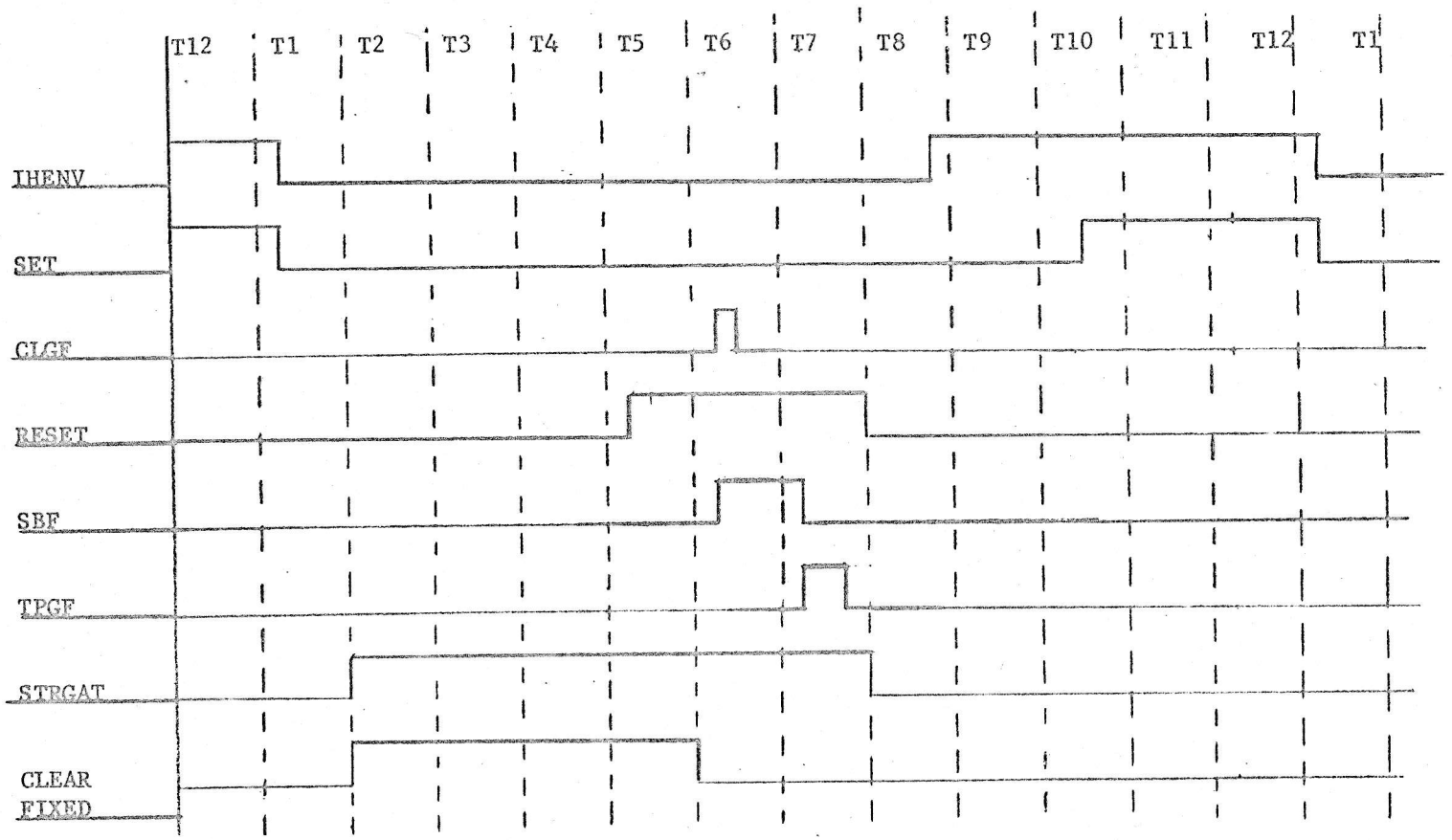
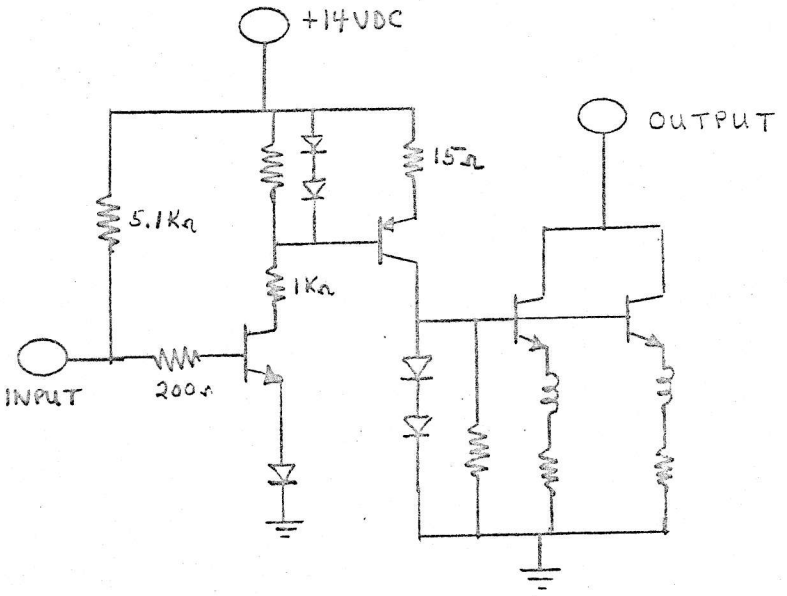
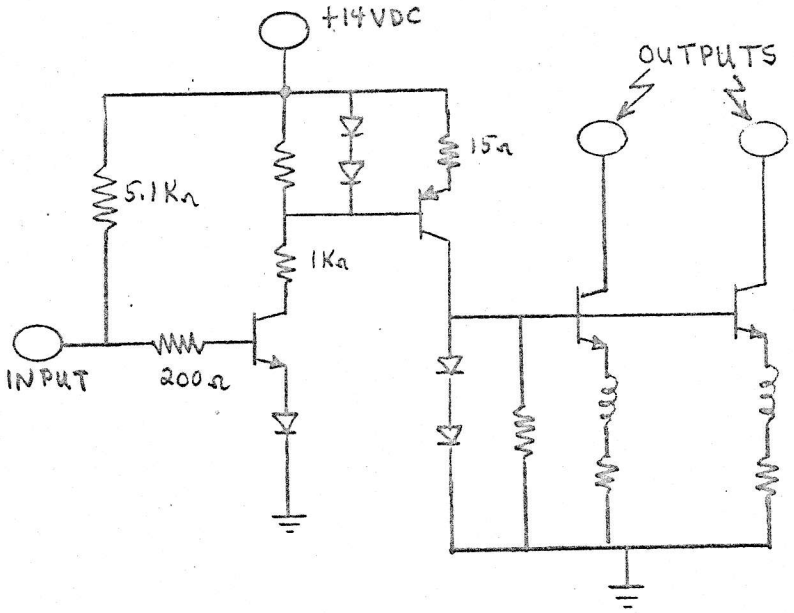


FIGURE 2

BLOCK II ROPE MEMORY TIMING DIAGRAM



SET & RESET DRIVER



CLEAR DRIVER

FIGURE 3. BLOCK II SET, RESET & CLEAR DRIVER DIAGRAM