Instrumentation Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Digital Dev. Memo #252

To: Eldon Hall
From: Don Bowler , Jack McKenna
Date: 20 April 1965
Subj: Attitude Hand Controller

This memo will be divided into the following sections:

I. Hand Controller Specifications

II. Analogue to Digital Converter Operation

III. Computer Operation

IV. Test Equipment Requirements (CTS)

V. Production - Packaging Considerations

I. HAND CONTROLLER SPECIFICATIONS

The hand controller specifications are contained in ICD LIS-370-10004. The specifications are as follows:

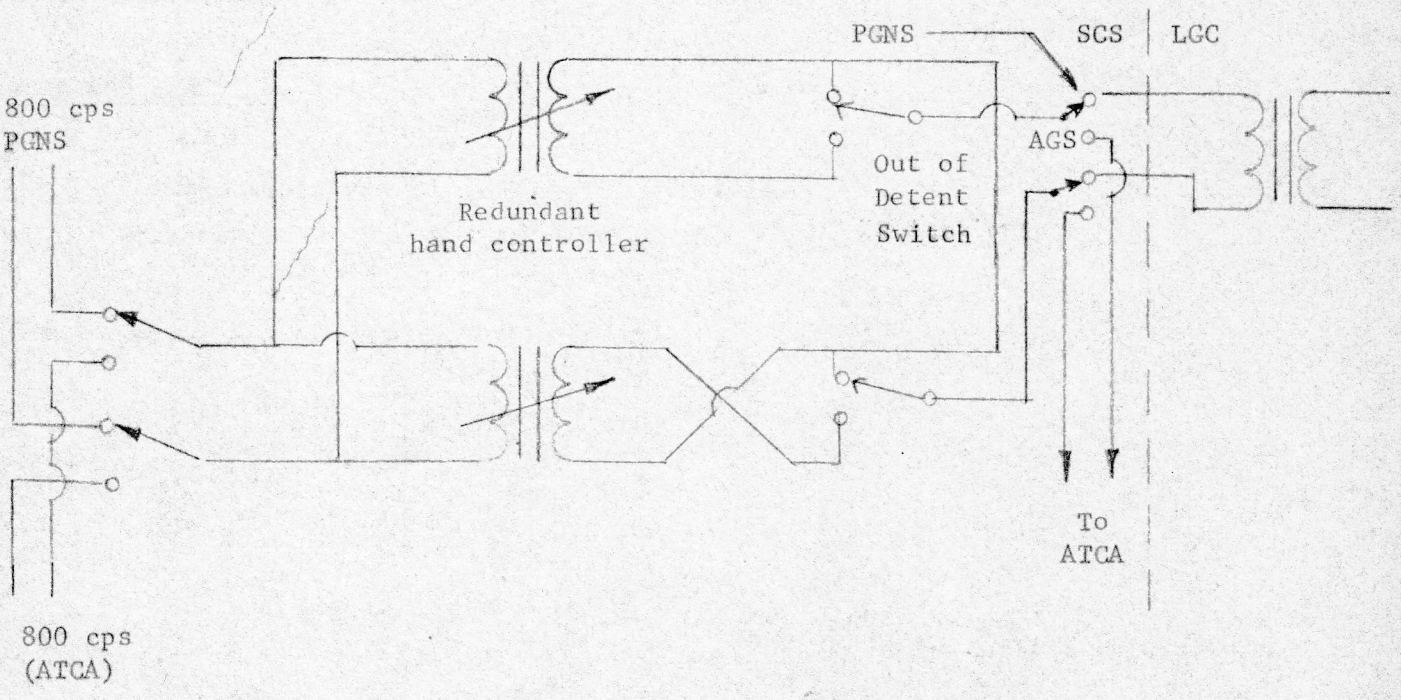


Fig. 1. Single Channel.

Hand Controller

Out of detent indication	3/4° ± 1/4°.
Null voltage	30mv. rms max., load 20k ohm.
Quadrature	10mv. rms max., load 20k ohm.
Scale factor	2.8 volts ± 0.14 volts rms at 11° hand controller position, load 20k ohm.
Source impedance	2k at 85°.
Rate Command	7.15°/sec - volt rms.
800 cps excitation	(PGNS 800 cps).
Phase shift	0 - 10° max into 20k ohms load.

In-phase output corresponds to positive rate command.

Linearity	5%

A Circuit

Linearity	± 10%, $1/2 < \theta < 12°$.
Quantization	32 states/11°.
Load impedance	Non-linear 2 - 20k.
Sample rate	5 - 8/sec.

PGNS 800 cps

Voltage amplitude	28v ± 2%.
Phase shift	± 10°.

II. ANALOGUE TO DIGITAL CONVERTER

One channel of the analogue to digital converter is shown in Fig. 2.

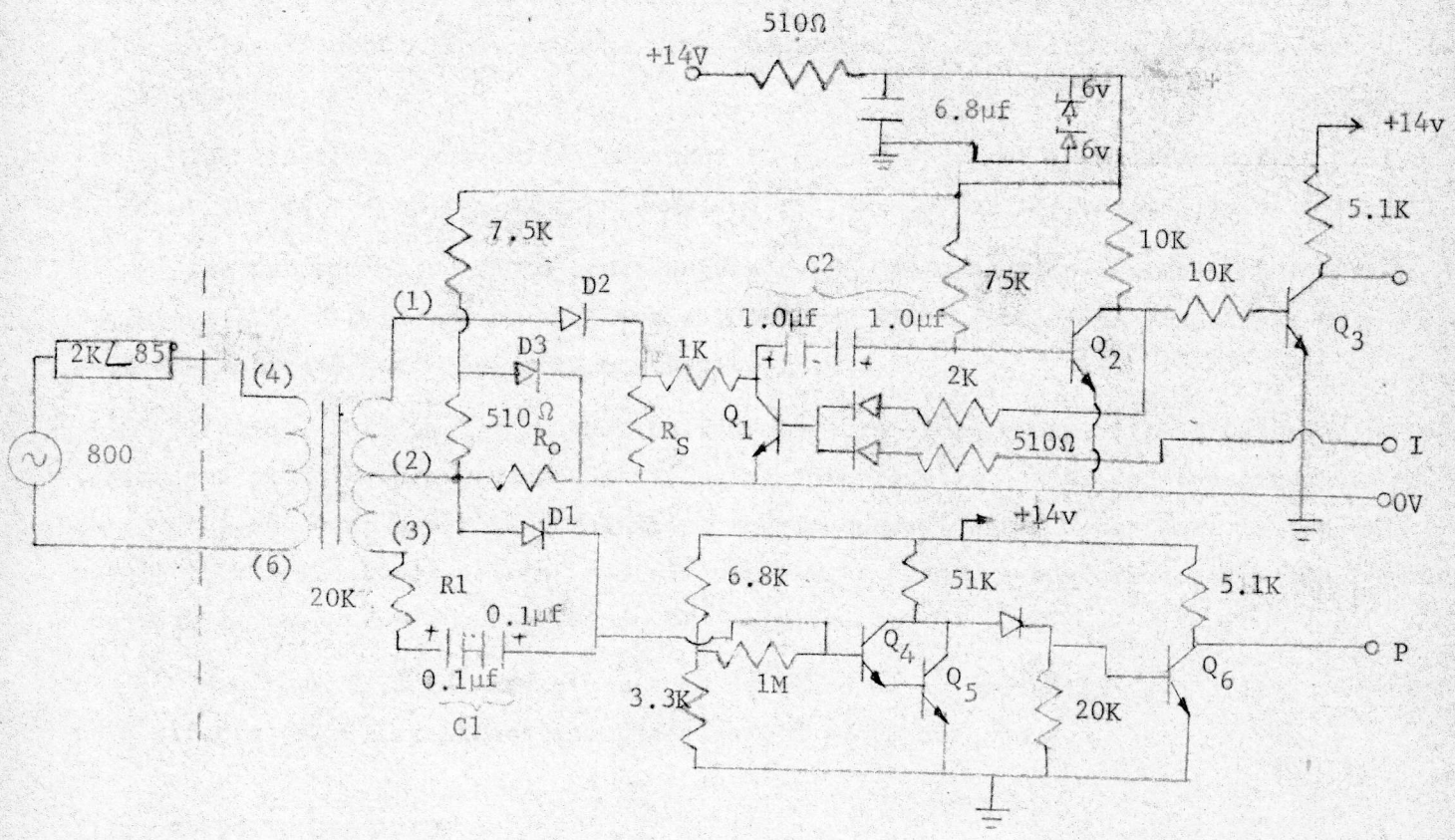


Fig. 2. Analogue to Digital Converter.

The upper half of the transformer secondary is used to charge a capacitor which on the application of a pulse at I holds off Q_2 for a length of time proportional to the peak voltage at the input.

The bottom half of the transformer is used to square up the input sinusoid in order to detect phase. The function of R1 and C1 is to provide some lead to make up for the lag in the source and together with D1 and the base to emitter junction of Q4 and Q5, provides a fairly constant load across the transformer. This load is shunted by the combination D2, C2, and R_S (actually R_S when C2 is charged up). The purpose of R_S is to allow C2 to discharge when the hand controller is not out of detent. It can also be used as a fine control to set the sensitivity of delay out for voltage in. The discharge time constant is fairly long, on the order of 0.2 seconds.

When the hand controller is taken out of detent C2 charges up through D2 (assuming Q1 off) and the base to emitter path of Q2. The charging time constant is a function of the source impedance and also the winding impedance of the transformer which is significant. That is, the D.C. resistance of one half the secondary of T1 is 525 ohms.

The effective charge time constant is on the order of 10 milliseconds. This is based on the fact that the maximum sampling rate is 30 cps for maximum input.

The purpose of D3 is to provide temperature compensation and R0 is a selected resistor. It is selected so that for a 100mv rms signal, one gets no output. It controls the dead band (noise insensitivity).

The impedance that the upper half of the transformer presents is the winding resistance plus 1k when the circuit is being interrogated. When the capacitor has charged up and one is not interrogating, the impedance of the upper half is approximately 180k. The lower half of the circuit always presents approximately a 20k impedance and that is the purpose of the diode D1 (see above).

Some test data for the circuit is attached as an appendix. Linearity, temperature effects, sampling effect and phase margin plots are shown.

III. COMPUTER OPERATION

Figure 3 indicates a preliminary mechanization.

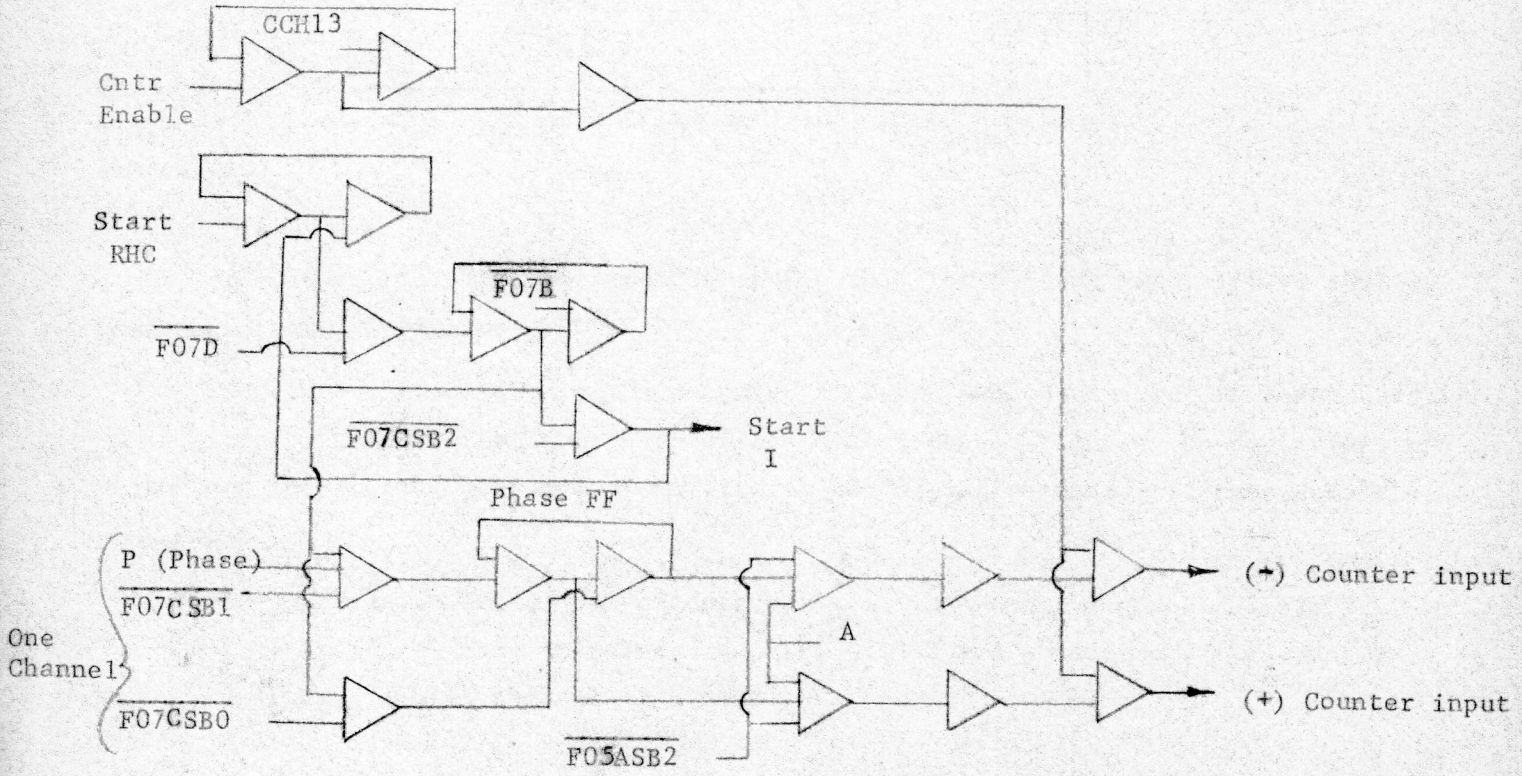


Fig. 3.

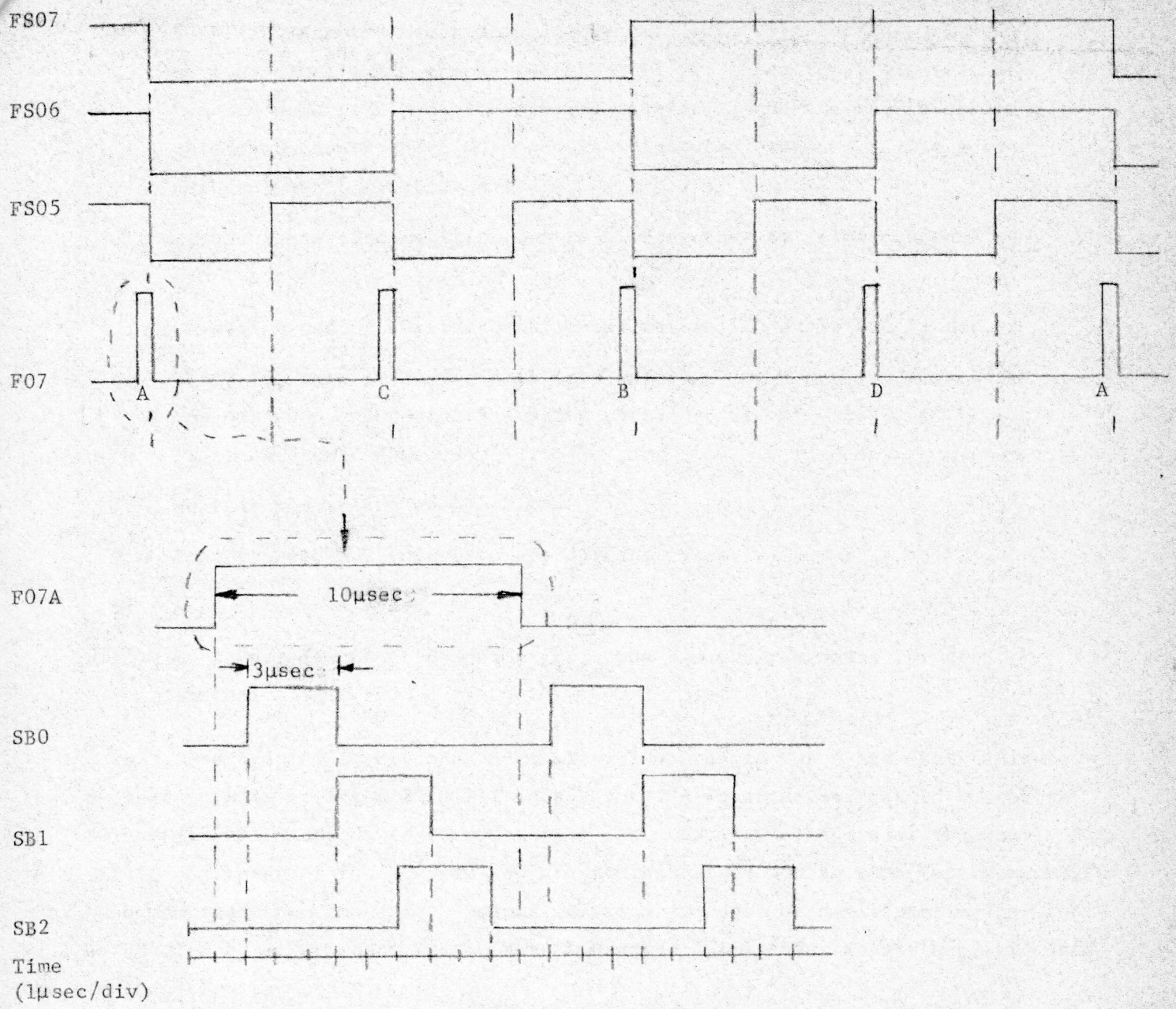


Fig. 4.

The appropriate timing is shown in Fig. 4. The 800 cps PGNS will be 180° out out phase with FS07 above.

The first indication to the computer that the hand controller is being used is that given by an interrupt generated by the out of detent signal. On receiving this interrupt the program goes into waitlist for 40-60 milliseconds. It then does the following:

1. Checks to see if out of detent signal is present, channel 31 bit 3.
2. If it is, then it resets counters 42, 43 and 44 and sets the counter enable bit, channel 13 bit 12.

3. Next, it sets the start RHC bit channel 13 bit 9. Setting RHC sets up a sequence which checks the phase of all three input signals, at the mid point (90°) of the 800 cps waveform (generates an interrogate pulse and counts the 3200 pps pulses into the counters on the appropriate lines). Figures 3 and 4.

4. It then goes into waitlist for 20 milliseconds to allow counters to get loaded.

5. On coming out of waitlist, it checks to see if enable bit is set.

6. If it is, then it puts a call into waitlist for milliseconds depending on the desired sampling rate (5-8 times 1 sec), (if it isn't it is in step 2 above).

7. Next it resets the enable bit.

8. Converts counter inputs to appropriate rates.

9. Goes into rate program.

(2') In step 2 if out of detent signal gone the program rests the trap channel 13 bit 12.

The above program is not the one that will be run in the system but indicates that one has to wait at least 25 milliseconds for the input capacitors to charge up and at least 10 milliseconds to read out into the counters. The use of the enable bit to indicate what part of the program you are coming out of and to stop the counters so that when you read them they have stopped counting (in case of a malfunction) probably will be handled by other means in the actual program. All these inputs are read into the counters simultaneously.

The phasing is determined from the original waveform to a tolerance of ± 20°. The phase drawing in the appendix indicates the circuitry could stand ± 45° so there is a safety factor of ± 25°. As seen in Figure 4 and 5 the phasing is determined just before each reading of the input and is centered in the center of the output 800 cps; set and reset pulses (90°).

IV. TEST EQUIPMENT REQUIREMENTS (CTS)

Since it will be necessary for the Computer Test Set (CTS) to test the hand controller an 800 cps in phase ($\overline{F07S}$) square wave has been provided at the interface.

The test set will have to have the ability to change phase (by 180°) and supply an 800 cps variable amplitude sinusoid. The sinusoid will have to be linear enough to check the linearity requirement of the computer circuitry (refer Section I). This is felt to be accomplished if the CTS performs the following four measurements:

1. 80 mv rms input no output.
2. 900 mv rms input 10 ± 1 counts.
3. 1800 mv rms input 21 ± 1 counts.
4. 2700 mv rms input 31 ± 2 counts.

Measurements to be made on all three counters at the same time. That is, the CTS could do the following:

1. Apply 800 cps voltage to all three inputs, setting the input to one of the 4 values above.
2. Clear counters 42 - 44.
3. Set out bits channel 13-8 and channel 13-9 (step 3 shouldn't occur sooner than 30 milliseconds after step 1).
4. Read counters.

V. PRODUCTION - PACKAGING CONSIDERATIONS

Both R_o and R_S for each of the three circuits should be positioned so that they can be changed if necessary. The nominal value of R_o is 1.1k and has been found to be quite repeatable in breadboard circuitry, however, if the noise level of the input were to be out of specification, one might need to change this value. R_o controls the dead band or noise immunity and R_S the slope of the voltage in vs counts out.

The components required in these circuits have been included in D.D. Memo #242. It would be desirable to select R_o and R_S after the rest of the circuitry has been potted.

R_o is selected with a nominal value of 120K ohms for R_S and a 100mv rms 800 cps sine wave to the input (strobe pulse removed while measuring). The source impedance will be 2K $\angle$ 85° (800 cps). The largest value of R_o (from the selected values) which does not cause an output at Q_3 with an input strobe at I is the value to be wired in. The strobe rate should be about 10/sec and the pulse width approximately 3 μsec.

R_S is selected next with the above value of R_o in place. The input is set to 2.8 volts rms and interrogated at the positive peak* (transformer pin #4 positive with respect to pin #6) of the input cycle at approximately 10 times/sec (the interrogate

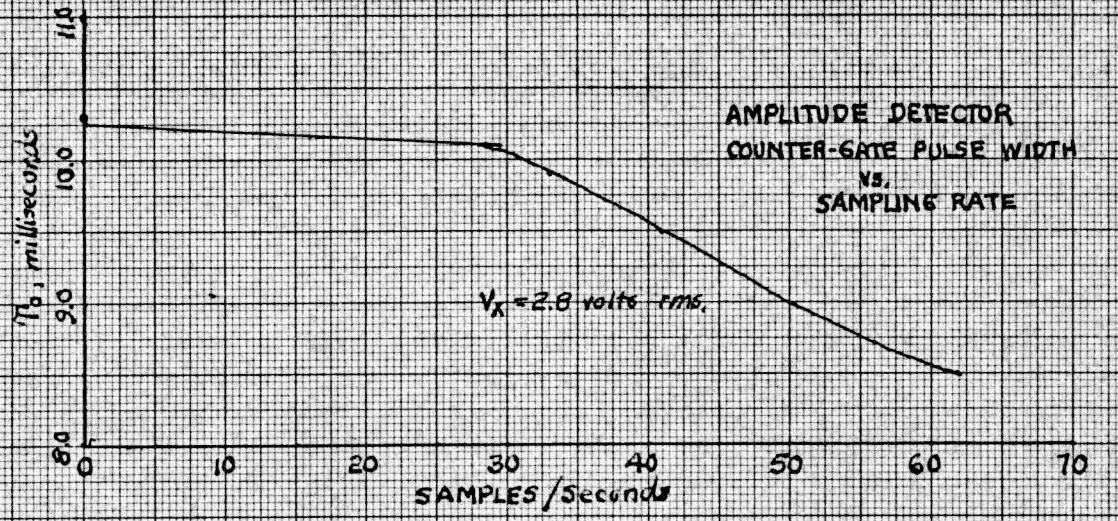
*If one is not able to synchronize the interrogate signal the error is of the order of 0.1 millisecond.

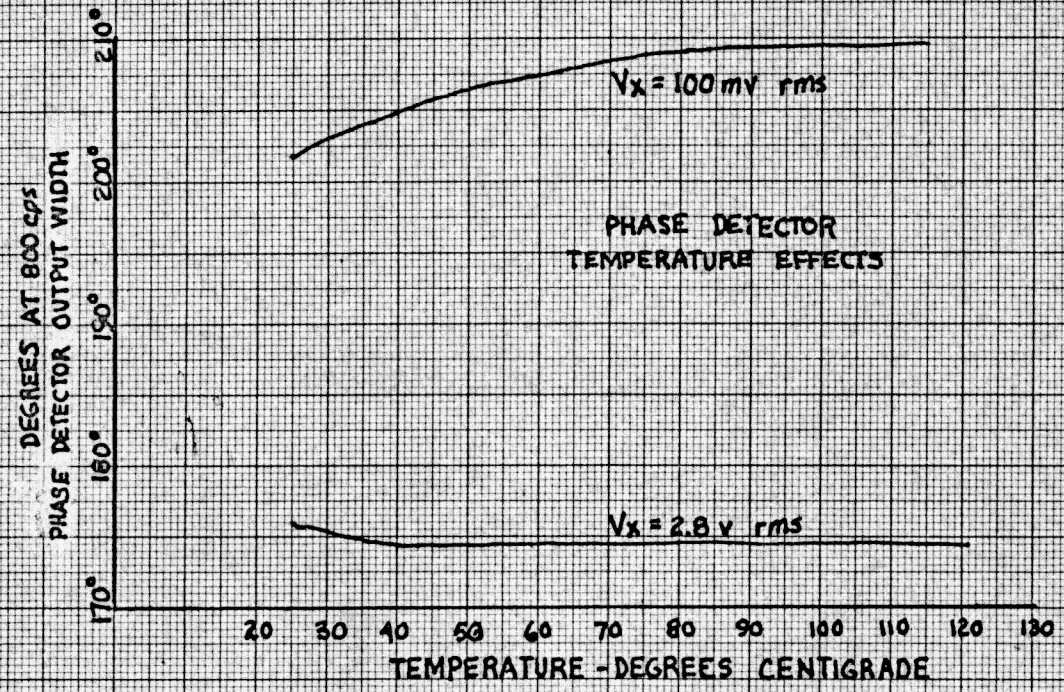
pulse should be off while measuring the input). The smallest value of R_S which produces an output greater than 10 milliseconds is the value to be wired in.

Dist.
D.D. Group
D. Hoag
M. Trageser
T. Lawton
R. Crisp
P. Felleman
N. Sears
E. Olsson
D. Scolamiero
C. Sperling
W. Dawson
W. Lund
J. Yackich
J. Lawrence
I. Laats

1.00 1.10 1.20 1.30 1.40 1.50

1/13/65





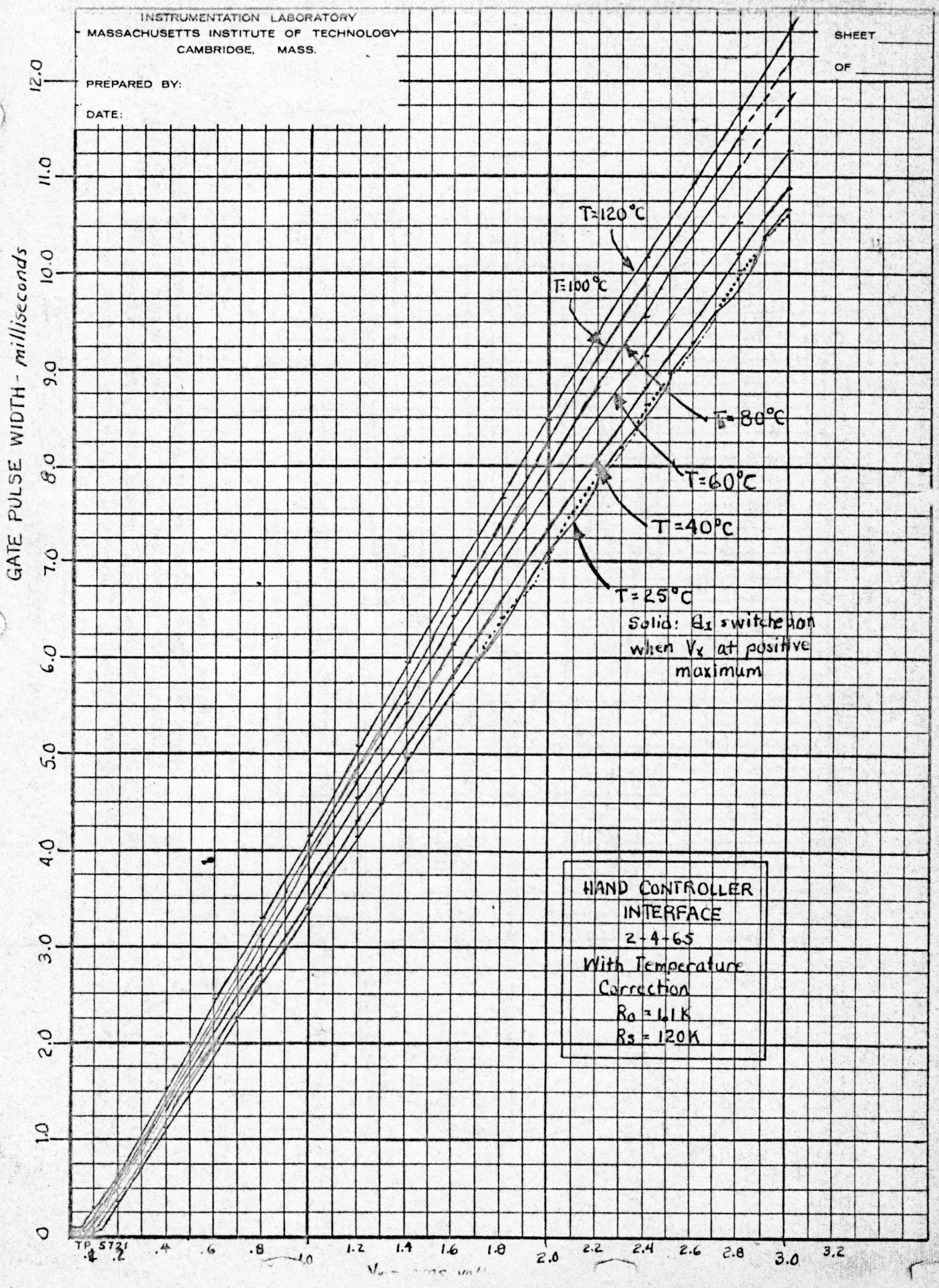
INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

PREPARED BY:

DATE:

SHEET _____

OF _____



PHASE DETECTOR

1/13/65

Solid Curves apply when amplitude detector presents high impedance. (When not sampling or charging). Broken curves apply for θ_1 on (gate pulse being delivered.) When charging capacitor, performance is between the dotted and solid curves.