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Digital Dev. Memo #255

To: Albert Hopkins
From: Donald Reible
Date: 20 May 1965
Subj: Block II Alarm Circuits

The purpose of this memorandum is to amend D.D. Memo #243 to include a brief description of the Warning Integrator Alarm which has been added to the Alarm Stick and the Scaler Alarm circuit which has been redesigned since D.D. Memo #243 was issued. In addition to the above mentioned changes, a +5 VDC voltage source has been added to the alarm stick. The incorporation of a voltage source eliminated the need for several zener diodes and nominal resistors which are generally required when a reference voltage must be applied to a threshold detector. Circuit equations are included in this memo only when they aid in describing the circuit from a system point of view, that is, in determining time intervals between pulses or time delay variations caused by variations in the power supply or component tolerances.

Scaler Alarm

For the Block II scaler alarm (see Fig. 3) the input will monitor the 3.125 cps scaler output instead of the 100 cps scaler output monitored in the Block computer. The operation of the scaler alarm circuit is as follows; when signal SCAS15 (3.125 cps) goes high, transistor Q1 turns on and its collector goes high; this collector signal is differentiated and fed to the base of Q3. When transistor Q3 turns on, it turns on transistor Q2 which now supplies the base drive required to hold transistor Q3 on. These two transistors will remain on until the charge stored on capacitor C2 is reduced to a point where the current flow is less than the "holding current" of transistors Q2 and Q3. Under normal circumstances the voltage present on C2 is less than the "turn-on" voltage of transistor Q5; therefore, transistors Q4, Q5, and Q6 are normally off and signal SCAFAL is low.

Resistor R9 and capacitor C2 form an integrating network with a time constant which is sufficiently long so that during the charging interval the voltage present on C2 is less than the "turn-on" voltage of Q5. For the purpose of analysis, assume that transistors Q2 and Q3 have just turned off; the voltage present on capacitor C2 is now low and will be defined as $V_{c2}(T_1)$. The voltage present on C2 will now rise and will behave according to equation 1 below.

$$V_{c2}(t) = [VS1 - V_{c2}(T_1)][1 - \epsilon^{-\frac{t}{\tau_2}}] + V_{c2}(T_1) \qquad [T_1 \leq t \leq T_2] \qquad (1)$$

where:

$VS1$ = BPLUS

$V_{c2}(T_1)$ = Initial voltage present on C2

$V_{c2}(t)$ = Voltage present on C2 as a function of time for $[T_1 \leq t \leq T_2]$

τ_2 = Time constant (R9)(C2).

T_2 = Time when Q2 and Q3 turn on.

Time relationships between the input signal (SCAS15) and the voltage present on C2 are shown in Fig. 1.

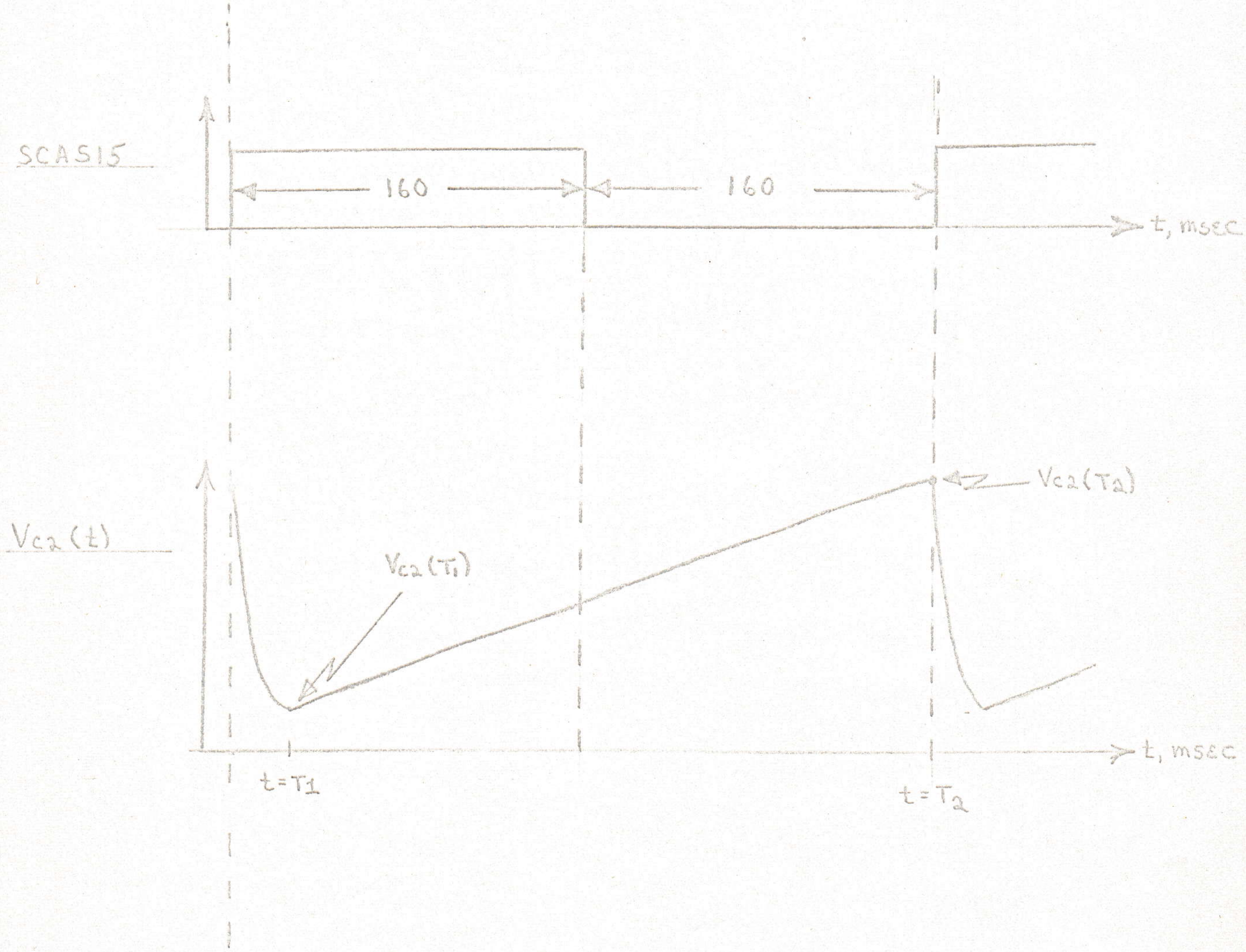

Fig. 1. Time relationship of SCAS15 and $V_{c2}(t)$.

Assuming the following constants:

$VS1 = 14$ volts.

$V_{c2}(T_1) = 0.8$ volts.

$\tau_2 = 0.884$ sec.

$[T_2 - T_1] = 317$ msec.

the voltage present on C2 at time T_2 may be calculated and yields

$$V_{c2}(T_2) = [13.2][1 - \epsilon^{-\frac{.317}{.884}}] + 0.8 = 4.76 \text{ volts.}$$

In order for the scaler alarm to function properly with a proper input frequency, the voltage present on C2 must always be less than the "turn-on" voltage of Q5. Assuming the minimum voltage for "turn-on" of Q5 is 6.3 volts, the worst-case voltage present on C2 must be less than this voltage. Worst-case occurs when the following constants exist:

$VS1 = 16.2$ volts.

$V_{c2}(T_1) = 1.0$ volts (assumed).

$\tau_2 = 0.78$ sec.

$(T_2 - T_1) = 0.317$ sec.

With these constants $V_{c2}(T_2)$ yields

$$V_{c2}(T_2) = (15.2)(1 - \epsilon^{-\frac{.317}{.780}}) + 1.0 = 6.075 \text{ volts.}$$

As the temperature increases the base to emitter voltage of transistor Q5 decreases causing the "turn-on" voltage to decrease, however, this decreased "turn-on" voltage is compensated by a decrease in $V_{c2}(T_1)$. The scaler alarm is designed so that if for some reason the input frequency decreases to 1.5625 cps an alarm condition will occur. If however the frequency were to increase to 6.25 cps, no alarm condition will occur.

Warning Integrator

The warning integrator performs the basic function of integrating pulses that are initiated whenever a Restart is called for by the computer. The input (due to logical gating) has a maximum input rate of six (6) pulses per second; each pulse has a duration of 1.125 milliseconds. Because of this gating, the warning integrator will not receive an input pulse each time a Restart is called for by the computer. The warning integrator (see Fig. 4) operates in the following manner. A positive pulse on the input (signal FILTIN) turns on transistor Q1 which, in turn, turns on a constant current source which supplies a fixed amount of charge to capacitor C1. This fixed amount of charge adds essentially a voltage step to capacitor C1. The occurrence of 5 pulses in rapid succession will cause the voltage on capacitor C1 to increase to the threshold voltage of transistor Q3A. When Q3A turns on Q4, Q5 and Q6 turn on; the turning on of these transistors causes the threshold detector to be regenerative. When Q6 turns on the threshold present on the base of transistor Q3B is lowered to approximately 2.0 volts which holds signal FLTOUT high for approximately 5 seconds.

When transistor Q2 turns on, the charge supplied to capacitor may be calculated from equation 2

$$Q_s = \int_0^{T_c} I\,dt = I \cdot T_c \qquad (2)$$

where T_c is the time duration of the positive portion of the FILTIN signal namely 1.125 milliseconds and I is the collector current of transistor Q2. Ignoring leakage current and assuming a transistor alpha of one, the collector current may be calculated

$$I = \frac{V_z + V_D - V_{be}}{R4}$$

Because R5 is extremely large, it can further be assumed that the total charge supplied by Q2 during the charging time interval is stored by C1. To determine the voltage change (ΔV) present on C1 after a charging time interval, the stored charge may be equated to the charge supplied

$$\Delta Q_{stored} = C1\ (\Delta V) = Q_{supplied} = I\ T_c$$

or

$$\Delta V = \frac{I\ T_c}{C1} = \frac{[V_z + V_D - V_{be}]}{[C1]\ R4}\ T_c \qquad (3)$$

Using the following constants, the maximum, minimum and nominal values of ΔV may be calculated.

the circuit. Voltage waveforms for the input (FILTIN) and the capacitor C1 with a periodic input are shown below in Fig. 2.

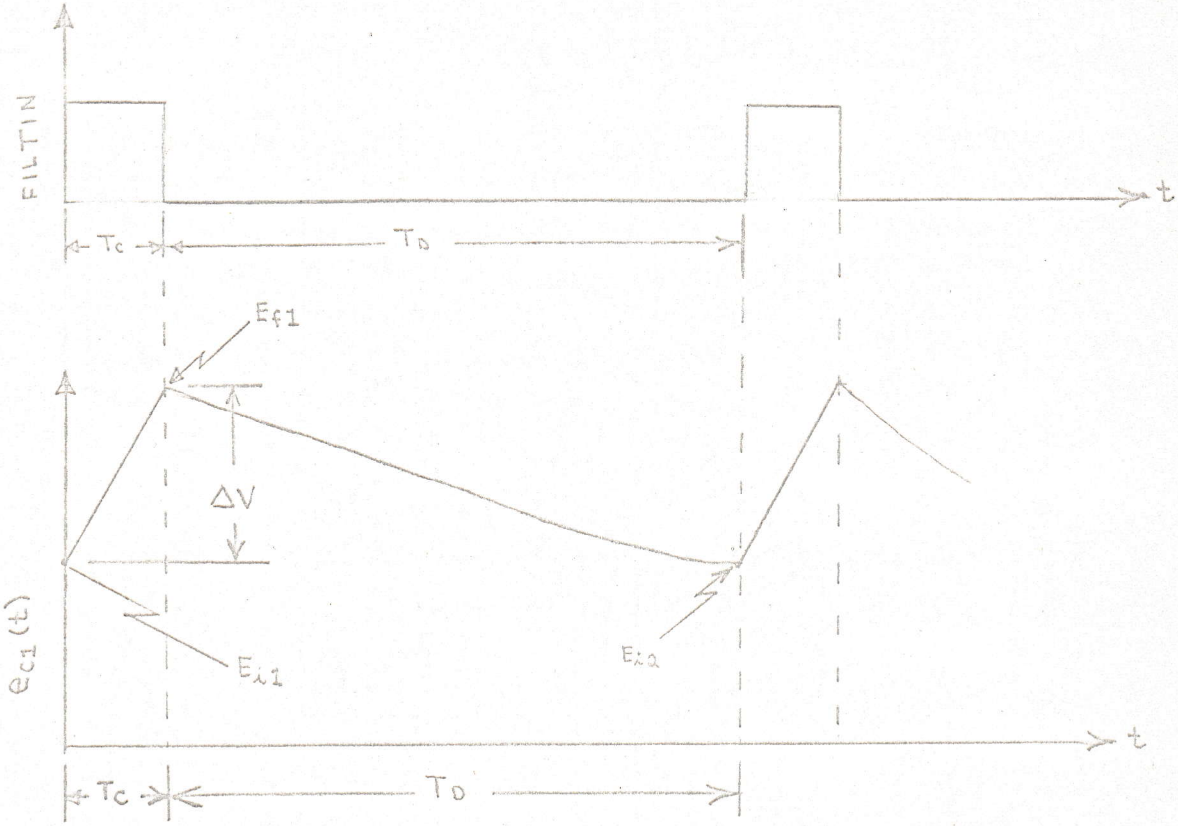

Fig. 2. FILTIN and $e_{c1}(t)$ voltage waveforms.

To obtain a mathematical solution, an initial voltage (E_{i1}) is assumed and successive equations are written and the appropriate unknown constant eliminated.

$$E_{fI} = E_{i1} + \Delta V \tag{6}$$

$$E_{i2} = E_{f1}\, \epsilon^{-\frac{T_D}{R_5\ C1}} = E_{i1} \tag{7}$$

In order to reach a threshold, E_{f1} must be equal to or greater than 4.0 volts. Since ΔV is known, T_D may be solved once E_{f1} is set equal to 4.0 volts. Therefore

$$T_D = -\ (R5)(C1)\ \mathrm{Ln}\ \frac{[E_{f1} - \Delta V]}{E_{f1}} \tag{8}$$

Substituting the appropriate constants into equation 8 results in (1) $\overline{T_D} = 2.05$ sec, (2) $T_{D(nom)} = 1.635$ sec and (3) $\underline{T_D} = 1.195$ sec. Thus it can be seen that with a periodic input, FILTIN pulses spaced 1.195 sec apart will result in an alarm condition. If C1 is initially discharged, the number of pulses which must be applied to the circuit to create an alarm condition is directly a function of the rate at which they occur. Experimentally it has been determined that six pulses spaced 1 second apart will create an alarm condition with C1 initially discharged, and if the pulse spacing is increased to 2 seconds, no alarm condition will occur.

In order to calculate the minimum input pulse rate which will maintain an alarm condition once a threshold voltage is reached, equations 6 and 7 are solved by eliminating E_{f1}; this results in equation 9.

$$T_D{}' = -\ (R5)(C1)\ \mathrm{Ln}\ \frac{E_{i1}}{E_{i1} + \Delta V} \tag{9}$$

In equation 9, $T_D{}'$ is the maximum time separation of pulses allowable after a threshold voltage is reached in order to maintain an alarm condition and E_{i1} is the reduced threshold voltage, namely 2.0 volts. Substituting the appropriate constants into equation 9 results in $\overline{T_D}{}' = 2.93$ sec, $T'_{D(nom)} = 2.51$ sec, and $\underline{T_D}{}' - 1.85$ sec. Thus it can be seen that with a periodic input, FILTIN pulses spaced 1.85 seconds apart will maintain an alarm condition once this state is reached.

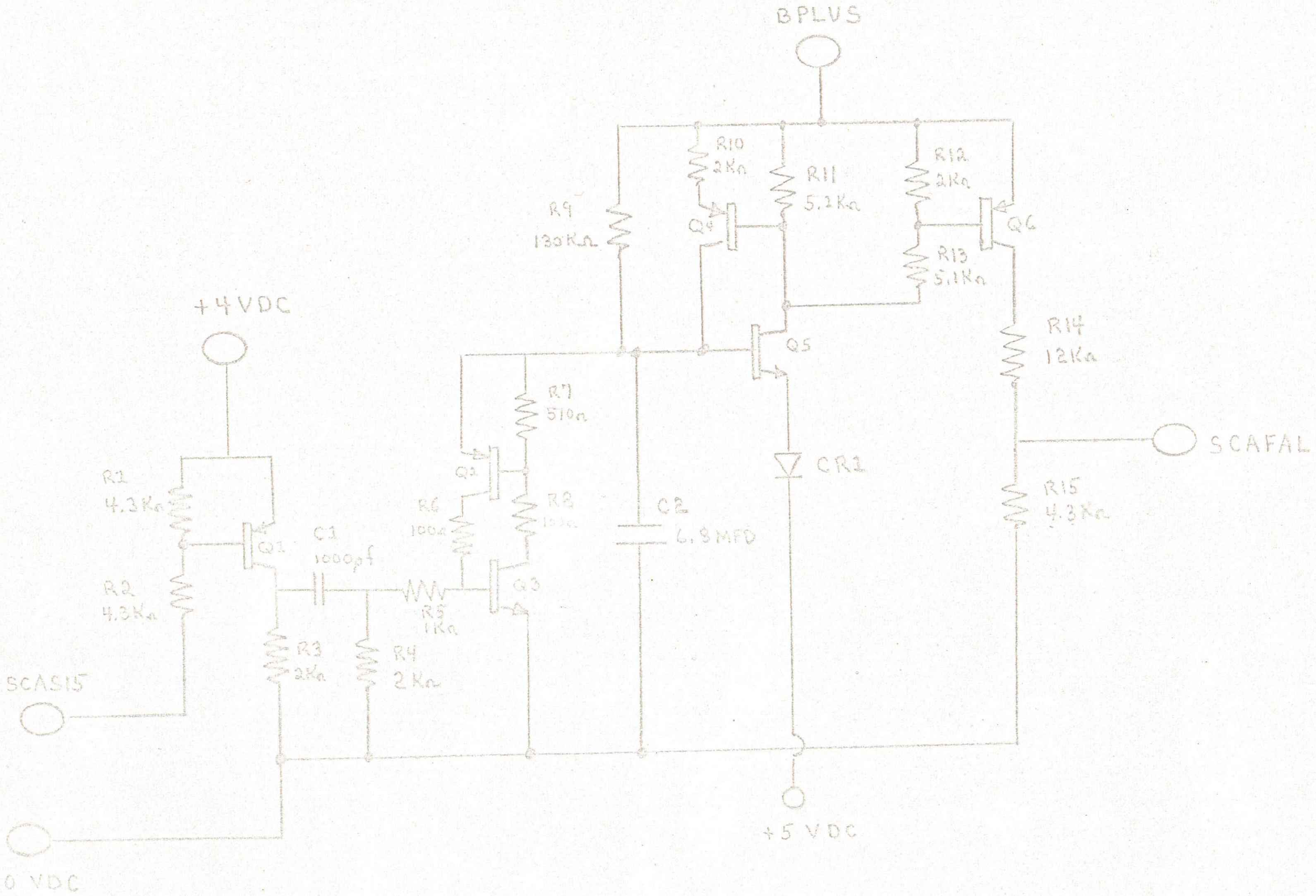

Fig. 3. Scaler Alarm Circuit Diagram.

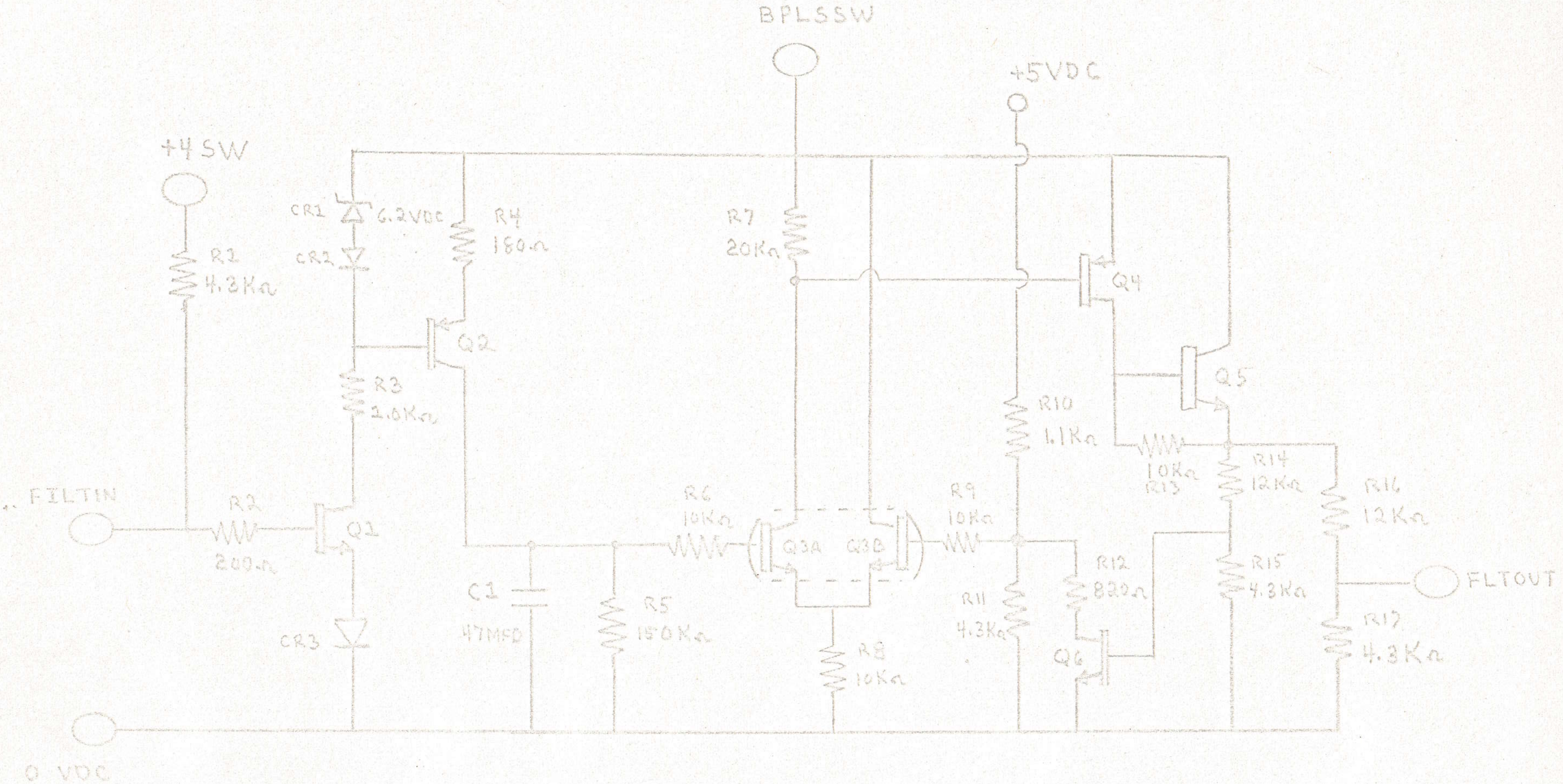

Fig. 4. Warning Integrator Circuit Diagram.