Instrumentation Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Digital Dev. Memo #362

To: Eldon Hall
From: Allen Harano
Date: 1 May 1967
Subj: Restart Monitor (Channel 77 Alarm Box)

A special test connector "Cover" has been fabricated for the Block II AGC. The features included in the "Cover" are: 1) nine flip-flop registers, set by AGC alarms, which can be interrogated as Channel 77 in the computer; 2) loading of all test connector inputs with 270 ohms to ground.

By interrogating Channel 77 after a Restart, the cause of the restart (parity fail, TC trap, etc.) can be determined (similar to observing the alarm panel on the Block I Nav DSKY).

The bit assignments for Channel 77 are as follows:

Bit 1	Parity Fail (E or F Memory)*
Bit 2	Parity Fail E Memory*
Bit 3	TC Trap
Bit 4	Rupt Lock
Bit 5	Night Watchman
Bit 6	Voltage Fail
Bit 7	Counter Fail
Bit 8	Scaler Fail
Bit 9	Scaler Double Frequency Alarm
Bits 10-16	Vacant

It should be noted that alarms contained in Bits 1-6 (and CH33-16) cause a RESTART, and those contained in Bits 7-9 cause an AGC WARNING (CH33-14). (See DDM #260 Rev. B for further details on the alarms.)

Operation of the Restart Monitor is identical to bits 11-16 of Channel 33. Occurrence of an alarm will set a corresponding flip-flop in Channel 77, which can then be interrogated by any of the channel read instructions (and address 77); Channel 77 is cleared by any of the channel write instructions (and address 77).

For present SUNDIAL and AURORA assemblies interrogation is accomplished via V01N10E, 77E, R1 will display Channel 77. To clear the register V21N10E, 77E, 0E is used.

A breadboard "Cover" was fabricated by the System Test Group and a preliminary functional checkout was performed with AGC-200M. A more detailed study of timing margins, etc. will be performed in the D.D. Lab when a computer is available.

The logic flow diagram is contained in MIT Dwg. #139944.

---

*Bit 1 is set by a parity fail in either erasable or fixed memory,
Bit 2 is set only by an erasable memory parity fail. Therefore bits 2,1=01→F memory,
Bits 2,1=11→E memory, Bits 2,1=10 → can't occur.

Dist.

E.C. Hall	R. Alonso	A. Harano	R. Lones -10
A. Hopkins	H. Thaler	H.R. Howie	R. Sheridan
Jim Miller	A. Laats		