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Digital Dev. Memo #382

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Subj: Erasable Memory Preservation - BLock II AGC

There has been some concern about the capability of the Block II AGC to preserve data loaded into its erasable memory when power is turned on and off. To determine if E-memory is indeed preserved during these transients, a test was performed using AGC-C200 in early August.

The test configuration was as follows: Computer subsystem with a breadboard Channel 77 alarm box, Sundial D ropes, K-start tape capability was provided using an Interface Test Console. The sequence of events was as follows:

1. Power is applied.

2. K-start tape is started which clears Channel 77 and then initiates an E-memory program that sum-checks approximately 5/8ths of the memory. This is the portion of E-memory that is not used by the Executive, Waitlist, Pinball, interrupts, etc. and should not change. Upon completion of the sum-check, locations 1366 and 1367 are zeroed and AGC self-check option 4 (Erascheck) is started. (This addresses all but the first 60 erasable locations.)

3. After sufficient delay the K-start tape initiates another program which checks location 1367 to insure Erascheck has completed one cycle. Channel 77 is then interrogated to see if any Parity Alarms have occurred. A program is then started which accesses every location in E-memory.

4. Power is shut off.

5. Steps 1 through 4 are repeated.

The computer was cycled on and off over 10,000 times with no failures occurring. (It appeared that a failure had occurred somewhere between the 6,500th and 8,000th cycle but this was tracked down to the CDU input counters -- each time the computer is powered up the outer and inner gimbal angle counters are decremented by one and the middle gimbal angle counter is incremented by one. After approximately 7000 increments the middle gimbal angle reaches 70° and the gimbal lock lamp is turned on. This also changes the contents of some of the erasable memory that is being sum checked. (It should be noted that this incrementing will depend on the particular gates in each computer and may not occur in some.)

To further verify the results the contents of several registers were compared. These were:

1. REDO Counter -- which counts the number of restarts.

2. Middle gimbal CDU counter -- which was incremented each time the computer was powered up.

3. Location 1300 -- which counted the number of times the E-memory summing program was started (step 2).

4. Location 1301 -- which counted the number of times Erascheck successfully completed one iteration.

5. Locations 1303 through 1307 -- which counted the number of times E bank 3 through E bank 7, respectively, were successfully summed.

Also SFAIL (the number of self-check failures) and location 1302 (which counted the number of parity alarms detected) were still zero.

If any parity alarms occurred before Channel 77 was cleared (step 2) or after Channel 77 was interrogated (step 3) the REDO counter would have contained a larger number than the number of times the E-memory program was started.

It was hoped that several thousand cycles could be run at a low voltage margin but, unfortunately, the tape reader failed causing a termination of the test.

From the results of the test we should be fairly confident that data loaded into E-memory will not be altered during power off.

Although no tests were performed when going into and out of Standby these transients should not cause problems. When going into Standby a logic signal stops computer activity before power is switched (when power is removed, the computer continues to operate until the voltages drop to a predetermined point).

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