Geo. Silver 4

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Digital Dev. Memo #483

To: Eldon Hall
From: Allen Harano
Date: 26 August 1969
Subj: LGC Radar Timing

Due to the large number of questions involving the LGC radar output circuitry, this memo will attempt to summarize all of the known peculiarities of the radar sequence.

The radar sequence is controlled by bits 1-3 of channel 13, which select one of the six parameters to be read from the radars, and bit 4 of channel 13 -- the "activity" bit -- which enables the sequence. Some sequential logic, including a four bit binary counter, is utilized to generate the actual pulse trains.

For normal operation the output waveforms are shown in Figure 1. T1(T3, T4, T5) is a pulse that requests the TIME 1 (TIME3, TIME4, TIME5) counter to be incremented. A simplified logic flow of the circuitry is shown in Figure 2 and a timing diagram of the internal logic is shown in Figure 3. Occurrance of a restart (signal GOJAM) clears channel 13 and resets FF1, FF2, and FF3 but does not reset the four bit binary counter. Thus if a restart occurs during the 80 ms "gate" period the sequence is terminated and no rupt is generated. The next time the activity bit is set the sequence will resume where it was terminated -- not from the beginning of the sequence. For example if the sequence had proceeded 30-40 ms before the restart the four bit binary counter would indicate "4", subsequent setting of the activity bit would increment the counter to 5 and set FF1 enabling "gate" pulses. These pulses would continue for 40 ms until the counter is incremented to "9" when the readout and rupt occur. The data read out of the radar should be half of the normal value since the high speed counter was enabled for only 40 ms, however the radar's shift register may not have been cleared prior to transferring the data and the result could be the logical OR of the first reading (30-40 ms) and the last reading (40 ms).

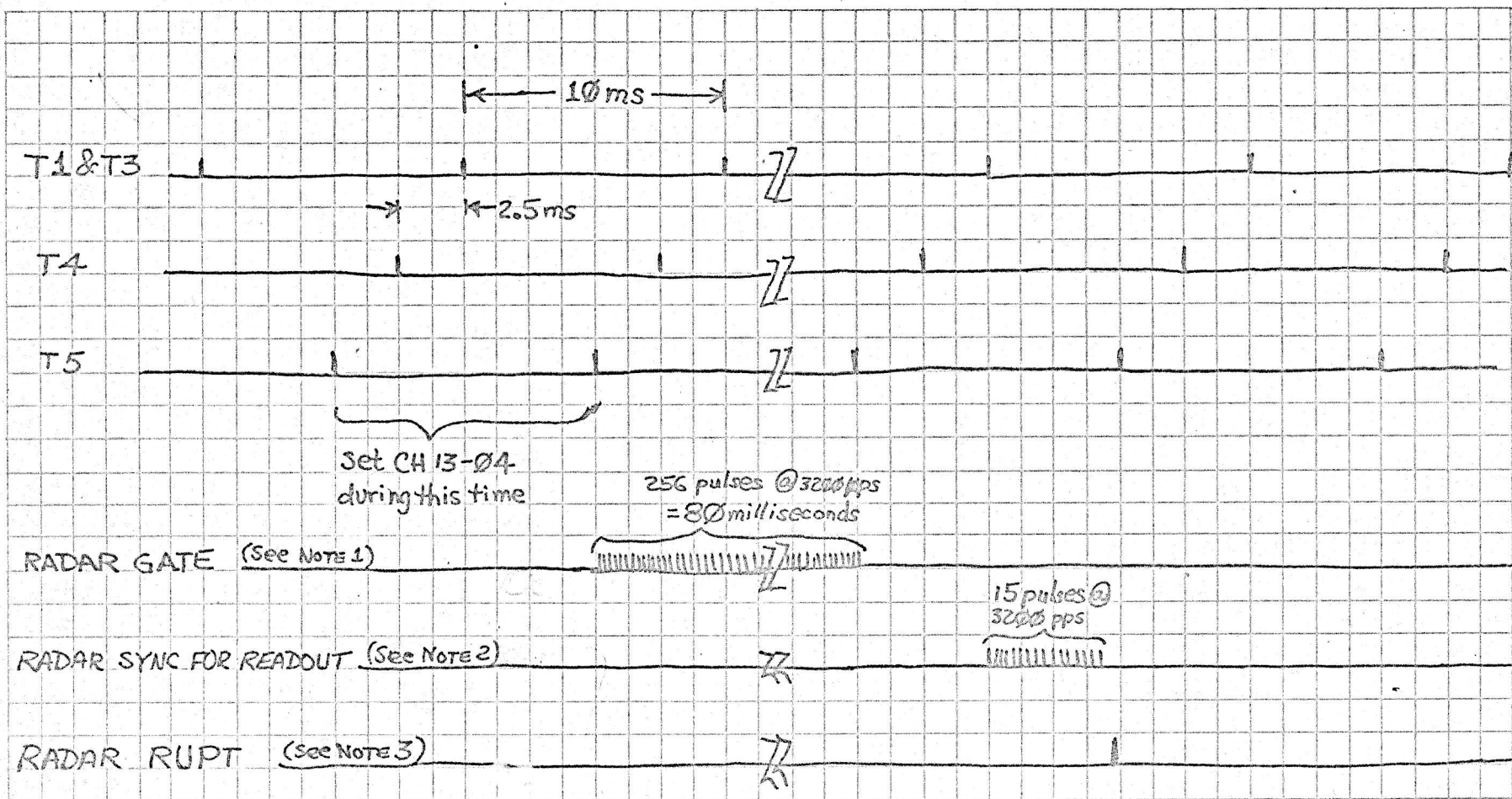
If the restart occurs when the four bit counter is in state "9" channel 13 and FF1 - FF3 are reset as before but within 5 ms signal GTSET will occur setting FF2. This action initiates the 15 pulse readout sequence and then causes a rupt. In this case up to 30 readout pulses could have been sent (0-15 before the restart and 15 after the restart).

When power is first applied to the LGC (or when coming out of STANDBY) the state of the four bit counter is indeterminate and can be any state between "0" and "15". If the state is "9" the 15 pulse readout sequence and rupt will occur as explained in the preceeding paragraph. Any other state will remain until the activity bit is set, causing the counter to increment, modulo 16, until state "9" is reached and a rupt occurs. In this case the first 80 ms "gate" duration can vary between 0 and 140 ms.

If the activity bit is prematurely cleared by the software the four bit counter is subsequently not advanced. If FF1 was set it will remain set resulting in a continuous "gate" pulse train.

A problem of "double pulsing" is analyzed in a memo issued by AC Electronics[1] and is caused by writing into channel 13 during a radar sequence. The problem is due

[1] EM-AGC-0766, T.M. Linden, LM-4 Radar Data Anomalies, 15 May 1969.



NOTES:
1. First "Radar Gate" Pulse Occurs 1/6400 sec after the First T5 after CH13-04 Is Set.
2. First "Radar Sync" Pulse Occurs at T3
3. Radar Rupt Occurs 3/6400 sec before T5. CH13-04 Is Reset By Radar Rupt.
4. T6 pulses are Not Coincident With T3, T4, or T5; → T6 (1600 pps)

FIGURE 1.

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LGC RADAR TIMING

PREPARED BY A. HAZARD

DATE: 1 DEC 1965

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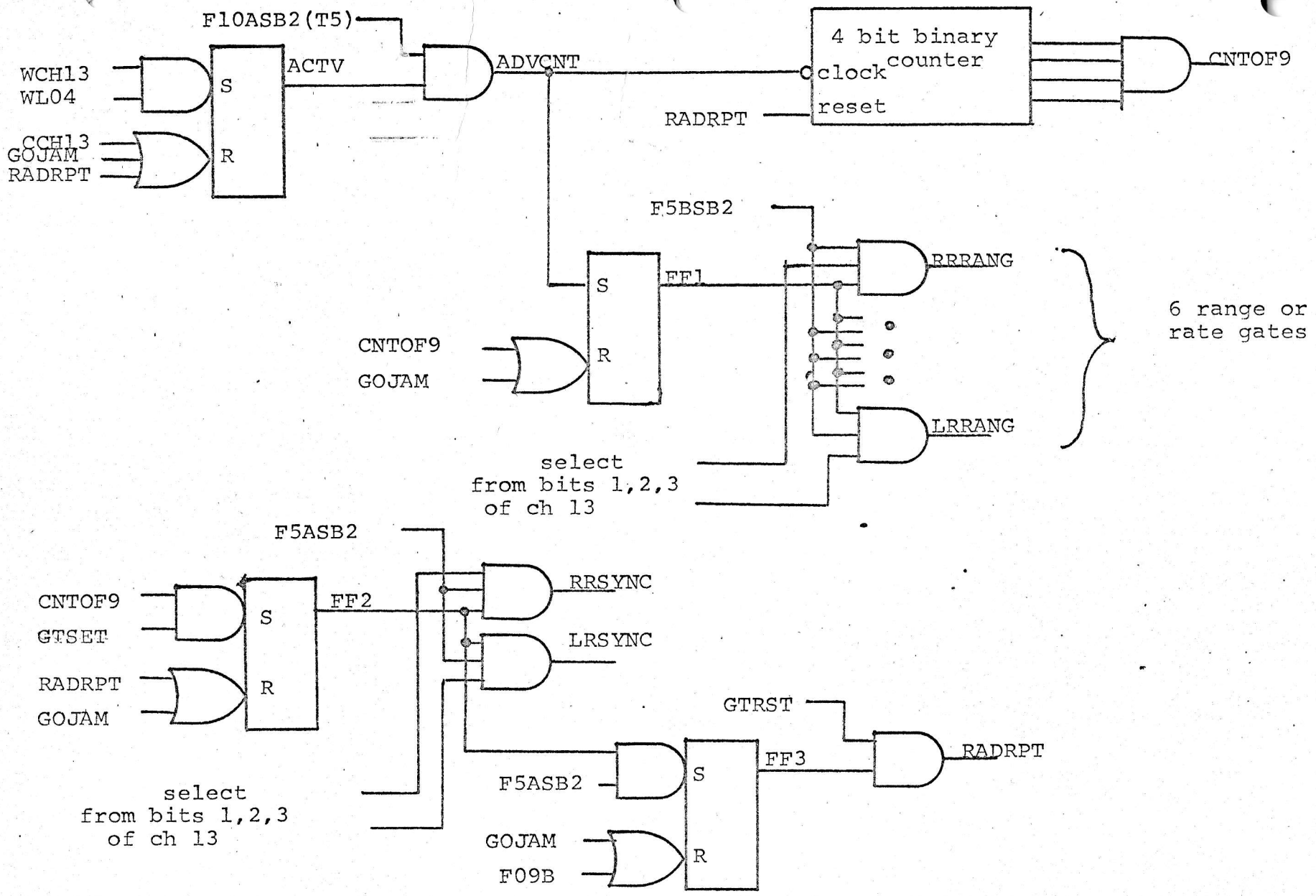
F10ASB2(T5)
WCH13
WL04
S
ACTV
CCH13
GOJAM
RADRPT
R
ADVCNT
4 bit binary counter
clock
reset
RADRPT
CNTOF9
F5BSB2
S
FF1
R
CNTOF9
GOJAM
RRRANG
LRRANG
6 range or rate gates
select from bits 1,2,3 of ch 13
F5ASB2
CNTOF9
GTSET
S
FF2
R
RADRPT
GOJAM
RRSYNC
LRSYNC
GTRST
F5ASB2
S
FF3
R
RADRPT
GOJAM
F09B
select from bits 1,2,3 of ch 13

Figure 2

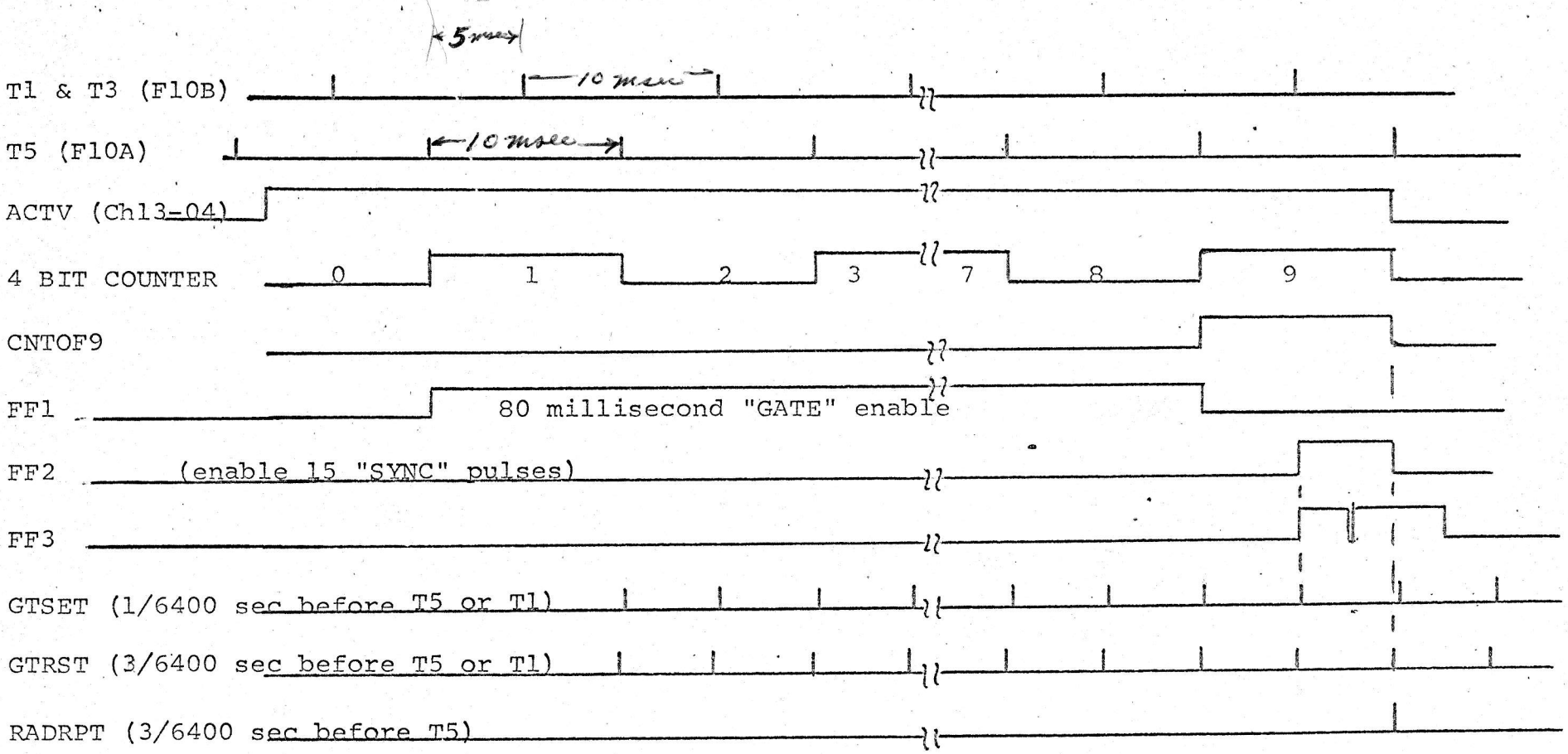
5 msec
10 msec
10 msec
T1 & T3 (F10B)
T5 (F10A)
ACTV (Ch13-04)
4 BIT COUNTER
0
1
2
3
7
8
9
CNTOF9
FF1
80 millisecond "GATE" enable
FF2
(enable 15 "SYNC" pulses)
FF3
GTSET (1/6400 sec before T5 or T1)
GTRST (3/6400 sec before T5 or T1)
RADRPT (3/6400 sec before T5)

Figure 3

TABLE I

RADAR CIRCUIT

CH13-03,02,01	Normal Operation	Remarks
0 0 0	No outputs.	None.
0 0 1	R.R. Range.	250 ns dropout of R.R. Sync for readout can occur if writing into channel 13.
0 1 0	R.R. Range Rate.	250 ns dropout of R.R. Sync for readout can occur if writing into channel 13.
0 1 1	No outputs.	R.R. Sync for readout will occur. 250 ns pulse on R.R. Range and R.R. Range rate, and 250 ns dropout on R.R. Sync can occur if writing into channel 13.
1 0 0	L.R. X Vel.	250 ns dropout on L.R.XVel and L.R. Sync can occur if writing into channel 13.
1 0 1	L.R. Y Vel.	250 ns dropout on L.R. Y Vel and L.R. Sync and a sliver pulse on L.R. X Vel can occur if writing into channel 13.
1 1 0	L.R. Z Vel.	250 ns dropout on L.R. Z Vel and L.R. Sync and a sliver pulse on L.R. X Vel can occur if writing into channel 13.
1 1 1	L.R. Range.	250 ns dropout on L.R. Range and L.R. Sync and a sliver pulse on L.R. X Vel, L.R. Y Vel, and L.R. Z Vel can occur if writing into channel 13.

to the mechanization of the flip-flops associated with channel 13 and related circuitry. The affects of writing into channel 13 during a radar sequence are summarized in Table I.

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Digital Dev. Memo 483 Rev. A

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Date: 28 August 1969
Subj: LGC Radar Timing

Paragraph 4 should be corrected to read as follows:

If the restart occurs when the four bit counter is in state "9" channel 13 and FF1-FF3 are reset as before but within 5 ms signal GTSET will occur setting FF2. This action initiates the 15 pulse readout sequence -- however, since bits 1-3 of channel 13 were cleared by the restart no pulses leave the AGC -- and then causes a rupt. In this case 0 to 15 readout pulses could have been sent.

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George -
I added this
page to the
memo sent to
O'Donnell.
Jim