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Digital Dev. Memo #497

To: Eldon Hall
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Date: 31 Oct. 1969
Subj: Behavior of AGC Counter Registers During Power-Up

The AGC contains several registers, known as counters, used to keep track of various events. These counters are actually specific locations ($0024\text{-}0060_8$) in erasable memory, not flip-flops. Previous investigations[1] have shown that erasable memory is not "disturbed" during power-up/down transients and the counters should not be changed by more than one count (one shift in the case of shift registers). Recently, however, some computers have exhibited the phenomenon of "zeroing" some counters during a power-down - power-up cycle. Investigation into this problem has revealed a mechanism where certain counters may be "zeroed" when power is applied, or the computer is brought from standby to operate. These counters are the "bi-directional" counters (loc $0032\text{-}0046_8$).

A simplified logic flow diagram of a typical "bi-directional" counter cell is shown in Fig. 1 along with some control logic common to all counters. Normal sequencing of a counter increment is as follows: a "plus" ("minus") increment request in the form of an input pulse to the AGC sets FF1 (FF2). At T10 the "OR" of FF1 and FF2 sets FF3, indicating an increment request is present for location xx. The output of FF3 is enabled by the counter cell priority chain when counter xx is the highest priority (smaller values of xx have higher priority). At the beginning of an increment memory cycle (INKL is true) signal CxxA causes address 00xx to be written into the computers address register. Presence of ADDRESSxx enables signal CxxP (CxxM) and at T02 causes flip-flop PINC (MINC) to be set (these flip-flops are PCDU, MCDU in the case of CDU registers, and SHINC, SHANC in the case of shift registers). Signal PINC (MINC) enables the proper adder control pulses to increment (decrement) location 00xx. At T07 of the cycle FF1, FF2 and FF3 are reset, indicating the increment request has been processed.

When power is initially applied FF3 may be in the "set" state, requesting an increment cycle on location xx. If FF1 and FF2 are both "reset", however, neither signal CxxP nor CxxM will occur. Thus flip-flops PINC and MINC will both remain "reset". This absence of information concerning the type of operation to be performed (increment or decrement) results in a result of zero which is written into location xx.

If FF1 or FF2, exclusively, is set, normal incrementing will occur. If FF1 and FF2 are both set the net result will be no change for "1's" complement counters (37-44) decrement for CDU counters (32-36), and shift in a low order "1" for shift counters (45, 46).

The "uni-directional" counters (24-31, 47-60) will not be zeroed by power on transients. A typical counter cell for these registers is shown in Fig. 2. Since the type of increment is known the same signal that supplies the counter address, CmmA, is also used to specify the type of increment (PINC, DINC, or SHINC). Note, however, that an increment cycle will occur if FF3 is "set" during power-on.

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[1] D.D. Memo #382, Erasable Memory Preservation - BL II AGC, 22 August 1967.

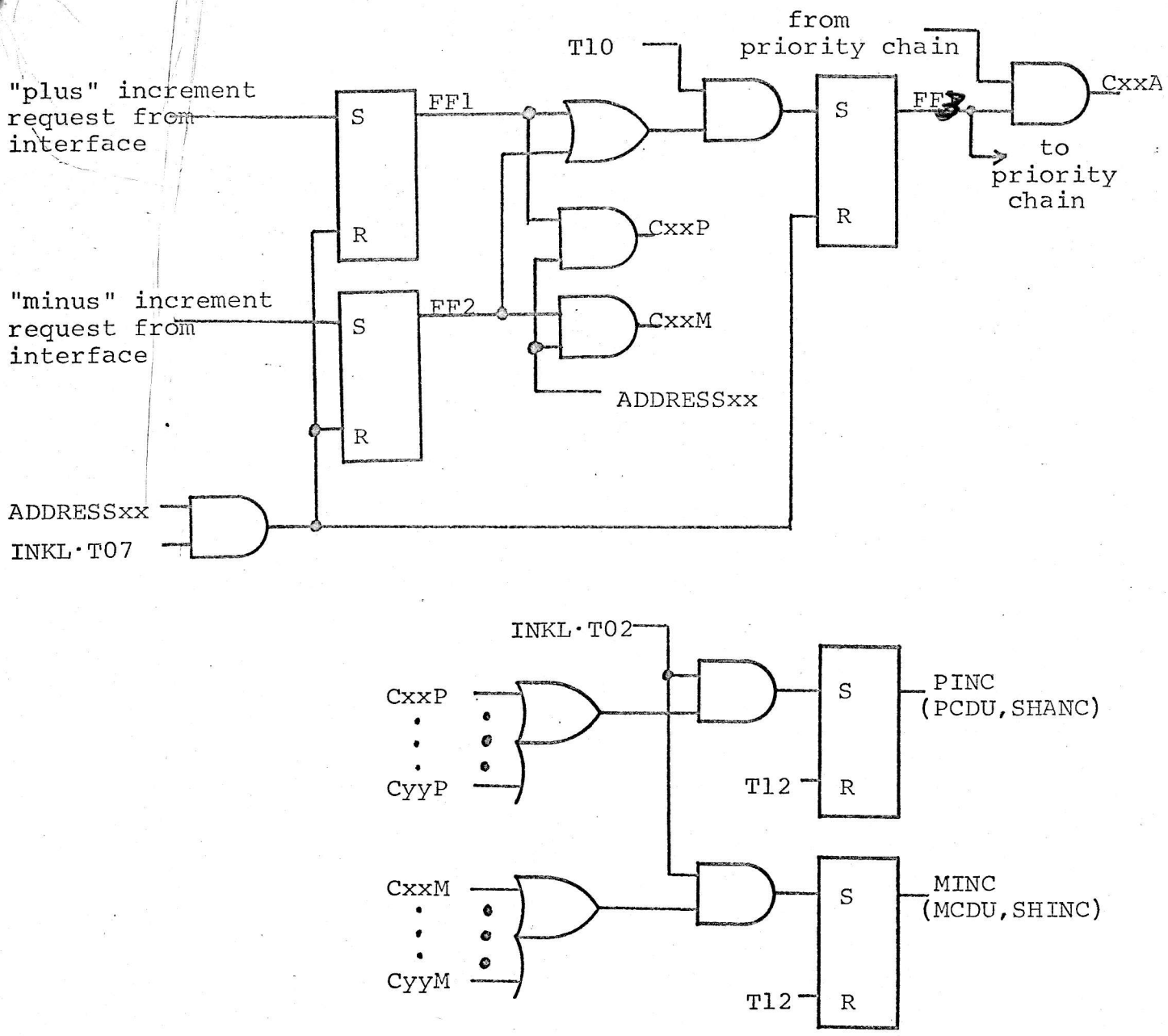

Figure 1. Bi-directional Counter Cell

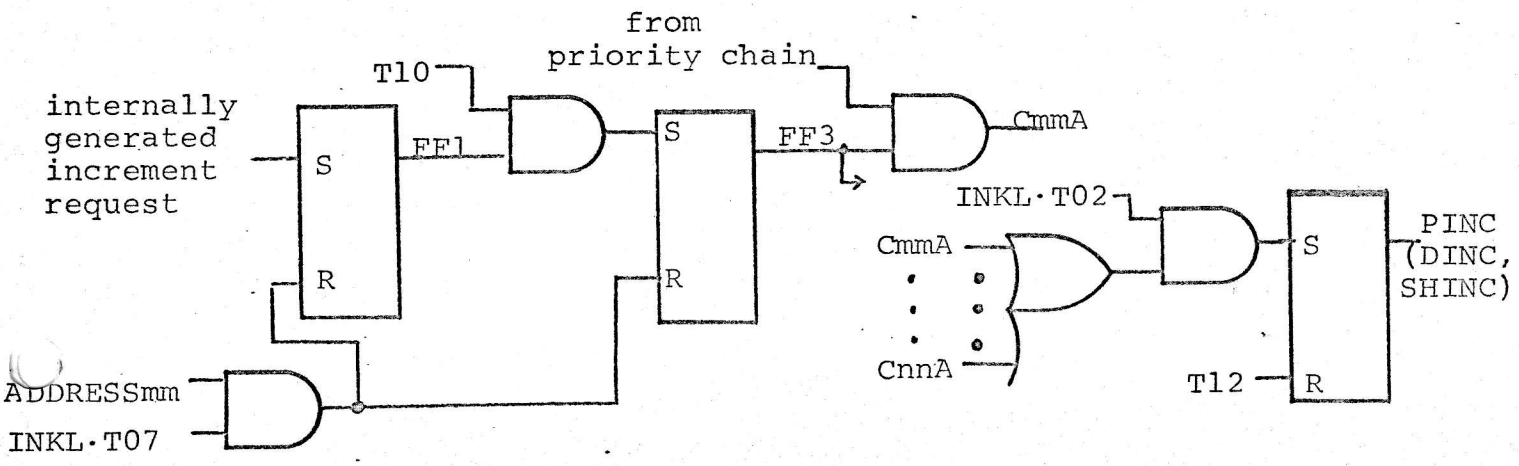

Figure 2. Uni-directional Counter Cell

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