MASSACHUSETTS INSTITUTE OF TECHNOLOGY

APOLLO

GUIDANCE AND NAVIGATION

E-1158

ERASABLE STORE MOD 3C

by

David Shansky

July 1962

MIT INSTRUMENTATION LABORATORY

CAMBRIDGE 39, MASSACHUSETTS

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

APOLLO

GUIDANCE AND NAVIGATION

Approved Eldon C Hall Date 7/17/62

ELDON C. HALL, ASSISTANT DIRECTOR
INSTRUMENTATION LABORATORY

Approved Milton B Trageser Date 7/18/62

MILTON B. TRAGESER, DIRECTOR
APOLLO GUIDANCE AND NAVIGATION PROGRAM

Approved Roger B Woodbury Date 7/19/62

ROGER B. WOODBURY, ASSOCIATE DIRECTOR
INSTRUMENTATION LABORATORY

E-1158

ERASABLE STORE MOD 3C

by

David Shansky

July 1962

MIT INSTRUMENTATION LABORATORY

CAMBRIDGE 39, MASSACHUSETTS

COPY # _____

ACKNOWLEDGEMENT

The advice and active assistance of Dr. Albert Hopkins and Dr. Ramon Alonso during the design, construction and debugging of the memory is gratefully acknowledged. Mr. Samuel T. Scott is to be credited for much of the Sense Amplifier thermal design and for that section of the report dealing with the effect of temperature on amplifier response.

This report was prepared under the auspices of DSR Project 55-191, sponsored by the Manned Spacecraft Center of the National Aeronautics and Space Administration through contract NAS9-153.

E-1158

ERASABLE STORE MOD 3C

ABSTRACT

An erasable ferrite memory consisting of 512 - 16 bit words has been assembled and is being tested in the Mod 3C computer. The memory has been designed for operation from 0^{o} to 100^{o}C. Characteristics of the cores selected and the circuits designed to fulfill this objective are discussed.

by David Shansky

July 1962

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

ERASABLE STORE MOD 3C

Introduction

A Ferrite coincident current memory, consisting of 512 - 16 bit words has been assembled for Mod 3C and is presently being tested.

The ferrite core array itself has been assembled using RCA 233 M1 ferrite cores. These cores produce a nominal 1 output of 50 mv when driven at 800 MAT at 25°C. Wiring in the array itself was specified to minimize the physical size of the memory and the number of permissible joints. The wiring of the X and Y selection axes is continuous, breaks being allowed only for the purpose of replacing cores which were found defective in test. The total size of the experiment array is approximately 1.25" x 2.25" x 1.25" exclusive of solder lugs. The memory itself has been operated over the temperature range -55°C to + 300°C with variable drive currents. The coefficient of coercive force vs. temperature, in the range 0°C to + 100°C is approximately -0.3%/°C. Figures 1 and 2 are photographs of the memory. Photographs of the output waveforms for a worst word pattern and a numerical summary of the entire stack are included in Appendix I. These waveforms were obtained by cycling the memory through all addresses with the memory storing a pattern which produces the worst disturb noises on the sense winding. The drive currents were held constant at $I_X = I_Y = I_Z = 400$ ma. The temperature was allowed to vary over a 100°C temperature interval.

One of the basic objectives of this design was to render the performance of the memory insensitive to temperature. This

has involved the design of current drivers whose temperature characteristic matched the particular core (memory cell) characteristic, and the design of sense amplifiers whose sensing threshold is a defined function of temperature, program and supply voltage. The characteristics of these building blocks will be discussed in more detail later in this report.

Address Selection

The address selection system discussed in MIT Instrumentation Laboratory Reports E-1074 (Erasable Ferrite Memory - Mod 3C Computer) was breadboarded and subsequently abandoned because of poor performance at the low-voltage operating margin (6 v). A transistor diode line selector, which performs well within the power supply excursion that the remainder of the computer must tolerate, is the present choice. In reference to Fig. 3, a simplified schematic of one element of the address selection system, it will be noted that line selection in the memory is performed in two steps. The output of the Erasable Memory Address Register (SS) is decoded to select two out of ten transistors represented in the Y dimension of memory Fig. 4, or two out of twelve transistors in the X dimension of memory Fig. 5. These four transistors are saturated by ACLE. CL FER ϕ_{123} is activated causing a current I_A to flow through winding W_1, switching core #1 to the 1 state. Transistor Q1 is saturated for a time determined by $t = \frac{n\Delta I}{V_{EB_{(SAT)}}} \cong 3\ \mu$sec. In a similar fashion, an additional current source I_A which is activated by CL FER $_{123}$ drives current through W_3 of switch core #2 saturating Q3 for the same length of time. Current source I_M is activated at Q2 and the current produced here is steered through only one memory line in the proper direction via Q1 and Q3. It should be noted that the address of the word that has been interrogated has effectively been stored in the cores which are a part of the steering mechanism, thus permitting a change in the state of the Memory Address

Register (SS), after the Read portion of the cycle has been completed.

During the Write portion of the cycle; another current source WFER$\mathcal{I}_{234}$ is activated clearing all of the cores in the selection system to the 0 state. The cores switch in a time determined again by $t = \frac{n \mathcal{I}}{V_{EB(SAT)}}$, saturating Q2 and Q4. Current source I_M is again activated and current is now steered in a direction opposite to the Read direction through the previously selected memory line.

Appropriate delays are provided between the selection of a steering core and the activation of the memory current source I_M to insure proper current steering in the presence of spurious coupling (noise) in the address selection cores. The Clear pulses supplied to these cores during Write time are adjusted in length so that the cores which have been addressed during Read time are completely switched during the Write portion of the cycle.

Driver Circuits

All of the various current sources used in the memory are characterized by their insensitivity to most of the transistor parameters and to power supply environment. They all have the same temperature coefficient, namely approximately 0.3%/^{o}C of the nominal room temperature value of current.

Referring to either the drawing of the Current Regulator, Fig. 6, or the Inhibit Driver, Fig. 7, one may observe that both of these consist of two similar circuits, one of which drives the other. Both of these circuits are current sources and each current source may be analysed in the following fashion. Consider the current source consisting of Diode D1, D2, D3, the 2N1410 and the 20Ω resistor. For a given collector current, the base-emitter voltage drop (V_{be}) may be assumed constant. Hence a constant voltage will appear across the 20Ω resistor, producing a constant emitter current. The collector will be equal to αI_e or approx-

imately 98% of the emitter current. The various semiconductor voltage drops will vary as a function of temperature giving rise to a change in current as a function of temperature. A curve of $I_c = f(t)$ may be seen by referring to Fig. 8. The switching performance of the combination of the memory core and the driver over a $100^{o}F$ temperature interval is shown in Fig. 9. It can be seen from this figure that there is no appreciable change in switching time, but there is an appreciable change in flux. The ceramicists at RCA are presently investigating the modification of the ferrite material to cure this condition. However, it should be noted that the material in its present condition is usable. (This will become obvious when the sense amplifier is discussed.)

Cascading two current sources, as is done in both the X and Y Regulator and the Inhibit Driver, has the effect of improving the performance of the current source by virtue of the diode current being held more constant. Rise time of the collector current is controlled by the addition of an inductance. The following equation describes the behavior of the emitter current.

$$I_e = \frac{V_{diode} - V_{be} + SL}{R}$$

The collector current is simply

$$I_c = \alpha I_e$$

This current will be independent of collector supply voltage as long as the transistor (s) is unsaturated. In saturation, the current will be determined by the supply voltage, the emitter resistance, and the saturation resistance of the transistor.

It will be noted from an inspection of the current source schematics that a number of silicon diodes are apparently redundant. These diodes were furnished to simplify packaging in Mod 3C, and coincidently enhance reliability.

Sense Amplifiers

The sense amplifiers for the Mod 3C memory accept signals from either the fixed (Rope) memory or the erasable (Ferrite) memory. It must be able to reject large amplitude (~ 1 v) common mode noise and amplify and rectify a core output signal of the order of 50 mv nominal in the presense of 10 mv of difference mode noise. The amplifier chosen for this application may be seen in Fig. 10. A differential amplifier Q1 and Q2, whose input is terminated by a network equal to the sense winding characteristic impedance, is the first stage of this amplifier. A current source, similar to the type previously described in the section dealing with the driver circuits, takes the place of the usual emitter resistor. This current establishes a constant voltage drop across the collector load resistors. The resistors used for emitter degeneration guarantee equal voltage drops at the collectors. Positive signals are OR'D together into the base of Q3 via diodes D1 and D2. The emitter of Q3 is held at a constant reference voltage (V_Y) with respect to ground. This voltage is adjusted to provide a threshold for noise rejection and signal acceptance. When the base-emitter junction of Q3 is forward biased, the transistor saturates, causing base current to flow in Q4. The collector of Q4 drives a standard Latch input equipped with an inhibiting gate. This gate is normally inhibited except during Read time to prevent spurious setting of the latches which constitute the Memory Output Register.

A special voltage source , Fig. 11, is furnished to drive the V_X and V_Y inputs. This voltage source has been designed to insure proper temperature tracking of the Difference Amplifier Collector rest potential and the threshold of conduction of Q3 in addition to compensating for the changes in voltage across the diodes and transistors as a function of temperature.

Temperature Effects On 3C Erasable Memory Sense Amplifiers

The temperature compensation scheme used for the 3C Erasable Memory Sense Amplifier depends on the similarity and linearity of forward biased semiconductor junction voltage variations with temperature. It has been established elsewhere that such junction voltage drops are matched and vary linearity to within about 10% for similarly produced units. The temperature compensation to be described is valid only for the case where all critical junctions are operating in the same temperature environment.

An experimental analysis and some conclusions that may be drawn which tend to demonstrate the applicability of the sense amplifier to a wide temperature environment are as follows.

Experimental Results

Figure 12 is a graph showing the temperature dependence required of V_Y to maintain a temperature independent voltage threshold (1's signal). The linearity of this graph demonstrates the feasability of using a temperature varying voltage source to control the sensing threshold. The voltage source shown in Fig. 11 has two controls. R_1 sets the voltage V_Y and thus the sensing threshold. R_2 sets the change in V_Y with power supply voltage and thus adjusts sensing threshold for variations in power supply voltage. The incremental output impedance is about 3-5Ω and thus the voltage source can be common to all the sense amplifiers.

Figure 13 is a graph showing variation of sense threshold and V_Y with temperature. Figure 14 shows the temperature dependence of the temperature compensated sense amplifier. For estimating worst cases and also for designing temperature dependent thresholds, it is useful to compute two parameters from the data.

Let V_T = voltage input threshold. Then $V_T = V_T\ (V_Y,\ T)$

$$\frac{dV_T}{dT} = \left.\frac{\partial V_T}{\partial T}\right|_{V_Y = \text{const.}} \left(+\frac{\partial V_Y}{\partial T}\right)\left(\frac{\partial V_T}{\partial V_Y}\right)_{T = \text{const.}}$$

Since the graphs are linear, $\left(\frac{\partial V_T}{\partial T}\right)_{V_Y}$ and $\left(\frac{\partial V_T}{\partial V_Y}\right)_T$ are constants and may be evaluated at any V_Y and T from the graphs. From Fig. 2, we have:

$$\frac{dV_T}{dT} = 0.31\ \frac{9}{5} = \left(\frac{\partial V_T}{\partial T}\right)_{V_Y} - 15 \times \frac{9}{5}\left(\frac{\partial V_T}{\partial V_Y}\right)_T$$

From Fig. 3:

$$\frac{dV_T}{dT} = 0 = \left(\frac{\partial V_T}{\partial T}\right)_{V_Y} - 7\ \left(\frac{\partial V_T}{\partial V_Y}\right)_T$$

Solving, we have

$$\left(\frac{\partial V_T}{\partial T}\right)_{V_Y} = -\ 0.196\ \text{mv}/^{\circ}\text{C}$$

$$\left(\frac{\partial V_T}{\partial V_Y}\right)_T = -\ 0.028 \approx \frac{1}{G_D}$$

Where G_D is the voltage gain of the differential amplifier.

Conclusions

When the differential voltage gains of all the sense amplifiers are matched at the operating point, it can be expected that a worst case mismatch in temperature coefficients of the sense amplifiers will be about 10% of

$$\left(\frac{\partial V_T}{\partial T} \right)_{V_Y}$$

or about 0.02 mv/^{o}C. Thus, temperature variations in sensing thresholds can be held to about 2 mv over a range of 100^{o}C. Other effects, such as variation of threshold with power supply voltage, mismatch in G_D, etc. give an estimated maximum combined mismatch of perhaps 8 to 10 mv over the total range of power supply voltage and temperature. Since all of these effects are independent of the threshold selected, we can operate at a threshold 1 of 50 mv with a signal to noise ratio as low as 2:1 and a variability of 20% in the sizes of ones and zeros. For smaller ampitude inputs these margins would be reduced.

Further Work

Roger Lamson has recently shown that the total flux switched by a ferrite core has a large negative temperature dependence. Since in a coincident current memory it is necessary to have the drive currents track with H_c, this means that the voltage input to the sense amplifier will decrease with temperature. Preliminary data for the ferrite cores used in 3C show a linear temperature dependence that is

$$E_{out} = 72 - 0.45T \text{ mv}$$

T measured in ^{o}C

This data is over the range from 27°C to 90°C. Compensation for this effect would have to be done in the sense amplifier since drive current tracks with H_c. A linear temperature compensation with V_Y would require that

$$\frac{dV_T}{dT} = -0.45 = -0.196 - 0.028 \frac{\partial V_Y}{\partial T}$$

or

$$\frac{\partial V_Y}{\partial T} = +9 \text{ mv}/^{\circ}\text{C}$$

The circuit shown in Fig. 11 is incapable of producing a V_Y with a positive temperature coefficient, therefore a different type of circuit would have to be used. Since a 5 v zener diode has a very small temperature coefficient, a circuit like that in Fig. 15 could be used. Actual design will be done after the ferrite characteristics are more certainly established.

At present the sense amplifiers in computer 3C are being used for both the rope memory and the erasable memory with transformers being used to match and isolate inputs. The rope cores produce outputs which are nominally about 2 μsec wide vs. 0.6 μsec for the ferrite memory. For the same probability of sensing a 1, it is necessary to apply a smaller nominal input from the rope cores, because of the sense amplifier's frequency response characteristic. Since the rope drivers have a linear negative temperature coefficient and since $\frac{\partial E}{\partial I} = \frac{\phi}{S}$ (where ϕ and S are characteristics of the tape wound cores) it is possible to achieve a temperature varying output from the rope cores which matches the temperature tracking of the sense amplifier. This will be done for the 3C computer.

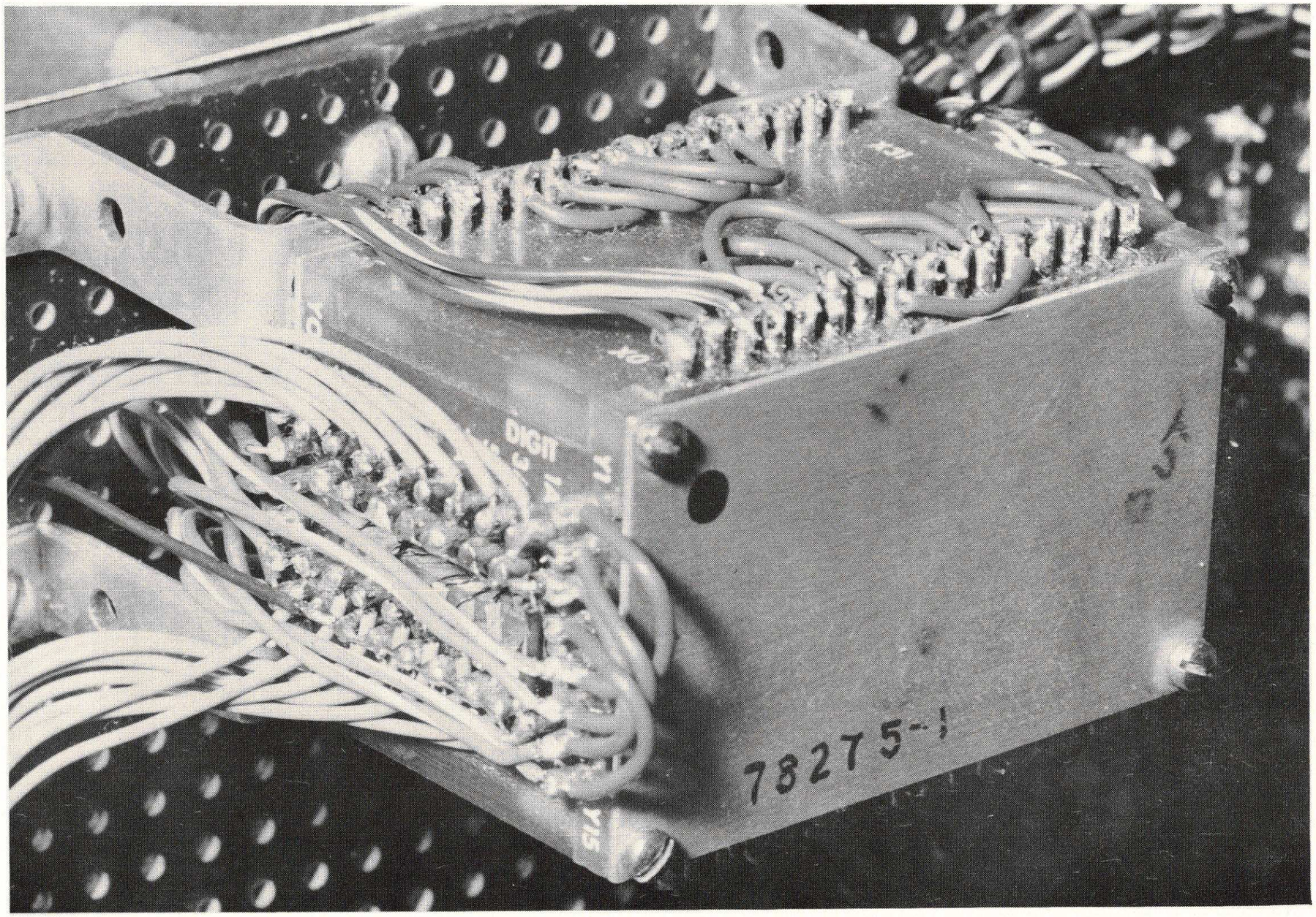


Fig. 1 The 512 word ferrite memory

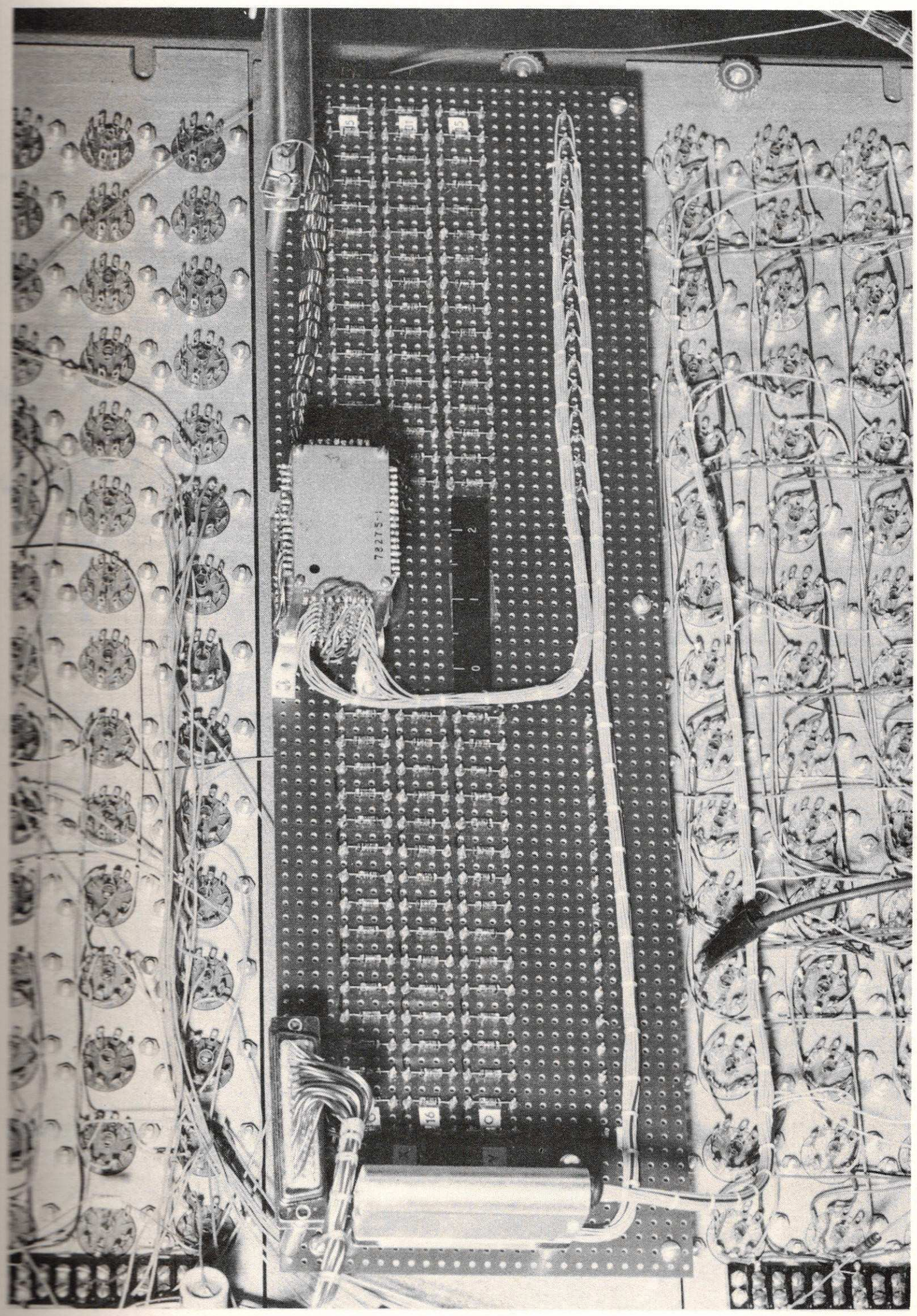


Fig. 2 The 512 word memory and selection electronics

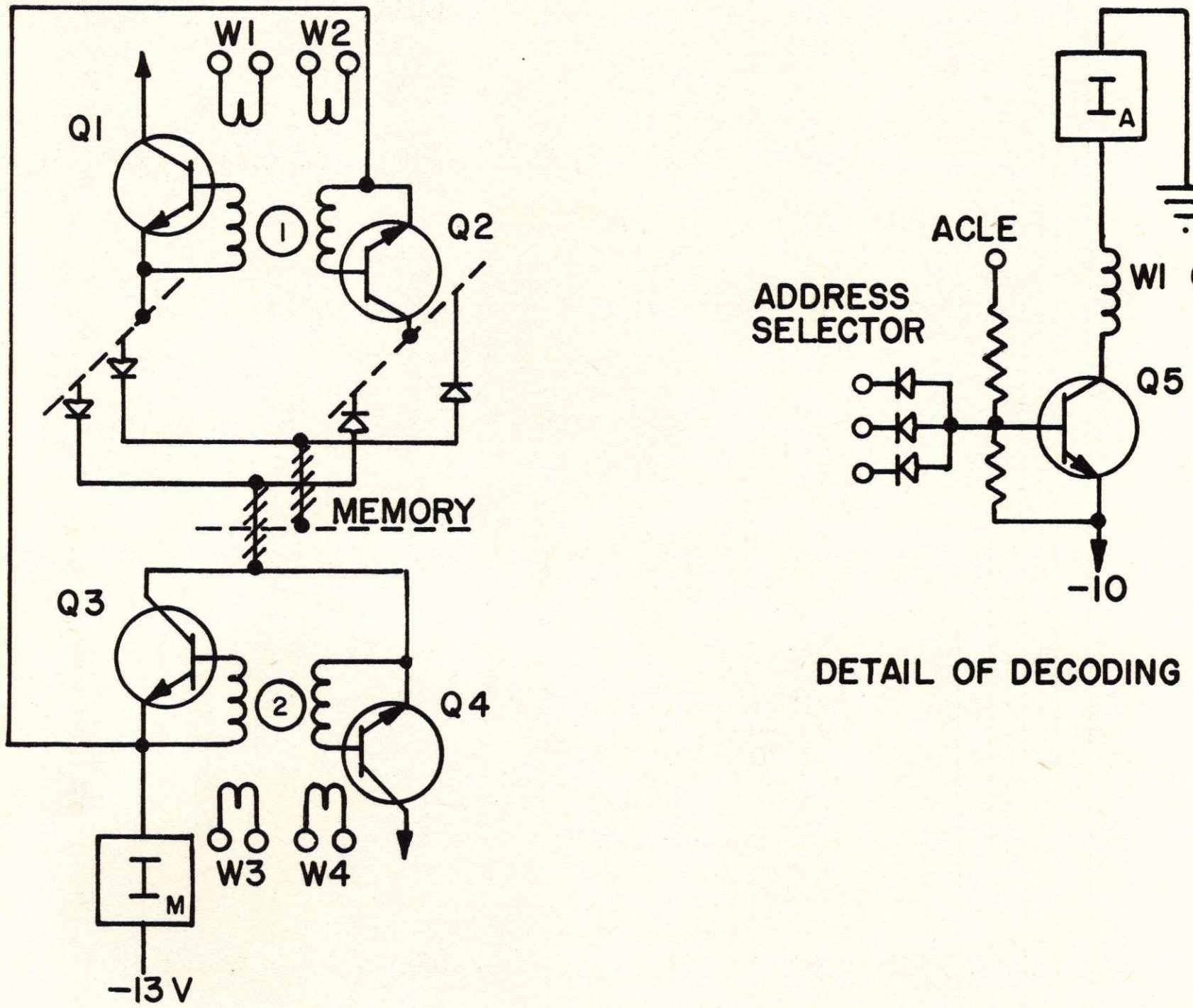
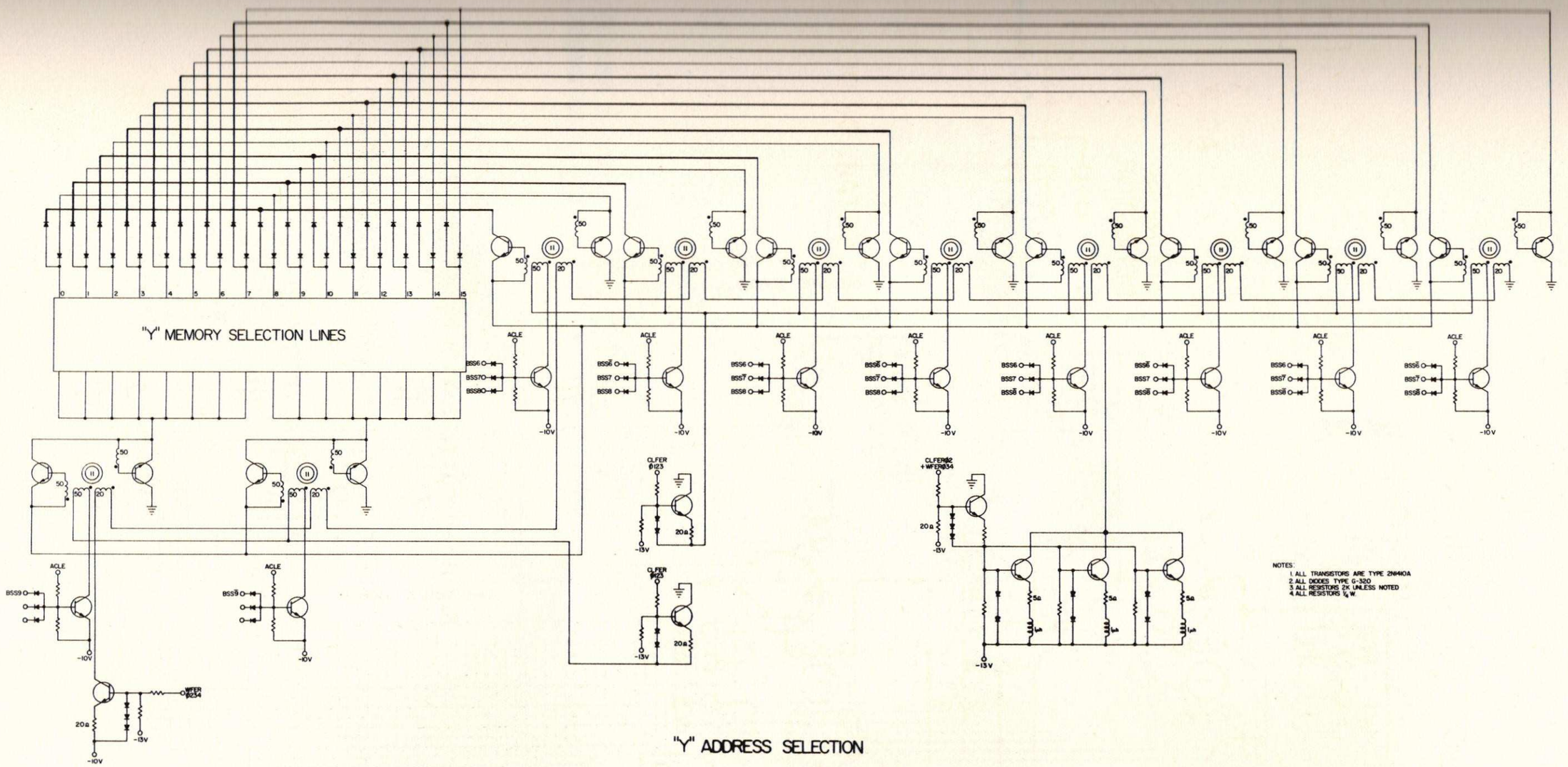


Fig. 3 Memory current steering simplified schematic



"Y" ADDRESS SELECTION

Fig. 4 The Y address selection

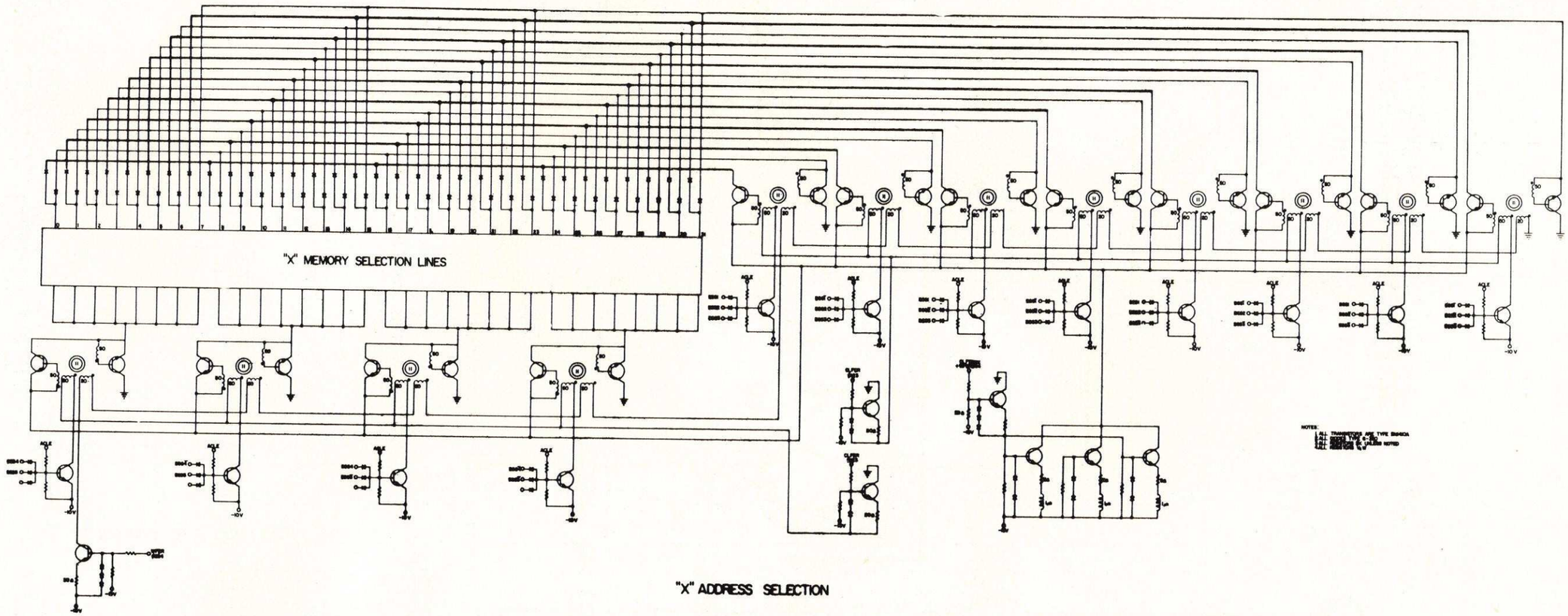


Fig. 5 The X address selection

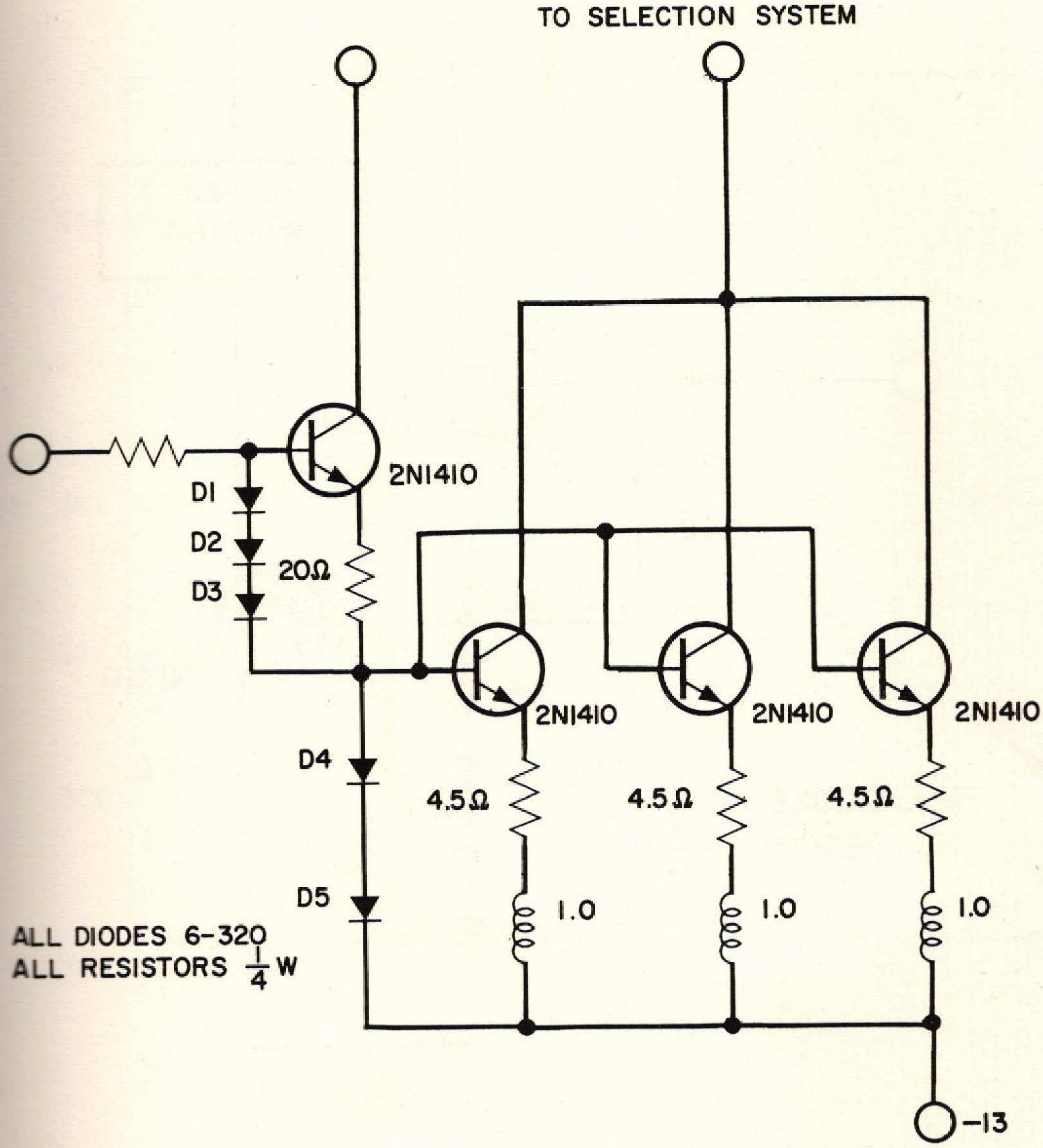


Fig. 6 Current regulator (X and Y axes)

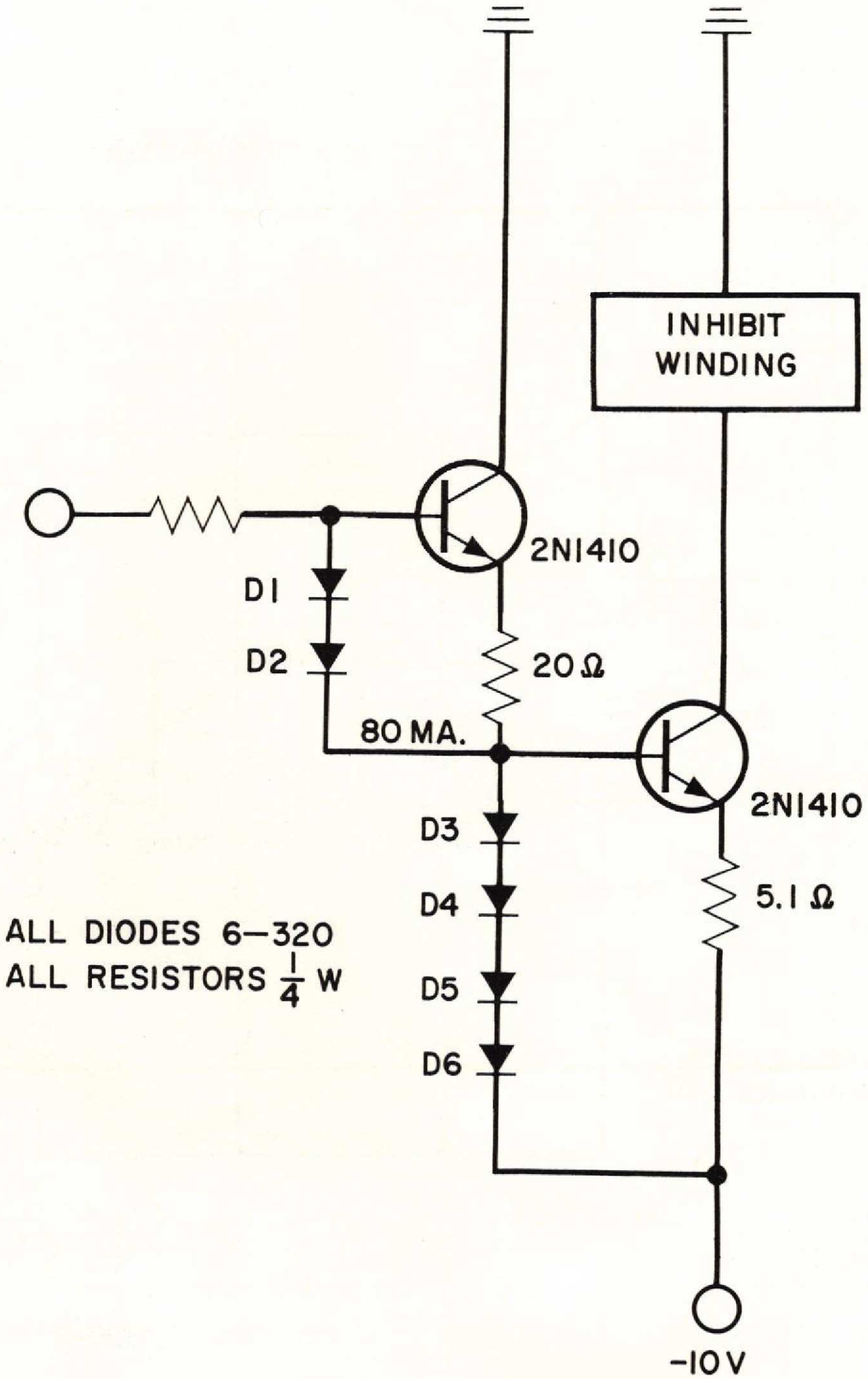


Fig. 7 Inhibit driver (Z plane)

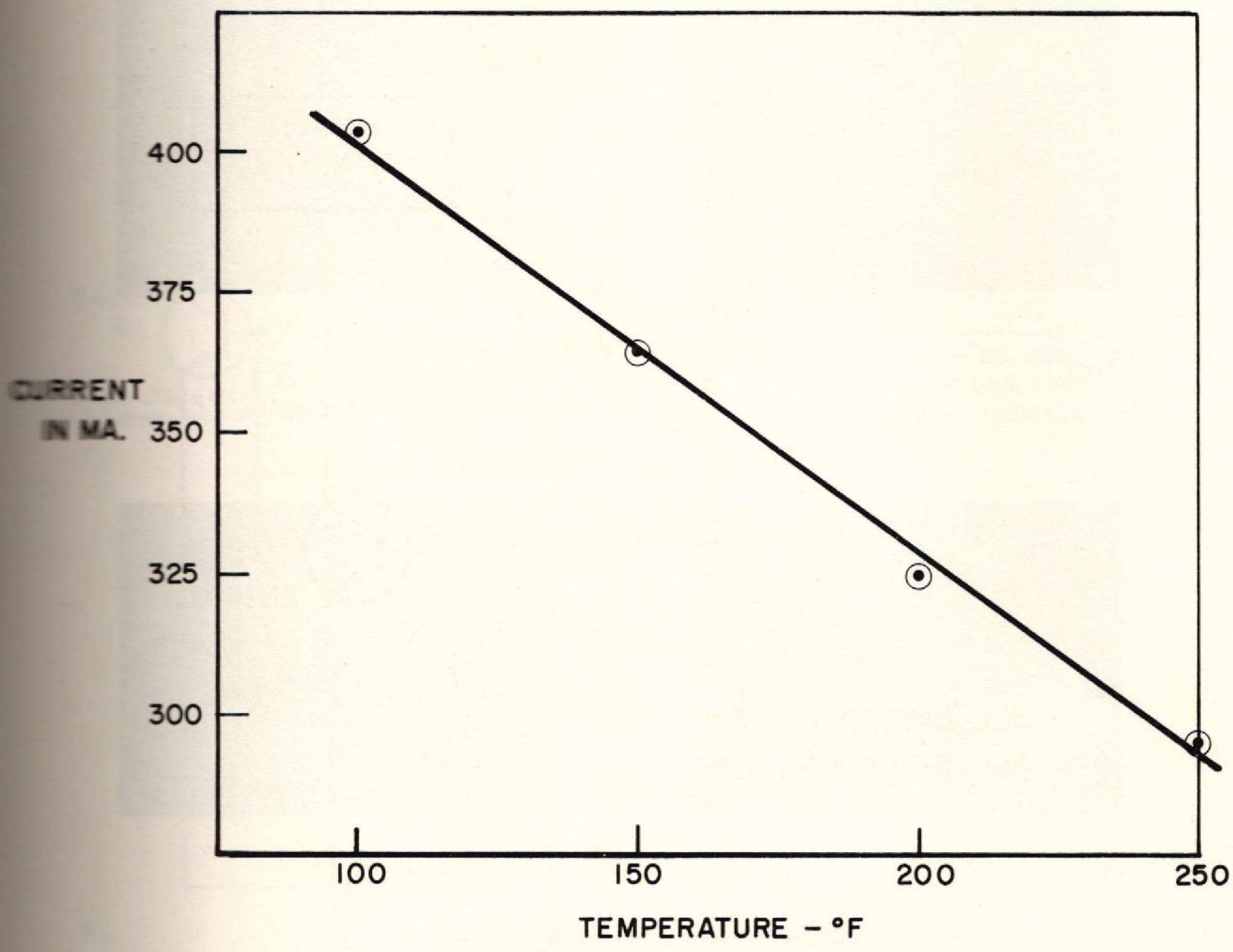
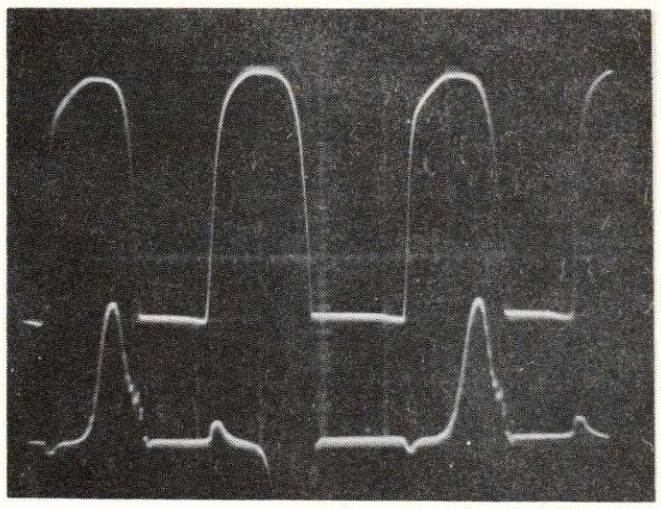
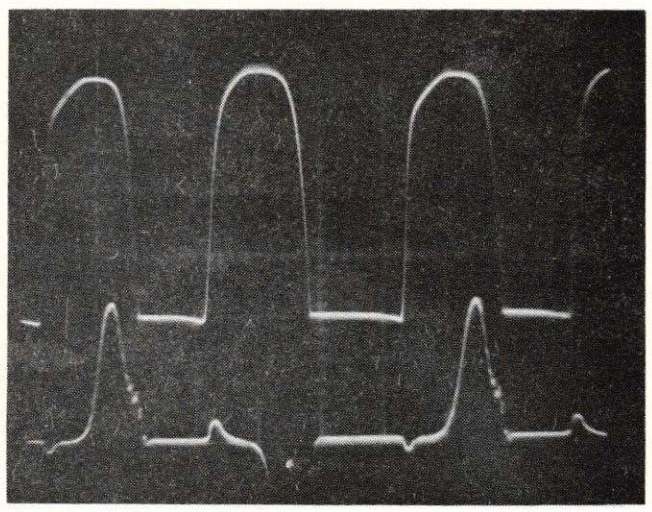


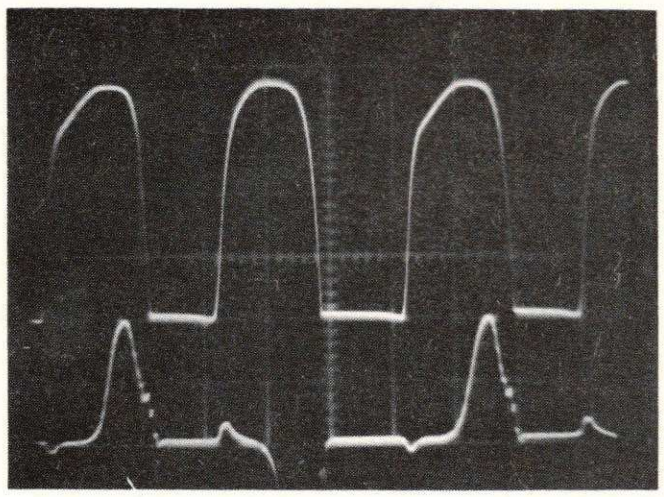
Fig. 8 I=f (t), current regulator



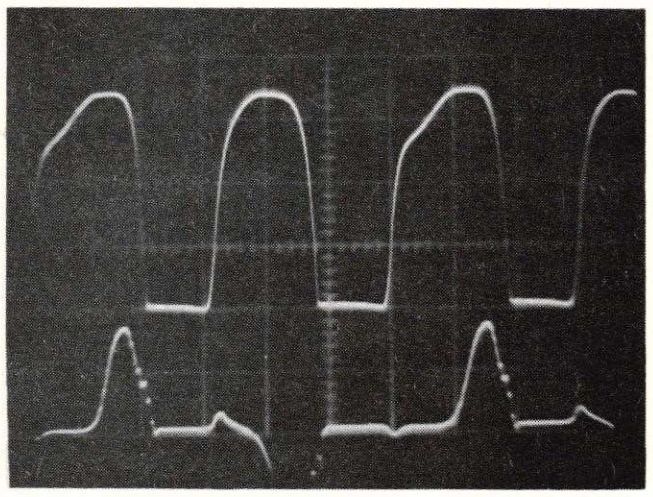
a) TEMP. 80°F
TOP: .050 VOLTS/CM
BOTTOM: 100 MA/CM
} X 1 μSEC/CM



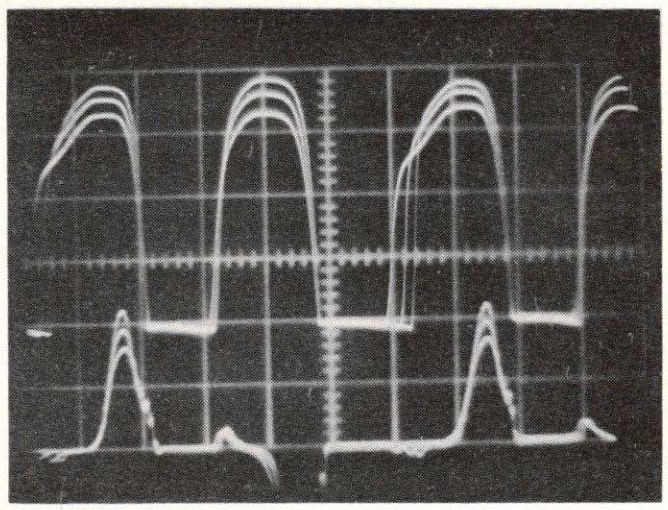
b) TEMP. 100°F
TOP: .050 VOLT/CM
BOTTOM: 100 MA/CM
} X 1 μSEC/CM



c) TEMP. 150°F

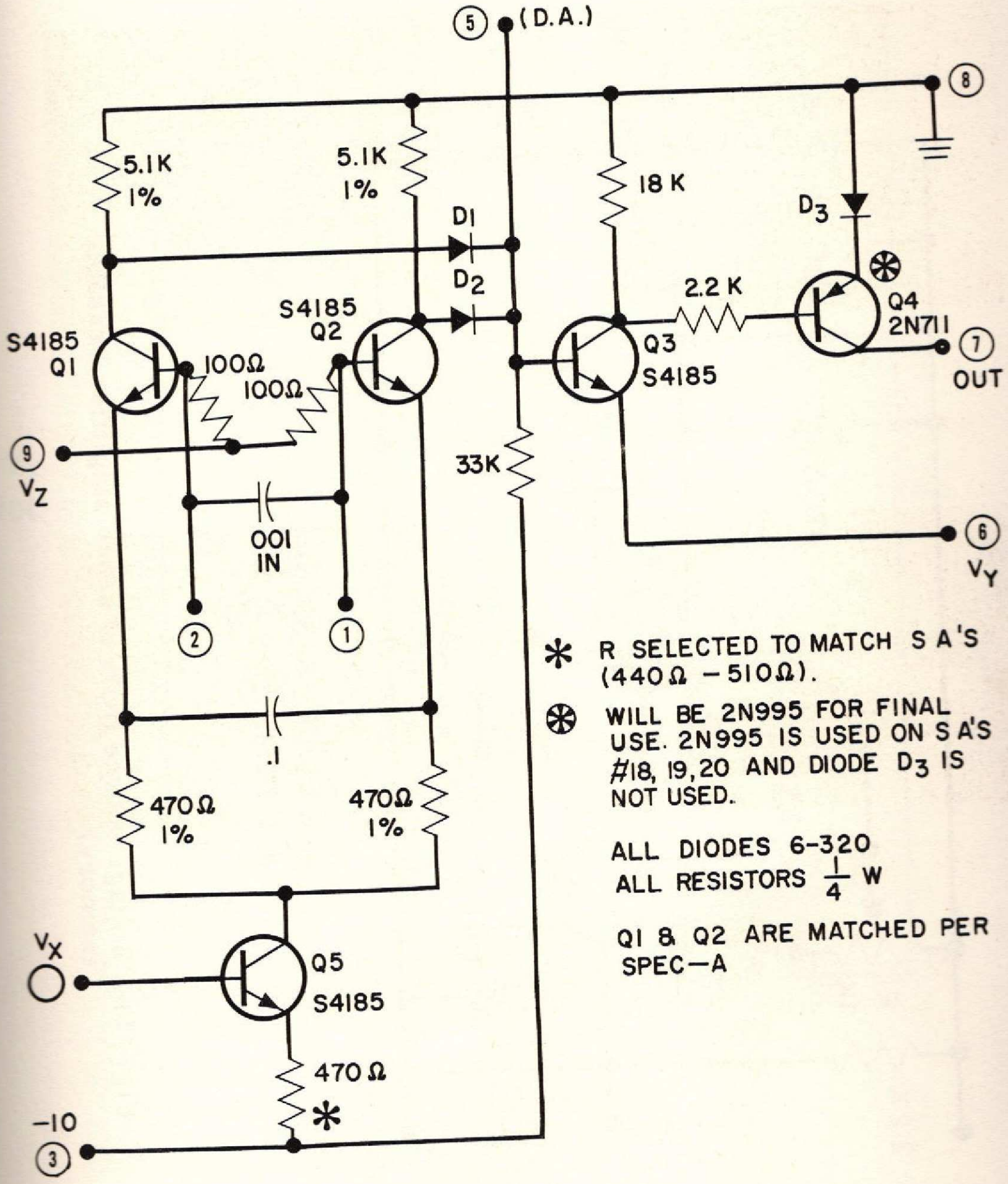


d) TEMP. 200°F.



e) 200°F, 150°F, 100°F

Fig. 9 **Combination of ferrite core and driver, illustrating constant T_S**



* R SELECTED TO MATCH S A'S (440Ω – 510Ω).

⊛ WILL BE 2N995 FOR FINAL USE. 2N995 IS USED ON S A'S #18, 19, 20 AND DIODE D_3 IS NOT USED.

ALL DIODES 6-320
ALL RESISTORS $\frac{1}{4}$ W

Q1 & Q2 ARE MATCHED PER SPEC–A

Fig. 10 Sense amplifier erasable memory

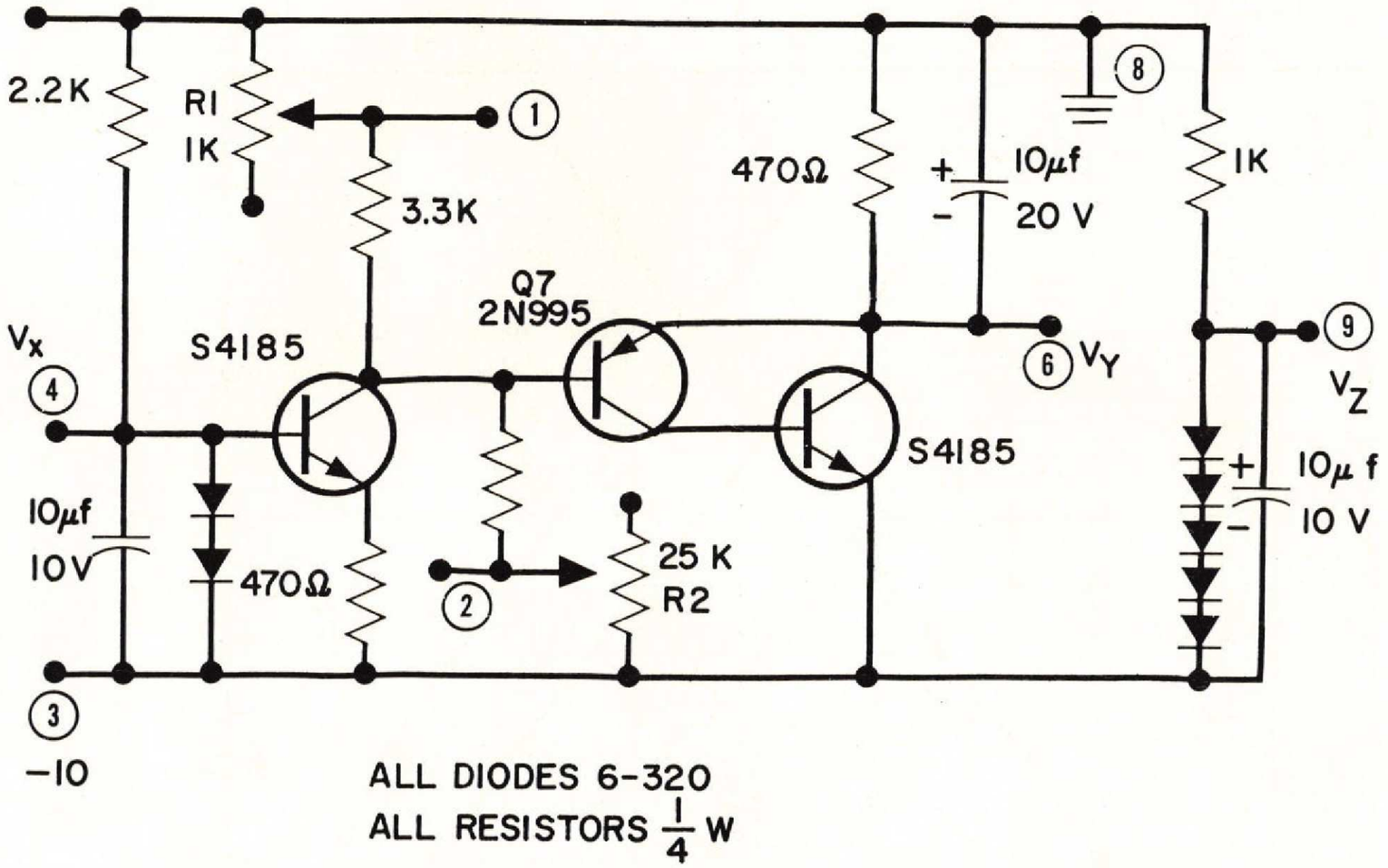


Fig. 11 Voltage source (part of sense amplifier erasable memory)

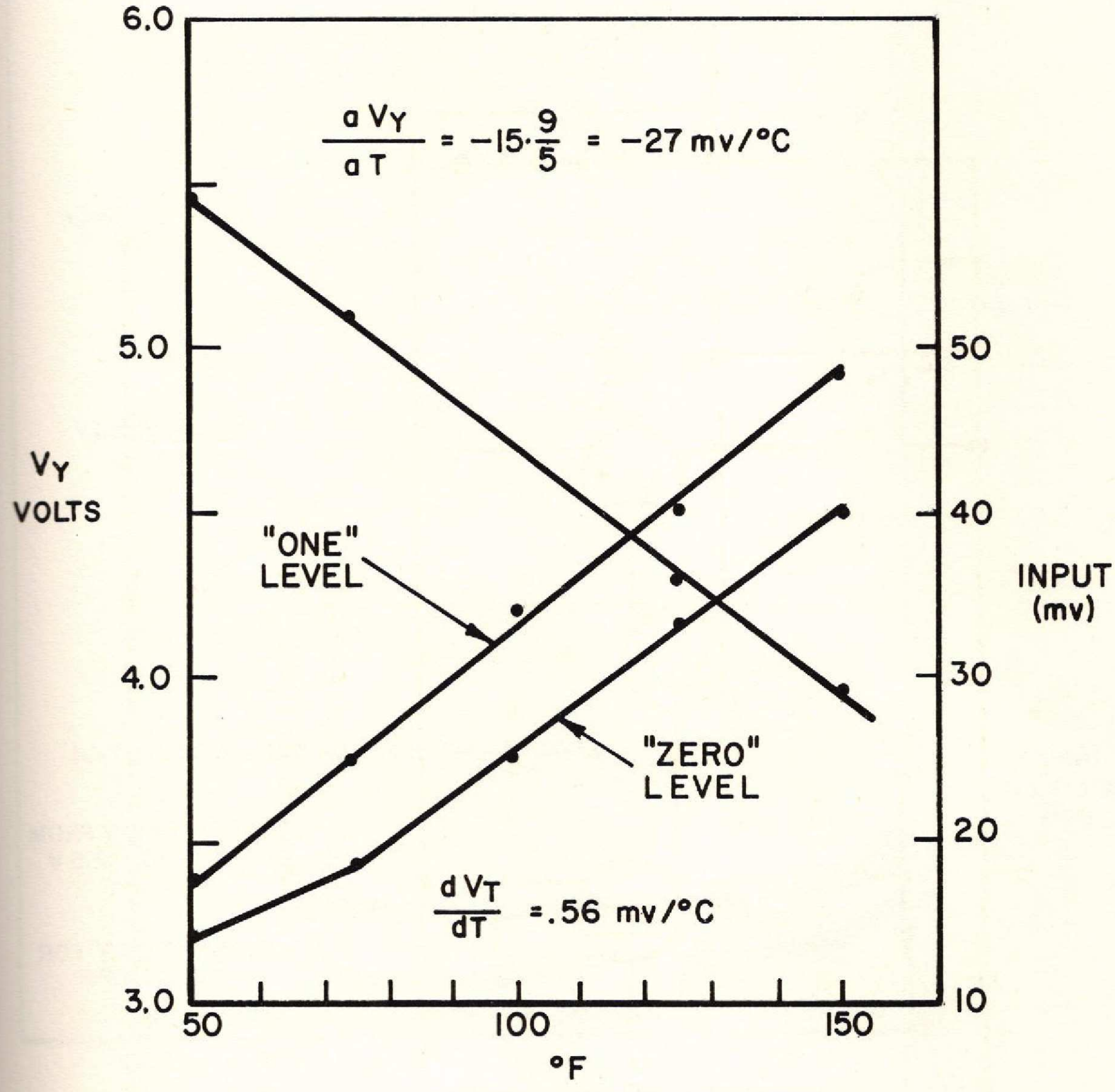


Fig. 12 Initial data with wrong temperature compensation

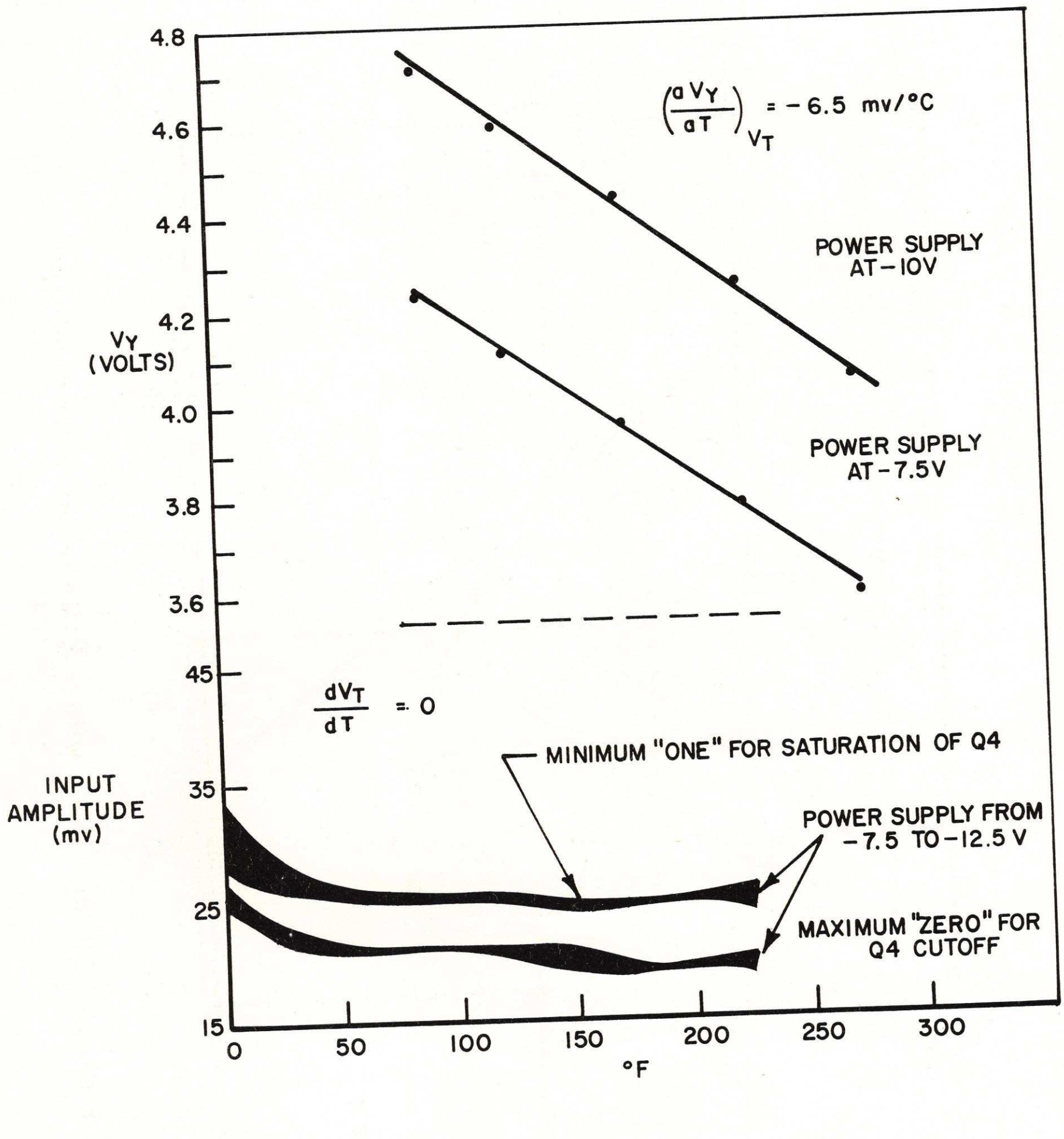


Fig. 13 Variation of sense threshold and V_Y with temperature

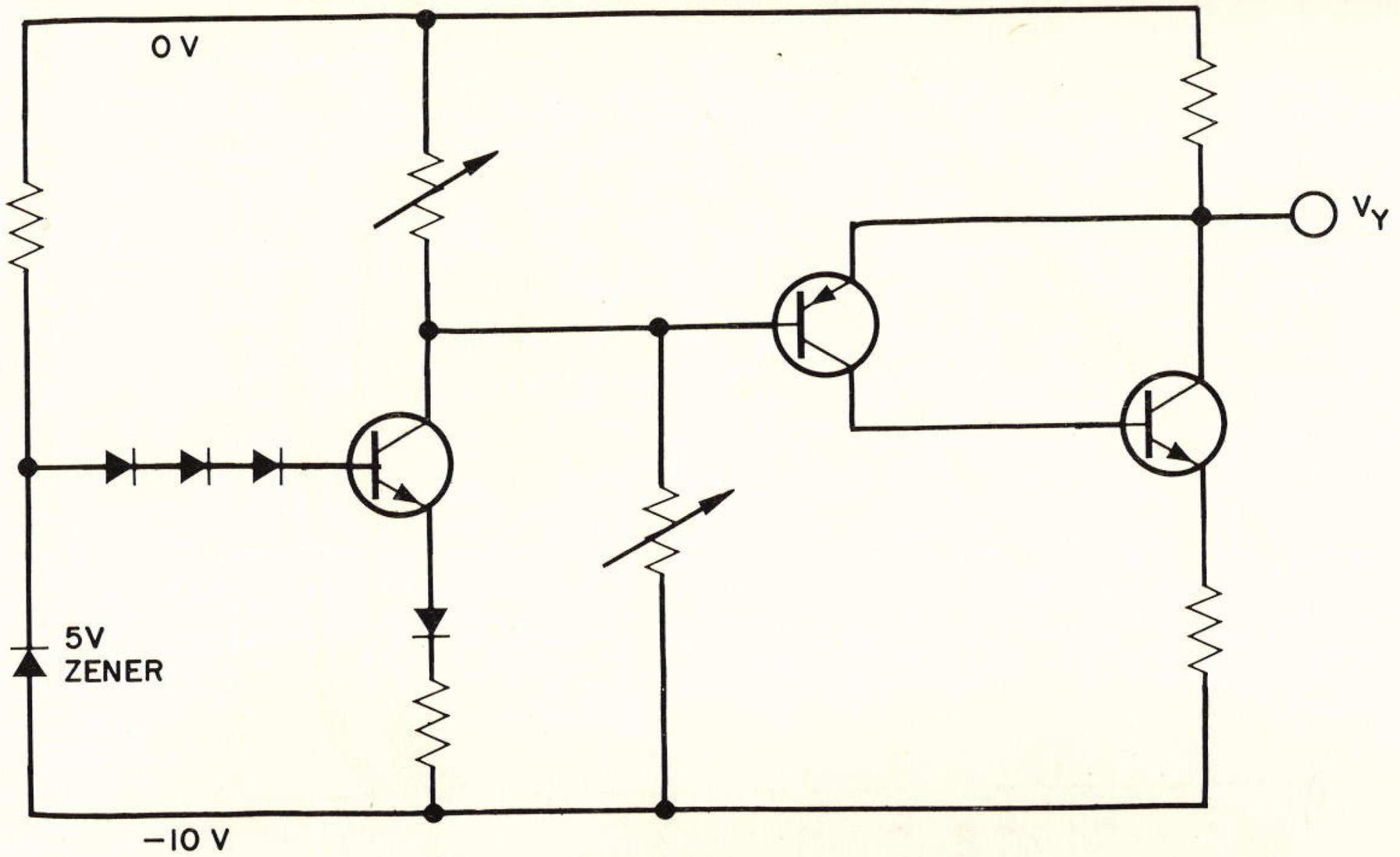


Fig. 15 Circuit for V_Y with positive temperature coefficient

Appendix I

HIGH DENSITY STACK 32 × 16 × 16

233M 1

$I_r/_2 = I_w/_2$ = Inhibit = 400 ma

T_r = 0.5 μsecs T_d = 3 μsec (50-50)

Temperature = 100°C

Plane #	uV_1 (mv)	Plane Noise (mv)	T_p (μsec)	T_s (μsec)
1	60 - 90	8	0.92 - 1.00	1.42 - 1.58
	60 - 90	8	0.94 - 1.00	1.44 - 1.56
2	60 - 88	7	0.94 - 1.00	1.46 - 1.56
	60 - 88	9	0.88 - 1.00	1.46 - 1.60
3	60 - 92	8	0.92 - 0.98	1.44 - 1.56
	64 - 90	8	0.92 - 0.98	1.44 - 1.56
4	60 - 90	8	0.92 - 0.98	1.46 - 1.58
	60 - 88	7	0.92 - 0.98	1.44 - 1.56
5	56 - 88	8	0.94 - 1.00	1.44 - 1.60
	56 - 88	8	0.94 - 1.00	1.44 - 1.56
6	60 - 92	8	0.92 - 0.98	1.46 - 1.58
	58 - 90	8	0.92 - 0.98	1.44 - 1.56
7	56 - 94	7	0.92 - 1.00	1.44 - 1.56
	62 - 96	8	0.94 - 1.00	1.44 - 1.56
8	64 - 94	8	0.90 - 0.98	1.44 - 1.58
	58 - 90	8	0.94 - 1.00	1.46 - 1.60
9	56 - 90	8	0.94 - 1.00	1.46 - 1.58
	52 - 88	7	0.92 - 1.00	1.44 - 1.60
10	62 - 90	8	0.94 - 0.98	1.46 - 1.56
	60 - 88	8	0.92 - 1.00	1.46 - 1.56
11	60 - 88	8	0.92 - 1.00	1.44 - 1.56
	56 - 90	8	0.92 - 1.00	1.46 - 1.58
12	60 - 88	8	0.88 - 1.00	1.50 - 1.66
	58 - 88	8	0.90 - 1.00	1.44 - 1.62
13	60 - 80	9	0.94 - 1.00	1.48 - 1.64
	58 - 80	9	0.92 - 1.00	1.48 - 1.60
14	60 - 88	8	0.92 - 0.98	1.44 - 1.56
	56 - 88	8	0.92 - 1.00	1.44 - 1.56
15	58 - 80	9	0.92 - 1.00	1.48 - 1.62
	60 - 80	9	0.92 - 1.00	1.48 - 1.64
16	60 - 84	9	0.92 - 0.98	1.48 - 1.64
	60 - 80	9	0.92 - 1.00	1.44 - 1.62

HIGH DENSITY STACK 32 × 16 × 16

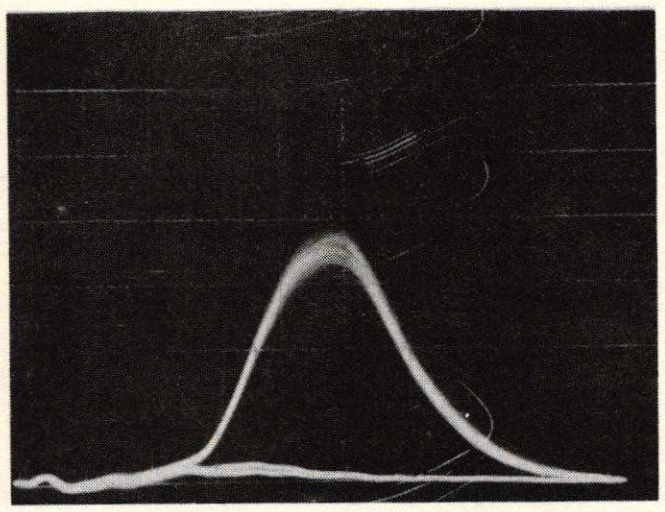
233M1 Cores

$I_r/2 = I_w/2$ = Inhibit = 400 ma

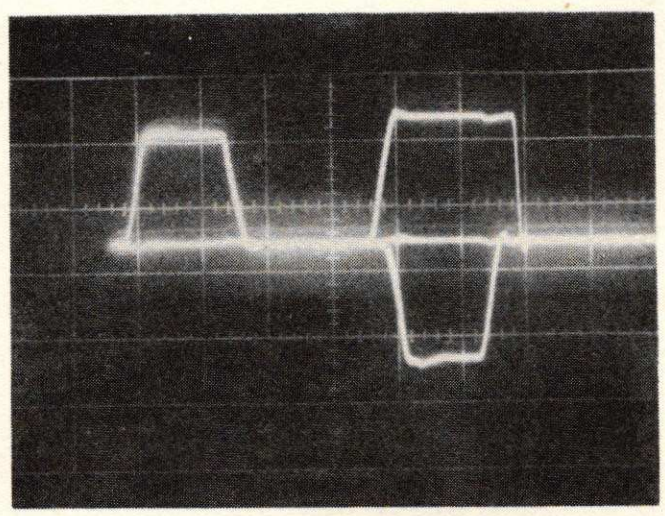
T_r = 0.5 μsec T_d = 3 μsec (50 -50)

Temperature = 0°C

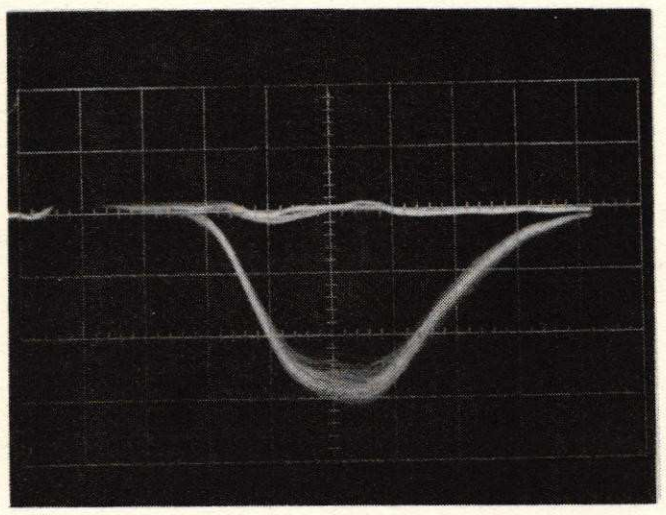
Plane #	uV_1 (mv)	Plane Noise (mv)	T_p (μsec)	T_s (μsec)
1	56 - 80	6	0.92 - 0.98	1.38 - 1.48
	56 - 80	6	0.92 - 0.98	1.40 - 1.48
2	56 - 80	6	0.94 - 1.00	1.36 - 1.50
	54 - 80	6	0.94 - 0.98	1.36 - 1.48
3	52 - 82	6	0.94 - 0.98	1.36 - 1.48
	56 - 80	6	0.94 - 0.98	1.36 - 1.48
4	52 - 88	6	0.96 - 0.98	1.36 - 1.48
	54 - 80	6	0.94 - 0.98	1.36 - 1.50
5	52 - 80	9	0.94 - 0.98	1.36 - 1.48
	52 - 80	6	0.92 - 0.98	1.38 - 1.50
6	56 - 80	9	0.94 - 0.98	1.36 - 1.48
	52 - 80	6	0.96 - 0.98	1.36 - 1.50
7	52 - 84	8	0.94 - 0.98	1.36 - 1.48
	52 - 84	6	0.94 - 0.98	1.36 - 1.50
8	52 - 84	8	0.94 - 0.98	1.36 - 1.48
	56 - 84	6	0.94 - 0.98	1.36 - 1.48
9	54 - 82	7	0.94 - 0.98	1.36 - 1.48
	50 - 80	6	0.94 - 0.98	1.36 - 1.48
10	56 - 80	6	0.94 - 0.98	1.36 - 1.48
	52 - 76	6	0.94 - 0.98	1.36 - 1.50
11	54 - 80	6	0.96 - 0.98	1.36 - 1.48
	50 - 78	6	0.94 - 0.98	1.36 - 1.50
12	48 - 72	6	0.94 - 0.98	1.36 - 1.48
	48 - 80	6	0.90 - 0.98	1.36 - 1.50
13	48 - 72	6	0.90 - 0.98	1.36 - 1.48
	48 - 72	6	0.94 - 0.98	1.36 - 1.50
14	56 - 80	6	0.94 - 0.98	1.36 - 1.50
	50 - 80	6	0.96 - 0.98	1.36 - 1.50
15	46 - 78	6	0.92 - 0.98	1.36 - 1.48
	46 - 78	6	0.88 - 0.96	1.36 - 1.50
16	48 - 78	6	0.90 - 0.96	1.36 - 1.50
	48 - 64	6	0.92 - 0.96	1.36 - 1.50



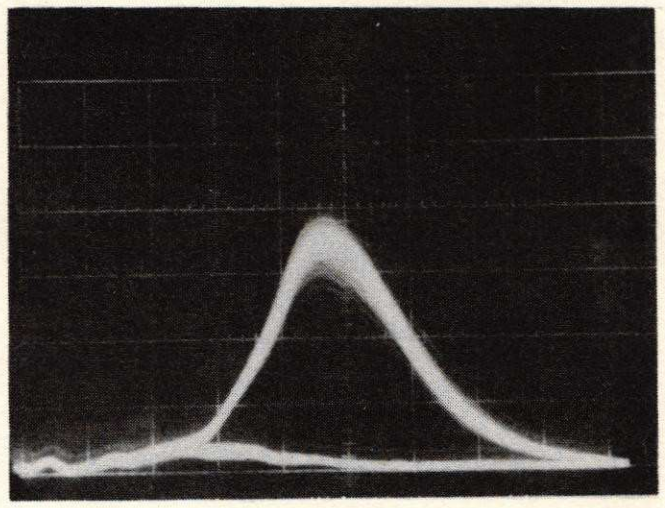
a) TEMP. 100°C
SW TIME 0.2 μSEC/CM
CAL 20 MV/CM



b)

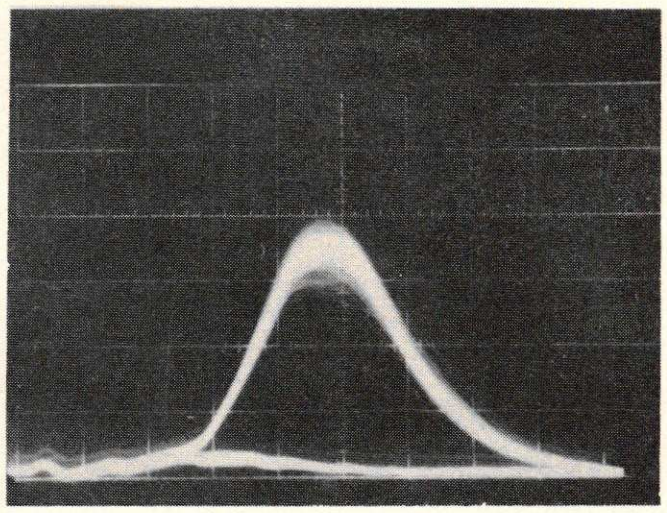


c) TEMP. 97°C
SW TIME 0.2 μSEC/CM
CAL 20 MV/CM

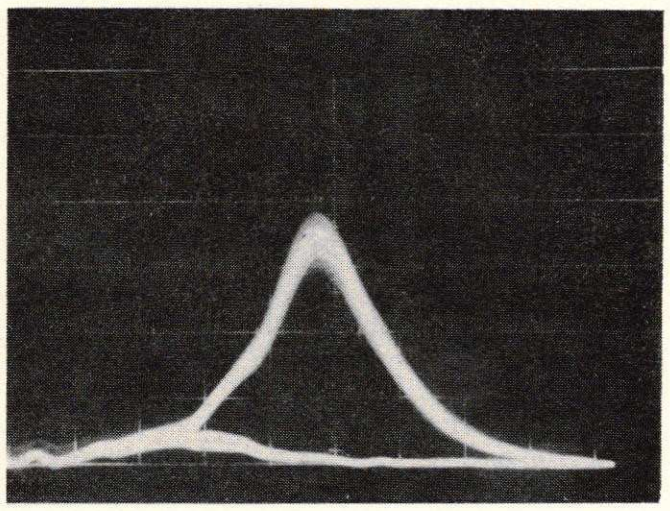


d) TEMP. 60°C
SW TIME 0.2 μSEC/CM
CAL 20 MV/CM

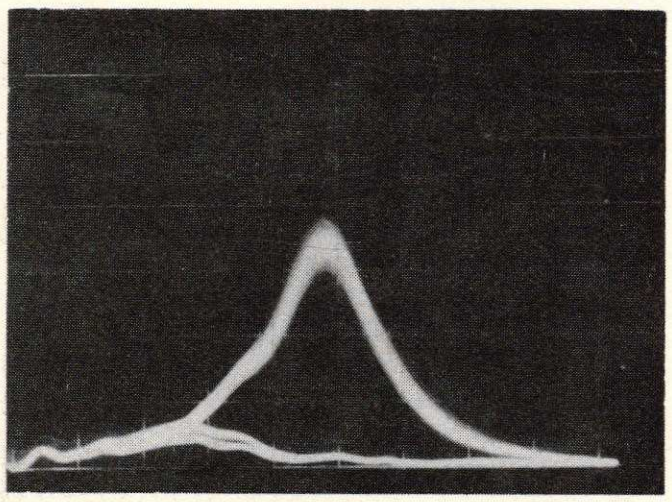
Fig. A-1



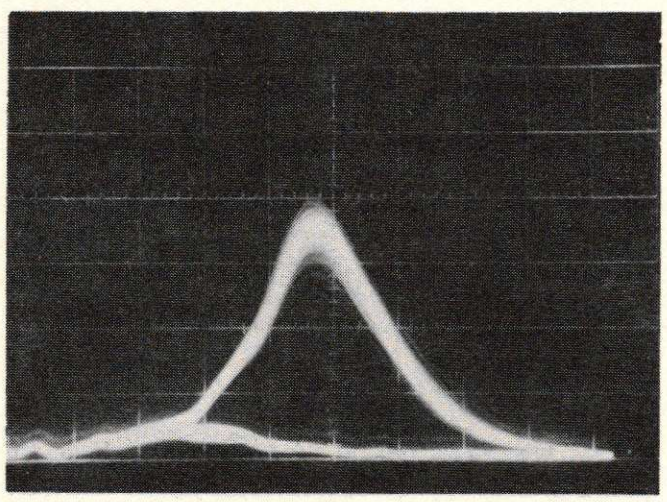
e' TEMP. 80° C
SUN TIME .2 μ SEC/CM
CAL 20 MV/CM



f) TEMP. 20°C
SUN TIME . 2 μ SEC/CM
CAL 20 MV/CM



g) TEMP. 0°C
SW TIME .2 μ SEC/CM
CAL 20 MV/CM



h) TEMP. 40°C
SW TIME .2 μ SEC/CM
CAL 20 MV/CM

Fig. A-1 (cont.)