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MIT/IL
Apollo Guidance and Navigation
Electronic Design Group Memo No. 46

Memo to: Pierre Sarda

From: John Barker

Date: 21 May 1968

Subject: Block II CDU Failure Modes While Operating Outside Acceptable IX Resolver Phase and Voltage Magnitudes. (22 Vrms with phase varied from 18 degrees to 63 degrees.)

Figure 1 presents the acceptable area of operation for the Block II CDU as the phase and magnitude of the IX Resolver outputs are varied. This area of operation is valid for balanced loading of the IX Resolver lines. Recent changes made to the S/C interfaces now present an unbalanced load condition on certain Resolver lines. A modification of Figure 1 operational boundaries may result because of these changes.

Figure 2 presents a functional block diagram of the CDU and will be used for explaining the failure mechanism as the phase and magnitude of the IX resolver lines are varied. The error signal generated by the IX and the 16X systems are equal to E sin $(\theta-\Psi)$. θ is the resolver angle and Ψ is the digital angle stored in the Read Counter. One other point to note at this time is that the presence of a IX error greater than the one speed system dead zone will override the 16X error and control the incrementing pulses to the Read Counter.

The results presented were taken with the CDU nominally at a Resolver angle of zero degrees. With this setting, the magnitude of the one speed Cos winding was reduced to 22 volts rms by lowering the excitation to the one speed resolver. Phase shift was introduced on the primary side of the resolver also. In this manner, balanced loading of the sine and cosine windings was simulated.

With the excitation fixed at 22 volts, the first instability point was encountered at 18 degrees of phase shift. The peak error observed in the Read Counter was 2.8125 degrees. The instability was produced in the following manner. As the magnitude of the IX Resolver's excitation is reduced, an error is produced at the output of the IX analog system. This

error results because the multiplication gains associated with the Cos θ input and with the Reference Signal input are mechanized to null each other at nominal system voltage levels. By lowering the resolver output voltages while the Reference signal remains fixed, a system error is created. The phase shift of the resolver signals enter the picture in the following manner.

The 800 Hz analog error signal from the CDU are normally interrogated at the 90 degree point of the carrier wave form. The Interrogation pulse is phase locked to the 28V 800 Hz Reference signal. As the Resolver outputs vary in phase with respect to the Interrogate pulse, the gains of the Sine and Cosine channels of the 1X analog system vary as the Cosine function of the phase shift. This introduces an additional error because these gains are used to null the Resolver outputs against the fixed Reference signal.

With the Resolver outputs lowered to a maximum output of 22 volts rms and with 18 degrees of phase shift introduced, a 1X error signal is generated which is large enough to exceed the 1X system dead zone. This error gates the incrementing pulses into the Read Counter. The state changes of the Read Counter in turn generated a 16X system error because the Resolver angle θ no longer equals the Read Counter angle ψ. As the Read Counter is incremented to an angle which will null the Coarse Error below the 1X dead zone, the 16X error increases. When the angle ψ is reached which drops the 1X system out of control, the 16X error will attempt to drive the Read Counter back to its zero condition. In this induced failure mode two error singals of opposite phase have been generated and their control of the Read Counter forces it to count up from zero to null the 1X system and down from this angle to null the 16X speed system. The result is an unstable condition where the CDU oscillates as control is passed back and forth between the 1X and 16X systems. The peak magnitude of the error introduced into the Read Counter is dependent on the amount of phase shift and the magnitude of the 1X resolver outputs with respect to the Reference Signal.

Peak errors induced into the CDU by maintaining the Resolver outputs at a 22 volt rms maximum and varying the phase shift from 18 degrees were:

1. 18° to 30°	2.8125° peak error
2. 30° to 56°	5.625° peak error
3. 56° to 63°	11 1/4° peak error

For the phase shifts from 18 degrees to 56 degrees or for the 2.8125 degrees and the 5.625 degrees peak errors, a fail indication was generated in the CDU. But for the 56 degrees to 63 degrees phase shift which had a peak error of 11 1/4 degrees, no fail signal was generated within the CDU. The reason for this can be explained in the following way. As the 1X system error increased to 11 1/4 degrees, the 16X error increased to a maximum at 5.625 degrees (90 degrees on 16X) and maintained a steady state error signal up until the 11 1/4 bit (180 degrees on 16X) was reached. At this point the 16X system has an ambiguous point. Because of the manner in which it is mechanized, the 16X system cannot differentiate between zero degrees and one hundred and eighty degrees. If the 1X error could be generated accurately enough, a stable condition between the 1X and 16X systems could be maintained. For this condition the 1X induced error would be nulled by setting the 11 1/4 degree bit and the 16X system would null because of the ambuguity. The pictures presented in this report for the 11 1/4 degrees peak error do not show this condition, but they show a small error between the two systems which results in an oscillation. The frequency of this oscillation is too low to trigger the Fail Circuit and no steady state error is generated to produce a Fail signal. The result is that for an induced error of 11 1/4 degrees, or very close to this point, no Fail indication will be received from the CDU. For all the other modes of instability up to this point a Fail signal was generated.

The following pictures present the modes of oscillation as the phase of the Resolver outputs are varied with the magnitude maintained at 22 Vrms.

Figure 3 illustrates various modes of oscillation with a peak error of 2.8125 degrees. Figures 3b, f, and g show the steady state error generated in the 16X system that triggers the Fail circuit. Figure 3c indicates the oscillation of the Up-line of the Read Counter for a stable oscillation mode.

Figure 3g illustrates an oscillation that changes modes over the period of observation. A longer period of surveillance would show a repeatable pattern of these changing modes. Figures 3d and 3e show the AOG pulses that are sent to the AGC during the oscillatory condition of two stable modes. They show oscillatory errors of plus and minus 0.133 degrees and 0.222 degrees respectively.

Figure 4 illustrates the oscillatory modes for the 5.625 degree peak error condition. 4a indicates that the Fine Error at the Main Summing Amplifier output has reaches its maximum amplitude and does not show an oscillatory modulation. The Coarse Error, however, shows the modulation effect of the oscillation. Figures 4c and 4d illustrate the amplitudes of the oscillations during different modes. 4c indicates a steady repeatable mode with a plus and minus peak of 0.133 degrees. Figure 4d illustrates a mode with plus and minus peaks of 0.133 degrees, but with a higher frequency lower peak oscillation of 0.045 degrees intermingled.

Figure 5 shows a mode of oscillation with a 11 1/4 degree peak error. 5a and 5b indicate the oscillation period is approximately 30 milliseconds. The Fine Error signal steady state error is no longer present, but this error has been transmitted to the AGC while establishing the unstable system condition between the 16X and 1X systems. Figure 5c illustrates that a plus and minus oscillatory error of 0.133 degrees is sent to the AGC.

The S/C systems that influence the 1X Resolver inputs to the CDU are the FDAI, the ORDEAL, and the Attitude Set Resolvers. These systems are switched on or off, or transfer switching takes place between two systems at various times during operation. A functional block diagram of this interface is included as Figure 6.

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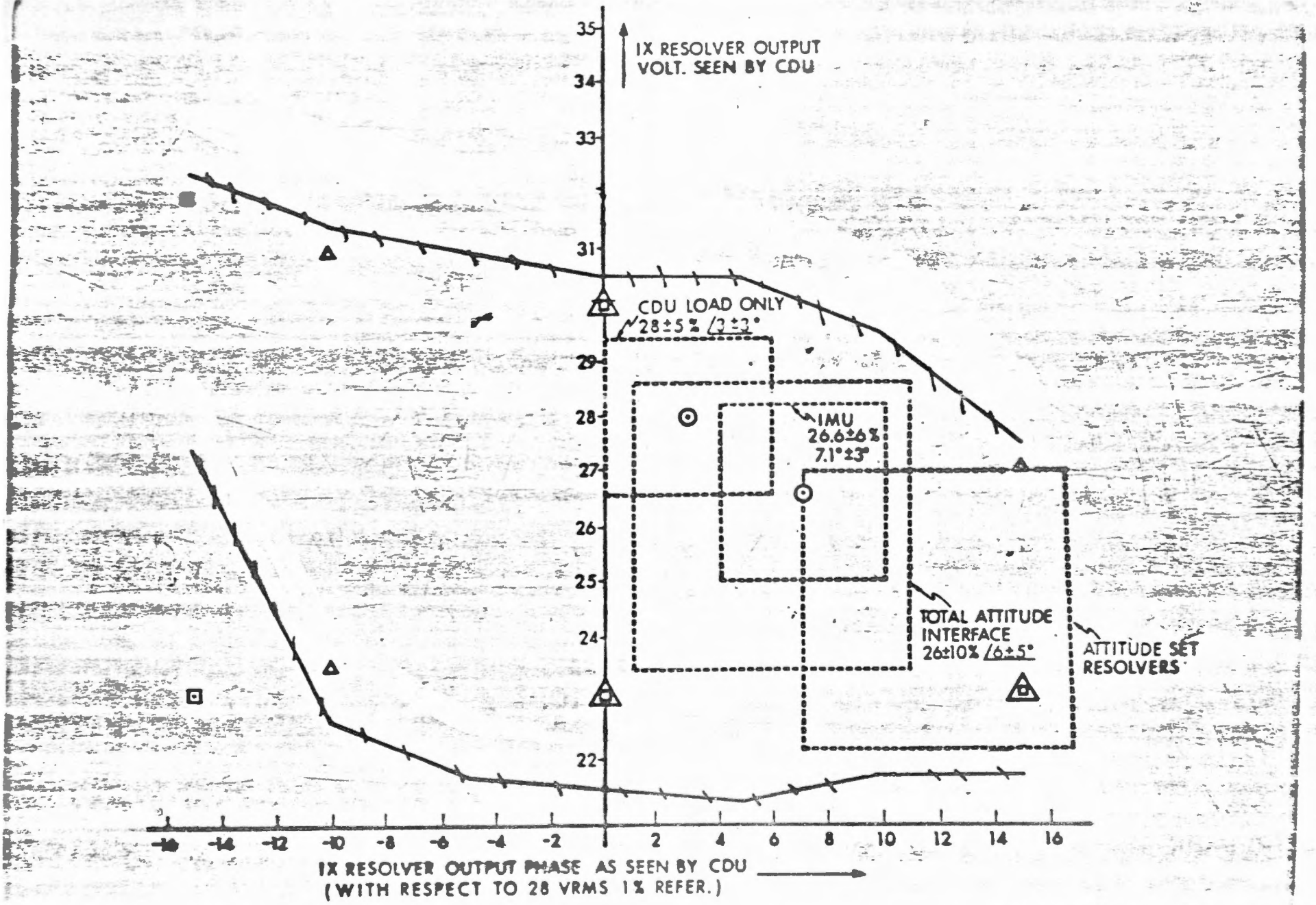

1X RESOLVER OUTPUT
VOLT. SEEN BY CDU
35
34
33
31
29
28
27
26
25
24
22
CDU LOAD ONLY
28±5% /3±3°
IMU
26.6±6%
7.1°±3°
TOTAL ATTITUDE
INTERFACE
26±10% /6±5°
ATTITUDE SET
RESOLVERS
-16
-14
-12
-10
-8
-6
-4
-2
2
4
6
8
10
12
14
16
1X RESOLVER OUTPUT PHASE AS SEEN BY CDU
(WITH RESPECT TO 28 VRMS 1% REFER.)

Fig. 1

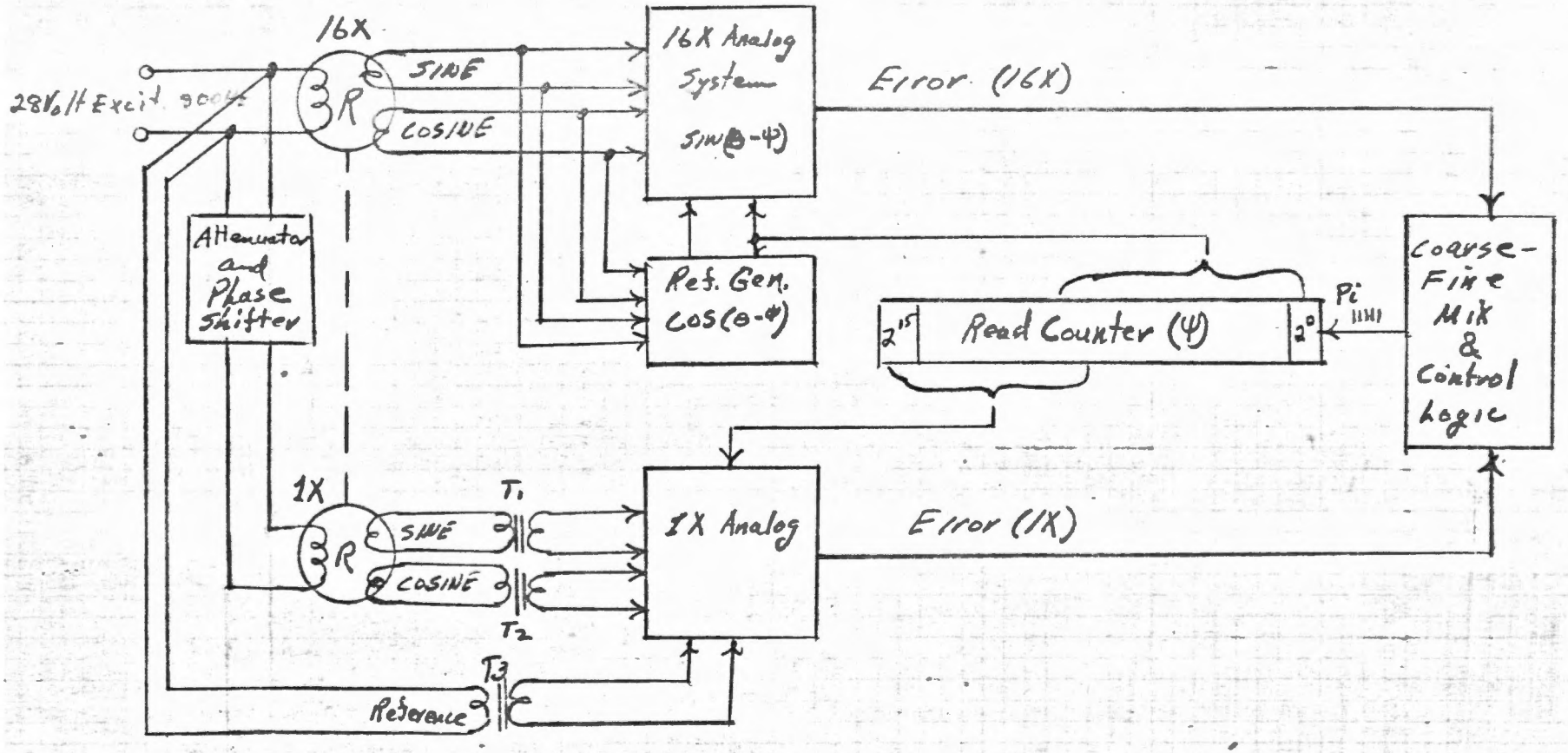
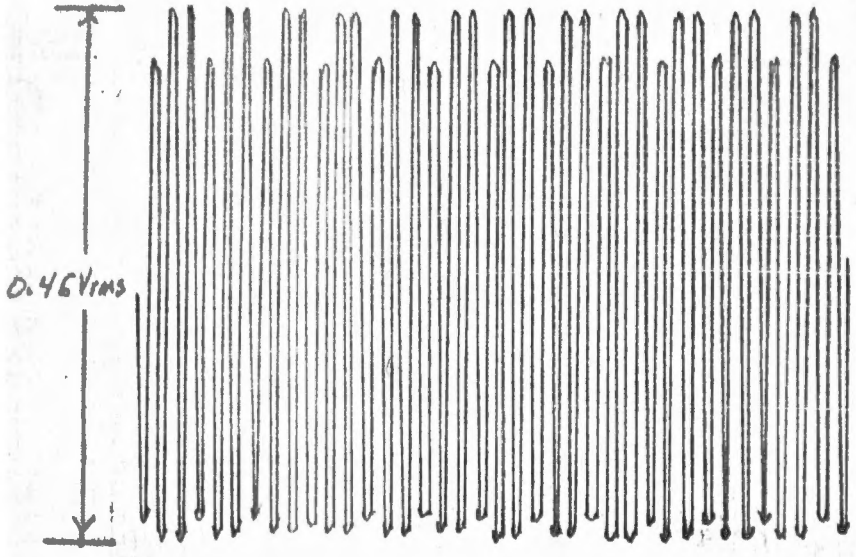


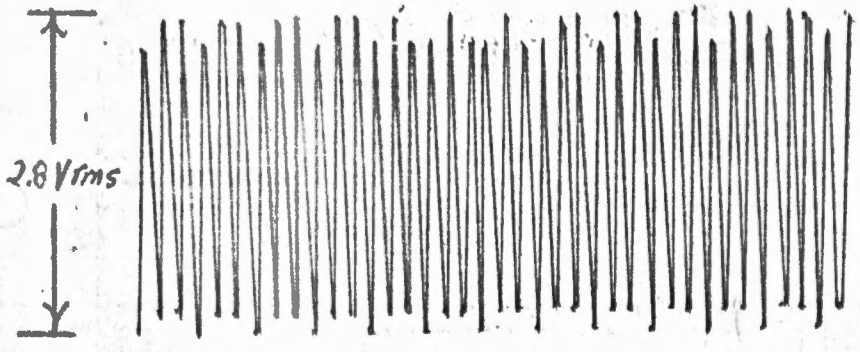
Fig. 2

Functional Block Diagram
Block II CDU Test
Mechanization



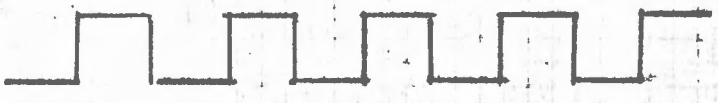
Coarse Error
18.5° Phase Shift
800 Hz
2.8125 Peak Error

Fig. 3a



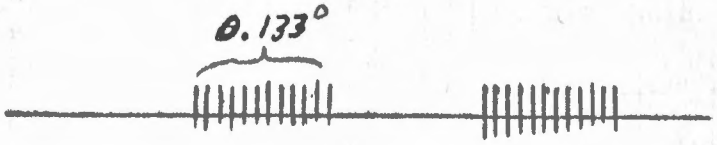
Fine Error
18.5° Phase Shift
800 Hz
2.8125 Peak Error

Fig. 3b



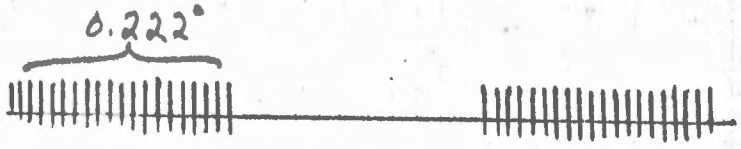
Read Counter
Up-Line
18.5° Phase Shift
2.8125 Peak Error

Fig. 3c



18° Phase Shift
2.8125° Peak Erro

Fig. 3d



18° Phase Shift
2.8125° Peak Erro

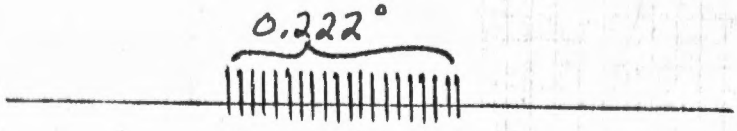
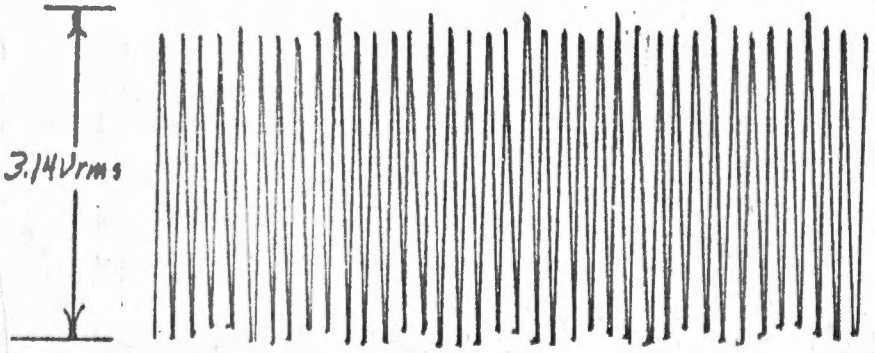
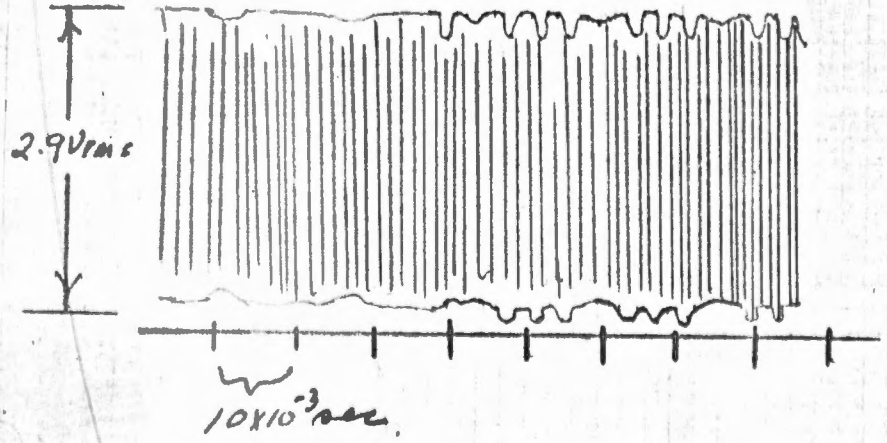


Fig. 3e



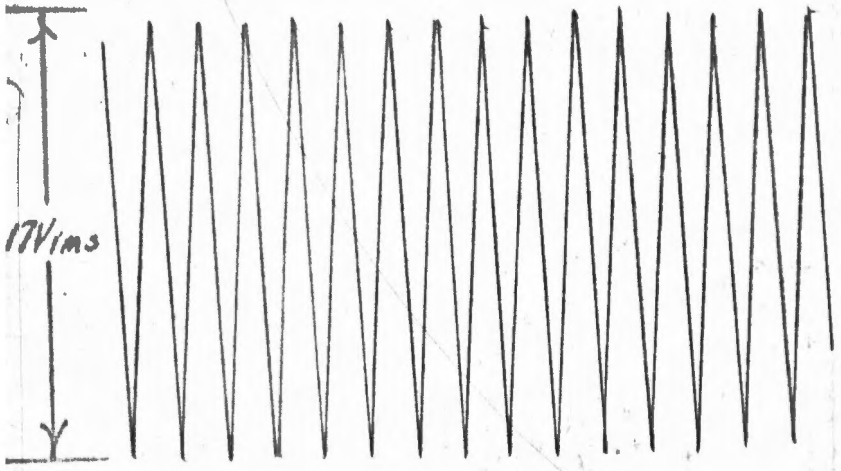
Fine Error
18.5° Phase Shift
2.8125 Peak Error
800 Hz

Fig. 3f



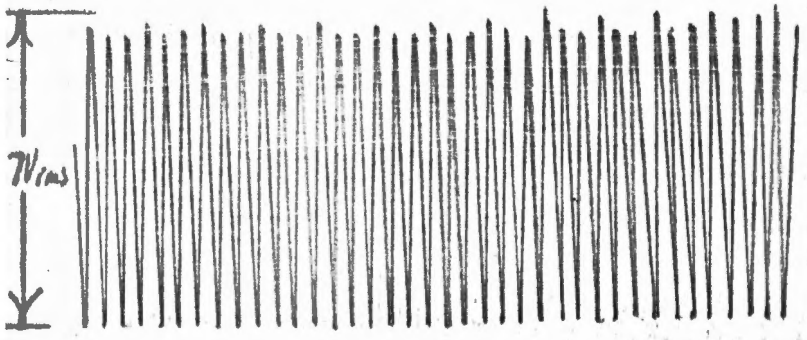
Fin-Error
18.5° Phase Shift
2.8125 Peak Error

Fig. 3g



Fine Error
30° Phase Shift
800Hz
5.625 Peak Error

Fig. 4a



Coarse Error
30° Phase Shift
800Hz
5.625 Peak Error

Fig. 4b

33° Phase Shift
5.625 Peak Error

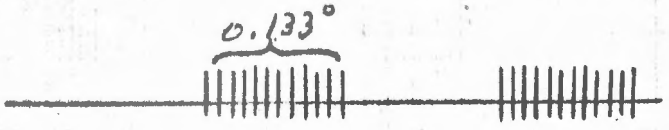
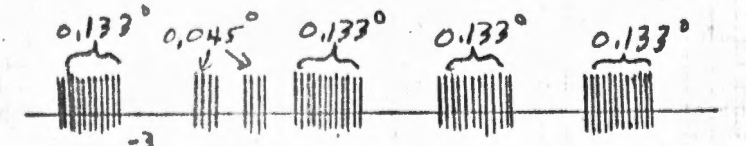


Fig. 4c



30° Phase Shift
5.625 Peak Error

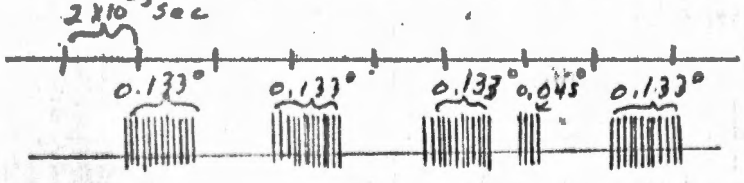
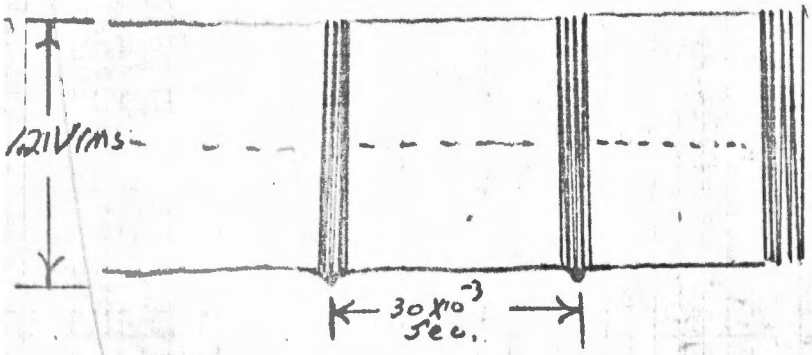
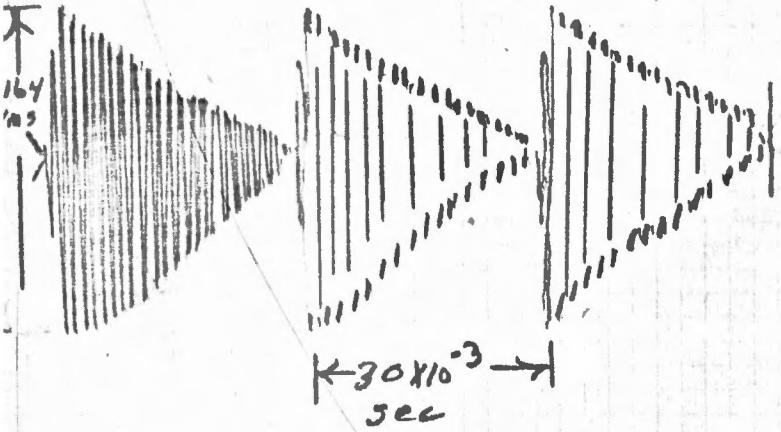


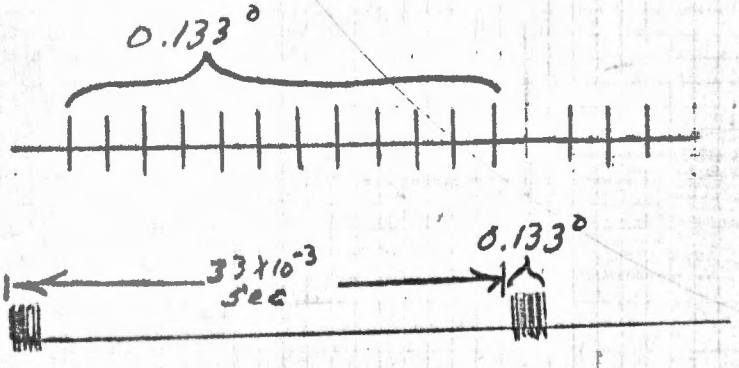
Fig. 4d.



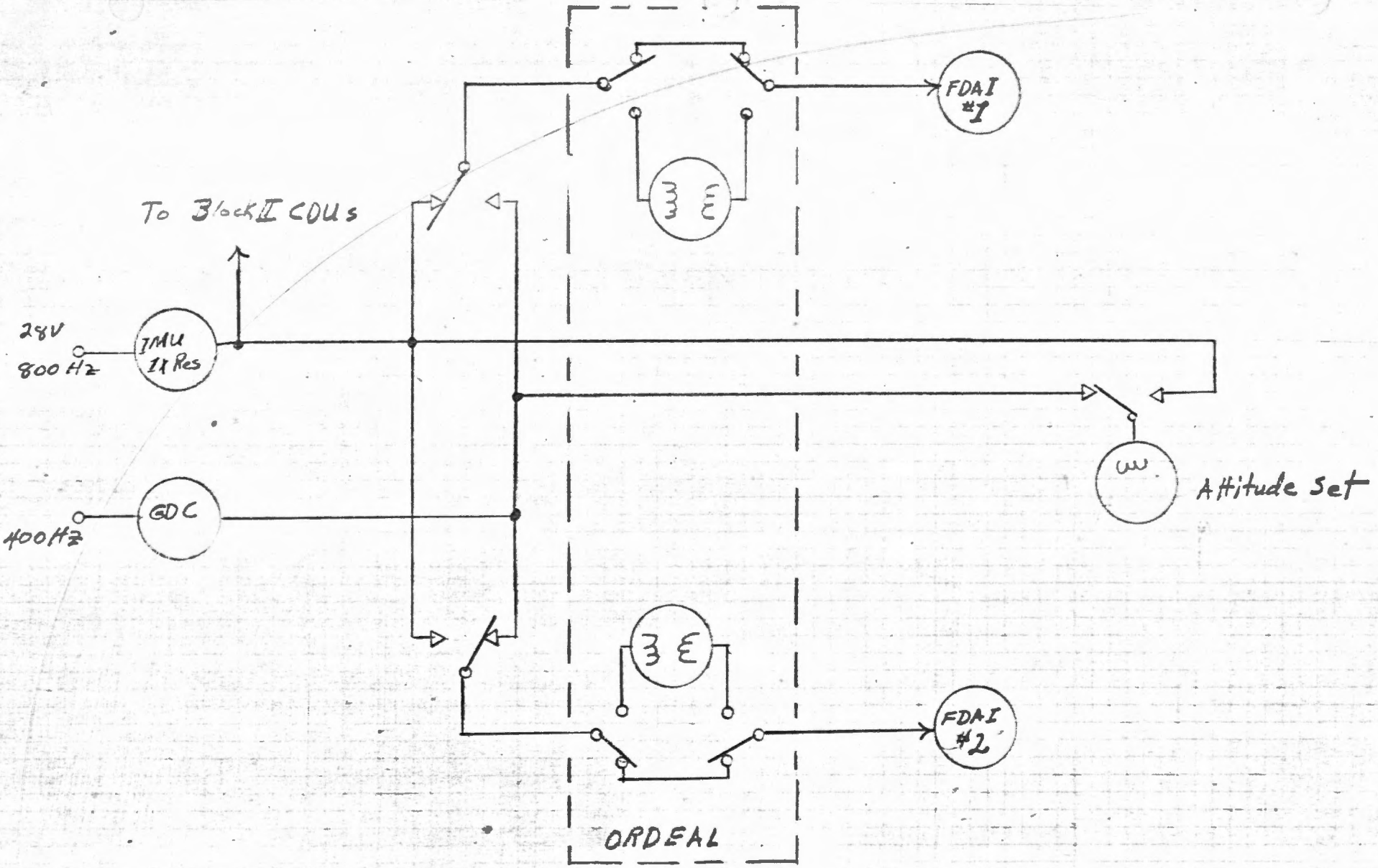
Coarse Error
56° Phase Shift
11¼° Peak Error
Fig. 5a



Fine Error
63° Phase Shift
11¼° Peak Error
Fig. 5b



60° Phase Shift
11¼° Peak Error
Fig 5c



Functional Block Diagram
S/C Loading Of IMU 1X
Resolvers

Fig 6