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ISS MEMO # 275

TO: R. H. Battin  
FROM: R. Crisp  
SUBJECT: Block II IRIG Pulse Torquing  
DATE: 9 November 1965

a. The timing requirements for Block II IRIG pulse torquing are spelled out on drawing #6015564 as follows:

Note 2. Gyro torque enable signal must be received at least 20 milliseconds prior to any torque set pulse.

3. Gyro select signal must be received at least one clock time (3200 cps) prior to any torque set pulses.

4. Gyro reset pulse must be given at least one clock time (3200 cps) prior to de-energizing the gyro select signal line

6. Current switch must be in reset condition prior to receiving gyro torque enable signal from the computer.

7. A positive AGC torque command ( $+\Delta\theta$ ) signal produces torque in the TM- winding of the gyro resulting in a positive rotation about the gyro input axis.

Due to the way the counter is mechanized (to ensure accurate output pulse timing) the delay required by note #3 is automatically obtained between activating the counter and the first set pulse. A similar delay exists between the removal of the activity bit and the first reset pulse, beware.

b. It is understood that the input to the pulse torque program will be a double precision angle scaled in revolutions. The address of the location is to be present in the A register as an ECADR.

- c. Measurements have shown that the first pulse is only worth 78.5% of one from an infinite train. The spread on this figure is about +2% so we consider it adequate to store this constant in fixed memory. The error due to this assumption can be further reduced by sending out a minimum pulse train of 16 pulses. (i.e. 0.25 CDU pulse). This also reduces the effect of timing errors in the set and reset pulses (see DDG Memo #173).
- d. In discussions with C. A. Muntz a scheme has evolved using the following coding sequence.

CA	ECADR
TC	BANKCALL
CADR	IMU/PULSE
TC	BANKCALL
CADR	IMUSTALL

We recommend that the gyro enable be turned off 50 millisecc (?) after a command has gone out unless a further command has been made, to prevent undue relay switching.

  

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RC:jdn

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