Spacecraft Research Division
NASA - Manned Spacecraft Center
Houston, Texas
September 28, 1962

MEMORANDUM for Chief, Spacecraft Research Division

Subject: August 16 to 31, 1962 trip to MIT Instrumentation Laboratory

1. A visit to MIT/IL was made for the purpose of achieving detailed familiarization with all aspects of the Apollo Guidance Computer. The persons contacted were:

J. Barnard	MSC
E. Hall	MIT
A. Hopkins	MIT
R. Alonso	MIT
D. Schansky	MIT
D. Hanley	MIT
J. Deyst	MIT
H. A. Koso	MIT
L. Barone	MIT

2. The trip activities primarily involved the collection of information concerning the design of the Apollo Guidance Computer from Albert Hopkins, Ramon Alonso, Dave Schansky and their associates. All portions of the computer were covered by discussion, study of prints and written material, and observance of the testing and operation of the computer. Brief periods were also spent with various other personnel concerning the AGC software, proposed laboratory use of VERDAN computers, and certain specific questions about the sextant.

3. During the first day, Albert Hopkins spent several hours discussing the overall computer design and design philosophy. This provided the background on which to build. From that time a pattern was set of: introduction to a circuit, study of the circuit, followed by a detailed explanation. The entire computer was covered in this manner including the areas of input-output and interface. Although this routine constituted the majority of the time, it was interrupted regularly in order to obtain other information as described in the following paragraphs.

4. At this time, the ferrite memory selection circuit was being debugged. The writer observed and in some instances assisted in the debugging.

5. The construction of the breadboard and construction techniques were noted. Also, the packaging techniques of the flyable computer was investigated.

6. Computer programing was discussed. This includes two areas: MH 800 programing which supports and aids the AGC programing, and that of the AGC itself. The first area is very nearly complete. It includes such programs as the assembler, simulation program, etc. In the second area, only certain subroutines, the interpretive routines, and a pre-launch platform alinement routine have been completed. The navigation equations are not yet being coded, therefore, only the planned navigation technique was discussed. The principal goal was to learn the function of the programs and subroutines, and to become more familiar with the programing development plans. To go further would have involved going into the coding of the computer or into the derivation of equations; the writer felt that this would have been of little value at this time.

7. Information was obtained concerning the proposed usage of VERDAN computers. The digital development group will use a VERDAN to simulate inputs and outputs in order to test the AGC interface. Also, a VERDAN will be utilized to simulate the resolution electronics between the sextant hand controller and the sextant drive.

8. Mr. J. Dahlen and Mr. D. A. Koso outlined the sextant errors and sighting difficulties due to spacecraft motion. This information has been passed on, as requested to Mr. Fred Pearce of the Spacecraft Research Division.

9. In general, an attempt was made to cover every aspect of the AGC with maximum concentration on computer circuit design and interface. Some pertinent notes on AGC features are listed in an enclosure. From the viewpoint of knowledge and data collected it is felt that the trip was very successful.

10. The two-week period was ample time for the collection of most of the fundamental data; however, a future trip would be advantageous after the computer is thoroughly debugged and operating in conjunction with other systems.

Charles D. Brady
AST, Control and Guidance Section

CDB: pj

TVC

RGC

Enc:
AGC Features

1. Major Features of the AGC

   a. Priority circuit: Input lines are not scanned; when an input becomes active, the computer interrupts its present task to tend to that input, returning to its former activity after the input has been dealt with. This is done on a priority basis; if more than one input becomes active at once, the one of highest priority is tended to first. This technique greatly assists efficient computer utilization.

   b. Variable speed: During periods of relative inactivity, the computer can operate at a reduced speed, thus decreasing power consumption.

   c. Low Power consumption: It is thought that the computer will consume less than 35 watts at its maximum speed and less than 10 watts at the minimum speed.

   d. Reliability: A MTBF of 4200 hours has been predicted. However, this may have been based on an original component count which included 1350 transistors. More recent information seems to indicate a count of over 2000 transistors. If this is correct, reliability should be diminished accordingly; this will be pursued further.

   e. Size: Although not severly pushing the "state-of-the-art," the use of core rope storage and good packaging technique provide a computing system of reasonably small size.

   f. Rugged construction: Excellent packaging techniques, including "wire wrap" interconnections between modules, create a computer of sturdy construction.

2. Input/Output

   a. Input

      (1) Incremental: A counter is incremented (decremented) upon receipt of an input pulse indicating an increase (decrease) of the input variable by a discreet amount. There are 26 erasable registers serving as counters.

(2) DC: A stage of an input register is set by some DC source, e.g., a toggle switch. This stage could represent an indicator key, e.g., an Engine "ON" key, or several stages could represent an input word, e.g., a word from the keyboard. There are at present six, fifteen bit input registers.

(3) Up link from GSE: Data is shifted serially from the GSE into the computer. The exact mechanization of this has not been determined. There will be no telemetry up link to the computer.

b. Output

(1) Pulse rate: Certain output functions are represented by pulse rates. These rates are used to drive such things as the CDU's, sextant, and IRIG's.

(2) DC: Outputs of bi-stable latches, each representing a stage of an output register, are used to provide DC levels to various equipment (including the pulse rate output circuit within the AGC). Examples of the functions of these levels are: transmit a word in parallel to the digital readout panel for display (several stages representing a word), start and cut-off engine, determine the magnitude and recipient of the pulse rates, etc. Six, fifteen-bit output registers are planned.

3. Down line to GSE, down telemetry: Data is shifted serially from the computer to either the GSE or to a down telemetry transmitter. An idea for the mechanization of this has been advanced, but the subject is still being discussed.