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AC SPARK PLUG DIVISION General Motors Corporation Milwaukee, Wisconsin	EXPERIMENTAL DESIGN EXHIBIT	XDE 34-T-41		REV B
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APOLLO GSE MONITOR PANEL (BLOCK I, SERIES 100, BLOCK II, AND LEM) SYSTEM DESIGN CRITERIA

1. SCOPE

1.1 This document establishes the system performance requirements for the Apollo GSE Monitor Panel monitoring and test circuits.

2. APPLICABLE DOCUMENTS

2.1 Unless otherwise indicated, the following documents shall form a part of this design criteria:

_____	Performance/Design and Product Configuration Requirements Ground Support Equipment for Apollo G & N System
2900207	Diagram, Mechanization Monitor Panel (Block I, Series 100, Block II and LEM)

3. REQUIREMENTS

3.1 General - The Monitor Panel's (MPL) function in the Optical Inertial Analyzer (OIA) is to provide visual and audible indications of normal and abnormal test conditions. The normal G & N System or Subsystem functions displayed, shall serve as interface verification for interfaces that may be present many times during testing. The abnormal conditions that are monitored shall be used to indicate a test condition that will cause improper G & N data to be obtained and to provide interlock circuits to prevent damage to the G & N System or Subsystem under test.

3.2 Circuits - The circuits required in the MPL to perform all necessary system and subsystem functions are as follows:

A. Passive Circuits
   1. 28 VDC Voltage Detectors
      a. Contact closure input
      b. Buffer resistor input
   2. 28 VDC Voltage Comparator
   3. 102.4 KC Detector
   4. Phase Angle Detector
   5. 28 V 800 CPS Voltage Comparator
   6. -28VDC Voltage Comparator
   7. Light Indication

B. Alarm Circuits
   1. 28 VDC G & N Power High-Low Sensor
   2. 115 V, 60 CPS 3-Phase High-Low Sensor

3. 2 V, 3200 CPS Voltage/Frequency Comparator
4. Coolant Supply, Coldplate Temperature, and TMC Alarm Indicators

C. Alarm Verification Circuits
1. 28 VDC G & N Power High-Low Sensor, high voltage test circuit
2. 28 VDC G & N Power High-Low Sensor, low voltage test circuit
3. 115 V, 60 cps 3-Phase High-Low Sensor, Phase A low sensor test circuit
4. 115 V, 60 cps 3-Phase High-Low Sensor, Phase B low sensor test circuit
5. 115 V, 60 cps 3-Phase High-Low Sensor, Phase C low sensor test circuit
6. 2 V, 3200 cps Voltage/Frequency Comparator, high frequency test circuit
7. 2 V, 3200 cps Voltage/Frequency Comparator, low frequency test circuit
8. 2 V, 3200 cps Voltage/Frequency Comparator, low voltage test circuit

D. Operational Circuits
1. Alarm Inhibit Circuit
2. Temperature Downmode Circuit
3. Alarm Battery Circuit
4. Flasher Circuit
5. GSE Configuration Circuits
6. Gimbal Dump Circuit
7. Status Relay Verification Circuits
8. Time Delay Circuits

3.2.1 Passive Circuits - The MPL shall have the capability to verify G & N interfaces by monitoring for the presence of signals or the loss of signals and providing a visual indication to the test conductor of the condition that has occurred.

3.2.1.1 28 VDC Voltage Detectors shall be used to monitor and indicate the following:

Block I, Series 100
a. Error Detect
b. IMU Delay
c. Gimbal Lock Caution
d. IMU Temperature Fail
e. Zero Optics
f. Mark
g. Not Mark

Block II
a. IMU Fail
b. ISS CDU Fail
c. Optics/RR CDU Fail
d. Star Presence
e. Zero Optics
f. Mark
g. Not Mark

LEM
- a. IMU Fail
- b. ISS CDU Fail
- c. Optics/RR CDU Fail

3.2.1.2 A 28 VDC Voltage Comparator shall be used to continuously monitor the IMU's TEMP WITHIN LIMITS signal during a Block II or LEM G&N or ISS test. An "IMU TEMP FAIL" visual indication shall be generated when the circuit operates.

3.2.1.3 102.4 KC Detectors shall be used tomonitor and indicate the following during Block I, Series 100 testing:

- a. IMU Fail
- b. ISS CDU Fail
- c. Accel Fail
- d. Star Presence

3.2.1.4 A Phase Angle Detector shall be used to monitor the IMU's middle gimbal cos 1X resolver error signal during Block II or LEM testing. A "Gimbal Lock Caution" indication shall be obtained at the circuit operate points.

3.2.1.5 A 28 V, 800 cps Voltage Comparator shall be used to continuously monitor the IMU Wheel Power, Phase A power source. A "Wheel Power Fail" visual indication shall be generated when the circuit operates.

3.2.1.6 A -28 VDC Voltage Comparator shall be used to continously monitor the PSA's -28 VDC Power Supply output. A "-28 VDC Fail" visual indication shall be generated when the circuit operates.

3.2.1.7 A light indication shall be obtained whenever 27 VDC, high and lo, is present at the "CGC/LGC Power Fail" interface during all G&N tests. Light indications will also be obtained whenever 27 VDC RLP HI is available at the MPL interfaces to light the "Ducosyn Excitation Monitor Inhibited" or the "Gimbal Dump Inhibited" indicators.

3.2.1.8 The MPL shall contain indicators that will continously monitor the G&N conditions which are normally monitored at the NAA Main Panel. These indicators shall also serve as an interface verification during Main DSKY Test. The Monitor Panel shall contain the following Light Indicators. 1-G&N Caution,2-ISS Warning, 3-ISS Warning LMP, 4-CGC/LGC Warning No. 1, 5-CGC/LGC Warning No. 2, 6-SIVB Cut Off 7-RR Auto Angle Enable, 8-SIVB Injection Sequence Start, 9-LEM Radar Hover Position Command, 10-Computer Standby, 11-Display Keyboard Spare SD444, 12-Display Keyboard Spare SD445.

3.2.2 Alarm Circuits - The MPL shall contain circuits that will continously monitor G&N and GSE powers and conditions that could cause equipment damage or abnormal test results. These circuits shall cause an audible alarm to sound and downmode the equipment to a safe mode condition.

3.2.2.1 A 28 VDC G&N Power High-Low Sensor is required to monitor the GSE's 28 VDC G&N Power Supply output. This circuit shall produce a visual flashing indication when a "G&N VOLTAGE HIGH" or a "G&N VOLTAGE LOW" condition exists. Both the high or the low voltage failure shall cause the GSE to downmode to an "OIA ON" mode with all power to the G&N system or subsystem removed.

3.2.2.2 A 115 V, 60 cps, 3-Phase High-Low Sensor is required to monitor all three phases of the 115 V, 60 cps prime power to the OIA. A "PRIME POWER HIGH" or a "PRIME POWER LOW" flashing visual indication shall be produced if any one or all of the prime power phase inputs is not within the required voltage limits. If this sensor operates, it shall override all other sensors that operate during the OIA pilot power mode.

3.2.2.3 A 2 V, 3200 cps Voltage/Frequency Comparator is required to monitor the 3200 cycle IMU Ducosyn excitation. This comparator shall produce a visual flashing indication of "Ducosyn Excitation Voltage Fail" or a "Ducosyn Excitation Frequency Fail" or both depending on the nature of the failure. This comparator shall operate with a 2 V, 3200 cps input in all G & N test configurations. During Block II and LEM testing the 28 V, 3200 cps ducosyn excitation shall be conditioned and converted to 2 V, 3200 cps in the Oscillograph Signal Selection Panel.

3.2.2.4 Coolant Supply, Coldplate Temperature, and Temperature Monitor Control Alarm Indicators - The MPL shall provide a visual flashing indication and produce an audible alarm when the following situations occur:

a. Loss of CLS Remote Alarm Control shall produce a "Coolant Supply Fail" indication. A "Coolant Supply Fail" indication only will occur when the Coolant Supply Fail Lamp signal is present.
b. Loss of the Coldplate Temperature Normal signal shall produce a "Coldplate Temp Fail" indication.
c. Loss of the Temperature Normal Lo signal shall produce a "Temperature Control Fail" indication.

3.2.3 Alarm Verification Circuits - The MPL shall provide circuits that will verify the operation of the MPL Alarm circuits upon a specific test command from the Test Selector Panel. The individual tests that will be performed will be as listed in paragraph 3.2-C.

3.2.4 Operational Circuits - In addition to the monitor circuits and alarm circuits, the MPL shall also contain certain circuits that enable the alarm, lights, and OIA downmoding to operate as required.

3.2.4.1 The MPL shall contain an Alarm Inhibit Circuit that will allow the alarm to be inhibited during normal GSE-G & N operations only when an alarm condition exists. The Alarm Inhibit Circuit shall only be enabled during an alarm situation, the circuit shall be latched in after the alarm is inhibited, and the alarm circuit shall be automatically reset and ready to ring again upon resetting the circuit causing the alarm to ring. A visual indication of the "Alarm Inhibit" situation shall be provided. An alternate action switch shall be provided on the MPL's rear panel that will allow the alarm to be disabled when the MPL is disconnected. If the MPL is in the OIA and the rear panel switch is thrown the "Alarm Inhibit" light shall be on.

3.2.4.2 During Block II and LEM testing only, the MPL shall provide a circuit that will disable the GSE-G & N power circuits when there is a coldplate temperature that is not within the required limits, or if there is a Coolant Supply high pressure or a low coolant flow rate to the IMU. If either of the temperature failures occurs, and the alarm is not inhibited by the operator pressing the Alarm Inhibit Button, the MPL shall cause a "G/N Power Modes Disabled" condition after 3 minutes and 40 seconds. The MPL shall provide a visual indication of the "G/N Power Modes Disabled" condition. This condition means that all GSE-G & N power control circuits, controlled from the Test Control Panel, have been disabled and if power were applied to the G & N system or subsystem it will be removed automatically. It will be impossible to apply G & N power when the "G/N Power Modes Disabled" light is on.

If the Alarm Inhibit Button is pressed by the test conductor, the alarm will be turned off and the test conductor will be allowed 3 minutes with a temperature failure condition before the alarm will ring again. If the operator does not press the Alarm Inhibit Button again, the "G/N Power Modes Disabled" condition will occur in 40 seconds. The test conductor can keep from being downmoded as long as the Alarm Inhibit Button is pressed each time the alarm rings. The alarm inhibit switch on the rear of the MPL or keeping the Alarm Inhibit Button depressed will not override the downmode circuit.

3.2.4.3 The MPL shall contain a chargeable battery that will provide power for light indications and an alarm if all power to the OIA were removed. The battery shall be charged at all times except during an alarm condition.

3.2.4.4 The MPL shall contain a flasher circuit to provide flashing light indications during alarm situations or other situations, such as Gimbal Dump, which do not ring the alarm. The flasher shall operate from pilot power or the battery if pilot power is removed. The indicator lamps shall serve as the flasher loads.

3.2.4.5 The MPL shall contain circuitry that will verify that all GSE-G & N configuration relays are operating properly. The GSE contains some circuits that are used for more than one G & N configuration. If the status relay, that enables multiple use for such circuitry were to fail, damage would occur both to G & N equipment or to GSE equipment. There are other situations where a status relay failure would disable required GSE circuits and the test conductor would not be aware of the situation.

The MPL shall provide the following GSE-G & N configuration indications:

a. G/N TEST CONFIGURATION
b. ISS TEST CONFIGURATION
c. OSS TEST CONFIGURATION
d. BLOCK I, SERIES 100
e. BLOCK II
f. LEM
g. GSE REF POWER (Measurement equipment calibration circuitry)
h. GSE CALIB. ENABLED (Measurement equipment calibration circuitry)

The following configuration indications will cause a "G/N Power Modes Disabled" condition:

a. G&N TEST CONFIG. AND ISS TEST CONFIG.
b. ISS TEST CONFIG. AND NOT ISS TEST CONFIG.
c. ISS TEST CONFIG. AND OSS TEST CONFIG.
d. G&N TEST CONFIG. AND OSS TEST CONFIG.
e. OSS TEST CONFIG. AND NOT OSS TEST CONFIG.
f. NOT G& TEST CONFIG. AND NOT ISS TEST CONFIG. AND NOT OSS TEST CONFIG.
g. BLOCK I, SERIES 100 AND NOT BLOCK I, SERIES 100
h. BLOCK I, SERIES 100 AND BLOCK II
i. BLOCK I, SERIES 100 and LEM
j. BLOCK II AND NOT BLOCK II
k. BLOCK II AND LEM
l. NOT BLOCK I, SERIES 100 AND NOT BLOCK II, AND NOT LEM
m. GSE REF POWER OR GSE CALIB. ENABLED

3.2.4.6 The MPL shall provide a visual flashing indicator when it receives a 27 VDC RLPHI signal from the Test Control Panel. During Inertial Subsystem (ISS) testing the visual cindication shall be the only Gimbal Dump function of the MPL because the Gimbal Dump circuits in the Gimbal Position Control Panel will be able to open the gimbal loops. During G&N system testing, however, the MPL will cause the ISS to downmode to the ISS Standby power mode so that all torquing would be disabled. This is done because the GSE does not have access to the inter loop interfaces during G&N system testing.

3.2.4.7 The MPL shall provide a verification of every G&N configuration gate that is used in the panel. For instance, if 3 relays are used for the Block II and LEM configuration conditions, there shall be a set of contacts used on each relay that will provide an RLP LO to the configuration verification circuitry (3.2.4.5) to verify that the relay is energized or deenergized.

3.2.4.8 The time delay circuits used in the MPL shall all be electronic time delays with a reset time of less than 30 milliseconds. The time tolerance shall be ±10%.

3.2.4.9 The MPL shall provide the capability of a remote alarm indication if 115V, 60 cps GSE Prime Power fails during PTC operation.

3.3 Performance - The circuits listed in paragraph 3.2 shall perform to the following requirements with all voltages as RMS values, all impedances as resistive loads, and all signals that originate from G&N circuits isolated from GSE grounds unless noted otherwise.

3.3.1 28 VDC Voltage Detector

a. Nominal level — 0 VDC
b. Trip Level — 28 (+2, -3) VDC
c. Source — Switch closure
Circuits
Block I, Series 100
1. Error Detect
2. IMU Delay
3. Gimbal Lock Caution

4. IMU Temp Fail
5. Zero Optics
6. Mark
7. Not Mark

Block II

1. Star Presence
2. Mark
3. Not Mark

d. Source - Through a 2KΩ resistor
Circuits
Block II and LEM
1. ISS CDU Fail
2. Optics/RR CDU Fail
3. IMU Fail

3.3.2 28 VDC Voltage Comparator

a.	Nominal Level	28 (+2, -3) VDC
b.	Trip Level	loss of 28 VDC
c.	Source	Through 3KΩ resistor

Circuits
1. IMU Temp Fail - Block II and LEM

3.3.3 102.4 KC Detector

a.	Nominal Level	0 Volts
b.	Trip Level	1 to 5 volts P.P. (E_s)
c.	Frequency	102.4 KC pulse train
d.	Pulse width	3 microseconds
e.	Pulse polarity	Positive
f.	Source	

Circuits
Block I, Series 100
1. IMU Fail
2. ISS CDU Fail
3. Accel Fail
4. Star Presence

3.3.4 Phase Angle Detector

a.	Nominal Level	Cosine winding of the MG 1X resolver
b.	Trip Level	All MG angles in excess of ± 60° ± 5° with respect to 0° Middle Gimbal Angle (Ref.) IMU 1X Resolver TR = 1 ± 2% (V_{excit} = 28.0 ± 1%)
c.	Frequency	800 CPS
d.	Detector Input Impedance	> 50K-ohms within 5%. Normal load on the IMU resolver (1X) is the G & N CDU and the GSE Gimbal Positioners.

Circuit
Block II and LEM
1. Gimbal Lock Caution

3.3.5 28 V, 800 cps Voltage Comparator

a.	Nominal Level	28 V ± 5%
b.	Frequency	800 cps sine wave
c.	Trip Level	decrease to 15 ± 1 V or less
d.	Source Impedance	3 ohms
e.	Minimum input impedance	
f.	Circuit must latch and remain on even in the OIA ON mode. A reset button must be pressed to reset the circuit and remove the visual display.	

Circuit
1. Wheel Power Fail

3.3.6 - 28 VDC Voltage Comparator

a.	Nominal Level	- 28 VDC ± 20%
b.	Trip Level	Loss of - 28 VDC
c.	Source Impedance	20K ohms - Block I 10K ohms - Block II and LEM
d.	Minimum input impedance	
e.	Circuit must latch and remain on even in the OIA ON mode. A reset button must be pressed to reset the circuit and remove the visual display	

Circuit
1. - 28 VDC Fail

3.3.7 2 V, 3200 cps Voltage/Frequency Comparator

a.	Nominal level	
	Voltage	2 V ± 1%
	Frequency	3200 cps ± 1 cps sine wave
b.	Trip level	
	Voltage	When voltage exceeds 2 V ± 10% for longer than 50 to 100 milliseconds

Frequency — 3168 ± 8 cps low or 3520 ± 35 cps high for longer than 50 to 100 milliseconds

c. Source impedance — approximately 20 ohms

d. Minimum Input Impedance

e. Circuit to be reset only after the failure is cleared and a momentary reset button depressed. This circuit in conjunction with the Test Control Panel shall cause the G & N to downmode from an ISS Operate Power mode to an ISS Standby Power mode if there is a ducosyn excitation malfunction.

3.3.8 Ducosyn Excitation Comparator Verification Tests - There shall be three verification tests. The normal inputs shall be removed and a test input with the following characteristics shall be switched to the comparator.

a. Low Frequency Test
   1. Test input - 2 V at 3160 to 3150 cps sine wave
   2. Switchover time less than 50 milliseconds.

b. High Frequency Test
   1. Test Input - 2 V at 3584 to 3680 cps sine wave
   2. Switchover time less than 50 milliseconds

c. Low Voltage Test
   1. Test input - 1.7 V ± .05 V, 3200 $^{+10\%}_{-1\%}$ cps
   2. Switchover time less than 50 milliseconds.

3.3.9 28 VDC G & N Power High-Low Sensor

a. Nominal Level — 28 (+2, -3) VDC

b. Trip Level — 32.5 ± .5 VDC high; 21.5 ± .5 VDC low

Trips if failure condition present for 20 to 40 milliseconds.

c. Circuit to be reset only after the failure is cleared and a momentary reset button is depressed.

3.3.10 28 VDC G & N Power Sensor Verification Tests - There shall be two G & N voltage verification tests. The normal input shall be removed and a test input with the following characteristics shall be switched to the sensor.

a. High Voltage Test
   1. Test input — 20% higher than nominal
   2. Switchover time less than 20 milliseconds

b. Low Voltage Test
   1. Test input — 20% lower than nominal
   2. Switchover time less than 20 milliseconds.

3.3.11 115 V, 60 cps 3-Phase High-Low Sensor

a. Nominal Level — 115 V, 60 cps

b. Trip Level — Less than 105 V or greater than 125 V, 60 cps

c. Circuit to be reset only after the failure is cleared and a momentary reset button is depressed.

3.3.12 115 V, 60 cps 3-Phase Sensor Verification Tests - There shall be three 115 V, 60 cps verification tests, one for each phase. These tests shall only exercise the low voltage sensor by switching out the normal input and switching in a test input of 90 ± 10% volts, 60 cps.

MONITOR PANEL INTERFACE
BLOCK I, SERIES 100, BLOCK II AND LEM

CROSS REFERENCE NO.	CONNECTOR PIN	NOMENCLATURE	SIGNAL DESCRIPTION
1	J1-FF or A	27 VDC RLP Lo or GSE Chassis Grd Bus	27 VDC RLP Lo or Chassis Grd
2	J1-B	GSE Shield Grd Bus	Shield Grd
3	J1-MM & PP	115 V, 60 cps Neutral	60 cps Neutral
161 TL	J3-W	Cos AMG 1X S3 (Hi)	0 to 26 V, 800 cps
162 TL	J3-X	Cos AMG 1X S1 (lo)	Cos AMG 1X Return
175 W	J3-LL	IMU Delay Light Hi	28 VDC Hi G & N
176 W	J3-MM	0 VDC IMU	0 VDC IMU
192	J3-h	800 cps, 28 V, 5% IMU Wheel PH A	28 V, 800 cps HI
194	J3-i	800 cps, 28 V, 5% IMU Wheel Lo	28 V, 800 cps Lo
275	J2-c	- 28 VDC	- 28 VDC
276	J2-d	0 VDC IMU	0 VDC IMU
374 W	J3-n	IMU FAIL RET	102.4 KC RETURN
375 W	J3-p	IMU FAIL HI	0 to 5 VPP, 102.4 KC Pulse Train
376 W	J2-y	CDU FAIL RET	102.4 KC Return
377 W	J2-z	CDU FAIL HI	0 to 5 VPP, 102.4 KC Pulse Train
378 W	J2-u	ACCEL FAIL RET	102.4 KC RETURN
379 W	J2-v	ACCEL FAIL HI	0 to 5 VPP 102.4KC Pulse Train
404	J2-BB	CMS 0 VDC	CMS 0 VDC
428 W	J3-v	IMU Temp Light (Main Panel)	27 VDC RLP Lo
429 W	J3-Y	Gimbal Lock Indication	27 VDC RLP Lo
430 W	J3-KK	G & N Error Light (Main Panel)	27 VDC RLP Lo
494	J1-EE	27 VDC RLP Hi	27 VDC RLP Hi Pil Pwr
536	J1-e	CLS Remote Alarm Control	27 VDC RLP Hi
537	J1-S	Coolant Supply Fail Lamp	27 VDC RLP Hi
587	J1-Z	27 VDC RLP Hi ISS Only	27 VDC RLP Hi
853	J1-p	Temp Normal Lo	60 cps Neutral
854 W	J1-r	60 cps TMC Conditioned	24 VAC, 60 cps Lo
855 W	J1-s	Temp Mon. Fail Ind. Enable	24 VAC, 60 cps Lo
896	J1-GG	115 V, 60 cps, PH A Pil. Pwr	115 V, 60 cps Hi
899	J2-AA	Remote Logic Pwr On	CMS 0 VDC
902	J2-S	27 VDC RLP Hi	27 VDC RLP Hi Pil Power
924	J1-C	Gimbal Dump Inhibit	27 VDC RLP Hi
925	J1-D	Ducosyn Exc. Mon. Inhibit Lamp Hi	27 VDC RLP Hi
926	J1-P	Gimbal Dump Interlock	27 VDC RLP Lo
927	J1-R	Gimbal Dump Indication	27 VDC RLP Hi
1374	J1-V	OIA ON Command	115 V, 60 cps, PH C
931	J1-a	G & N Power Modes Enable	27 VDC RLP Hi
932	J1-d	OIA ON G & N Pwr Normal	27 VDC RLP Hi

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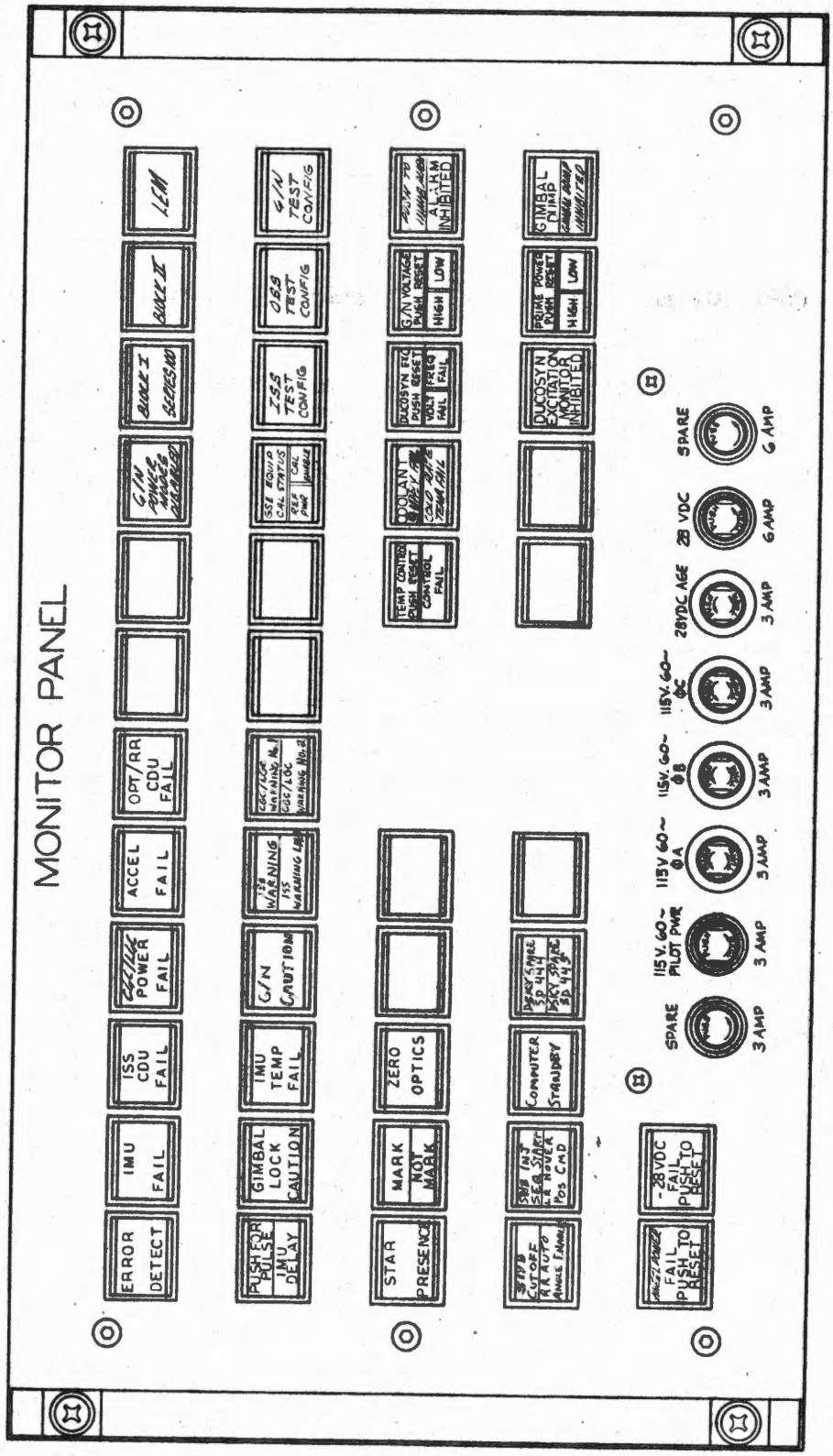
CROSS REFERENCE NO.	CONNECTOR & PIN	NOMENCLATURE	SIGNAL DESCRIPTION
1028	J1-g	Ducosyn Sensor Override	27 VDC RLP Hi Pil Pwr
935	J1-i	Test Start Light	27 VDC RLP Hi
936	J1-j	IMU Ducosyn Exc. Mon. Hi	2 V, 3200 cps Hi
937	J1-k	IMU Ducosyn Exc. Mon. Lo	2 V, 3200 cps Lo
938	J1-q	Temp Control Latch Reset	115 V, 60 cps Neutral
939	J1-t	CGC/LGC Power Fail Lo	27 VDC Lo
940	J1-u	Phase C Fail Test	27 VDC RLP Hi
941	J1-v	Phase B Fail Test	27 VDC RLP Hi
942	J1-w	Phase A Fail Test	27 VDC RLP Hi
943	J1-x	Ducosyn Fail Low Volt. Test	27 VDC RLP Hi
944	J1-y	Ducosyn Fail Hi Freq. Test	27 VDC RLP Hi
945	J1-z	Ducosyn Fail Low Freq. Test	27 VDC RLP Hi
946	J1-AA	G & N Power High Test	27 VDC RLP Hi
947	J1-BB	G & N Power Low Test	27 VDC RLP Hi
948	J1-JJ	Alarm Test Relay Low	27 VDC RLP Lo
743	J1-KK	27 VDC RLP Hi ISS Operate	27 VDC RLP Hi
950	J1-LL	115 V, 60 cps, PH B	115 V, 60 cps, Ph B
951	J1-MM	115 V, 60 cps, PH C	115 V, 60 cps, Ph C
952	J1-NN	115 V, 60 cps, Ph A	115 V, 60 cps, Ph A
954	J2-W	2 Sec. T.D. Latch	27 VDC RLP Hi Pil Pwr
955	J2-Z	Initiate 2 Sec. T.D.	27 VDC RLP Hi
957	J2-b	Wheel Run-Up Signal	27 VDC RLP Hi
958	J3-N	Fail Ind. G & N Hi	27 VDC RLP Hi
959	J3-P	Fail Ind. G & N Lo	27 VDC RLP Lo
960	J3-R	CTR IMU Delay Hi	27 VDC RLP Hi Pulse
961	J3-S	CTR IMU Delay Lo	27 VDC RLP Lo
1029	J3-t	Temp. Cont. Switchover Enable	27 VDC RLP Lo
1419 W	J3-NN	Star Presence Hi	0 to 5 VPP, 102.4 KC Pulse Train
1420 W	J3-PP	Star Presence Lo	102.4 KC Return
1423 TW	J3-AA	Optics Zero Encoder Indication	27 VDC RLP Hi (Optics Pwr)
1424 TW	J3-CC	Not Mark	27 VDC RLP Hi (Optics Pwr)
1425 TW	J3-EE	Mark	27 VDC RLP Hi (Optics Pwr)
1427	J1-CC	28 VDC G & N Power Hi	28 VDC G & N Pwr Hi
1428	J1-DD	28 VDC G & N Power Lo	28 VDC G & N Pwr Lo
1579 TL	J2-t	Block II and LEM Status Indication	27 VDC RLP Hi
1580	J2-DD	GSE Reference Power Selected	27 VDC RLP Lo
1633	J2-EE	G & N Test Config. Ind.	27 VDC RLP Lo
1634 TL	J3-q	IMU Fail	28 VDC G & N Pwr Hi (2K Buffer)
1635 TL	J2-x	CDU Fail	28 VDC G & N Pwr Hi (2K Buffer)
1636 TL	J2-w	Optics/RR CDU Fail	28 VDC G & N Pwr Hi (2K Buffer)

CROSS REFERENCE	CONNECTOR & PIN	NOMENCLATURE	SIGNAL DESCRIPTION
1637 TL	J3-u	Temp Within Limits	28 VDC G & N Pwr Hi (2K Buffer)
1638 T	J3-JJ	Star Acquired	27 VDC RLP Hi
1639 TL	J1-n	Coldplate Temp Normal	27 VDC RLP Hi
1640	J2-FF	ISS Test Config. Ind.	27 VDC RLP Lo
1641	J2-GG	Not ISS Test Config. Ind.	27 VDC RLP Lo
1642	J2-HH	OSS Test Config. Ind.	27 VDC RLP Lo
1643	J2-JJ	Not OSS Test Config. Ind.	27 VDC RLP Lo
1644	J2-KK	Block I, Series 100 Ind.	27 VDC RLP Lo
1645	J2-LL	Not Block I, Series 100 Ind.	27 VDC RLP Lo
1646	J2-MM	Block II Ind.	27 VDC RLP Lo
1647	J2-NN	Not Block II Ind.	27 VDC RLP Lo
1648 L	J2-PP	LEM Configuration Ind.	27 VDC RLP Lo
1400	J3-A	Remote No Temp Alarm Output	As Req'd at Lab Facility
1401	J3-B	Remote Temp Alarm Input	" " " " "
1402	J3-C	Remote Temp Alarm Output	" " " " "
1399	J3-D	Remote No Temp Alarm Output	" " " " "
1398	J3-E	Remote Temp. Alarm Common	" " " " "
1397	J3-F	Remote Temp Alarm Output	" " " " "
1656	J2-CC	GSE Calib Enabled Ind.	27 VDC RLP Lo
1657	J1-b	CGC/LGC Power Fail Hi	27 VDC RLP Hi
1689 TL	J1-m	TMC Reset	27 VDC RLP Hi Pil Pwr
1432	J2-X	Remote Single Print	DVM Pwr Grd
1433	J2-Y	DVM Power GRD	DVM Pwr Grd
968	J3-U	800 cps 0 Deg. ISS Ref Hi (Buffered)	28V, 800 cps Hi
969	J3-V	800 cps 0 Deg. ISS Ref Lo (Buffered)	28V, 800 cps Lo
1743	J3-G	Remote No Power Fail Output	As Required at Lab Facility
1744	J3-H	Remote Power Fail Output	As Required at Lab Facility
1745	J3-J	Remote Power Alarm Common	As Required at Lab Facility'
1826TL	J2-M*	G&N Caution Light	27 VDC RLP HI
1827TL	J2-J*	ISS Warning Light	27 VDC RLP HI
1828TL	J2-H*	CGC/LGC Warning No. 1	27 VDC RLP HI
1829TL	J2-I*	CGC/LGC Warning No. 2	27 VDC RLP HI
1830TL	J2-K*	ISS Warning LMP	27 VDC RLP HI
1831T	J2-P*	SIVB Cut OFF	27 VDC RLP HI
1832T	J2-R*	SIVB INJ Seq. Start	27 VDC RLP HI
1833L	J2-Q*	RR Auto Angle Enable	27 VDC RLP HI
1834L	J2-S*	LR Hover Pos. CMD.	27 VDC RLP HI
1835TL	J2-N*	Computer Standby	27 VDC RLP HI
1836TL	J2-F*	DSKY Spare SD444	27 VDC RLP HI
1837 TL	J2-G*	DSKY Spare SD445	27 VDC RLP HI



Approved:

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DG/sj